ZSSC4162D-01

Automotive Resistive Sensor Signal Conditioner with SENT Output

Description

The ZSSC4162D-01 is a member of Renesas' family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor element signals. Featuring a maximum analog pre-amplification up to 200, the ZSSC4162D-01 is configurable to nearly all resistive bridges.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity are accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4162D-01 nonvolatile memory (NVM), which is reliable in automotive applications.

The ZSSC4162D-01 supports use of an external diode, external RTD (PTC/NTC), or internal PTAT as a temperature reference.

Measured values are provided via a digital SENT interface. The SENT interface enables transmission of sensor data via its Fast Channel as well as transmission of supplementary data via its Serial Data Message (SDM) Channel (also referred to as the "slow" channel) using only one output pin. End-of-line calibration is also supported through this output pin via the ZACwire™ One-Wire Interface (OWI). The ZSSC4162D-01 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4162D-01 is optimized for automotive environments by over-voltage and reverse-polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Fluid brake pressure and temperature sensing (PV)
- Fuel pressure and temperature sensing
- Gas/air pressure and temperature sensing
- Hydraulic pressure and temperature sensing (e.g., steering systems with hydraulic steering support)
- Pneumatic pressure and temperature sensing (e.g., air brake systems, pneumatic shock absorbers)

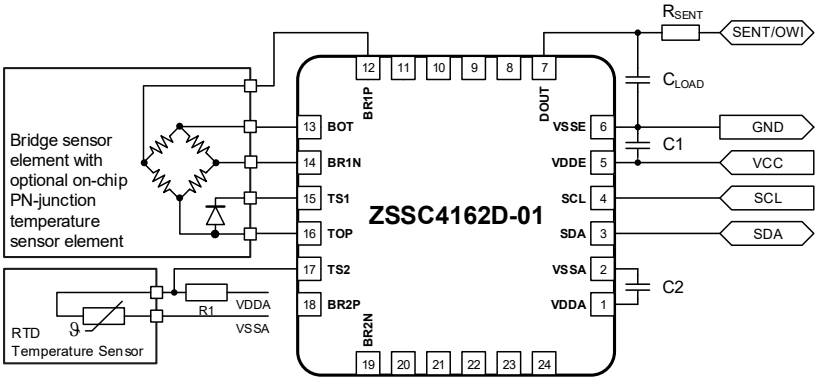
Available Support

- Evaluation Kit
- Application Notes
- Calculation Tools

Features

- One differential full-bridge sensor element measurement
- One internal chip temperature measurement
- One external diode temperature measurement
- One external RTD temperature measurement
- Digital compensation for offset, gain, and higher order nonlinearity as well as temperature coefficients of the differential sensor element input signal
- Operating temperature range: -40°C to 150°C
- Accuracy as high as ±0.50% full scale at -40°C to 150°C (see the electrical characteristics table for conditions)
- Outstanding accuracy for NTC: within ±1°C
- NVM memory for configuration, calibration data, and configurable measurement and conditioning functionality
- SENT output compliant to SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4) standard
- Supports output of one or more sensor signals and product identification via a single SENT interface connection
- Configurable for nearly all resistive bridge sensors
- One-pass, end-of-line calibration algorithm minimizes production costs
- No external trimming or components required
- Qualified according to AEC-Q100 Grade 0 standard
- Supply voltage: 4.75V to 5.25V
- Over-voltage and reverse-polarity protection up to ±18V
- Bridge sensor input span: 1mV/V to 800mV/V
- Bridge sensor signal ADC resolution: 14-bit to 18-bit
- Output resolution: 12-bit via SENT interface
- Package: 24-QFN (4 × 4 mm; wettable flanks)

ZSSC4162D-01 Basic Circuit



Contents

List of Figures

List of Tables

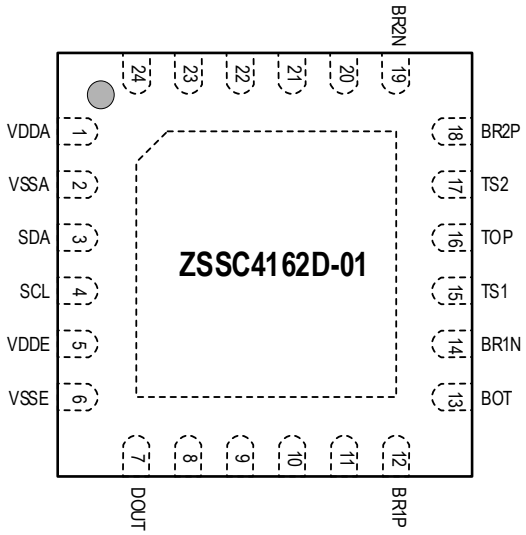
1. Pin Assignments

The ZSSC4162D-01 is available in a 24-QFN (4 × 4 mm; wettable flanks) RoHS-conformant package.

Note: The backside of the 24-QFN package (exposed pad; see section 14) is electrically connected to VSSA.

Recommendation: Solder the QFN exposed pad to the PCB, even if electrically redundant, to ensure adequate thermal performance and to reduce mechanical stress and solder joint failure risk.

Figure 1. Pin Assignments for 4 × 4 mm 24-QFN Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

24-QFN Pin #	Pin Name	Type	Description
1	VDDA	Supply	Internal supply [a]
2	VSSA	Supply	Internal ground
3	SDA	I/O	I2C data input/output (optional communication interface) [b],[c]
4	SCL	Input	I2C clock (optional communication interface) [b],[c]
5	VDDE	Supply	External supply
6	VSSE	Supply	External ground
7	DOUT	I/O	SENT output and One-Wire Interface (OWI) input/output
8 to 11	n.c.	–	No connection – unused
12	BR1P	Input	Positive bridge sensor input [d]
13	BOT	Supply	Negative bridge supply voltage
14	BR1N	Input	Negative bridge sensor input [d]
15	TS1	Input	External temperature sensor input 1
16	TOP	Input	Positive bridge supply voltage
17	TS2	Input	External temperature sensor input 2

24-QFN Pin #	Pin Name	Type	Description
18	BR2P	Input	Positive bridge sensor input 2 [d]
19	BR2N	Input	Negative bridge sensor input 2 [d]
20 to 24	n.c.	–	No connection – unused
–	EPAD	Supply	Internal ground; connected to VSSA [e]

[a] Do not supply VDDA externally.

[b] Internal pull-up.

[c] No connection required.

[d] Only one of the two sensor input options can be used: sensor input 1 (BR1P and BR1N) or sensor input 2 (BR2P and BR2N).

[e] Ground; can be shorted externally to VSSA (pin 2).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZSSC4162D-01 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.8 for information about over-voltage protection, reverse polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

Specification	Symbol	Parameter	Conditions	Min	Max	Unit
DS_001	V_{VDDE_ABS}	Supply voltage		-18	18	V
DS_002	V_{DOUT_ABS}	Voltage at the DOUT pin		-18	18	V
DS_003	V_{DIFF_ABS}	Pin voltage difference	Voltage between any two of these pins: VDDE, DOUT, and VSSE	-18	18	V
DS_004	V_{VDDA_ABS}	Analog supply voltage	On-chip controlled voltage; do not supply VDDA externally	-0.3	6	V
DS_005	V_{PIN_ABS}	Voltage at all other pins	Maximum voltage is V_{VDDA} + 0.3V	-0.3	6	V
DS_006	T_{J_ABS}	Junction temperature	Note: See section 7.8 regarding over-voltage protection	-40	160	°C
DS_007	T_{STOR_ABS}	Storage temperature		-55	155	°C

4. Operating Conditions

The operating conditions below specify the conditions that the application circuit must provide to the device during operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in section 5.

Table 3. Operating Conditions

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_009	V_{VDDE}	Supply voltage	VDDE to VSSE.	4.75	5	5.25	V
DS_010	V_{VDDE_EXTD}	Extended supply voltage [a]	VDDE to VSSE; derated accuracy as specified with DS_059.	4.5	5	5.5	V
DS_011	V_{VDDE_OP}	Operating supply voltage [a]	VDDE to VSSE; derated accuracy. Note for a supply greater than 5.5V: Above the ZSSC4162D-01 over-voltage limitation threshold, the output potential is clipped at this threshold.	4		6	V
DS_012	T_{AMB}	Ambient temperature [b], [c]	Temperature range.	-40		150	°C
Informational [d]	$R_{th\_JA\_QFN24}$	Thermal resistance 24-QFN [a]	According to JESD 51.		32		K/W
DS_185	R_{BR}	Bridge sensor resistance [a], [e]	One sensor bridge at pins BR1P and BR1N or BR2P and BR2N.	1		15	kΩ
	I_{VDDA}	VDDA current	Must be considered for bridge resistance and external temperature measurement options.			3.5	mA

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Temperature stress over lifetime is restricted to the Temperature Profile described in section 12 or to similar stress caused by equivalent temperature profiles. Contact Renesas for temperature stress calculation support.

[c] Assuming application conditions according to test board design as per JESD51-7 and natural convection test conditions as per JESD51-2.

[d] Package-related parameter.

[e] Symmetric behavior and identical electrical properties (especially the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

5. Electrical Characteristics

All parameter values are valid under the operating conditions specified in section 4 (unless otherwise stated). All parameters are valid for the ambient temperature range T_{AMB} and for the supply voltage range V_{VDDE} = 4.75V to 5.25V. Unless otherwise defined, the parameters are related to the ZSSC4162D-01 itself. All voltages are referenced to the VSSA pin.

The following parameters are specified based on a ZSSC4162D-01 main channel configuration setup using a PGA gain of 100 and assuming a resulting ADC input range usage of ≥ 50%FS. Further preconditions are an ADC resolution of 14 bits, an oscillator frequency of 8MHz (calibrated by Renesas in production), and an ADC clock frequency of 1MHz (1st step) / 2MHz (2nd step).

Table 4. Electrical Parameters

Note: See important table notes at the end of this table.

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.1 Supply Current and System Operating Conditions							
DS_015	I_S	Supply current	Excluding bridge sensor and RTD supply current; excluding output current at DOUT pin; oscillator adjusted to f_{OSC} = 8MHz		8	10	mA
DS_016	P_{OV}	Overvoltage power consumption [a]	5.5V < V_{VDDE} < 18V; excluding sensor and output load			300	mW
DS_017	$V_{OV\_LIM\_TH}$	Overvoltage limitation threshold [a]	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	5.55		18	V
DS_018	$V_{OV\_OFF\_TH}$	Over-voltage switch-off threshold [a]	The ZSSC4162D-01 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	7		12	V
DS_019	$t_{OV\_OFF\_DLY}$	Over-voltage switch-off delay [a]	The ZSSC4162D-01 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.		10	25	ms
DS_020	$I_{S\_OV\_OFF}$	Supply current limitation in the event of over-voltage switch-off [a]	Overvoltage switch-off is activated if the supply voltage exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$. V_{VDDE} < 18V; excluding sensor and output load.			10	mA
DS_178	V_{DDA}	Analog supply voltage	V_{DDA} is limited if V_{DDE} exceeds the threshold $V_{OV\_OFF\_TH}$.	0.9		1.0	V_{DDE}
DS_021	V_{SENS}	Bridge sensor supply voltage	$V_{SENS} = V_{TOP} – V_{BOT}$ at $R_{BR} \geq 1k\Omega$ where V_{TOP} is the voltage at the TOP pin and V_{BOT} is the voltage at BOT pin.	0.9		1.0	V_{VDDA}

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_022	V_{POR_OFF}	Power-on reset off-threshold	V_{VDDA} measured referenced to VSSA; POR is active until V_{VDDA} exceeds this threshold.	3.3		3.8	V
DS_023	V_{POR_ON}	Power-on reset on-threshold	V_{VDDA} measured referenced to VSSA; POR is activated if V_{VDDA} falls below this threshold.	3.0		3.6	V
DS_024	V_{POR_HYST}	Power-on reset hysteresis [a]	$V_{POR\_ON} – V_{POR\_OFF}$		0.4		V
DS_025	f_{OSC}	Oscillator frequency	Calibrated oscillator frequency.	7.6	8	8.6	MHz
DS_026	TC_{OSC}	Oscillator frequency temperature coefficient [a]		-200		200	ppm/K
5.2 Analog Front-End Characteristics							
DS_027	V_{IN_SPAN}	Differential input span	Analog gain: 1 to 200	1		800	mV/V
DS_028	$V_{IN\_RNG\_1}$	Input voltage range	Analog gain = 1 Corresponds to V_{ADC_IN}	0.05		0.95	V_{SENS}
DS_029	$V_{IN\_RNG\_2}$		Analog gain = 2 to 200	0.3		0.65	V_{SENS}
DS_030	C_{IN}	Capacitance at input [a]	Capacitance at pins BR1P and BR1N or BR2P and BR2N to VSSA; requirement for timing parameters	0		12	nF
5.3 A/D Conversion Refer to section 7.2.4.							
DS_034	DNL_{ADC}	DNL [a]				0.95	LSB
DS_035	INL_{ADC}	INL	Best fit		3	8	LSB_{14}
5.4 Differential Bridge Sensor Measurement (Refer to section 7.4.1)							
Informational		ADC resolution [a]		14		18	Bit
DS_033	V_{ADC_IN}	ADC input range [a]	Differential input signal range depending on analog gain a_{PGA} and ADC range shift rs_{ADC}: $V_{ADC\_IN} = V_{IN} \times a_{PGA} + rs_{ADC} \times V_{SENS}$ rs_{ADC} = [0.0625, 0.125, 0.25, 0.5]	0.05		0.95	V_{SENS}
			Restriction for analog gain > 100.	0.1		0.9	V_{SENS}
DS_043	R_{BRSC_TH}	Sensor connection loss detection threshold	Fault check BRSC: Sensor pin to ZSSC4162D-01 pin connection; without capacitive load at pins BR1P and BR1N in the event of a connection loss.	20		240	kΩ
DS_044	R_{BRSS_TH}	Sensor short detection threshold[a]	Fault check BRSS: Sensor input pin BRxN to input pin BRxP.	50		800	Ω

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_056	OUR	Output update rate [a]	Internal output update of differential bridge measurement; asynchronous to SENT transmission.			1	ms
DS_057	ORT	Output response time [a]	100% input step of differential bridge measurement [d].			3.5	ms
DS_059	F_{ALL_BR}	Overall failure Deviation from ideal line including INL, gain, offset, and temperature impacts; excluding sensor-caused effects	Differential sensor readout V_{VDDE} = 4.75V to 5.25V			0.5	%FS
	$F_{ALL\_BR\_EXTD}$ [a]		Differential sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V			1.0	%FS
	$F_{ALL\_DERATED}$ [a]		In the operating supply voltage range V_{VDDE_OP}.			5	%FS
DS_058	RE	Ratiometricity error	Maximum error for V_{VDDE} from 5V to 4.75V or to 5.25V. Ratiometricity error is already contained in overall failure (DS_059).			500	ppm
5.5 Internal Temperature Measurement Refer to section 7.4.2.							
Informational		ADC resolution [a]		13		13	Bit
Informational		Output update rate [a]	Internal output update of measurement; asynchronous to SENT transmission.		8	10	ms
Informational		Output response time [a]	100% input step of measurement [d].			25	ms
DS_036	ST_{TSI}	Internal temperature PTAT sensitivity	Raw values, without conditioning calculation; analog gain = 12.6.	20			LSB_{14} /K
5.6 External Diode Temperature Measurement Refer to section 7.4.3							
Informational		ADC resolution [a]		13		13	Bit
Informational		Output update rate [a]	Internal output update of measurement, asynchronous to SENT transmission		8	10	ms
Informational		Output response time [a]	100% input step of measurement [d]			25	ms
Informational	OPR_{TS}	Temperature sensor range [a]	Important: This range exceeds the operating conditions for T_{AMB}.	-60		200	°C
DS_037	A_{TSE_D}	External temperature diode channel gain		10			LSB_{14} /mV
DS_038	I_{TSE_D}	External temperature diode bias current		10	20	40	µA
DS_039	V_{TSE_D}	External temperature diode input range [a]	Related to V_{TOP}, absolute measurement	-1		-0.2	V

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.7 External RTD Temperature Measurement Refer to section 7.4.4.							
Informational		ADC resolution [a]			14		Bit
DS_171	V_{RTD_IN}	Input voltage range on TSx pin		0.02		0.98	V_{DDA}
DS_172	I_{RTD_SUP}	Supply current	RTD connected on VDDA and VSSA.			3.5	mA
DS_174	F_{RTD_MEAS}	Analog measurement failure				0.15	%FSR
DS_175	OUR_{RTD}	Output update rate [a]	Internal output update of RTD measurement.			10	ms
DS_176	ORT_{RTD}	Output response time [a]	100% input step of RTD measurement[d]			25	ms
5.8 NTC Temperature Measurement Refer to section 7.4.4							
Informational		NTC temperature range		-55		200	°C
DS_177	F_{NTC_MATH}	NTC conditioning failure	2500 < β < 4600			0.1	%FSR
5.9 SENT Output Refer to SAE J2716 Specification JAN2010 (Rev.3) and APR2016 (Rev. 4) for detailed specifications for the SENT Physical and Software Layer.							
DS_048	t_{TICK}	Tick time [a]	Adjustment step = 1µs	3		90	µs
DS_049	t_{TICK_JITTER}	Tick time jitter [a], [c]	Valid for tick time ≤ 10µs, 6-sigma value			300	ns
DS_050	n_{SDM}	Number of SDMs	Absolute count of different messages	0		32	
DS_051	n_{SDM_CYC}	Number of SDM in SDM cycle	Message count in SDM cycle, including use of different priority levels.	0		64	
DS_052	n_{SDM_PRIO}	SDM transmission priority levels		1		3	
DS_053	t_{PAUSE}	Pause length	Fixed frame length.	12		768	t_{TICK}
DS_054	t_{FRAME}	Frame length	Pause pulse disabled, 6 data nibbles, and variable frame length.	154		270	t_{TICK}
			Pause pulse enabled, 6 data nibbles, and fixed frame length.	282		922	t_{TICK}

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.10 System Response							
DS_046	DTI	Diagnostic testing interval[a]				10	ms
DS_047	FMT	Fault messaging time [a]	t_{TICK} = 3µs, SENT pause pulse enabled, and the SENT frame length is set to the minimum.			25	ms
DS_055	$t_{STARTUP}$	Startup time [a]	Time to first valid output after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz[d]			10	ms

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] The temperature sensor range is the calibration target for the SENT output of the SDM temperature channels. This target can be adjusted.

[c] Compliant to SENT – Rev. 4.0. Sent – Rev. 3.0 specifies a maximum jitter of 50ns at tick time = 3µs and maximum jitter of 250ns at tick time = 10µs.

[d] t_{TICK} = 3µs, transmission on SENT Fast Channel, SENT pause pulse enabled, and the SENT frame length is set to the minimum.

6. Interface Characteristics and Nonvolatile Memory

Table 5. Interface Characteristics and Nonvolatile Memory

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6.1 ZACwire™ One-Wire Interface One-wire communication at the DOUT pin.							
DS_060	t_{PWRUP}	Power-on time [a]	Time to ready for communication after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz.			3.0	ms
DS_061	$t_{OWI\_STARTWIN}$	Start window [a]	OWI can be enabled within a 5ms (maximum) window after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz.		250		ms
DS_062	$V_{OWI\_IN\_H}$	OWI voltage level HIGH [a]	Master to slave.	0.80			V_{VDDE}
DS_063	$V_{OWI\_IN\_L}$	OWI voltage level LOW [a]	Master to slave.			0.20	V_{VDDE}
DS_064	$V_{OWI\_OUT\_L}$	Slave output level LOW	Open drain; I_{OL} < 2mA.			0.1	V_{VDDE}
6.2 Selected I2C Interface Parameters The I2C interface complies with the *I2C Bus Specification, Version 6.0, April 4, 2014.*							
Informational	f_{SCL}	SCL clock frequency		0		400	kHz
Informational	$V_{I2C\_IN\_IL}$	Input LOW-level voltage		-0.5	-	$0.15V_{DDA}$ [c]	V
Informational	$V_{I2C\_IN\_IH}$	Input HIGH-level voltage		0.7 V_{DD}	-	V_{DDA}+0.5V	V
Informational	V_{OL}	Output LOW-level voltage	(Open-drain or open-collector) at 3mA sink current; V_{DDE} = 5V.	0	-	0.4	V
Informational	R_{I2C}	Internal pull-up resistor		25		100	kΩ
6.3 Nonvolatile Memory							
DS_065	T_{AMB_NVM}	Ambient temperature for NVM programming [b]		-40		125	°C
DS_066	N_{NVM_PAGE}	NVM page count [a]	Pages available for writing	22			
DS_067	t_{NVM_RET}	Data retention [a]	Temperature profile. [d]	15			years
DS_068.1	$t_{NVM\_WRI\_DIFF}$	Programming time without soaking [a]	Per programmed data word in differential mode.			1.7	ms
DS_068.2	$t_{NVM\_WRI\_RED}$		Per programmed data word in redundant mode.			3.3	

[a] No measurement in volume production; parameter is guaranteed by design and/or quality observation.

[b] Take into consideration additional package and temperature range restrictions.

[c] Different from the referenced I2C-bus specification.

[d] Over lifetime and valid for the dice. Note that the package can cause additional restrictions.

7. Circuit Description

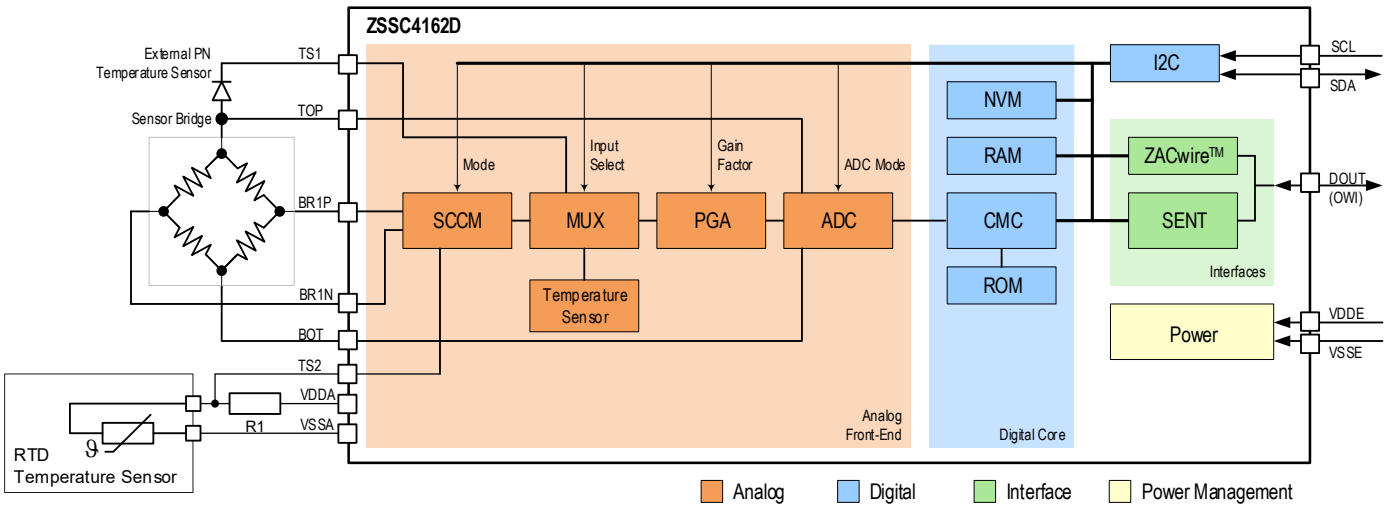
7.1 General Operation Description

The ZSSC4162D-01 is a sensor signal conditioner for readout of resistive bridge sensors. The sensor signal is pre-amplified and converted to a digital signal by the analog-to-digital-converter (ADC). Then the digital conversion result is offset compensated and gain adjusted. Temperature coefficients and nonlinearity of the sensing element are compensated, if necessary. Then the calculated conditioning result is output using the SENT protocol.

Signal conditioning processes the following tasks:

- Measurement of the voltage signal of the connected resistive sensing element
- Measurement of temperature
- Conditioning calculation for the sensor signal
- SENT output of the conditioning result

Figure 2. Block Diagram



SCCM	Sensor Check and Common Mode Adjustment Unit
MUX	Multiplexer
PGA	Programmable Gain Amplifier
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
ROM	Read-Only Memory for Correction Formula and Algorithm
NVM	Nonvolatile Memory for Configuration and Conditioning Coefficients
RAM	Volatile Memory for Configuration and Conditioning Coefficients
SENT	SENT Controller and SENT Physical Layer Output Stage
ZACwire™	Digital One-Wire Interface
I2C	I2C Digital Interface
Power	Power Management and Protection Unit

7.2 Analog Front-End

The analog front-end (AFE) consists of the sensor connection check module (SCCM), the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation. An internal PTAT is used to measure the die temperature.

7.2.1 SCCM

The sensor check and common mode block (SCCM) implements the self-diagnostic features for the analog front-end. The SCCM provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions.

7.2.2 Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path allowing the use of a single ADC. It allows a very flexible signal routing between the sensors and the ZSSC4162D.

7.2.3 Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. Alternatively, the PGA can be bypassed and the sensor signal can be input directly to the ADC. The gain is adjustable for the bridge measurement task in order to provide an ADC input signal span of greater than 50% FS.

Table 6 shows the adjustable gains of the PGA, the corresponding signal spans, and the common mode range limits.

Table 6. Adjustable PGA Gains and Resulting Sensor Signal Spans and Common Mode Ranges

Nominal PGA Gain a_{PGA}	Maximum Input Span V_{IN_SPAN} [mV/V]	Input Common Mode Range V_{IN_CM} [% V_{VDDA}]
PGA bypassed	800	5 to 95
2.08	385	30 to 65
3.15	254	30 to 65
4.31	186	30 to 65
6.25	128	30 to 65
8.31	96	30 to 65
12.6	63	30 to 65
17.3	46	30 to 65
25.0	32	30 to 65
33.2	24	30 to 65
50.4	16	30 to 65
69.0	12	30 to 65
100.0	8	30 to 65
138.0	6	30 to 65
200.0	4	30 to 65

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

7.2.4 Analog-to-Digital Converter

The analog-to-digital converter (ADC) is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC allows adjusting the A/D conversion input voltage range shift.

7.3 Signal Conditioning

7.3.1 Internal Temperature Sensor Signal Conditioning

The internal temperature sensor signal conditioning is processed every time that a new measurement result value *T_int* is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset and gain and of the nonlinearity.

$$tsi\_comp = 2^{-40} * 2^{w_{tsi\_2}} * c_{tsi\_2} * T\_int^2 + 2^{-25} * 2^{w_{tsi\_1}} * c_{tsi\_1} * T\_int + 2^{-9} * 2^{w_{tsi\_0}} * c_{tsi\_0} \quad (1)$$

The conditioning coefficients c_{tsi_i} are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_{tsi_i} are unsigned 4-bit values (uint4).

The normalized conditioning result of the internal temperature sensor *tsi_comp* is stored as a signed 16-bit value (sint16, two's complement) in the RAM output memory. This value can be assigned to a SENT SDM output channel and can be selected as *ts_comp* for the conditioning calculation of the full-bridge sensor signal.

7.3.2 External Temperature Sensor Signal Conditioning

The external RTD temperature sensor signal conditioning provides two paths that are processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset and gain and of the nonlinearity.

The first path provides a polynomial conditioning which is intended for PTC sensors. The transfer function of the conditioning output with input from the measurement is as follows:

$$Output = 2^{w_2-40} c_2 * Input^2 + 2^{w_1-25} c_1 * Input^1 + 2^{w_0-9} c_0 \quad (2)$$

The conditioning coefficients c_i are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_i are unsigned 4-bit values (uint4).

The second path is a spline function that is optimized for NTC sensors. The default NTC characteristic that is calibrated is given in Table 7. The coefficients must be calculated for every NTC – RTD once. It can be selected which conditioning result of both paths is stored as a signed 16-bit value (sint16, two's complement) in the RAM Output Memory. This value can be assigned to a SENT FC or SDM output.

$$Input = Z \qquad Z \in [0; 2^{15}) \quad (3)$$

$$x = (ld(Input) - ld(2^{15} - \text{Input})) * 2^{11} \qquad Input \in [1; 2^{15}] \quad (4)$$

3rd order spline:

$$s_{j(x)} = \underbrace{2^{-56} * 2^{w_{j3}} * c_{j3} * x^3 + 2^{-41} * 2^{w_{j2}} * c_{j2} * x^2 + 2^{-25} * 2^{w_{j1}} * c_{j1} * x + 2^{-9} * 2^{w_{j0}} * c_{j0}}_{\text{SPLINEWGTN Spline}} \quad s_{j(x)} \in \left[-2^{15}; 2^{15}\right) \tag{5}$$

$$Output = \frac{s_{j(x)} + offset}{2} * \frac{2^{15}}{gain} \quad Output \in \left[-2^{15}; 2^{15}\right) \tag{6}$$

j (Spline Segment)	*x* (Polynomial Input Range)	Spline Segment Boarder Recommendation
0	$x < x_0$	x_0 = Z(80°C) x_1 = Z(0°C)
1	$x_0 \leq x < x_1$	
2	$x \geq x_1$	

Table 7. NTC Mathematic Coefficients

Calibration Coefficient Name	Range	Formulaic Character	Description
CoeffCal4Offset	$[-2^{15}; 2^{15})$	*offset*	Supports 1 or 2 point calibration in production.
CoeffCal4Gain	$[-2^{15}; 2^{15})$	*gain*	
CoeffCal4Spline1	[0; 15]	w_{03}; w_{02}; w_{01}; w_{00}	Spline coefficients and weights. Calculated for an external resistor network and NTC characteristic.
CoeffCal4Spline2	$[-2^{15}; 2^{15})$	c_{03}	
CoeffCal4Spline3	$[-2^{15}; 2^{15})$	c_{02}	
CoeffCal4Spline4	$[-2^{15}; 2^{15})$	c_{01}	
CoeffCal4Spline5	$[-2^{15}; 2^{15})$	c_{00}	
CoeffCal4Spline6	$[0; 2^{15})$	x_0	
CoeffCal4Spline7	[0; 15]	w_{13}; w_{12}; w_{11}; w_{10}	
CoeffCal4Spline8	$[-2^{15}; 2^{15})$	c_{13}	
CoeffCal4Spline9	$[-2^{15}; 2^{15})$	c_{12}	
CoeffCal4Spline10	$[-2^{15}; 2^{15})$	c_{11}	
CoeffCal4Spline11	$[-2^{15}; 2^{15})$	c_{10}	
CoeffCal4Spline12	$[0; 2^{15})$	x_1	
CoeffCal4Spline13	[0; 15]	w_{23}; w_{22}; w_{21}; w_{20}	
CoeffCal4Spline14	$[-2^{15}; 2^{15})$	c_{23}	
CoeffCal4Spline15	$[-2^{15}; 2^{15})$	c_{22}	
CoeffCal4Spline16	$[-2^{15}; 2^{15})$	c_{21}	
CoeffCal4Spline17	$[-2^{15}; 2^{15})$	c_{20}	

7.3.3 Full Bridge Sensor Signal Conditioning

The full-bridge sensor signal conditioning is processed every time that a new measurement result value *br* is available from the analog-to-digital conversion. The conditioning calculation provides compensation of the temperature dependent offset and gain and of the nonlinearity.

Temperature dependent offset calculation up to 2nd order using temperature value *ts_comp from Bridge1 Temp. Mux*:

$$br\_offset = 2^{-40} * 2^{w_{o2}} * c_{o2} * ts\_comp^2 + 2^{-25} * 2^{w_{o1}} * c_{o1} * ts\_comp + 2^{-9} * 2^{w_{o0}} * c_{o0} \quad (7)$$

Temperature dependent gain calculation up to 2nd order using conditioned temperature value *ts_comp*:

$$br\_gain = 2^{-40} * 2^{w_{g2}} * c_{g2} * ts\_comp^2 + 2^{-25} * 2^{w_{g1}} * c_{g1} * ts\_comp + 2^{-9} * 2^{w_{g0}} * c_{g0} \quad (8)$$

Offset and gain compensation of the bridge sensor signal *br*:

$$Y = 2^{14} * (br + br\_offset) * br\_gain^{-1} \quad (9)$$

Nonlinearity compensation up to 3rd order:

$$br\_comp = 2^{-56} * 2^{w_{l3}} * c_{l3} * Y^3 + 2^{-41} * 2^{w_{l2}} * c_{l2} * Y^2 + 2^{-25} * 2^{w_{l1}} * c_{l1} * Y + 2^{w_{l0}} * c_{l0} * 2^{-9} \quad (10)$$

The conditioning coefficients c_{oi}, c_{gi} and c_{li} are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_{oi}, w_{gi} and w_{li} are unsigned 4-bit values (uint4).

All intermediate results and the final conditioning results *br_comp* for the full-bridge sensor are stored as signed 16-bit values (sint16, two's complement) in the RAM output memory. These values can be low-pass filtered and can be assigned to SENT Fast output channels.

7.3.4 Conditioning Cycle

The conditioning cycle is the sequence of equations and supervision functions processed during the Normal Operation Mode (NOM). It uses raw measurement results from the measurement cycle and delivers conditioned data for output.

7.3.5 Digital Interface

The ZSSC4162D-01 provides a digital interface for the calibration. The I2C controller and physical layer for I2C transmission complies with the *I2C Bus Specification, Rev.6 – April 4, 2014*.

The ZSSC4162D-01 supports the following bus selection.

Bidirectional bus options:

- Standard Mode (Sm), which has a bit rate up to 100kbit/s
- Fast Mode (Fm), which has a bit rate up to 400kbit/s

7.4 Signal Path

The ZSSC4162D-01 signal path consists of the analog front-end (AFE), the digital signal processing unit, the SENT controller, and the SENT physical interface (SENT PHY). In addition, this is supported by the ZACwire™ serial digital one-wire interface (OWI).

Table 8. Requirements – Main Signal Path Polarity

Specification	Parameter	Description
DP_040	Main signal path polarity	The resistive bridge sensor element signal is input via the BR1P and BR1N or BR2P and BR2N pins and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{VDDA}/2$) so that it is possible to process positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the analog-to-digital converter (ADC).

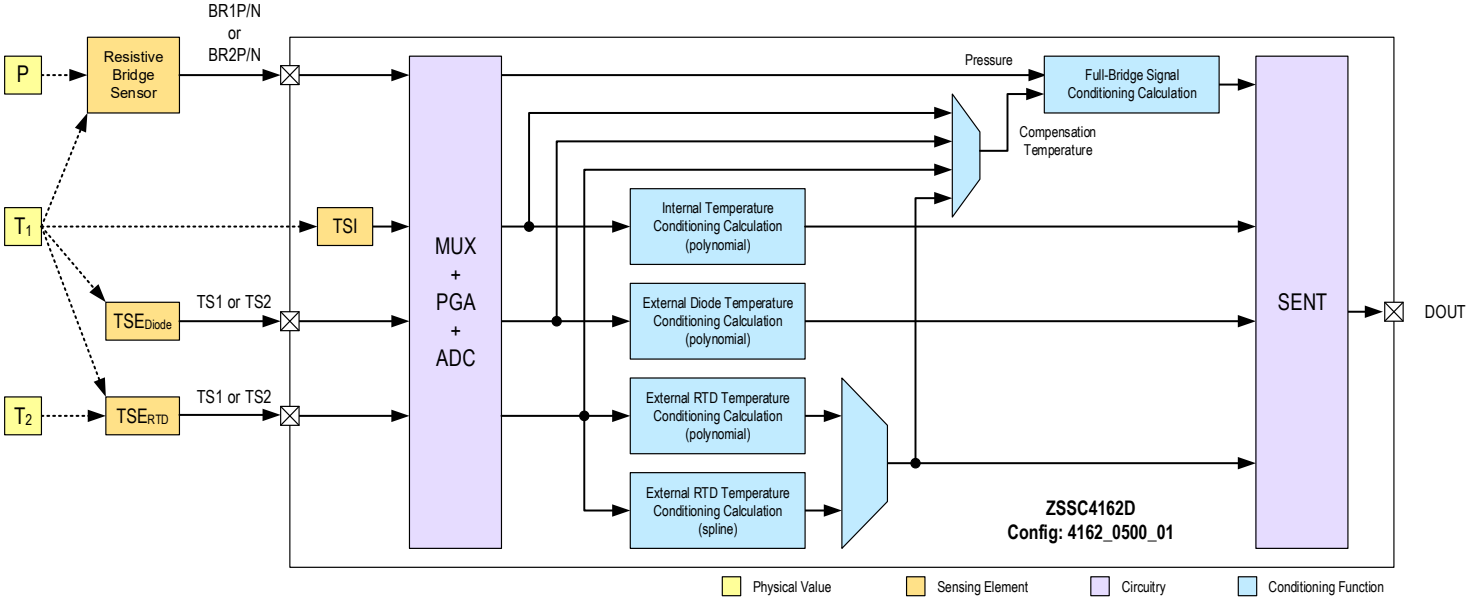
A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensors can either be an external diode or an internal proportional-to-absolute-temperature (PTAT) source as selected by NVM configuration.

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the DOUT pin.

During the calibration process, raw measurement values can be requested via the digital interfaces.

The ZSSC4162D-01 provides SENT transmission according to the *SAE J2716 SENT Specification*. Depending on the programmed configuration, there are several SENT output modes. These modes include assignment of the various sensor signals to the SENT Fast and Serial Data Message (SDM) communication channels as well as the configuration of the SENT frame itself.

Figure 3. Main Signal Path



7.4.1 Full-Bridge Sensor Measurement

The ZSSC4162D-01 measures a differential sensor signal (BR1P to BR1N or BR2P to BR2N); i.e. a bridge or voltage source type signal. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to (V_{TOP} – V_{BOT}).

The following parameter settings can be selected by the user.

- Gain: 2.1 to 200
- Range shift: 1/16, 1/8, 1/4, or 1/2
- Input multiplexer: BR1P/BR1N, BR1N/BR1P, BR2P/BR2N, or BR2N/BR2P
- Measurement resolution: 14 bits, 15 bits, 16 bits, 17 bits, or 18 bits

7.4.2 Internal Temperature Measurement

The ZSSC4162D-01 supports temperature measurement by the ZSSC4162D-01's internal PTAT sensor.

7.4.3 External Diode Temperature Measurement

Following parameters are selectable:

- Input multiplexer: TS1 or TS2

7.4.4 External RTD Temperature Measurement

A ratiometric measurement is implemented using VDDA and VSSA as the internal reference voltage. For every measurement result, an automatic offset compensation is performed.

In the case of an NTC sensor, it is recommended to use the value of R_{25} as the pull-up resistor. The temperature measurement error must be calculated from the sum of the failures F_{NTC_MATH}, F_{RTD_MEAS}, and F_{NTC_Sensor}. As the sensor sensitivity might change over the temperature measurement range, F_{NTC_Sensor} might also change and typically increases on the temperature corners.

Following parameters are selectable:

- Input multiplexer: TS1 or TS2
- Gain: 1.0 to 200

7.5 SENT Output

7.5.1 Overview

ZSSC4162D-01 provides three different digital interfaces for the output of data and status messages:

- The SENT controller and physical layer for SENT transmission enable readout of conditioned sensor data in compliance with SAE J2716 JAN2010 and SAE J2716 APR2016.
- The ZACwire™ interface for one-wire communication supports the sensor configuration and manufacturing process.
- The I2C interface supports the sensor configuration and manufacturing process.

The SENT interface is the main application output interface. The configuration of the SENT frame format and the assignment of signals and fault messages to the SENT output channels are configurable.

In addition to other protocols, the SENT interface supports the application-specific SENT protocols High Temperature Sensor (T or T/t), Single High Temperature Secure Sensor (T/S or T/S/t) and High Temperature / High Temperature Sensor (T1/T2 or T1/T2/t).

Table 9. Requirements – SENT Output Protocol

No.	Parameter
DP_017	SENT High Temperature Sensor T and T/t protocol
DP_018	SENT High Temperature Secure Sensor T/S and T/S/t protocol
DP_019	SENT High Temperature / High Temperature Sensor T1/T1 and T1/T2/t protocol

7.5.2 SENT Fast Channel Modes and Frame Format

The ZSSC4162D-01 SENT interface supports various frame configurations:

- SENT Fast Channel Mode: one or two Fast data channels.
- SENT Transmission Mode: fixed SENT frame length and adjustable pause pulse, or SENT transmission without pause pulse.

The ZSSC4162D-01 provides the following different Fast data channel modes:

- 12-bit FC1 (3 nibbles) (H.2 *)
- 12-bit FC1 and 12-bit FC2 (6 nibbles) (H.1 *)
- 12-bit FC1, 8-bit rolling counter and 4-bit zero (6 nibbles) (H.5 *)
- 12-bit FC1, 8-bit rolling counter and 4-bit MSN of FC1 inverted (6 nibbles) (H.4 *)

The SENT frame transmission is not synchronized to the ZSSC4162D-01 internal output data update. The internal output data update is determined by the fixed ADC resolution for the sensor element signal measurements and supervision function measurements. The output update rate and the SENT frame length are generally different. Depending on the SENT frame length used, it is possible that individual data is either sent twice or it is skipped and not sent at all. After power-on, the initial output values of the SENT Fast data channels are defined by the selected SENT output mode as described in section 7.5.4.

Table 10. Requirements – SENT Fast Channel Modes and Frame Format

No.	Parameter	Value
DP_020	Fast channel modes	4
DP_021	Fast channel 1 data	Bridge / RTD
DP_022	Fast channel 2 data	Bridge / RTD

* According to SAE J2716 SENT specification APR2016 (Rev. 4.0) because JAN2010 does not provide Appendix H “SENT data frame formats”.

7.5.3 SENT SDM Channel Modes

The ZSSC4162D-01 SENT interface supports up to 32 different serial data messages (SDM) transmitted in the SDM data channels. The SDM format, the number of SDMs, and the transmission priority are configurable as illustrated in the examples given in Table 11 and Figure 4.

- Enhanced SDM format with up to 32 SDMs.
- Mode with no SDM available (SDM bits in the status nibble are set to “0”).
- Configurable SDM IDs.
- Three priority levels; configurable sequence of SDMs per priority level.

Also see section 8.2 regarding fault messaging using the SDM Channel. For programming instructions and descriptions of the fields used during configuration, refer to the *Configuration Description Report* (CDR) included with the product delivery or available on request (see contact information on last page).

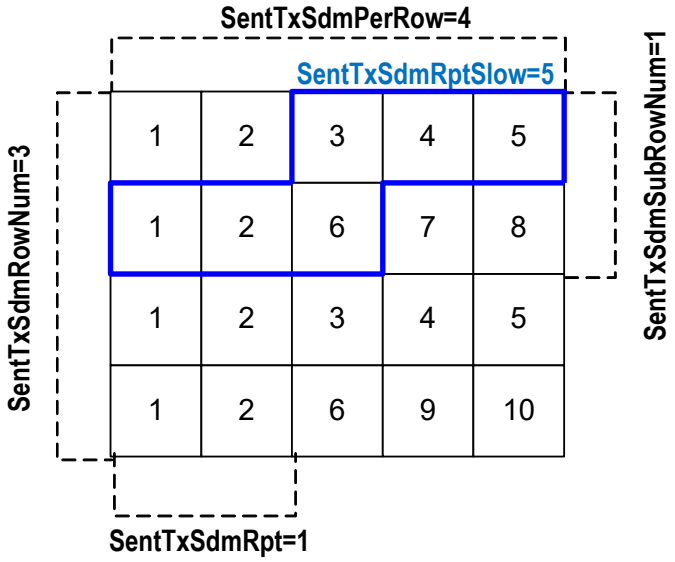
Table 11. Example of SDM ID Priority Level and Sequence Configuration

Priority Level	SDM ID			
1	1	2		
2	3	4	5	6
3	7	8	9	10

Configuration via Field	Value
SentTxSdmRpt	1
SentTxSdmRowNum	3
SentTxSdmPerRow	4
SentTxSdmRptSlow	5
SentTxSdmSubRowNum	1

Figure 4. SDM Cycle Example

Note: The **blue** line indicates the number of second-priority SDMs that are repeated in a cycle (adjusted by *SentTxSdmRptSlow*).



7.5.4 SENT Output Operation Modes

The ZSSC4162D-01 provides SENT output of the conditioned sensor element measurement results at the DOUT pin. This pin is also connected to the ZACwire™ interface for “End of Line” communication using a one-wire communication protocol (OWI).

There are four different modes for starting the OWI communication in combination with the SENT output:

After Initialization:

- SENT transmission starts immediately after the initialization phase.
- During the initialization, the DOUT pin is set to the output idle state.
- SENT data channels are set to their initial value (usually “0”) until the first valid conditioned differential bridge values are available.
- OWI Rx is enabled in parallel with the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting Command Mode (CM) during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

After the First Measurement:

- SENT transmission starts after the first measurement and conditioning cycle and thus with the first valid conditioned bridge values.
- During the initialization and the first cycle, the DOUT pin is set to the output idle state.
- SENT data channels start transmission with valid values.
- This mode allows the fastest possible transmission of the first conditioned bridge data after power on.
- OWI Rx is enabled in parallel with the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting CM during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

After 250ms:

- SENT transmission starts only after a time window (about 250ms); the DOUT pin is set to the output idle state.
- DOUT is weakly pulled to VDDA (pull-up current: ~2.5µA). OWI Rx is enabled for a specified time window.
- OWI communication can be started by transmitting the command for starting CM during this time window.

Disable SENT:

- SENT transmission is disabled. OWI Rx/Tx is enabled without time limitation. OWI communication can be started by transmitting the command for starting CM.

All fault checks are processed in the initialization phase before calculating the first conditioned bridge signal. In the event of a detected failure and when no fault filtering is activated, the transmission starts with transmitting a fault code instead of transmitting invalid bridge data (different from initialization value “0”) via the SENT interface in all SENT modes.

The output idle state of the ZSSC4162D-01 is defined as follows:

- The DOUT pin is switched to high impedance; DOUT is weakly pulled to VDDA (pull-up current: ~2.5µA).
- The final resulting potential at the output is defined by the (pull-up) load resistor at the SENT communication line.

Table 12. Requirements – SENT Output Operation Modes and Initialization Behavior

No.	Parameter	Value	Unit
DS_079	Number of SENT output operation modes	4	–

7.5.5 SENT Pulse Shaping

The ZSSC4162D-01 has several fixed adjustment options optimized for rise and fall times depending on the SENT tick time. This helps to get optimal EMC performance regarding electromagnetic emission.

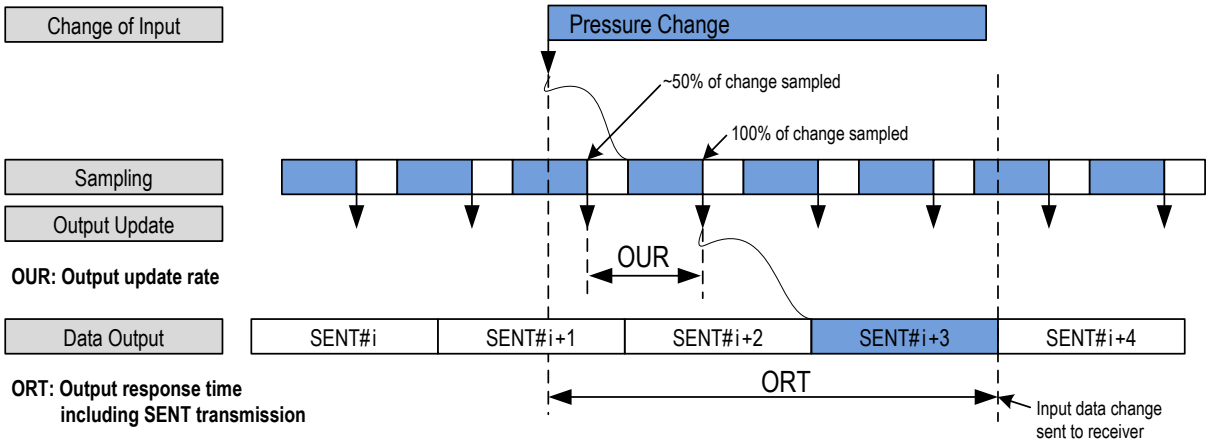
7.6 Timing Definitions

The timing for the update of the SENT output and for the fault messaging is defined in Figure 5. The relevant timing parameters are listed in Table 13.

Table 13. Timing Parameter

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the SENT transmission of this signal event

Figure 5. Output Update Timing Diagram



7.7 NVM OEM Data Memory

The ZSSC4162D-01 provides a NVM memory area for the storage of OEM data, which is physically part of the one-time programmable (OTP) NVM memory module, but it is delimited from the configuration and calibration data by dedicated commands for READ and WRITE access. Data protection and multiple-time programming data management must be implemented by the OEM.

Table 14. NVM OEM Data Memory

Requirement	Parameter	Value	Unit
DS_081	NVM OEM data memory (OTP)	64	16-bit words
DS_082	NVM OEM data memory (OTP) with dedicated command set	64	16-bit words

7.8 Over-Voltage and Short-Circuit Protection

The ZSSC4162D-01 is designed for a 5V supply provided by an electronic control unit (ECU). The ZSSC4162D-01 and the connected sensor elements are protected from over-voltage and reverse-polarity damage by an internal supply voltage limiter. The DOUT pin is protected from short circuits, over-voltage, and reverse polarity. These functions are described in Table 15 and are valid for operation of the ZSSC4162D-01 in the application circuit shown in section 11 within the specifications of the absolute maximum ratings given in section 3.

Note: The specified junction temperature range T_J (refer to Table 2) is in force not only for operation but also for all protection cases listed in Table 15. In the event of an over-voltage, the device might have increased power dissipation. Depending on the sensor elements and the output load, this might lead to a violation of the maximum junction temperature.

Table 15. Over-Voltage, Reverse-Polarity, and Short -Circuit Protection

Specification	Symbol	Parameter	Description	Min	Typ	Max	Unit
Over-Voltage and Reverse-Polarity Protection							
DS_085	V_{VDDE_OV1}	Maximum voltage at VDDE to VSSE	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_086	V_{VDDE_OV2}	Maximum voltage at VDDE to DOUT [a]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_087	V_{DOUT_OV1}	Maximum voltage at DOUT to VSSE	Independent of resistance between VDDE and DOUT or VSSE	0		18	V
DS_088	V_{DOUT_OV2}	Maximum voltage at DOUT to VDDE[a]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_089	V_{VSSE_OV1}	Maximum voltage at VSSE to VDDE[a]	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_090	V_{VSSE_OV2}	Maximum voltage at VSSE to DOUT[a]	Independent of resistance between VDDE and DOUT or VSSE	0		18	V
Short Circuit Protection							
DS_091	$I_{VDDA\_SHRT\_VSSA}$	Current limitation in the event of a VDDA to VSSA short circuit	The output is deactivated (high Z). The supply current is limited to 60mA.			60	mA
DS_092	$I_{DOUT\_SHRT\_VSSE}$	Current limitation in the event of a DOUT to VSSE short circuit	Output is activated; output current limitation has been adjusted	-10		-2	mA
DS_093	$I_{DOUT\_SHRT\_VDDE}$	Current limitation in the event of a DOUT to VDDE short circuit	Output is activated, output current limitation has been adjusted	2		10	mA

[a] Reverse polarity condition.

8. Fault-Safe Operation

8.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4162D-01 and of the connected sensing elements at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described below depending on the diagnostic mode.

The ZSSC4162D-01 differentiates between two DMs with different behavior: Static Diagnostic Mode and Temporary Diagnostic Mode.

Static Diagnostic Mode

- Measurement and conditioning cycle are interrupted.
- The update of I2C output registers is stopped, and the register content is initialized with 8000_{HEX}.
- The ZACwire™ interface for one-wire communication (OWI) is enabled; both RAM output pages are readable. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing.
- The watchdog can trigger the Static Diagnostic Mode (or a full chip reset, depending on customizable settings)
- The ZSSC4162D-01 can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering (see below).
- The update of I2C output registers is continued; a fault code is available on a dedicated I2C output register.
- The ZSSC4162D-01 returns to Normal Operation Mode (NOM) including I2C transmission of valid sensor signal if fault checks do not detect continuation of fault conditions.

Fault Confirmation

The fault confirmation of the ZSSC4162D-01 is defined as follows:

- Fault confirmation is only processed for fault checks assigned to the Temporary DM.
- Fault confirmation is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.
- Fault confirmation is an up-and-down event counter that allows confirmation of a failure event.

8.2 Fault Messaging

8.2.1 Overview

The SENT interface offers three different options for fault messaging:

- Fault codes in the data channels (the Fast Channels as well as the SDM Channels; e.g., the channel used for temperature)
- Two status bits in the SENT status nibble
- SDM Channel status word

8.2.2 SENT Fast Channel Fault Codes

For the 12-bit SENT Fast Channel, the output value interval [4089, 4095] is reserved for fault codes. This is according to the SENT standard. In addition, the value 0 is used to signal initialization (no valid data available).

In the ZSSC4162D-01, the SENT Fast Channel fault codes are selectable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the fault code of the highest prioritized fault is transmitted.

8.2.3 SENT Status Bits

According to the SENT standard, the SENT status nibble contains two bits for status information. The assignment of the status bits to the individual detectable faults is configurable.

8.2.4 SENT SDM Channel Status Codes

The SENT standard defines a SMD Channel status word assigned to the SDM identifier #01.

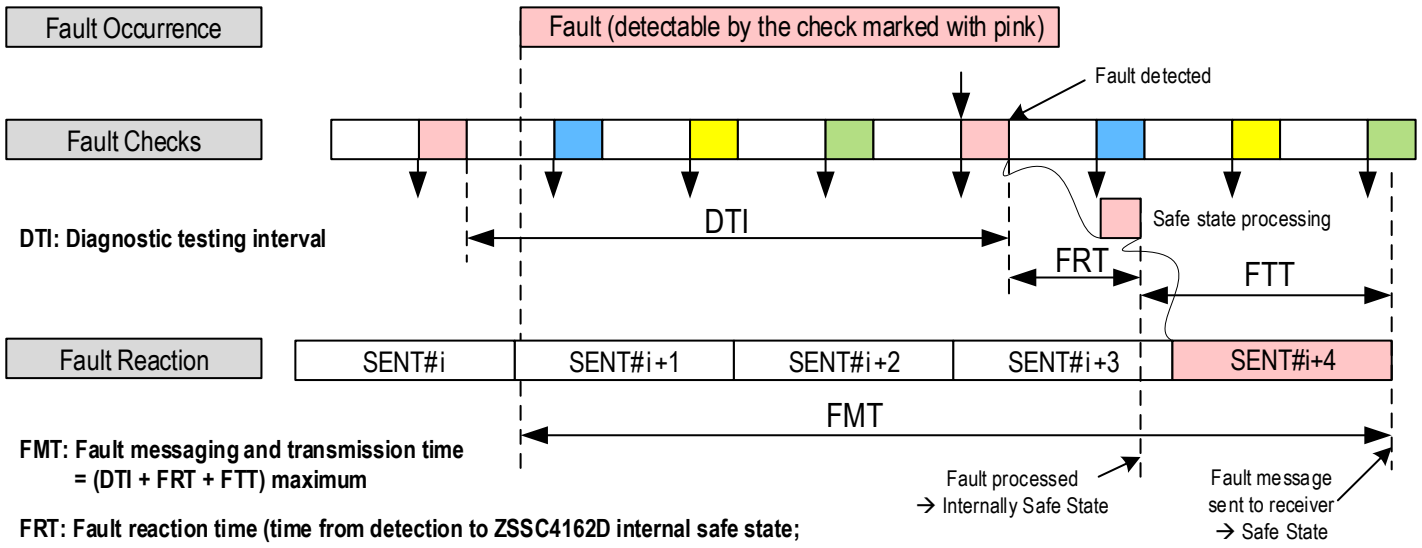
In the ZSSC4162D-01, the SENT SMD Channel status codes are freely programmable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the status code of the highest prioritized fault is transmitted.

8.2.5 Timing Definitions

The timing for the fault messaging is illustrated in Figure 6. See section 5.10 in Table 4 for the fault messaging time (FMT) specifications. Refer to the *Configuration Description Report* (CDR) regarding the timing for the diagnostic testing interval (DTI).

Figure 6. Fault Messaging Timing Diagram

Note: In this figure, the different colors indicate the different fault checks processed in the cycle.



9. Fault Checks

9.1 Overview

The ZSSC4162D-01 implements diagnostic mechanisms. Table 16 lists the available fault checks.

Table 16. Fault Checks Overview

Note: See important notes at the end of this table.

Specification	Identifier	Fault Check
ZSSC4162D-01 Self-Supervision Fault Checks		
DS_094	VDDAPOR	Analog supply voltage V_{VDDA} under-voltage check; power-on reset (POR)
DS_095	VDDDBOD	Digital supply under-voltage check; brownout detection (BOD)
DS_096	OSCFAIL	Oscillator-fail check based on a second oscillator/timer; reset after oscillator restart
DS_097	ROMCRC	ROM content CRC check
DS_098	NVMCRC	NVM content CRC check
DS_099	RAMCRC	RAM content CRC check
DS_100	RAMPRTY	RAM content parity check
DS_101	WWDG	Windowed watchdog; microcontroller and measurement and conditioning cycle active check
DS_102	INITCRC	Measurement and conditioning initialization check; processing, order, and configuration
DS_103	MCYCCRC	Measurement cycle operation check; processing, order, and configuration
	AFEMUX	AFE input multiplexer operation check
	REGCRC	Configuration register content CRC check
DS_104	CCYCCRC	Conditioning cycle operation check; processing, order, and configuration
DS_106	SENTPHY	SENT transmission monitoring
DS_107	CHIPP	Chipping check
DS_108	COMP	Computational check; microcontroller conditioning calculation, code processing, and peripheral bus access check
DS_110	ADCOFFSRNG	ADC offset range check; ADC operation check
DS_111	AFEGAIN	AFE gain check
DS_112	VDDARNG	Analog supply voltage V_{VDDA} range check; front-end and sensor supply
DS_173	BRSRAW	Full-bridge sensor raw data check
Sensing Element Fault Checks		
DS_113	BRSC	Bridge sensor connection check
DS_114	BRSS	Bridge sensor short check
DS_116	TSI	Internal temperature sensor operation check
DS_117	TSEC	External temperature sensor connection check

Specification	Identifier	Fault Check
Environment and Operating Condition Fault Checks		
DS_118	BRSRNGH	Bridge sensor conditioning result range check: upper limit
DS_119	BRSRNGL	Bridge sensor conditioning result range check: lower limit
DS_120	TSIRNG	Internal temperature sensor range check (over-temperature/under-temperature)
DS_121	TSERNG	External temperature sensor range check (over-temperature/under-temperature)
DS_122	VDDEUV	Supply voltage V_{VDDE} under-voltage check
DS_123	VDDEOV	Supply voltage V_{VDDE} over-voltage check
DS_124	CSAT	Conditioning calculation saturation check

9.2 Fault Checks for ZSSC4162D-01 Self-Supervision

The ZSSC4162D-01 provides several fault checks which supervise the ZSSC4162D-01 hardware itself.

Table 17. ZSSC4162D-01 Hardware Fault Checks

Note: See important notes at the end of this table.

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_094	V_{VDDA} under-voltage check (VDDAPOR); power-on reset	< 200µs	–	Always on	Static	1
DS_095	Digital supply under-voltage check (VDDDBOD); brownout detection	< 200µs	–	Always on	Static	1
DS_096	Oscillator fail check (OSCFAIL)	< 200µs	–	Always on	Static	1
DS_097	ROM CRC check (ROMCRC)	< FMT	–	Always on	Static	1
DS_098	NVM CRC check (NVMCRC)	$t_{STARTUP}$	Page-wise 16-bit CRC	Always on	Static	1
DS_099	RAM CRC check (RAMCRC)	< FMT	Page-wise 16-bit CRC	Always on	Static	1
DS_100	RAM parity check (RAMPRTY)	< FMT	–	Always on	Static	1
DS_101	Windowed watchdog (WWDG)	< 2 × OUR	–	Always on	Static	1
DS_102	Initialization phase check (INITCRC)	$t_{STARTUP}$	16-bit CRC	Enable/ Disable	Static	1
DS_103	Measurement cycle check (MCYCCRC) including ▪ AFE input multiplexer check (AFEMUX) ▪ Register data check (REGCRC)	< FMT	16-bit CRC	Enable/ Disable	Static	1

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_104	Conditioning cycle check (CCYCCRC)	< FMT	16-bit CRC	Enable/ Disable	Static	1

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

Table 18. ZSSC4162D-01 Operation and Cycle Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_106	SENT transmission monitoring (SENTPHY) [c]	< FMT	–	Enable/ Disable	Temporary	2
DS_107	Chipping check (CHIPP)	< FMT	–	Enable/ Disable	Temporary	2
DS_108	Computational check (COMP) including microcontroller arithmetic, code processing, and bus access	< FMT	–	Enable/ Disable	Temporary	2
DS_110	ADC offset check (ADCOFFSRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	3
DS_111	AFE gain check (AFEGAIN)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	4
DS_173	Full-bridge sensor raw data check (BRSRAW)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	4
DS_112	Analog supply voltage check (VDDARNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	15

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

[c] SENTPHY is not applicable for SENT tick times less than 3µs.

9.3 Fault Checks for Sensing Element Supervision

The ZSSC4162D-01 provides several fault checks that supervise the sensing elements.

Table 19. Sensing Element Fault Checks

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_113	Bridge sensor connection check (BRSC)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	6
DS_114	Bridge sensor short check (BRSS)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	7
DS_116	Internal temperature sensor operation check (TSI)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	9
DS_117	External temperature sensor connection check (TSEC)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	10

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

9.4 Fault Checks for Environment and Operating Condition Supervision

The ZSSC4162D-01 provides several fault checks that supervise the environment and operating conditions.

Table 20. Environment and Operating Condition Fault Checks

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_118	Bridge sensor range check upper limit (BRSRNGH)	< FMT	Upper limit	Enable/ Disable	Temporary	13
DS_119	Bridge sensor range check lower limit (BRSRNGL)	< FMT	Lower limit	Enable/ Disable	Temporary	13
DS_120	Internal temperature sensor range check (TSIRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	9
DS_121	External temperature sensor range check (TSERNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	11
DS_122	Supply V_{VDDE} under-voltage check (VDDEUV)	< FMT	Lower limit	Enable/ Disable	Temporary	15
DS_123	Supply V_{VDDE} overvoltage check (VDDEOV)	< FMT	Upper limit	Enable/ Disable	Temporary	14
DS_124	Conditioning calculation saturation (CSAT)	< FMT	–	Enable/ Disable	Temporary	16

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

Table 21. SENT Transmission Fault Checks

Note: SENT transmission fault checks must be implemented on the SENT receiver.

Fault Check	Messaging Time	Adjustable	Notes	Priority [a]
SENT CRC (SENTCRC)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT tick time (SENTTICK)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT timeout (SENTIMEOUT)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT sync time (SENTSYNC)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT idle state (SENTIDLE)	t_{FRAME}	n.a.	SENT receiver	n.a.

[a] Prioritization describes the default fault messaging order (“1” means highest priority).

9.5 Fault Check Limit Settings

ZSSC4162D-01 provides several fault checks based on the monitoring of a physical value. A fault is detected if the measurement value exceeds or falls below a given limit. For every measurement, there are specific transfer characteristics from the monitored physical value to the measurement value. The reverse function maps a limit to a specific physical value. Because of the part-dependent measurement tolerance, a defined limit spreads out over a certain value range determined by a lower and an upper threshold. Thus a fault is securely detected as illustrated in Figure 7 if the physical value falls below the lower threshold (A) coming from the lower limit, or if it exceeds the upper threshold (D) coming from the upper limit. Otherwise it is ensured that no fault is messaged if the physical value is in the range between the upper threshold (B) coming from the lower limit and the lower threshold (C) coming from the upper limit. Table 22 shows the resulting fault detection characteristics.

Figure 7. General Fault Thresholds

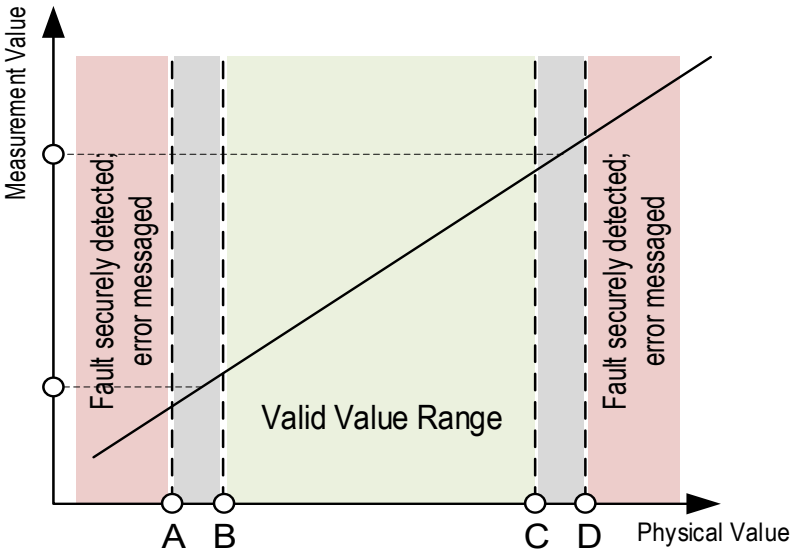


Table 22. Fault Check Threshold Definition

Threshold	Description
A	Below this threshold, the monitored physical value is erroneous; fault is securely detected and messaged.
B	Above this threshold, the monitored physical value is in the permitted range; no fault is messaged.
C	Below this threshold, the monitored physical value is in the permitted range; no fault is messaged.
D	Above this threshold, the monitored physical value is erroneous; fault is securely detected and messaged.

The 4162_0500_01 configuration provides default limits for the fault checks. These limits and the resulting thresholds are listed in Table 23.

Note that there are several fault checks that evaluate a conditioned measurement value. In this case, the specified thresholds refer directly to the conditioned value and the limits are derived from the specified target transfer function. For limit adjustments, the fault checks can be classified into three types:

- Type I – no calibration or limit adjustment necessary.
  The coefficients and limits are part of the configuration and are not allowed to change. They are silicone-related and independent from the application or the pressure sensor itself.
- Type II – calibration or limit adjustment is necessary once per application.
  The coefficients and limits need to be evaluated on the module level once per application. After validation, they are valid for every module and can be used in production.
- Type III – calibration or limit adjustment is necessary during production.
  The coefficients or limits need to be calculated during production for every module individually.

Table 23. Fault Check Limits

Fault Check	Monitored Physical Value	Type	Default Thresholds				
			A	B	C	D	Unit
BRSS	Bridge sensor short	I	50	800	–		Ω
BRSC	Bridge sensor connection [a]		-	-	20	240	kΩ
TSI	PTAT voltage (internal temperature sensor) ADC raw data result		4		96		% FSR
VDDEOV	Supply voltage V_{VDDE} over-voltage check		-	-	5.5	5.7	V
VDDEUV	Supply voltage V_{VDDE} under-voltage check		4.3	4.5	-	-	V
VDDARNG	Analog supply voltage V_{VDDA} range check; front-end and sensor supply		4.3	4.5	-	-	V
AFEGAIN	AFE gain check		-2.5		2.5		% gain
ADCOFFSRNG	ADC offset range check; ADC operation check		-2		2		% FSR
BRSRAW	Full-bridge (differential signal) ADC raw data result [b]	II	4		96		% FSR
TSIRNG	Conditioned on-chip temperature [c], [d]		-50	-40	150	165	°C
TSERNG	External temperature sensor range check [e]		Custom				°C
BRSRNG	Conditioned full-bridge sensor signal		Custom				% Data Output
TSEC	External temperature sensor connection check [e]		0	0.02	0.98	1	%VDDA

[a] Refer to section 9.5.2 for details in application usage.

[b] Refer to section 9.5.1 for details for application usage.

[c] If the absolute temperature value accuracy is relevant, an on-chip temperature calibration is necessary for accuracy better than ±10K.

[d] Limits are related to junction temperature measured with the internal PTAT sensor.

[e] By default, no external temperature sensor is activated and the fault check limits are selected to deactivate the failure detection.

9.5.1 BRSRAW

The limits of the ADC raw data check must be adjusted depending on the selected ADC resolution for the full-bridge measurement. The ADC raw data measurement register range is $[0,2^{15})$. If the resolution is higher than 14 bit, the digital zooming is activated and the range of the ADC results is different.

Table 24. BRSRAW Thresholds

ADC Resolution [bits]	ADC Result Range	Lower Limit	Upper Limit
14	$[0,2^{15})$	$0.04 * (2^{15-1})$	$0.96 * (2^{15-1})$
15			
16	$(-2^{15},2^{15})$	-32767	32766
17			
18			

9.5.2 BRSC

The limits for this check cannot be changed. The sensor connection check is sensitive to bridge common mode variation. It will trigger the Temporary Diagnostic Mode if the common mode changes more than ±15% referenced to the bridge supply voltage. This behavior is not a failure and is given by system design. The application design must account for this behavior on the module development level.

10. Configuration and Adjustment

The ZSSC4162D-01 is based on a dedicated configuration that must be adjusted for the application. This includes the adjustment of some ZSSC4162D-01 parameters, the configuration of the sensor signal measurements, the calibration of the sensor conditioning calculation, and the setup of the SENT protocol.

Table 25. Sensor Signal Measurement Configuration

Specification	Parameter	Conditions	Value	Unit
DS_127	Gain P1	Full-bridge sensor signal gain (adjustment steps)	14	–
DS_129	Gain TSE	External temperature sensor signal gain (adjustment steps)	14	–
DS_130	Source select for BR temperature compensation	Selection of the temperature signal used for temperature compensation of the main sensor signal	TSI / TSE	–
DS_131	Source select for SENT temperature output	Selection of the temperature signal used for the SENT temperature measurement output	TSI / TSE	–
DS_132	TSE type	External temperature sensor type	Diode	–

Table 26. Calibration of Sensor Signal Conditioning Calculation

Requirement	Parameter	Conditions	Value	Unit
DS_133	Full-bridge signal offset compensation	Coefficients for 2nd order temperature compensation (number of coefficients)	4	16-bit words
DS_134	Full-bridge signal gain compensation	Coefficients for 2nd order temperature compensation (number of coefficients)	4	16-bit words
DS_135	Full-bridge signal nonlinearity compensation	Coefficients for 3rd order nonlinearity compensation (number of coefficients)	5	16-bit words
DS_136	Full-bridge signal filter	Conditioned full-bridge signal filter: average and differential coefficients	1	16-bit words
DS_141	Temperature TSI conditioning	Temperature from internal temperature sensor; coefficients for gain, offset, and 2nd order nonlinearity compensation	4	16-bit words
DS_142	Temperature TSI filter	Conditioned internal temperature signal filter: average and differential coefficients	2	–
DS_143	Temperature TSE conditioning	Temperature from external temperature sensor; coefficients for gain, offset, and 2nd order nonlinearity compensation	4	16-bit words
DS_144	Temperature TSE filter	Conditioned external temperature signal filter: average and differential coefficients	2	–

Table 27. SENT Protocol Configuration

Requirement	Parameter	Conditions	Value	Unit
DS_147	Tick time	Clock tick times	[2.4 to 128]	µs
DS_148	Frame length	Enables constant frame length	[282 to 1024]	Clock ticks
DS_149	Sensor type	Single Sensor (P/t), Single Secure Sensor (P/S/t), Pressure-Pressure Sensor (P1/P2/t)	Selectable	–
DS_151	SDM priority	Up to 3 priority levels	Configurable	–
DS_152	SDM ID	SDM Identifier	Programmable	–
DS_153	SDM data	Static SDM data	Programmable	–
DS_154	SDM initial data	Initial data for SDM signal channels	Programmable	–
DS_155	Temperature SDM	Priority level for SENT SDM channel of conditioned temperature output	Configurable	–
DS_156	Status SDM	Diagnostic codes	Programmable	–

Table 28. Fault Handling Configuration

Requirement	Parameter	Conditions	Value	Unit
DS_157	Watchdog reset	The Static Diagnostic Mode results in a functional halt or in a reset after a watchdog timeout	Selectable	–
DS_158	BRSRNGH limits	Full-bridge sensor conditioning result check upper limit	Upper limit	16-bit words
DS_159	BRSRNGL limits	Full-bridge sensor conditioning result check lower limit	Lower limit	16-bit words
DS_161	TSIRNG limits	Internal temperature sensor range check limits	Upper limit, lower limit	16-bit words
DS_162	TSE limits	External temperature sensor connection check limits	Upper limit, lower limit	16-bit words
DS_163	TSERNG limits	External temperature sensor range check limits	Upper limit, lower limit	16-bit words
DS_164	CMR limits	Common mode voltage check limits	Upper limit, lower limit	16-bit words
DS_165	AFEGAIN input	AFE gain check input voltages	2 AFEDAC configurations	16-bit words
DS_166	AFEGAIN limits	AFE gain check limits	2 upper limits, 2 lower limits	16-bit words
DS_167	COMP input	Computation check input value	Input value	16-bit word
DS_168	COMP limits	Computation check limits	Upper limit, lower limit	16-bit words
Informational [a]	MCYCCRC value	Measurement cycle check expected CRC	Initial CRC, cycle CRC	16-bit words
Informational [a]	CCYCCRC value	Conditioning cycle check expected CRC	Initial CRC, cycle CRC	16-bit words

[a] Generation of the expected CRCs for MCYCCRC and CCYCCRC fault checks is supported by a dedicated command.

11. Application Circuit and External Components

Table 29. Application Circuit Example with Full-Bridge Input BR1

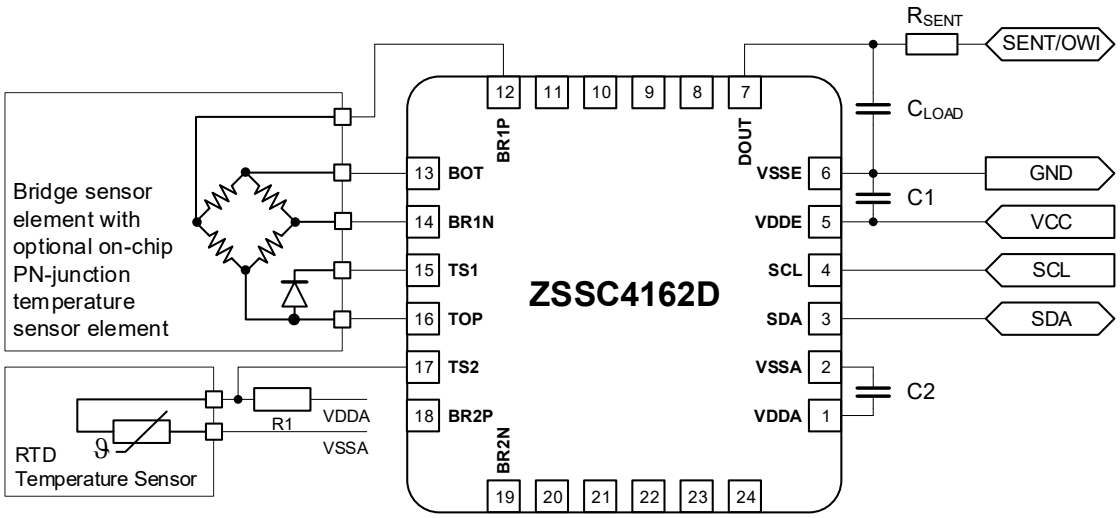
Specification	Circuit Diagram
DP_043	
	Application features: ▪ 5V module is powered by the application's electronic control unit (ECU). ▪ Sensor module with 3-pin connector provides pressure and medium or ambient temperature measurement data via SENT output. ▪ Temperature signal for pressure signal correction can be derived either from the on-chip PTAT or from an external diode or RTD (connected to TS1 or TS2). ▪ End-of-line calibration uses one-wire communication via the DOUT pin.

Table 30. Dimensioning of External Components for the Application Example

Note: The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

Specification	Component	Symbol	Conditions	Min	Typical	Max	Unit
DP_044	Capacitor	C1	V_{MAX} ≥ 32V		100 ± 20%		nF
	Capacitor	C2	V_{MAX} ≥ 10V		100 ± 20%	470 + 20%	nF
	Capacitor	C_{LOAD}	V_{MAX} ≥ 32V		2.2 ± 20%		nF
	Resistor	R_{SENT}				50	Ω
	Resistor	R1		1.6	R_{25}		kΩ

12. ESD Protection and EMC Specification

12.1 ESD Protection

All pins have an ESD protection of up to 2kV according to the Human Body Model (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and DOUT pins have an additional ESD protection of up to 4kV (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7).

The levels of ESD protection are tested with devices in a 4 × 4 mm 24-QFN package during the product qualification.

12.2 Electromagnetic Emission

The wired emission of the externally connected pins of the ZSSC4162D-01 is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

Measurements must be performed with the application circuit described in section 11; SENT transmission uses a tick time of 9µs.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 Code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN.*

12.3 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard:

Measurements must be performed with the application circuit described in section 11; the sensor bridge is replaced by a 3-resistor string connected to TOP, BR1P, BR1N, and BOT; SENT transmission uses a tick time of 9µs.

Table 31 gives the specifications for the DPI tests. RES refers to the coupling impedance. CAP refers to the injection capacitance.

Table 31. Conducted Susceptibility (DPI) Tests

Requirement	Test	Frequency Range	Power [dBm]	Load Pins	Protocol	Error Band[a]	Comment
DS_169	DPI, direct coupled	1MHz to 10MHz	20dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP= 4.7nF
DS_170	DPI, direct coupled	>10MHz	30dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP = 4.7nF

[a] Error band regarding main signal (SENT FC1).

13. Reliability and RoHS Conformity

The ZSSC4162D-01 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

The ZSSC4162D-01 complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded at https://www.renesas.com/eu/en/document/cer/green-products-rohs-material-declaration-certificate.

13.1 Calculation of Power Dissipation and Junction Temperature

Calculation examples for self-heating (maximum thermal resistor in 24-QFN package is $R_{th\_JA\_QFN24}$ = 32K/W):

- Normal Operation:
  - Maximum supply current at 5.5V is 10mA Minimum SENT load resistance of 10kΩ

    Maximum power dissipation is P_{max} = 5.5V ∗ 10mA + 5.5V ∗ 5.5V / 10kΩ = 58mW.

    Temperature difference: $T_J - T_{AMB}$ = 32K/W ∗ 58mW = 1.9K.

    → With the conditions above, the maximum junction temperature T_J is ~2K greater than the ambient temperature T_{AMB}.
- Over-Voltage Conditions (18V):

  Maximum power dissipation is $P_{max,OV}$ = 300mW; output is switched off.

  Temperature difference: T_J - T_{AMB} = 32K/W × 300mW = 9.6K.

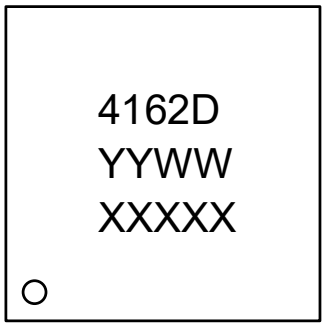
→ With these conditions, the maximum junction temperature T_J is ~10K greater than the ambient temperature T_{AMB}.

14. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

Package Outline Drawing Package Code: NLG24S2 24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch

15. Marking Diagram



1. "4162D-01" is the truncated part number.
2. "YYWW" is the last digits of the year and week that the part was assembled.
3. "XXXXX" is the last digits of the lot number.

16. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
ASIL	Automotive Safety Integrity Level
BOD	Brownout Detection
BR	Bridge Sensor
CDR	Configuration Description Report
CM	Command Mode
CMC	Calibration Microcontroller; optimized microcontroller architecture for Renesas signal conditioners
CMV	Common Mode Voltage
DM	Diagnostic Mode
DNL	Differential Nonlinearity
DTI	Diagnostic Testing Interval; the rate of fault check processing
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FMT	Fault Messaging Time; latency from the fault event to the completion of the transmission of the fault message
FS	Full Scale
FTT	Fault Transmission Time
HBM	Human Body Model
I/O	Input/Output
I2C	Inter-Integrated Circuit; serial two-wire data bus
INL	Integral Nonlinearity
LSB	Least Significant Bit
LSN	Least Significant Nibble
MSB	Most Significant Bit
MSN	Most Significant Nibble
MUX	Multiplexer
MTP	Multiple-Time Programmable
n.a.	Not Applicable
n.c.	Not Connected
NOM	Normal Operation Mode
NVM	Nonvolatile Memory

Term	Description
OTP	One-Time Programmable
OWI	One-Wire Interface
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
POR	Power-On Reset
PTAT	Proportional-to-Absolute Temperature
PWR	Power Management and Protection Unit
QFN	Quad-Flat No-Leads – ZSSC4162D-01 package
RAM	Volatile Memory for Configuration and Conditioning Coefficients
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory
RTD	Resistive Temperature Device
SCCM	Sensor Check and Common Mode Adjustment Unit
SSC	Sensor Short Check (diagnostic task) or Sensor Signal Conditioner
TSI	Internal Temperature Sensor
TQE	Extended Temperature Range Identifier
ZACwire™	Renesas-Specific One-Wire Interface (OWI)

17. Ordering Information

Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC4162DE4R	Single bridge input, SENT output, internal and/or external temperature measurement, 4 × 4 mm 24-QFN, wettable flanks	MSL1	13” Reel	-40°C to 150°C
ZSSC4160EVKV1P5	ZSSC416x SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, 10 Samples.			

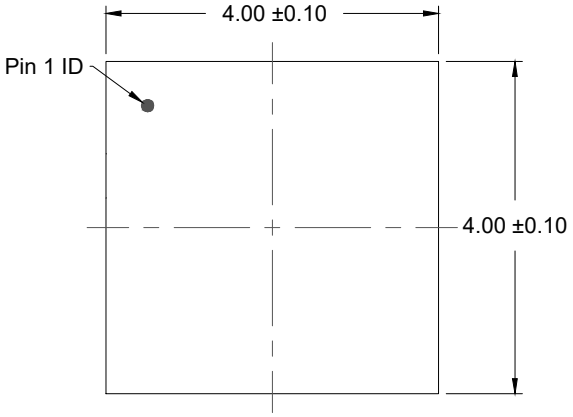
Contact Renesas for additional options.

18. Revision History

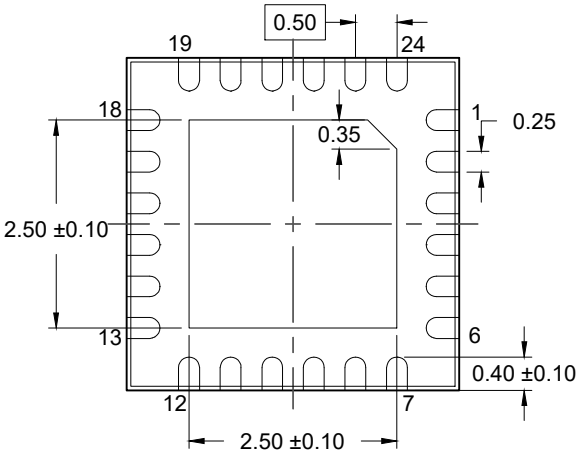
Revision Date	Description of Change
Apr 23, 2026	▪ Updated QFN-20L package recommendation (see “Pin Assignments”) ▪ Split programming time into 2x parameters (see “Nonvolatile Memory”: DS_068) ▪ Completed other minor changes
January 21, 2025	▪ DS_065: decreased the max limit to 125 ▪ DS_066: Parameter changed
February 1, 2022	▪ Correcting BRSRAW Thresholds for 15 bits ▪ Correcting calculation of power dissipation ▪ Evaluation Kit ordering code updated ▪ ZSSC4162DE4W removed from ordering codes
November 18, 2020	▪ Datasheet Template Update
July 30, 2019	▪ DS_105 removed ▪ Correcting DS_064, DS_092 and DS_093
July 4, 2019	▪ Removing irrelevant footnote from Table 30
April 18, 2019	▪ Rename product from “ZSSC4162D” to “ZSSC4162D-01” ▪ Update of Ordering information
March 6, 2019	Initial release.

Package Outline Drawing

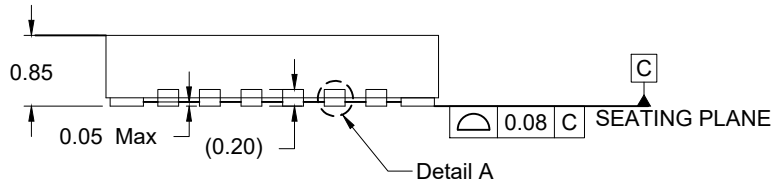
PSC-4192-05
NLG24S2
24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch
Rev.08, Jun 20, 2025



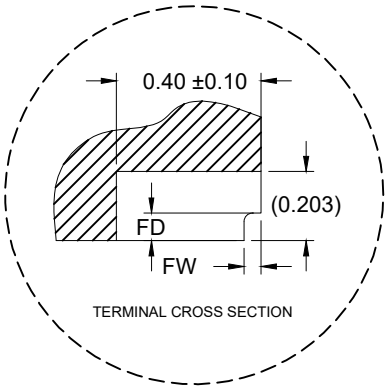
TOP VIEW



BOTTOM VIEW



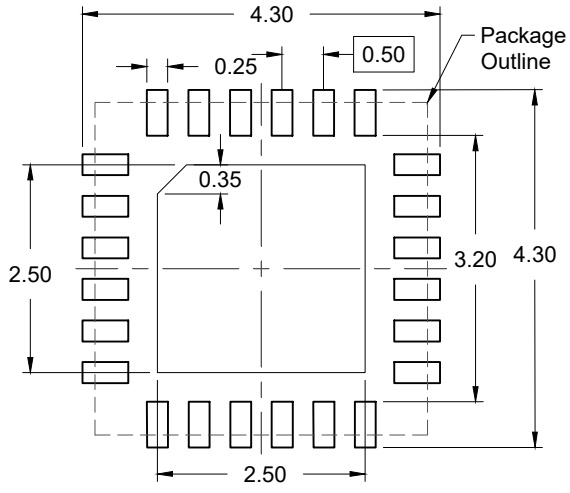
SIDE VIEW



DETAIL A

Table 1: Dimensions of wettable flank (DETAIL A)

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.010	0.075



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

Notice

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