ZSSC4161D-01

Automotive Resistor Sensor Signal Conditioner with I2C Output

Description

The ZSSC4161D-01 is a member of Renesas' family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor element signals. Featuring a maximum analog pre-amplification up to 200, the ZSSC4161D-01 is configurable to nearly all resistive bridges. This datasheet specifies the specific configuration 4161_0500_01.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity are accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4161D-01 nonvolatile memory (NVM), which is reliable in automotive applications.

ZSSC4161D-01 supports use of an external diode or internal PTAT as a temperature reference.

Measured values are provided via a digital I2C interface. The I2C interface enables transmission of sensor data according to the standard interface description. End-of-line calibration is also supported through this interface. The ZSSC4161D-01 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly costs low as no trimming by external devices or lasers is needed.

The ZSSC4161D-01 is optimized for automotive environments by overvoltage and reverse polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Fluid brake pressure sensing (PV)
- Hydraulic pressure sensing
  (e.g., steering systems with hydraulic steering support)
- Pneumatic pressure sensing
  (e.g., air brake systems; pneumatic shock absorbers)

Features

- One differential full bridge sensor element measurement
- One internal chip temperature measurement
- Digital compensation for offset, gain, and higher order nonlinearity as well as temperature coefficients of the differential and half bridge sensor element input signal
- Operating temperature range: -40°C to 150°C
- Accuracy as high as ±0.50% full scale at -40°C to 150°C (see the electrical characteristics table for conditions)
- NVM memory for configuration, calibration data, and configurable measurement and conditioning functionality
- One-pass, end-of-line calibration algorithm minimizes production costs
- I2C interface for programming, calibration, and data output
- Alternative ZACwire™ one-wire interface (OWI) on DOUT pin available for programming/calibration/fault-communication
- No external trimming or components required
- Qualified according to AEC-Q100 Grade 0

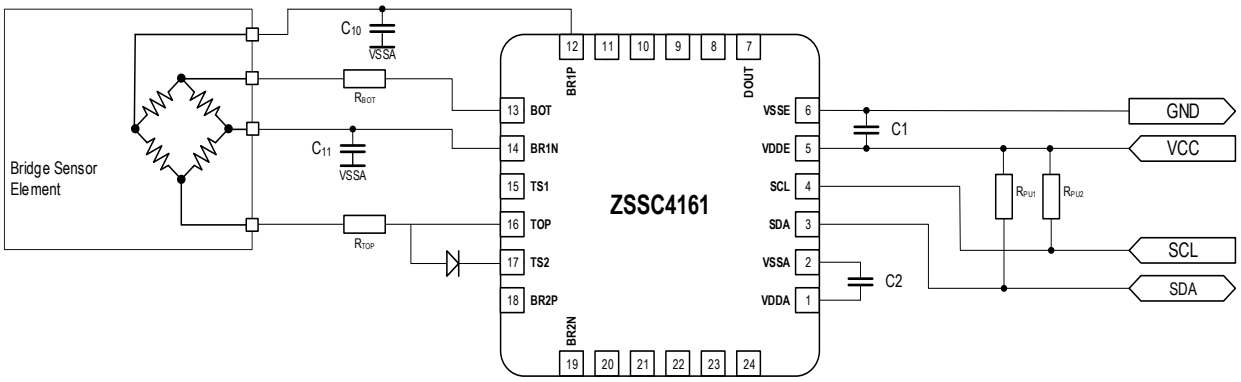
Physical Characteristics

- Supply voltage: 4.5V to 5.5V
- Over-voltage and reverse polarity protection up to ±18V
- Bridge sensor element input span: 1mV/V to 800mV/V
- Output resolution: 15-bit via I2C interface
- Package: 24-QFN (4 × 4 mm; wettable flanks) or bare die

Available Support

- Evaluation kit
- Application notes
- Calculation tools

ZSSC4161D-01 Basic Circuit



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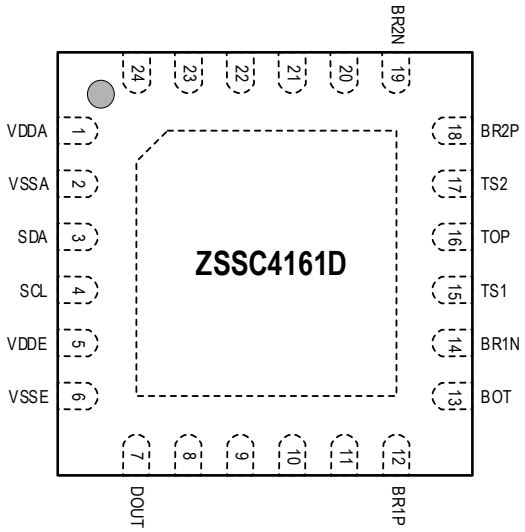
1. Pin Assignments

The ZSSC4161D-01 is available in a 24-QFN (4 x 4 mm; wettable flanks) RoHS-conformant package.

Note: The backside of the 24-QFN package (exposed pad; see section 13) is electrically connected to VSSA.

Recommendation: Solder the QFN exposed pad to the PCB, even if electrically redundant, to ensure adequate thermal performance and to reduce mechanical stress and solder joint failure risk.

Figure 1. 24-QFN Pin Assignments – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Note: See important notes at the end of the table.

24-QFN Pin #	Pin Name	Type	Description
1	VDDA	Supply	Internal supply [a]
2	VSSA	Supply	Internal ground
3	SDA	I/O	I2C data input/output with internal pull-up [b], [c]
4	SCL	Input	I2C clock, with internal pull-up [b], [c]
5	VDDE	Supply	External supply
6	VSSE	Supply	External ground
7	DOUT	I/O	Not used
8 to 11	–		n.c.
12	BR1P	Input	Positive bridge sensor input 1 [d]
13	BOT	Supply	Negative bridge supply voltage
14	BR1N	Input	Negative bridge sensor input 1 [d]
15	TS1	Input	Diode sensor input
16	TOP	Supply	Positive bridge supply voltage

24-QFN Pin #	Pin Name	Type	Description
17	TS2	Input	Diode sensor input
18	BR2P	Input	Positive bridge sensor input 2 [d]
19	BR2N	Input	Negative bridge sensor input 2 [d]
20 to 24	–	–	n.c.
-	EPAD	Supply	Internal ground; connected to VSSA [e]

[a] Do not supply VDDA externally.

[b] Internal pull-up.

[c] No connection required.

[d] Only one of the two sensor input options can be used: sensor input 1 (BR1P and BR1N) or sensor input 2 (BR2P and BR2N).

[e] Ground; can be shorted externally to VSSA (pin 2).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZSSC4161D-01 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.2.4 for information about overvoltage protection, reverse polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

Specification	Symbol	Parameter	Conditions	Min	Max	Unit
DS_177	V_{VDDE_ABS}	Supply voltage		-18	18	V
DS_178	V_{DOUT_ABS}	Voltage at the DOUT pin		-18	18	V
DS_179	V_{DIFF_ABS}	Pin voltage difference	Voltage between any two of these pins: VDDE, DOUT, and VSSE	-18	18	V
DS_180	V_{VDDA_ABS}	Analog supply voltage	On-chip controlled voltage; do not supply VDDA externally	-0.3	6	V
DS_181	V_{PIN_ABS}	Voltage at all other pins	Maximum voltage is V_{VDDA} + 0.3V	-0.3	6	V
DS_182	T_{J_ABS}	Junction temperature	Note: See section 7.2.4 regarding overvoltage protection	-40	160	°C
DS_183	T_{STOR_ABS}	Storage temperature		-55	155	°C

4. Operating Conditions

The operating conditions below specify the conditions that the application circuit must provide to the device during operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in section 5.

Table 3. Operating Conditions

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_009	V_{VDDE}	Supply voltage	VDDE to VSSE	4.75	5	5.25	V
DS_010	V_{VDDE_EXTD}	Extended supply voltage [a]	VDDE to VSSE; derated accuracy as specified with DS_059.	4.5	5	5.5	V
DS_011	V_{VDDE_OP}	Operating supply voltage [a]	VDDE to VSSE; derated accuracy Note for a supply greater than 5.5V: Above the ZSSC4161D-01 overvoltage limitation threshold, the output potential is clipped at this threshold.	4		6	V
DS_012	T_{AMB}	Ambient temperature [a], [c]	Temperature range	-40		150	°C
Informational [d]	$R_{th\_JA\_QFN24}$	Thermal resistance 24-QFN [a]	According to JESD 51		32		K/W
DS_185	R_{BR}	Bridge sensor resistance [a], [e]	One sensor bridge at pins BR1P and BR1N or BR2P and BR2N	1		15	kΩ

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Temperature stress over lifetime is restricted to the Temperature Profile described in section 12 or to similar stress caused by equivalent temperature profiles. Contact Renesas for temperature stress calculation support.

[c] Assuming application conditions according to Test Board Design as per JESD51-7 and natural convection Test Conditions as per JESD51-2.

[d] Package-related parameter.

[e] Symmetric behavior and identical electrical properties (especially the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

5. Electrical Characteristics

All parameter values are valid under the operating conditions specified in section 4 (unless otherwise stated). All parameters are valid for the ambient temperature range T_{AMB} and for the supply voltage range V_{VDDE} = 4.75 to 5.25 V. Unless otherwise defined, the parameters are related to the ZSSC4161D-01 itself. All voltages are referenced to VSSA pin.

The following parameters are specified based on a ZSSC4161D-01 main channel configuration setup using a PGA gain of 100 and assuming a resulting ADC input range usage of ≥ 50%FS. Further preconditions are an ADC resolution of 14 bits, a 2-step A/D conversion scheme using an MSB-to-LSB ratio of 8/6 bit, an oscillator frequency of 8MHz, and an ADC clock frequency of 1MHz (1st step) / 2MHz (2nd step).

Table 4. Electrical Parameters

Note: See important table notes at the end of this table.

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.1 Supply Current and System Operating Conditions							
DS_015	I_S	Supply current	Excluding sensor supply current and excluding output current at DOUT pin; oscillator adjusted to f_{OSC} = 8MHz		8	10	mA
DS_016	P_{OV}	Overvoltage power consumption [a]	5.5V < V_{VDDE} < 18V; excluding sensor and output load			300	mW
DS_017	$V_{OV\_LIM\_TH}$	Overvoltage limitation range[a]	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	5.55		18	V
DS_018	$V_{OV\_OFF\_TH}$	Overvoltage switch-off threshold [a]	The ZSSC4161D-01 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	7		12	V
DS_019	$t_{OV\_OFF\_DLY}$	Overvoltage switch-off delay [a]	The ZSSC4161D-01 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.		10	25	ms
DS_020	$I_{S\_OV\_OFF}$	Supply current limitation in the event of overvoltage switch-off [a]	Overvoltage switch-off is activated if the supply voltage exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$. V_{VDDE} < 18V; excluding sensor and output load			10	mA
DS_184	V_{VDDA}	Analog supply voltage	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	0.9		1.0	V_{VDDE}
DS_021	V_{SENS}	Bridge sensor supply voltage	$V_{SENS} = V_{TOP} – V_{BOT}$ at $R_{BR} ≥ 1k\Omega$ where V_{TOP} is the voltage at the TOP pin and V_{BOT} is the voltage at BOT pin.	0.9		1.0	V_{VDDA}
DS_022	V_{POR_OFF}	Power-on reset (POR) off-threshold	V_{VDDA} measured referenced to VSSA; POR is active until V_{VDDA} exceeds this threshold.	3.3		3.8	V
DS_023	V_{POR_ON}	Power-on reset on-threshold	V_{VDDA} measured referenced to VSSA; POR is activated if V_{VDDA} falls below this threshold.	3.0		3.6	V
DS_024	V_{POR_HYST}	Power-on reset hysteresis [a]	$V_{POR\_ON} – V_{POR\_OFF}$		0.4		V

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_025	f_{OSC}	Oscillator frequency	Calibrated oscillator frequency.	7.6	8	8.6	MHz
DS_026	TC_{OSC}	Oscillator frequency temperature coefficient [a]		-200		200	ppm/K
5.2 Analog Front-End Characteristics							
DS_027	V_{IN_SPAN}	Differential input span	Analog gain: 1 to 200	1		800	mV/V
DS_028	$V_{IN\_RNG\_1}$	Input voltage range	Analog gain = 1 Corresponds to V_{ADC_IN}	0.05		0.95	V_{SENS}
DS_029	$V_{IN\_RNG\_2}$		Analog gain = 2 to 200	0.3		0.65	V_{SENS}
DS_030	C_{IN}	Capacitance at input [a]	Capacitance at pins BR1P and BR1N or BR2P and BR2N to VSSA; requirement for timing parameters	0		12	nF
5.3 A/D Conversion Refer to section 7.1.1.4.							
DS_032	r_{ADC}	ADC resolution [a]	Fixed resolution selection for full bridge signal	14		18	Bit
DS_033	V_{ADC_IN}	ADC input range [a]	Differential input signal range for full bridge depending on analog gain a_{PGA} and ADC range shift rs_{ADC}: $V_{ADC\_IN} = V_{IN} \times a_{PGA} + rs_{ADC} \times V_{SENS}$	0.05		0.95	V_{SENS}
			Restriction for analog gain > 100	0.1		0.9	V_{SENS}
DS_034	DNL_{ADC}	DNL [a]				0.95	LSB
DS_035	INL_{ADC}	INL	Best fit		3	8	LSB_{14}
5.4 Temperature Measurement							
DS_036	ST_{TSI}	Internal temperature PTAT sensitivity[a]	Raw values, without conditioning calculation; analog gain = 12.6	20			LSB_{14} /K
DS_037	A_{TSE_D}	External temperature diode channel gain		10			LSB_{14} /mV
DS_038	I_{TSE_D}	External temperature diode bias current		10	20	40	µA
DS_039	V_{TSE_D}	External temperature diode input range [a]	Related to V_{TOP}, absolute measurement	-1		-0.2	V
5.5 Sensor Diagnostic Tasks							
DS_043	R_{BRSC_TH}	Sensor connection loss detection threshold[a]	Fault check BRSC: Sensor pin to ZSSC4161D-01 pin connection; without capacitive load at bridge input pins	20		100	kΩ
DS_044	R_{BRSS_TH}	Sensor short detection threshold[a]	Fault check BRSS: Sensor input pin BRxN to input pin BRxP	50		800	Ω

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.6 System Response							
DP_036	$t_{STARTUP}$	Startup time [a]	Time to first valid output after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz			7	ms
DP_037	OUR	Output update rate [a], [b]	ZSSC4161D-01 internal output update, asynchronous to I2C transmission (see section 7.1.3.1)		0.7	1	ms
DP_012	ORT	Output response time [a], [b]	100% input step	1.3		2	ms
DP_060	FMT	Fault message time				20	ms
5.7 System Accuracy							
DS_058	RE	Ratiometricity error	Maximum error for V_{VDDE} from 5V to 4.75V or to 5.25V Ratiometricity error is already contained in overall failure (DS_059).			500	ppm
DS_059	F_{ALL_BR}	Overall failure Deviation from ideal line including INL, gain, offset, and temperature impacts; excluding sensor-caused effects	Differential sensor readout V_{VDDE} = 4.75V to 5.25V			0.5	%FS
	$F_{ALL\_BR\_EXTD}$ [a]		Differential sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V			1.0	%FS
	F_{ALL_HBR} [a]		Single-ended sensor readout V_{VDDE} = 4.75V to 5.25V			1.0	%FS
	$F_{ALL\_HBR\_EXTD}$ [a]		Single-ended sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V			1.5	%FS
	$F_{ALL\_DERATED}$ [a]		In the operating supply voltage range V_{VDDE_OP}			5	%FS
5.8 Nonvolatile Memory							
DS_065	T_{AMB_NVM}	Ambient temperature for NVM programming		-40		150	°C
DS_066	N_{NVM_MTP}	Re-write cycles [a]	Multiple-time programmable approach is supported	4			
DS_067	t_{NVM_RET}	Data retention [a]	Temperature profile [c]	15			years
DS_068.1	$t_{NVM\_WRI\_DIFF}$	Programming time without soaking [a]	Per programmed data word in differential mode			1.7	ms
DS_068.2	$t_{NVM\_WRI\_RED}$		Per programmed data word in redundant mode			3.3	

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Time values are given based on a system clock frequency of 8MHz.

[c] Over lifetime and valid for the dice. Note that the package can cause additional restrictions.

6. Interface Characteristics

The I2C interface complies with the *I2C Bus Specification, Version 6.0, April 4, 2014.*

Table 5. Interface Characteristics

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6.1 Selected I2C Interface Parameters							
Informational	f_{SCL}	SCL clock frequency		0		400	kHz
DS_048	$V_{I2C\_IN\_IL}$	Input LOW-level voltage		-0.5	-	$0.15V_{DDA}$[a]	V
DS_049	$V_{I2C\_IN\_IH}$	Input HIGH-level voltage		0.7 V_{DD}	-	V_{DDA}+0.5V	V
DS_051	V_{OL}	Output LOW-level voltage	(Open-drain or open-collector) at 3 mA sink current; V_{DDE} = 5V	0	-	0.4	V
Informational	R_{I2C}	Internal pull-up resistor [b]		25		100	kΩ

[a] Different from the referenced I2C-bus specification.

[b] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

7. Circuit Description

7.1 General Operation Description

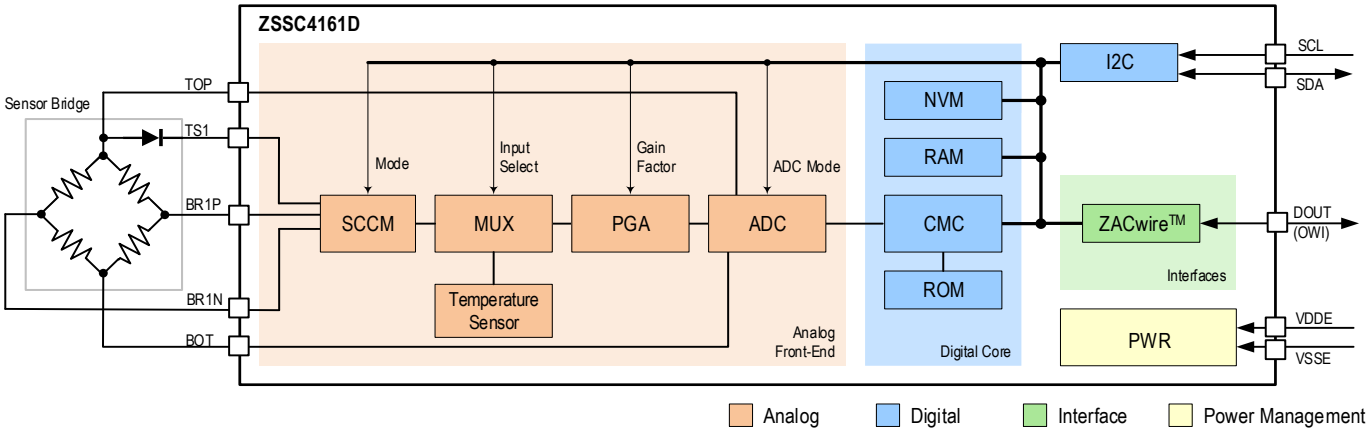
The ZSSC4161D-01 is a sensor signal conditioner for readout of resistive bridge sensor elements. This bridge sensor element signal is pre-amplified and converted to a digital signal by the ZSSC4161D-01's analog-to-digital-converter (ADC). Then the digital conversion results are offset compensated and gain adjusted. Temperature coefficients and nonlinearity of the bridge sensing element are compensated if necessary. Nonlinearity of the external temperature sensing elements is compensated. Then all calculated conditioning results can be output using the I2C protocol.

The ZSSC4161D-01 can measure a differential full bridge signal from the BR1P and BR1N pins or the BR2P and BR2N pins. All input pins are routed to the same multiplexer (MUX) for processing.

Signal conditioning processes the following tasks:

- Measurement of the voltage signal of the connected resistive sensing element
- Measurement of the internal temperature
- Measurement of the voltage signal of a connected temperature sensing diode
- Conditioning calculation for all sensor signals
- I2C output of the conditioning result

Figure 2. Block Diagram



SCCM	Sensor Check and Common Mode Adjustment Unit
MUX	Multiplexer
PGA	Programmable Gain Amplifier
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
ROM	Read-Only Memory for Correction Formula and Algorithm
NVM	Nonvolatile Memory for Configuration and Conditioning Coefficients
RAM	Volatile Memory for Configuration and Conditioning Coefficients
I2C	I2C Digital Interface
PWR	Power Management and Protection Unit

7.1.1 Analog Front-End

The analog front-end (AFE) consists of the sensor connection check module (SCCM), the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation. An internal PTAT is used to measure the die temperature.

7.1.1.1 SCCM

The sensor check and common mode block (SCCM) implements the self-diagnostic features for the analog front-end. The SCCM provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions.

7.1.1.2 Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path allowing the use of a single ADC. It allows a very flexible signal routing between the sensors and the ZSSC4161D-01.

7.1.1.3 Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. Alternatively, the PGA can be bypassed and the sensor signal can be input directly to the ADC. The gain is adjustable for the bridge measurement task in order to provide an ADC input signal span of greater than 50% FS.

Table 6 shows the adjustable gains of the PGA, the corresponding signal spans, and the common mode range limits.

Table 6. Adjustable PGA Gains with Resulting Sensor Signal Spans and Common Mode Ranges

Nominal PGA Gain a_{PGA}	Maximum Input Span V_{IN_SPAN} [mV/V]	Input Common Mode Range V_{IN_CM} [% V_{VDDA}]
PGA bypassed	800	5 to 95
2.08	385	30 to 65
3.15	254	30 to 65
4.31	186	30 to 65
6.25	128	30 to 65
8.31	96	30 to 65
12.6	63	30 to 65
17.3	46	30 to 65
25.0	32	30 to 65
33.2	24	30 to 65
50.4	16	30 to 65
69.0	12	30 to 65
100.0	8	30 to 65
138.0	6	30 to 65
200.0	4	30 to 65

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

7.1.1.4 Analog-to-Digital Converter

The analog-to-digital converter (ADC) is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC allows adjusting the A/D conversion input voltage range shift.

7.1.2 Signal Conditioning

7.1.2.1 Internal Temperature Sensor Signal Conditioning

The internal temperature sensor signal conditioning uses ROM-resident formulas and temperature-sensor-specific coefficients stored in NVM. This calculation is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset, gain, and nonlinearity. Signal conditioning will adapt the temperature sensor element input data to the range of the normalized output format.

The conditioning coefficients for each compensation calculation are stored in the NVM during the calibration process. The coefficients are split into a 16-bit singed integer and a 4-bit unsigned weight ($c_i * 2^{w_i}$). Contact Renesas for the *Configuration Description Report* for details of the transfer function. See the last page for contact information.

7.1.2.2 Full Bridge Sensor Signal Conditioning

The full-bridge sensor element signal conditioning uses ROM-resident formulas and temperature-sensor-specific coefficients stored in NVM. This calculation is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of the temperature-dependent offset and gain and of the nonlinearity.

The conditioning coefficients for each compensation calculation are stored in the NVM during the calibration process. The coefficients are split into a 16-bit singed integer and a 4-bit unsigned weight ($c_i * 2^{w_i}$). See the *Configuration Description Report* for details of the transfer function.

All intermediate results and the final conditioning results for the full-bridge sensor is stored as signed 16-bit values (sint16, two's complement) in the RAM Output Memory. These values can be low-pass filtered and can be assigned to the I2C output registers.

7.1.2.3 Conditioning Cycle

The conditioning cycle is the sequence of equations and supervision functions processed during the Normal Operation Mode (NOM). It uses raw measurement results from measurement cycle and delivers conditioned data for output.

7.1.3 Output Interface

The ZSSC4161D-01 provides a digital interface for the output of data and status messages. The I2C controller and physical layer for I2C transmission complies with the *I2C-bus specification Rev.6 – April 4, 2014* and enables the readout of conditioned sensor signal data during NOM.

The ZSSC4161D-01 supports the following bus selection for speed in applications.

Bidirectional bus options:

- Standard-mode (Sm), which has a bit rate up to 100 kbit/s
- Fast-mode (Fm), which a bit rate up to 400 kbit/s

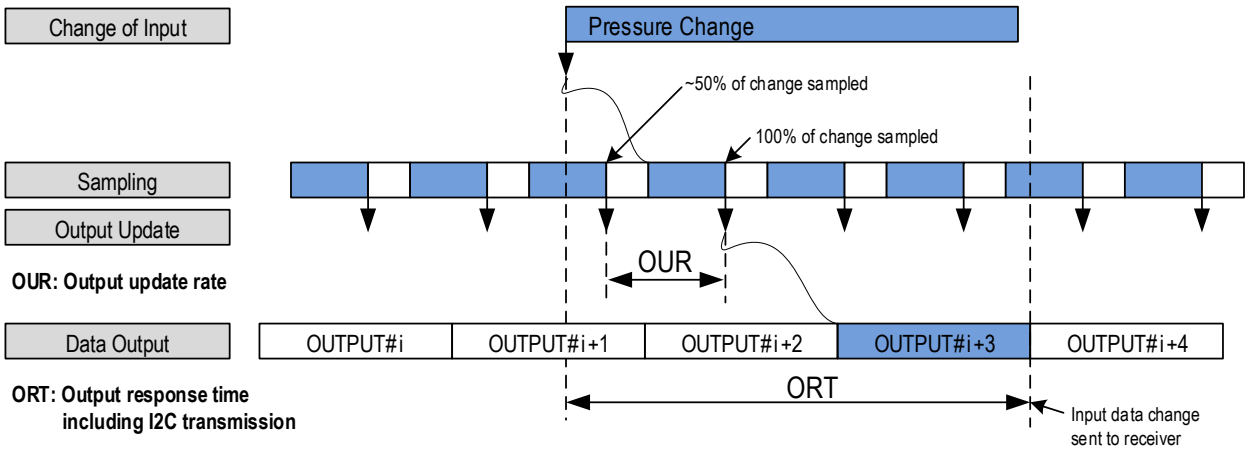
7.1.3.1 Timing Definitions

The timing for the update of the output is defined in Figure 3. The relevant timing parameters are listed in Table 7. See the OUR and ORT specifications in section 5.6 in Table 4.

Table 7. Timing Parameters

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the I2C transmission of this signal event

Figure 3. Output Update Timing Diagram



7.1.4 NVM OEM Data Memory

The ZSSC4161D-01 provides a NVM memory area for the storage of OEM data, which is physically part of the one-time programmable (OTP) NVM memory module, but it is delimited from the configuration and calibration data by dedicated commands for read and write access. Data protection and multiple-time programming data management must be implemented by the OEM.

Table 8. NVM OEM Data Memory

No.	Parameter	Number of Registers	Unit
DS_081	NVM OEM data memory (OTP)	8	16-bit words
DS_082	NVM OEM data memory (OTP) with dedicated command set	24	16-bit words

7.2 Signal Path

The ZSSC4161D-01 signal path consists of the analog front-end (AFE), the digital signal processing unit, the I2C controller, and the I2C physical interface (I2C PHY).

Table 9. Signal Path Specification

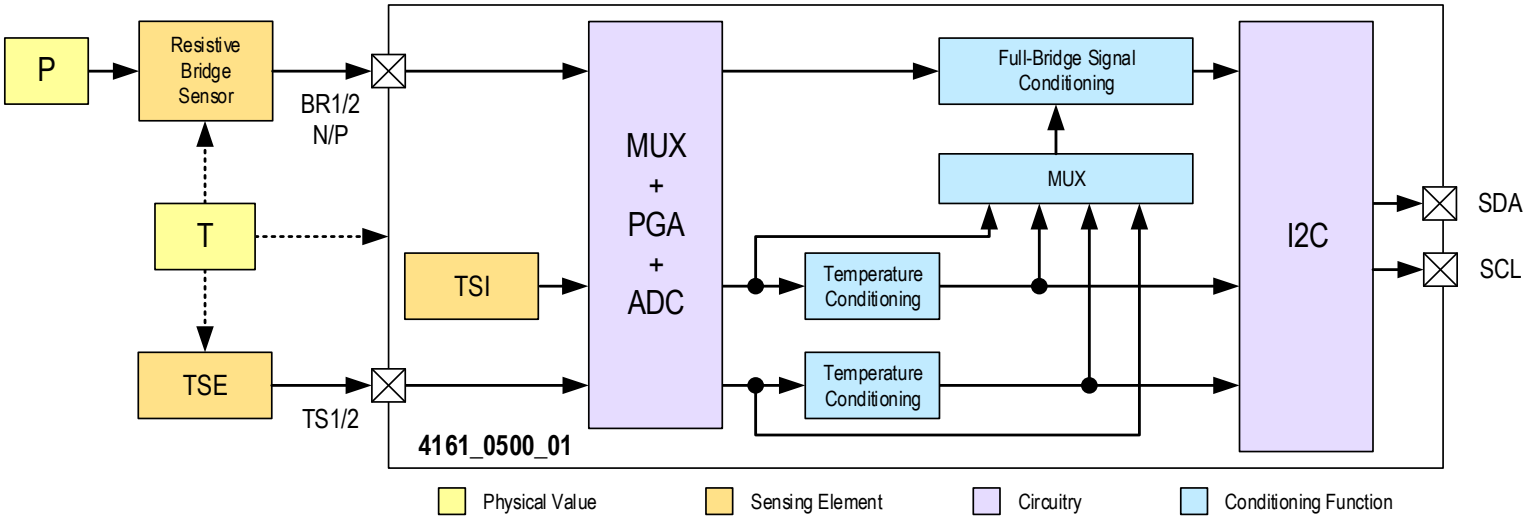
Specification	Parameter	Description
DP_040	Main Signal Path Polarity	The resistive bridge sensor element signal is input via the BR1P and BR1N or BR2P and BR2N pins and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{VDDA}/2$) so that it is possible to process positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC).

A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature is measured from the internal proportional-to-absolute-temperature (PTAT) and/or by an external diode (only one source can be used for bridge temperature compensation).

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed in the NVM during the calibration process.

During the calibration process, raw measurement values can be requested via the digital interfaces.

Figure 4. Main Signal Path (Example P1/t Sensor)



7.2.1 Full Bridge Sensor Measurement

The ZSSC4161D-01 measures a differential sensor signal (BR1P to BR1N or BR2P to BR2N); i.e. a bridge or voltage source type signal. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to ($V_{TOP} – V_{BOT}$).

The following parameter settings can be selected by the user.

- Gain: 2.1 to 200
- Range Shift: 1/16, 1/8, 1/4, or 1/2
- Input Multiplexer: BR1P/BR1N, BR1N/BR1P, BR2P/BR2N, or BR2N/BR2P
- Measurement resolution: 14 bits, 15 bits, 16 bits, 17 bits, or 18 bits

7.2.2 Internal Temperature Measurement

The ZSSC4161D-01 supports temperature measurement by chip internal PTAT sensor.

7.2.3 External Temperature Measurement

Following parameters are adjustable:

- Range Shift: 1/16 and 1/4
- Input Multiplexer: TS1 or TS2

7.2.4 Overvoltage and Short Circuit Protection

The ZSSC4161D-01 is designed for a 5V supply provided by an electronic control unit (ECU). The ZSSC4161D-01 and the connected sensor elements are protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The DOUT pin is protected from short circuits, over-voltage, and reverse polarity. These functions are described in Table 10 and are valid for operation of the ZSSC4161D-01 in the application circuit shown in section 10 within the specifications of absolute maximum ratings given in section 3.

Note: The specified junction temperature range T_J (Table 2) is in force not only for operation but also for all protection cases listed in Table 10. In the event of an over-voltage, the device might have increased power dissipation. Depending on the sensor elements and the output load, this may lead to a violation of the maximum junction temperature.

Table 10. Overvoltage, Reverse Polarity, and Short Circuit Protection

Specification	Symbol	Parameter	Description	Min	Typ	Max	Unit
Overvoltage and Reverse Polarity Protection							
DS_085	V_{VDDE_OV1}	Maximum voltage at VDDE to VSSE	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_086	V_{VDDE_OV2}	Maximum voltage at VDDE to DOUT [a]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_087	V_{DOUT_OV1}	Maximum voltage at DOUT to VSSE	Independent of resistance between VDDE and DOUT or VSSE	0		18	V
DS_088	V_{DOUT_OV2}	Maximum voltage at DOUT to VDDE[a]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_089	V_{VSSE_OV1}	Maximum voltage at VSSE to VDDE[a]	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_090	V_{VSSE_OV2}	Maximum voltage at VSSE to DOUT[a]	Independent of resistance between VDDE and DOUT or VSSE	0		18	V
Short Circuit Protection							
DS_091	$I_{VDDA\_SHRT\_VSSA}$	Current limitation in the event of a VDDA to VSSA short circuit				60	mA
DS_092	$I_{DOUT\_SHRT\_VSSE}$	Current limitation in the event of a DOUT to VSSE short circuit	Output is activated, output current limitation has been adjusted	-10		-2	mA
DS_093	$I_{DOUT\_SHRT\_VDDE}$	Current limitation in the event of a DOUT to VDDE short circuit	Output is activated, output current limitation has been adjusted	2		10	mA

[a] Reverse polarity condition.

8. Fault-Safe Operation

8.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4161D-01 and of the connected sensing elements at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described below depending on the diagnostic mode.

The ZSSC4161D-01 differentiates between two DMs with different behavior: Static Diagnostic Mode and Temporary Diagnostic Mode.

Static Diagnostic Mode

- Measurement and conditioning cycle are interrupted.
- The update of I2C output registers is stopped, and the register content is initialized with 8000_{HEX}.
- The ZACwire™ interface for one-wire communication (OWI) is enabled; both RAM output pages are readable. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing.
- The watchdog can trigger the Static Diagnostic Mode (or a full chip reset, depending on customizable settings)
- The ZSSC4161D-01 can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering (see below).
- The update of I2C output registers is continued; a fault code is available on a dedicated I2C output register.
- The ZSSC4161D-01 returns to Normal Operation Mode (NOM) including I2C transmission of valid sensor signal if fault checks do not detect continuation of fault conditions.

Fault Confirmation

The fault confirmation of the ZSSC4161D-01 is defined as follows:

- Fault confirmation is only processed for fault checks assigned to the Temporary DM.
- Fault confirmation is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.
- Fault confirmation is an up-and-down event counter that allows confirmation of a failure event.

8.2 Fault Messaging

8.2.1 Overview

The I2C interface offers two different options for fault messaging:

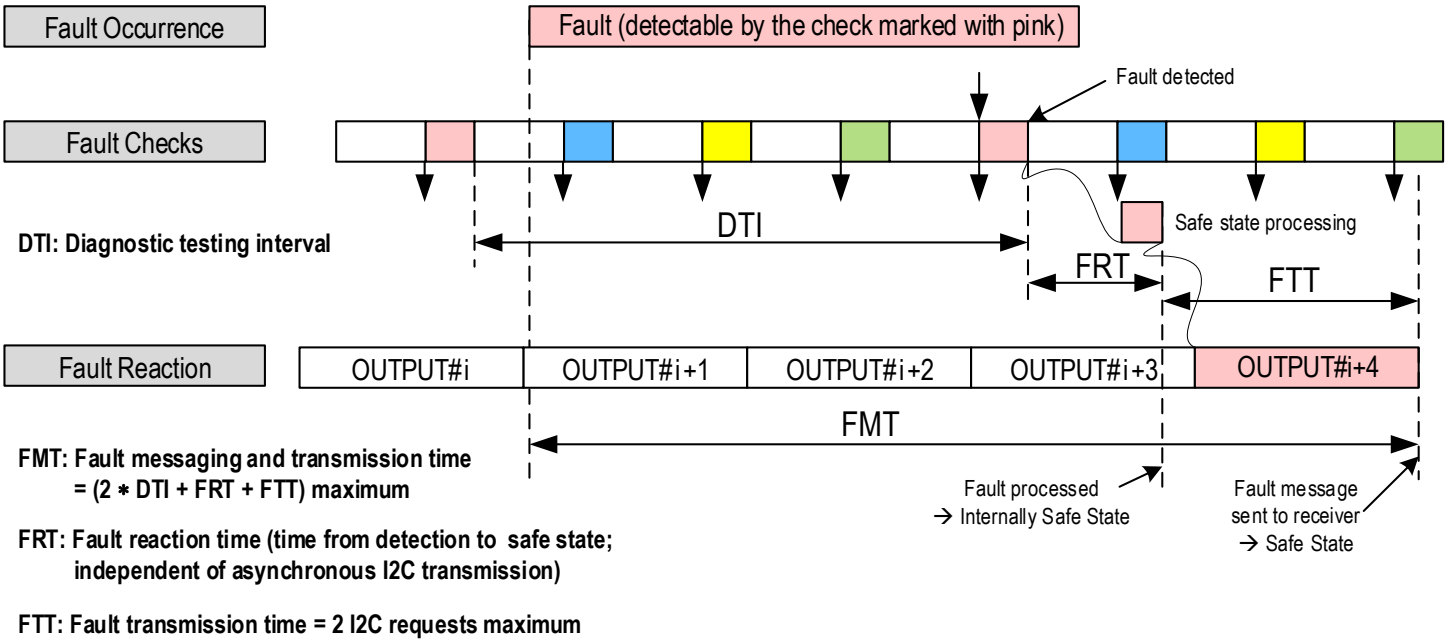
- Fault indicator bit in the data registers (bit 15 MSB indicates an active fault)
- Error code register

8.2.2 Timing Definitions

The timing for the fault messaging is defined in Figure 5. See section 5.6 in Table 4 for the fault messaging time (FMT) specifications. Refer to the *Configuration Description Report* regarding the timing for the diagnostic testing interval (DTI). This document is available on request from Renesas; see the last page for contact information.

Figure 5. Fault Messaging Timing Diagram

Note: In this figure, the different colors indicate the different fault checks processed in the cycle.



9. Fault Checks

9.1 Overview

The ZSSC4161D-01 implements basic diagnostic mechanisms. Table 11 lists the available fault checks.

Table 11. Fault Checks Overview

Specification	Identifier	Fault Check
ZSSC4161D-01 Self-Supervision Fault Checks		
DS_094	VDDAPOR	Analog supply voltage V_{VDDA} under-voltage check; power-on reset (POR)
DS_095	VDDDBOD	Digital supply under-voltage check; brownout detection (BOD)
DS_096	OSCFAIL	Oscillator-fail check based on a second oscillator/timer
DS_097	ROMCRC	ROM content CRC check
DS_098	NVMCRC	NVM content CRC check
DS_099	RAMCRC	RAM content CRC check
DS_100	RAMPRTY	RAM content parity check
DS_101	WWDG	Windowed watchdog; microcontroller and measurement and conditioning cycle active check
DS_102	INITCRC	Measurement and conditioning initialization check; processing, order, and configuration
DS_103	MCYCCRC	Measurement cycle operation check; processing, order, and configuration
	AFEMUX	AFE input multiplexer operation check
	REGCRC	Configuration register content CRC check
DS_104	CCYCCRC	Conditioning cycle operation check; processing, order, and configuration
DS_107	CHIPP	Chipping check
DS_110	ADCOFFSRNG	ADC offset range check; ADC operation check
DS_111	AFEGAIN	AFE gain check
Sensing Element Fault Checks		
DS_113	BRSC	Bridge sensor connection check
DS_114	BRSS	Bridge sensor short check
DS_115	BRSCMRNG	Bridge sensor common mode range check and sensor input leakage check
DS_116	TSI	Internal temperature sensor operation check
DS_117	TSEC	External temperature sensor connection check
Environment and Operating Condition Fault Checks		
DS_118	BRSRNGH	Bridge sensor conditioning result range check: upper limit
DS_119	BRSRNGL	Bridge sensor conditioning result range check: lower limit
DS_120	TSIRNG	Internal temperature sensor range check (over-temperature/under-temperature)
DS_121	TSERNG	External temperature sensor range check (over-temperature/under-temperature)
DS_124	CSAT	Conditioning calculation saturation check

9.2 Fault Checks for ZSSC4161D-01 Self-Supervision

The ZSSC4161D-01 provides several fault checks that supervise the ZSSC4161D-01 hardware.

Table 12. ZSSC4161D-01 Hardware Fault Checks

Note: See important notes at the end of this table.

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type
DS_094	V_{VDDA} under-voltage check (VDDAPOR); power-on reset	< 200µs	–	Always on	Static
DS_095	Digital supply under-voltage check (VDDDBOD); brownout detection	< 200µs	–	Always on	Static
DS_096	Oscillator fail check (OSCFAIL)	< 200µs	–	Always on	Static
DS_097	ROM CRC check (ROMCRC)	< FMT	–	Always on	Static
DS_098	NVM CRC check (NVMCRC)	$t_{STARTUP}$	Page-wise 16-bit CRC	Always on	Static
DS_099	RAM CRC check (RAMCRC)	< FMT	Page-wise 16-bit CRC	Always on	Static
DS_100	RAM parity check (RAMPRTY)	< FMT	–	Always on	Static
DS_101	Windowed watchdog (WWDG)	< 2 ∗ OUR	–	Always on	Static
DS_102	Initialization phase check (INITCRC)	$t_{STARTUP}$	16-bit CRC	Enable/ Disable	Static
DS_103	Measurement cycle check (MCYCCRC) including ▪ AFE input multiplexer check (AFEMUX) ▪ Register data check (REGCRC)	< FMT	16-bit CRC	Enable/ Disable	Static
DS_104	Conditioning cycle check (CCYCCRC)	< FMT	16-bit CRC	Enable/ Disable	Static

[a] "Enable/Disable" indicates that the user can enable or disable the check.

Table 13. 4161_0500_01 Operation and Cycle Fault Checks

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type
DS_107	Chipping check (CHIPP)	< FMT	–	Enable/ Disable	Static
DS_110	ADC offset check (ADCOFFSRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary
DS_111	AFE gain check (AFEGAIN)	< FMT	Lower/upper limit	Enable/ Disable	Temporary
DS_171	Bridge measurement raw data check (BRSRAW)	< FMT	Lower/upper limit	Enable/ Disable	Temporary

[a] "Enable/Disable" indicates that the user can enable or disable the check.

9.3 Fault Checks for Sensing Element Supervision

The 4161_0500_01 configuration provides several fault checks that supervise the sensing elements.

Table 14. Sensing Element Fault Checks

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type
DS_113	Full bridge sensor connection check (BRSC)	< FMT	Lower/upper limit	Enable/ Disable	Temporary
DS_114	Bridge sensor short check (BRSS)	< FMT	Lower/upper limit	Enable/ Disable	Temporary
DS_115	Bridge sensor common mode range check (BRSCMRNG) including sensor input leakage check	< FMT	Lower/upper limit	Enable/ Disable	Temporary
DS_116	Internal temperature sensor operation check (TSI)	< FMT	Lower/upper limit	Enable/ Disable	Temporary

[a] "Enable/Disable" indicates that the user can enable or disable the check.

9.4 Fault Checks for Environment and Operating Condition Supervision

The 4161_0500_01 configuration provides several fault checks that supervise the environment and operating conditions.

Table 15. Environment and Operating Condition Fault Checks

Specification	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type
DS_118	Bridge sensor range check upper limit (BRSRNGH)	< FMT	Upper limit	Enable/ Disable	Temporary
DS_119	Bridge sensor range check lower limit (BRSRNGL)	< FMT	Lower limit	Enable/ Disable	Temporary
DS_120	Internal temperature sensor range check (TSIRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary
DS_124	Saturation check for all signal conditioning (CSAT)	< 22ms	–	Enable/ Disable	Temporary

[a] "Enable/Disable" indicates that the user can enable or disable the check.

9.5 Fault Check Limit Settings

ZSSC4161D-01 provides several fault checks based on the monitoring of a physical value. A fault is detected if the measurement value exceeds or falls below a given limit. For every measurement, there are specific transfer characteristics from the monitored physical value to the measurement value. The reverse function maps a limit to a specific physical value. Because of the part-dependent measurement tolerance, a defined limit spreads out over a certain value range determined by a lower and an upper threshold. Thus a fault is securely detected as illustrated in Figure 6 if the physical value falls below the lower threshold (A) coming from the lower limit, or if it exceeds the upper threshold (D) coming from the upper limit. Otherwise it is ensured that no fault is messaged if the physical value is in the range between the upper threshold (B) coming from the lower limit and the lower threshold (C) coming from the upper limit. Table 16 shows the resulting fault detection characteristics.

Figure 6. General Fault Thresholds

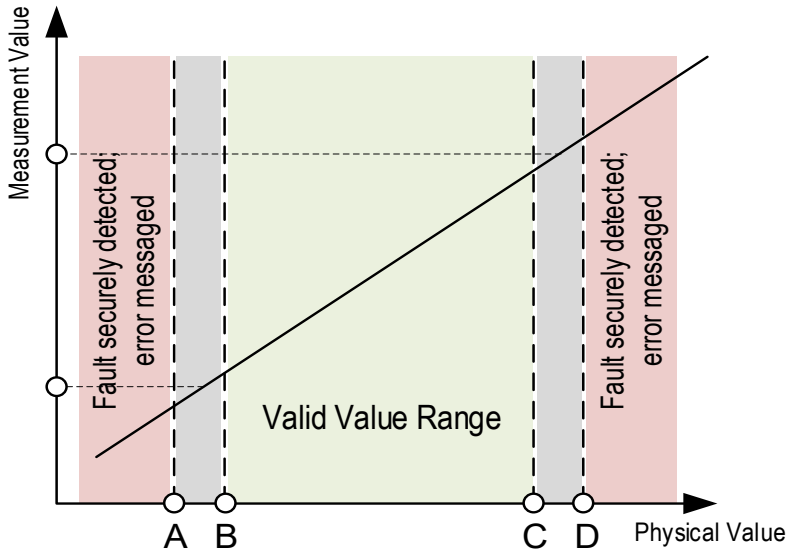


Table 16. Fault Check Threshold Definition

Threshold	Description
A	Below this threshold, the monitored physical value is erroneous; fault is securely detected and messaged.
B	Above this threshold, the monitored physical value is in the permitted range; no fault is messaged.
C	Below this threshold, the monitored physical value is in the permitted range; no fault is messaged.
D	Above this threshold, the monitored physical value is erroneous; fault is securely detected and messaged.

The 4161_0500_01 configuration provides default limits for the fault checks. These limits and the resulting thresholds are listed in Table 17.

Note that there are several fault checks which evaluate a conditioned measurement value. In this case, the specified thresholds refer directly to the conditioned value and the limits are derived from the specified target transfer function. For limit adjustments, the fault checks can be classified into three types:

- Type I – no calibration and limit adjustment necessary.
  The coefficients and limits are part of the configuration and are not allowed to change. They are silicone-related and independent from the application or the pressure sensor itself.
- Type II – calibration or limit adjustment is necessary once per application.
  The coefficients and limits needs to be evaluated on the module level once per application. After validation, they are valid for every module and can be used in production.
- Type III – calibration or limit adjustment is necessary during production.
  The coefficients or limits need to be calculated during production for every module individually.

Table 17. Fault Check Limits

Fault Check	Monitored Physical Value	Type	Default Thresholds				
			A	B	C	D	Unit
BRSS	Bridge sensor short	I	50	800	–		Ω
BRSC	Bridge sensor connection [a]				20	100	kΩ
TSI	PTAT voltage (internal temperature sensor) ADC raw data result		4		96		% FSR
TSEC	External temperature sensor connection check [b]		0.18	0.20	0.98	1.0	V
ADCOFFSRNG	ADC offset range check; ADC operation check	II	-2		2		% FSR
TSIRNG	Conditioned on-chip temperature [c], [d]		Custom				°C
TSERNG	External temperature sensor range check [b]		Custom				°C
BRSRAW	Full-bridge (differential signal) ADC raw data result		Refer to section 9.5.1.				% FSR
BRSRNG	Conditioned full-bridge sensor signal		Custom				% Data Output
BRSCMRNG	Conditioned full-bridge common mode voltage		Custom				% V_{CM}

[a] Refer to section 9.5.2 for details in application usage.

[b] By default, no external temperature sensor is activated and the fault check limits are selected to deactivate the failure detection.

[c] If absolute temperature value accuracy is relevant, an on-chip temperature calibration is necessary for accuracy better than ±3K.

[d] Limits are related to junction temperature measured with internal PTAT sensor.

9.5.1 BRSRAW

The limits of the ADC raw data check must be adjusted depending on the selected ADC resolution for the full-bridge measurement. The ADC raw data measurement register range is $[0,2^{15})$. If the resolution is higher than 14 bit, the digital zooming is activated and the range of the ADC results is different.

Table 18. BRSRAW Thresholds

ADC Resolution [bits]	ADC Result Range	Lower Limit	Upper Limit
14	$[0,2^{15})$	$0.04 \times (2^{15-1})$	$0.96 \times (2^{15-1})$
15			
16	$(-2^{15},2^{15})$	-32767	32766
17			
18			

9.5.2 BRSC

The limits for this check cannot be changed. The sensor connection check is very sensitive to bridge common mode variation. It will trigger the Temporary Diagnostic Mode if the common mode changes more than ±15% referenced to the bridge supply voltage. This behavior is not a failure and is given by system design. The fault check must be deactivated if the sensor common mode drift is higher. The application design must account for this behavior on the module development level.

10. Application Circuit and External Components

Table 19. Application Circuit Example with Full Bridge Input BR1

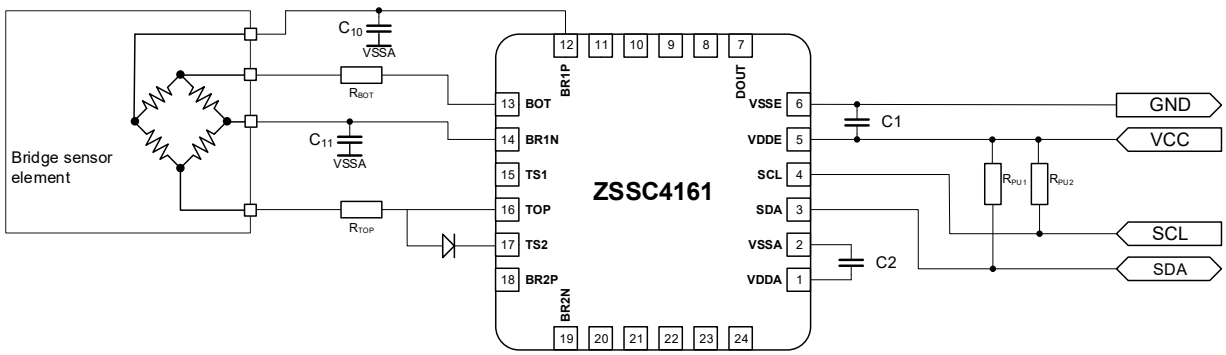
Specification	Circuit Diagram
DP_043	

Table 20. Dimensioning of External Components for the Application Example

Specification	Part	Component [a]	Component Requirements	Min	Typical	Max	Unit
DP_044	Capacitor [b]	C1	V_{MAX} ≥ 32V, SMD MLCC type		100 ± 20%	TBD	nF
	Capacitor [b]	C2	V_{MAX} ≥ 10V, SMD MLCC type		100 ± 20%	470 + 20%	nF
	Capacitor	C_{10}, C_{11}	V_{MAX} ≥ 10V, SMD MLCC type			1.2	nF
	Resistor	R_{TOP}, R_{BOT}	Resistance of R_{TOP} must be equal to R_{BOT}	0	0	$\frac{10k - R_{BR}}{2}$	Ω
	Resistor	R_{UP1}			4.7		kΩ
	Resistor	R_{UP2}			4.7		kΩ

[a] Refer to the circuit diagram in specification DP_043 for locations of components.

[b] Device is mandatory for meeting specifications described under the “Electrical Characteristics” in section 5.

Note: The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

11. ESD Protection and EMC Specification

11.1 ESD Protection

All pins have an ESD protection of up to 2kV according to the Human Body Model (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and DOUT pins have an additional ESD protection of up to 4kV (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7).

The levels of ESD protection are tested with devices in a 4 × 4 mm 24-QFN package during the product qualification.

11.2 Electromagnetic Emission

The wired emission of the externally connected pins of the ZSSC4161D-01 is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

To verify EMC performance, measurements must be performed with the application circuit described in Table 19.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN.*

11.3 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard.

To verify EMC performance, measurements must be performed with the application circuit described in Table 19; the sensor bridge element is replaced by a 3-resistor string connected to TOP, BR1P, BR1N, and BOT.

Table 21 gives the specifications for the DPI tests. RES refers to the coupling impedance. CAP refers to the injection capacitance.

Table 21. Conducted Susceptibility (DPI) Tests

Specification	Test	Frequency Range	Power [dBm]	Load Pins	Protocol	Error Band [a]	Comment
DS_169	DPI, direct coupled	1MHz to 10MHz	20dBm	VDDE	I2C	±1%	RES = 50Ω CAP= 4.7nF
DS_170	DPI, direct coupled	>10MHz	30dBm	VDDE	I2C	±1%	RES = 50Ω CAP = 4.7nF

[a] Error band regarding main signal.

12. Reliability and RoHS Conformity

The ZSSC4161D-01 is qualified according to the AEC-Q100 standard, operating temperature grade 0. Information about safety and reliability can be found in the functional safety manual.

The ZSSC4161D-01 complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded at https://www.renesas.com/eu/en/document/cer/green-products-rohs-material-declaration-certificate.

Overvoltage Conditions (18V):

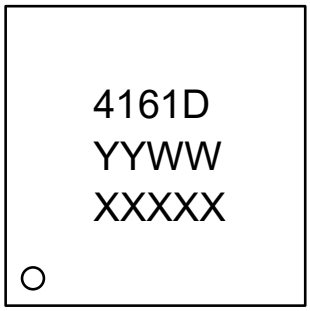
- Maximum power dissipation is $P_{max,OV}$ = 300mW; output is switched off.
- Temperature difference: T_J - T_{AMB} = 32K/W ∗ 300mW = 9.6K→ With these conditions, the maximum junction temperature T_J is ~10K greater than the ambient temperature T_{AMB}.

13. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.renesas.com/eu/en/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-085-mm-body-050mm-pitch-epad-250-x-250-mm-wettable-flank

14. Marking Diagram



Line 1: “4161D” is the truncated part number.

Line 2: “YYWW” is the last digits of the year and week that the part was assembled.

Line 3: “XXXXX” is the last digits of the lot number.

15. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
ASIL	Automotive Safety Integrity Level
BOD	Brownout Detection
BR	Bridge Sensor
CM	Command Mode
CMC	Calibration Microcontroller; optimized microcontroller architecture for Renesas signal conditioners
CMV	Common Mode Voltage
DM	Diagnostic Mode
DNL	Differential Nonlinearity
DTI	Diagnostic Testing Interval; the rate of fault check processing
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FMT	Fault Messaging Time; latency from the fault event to the completion of the transmission of the fault message
FS	Full Scale
FTT	Fault Transmission Time
HBM	Human Body Model
I/O	Input/Output
I2C	Inter-Integrated Circuit; serial two-wire data bus
INL	Integral Nonlinearity
LSB	Least Significant Bit
LSN	Least Significant Nibble
MSB	Most Significant Bit
MSN	Most Significant Nibble
MUX	Multiplexer
MTP	Multiple-Time Programmable
n.a.	Not Applicable
NOM	Normal Operation Mode
NVM	Nonvolatile Memory
OTP	One-Time Programmable
OWI	One-Wire Interface

Term	Description
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
POR	Power-On Reset
PTAT	Proportional-to-Absolute Temperature
PWR	Power Management and Protection Unit
QFN	Quad-Flat No-Leads – ZSSC4161D-01 package
RAM	Volatile Memory for Configuration and Conditioning Coefficients
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory
RTD	Resistance Temperature Device
SCCM	Sensor Check and Common Mode Adjustment Unit
SSC	Sensor Short Check (diagnostic task) or Sensor Signal Conditioner
TSI	Internal Temperature Sensor
TQE	Extended Temperature Range Identifier
ZACwire™	Renesas-specific one-wire interface (OWI)

16. Ordering Information

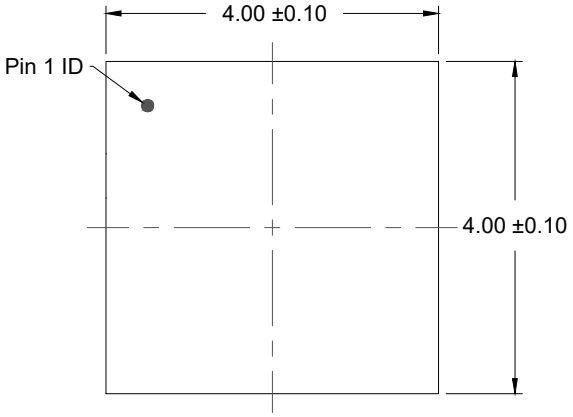
Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC4161DE1B	Single bridge input, SENT output, internal and/or external temperature measurement, tested wafer	n.a.	Wafer Boxes	-40°C to 150°C
ZSSC4161DE1C	Single bridge input, SENT output, internal and/or external temperature measurement, tested die sawn on frame	n.a.	Frame Boxes	-40°C to 150°C
ZSSC4161DE1D-ES	Single bridge input, SENT output, internal and/or external temperature measurement, tested die in waffle pack	n.a.	Waffle Pack	-40°C to 150°C
ZSSC4161DE4R	Single bridge input, SENT output, internal and/or external temperature measurement, 4 × 4 mm 24-QFN, wettable flanks (NLG24P5)	MSL1	13” Reel	-40°C to 150°C
ZSSC416XEVKV1P5	ZSSC416x SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, 10 Samples.			

17. Revision History

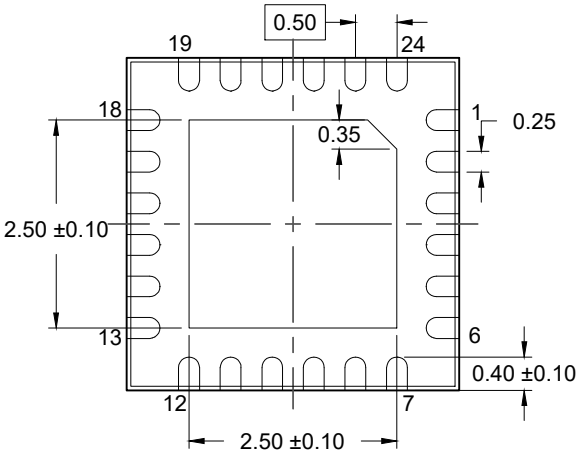
Revision Date	Description of Change
Apr 27, 2026	• Updated QFN-20L package recommendation (see “Pin Assignments”) • Split programming time into 2x parameters (see “Nonvolatile Memory”: DS_068) • Completed other minor changes
January 21, 2025	• Adding parameters A_{TSE_D}, I_{TSE_D} and V_{TSE_D} • Correcting BRSRAW Thresholds for 15bits • ZSSC4161DE4W removed
November 18, 2020	• Ordering Information updated
November 07, 2019	• Correct DS_092 and DS_093 • DP_060 changed (FMT from 10ms to 20ms)
April 18, 2019	• Update for order codes • Rename product from “ZSSC4161D” to “ZSSC4161D-01”
October 2, 2018	Initial release.

Package Outline Drawing

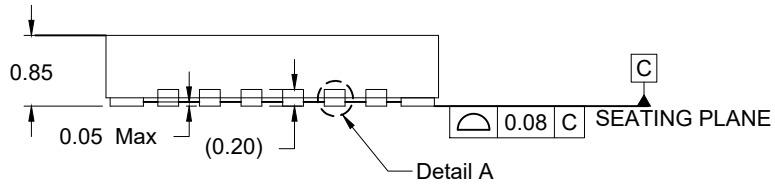
PSC-4192-05
NLG24S2
24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch
Rev.08, Jun 20, 2025



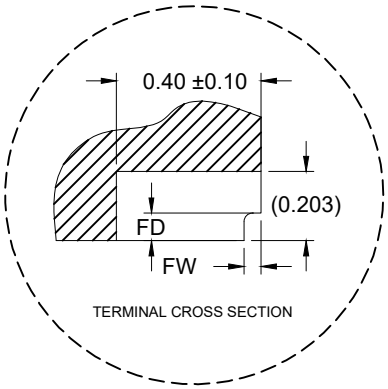
TOP VIEW



BOTTOM VIEW



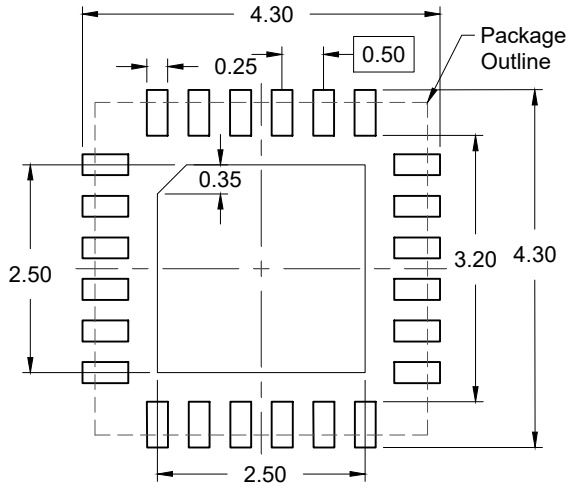
SIDE VIEW



DETAIL A

Table 1: Dimensions of wettable flank (DETAIL A)

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.010	0.075



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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