

**Brief Description**

The ZSLS7025, one of our ZSLS Family of LED control ICs, is a constant current boost converter designed for driving high-brightness LEDs. It is optimal for driving multiple white LEDs connected in series so that the LED current is uniform for better brightness and color control. The wide input voltage range and high output current enables diverse industrial, after-market automotive, and consumer lighting applications.

The ZSLS7025 output current is adjustable via an external current sense resistor and can deliver stable constant output current from a few milliamps up to 2A or higher.

The ZSLS7025 drives a constant current into the load. The control loop features a pulse frequency modulated (PFM) architecture that is inherently stable and does not need loop compensation.

The ZSLS7025 supports pulse-width modulation (PWM) or linear voltage dimming, which allows flexible control of the LED luminance.

The ZSLS7025 can operate in applications with a wide input voltage range from 5V to 100V. An integrated over-voltage protection (OVP) circuit protects the system, even under no-load conditions. The over-voltage protection is adjustable via external resistors  $R_1$  and  $R_2$ .

**Features**

- Wide application input voltage range: 5V to 100V (Higher voltage supported. See section 2.1 in the data sheet.)
- Constant current output limited only by external component selection
- No loop compensation required
- Internal over-voltage protection
- Internal over-temperature protection
- Brightness control via PWM or DC voltage control signal input
- SOP-8 package

**Benefits**

- High efficiency: up to 95%
- Minimum bill of materials
- Small form-factor package

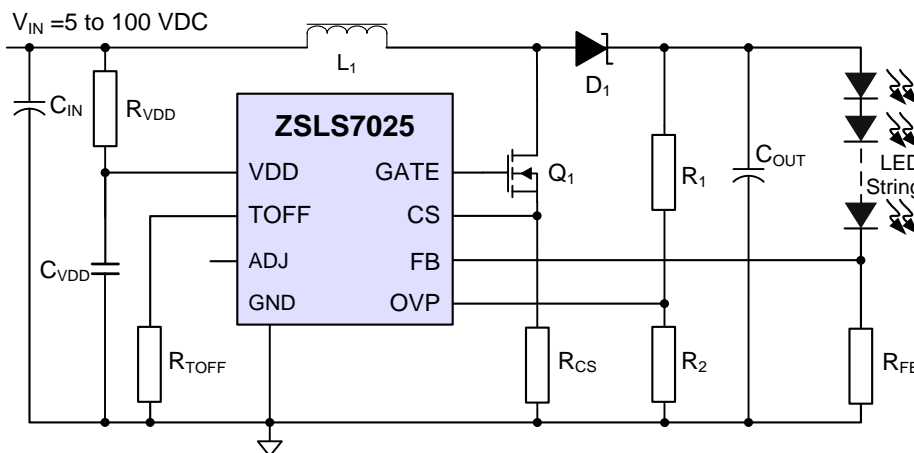
**Available Support**

- Demonstration Kit

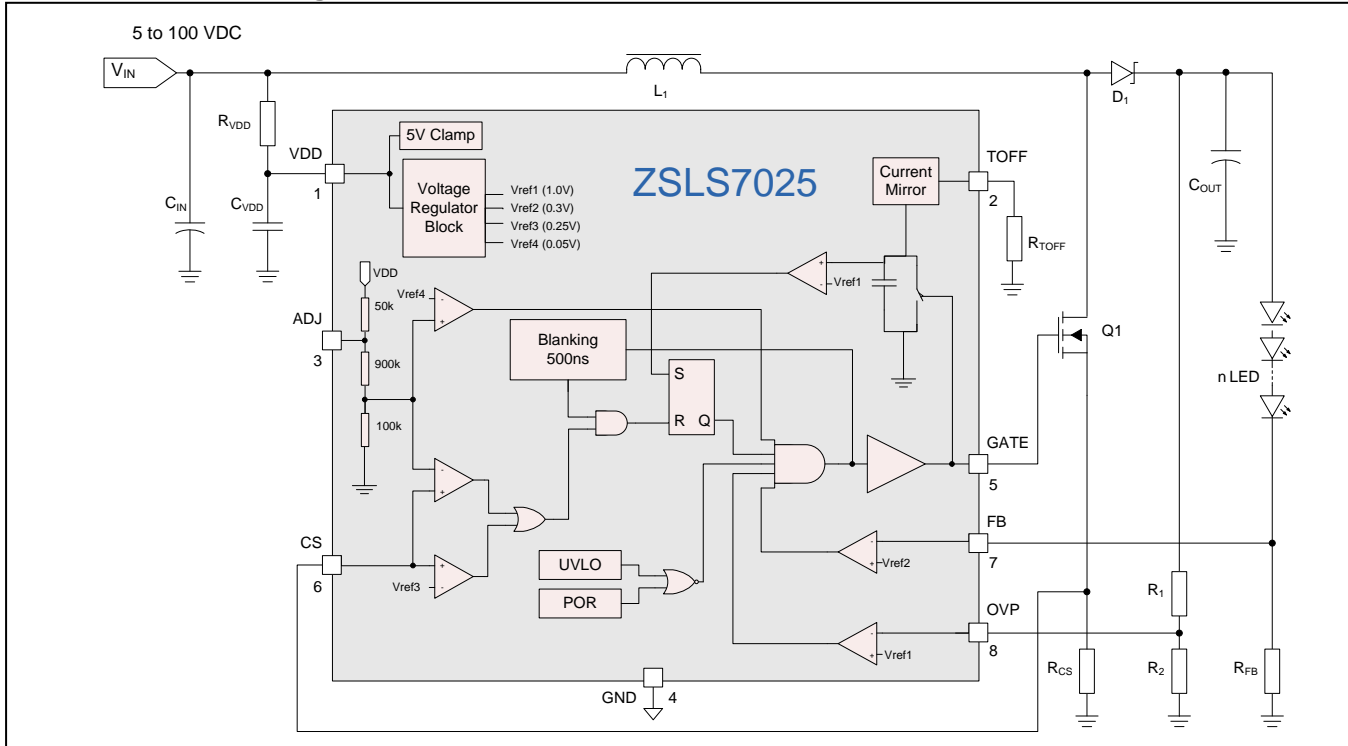
**Physical Characteristics**

- Junction temperature: -40°C to 125°C
- RoHS compliant

**ZSLS7025 Typical Application Circuit**



ZSLS7025 Block Diagram



Typical Applications

- ❖ Retro-fit Lighting
- ❖ MR16 Lights
- ❖ SELV Lighting
- ❖ Signage and Outdoor Lighting
- ❖ Architectural/Building Lighting
- ❖ Replacement Tubes
- ❖ LED Backlighting
- ❖ General Purpose Low-Voltage Industrial and Consumer Applications

Ordering Information

Product Sales Code	Description	Package
ZSLS7025ZI1R	ZSLS7025 – Boost LED Driver	SOP-8 (Tape & Reel)
ZSLS7025KIT-D1	ZSLS7025PCB-D1 Demo Board, 1 ZLED-PCB10, and 5 ZSLS7025 ICs	Kit

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# 1 IC Characteristics

Stresses beyond those listed under “Absolute Maximum/Minimum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those recommended under “Recommended Operating Conditions” (section 1.2) is not implied. Exposure to absolute–maximum conditions for extended periods may affect device reliability.

## 1.1 Absolute Maximum/Minimum Ratings

**Table 1.1 Absolute Maximum Ratings**

No.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.1.1	Voltage on VDD pin (also see specification 1.2.2 and 1.2.3)	$V_{DD}$		-0.3		6	V
1.1.2	All other pins to GND			-0.3		6	V
1.1.3	Maximum input current on VDD pin <sup>1)</sup>	$I_{DD}$				10	mA
1.1.4	ESD performance		Human Body Model			±3.5	kV
1.1.5	Junction temperature	$T_{jMAX}$		-40		150	°C
1.1.6	Storage temperature	$T_{ST}$		-65		150	°C

1) Exceeding VDD maximum input current could cause the pin to not clamp at 5V.

## 1.2 Operating Conditions

**Table 1.2 Operating Conditions**

No.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.2.1	Junction temperature	$T_{OP}$		-40		125	°C
1.2.2	Supply voltage <sup>1)</sup> (also see specification 1.1.1)	$V_{IN}$	Supply voltage connected to VDD pin via series resistor $R_{VDD}$ (see section 4.2.1)	5		100	V
1.2.3	VDD pin <sup>1)2)</sup> (also see specification 1.1.1)	$V_{DD}$	Supply voltage connected to VDD pin via series resistor $R_{VDD}$ (see section 4.2.1)	4.3		5.6	V

1) Supply voltage should be connected to the VDD pin via  $R_{VDD}$ .  
 2) Voltage set according to the clamping of the internal shunt regulator (see section 2.3).

### 1.3 Electrical Parameters

Except as noted, test conditions for the following specifications are  $V_{IN} = 10V$ ,  $R_{VDD} = 10K\Omega$ , ADJ floating, and  $T_{OP} = 25^{\circ}C$  (typical).

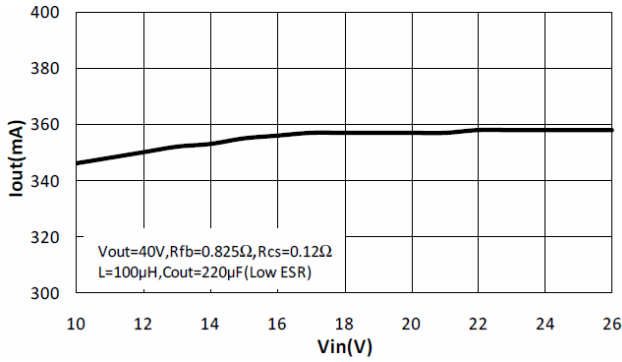
Production testing of the chip is performed at  $25^{\circ}C$  unless otherwise stated. Functional operation of the chip and specified parameters at other temperatures are guaranteed by design, characterization, and process control.

**Table 1.3** *Electrical Parameters*

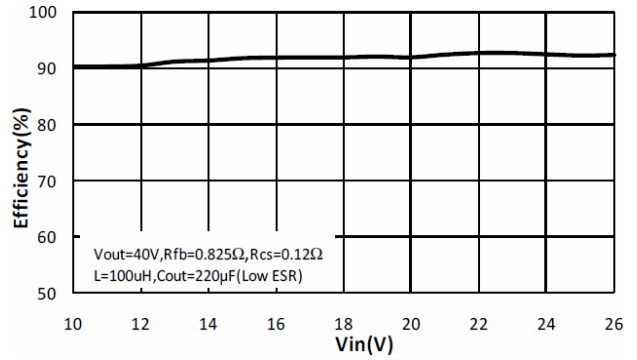
No.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.3.1	VDD pin clamp voltage	$V_{DD}$	$R_{VDD} = 10K\Omega$	4.3	5	5.6	V
1.3.2	Under-voltage threshold	$V_{UVLO\_TH}$	$V_{DD}$ rising	2.0	2.7	3.0	V
1.3.3	Under-voltage threshold hysteresis	$V_{UVLO\_HYS}$			300		mV
1.3.4	Quiescent supply current	$I_{SS}$	$V_{DD} = 5V$		250	400	$\mu A$
			$V_{DD} = 2.5V$ (under-voltage)		50	75	$\mu A$
1.3.5	Peak-current sense threshold voltage	$V_{CS\_TH}$	ADJ pin = 5V	215	240	265	mV
1.3.6	Peak current sense blanking interval	$t_{BLANK}$	$V_{CS} = V_{CS\_TH} + 50mV$		500		ns
1.3.7	Fixed turn-off interval	$t_{OFF}$	$R_{TOFF} = 250K\Omega$		10		$\mu s$
1.3.8	Peak-current control low threshold voltage	$V_{ADJ}$			0.5		V
	Peak-current control high threshold voltage				2.4		V
1.3.9	Over-temperature protection (OTP) threshold	$T_{OTP}$			125		$^{\circ}C$
1.3.10	OTP threshold hysteresis	$T_{OTP\_HYS}$			20		$^{\circ}C$
1.3.11	Internal feedback reference voltage	$V_{FB}$		0.29	0.3	0.31	V
1.3.12	Over-voltage input threshold	$V_{OVP\_TH}$		0.9	1.0	1.1	V

### 1.4 Typical Performance Characteristics Graphs

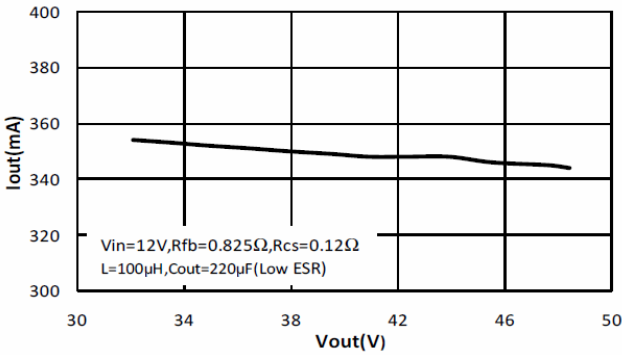
**Figure 1.1**  $V_{IN}$  vs.  $I_{OUT}$  with  $V_{OUT} = 40V$



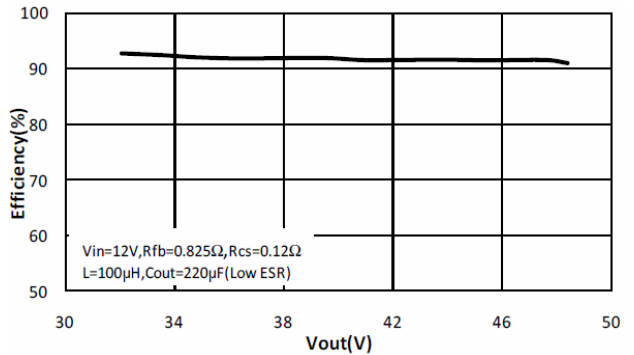
**Figure 1.2**  $V_{IN}$  vs. Efficiency with  $V_{OUT} = 40V$



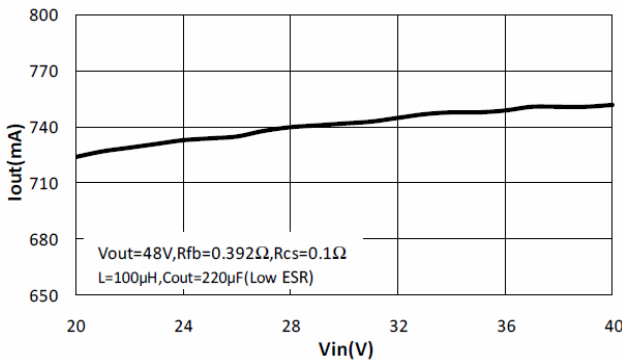
**Figure 1.3**  $V_{OUT}$  vs.  $I_{OUT}$  with  $V_{IN} = 12V$



**Figure 1.4**  $V_{OUT}$  vs. Efficiency with  $V_{IN} = 12V$



**Figure 1.5**  $V_{IN}$  vs.  $I_{OUT}$  with  $V_{OUT} = 48V$



**Figure 1.6**  $V_{IN}$  vs. Efficiency with  $V_{OUT} = 48V$

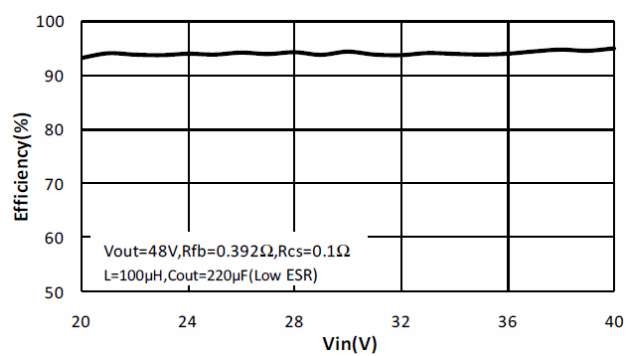


Figure 1.7  $V_{OUT}$  vs.  $I_{OUT}$  with  $V_{IN} = 24V$

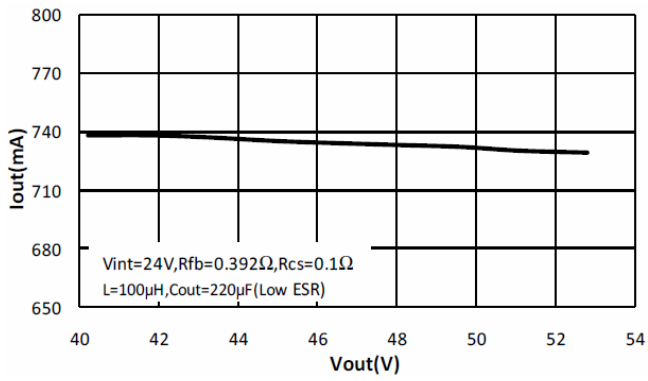
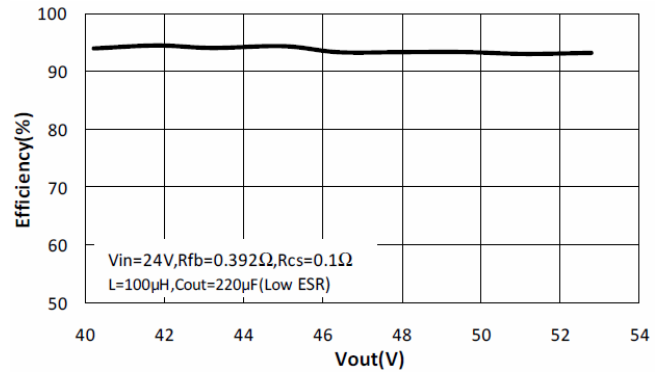


Figure 1.8  $V_{OUT}$  vs. Efficiency with  $V_{IN} = 24V$



## 2 Circuit Description

### 2.1 ZSLS7025 Overview

The ZSLS7025 is a constant current boost converter. Its output current is adjustable via an external current sense resistor, and it can deliver stable constant output current from a few milliamps up to 2A or higher.

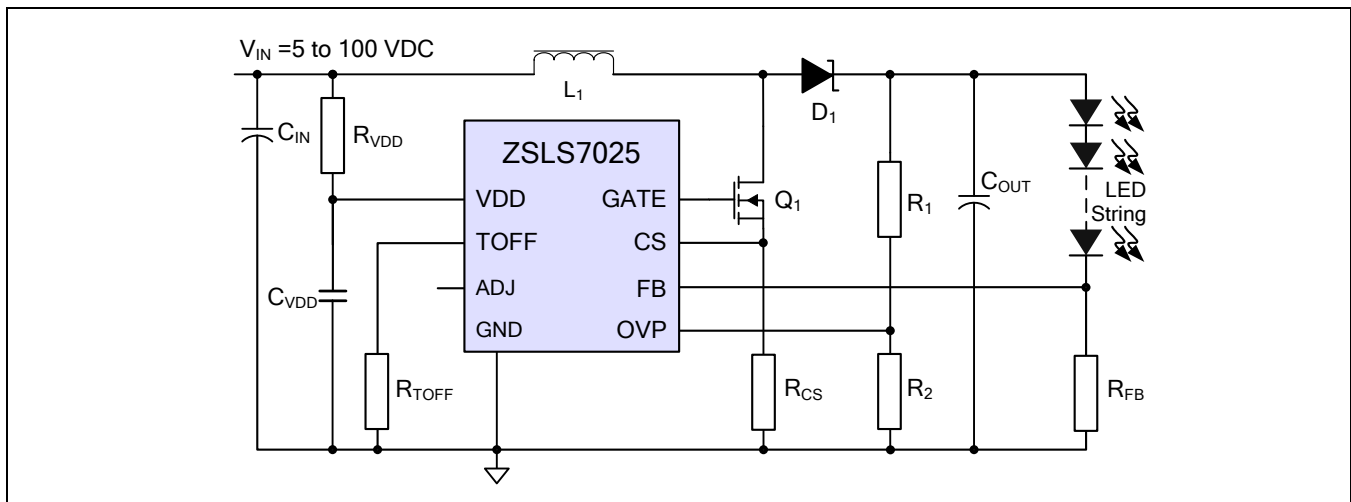
The ZSLS7025 drives a constant current into the load, automatically adjusting the output voltage according to the load. The control loop features a pulse frequency modulated (PFM) architecture that is inherently stable and does not need loop compensation.

The ZSLS7025 can operate in applications with a wide input voltage range from 5V to 100V.  $V_{IN}$  voltages above 100V can be supported if logic level MOSFETs for the higher voltage rating are available. An integrated over-voltage protection (OVP) circuit protects the system, even under no-load conditions. The over-voltage protection is adjustable via external resistors  $R_1$  and  $R_2$ . The minimum load voltage must always be higher than the maximum  $V_{IN}$ , and the drain voltage rating of the switching transistor ( $Q_1$ ) must be higher than the over-voltage shut-off limit.

Note: The ZSLS7025 has an internal 5V shunt regulator connected to the VDD pin. The  $R_{VDD}$  series resistor must be connected between the VDD pin and  $V_{IN}$  to limit current flow.

See section 4.2 for requirements for selecting the external components referred to in the following sections.

**Figure 2.1 Typical ZSLS7025 Circuit Diagram**



### 2.2 Boost Converter

The ZSLS7025's boost converter uses a peak-current mode topology. The CS pin voltage in conjunction with the current-sense resistor  $R_{CS}$  determines the peak current in the inductor ( $L_1$ ).  $Q_1$  is turned on and off by the output of an RS flip-flop that is set when the voltage on the FB pin drops below the internal threshold of 300 mV. After  $Q_1$  has been switched on, a blanking timer disables the current sense input CS to avoid immediate spurious shut-off as a result of the switching transient when  $Q_1$  discharges the parasitic capacitances on its drain node to ground. After the blanking time  $t_{BLANK}$  (see parameter 1.3.6 in section 1.3) has elapsed, the current through the inductor is sensed as a voltage drop across  $R_{CS}$ , and when the voltage reaches the peak-current sense threshold voltage  $V_{CS\_TH}$  (see parameter 1.3.5 in section 1.3), the flip-flop is reset and  $Q_1$  is turned off. Once  $Q_1$  is turned off, the inductor reverses polarity, providing the voltage boost, and the inductor current will decrease until the input voltage on the FB pin drops below the internal feedback reference voltage  $V_{FB}$ , (see parameter 1.3.11 in section 1.3).  $Q_1$  is then turned on again, and this operation repeats in each cycle.

When the input voltage on the FB pin does not exceed the internal feedback reference voltage  $V_{FB}$ , such as during start-up,  $Q_1$  will remain off for the configured minimum  $t_{OFF}$  time (see sections 2.8 and 2.9), and then it is switched on again.

### 2.3 Internal 5V Regulator

The ZSLS7025 includes an internal 5V (typical) shunt regulator connected to the VDD pin which maintains a 5V power supply for the gate driver and control circuitry. Connect  $V_{IN}$  to the VDD pin via the current limiting series resistor  $R_{VDD}$  (see section 4.2.1 for required values). Consideration should be given to the tolerances on the VDD pin operating conditions (see section 1.2, parameter 1.2.3) and  $V_{IN}$ .

### 2.4 Input Current

The current required by the ZSLS7025 is 0.25mA (typical) plus the switching current of the external MOSFET,  $Q_1$ . The switching frequency of  $Q_1$  affects the amount of current required, as does  $Q_1$ 's gate charge requirement (found in the MOSFET manufacturer's data sheet).

$$I_{IN} \approx 0.25\text{mA} + Q_G \times f_S \quad (1)$$

Where

$f_S$  = switching frequency of  $Q_1$

$Q_G$  = gate charge of  $Q_1$

### 2.5 LED Current Control

The ZSLS7025 regulates the LED current by sensing the voltage across the external feedback resistor  $R_{FB}$  in series with the LEDs. The voltage is sensed via the FB pin where the internal feedback reference voltage  $V_{FB}$  is 0.3V (typical; see section 1.3, parameter 1.3.11). The LED current can easily be set according to equation (2).

$$I_{OUT} = \frac{V_{FB}}{R_{FB}} = \frac{0.3\text{V}}{R_{FB}} \quad (2)$$

Where

$I_{OUT}$  = Average output current through the LED(s) in amperes

$V_{FB}$  = Internal feedback reference voltage

Note: For an accurate LED current, a precision resistor is required for  $R_{FB}$  (1% is recommended).

### 2.6 Dimming Control

There are three options for LED dimming:

- DC voltage dimming control
- RC-filtered PWM signal dimming control
- PWM signal with a dimming control MOSFET( $Q_2$ )

### 2.6.1 Dimming Control Using an External DC Control Signal

The LED output current can be set below the nominal average value defined by equation (2) using an external DC voltage control signal superimposed on the FB pin as shown in the example circuit in Figure 2.2. As the DC control signal,  $V_{DC}$ , increases, the current through  $R_3$  increases with a subsequent increase in the voltage at the FB pin. This causes the ZSLS7025 to compensate by reducing the output current through the LED string. Consequently, the output current is inversely proportional to the DC control voltage.

**Note:** It is important to ensure that the LED output voltage  $V_{OUT}$  remains higher than the input voltage  $V_{IN}$  in dimming applications.

The output current controlled by the DC voltage on FB can be calculated using equation (3).

$$I_{OUT} = \frac{V_{FB} - \left( \frac{R_3 \times (V_{DC} - V_{FB})}{R_4} \right)}{R_{FB}} \quad (3)$$

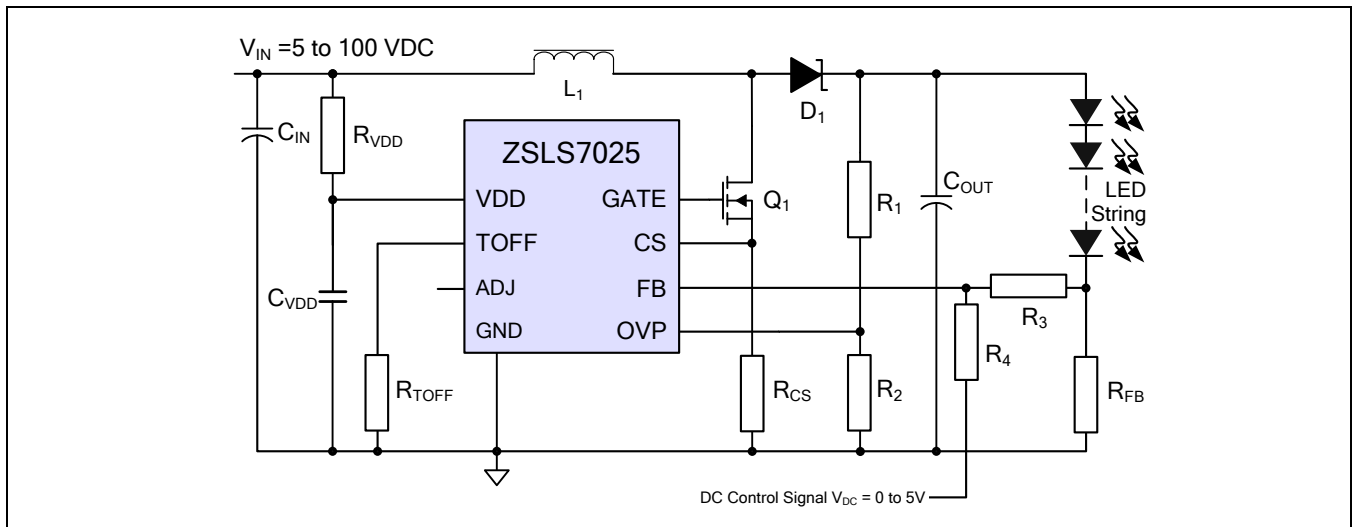
Where

$I_{OUT}$  = Output current through the LED(s) with a DC control voltage

$V_{FB}$  = Internal feedback reference voltage (see section 1.3, parameter 1.3.11)

$V_{DC}$  = External DC control voltage

**Figure 2.2 Example Circuit for Controlling Output Current via an External DC Control Voltage**



### 2.6.2 Dimming Control Using an RC Filter to Convert a PWM Signal to a DC Voltage

As shown in Figure 2.3, a filtered PWM signal can be used as an adjustable DC voltage for LED dimming control, and it functions the same as the DC control signal described in section 2.6.1. An external RC filter converts the PWM signal to a DC voltage, which is summed with the FB voltage to regulate the output current. Using a fixed frequency PWM signal and changing the duty cycle adjusts the average LED current. The LED current can be calculated with equation (4):

$$I_{OUT} = \frac{V_{FB} - \left( \frac{R_3 \times (V_{PWM} \times D_{PWM} - V_{FB})}{R_4 + R_5} \right)}{R_{FB}} \quad (4)$$

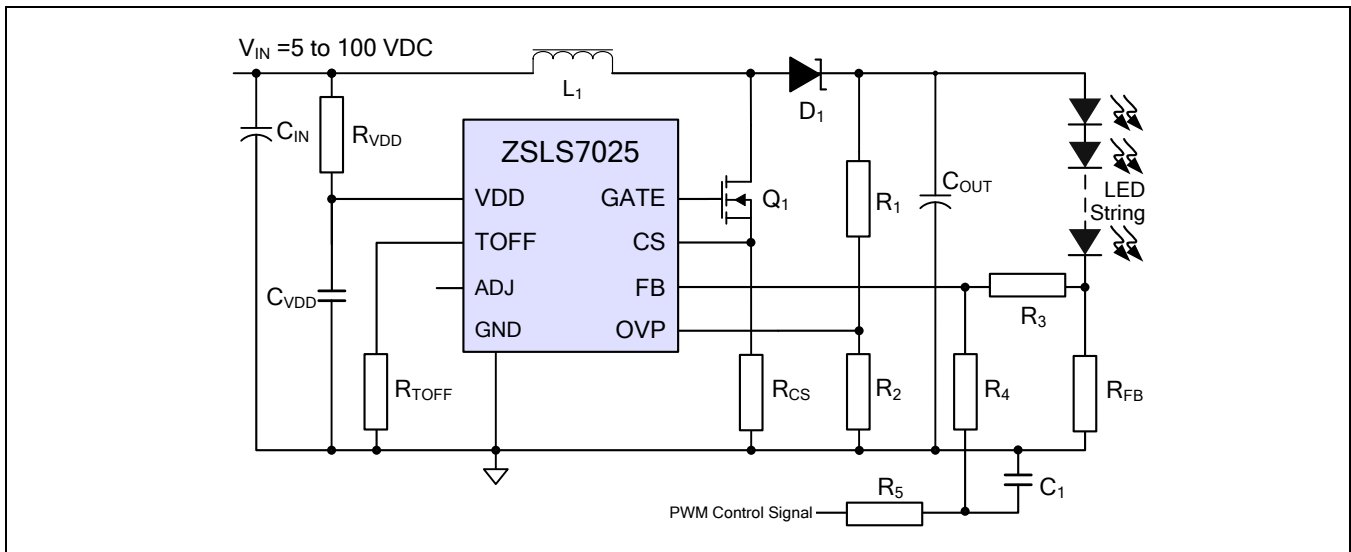
Where

- $I_{OUT}$  = Output current through the LED(s) with a PWM control voltage
- $V_{FB}$  = Internal feedback reference voltage (see section 1.3, parameter 1.3.11)
- $V_{PWM}$  = External PWM control voltage
- $D_{PWM}$  = Duty cycle of the PWM control signal

The LED current is inversely proportional to the PWM duty cycle; i.e., when the PWM signal has a 100% duty cycle, the output current is minimum, ideally zero, and when the PWM signal has a 0% duty cycle, the output current is at its maximum. See the example in section 4.4 for more details.

Note: Care must be taken to ensure that the minimum required current is not already exceeded when the LEDs are connected to  $V_{IN}$ .

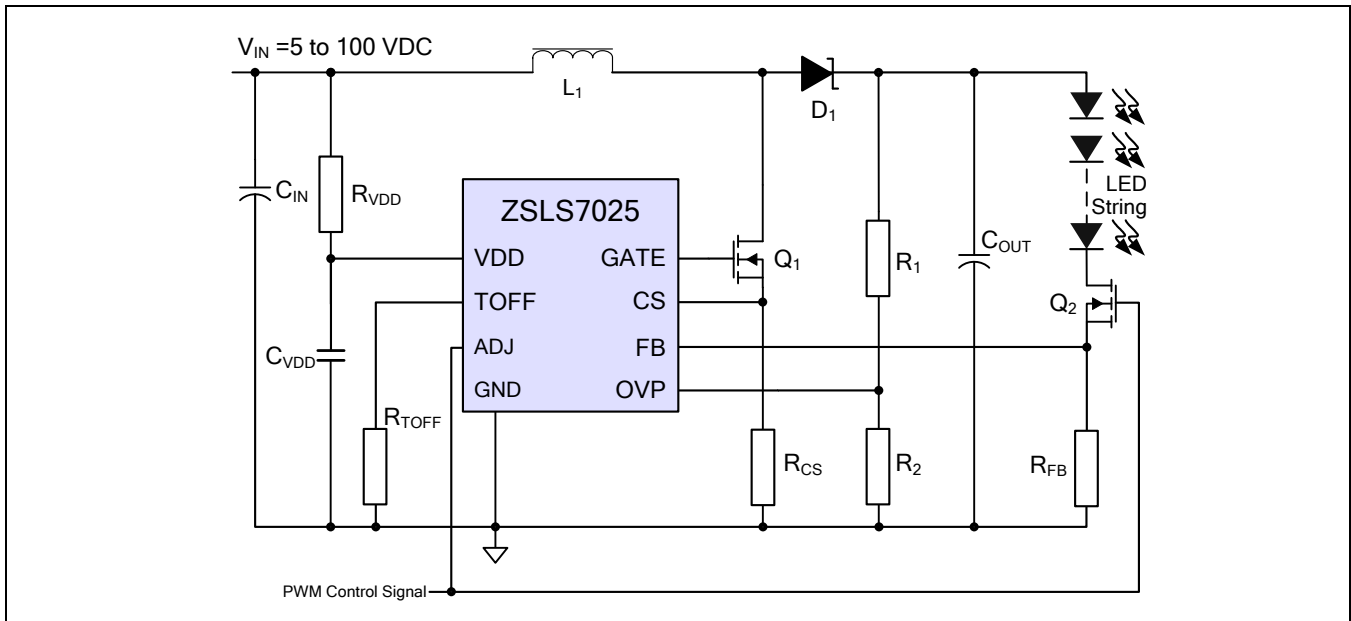
**Figure 2.3 RC Filter PWM Dimming Circuit**



### 2.6.3 PWM Dimming with a Dimming Control MOSFET (Q<sub>2</sub>)

Figure 2.4 shows the configuration for using an external PWM signal with a dimming control MOSFET Q<sub>2</sub>. When the PWM input is high (V<sub>H</sub>>2.4V), Q<sub>2</sub> is on and the ZSLS7025 operates normally to regulate the output current. When the PWM signal is low (V<sub>L</sub><0.5V), Q<sub>2</sub> is off; the input voltage on the FB pin will be below V<sub>FB</sub> and the ZSLS7025 is shutdown. Using a fixed frequency PWM signal and changing the duty cycle adjusts the average LED current. The recommended 5V PWM frequency is between 200Hz and 1KHz.

Figure 2.4 PWM Dimming Circuit Using a Dimming Control MOSFET (Q<sub>2</sub>)



### 2.7 Peak Input Current Control

The ZSLS7025 limits the peak inductor current and therefore the peak input current through the feedback path of R<sub>CS</sub> connected from the source of the external MOSFET (Q<sub>1</sub>) to ground. The required average input current is based on the boost ratio V<sub>OUT</sub>/V<sub>IN</sub> and the designed value for average LED current. The required average input current can be calculated with equation (5):

$$I_{IN\_AVG} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{5}$$

Where

η = Assumed power conversion efficiency (recommended value for calculation: 0.9)

In general, setting the peak inductor current to 1.5 times the average input current is sufficient to maintain good regulation of the output current.

$$I_{IN\_PEAK} = 1.5 \times I_{IN\_AVG} = \frac{V_{CS\_TH}}{R_{CS}} \tag{6}$$

Where

$$V_{CS\_TH} = V_{ADJ}/10 \text{ if } 0.5V < V_{ADJ} \leq 2.4V \text{ or}$$

$$V_{CS\_TH} = 0.24V \text{ if } V_{ADJ} > 2.4V \text{ or if the ADJ pin is floating}$$

### 2.8 Setting the Minimum Off-Time $t_{OFF\_MIN}$

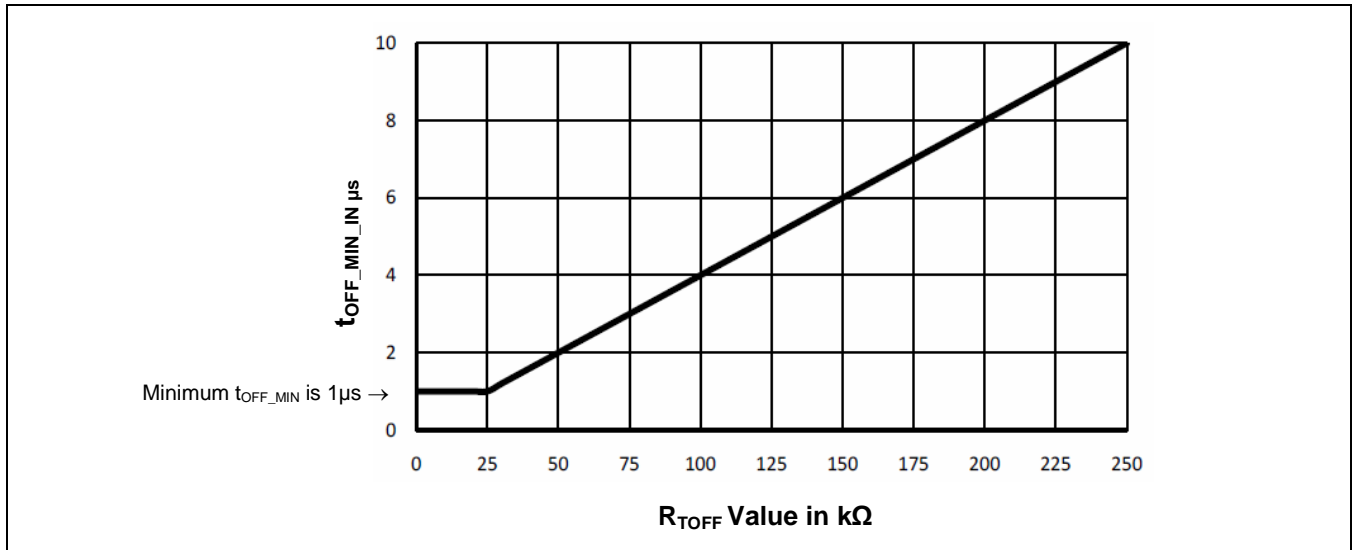
The ZSLS7025 operates in a pulsed frequency modulation (PFM) mode. In nominal operation, on-time and off-time are determined according to equations (8), (9), (10), and (11). In most applications, the recommended value for  $t_{OFF\_MIN}$  is 1 $\mu$ s. The relationship between  $t_{OFF\_MIN}$  and  $R_{TOFF}$  is shown in equation (7) and Where  $t_{OFF\_MIN}$  is in  $\mu$ s and  $R_{TOFF}$  is in  $\Omega$ .

Figure 2.5.  $t_{OFF\_MIN}$  is valid as long as  $V_{FB}$  has not reached the threshold of 300 mV.

$$t_{OFF\_MIN} = 40 \times 10^{-12} \times R_{TOFF} \tag{7}$$

Where  $t_{OFF\_MIN}$  is in  $\mu$ s and  $R_{TOFF}$  is in  $\Omega$ .

**Figure 2.5** Minimum Off-Time  $t_{OFF\_MIN}$  vs.  $R_{TOFF}$



### 2.9 Switching Frequency and Inductor Value

The inductance value of the inductor ( $L_1$ ) directly determines the switching frequency of the converter. Under fixed conditions, the inductance is inversely proportional to the switching frequency; i.e., the larger the inductance, the lower the switching frequency. A higher switching frequency will reduce the value required for the inductor but will increase the switching loss in the external MOSFET,  $Q_1$  (see section 2.4).

The switching frequency  $f$  in Hertz can be calculated from  $t_{ON}$  and  $t_{OFF}$  in seconds with equation (8).

$$f = \frac{1}{(t_{ON} + t_{OFF})} \quad (8)$$

The ripple current in the inductor can be calculated with equation (9).

$$I_{RIPPLE} = 2 \times (I_{IN\_PEAK} - I_{IN\_AVG}) \quad (9)$$

The  $Q_1$  on-time,  $t_{ON}$ , can be calculated with equation (10).

$$t_{ON} \approx \frac{(I_{RIPPLE} \times L_1)}{V_{IN} - I_{IN\_AVG} \times (R_L + R_{DS(ON)} + R_{CS})} \quad (10)$$

Where

$R_L$  = the DC resistance of inductor  $L_1$  in  $\Omega$

$R_{DS(ON)}$  = the on-resistance of  $Q_1$  in  $\Omega$  (see manufacturer's specifications)

$L_1$  = the value of the inductor  $L_1$  in Henries

The  $Q_1$  off-time,  $t_{OFF}$ , can be calculated with equation (11).

$$t_{OFF} \approx \frac{I_{RIPPLE} \times L_1}{V_{OUT} + V_D + (I_{IN\_AVG} \times R_L) - V_{IN}} \quad (11)$$

Where

$V_D$  = the forward voltage of the diode  $D_1$  at the required load current in volts

Note: The selection of inductor  $L_1$  must ensure that  $t_{OFF}$  is longer than the  $t_{OFF\_MIN}$  as calculated in equation (7). If not, the converter cannot output the required current.

The recommended switching frequency is  $20\text{kHz} < f < 200\text{kHz}$ . Lower than  $20\text{kHz}$  will cause audio noise of the inductor, and a frequency that is too high will increase the switching loss in  $Q_1$ .

With a fixed  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{IN\_AVG}$ , and  $I_{IN\_PEAK}$ , the switching frequency is inversely proportional to the inductor value.

## 2.10 DC Power Loss

The  $R_{DS(ON)}$  of the external MOSFET,  $Q_1$ , determines the DC power loss, which can be calculated with equation (12).

$$P_{DISS} \approx I_{IN\_AVG}^2 \times R_{DS(ON)} \times D_{Q1} \approx I_{IN\_AVG}^2 \times R_{DS(ON)} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{1}{\eta} \quad (12)$$

Where

$D_{Q1}$  = the duty cycle for  $Q_1$

$\eta$  = Assumed power conversion efficiency (recommended value for calculation: 0.9)

### 3 Operating Conditions

#### 3.1 Under-Voltage Lockout

The under-voltage lockout (UVLO) function monitors the voltage on the ZSLS7025's VDD pin. If this voltage is lower than the UVLO threshold minus the UVLO hysteresis ( $V_{UVLO\_TH} - V_{UVLO\_HYS}$ ), the ZSLS7025 is disabled.

If the voltage on the VDD pin reaches a level higher than the UVLO threshold ( $V_{UVLO\_TH}$ ), the lock-out function turns off and the ZSLS7025 is re-enabled. See parameters 1.3.2 and 1.3.3 in section 1.3 for the  $V_{UVLO\_TH}$  threshold and  $V_{UVLO\_HYS}$  hysteresis, respectively.

#### 3.2 Over-Voltage Protection

Open-load protection is achieved through the ZSLS7025's over-voltage protection (OVP). In boost converters, an LED string failure can cause the feedback voltage ( $V_{FB}$ ) to always be zero. If this happens, the ZSLS7025 will keep boosting the output voltage higher and higher. If the output voltage reaches the programmed OVP threshold, the protection mechanism will be triggered and stop the switching action. To ensure that the circuit functions properly, the OVP setting resistor divider,  $R_1$  and  $R_2$ , must be set with appropriate values given by equation (13). The recommended OVP voltage is either 1.25 times the normal output voltage or 5V higher than the normal output voltage, whichever is higher.

$$V_{OVP} = V_{OVP\_TH} \times \frac{(R_1 + R_2)}{R_2} \tag{13}$$

Where

$V_{OVP\_TH}$  = Over-voltage input threshold: 1.0V (typical; see parameter 1.3.12 in section 1.3)

$V_{OVP}$  = Output voltage OVP level

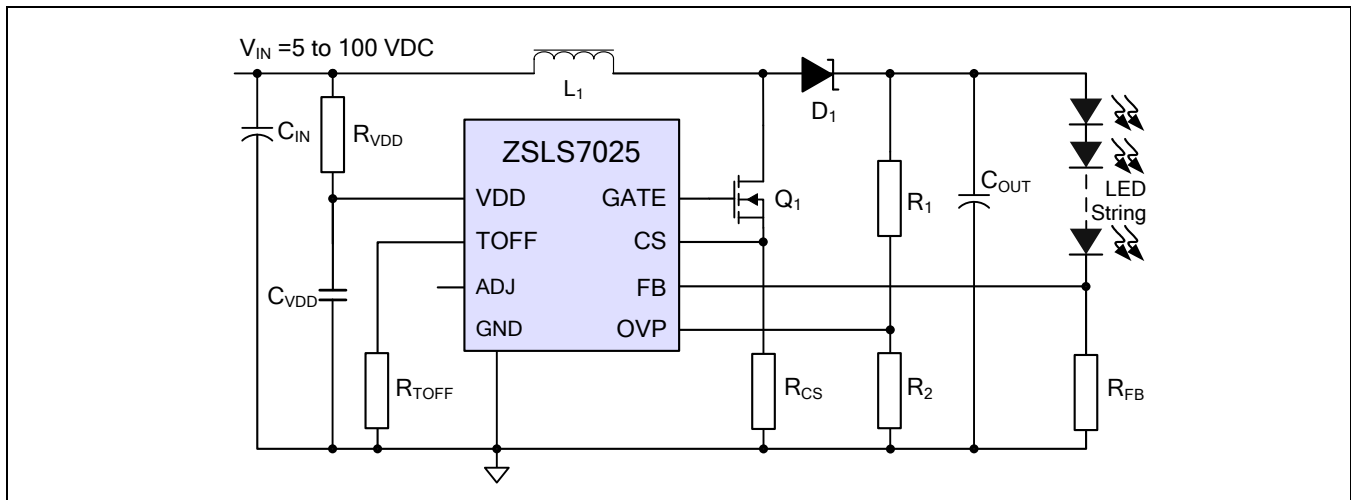
## 4 Application Circuit Design

### 4.1 Applications

The ZSLS7025 is ideal for driving white HB-LEDs in diverse industrial, after-market automotive, and consumer lighting applications using low supply voltages, such as SELV applications. It is optimal for driving multiple white HB-LEDs connected in series so that the LED current is uniform for better brightness and color control. It features a wide input range and high output current.

Figure 4.1 demonstrates the typical application with the external components described in section 4.2. Figure 2.2, Figure 2.3, and Figure 2.4 demonstrate various dimming applications.

**Figure 4.1 Typical ZSLS7025 Application Circuit**



### 4.2 External Component Selection

Note: Also see section 4.3 for layout guidelines for the following external components.

#### 4.2.1 Series Resistor $R_{VDD}$

The ZSLS7025 has an internal 5V shunt regulator connected to the VDD pin. The  $R_{VDD}$  series resistor must be connected between the VDD pin and  $V_{IN}$  to limit current flow. See section 2.1 regarding input voltages over 100V.

#### 4.2.2 Inductor $L_1$

See section 2.9 for calculating the proper value for  $L_1$ . Select an inductor with a current rating higher than the input average current and a saturation current over the calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum total LED current. Also ensure that the inductor has a low DCR (copper wire resistance) to minimize the  $I^2R$  power loss.

#### 4.2.3 High Frequency Noise Filter Capacitor $C_{VDD}$

External capacitor  $C_{VDD}$  forms a high-frequency noise filter for the VDD pin. For all configurations, use  $C_{VDD}$  to bypass the VDD pin using a low ESR capacitor (a 10 $\mu$ F ceramic capacitor is recommended) to provide a high frequency path to GND.

#### 4.2.4 Input Capacitor $C_{IN}$

The  $C_{IN}$  input capacitor connected to  $V_{IN}$  will supply the transient input current for the power inductor. A value of 100 $\mu$ F or higher is recommended to prevent excessive input voltage ripple. Also see section 4.2.3.

#### 4.2.5 Output Capacitor $C_{OUT}$ for Reducing Output Ripple

The output capacitor ( $C_{OUT}$ ) holds the output current while the  $Q_1$  external MOSFET turns ON. This capacitor directly impacts the line regulation and the load regulation.

Using a low ESR capacitor can minimize output ripple voltage and improve output current regulation. For most applications, a 220 $\mu$ F low ESR capacitor will be sufficient. Proportionally lower ripple can be achieved with higher capacitor values.

#### 4.2.6 Schottky Rectifier Diode $D_1$

The  $D_1$  external diode for the ZSLS7025 should be a Schottky diode with a low forward voltage drop and fast switching speed. The diode's average current rating must exceed the application's average output current. The diode's maximum reverse voltage rating must exceed the over-voltage protection of the application. For PWM dimming applications, note the reverse leakage of the Schottky diode. Lower leakage current will drain the output capacitor less during PWM low periods, allowing for higher PWM dimming ratios.

#### 4.2.7 External MOSFET $Q_1$

The  $Q_1$  external MOSFET must have a  $V_{DS}$  rating that exceeds the maximum over-voltage protection (OVP) level configured for the application. The  $V_{GS(th)}$  of the MOSFET should be not higher than 4V. The MOSFET's current rating must be higher than the input peak current ( $I_{IN\_PEAK}$ ). Determine the power dissipation within  $Q_1$  and check if the thermal resistance of the MOSFET package causes the junction temperature to exceed maximum ratings. Also see section 2.10 regarding the effect of the MOSFET  $R_{DS(ON)}$  on DC power loss.

### 4.3 Application Circuit Layout Requirements

The guidelines in this section are strongly recommended when laying out application circuits. As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If the layout is not well-designed, the regulator could show instability as well as EMI problems. For additional guidelines, refer to the IDT application note *PCB Layout Design Guidelines for LED Driver Circuits* available at <http://www.IDT.com>.

- Wide traces should be used for connection of the high current loop to minimize the EMI and unnecessary loss.
- The external components ground should be connected to the ZSLS7025 ground and should be as short as possible. It is especially important that the  $R_{FB}$  ground to ZSLS7025 ground connection is as short and wide as possible to have an accurate LED current.
- The capacitors  $C_{IN}$ ,  $C_{VDD}$ , and  $C_{OUT}$  should be placed as close as possible to the ZSLS7025 for good filtering. It is especially important that the  $C_{OUT}$  output capacitor connection is as short and wide as possible.
- The  $Q_1$  external MOSFET drain is a fast switching node (also applies to  $Q_2$  if the PWM is accomplished with a dimming control MOSFET as described in section 2.6.3). The inductor  $L_1$  and Schottky diode  $D_1$  should be placed as close as possible to the drain, and the connection should be kept as short and wide as possible. Avoid other traces crossing and routing too long in parallel with this node to minimize the noise coupling into these traces. The feedback pins (i.e., CS, FB, OVP) should be as short as possible and routed away from the inductor, Schottky diode, and  $Q_1$ . The feedback pins and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
- The thermal pad on the back of the external MOSFET package must be soldered to the large ground plane for ideal heat distribution.

### 4.4 Application Example

This section provides an example of an application design for the ZSLS7025 for the RC-filter PWM application described in section 2.6.2 and shown again for reference in Figure 4.2.

Design criteria:

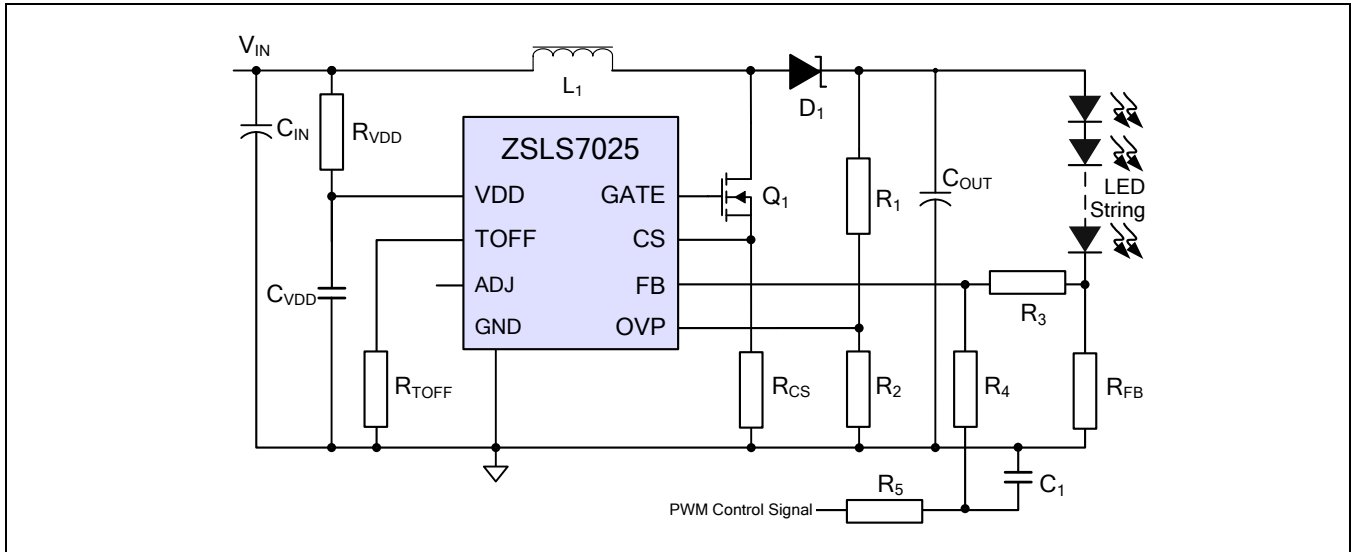
$$V_{IN} = 12 \text{ to } 24 \text{ V}$$

$$I_{OUT} = 350\text{mA}$$

$$V_{OUT} = 30 \text{ to } 40\text{V} \text{ (9 to 12 LEDs, } V_f = 3.3\text{V)}$$

To calculate the worst case parameters, use the minimum input voltage, maximum output voltage, and maximum output current; i.e.,  $V_{IN} = 12\text{V}$ ,  $I_{OUT} = 350\text{mA}$ , and  $V_{OUT} \approx 40\text{V}$  (12 LEDs,  $V_f = 3.3\text{V}$ ).

Figure 4.2 Application Design Example – RC Filter PWM Dimming Circuit



#### 4.4.1 Selecting $R_{VDD}$ , $C_{IN}$ , and $C_{VDD}$

Assume  $I_{IN} = 2.5\text{mA}$ .

$$R_{VDD} = \frac{V_{IN} - V_{DD}}{I_{IN}} \approx 3\text{k}\Omega \quad (14)$$

→ Choose  $C_{IN}$  as  $220\mu\text{F}/35\text{V}$  and  $C_{VDD}$  as  $10\mu\text{F}/16\text{V}$ .

#### 4.4.2 Selecting $R_{TOFF}$ to Set Minimum $t_{OFF}$

The recommended value for  $t_{OFF\_MIN}$  is  $1\mu\text{s}$ .

$$t_{OFF\_MIN} = 40 \times 10^{-12} \times R_{TOFF} = 1\mu\text{s} \quad (15)$$

→ Choose  $R_{TOFF} = 24\text{k}\Omega$ .

#### 4.4.3 Selecting $R_{FB}$ to Set Output Current and $C_3$

$$R_{FB} = \frac{V_{FB\_TH}}{I_{OUT}} \approx 0.86\Omega \quad (16)$$

→ Choose  $C_3 = 220\mu\text{F}/63\text{V}$  (low ESR electrolytic capacitor).

#### 4.4.4 Selecting R<sub>3</sub>, R<sub>4</sub>, R<sub>5</sub> and C<sub>1</sub>

R<sub>3</sub>, R<sub>4</sub>, and R<sub>5</sub> can be obtained by

$$I_{OUT} = \frac{V_{FB} - \left( \frac{R_3 \times (V_{PWM} \times D_{PWM} - V_{FB})}{R_4 + R_5} \right)}{R_{FB}} \quad (17)$$

Substitute D<sub>PWM</sub>=100%, V<sub>PWM</sub>= 5V, and I<sub>OUT</sub>=0 in the equation, and the result is

$$0 = \frac{0.3 - \left( \frac{R_3 \times (5 \times 100\% - 0.3)}{R_4 + R_5} \right)}{0.86} \quad (18)$$

which can be simplified to

$$15.66 \times R_3 = R_4 + R_5$$

The low pass filter formed by R<sub>5</sub> and C<sub>1</sub> must have a corner frequency much lower than the PWM frequency. As the corner frequency of the filter decreases, the response time of the LED current to changes in PWM increases. Choose a corner frequency 50 times lower than f<sub>PWM</sub>.

$$R_5 \times C_1 \geq \frac{50}{2\pi f_{PWM}} \quad (19)$$

Assume f<sub>PWM</sub> is 200Hz (or higher) and choose C<sub>1</sub> = 0.1μF, and the result is R<sub>5</sub> ≥400kΩ.

→ Choose C<sub>4</sub> = 0.1μF, R<sub>5</sub> = 400kΩ.

Choose a nominal value for R<sub>4</sub>, and then calculate R<sub>3</sub>.

→ Choose R<sub>4</sub> = 10kΩ, then R<sub>3</sub> = 26.2kΩ.

Substitute D<sub>PWM</sub>=0, V<sub>PWM</sub>= 5V and I<sub>OUT</sub>= 350mA in the equation, and the result is

$$I_{OUT} = \frac{V_{FB} - \left( \frac{R_3 \times (V_{PWM} \times D_{PWM} - V_{FB})}{R_4 + R_5} \right)}{R_{FB}} = \frac{0.3 - \left( \frac{26.2 \times (5 \times 0\% - 0.3)}{400 + 10} \right)}{R_{FB}} = 0.35A \quad (20)$$

So, R<sub>FB</sub> =0.91Ω. (With the RC filter PWM dimming, R<sub>FB</sub> will be different than in the no dimming application shown in Figure 2.1.)

#### 4.4.5 R<sub>CS</sub> for Setting Input Peak Current

Assume that

$$\begin{aligned} I_{IN\_PEAK} &= 1.5 \times I_{IN\_AVG} = 1.5 \times \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \\ &= 1.5 \times \frac{40 \times 0.35}{12 \times 0.9} \approx 1.95A \end{aligned} \quad (21)$$

Where  $\eta$  is the assumed power conversion efficiency (the recommended value for this calculation is 0.9)

$$R_{CS} = \frac{V_{CS\_TH}}{I_{IN\_PEAK}} = 0.123\Omega \quad (22)$$

→ Choose  $R_{CS} = 0.123\Omega$ ,  $I_{IN\_PEAK} = 1.95A$

#### 4.4.6 L<sub>1</sub> for Setting the Frequency

Input average current:

$$I_{IN\_AVG} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} = 1.3A \quad (23)$$

The ripple current in the inductor:

$$I_{RIPPLE} = 2 \times (I_{IN\_PEAK} - I_{IN\_AVG}) = 1.3A \quad (24)$$

According to  $t_{OFF} > t_{OFF\_MIN}$ :

$$t_{OFF} = \frac{I_{RIPPLE} \times L_1}{V_{OUT} + V_D + (I_{IN\_AVG} \times R_L) - V_{IN}} > 1\mu s \quad (25)$$

This gives  $L_1 > 22\mu H$ .

Assume  $L_1 = 22\mu H$  and  $R_L + R_{DS(ON)} + R_{CS} = 0.4\Omega$

$$t_{ON} = \frac{(I_{RIPPLE} \times L_1)}{V_{IN} - I_{IN\_AVG} \times (R_L + R_{DS(ON)} + R_{CS})} \approx 2.5\mu s \quad (26)$$

Then the assumed switching frequency:

$$f' = \frac{1}{(t_{ON} + t_{OFF})} \approx 285kHz \quad (27)$$

The recommended switching frequency,  $20\text{kHz} < f < 200\text{kHz}$ , according to the switching frequency, is inversely proportional to the inductor value; for example, select  $L_1=100\ \mu\text{H}$ .

Therefore

$$f = f' \times \frac{22}{100} \approx 63\text{kHz} \quad (28)$$

The saturation current of the inductor must exceed the input peak current ( $I_{\text{IN\_PEAK}}$ ).

#### 4.4.7 $R_1$ and $R_2$ for Setting OVP

Set  $V_{\text{OVP}} = V_{\text{OUT}} + 5\text{V} = 45\text{V}$

$$V_{\text{OVP}} = V_{\text{OVP\_TH}} \times \frac{(R_1 + R_2)}{R_2} \quad (29)$$

→Choose  $R_2 = 10\text{k}\Omega$ , then  $R_1 = 470\text{k}\Omega$ .

#### 4.4.8 $Q_1$ External MOSFET and $D_1$ Diode

Power losses in the  $Q_1$  external MOSFET should be minimized. Conduction losses increase with  $R_{\text{DS(on)}}$ , and switching losses increase with gate/drain charge and frequency. Therefore, selecting a MOSFET with low  $R_{\text{DS(on)}}$  and low gate/drain charge for the  $Q_1$  external MOSFET will help to optimize efficiency.

The MOSFET's current rating must be higher than the input peak current  $I_{\text{IN\_PEAK}}$ .  $Q_1$  must have a  $V_{\text{DS}}$  rating that exceeds the maximum over-voltage protection (OVP) level configured for the application.

The average and peak current of the diode  $D_1$  must exceed the output average current and input peak current. The diode's maximum reverse voltage rating must exceed the over-voltage protection of the application.

## 5 ESD Protection

All pins have an ESD protection of  $\geq \pm 3500V$  according to the Human Body Model (HBM). The ESD test follows the Human Body Model based on MIL 883-H, Method 3015.8.

## 6 Pin Configuration and Package

Figure 6.1 ZSLS7025 Pin Assignments

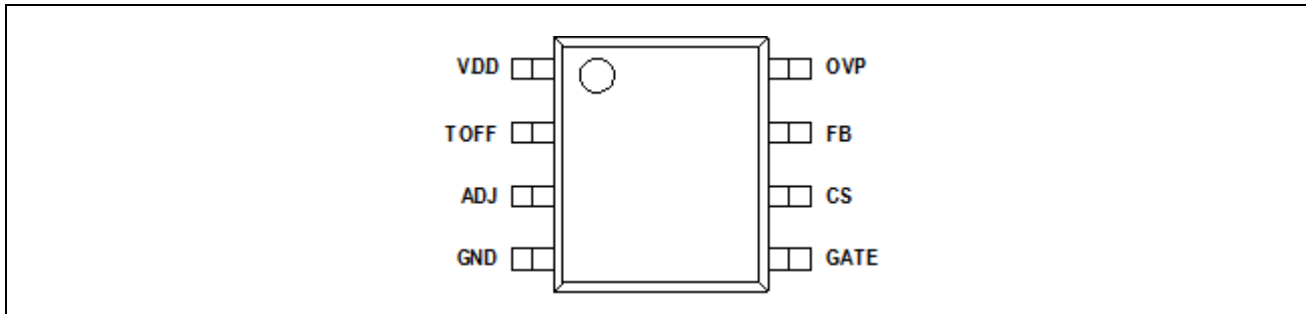
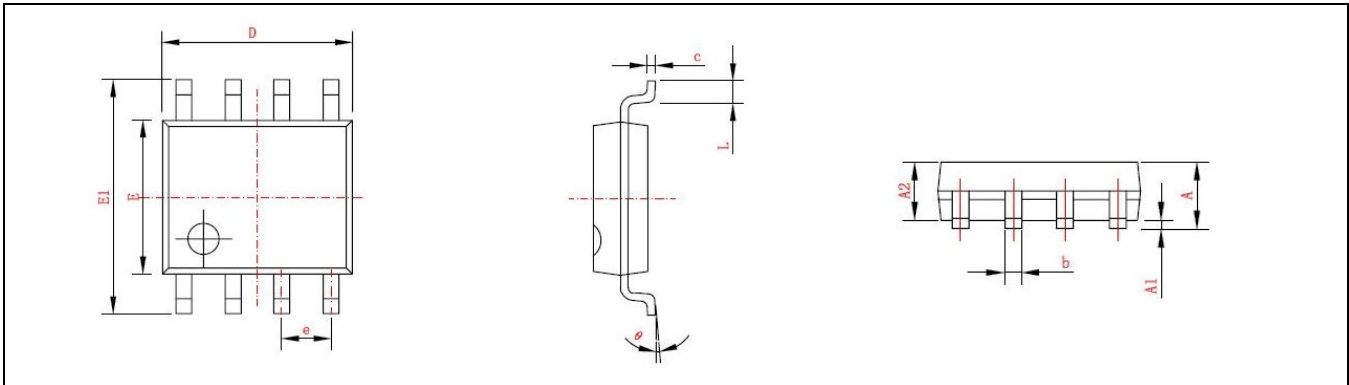


Table 6.1 Pin Description SOP-8

Pin Name	NO.	Description
VDD	1	Positive power supply input pin. Internally clamped at 5V (typical).
TOFF	2	Pin for setting off time. An external resistor, $R_{TOFF}$ , connected to this pin forms an RC discharge path to generate the constant minimum off time of the $Q_1$ external MOSFET.
ADJ	3	Enable and input peak current control pin. This pin is pulled up to 4.5V internally to set $V_{CS\_TH} = 0.24V$ if ADJ is floating. If $V_{ADJ} < 0.5V$ , the $Q_1$ external MOSFET shuts down. If $0.5 \leq V_{ADJ} \leq 2.4V$ , $V_{CS\_TH} = V_{ADJ}/10$ . If $V_{ADJ} > 2.4V$ , $V_{CS\_TH} = 0.24V$ .
GND	4	Ground.
GATE	5	Driver's output for the gate of the $Q_1$ external MOSFET.
CS	6	Current sense input for the boost, peak-current control loop.
FB	7	Feedback voltage input pin. Used to regulate the current of the LEDs by keeping $V_{FB} = 0.3V$ .
OVP	8	Overvoltage protection input pin. If the voltage at OVP exceeds the over-voltage input threshold, $V_{OVP\_TH}$ , the GATE output shuts down.

Figure 6.2 SOP-8 Package Dimensions and Pin Assignments



SOP-8 Package Dimensions (mm, except $\theta$ )			
<b>A</b>	1.550 ± 0.200	<b>E</b>	3.900 ± 0.100
<b>A1</b>	0.175 ± 0.075	<b>E1</b>	6.000 ± 0.200
<b>A2</b>	1.450 Typical	<b>e</b>	1.270 Typical
<b>b</b>	0.420 ± 0.090	<b>L</b>	0.835 ± 0.435
<b>c</b>	0.214 ± 0.036	<b><math>\theta</math></b>	4° ± 4°
<b>D</b>	4.900 ± 0.200		

## 7 Glossary

Term	Description
HB	High Brightness
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
RS Flip-Flop	Reset-Set Flip-Flop
UVLO	Under-Voltage Lockout

## 8 Ordering Information

Product Sales Code	Description	Package
ZSLS7025ZI1R	ZSLS7025 – Boost LED Driver	SOP-8 (Tape & Reel)
ZSLS7025KIT-D1	ZSLS7025PCB-D1 Demo Board, 1 ZLED-PCB10, and 5 ZSLS7025 ICs	Kit

## 9 Document Revision History

Revision	Date	Description
1.00	June 28, 2012	First issue.
	April 20, 2016	Changed to IDT branding.

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