# X80000, X80001

## Smart Power Plug™ Penta-Power Sequence Controller with Hot Swap

FN8148
Rev 0.00
March 18, 2005

The X80000 contains three major functions: a power communications controller, a power sequencing controller, and a hotswap controller.

The power communications controller allows smart power supply control via the backplane using the SMBus protocol. The system can check for voltage, current, and manufacturing ID compliance before board insertion. The power distribution network can monitor the status of the negative voltage supply, DC voltage supplies, and hardshort events by accessing the Fault Detection Register and General Purpose EEPROM of the device. Each device has a unique slave address for identification.

The power sequencer controller time sequences up to five DC-DC modules. The X80000 allows for various hardwired configurations, either parallel or relay sequencing modes. The power good, enable and voltage good signals provide for flexible DC-DC timing configurations. Each voltage enable signal has a programmable delay. In addition, the voltage good signals can be monitored remotely via the fault detection register (thru the SMBus).

The hot swap controller allows a board to be safely inserted and removed from a live backplane without turning off the main power supply. The X80000 family of devices offers a modular, power distribution approach by providing flexibility to solve the hotswap and power sequencing issues for insertion, operations, and extraction. Hardshort Detection and Retry with Delay, Noise filtering, Insertion Overcurrent Bypass, and Gate Current selection are some of the programmable features of the device.

During insertion, the gate of an external power MOSFET is clamped low to suppress contact bounce. The undervoltage/overvoltage circuits and the power on reset circuitry suppress the gate turn on until the mechanical bounce has ended. The X80000 turns on the gate with a user set slew rate to limit the inrush current and incorporates an electronic circuit breaker set by a sense resistor. After the load is successfully charged, the PWRGD signal is asserted; indicating that the device is ready to power sequence the DC-DC power bricks.

## Features

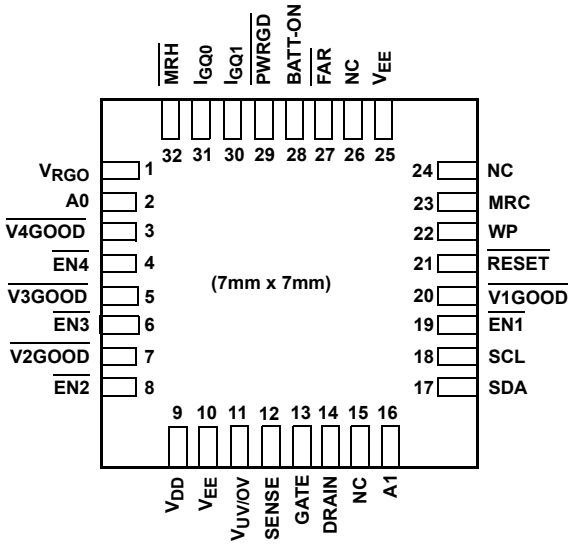
- Integrates Three Major Functions
  - Smart Power Plug communications
  - Programmable power sequencing
  - Programmable Hot Swap controller
- Smart Power Plug™
  - Intelligent board insertion allows verification of board and power supply resources prior to system insertion.
  - Fault detection register records the cause of the faults
  - Soft extraction
  - Soft re-insertion
  - Remote gate shutdown/turn on
  - Power ID/manufacturing ID memory (2kb of EEPROM)
- Programmable Power Sequencing
  - Sequence up to 5 DC/DC converters.
  - Four independent voltage enable pins
  - Four programmable time delay circuits
  - Soft Power Sequencing - restart sequence without power cycling.
- Hot Swap Controller
  - Programmable overvoltage and undervoltage protection
  - Undervoltage lockout for battery/redundant supplies
  - Programmable slew rate for external FET gate control
  - Electronic circuit breaker - overcurrent detection and gate shut-off
  - Programmable overcurrent limit during Insertion
  - Programmable hardshort retry with retry failure flag
  - Typically operates from -30V to -80V. Tolerates transients to -200V (limited by external components)
- Available Packages
  - 32-lead Quad No-Lead Frame (QFN)

## Applications

- -48V Hot Swap Power Backplane/Distribution Central Office, Ethernet for VOIP
- Card Insertion Detection
- Power Sequencing DC-DC/Power Bricks
- IP Phone Applications
- Databus Power Interfacing
- Custom Industrial Power Backplanes
- Distributed Power Systems

## Pinout

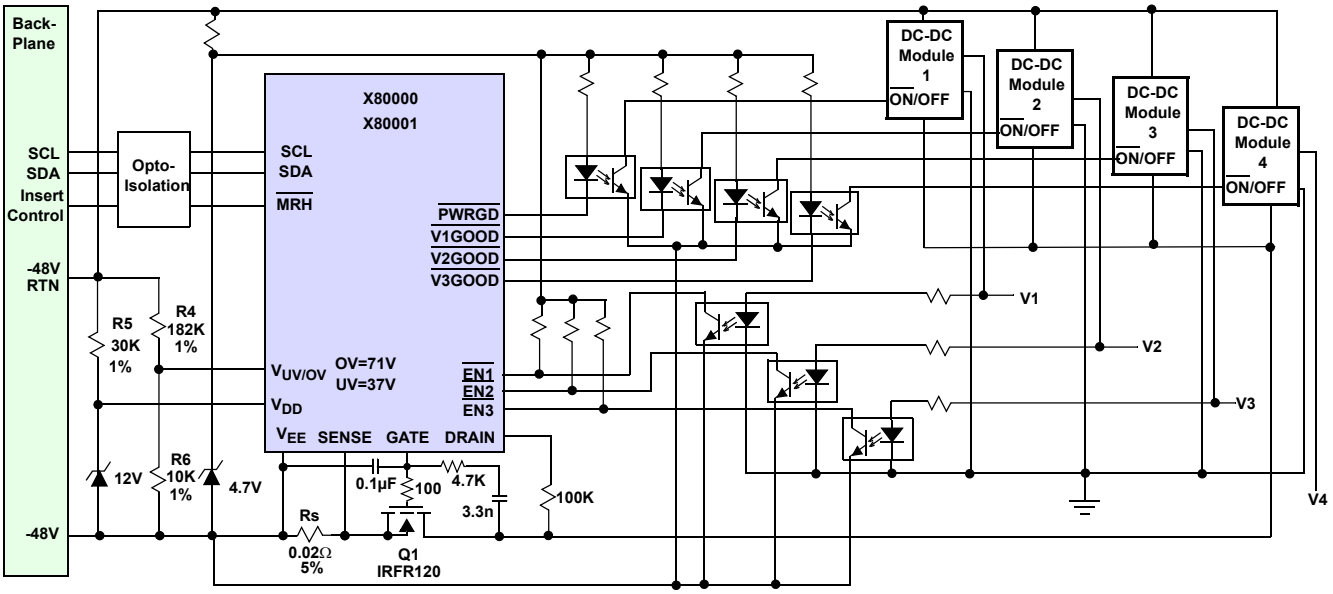
**X80000, X80001**
**(7X7 QFN)**
TOP VIEW




## Ordering Information

| PART NUMBER | OV | UV1 | UV2 | TEMP RANGE | PKG | PART MARK |
|---|---|---|---|---|---|---|
| X80000Q32I | 74.9 | 42.4 | 33.2 | I | 32 Ld QFN | 80000I |
| X80001Q32I | 68.0 | 42.4 | 33.2 | I | 32 Ld QFN | 80001I |

## Typical Application



## Absolute Maximum Ratings

Temperature under bias . . . . . –65°C to +135°C
Storage temperature . . . . . –65°C to +150°C
Voltage on given pin (Hot Side Functions):
- $V_{ov/uv\ pin}$ . . . . . 5.5V + $V_{EE}$
- SENSE pin . . . . . 400mV + $V_{EE}$
- $V_{EE}$ pin . . . . . -80V
- DRAIN pin . . . . . 48V + $V_{EE}$
- PWRGD pin . . . . . 7V + $V_{EE}$
- GATE pin . . . . . $V_{DD}$ + $V_{EE}$
- FAR pin . . . . . 7V + $V_{EE}$
- MRH pin . . . . . 5.5V + $V_{EE}$
- BATT_ON pin . . . . . 5.5V + $V_{EE}$

Voltage on given pin (Cold Side Functions):
- ENi pins (i = 1 to 4) . . . . . 5V
- ViGOOD pins (i = 1 to 4) . . . . . 5.5V + $V_{EE}$
- RESET pin . . . . . 5.5V + $V_{EE}$
- SDA, SCL, WP, A0, A1 pins . . . . . 5.5V + $V_{EE}$
- MRC pin . . . . . 5.5V + $V_{EE}$
- IGQ1 and IGQ0 pins . . . . . 5.5V + $V_{EE}$
- $V_{DD}$ pin . . . . . 14V + $V_{EE}$

D.C. output current . . . . . 5mA
Lead temperature (soldering, 10 seconds) . . . . . 300°C

## Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to 85°C
Supply Voltage ($V_{DD}$) . . . . . 12V

*CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Specifications Standard Settings

Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $V_{DD}$ | Supply Operating Range | | 10 | 12 | 14 | V |
| $I_{DD}$ | Supply Current | | | 2.5 | 5 | mA |
| $V_{RGO}$ | Regulated 5V output | $I_{RGO}$ = 10µA | 4.5 | | 5.5 | |
| $I_{RGO}$ | $V_{RGO}$ current output | | | | 50 | µA |
| $I_{GATE}$ | Gate Pin Current | Gate Drive On, $V_{GATE} = V_{EE}$, $V_{SENSE} = V_{EE}$ (sourcing) | 46.2 | 52.5 | 58.8 | µA |
| | | $V_{GATE} - V_{EE}$ = 3V $V_{SENSE}-V_{EE}$ = 0.1V (sinking) | | 9 | | mA |
| $V_{GATE}$ | External Gate Drive (Slew Rate Control) | $I_{GATE}$ = 50µA | $V_{DD}$-0.01 | | $V_{DD}$ | V |
| $V_{PGA}$ | Power Good Threshold (PWRGD High to Low) | Referenced to $V_{EE}$ $V_{UV1} < V_{UV/OV} < V_{OV}$ | 0.9 | 1 | 1.1 | V |
| $V_{IHB}$ | Voltage Input High (BATT_ON) | | $V_{EE}$ + 4 | | $V_{EE}$ + 5 | V |
| $V_{ILB}$ | Voltage Input Low (BATT_ON) | | | | $V_{EE}$ + 2 | V |
| $I_{LI}$ | Input Leakage Current (MRH, MRC) | $V_{IL}$ = GND to $V_{CC}$ | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current (V1GOOD, V2GOOD, V3GOOD, V4GOOD, RESET) | All ENi = $V_{RGO}$ for i = 1 to 4 | | | 10 | µA |
| $V_{IL}$ | Input LOW Voltage (MRH, MRC, IGQ0, IGQ1) | | -0.5 + $V_{EE}$ | | ($V_{EE}$ + 5) x 0.3 | V |
| $V_{IH}$ | Input HIGH Voltage (MRH, MRC, IGQ0, IGQ1) | | ($V_{EE}$ + 5) x 0.7 | | ($V_{EE}$ + 5) + 0.5 | V |

## Electrical Specifications Standard Settings

Over the recommended operating conditions unless otherwise specified. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage ($\overline{RESET}$, $\overline{V1GOOD}$, $\overline{V2GOOD}$, $\overline{V3GOOD}$, $\overline{V4GOOD}$, $\overline{FAR}$, $\overline{PWRGD}$) | $I_{OL}$ = 4.0mA | | | $V_{EE}$ + 0.4 | V |
| $C_{OUT}$ (Note 1) | Output Capacitance ($\overline{RESET}$, $\overline{V1GOOD}$, $\overline{V2GOOD}$, $\overline{V3GOOD}$, $\overline{V4GOOD}$, $\overline{FAR}$) | $V_{OUT}$ = 0V | | | 8 | pF |
| $C_{IN}$ (Note 1) | Input Capacitance ($\overline{MRH}$, MRC) | $V_{IN}$ = 0V | | | 6 | pF |
| $V_{OC}$ | Overcurrent threshold | $V_{OC} = V_{SENSE} - V_{EE}$ | 45 | 50 | 55 | mV |
| $V_{OCI}$ | Overcurrent threshold (Insertion) | $V_{OC} = V_{SENSE} - V_{EE}$<br>$\overline{PWRGD}$ = HIGH<br>Initial Power Up condition | 135 | 150 | 165 | mV |
| $V_{OVR}$ | Overvoltage threshold (rising) | | | | | |
| | X80000 | Referenced to $V_{EE}$ | 3.85 | 3.90 | 3.95 | V |
| | X80001 | | 3.49 | 3.54 | 3.59 | V |
| $V_{OVF}$ | Overvoltage threshold (falling) | | | | | |
| | X80000 | Referenced to $V_{EE}$ | 3.82 | 3.87 | 3.92 | V |
| | X80001 | | 3.46 | 3.51 | 3.56 | V |
| $V_{UV1R}$ | Undervoltage 1 threshold (rising) | Referenced to $V_{EE}$<br>BATT-ON = $V_{EE}$ | 2.19 | 2.24 | 2.29 | V |
| $V_{UV1F}$ | Undervoltage 1 threshold (falling) | | 2.16 | 2.21 | 2.26 | V |
| $V_{UV2R}$ | Undervoltage 2 threshold (rising) | Referenced to $V_{EE}$<br>BATT-ON = $V_{RGO}$ | 1.71 | 1.76 | 1.81 | V |
| $V_{UV2F}$ | Undervoltage 2 threshold (falling) | | 1.68 | 1.73 | 1.78 | V |
| $V_{DRAINF}$ | Drain sense voltage threshold (falling) | Referenced to $V_{EE}$ | 0.9 | 1 | 1.1 | V |
| $V_{DRAINR}$ | Drain sense voltage threshold (rising) | Referenced to $V_{EE}$ | 1.2 | 1.3 | 1.4 | V |
| $V_{TRIP1}$ (Note 1) | $\overline{EN1}$ Trip Point Voltage | Referenced to $V_{EE}$ | | $V_{RGO} \div 2$ | | V |
| $V_{TRIP2}$ (Note 1) | $\overline{EN2}$ Trip Point Voltage | Referenced to $V_{EE}$ | | | | V |
| $V_{TRIP3}$ (Note 1) | $\overline{EN3}$ Trip Point Voltage | Referenced to $V_{EE}$ | | | | V |
| $V_{TRIP4}$ (Note 1) | $\overline{EN4}$ Trip Point Voltage | Referenced to $V_{EE}$ | | | | V |
| **AC CHARACTERISTICS** | | | | | | |
| $t_{FOC}$ | Sense High to Gate Low | | 1.5 | 2.5 | 3.5 | µs |
| $t_{FUV}$ | Under Voltage conditions to Gate Low | | 0.5 | 1 | 1.5 | µs |
| $t_{FOV}$ | Overvoltage Conditions to Gate Low | | 1.0 | 1.5 | 2 | µs |
| $t_{VFR}$ | Overvoltage/undervoltage failure recovery time to Gate =1V. | $V_{DD}$ does not drop below 3V, No other failure conditions. | 1.2 | 1.6 | 2 | µs |
| $t_{BATT\_ON}$ | Delay BATT_ON Valid | | | 100 | | ns |
| $t_{MRC}$ | Minimum time high for reset valid on the MRC pin | | 5 | | | µs |
| $t_{MRH}$ | Minimum time high for reset valid on the $\overline{MRH}$ pin | | 5 | | | µs |
| $t_{MRCE}$ | Delay from MRC enable to $\overline{PWRGD}$ HIGH | No Load | 1.0 | | 1.6 | µs |
| $t_{MRCD}$ | Delay from MRC disable to $\overline{PWRGD}$ LOW | Gate is On, No Load | 200 | | 400 | ns |
| $t_{MRHE}$ | Delay from $\overline{MRH}$ enable to Gate Pin LOW | $I_{GATE}$ = 60µA, No Load | 1.0 | 1.6 | 2.4 | µs |

## Electrical Specifications Standard Settings

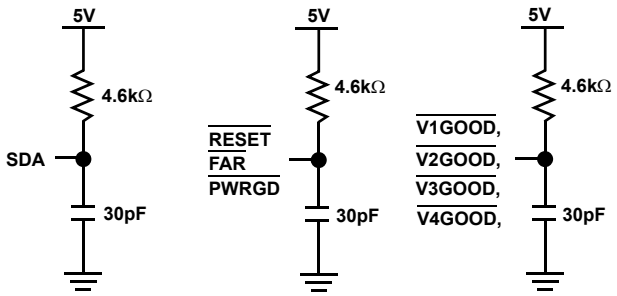
Over the recommended operating conditions unless otherwise specified. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{MRHD}$ | Delay from $\overline{MRH}$ disable to GATE reaching 1V | $I_{GATE}$ = 60µA, No Load | 1.8 | | 2.6 | µs |
| $t_{\overline{RESET}\_E}$ | Delay from $\overline{PWRGD}$ or $\overline{ViGOOD}$ to $\overline{RESET}$ valid LOW | | | | 1 | µs |
| $t_{QC}$ | Delay from IGQ1 and IGQ0 to valid Gate pin current | | | | 1 | µs |
| $t_{SC\_RETRY}$ | Delay between retries | TSC1 = 0; TSC0 = 0 | 90 | 100 | 110 | ms |
| $t_{NF}$ | Noise Filter for Overcurrent | TF1 = 0; TF0 = 1 | 4.5 | 5 | 5.5 | µs |
| $t_{DPOR}$ | Device Delay before Gate assertion | | 45 | 50 | 55 | ms |
| $t_{SPOR}$ | Delay after $\overline{PWRGD}$ and all $\overline{ViGOOD}$ signals are active before $\overline{RESET}$ assertion | TPOR1 = 0; TPOR0 = 0 | 90 | 100 | 110 | ms |
| $t_{TO}$ | $\overline{ViGOOD}$ turn off time | | | 50 | | ns |
| $t_{PDHLPG}$ (Note 1) | Delay from Drain good to $\overline{PWRGD}$ LOW | Gate = $V_{DD}$ | | | 1 | µs |
| $t_{PDLHPG}$ (Note 1) | Delay from Drain fail to $\overline{PWRGD}$ HIGH | Gate = $V_{DD}$ | | | 1 | µs |
| $t_{PGHLPG}$ (Note 1) | Delay from Gate good to $\overline{PWRGD}$ LOW | Drain = $V_{EE}$ | | | 1 | µs |
| $t_{PGLHPG}$ (Note 1) | Delay from Gate fail to $\overline{PWRGD}$ HIGH | Drain = $V_{EE}$ | | | 1 | µs |

NOTE:

1. This parameter is based on characterization data.

## *Equivalent A.C. Output Load Circuit*




## *A.C. Test Conditions*

| | |
|---|---|
| Input pulse levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing levels | $V_{CC}$ x 0.5 |
| Output load | Standard output load |

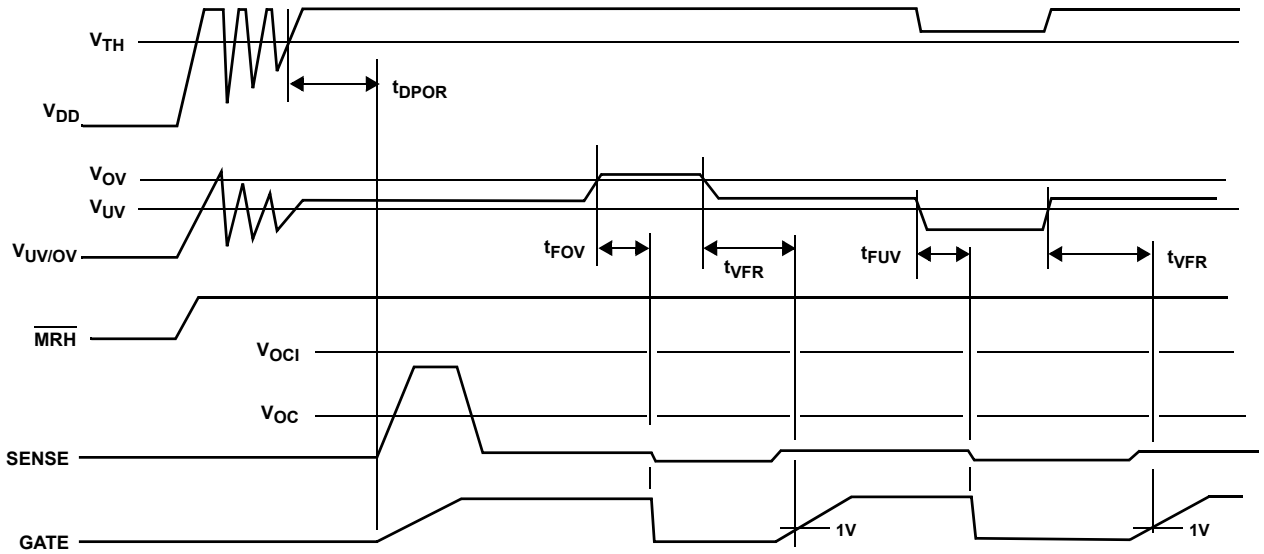



FIGURE 1. OVERVOLTAGE/UNDERVOLTAGE GATE TIMING

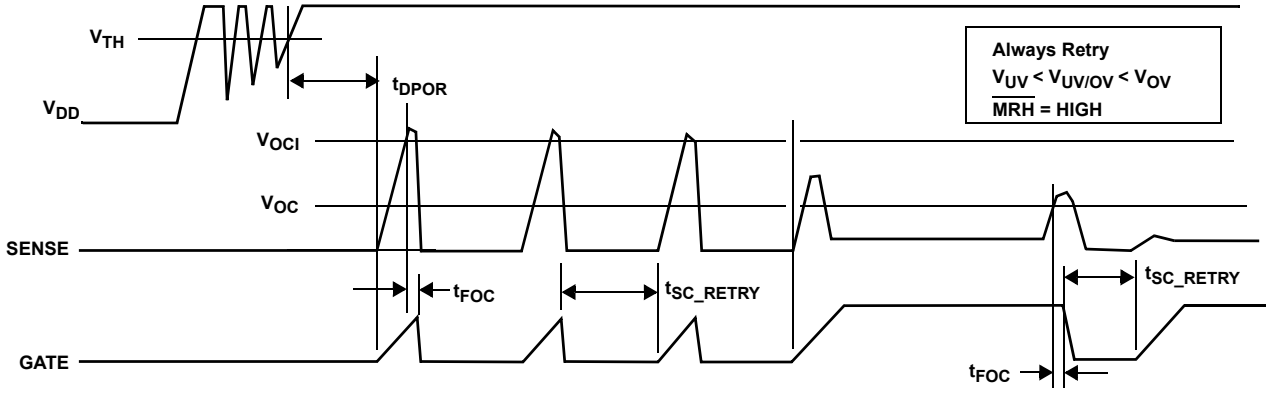



FIGURE 2. OVERCURRENT GATE TIMING

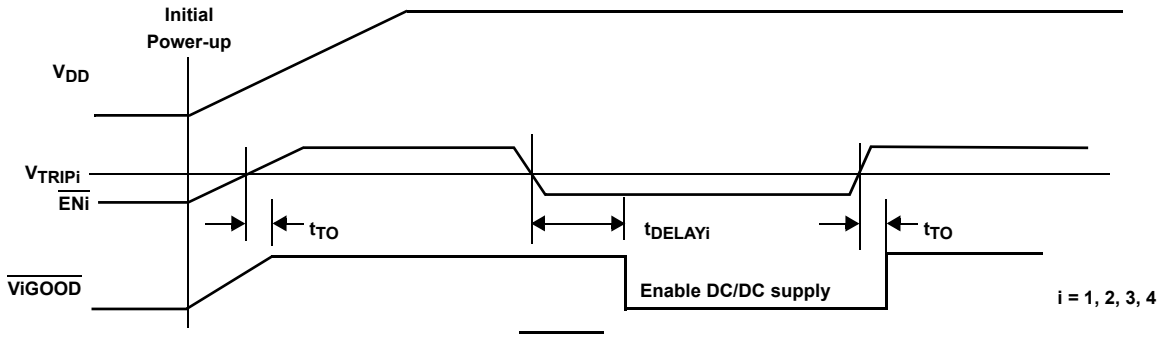



FIGURE 3. $\overline{\text{ViGOOD}}$ TIMINGS

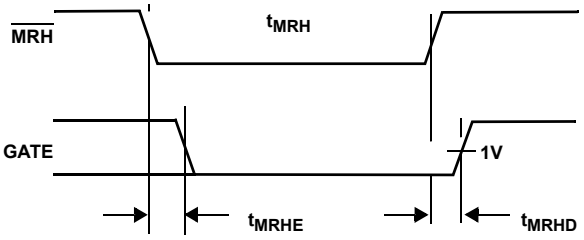



FIGURE 4. MANUAL RESET (HOT SIDE) $\overline{MRH}$

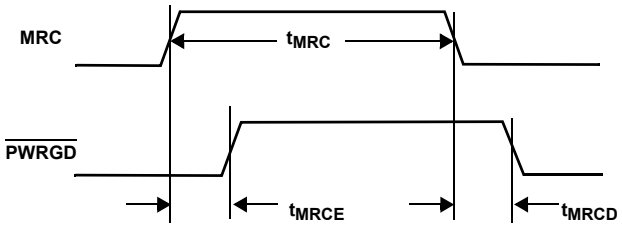



FIGURE 5. MANUAL RESET (COLD SIDE) MRC

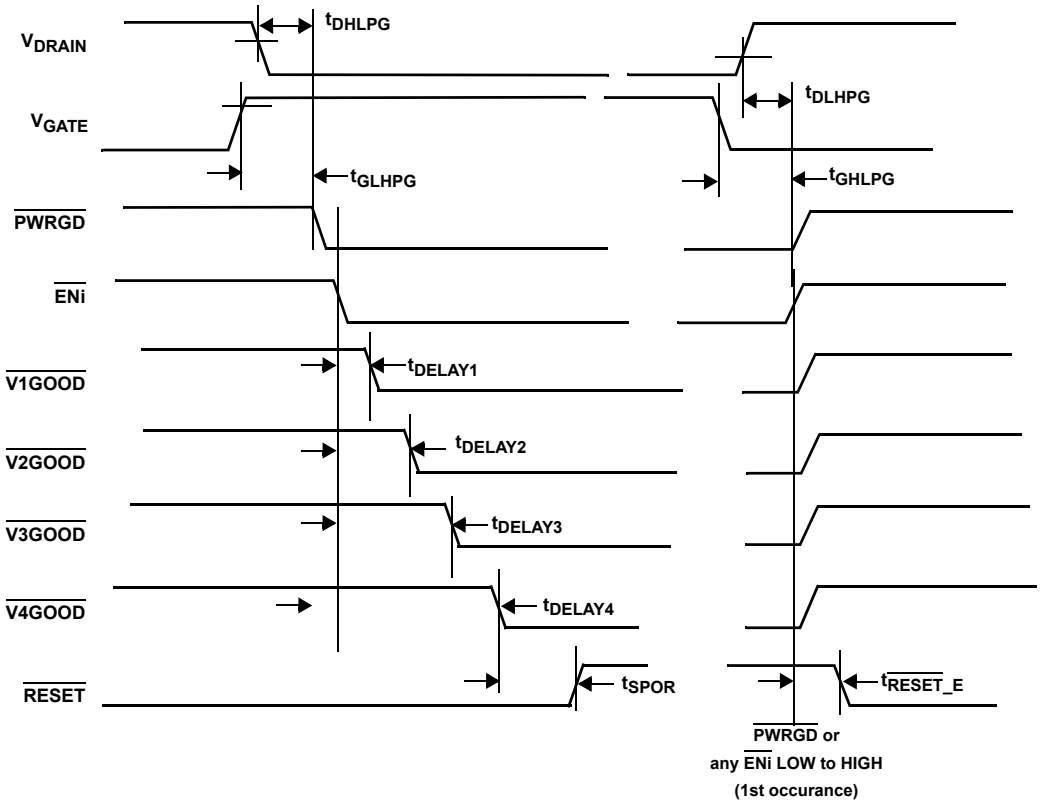



FIGURE 6. $\overline{PWRGD}$ AND $\overline{RESET}$ TIMINGS

## Electrical Specifications Programmable Parameters

Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| VCB | Over Current Trip Voltage Range | Factory Setting is 50mV (see VOCI). | 30 | | 100 | mV |
| $I_{GATE}$ | ($V_{CB}$ = $V_{SENSE}$ - $V_{EE}$) | For other options, contact Intersil. | -12 | | 12 | % |
| | Gate Pin Pull-Up Current. (error) (current) | Gate Drive On; $V_{GATE}$ = $V_{EE}$, IGQ1=0; IGQ0=0 | | | | |
| | IG3 = 0; IG2= 0; IG1 = 0; IG0 = 0 | Factory Default | 9.2 | 10.5 | 11.8 | µA |
| | IG3 = 0; IG2= 0; IG1 = 0; IG0 = 1 | | | 21.0 | | µA |
| | IG3 = 0; IG2= 0; IG1 = 1; IG0 = 0 | | | 31.5 | | µA |
| | IG3 = 0; IG2= 0; IG1 = 1; IG0 = 1 | | | 42.0 | | µA |
| | IG3 = 0; IG2= 1; IG1 = 0; IG0 = 0 | | 46.2 | 52.5 | 58.5 | µA |
| | IG3 = 0; IG2= 1; IG1 = 0; IG0 = 1 | | | 63.0 | | µA |
| | IG3 = 0; IG2= 1; IG1 = 1; IG0 = 0 | | 64.7 | 73.5 | 82.3 | µA |
| | IG3 = 0; IG2= 1; IG1 = 1; IG0 = 1 | | | 84.0 | | µA |
| | IG3 = 1; IG2= 0; IG1 = 0; IG0 = 0 | | | 94.5 | | µA |
| | IG3 = 1; IG2= 0; IG1 = 0; IG0 = 1 | | | 105.0 | | µA |
| | IG3 = 1; IG2= 0; IG1 = 1; IG0 = 0 | | | 115.5 | | µA |
| | IG3 = 1; IG2= 0; IG1 = 1; IG0 = 1 | | | 126.0 | | µA |
| | IG3 = 1; IG2= 1; IG1 = 0; IG0 = 0 | | | 136.5 | | µA |
| | IG3 = 1; IG2= 1; IG1 = 0; IG0 = 1 | | | 147.0 | | µA |
| | IG3 = 1; IG2= 1; IG1 = 1; IG0 = 0 | | 138.6 | 157.5 | 176.4 | µA |
| | IG3 = 1; IG2= 1; IG1 = 1; IG0 = 1 | | | 168.0 | | µA |
| | IG3-IG0 = Don't Care | IGQ1=0; IGQ0=1 | 9.2 | 10.57 | 11.8 | µA |
| | IG3-IG0 = Don't Care | IGQ1=1; IGQ0=0 | 64.7 | 73.5 | 82.3 | µA |
| | IG3-IG0 = Don't Care | IGQ1=1; IGQ0=1 | 138.6 | 157.5 | 176.4 | µA |
| $V_{PGA}$ | Power Good Threshold Accuracy | $V_{DRAIN}$ - $V_{EE}$, High to Low Transition. Default Factory Setting is 47V. | | ±400 | | mV |
| $V_{OCI}$ | Over current threshold (Insertion) | Referenced to VEE | | | | |
| | VS1 = 0 VS0 = 0 | PWRGD = HIGH | 45 | 50 | 55 | mV |
| | VS1 = 0 VS0 = 1 | Factory Default | 90 | 100 | 110 | mV |
| | VS1 = 1 VS0 = 0 | | 135 | 150 | 165 | mV |
| | VS1 = 1 VS0 = 1 | | 180 | 200 | 220 | mV |
| **AC CHARACTERISTICS** | | | | | | |
| $t_{SC\_RETRY}$ | Delay between Retries | Factory Default | | | | |
| | TSC1 = 0 TSC0 = 0 | | 90 | 100 | 110 | ms |
| | TSC1 = 0 TSC0 = 1 | | 450 | 500 | 550 | ms |
| | TSC1 = 1 TSC0 = 0 | | 0.9 | 1 | 1.1 | s |
| | TSC1 = 1 TSC0 = 1 | | 4.5 | 5 | 5.5 | s |

## Electrical Specifications Programmable Parameters

Over the recommended operating conditions unless otherwise specified. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{NF}$ | Noise Filter for Overcurrents | Factory Default | | | | |
| | F1 = 0 F0 = 0 | | | 0 | | µs |
| | F1 = 0 F0 = 1 | | 4.5 | 5 | 5.5 | µs |
| | F1 = 1 F0 = 0 | | 9 | 10 | 11 | µs |
| | F1 = 1 F0 = 1 | | 18 | 20 | 22 | µs |
| $t_{SPOR}$ | Delay before $\overline{RESET}$ assertion | Factory Default | | | | |
| | TPOR1 = 0 TPOR0 = 0 | | 90 | 100 | 110 | ms |
| | TPOR1 = 0 TPOR0 = 1 | | 450 | 500 | 550 | ms |
| | TPOR1 = 1 TPOR0 = 0 | | 0.9 | 1 | 1.1 | s |
| | TPOR1 = 1 TPOR0 = 1 | | 4.5 | 5 | 5.5 | s |
| $t_{DELAYi}$ | Time Delay used in Power Sequencing (i = 1 to 4) | Factory Default | | | | |
| | TiD1 = 0 TiD0 = 0 | | 90 | 100 | 110 | ms |
| | TiD1 = 0 TiD0 = 1 | | 450 | 500 | 550 | ms |
| | TiD1 = 1 TiD0 = 0 | | 0.9 | 1 | 1.1 | s |
| | TiD1 = 1 TiD0 = 1 | | 4.5 | 5 | 5.5 | s |

## Serial Interface

Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $I_{CC1}$ (Note 1) | Active Supply Current ($V_{DD}$) Read to Memory or CRs | $V_{IL} = V_{CC} \times 0.1$<br>$V_{IH} = V_{CC} \times 0.9$,<br>$f_{SCL}$ = 400kHz | | | 2.5 | mA |
| $I_{CC2}$ (Note 1) | Active Supply Current ($V_{DD}$) Write to Memory or CRs | | | | 3.0 | mA |
| $I_{LI}$ | Input Leakage Current (SCL, WP, A0, A1) | $V_{IL}$ = GND to $V_{CC}$ | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current (SDA) | $V_{SDA}$ = GND to $V_{CC}$<br>Device is in Standby (Note 2) | | | 10 | µA |
| $V_{IL}$ (Note 3) | Input LOW Voltage (SDA, SCL, WP, A0, A1) | | -0.5 + VEE | | $(V_{EE} + 5) \times 0.3$ | V |
| $V_{IH}$ (Note 3) | Input HIGH Voltage (SDA, SCL, WP, A0, A1) | | $(V_{EE} + 5) \times 0.7$ | | $(V_{EE} + 5) + 0.5$ | V |
| $V_{HYS}$ | Schmitt Trigger Input Hysteresis | | | | | |
| | Fixed input level | | $V_{EE}$ + 0.2 | | | V |
| | $V_{CC}$ related level | | .05 x ($V_{EE}$ + 5) | | | V |
| $V_{OL}$ | Output LOW Voltage (SDA) | $I_{OL}$ = 4.0mA (2.7-5.5V)<br>$I_{OL}$ = 2.0mA (2.4-3.6V) | | | $V_{EE}$ + 0.4 | V |
| **AC CHARACTERISTICS** | | | | | | |
| $f_{SCL}$ | SCL Clock Frequency | | | | 400 | kHz |
| $t_{IN}$ | Pulse width Suppression Time at inputs | | 50 | | | ns |
| $t_{AA}$ | SCL LOW to SDA Data Out Valid | | 0.1 | | 1.5 | µs |

### Serial Interface (Continued)

Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{BUF}$ | Time the bus is free before start of new transmission | | 1.3 | | | µs |
| $t_{LOW}$ | Clock LOW Time | | 1.3 | | | µs |
| $t_{HIGH}$ | Clock HIGH Time | | 0.6 | | | µs |
| $t_{SU:STA}$ | Start Condition Setup Time | | 0.6 | | | µs |
| $t_{HD:STA}$ | Start Condition Hold Time | | 0.6 | | | µs |
| $t_{SU:DAT}$ | Data In Setup Time | | 100 | | | ns |
| $t_{HD:DAT}$ | Data In Hold Time | | 0 | | | µs |
| $t_{SU:STO}$ | Stop Condition Setup Time | | 0.6 | | | µs |
| $t_{DH}$ | Data Output Hold Time | | 50 | | | ns |
| $t_R$ | SDA and SCL Rise Time | | 20 +.1Cb (Note 1) | | 300 | ns |
| $t_F$ | SDA and SCL Fall Time | | 20 +.1Cb (Note 1) | | 300 | ns |
| $t_{SU:WP}$ | WP Setup Time | | 0.6 | | | µs |
| $t_{HD:WP}$ | WP Hold Time | | 0 | | | µs |
| Cb | Capacitive load for each bus line | | | | 400 | pF |
| $t_{WC}$ (Note 2) | EEPROM Write Cycle Time | | | 5 | 10 | ms |

NOTE:

2. $t_{WC}$ is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

## *Timing Diagrams*

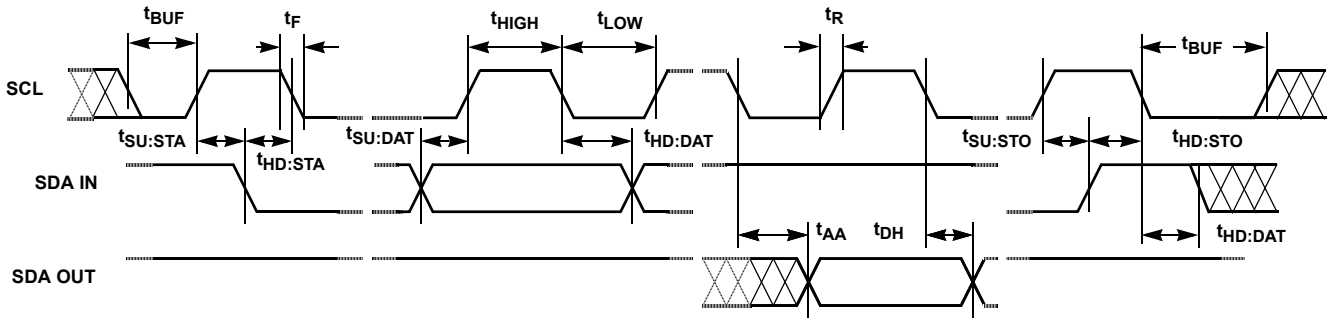



**FIGURE 7. BUS TIMING**

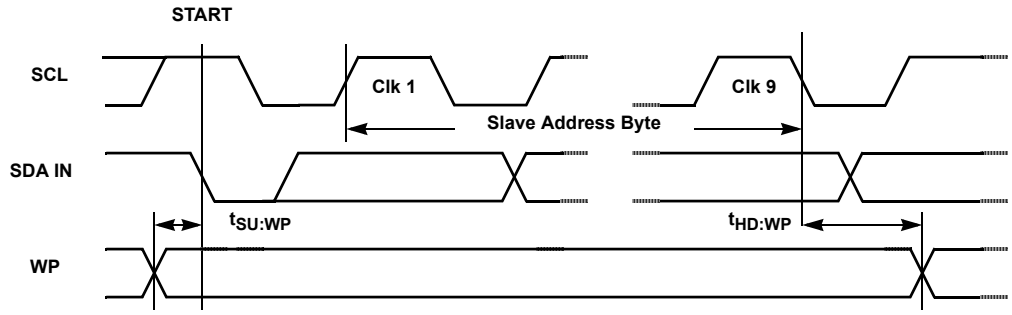



FIGURE 8. WP PIN TIMING

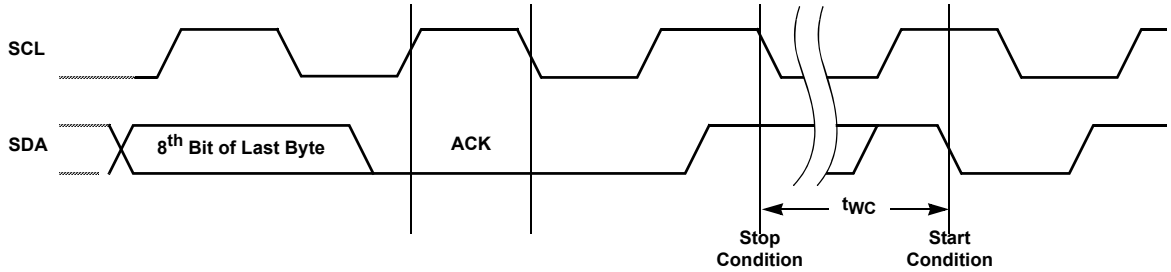



FIGURE 9. WRITE CYCLE TIMING

## *Symbol Table*

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |

## *Typical Performance Characteristics*

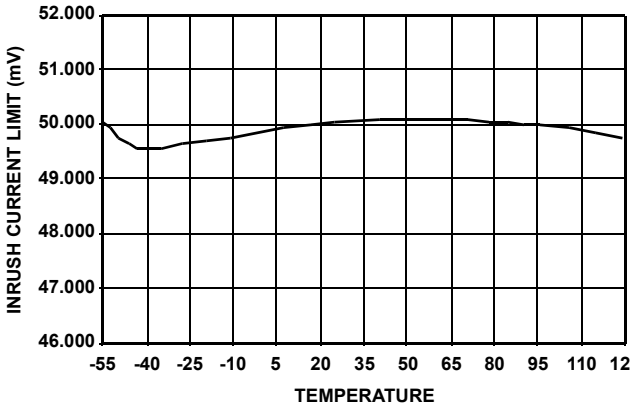



FIGURE 10. OVERCURRENT THRESHOLD vs TEMPERATURE

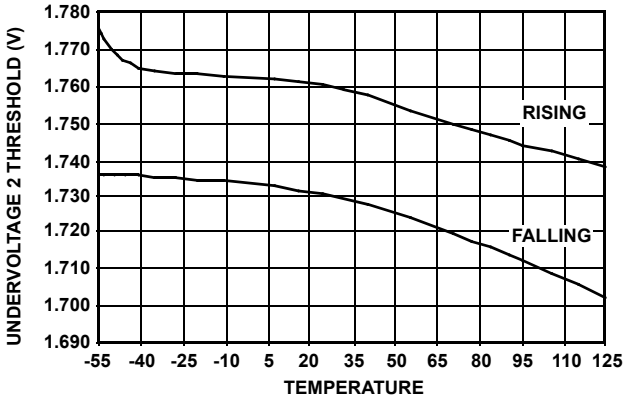



FIGURE 11. UNDERVOLTAGE 1 THRESHOLD vs TEMPERATURE

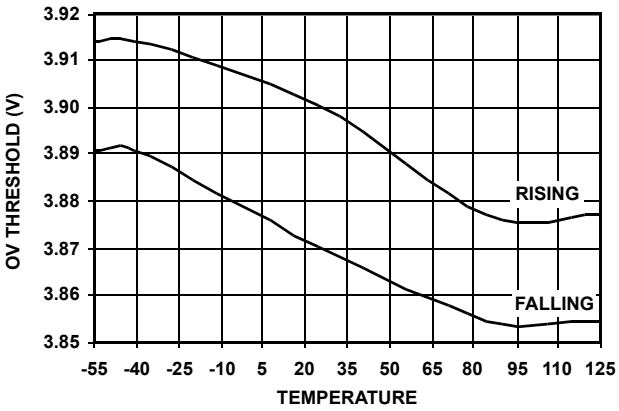



FIGURE 12. OVERVOLTAGE THRESHOLD vs TEMPERATURE

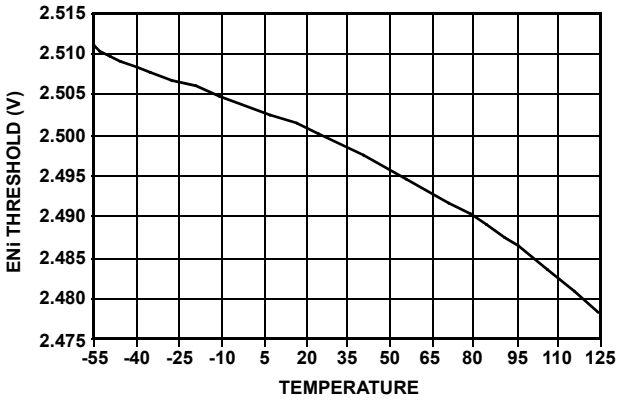



FIGURE 13. $\overline{ENi}$ THRESHOLD vs TEMPERATURE

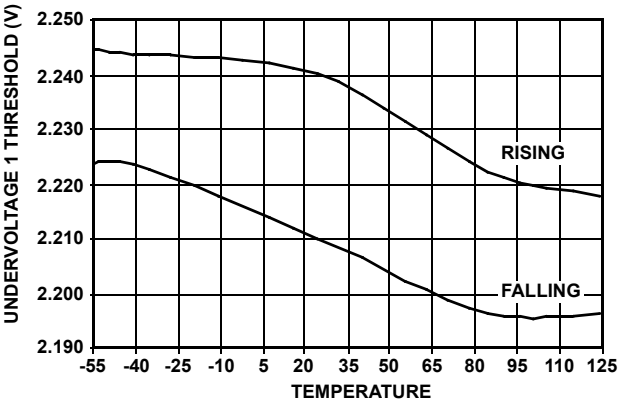



FIGURE 14. UNDERVOLTAGE 1 THRESHOLD vs TEMPERATURE

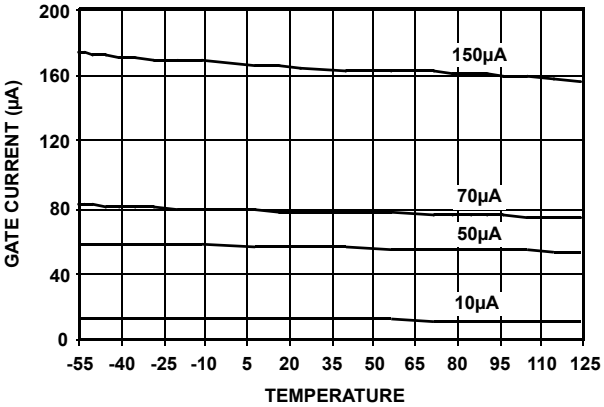



FIGURE 15. $I_{GATE}$ (SOURCE) vs TEMPERATURE

## *Typical Performance Characteristics* (Continued)

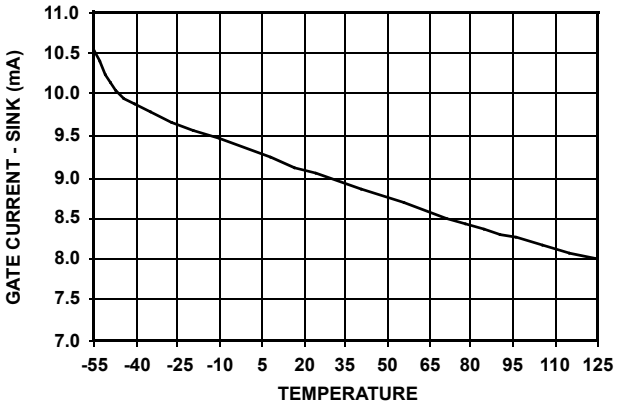



FIGURE 16. $I_{GATE}$ (SINK) vs TEMPERATURE

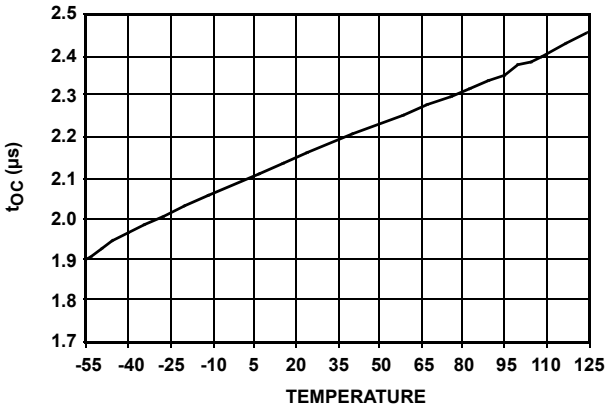



FIGURE 17. $t_{FOC}$ vs TEMPERATURE

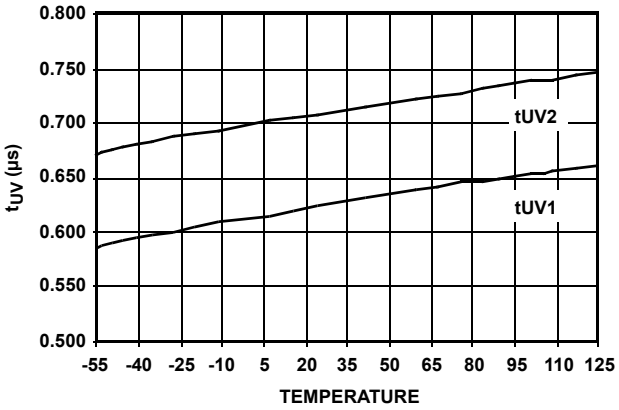



FIGURE 18. $t_{FUV}$ vs TEMPERATURE

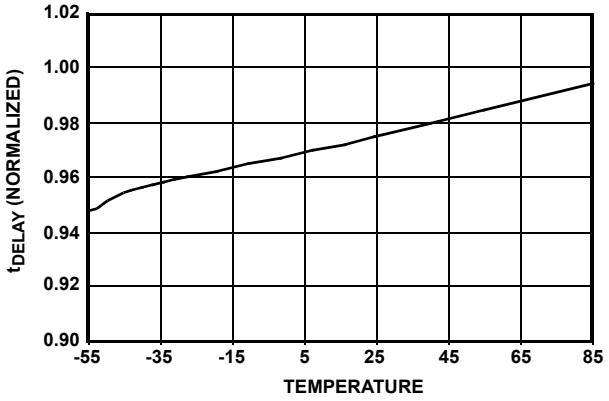



FIGURE 19. $t_{DELAYi}$ vs TEMPERATURE

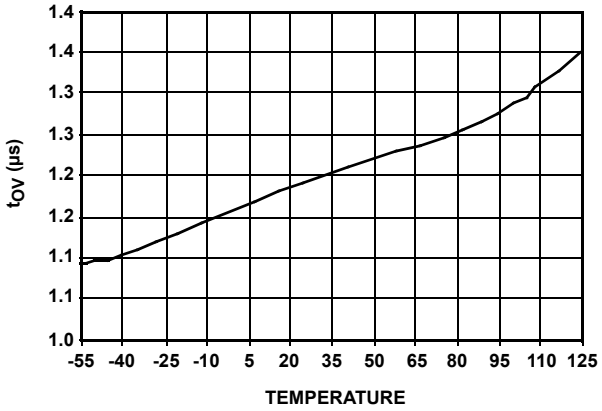



FIGURE 20. $t_{FOV}$ vs TEMPERATURE

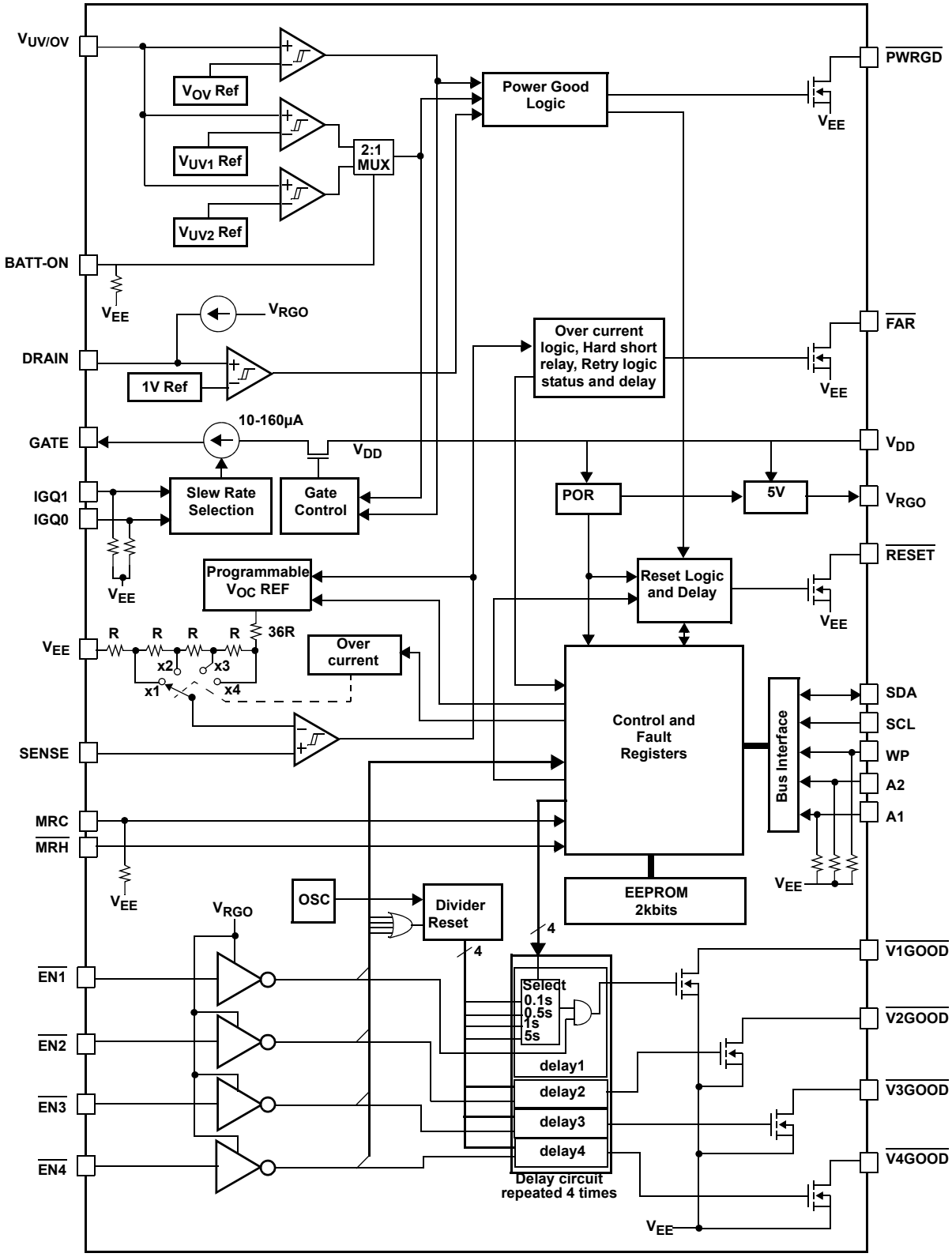
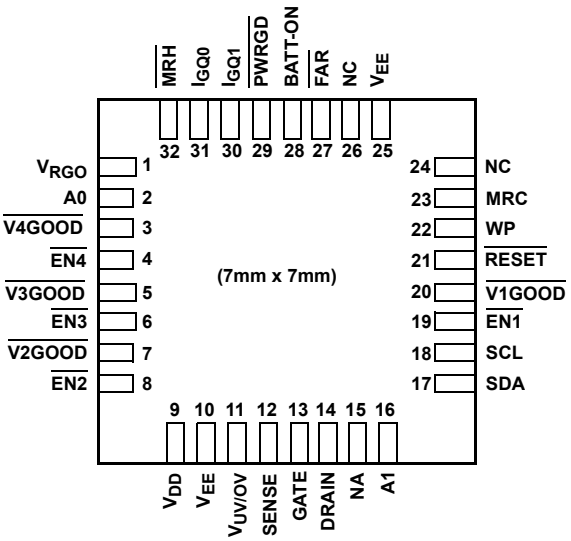



FIGURE 21. BLOCK DIAGRAM

## Pin Configuration

**X80000/X80001**

32-lead QFN Quad Package




## Pin Descriptions

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{RGO}$ | **Regulated 5V output.** Used to pull-up user programmable inputs IGQ0, IGQ1, BATT-ON, A1, A0, and WP (if needed). |
| 2 | A0 | **Address Select Input.** It has an internal pulldown resistor. (>10MΩ typical)<br>The A0 and A1 bits allow for up to 4 X80000 devices to be used on the same SMBus serial interface. |
| 3 | $\overline{V4GOOD}$ | **V4 Voltage Good Output.** This open drain output goes LOW when $\overline{EN4}$ is less than $V_{TRIP4}$ and goes HIGH when $\overline{EN4}$ is greater than $V_{TRIP4}$. There is a user selectable delay circuitry on this pin. |
| 4 | EN4 | **V4 Voltage Enable Input.** Fourth voltage enable pin. If unused connect to $V_{RGO}$. |
| 5 | $\overline{V3GOOD}$ | **V3 Voltage Good Output (Active Low).** This open drain output goes LOW when $\overline{EN3}$ is less than $V_{TRIP3}$ and goes HIGH when $\overline{EN3}$ is greater than $V_{TRIP3}$. There is a user selectable delay circuitry on this pin. |
| 6 | EN3 | **V3 Voltage Enable Input.** Third voltage enable pin. If unused connect to $V_{RGO}$. |
| 7 | $\overline{V2GOOD}$ | **V2 Voltage Good Output (Active Low).** This open drain output goes LOW when $\overline{EN2}$ is less than $V_{TRIP2}$ and goes HIGH when $\overline{EN2}$ is greater than $V_{TRIP2}$. There is a user selectable delay circuitry on this pin. |
| 8 | $\overline{EN2}$ | **V2 Voltage Enable Input.** Second voltage enable pin. If unused connect to $V_{RGO}$. |
| 9 | $V_{DD}$ | **Positive Supply Voltage Input.** |
| 10 | $V_{EE}$ | **Negative Supply Voltage Input.** |
| 11 | $V_{UV/OV}$ | **Analog Undervoltage and Overvoltage Input.** Turns off the external N-channel MOSFET when there is an undervoltage or overvoltage condition. |
| 12 | SENSE | **Circuit Breaker Sense Input**. This input pin detects the overcurrent condition. |
| 13 | GATE | **Gate Drive Output.** Gate drive output for the external N-channel MOSFET. |
| 14 | DRAIN | **Drain**. Drain sense input of the external N-channel MOSFET. |
| 15 | NA | **Not Available.** Do not connect to this pin. |
| 16 | A1 | **Address Select Input.** It has an internal pulldown resistor. (>10MΩ typical)<br>The A0 and A1 bits allow for up to 4 X80000 devices to be used on the same SMBus serial interface. |
| 17 | SDA | **Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull up resistor and the input buffer is always active (not gated). |
| 18 | SCL | **Serial Clock.** The Serial Clock controls the serial bus timing for data input and output. |
| 19 | $\overline{EN1}$ | **V1 Voltage Enable Input.** First voltage enable pin. If unused connect to $V_{RGO}$. |

## Pin Descriptions (Continued)

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 20 | $\overline{\text{V1GOOD}}$ | **V1 Voltage Good Output (Active Low).** This open drain output goes LOW when $\overline{\text{EN1}}$ is less than $V_{TRIP1}$ and goes HIGH when $\overline{\text{EN1}}$ is greater than $V_{TRIP1}$. There is a user selectable delay circuitry on this pin. |
| 21 | $\overline{\text{RESET}}$ | **RESET Output.** This open drain pin is an active LOW output. This pin will be active until $\overline{\text{PWRGD}}$ goes active and the power sequencing is complete. This pin will be released after a programmable delay. |
| 22 | WP | **Write Protect. Input Pin.** WP HIGH (in conjunction with WPEN bit=1) prevents writes to any memory location in the device. It has an internal pulldown resistor. (>10MΩ typical) |
| 23 | MRC | **Manual Reset Input Cold-side.** Pulling the MRC pin HIGH initiates a system side RESET. The MRC signal must be held HIGH for 5µsecs. It has an internal pulldown resistor. (>10MΩ typical) |
| 24 | NC | **No Connect.** No internal connections. |
| 25 | $V_{EE}$ | **Negative Supply Voltage Input.** |
| 26 | NC | **No Connect.** No internal connections. |
| 27 | $\overline{\text{FAR}}$ | **Failure After Re-try ($\overline{\text{FAR}}$)** output signal. Failure After Re-try ($\overline{\text{FAR}}$) is asserted after a number of retries. Used for Overcurrent and hardshort detection. |
| 28 | BATT-ON | **Battery On Input**. This input signals that the battery backup (or secondary supply) is supplying power to the backplane. It has an internal pulldown resistor. (>10MΩ typical) |
| 29 | $\overline{\text{PWRGD}}$ | **Power Good Output.** This output pin enables a power module. |
| 30 | IGQ1 | **Gate Current Quick Select Bit 1 Input.** This pin is used to change the gate current drive and is intended to allow for current ramp rate control of the gate pin of an external FET. It has an internal pulldown resistor. (>10MΩ typical) |
| 31 | IGQ0 | **Gate Current Quick Select Bit 0 Input.** This pin is used to change the gate current drive and is intended to allow for current ramp rate control of the gate pin of an external FET. It has an internal pulldown resistor. (>10MΩ typical) |
| 32 | $\overline{\text{MRH}}$ | **Manual Reset Input Hot-side.** Pulling the $\overline{\text{MRH}}$ pin LOW initiates a GATE pin reset (GATE pin pulled LOW). The $\overline{\text{MRH}}$ signal must be held LOW for 5µsecs (minimum). |

## Functional Description

### Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or DC/DC converter can draw huge transient currents as they charge up (See Figure 22). This transient current can cause permanent damage to the board's components and cause transients on the system power supply.

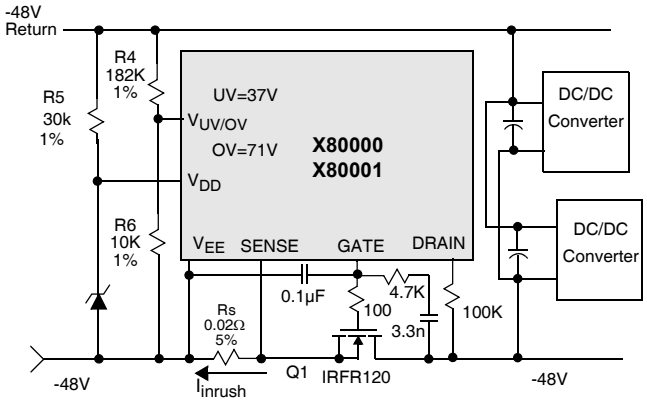



FIGURE 22. TYPICAL -48V HOTSWAP APPLICATION CIRCUIT

The X80000 is designed to turn on a board's supply voltage in a controlled manner (see Figure 23), allowing the board to be safely inserted or removed from a live backplane. The device also provides undervoltage, overvoltage and overcurrent protection while keeping the power module (DC-DC converter) off until the backplane input voltage is stable and within tolerance.

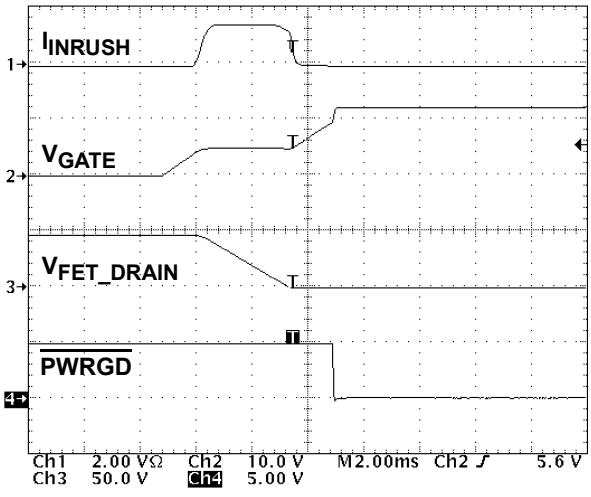



FIGURE 23. TYPICAL INRUSH WITH GATE SLEW RATE CONTROL

### *Overvoltage and Undervoltage Shutdown*

The X80000 provides overvoltage and undervoltage protection circuits.

When an overvoltage ($V_{OV}$) or undervoltage ($V_{UV1}$ and $V_{UV2}$) condition is detected, the GATE pin will be immediately pulled low. The undervoltage threshold $V_{UV1}$ applies to the normal operation with a main supply. The undervoltage threshold $V_{UV2}$ assumes the system is powered by a battery. When using a battery backup, the BATT-ON pin is pulled to $V_{RGO}$. The default thresholds have been set so the external resistance values determine the overvoltage threshold, a main undervoltage threshold and a battery undervoltage threshold.

As shown in Figure 26, this circuit block contains comparators and programmable voltage references to monitor the single overvoltage and dual undervoltage trip points. During manufacturing, Intersil programmed the overvoltage and undervoltage trip points as shown in Table 1 below. Custom values are possible.

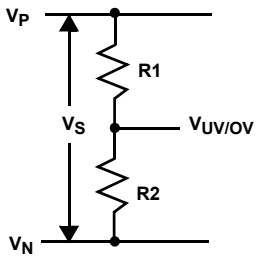
A resistor divider connected between the plus and minus input voltages and the $V_{UV/OV}$ pin (see Figure 24) determines the overvoltage and undervoltage shutdown voltages and the operating voltage range. Using the thresholds in Table 1 and the equations of Figure 24 the desired operating voltage can be determined. Figure 25 shows the resistance values for various operating voltages.

**TABLE 1. OVERVOLTAGE/UNDERVOLTAGE DEFAULT THRESHOLDS**

| SYMBOL | DESCRIPTION | THRESHOLD FALLING | THRESHOLD RISING | MAX/MIN VOLTAGE (Note 1) | LOCKOUT VOLTAGE (Note 2) |
|---|---|---|---|---|---|
| $V_{OV}$ | Overvoltage (X80000) | 3.87V | 3.9V | 74.3 | 74.9 |
| $V_{OV}$ | Overvoltage (X80001) | 3.51V | 3.54V | 67.4 | 68 |
| $V_{UV1}$ | Undervoltage 1 | 2.21V | 2.24V | 43.0 | 42.4 |
| $V_{UV2}$ | Undervoltage 2 | 1.73V | 1.76V | 33.8 | 33.2 |

NOTES:

1. Max/Min Voltage is the maximum and minimum operating voltage assuming the recommended $V_{UV/OV}$ resistor divider.
2. Lockout voltage is the voltage where the X80000/1 turns off the FET.




Voltage divider:

$$V_{UV/OV} = V_S\left(\frac{R2}{R1+R2}\right)$$

or:

$$V_S = V_{UV/OV}\left(\frac{R1+R2}{R2}\right)$$

**FIGURE 24. OVERVOLTAGE UNDERVOLTAGE DIVIDER**

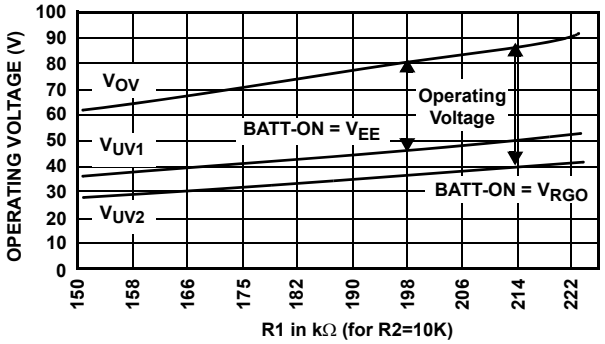



**FIGURE 25. OPERATING VOLTAGE vs RESISTOR RATIO**

### Battery Back Up Operations

An external signal, BATT-ON, is provided to switch the undervoltage trip point. The BATT-ON signal is a LOGIC HIGH if $V_{IHB} > V_{EE} + 4V$ and is a LOGIC LOW if $V_{ILB} < V_{EE} + 2V$. The time from a BATT-ON input change to a valid new undervoltage threshold is 100ns. See Electrical Specifications for more details.

Note: The $V_{UV/OV}$ pin must be limited to less than $V_{EE} + 5.5V$ in worst case conditions. Values for R1 and R2 must be chosen such that this condition is met. Intersil recommends R1 = 182kΩ and R2 = 10kΩ to conform to factory settings.

**TABLE 2. SELECTING BETWEEN UNDERVOLTAGE TRIP POINTS**

| PIN | DESCRIPTION | TRIP POINT SELECTION |
|---|---|---|
| BATT-ON | Undervoltage Trip Point Selection Pin | If BATT-ON = 0, $V_{UV1}$ trip point is selected; If BATT-ON = 1, $V_{UV2}$ trip point is selected. |

$V_{UV1}$ and $V_{UV2}$ are undervoltage thresholds.

### Overvoltage/Undervoltage Fault Condition Flags

On any overvoltage or undervoltage violation, the X80000 cuts-off the GATE. This condition also sets the fault-overvoltage (FOV) or fault-undervoltage1/2 (FUV1/2) bits low. These bits are readable through the SMBus. To clear the fault bits, the fault condition must first be rectified (by the system) then

cleared by a write to Fault Detection Register. Please refer to FDR section. See Table 2.

**TABLE 3. OVERVOLTAGE/UNDERVOLTAGE FLAG BITS**

| SYMBOL | VIOLATION (ON) | NORMAL (OFF) |
|---|---|---|
| FOV | FOV = 0, when $V_{UV/OV} > V_{OV}$ (Overvoltage) | FOV = 1, when $V_{UV/OV} < V_{OV} + 0.2V$ and reset by a write operation |
| FUV1/2 | FUV1/2 = 0, when $V_{UV/OV} < V_{UV1/2}$ (Undervoltage) | FUV1/2 = 1, when $V_{UV/OV} > V_{UV1/2} - 0.2V$ and reset by a write operation |

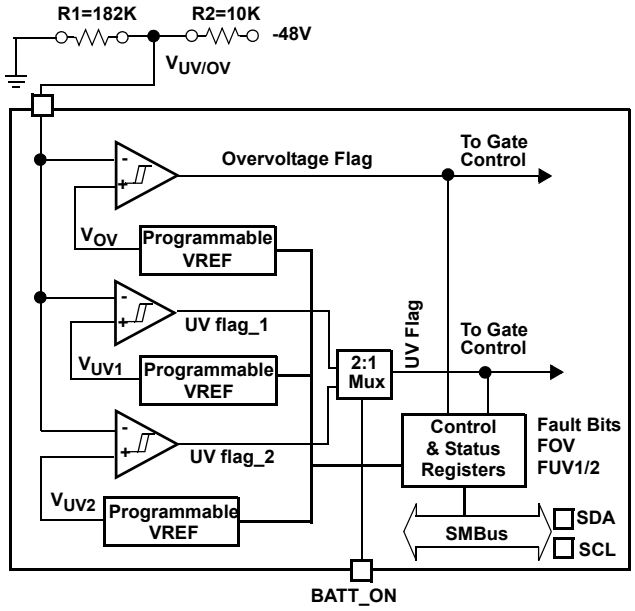



**FIGURE 26. PROGRAMMABLE UNDERVOLTAGE AND OVERVOLTAGE FOR PRIMARY AND BATTERY BACKUP**

## *Overcurrent Protection (Circuit Breaker Function)*

The X80000 overcurrent circuit provides the following functions:

- Overcurrent shut-down of the power FET and external power good indicators.
- Noise filtering of the current monitor input.
- Relaxed overcurrent limits for initial board insertion.
- Overcurrent recovery retry operation.
- Flag of overcurrent fault condition.
- Flag of overcurrent retry failure.

A sense resistor, placed in the supply path between $V_{EE}$ and SENSE (see Figure 22) generates a voltage internal to the X80000. When this voltage exceeds 50mV, an over current condition exists and an internal “circuit breaker” trips, turning off the gate drive to the external FET. The actual overcurrent level is dependent on the value of the current sense resistor. For example a 20mΩ sense resistor sets the overcurrent level to 2.5A.

Intersil’s X80000 provides a safety mechanism during insertion of the board into the back plane. During insertion of the board into the backplane large currents may be induced. In order to prevent premature shut down of the external FET, the X80000 allows for a choice of up to 4 times the overcurrent setting during insertion.

After the $\overline{PWRGD}$ signal is asserted, the X80000 switches back to the normal overcurrent setting. The overcurrent threshold voltage during insertion can be changed from 50mV to 100mV, 150mV, or 200mV, by setting bits in Control Register CR4.

After the Power FET turns off due to an overcurrent condition, a retry circuit turns the FET back on after a delay of $t_{SC\_RETRY}$. If the overcurrent condition remains, the FET again turns off. This sequence repeats until the overcurrent condition is released. There are various other options that program the retry circuit to change the number of retries or to not retry. An optional output signal, $\overline{FAR}$, indicates a failure after retry.

### Overcurrent Shut-down

As shown in Figure 27, this circuit block contains a resistor ladder, a comparator, a noise filter and a programmable voltage reference to monitor for overcurrent conditions.

The overcurrent voltage threshold ($V_{OC}$) is 50mV. This can be factory set, by special order, to any setting between 30mV and 100mV. $V_{OC}$ is the voltage between the SENSE and $V_{EE}$ pins and across the $R_{SENSE}$ resistor. If the selected sense resistor is 20mΩ, then 50mV corresponds to an overcurrent of 2.5A.

If an overcurrent condition is detected, the GATE is turned off, all power good indicators go inactive and an overcurrent failure bit (FOC) is set.

### Overcurrent Noise Filter

The X80000 has a noise (low pass) filter built into the overcurrent comparator. The comparator will thus ignore current spikes shorter than 5µs. Other filter options are provided by setting control bits in register CR4. The control bits set the comparator to ignore current spikes shorter that 5µs, 10µs or 20µs and allow the filter to be turned off.

**TABLE 4. NOISE FILTER FOR OVER CURRENTS**

| F1 | F0 | $t_{NF}$ (maximum noise input pulse width) |
|---|---|---|
| 0 | 0 | 0µs |
| 0 | 1 | 5µs |
| 1 | 0 | 10µs |
| 1 | 1 | 20µs |

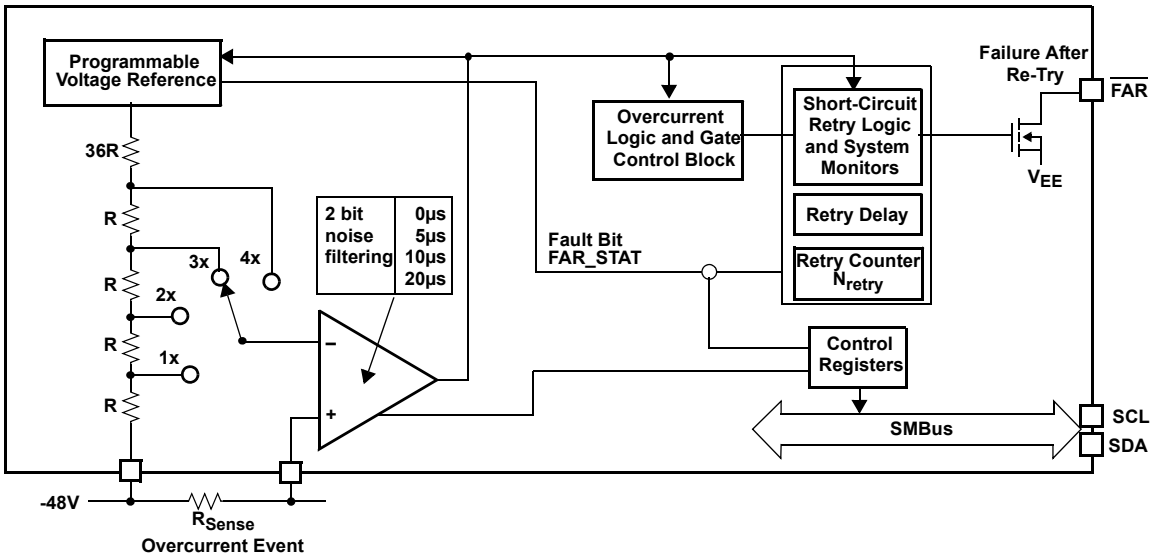



FIGURE 27. OVERCURRENT DETECTION/SHORT CIRCUIT PROTECTION WITH PROGRAMMBLE RETRY AND FLAG MONITORS

### Overcurrent During Insertion

Insertion is defined as the first plug-in of the board to the backplane. In this case, the X80000 is initially fully powered off prior to the hot plug connection to the mains supply. This condition is different from a situation where the mains supply has temporarily failed resulting in a partial recycle of the power. This second condition will be referred to as a power cycle.

During insertion, the board can experience high levels of current for short periods of time as power supply capacitors charge up on the power bus. To prevent the overcurrent sensor from turning off the FET inadvertently, the X80000 has the ability to allow more current to flow through the powerFET and the sense resistor for a short period of time until the FET turns on and the $\overline{\text{PWRGD}}$ signal goes active. In the standard setting, 200mV is allowed across sense resistor the during insertion (10A assuming a 20mW resistor). Two bits in register CR4 select the insertion current limit of 1X, 2X, 3X or 4X the base setting of 50mV. This provides a mechanism to reduce insertion issues associated with huge current surges.

TABLE 5. INSERTION OVERCURRENT THRESHOLD OPTIONS

| VS1 | VS0 | $V_{OCI}$ |
|---|---|---|
| 0 | 0 | 50mV (1X) |
| 0 | 1 | 100mV (2X) |
| 1 | 0 | 150mV (3X) |
| 1 | 1 | 200mV (4X) |

### Hardshort Protection - Programmable Retry

In the event on an overcurrent or hard short condition, the X80000 includes a retry circuit. This circuit waits for 100ms, then attempts to again turn on the FET. If the fault condition still exists, the FET turns off and a retry counter (SC_Counter) increments. After the selected number of failed trys, the X80000 sets a Failed After Retry Status (FAR_STAT) fault bit, sets the $\overline{\text{FAR}}$ pin LOW and goes into an idle state. In this state the GATE pin will not go active until the device is cleared.

The retry circuit can be programmed to handle the retry operation in one of eight ways (See Table 6). The options allow retries from zero to unlimited and specifies when to assert the $\overline{\text{FAR}}$ (Failure After Re-Try) signal. In the “Always Retry” case there is no idle state, so when the overcurrent condition clears, the GATE goes active and the FET turns on.

There are four optional retry delay periods. These are 100ms, 500ms, 1s, and 5s. These are programmed by bits located in the CR2 register.

After $\overline{\text{FAR}}$ is asserted, there are two ways to clear the hardshort protection:

1. Master Reset Hot Side. The master reset pin, $\overline{\text{MRH}}$, can be asserted by pulling it LOW. Upon $\overline{\text{MRH}}$ assertion, all default values are restored and the retry is cleared.
2. Power cycle the part, turning $V_{DD}$ OFF, then ON.

If an overcurrent condition does not occur on any retry, the gate pin will proceed to open at the user defined slew rate.

### Overcurrent Fault Condition Flags

On any overcurrent violation, the X80000 will cut-off the GATE, turning off the voltage to the load, and setting all power good pins to their disabled state. In this condition, the fault-overcurrent bit (FOC) goes LOW. To clear FOC, remove the over current condition, then write to the control register. Refer to instructions on writing to the FDR (See Table 8).

When exceeding the overcurrent retry limit, the status bit “FAR_STAT” is set to ‘1’ and the $\overline{\text{FAR}}$ pin is asserted. To clear

FAR_STAT, write to the control register. Refer to instructions on writing to the FDR (See Table 9).

**TABLE 6. RETRY AND EVENT SEQUENCE OPTIONS**

| NR2 | NR1 | NR0 | $N_{RETRY}$ AND RETRY SEQUENCE OF EVENTS (FAILURE MODE) |
|---|---|---|---|
| 0 | 0 | 0 | Always Retry, Do Not assert $\overline{FAR}$ pin (Default) |
| 0 | 0 | 1 | $N_{RETRY}$ = 1 (one retry), assert $\overline{FAR}$ pin after $N_{RETRY}$, STOP retry, and shutoff GATE pin |
| 0 | 1 | 0 | $N_{RETRY}$ = 2 (two retries), assert $\overline{FAR}$ pin after $N_{RETRY}$, STOP retry, and shutoff GATE pin |
| 0 | 1 | 1 | $N_{RETRY}$ = 3 (three retries), assert $\overline{FAR}$ pin after $N_{RETRY}$, STOP retry, and shutoff GATE pin |
| 1 | 0 | 0 | $N_{RETRY}$ = 4 (four retries), assert $\overline{FAR}$ pin after $N_{RETRY}$, STOP retry, and shutoff GATE pin |
| 1 | 0 | 1 | $N_{RETRY}$ = 5 (five retries), assert $\overline{FAR}$ pin after $N_{RETRY}$, STOP retry, and shutoff GATE pin |
| 1 | 1 | 0 | Always Retry, assert $\overline{FAR}$ pin after 1st retry; clear $\overline{FAR}$ when FOC cleared, do not shutoff GATE pin. |
| 1 | 1 | 1 | $N_{RETRY}$ = 0 (no retry), asset $\overline{FAR}$, and shutoff GATE pin. |

**TABLE 7. RETRY EVENT DELAY OPTIONS**

| TSC1 | TSC0 | $t_{SC\_RETRY}$, DELAY BETWEEN RETRIES |
|---|---|---|
| 0 | 0 | 100 miliseconds |
| 0 | 1 | 500 miliseconds |
| 1 | 0 | 1 second |
| 1 | 1 | 5 seconds |

**TABLE 8. OVERCURRENT FLAG BIT**

| STATUS BIT | VIOLATION (ON) | NORMAL (OFF) |
|---|---|---|
| FOC | FOC = 0, when $V_{RSENSE} > V_{OC}$ | FOC = 1, when: $V_{RSENSE} < V_{OC}$ - 0.2V and reset by a write operation or hardshort retry is initiated. |

**TABLE 9. RETRY COUNT FAILURE STATUS BIT**

| STATUS BIT | CONDITION |
|---|---|
| FAR_STAT | if FAR_STAT = 1, $\overline{FAR}$ is asserted. if FAR_STAT = 0, $\overline{FAR}$ is deasserted |

### *Gate Drive Output Slew Rate (Inrush Current) Control*

The gate output drives an external N-Channel FET. The GATE pin goes high when no overcurrent, undervoltage or overvoltage conditions exist.

The X80000 provides an $I_{GATE}$ current of 50µA to provide on-chip slew rate control to minimize inrush current. This current is programmable from 10µA to 160uA (in 10µA steps) to allow the X80000 to support various load conditions (See Figure 23 and Figure 28). $I_{GATE}$ is chosen to limit the inrush current and to provide the best charge time for a given load, while avoiding overcurrent conditions. The user programs the $I_{GATE}$ current using four $I_{GATE}$ control bits.

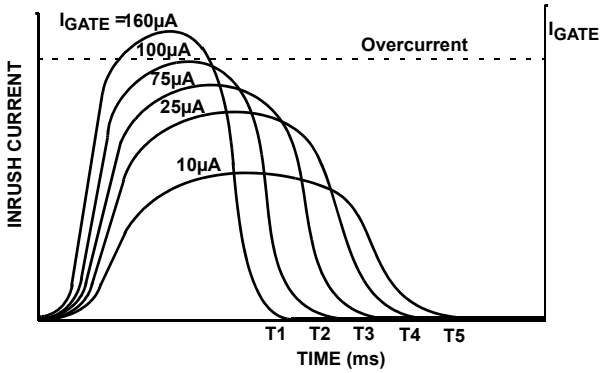



**FIGURE 28. SELECTING $I_{GATE}$ CURRENT FOR SLEW RATE CONTROL ON THE GATE PIN**

For applications that require different ramp rates during insertion and start-up and operations modes, the X80000 provides two external pins, IGQ1 and IGQ0, that allow the user to switch to different GATE currents on-the-fly by selecting one of four pre-selected $I_{GATE}$ currents. When IGQ0 and IGQ1 are left unconnected, the gate current is determined by the gate control bits. The other three settings are 10µA, 70µA and 150µA. Typically, the delay from IGQ1 and IGQ0 selection to a change in the GATE pin current is less than 1 µsecond.

### *Programmable Slew Rate (Gate) Control*

As shown in Figure 29, this circuit block contains a selectable current source ($I_{GATE}$) that drives the 50µA current into the GATE pin. This current provides a controlled slew rate for the FET.

X80000 allows the user to change the gate current to one of sixteen possible $I_{GATE}$ values. The options allow currents of between 10µA to 160µA in 10µA increments.

Once the overcurrent condition and the amount of load is known, an appropriate slew rate can be determined and

selected for the external FET. This will ensure proper operation to control Inrush currents during hot insertion modes.

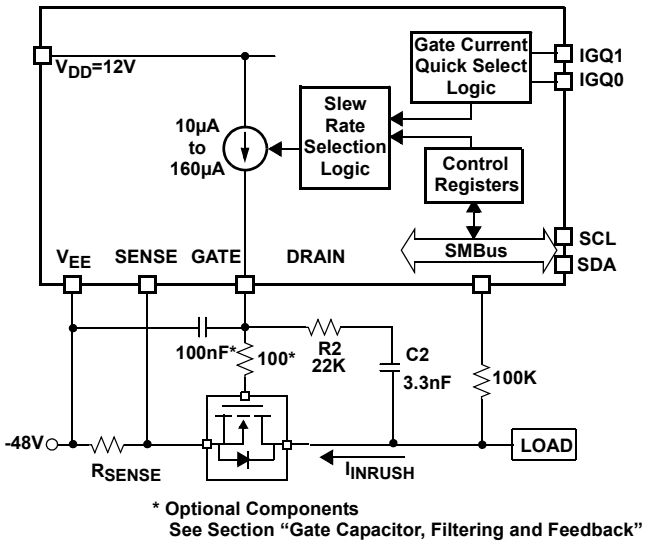



**FIGURE 29. PROGRAMMBLE SLEW RATE (INRUSH CURRENT) CONTROL**

### Software Slew Rate Control

Users can adjust the slew rate control by using an SMBus write command to change the slew rate control bits. This allows adaptation in the case of changing load conditions, creates a modular design for downstream DC-DC supplies, and provides control of the load on the hot voltage when slew rates vs. loads vary.

### Gate Capacitor, Filtering and Feedback

In Figure 29, the FET control circuit includes an FET feedback capacitor $C_2$, which provides compensation for the FET during turn on. The capacitor value depends on the load, the FET gate current, and the maximum desired inrush current.

The value of C2 can be selected with the following formula:

$$C2 = \frac{I_{GATE} \times C_{LOAD}}{I_{INRUSH}}$$

Where:

$I_{GATE}$ = FET Gate current

$I_{INRUSH}$ = Maximum desired inrush current

$C_{LOAD}$ = DC/DC bulk capacitance

With the X80000, there is some control of the gate current with the IGQ pins and IGx bits, so one selection of C2 can cover a wide range of possible loading conditions. Typical values for C2 range from 2.2 to 4.7nF.

When power is applied to the system, the FET tries to turn on due to its internal gate to drain capacitance (Cgd) and the feedback capacitor C2 (see Figure 29). The X80000 device, when powered, pulls the gate output low to prevent the gate voltage from rising and keep the FET from turning on.

However, unless $V_{DD}$ powers up very quickly, there will be a brief period of time during initial application of power when the X80000 circuits cannot hold the gate low. The use of an external capacitor (C1) prevents this. Capacitors C1 and C2 form a voltage divider to prevent the gate voltage from rising above the FET turn on threshold before the X80000 can hold the gate low. Use the following formula for choosing C1.

$$C1 = \frac{V1 - V2}{V2} C2$$

Where:

V1 = Maximum input voltage,

V2 = FET threshold Voltage,

C1 = Gate capacitor,

C2 = Feedback capacitor.

In a system where $V_{DD}$ rises very fast, a smaller value of C1 may suffice as the X80000 will control voltage at the gate before the voltage can rise to the FET turn on threshold. The circuit of Figure 29 assumes that the input voltage can rise to 80V before the X80000 sees operational voltage on $V_{DD}$. If C1 is used then the series resistor R1 will be required to prevent high frequency oscillations.

**TABLE 10. $I_{GATE}$ OUTPUT CURRENT OPTIONS**

| IG3 | IG2 | IG1 | IG0 | $I_{GATE}$ (µA) | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 10 | |
| 0 | 0 | 0 | 1 | 20 | |
| 0 | 0 | 1 | 0 | 30 | |
| 0 | 0 | 1 | 1 | 40 | |
| 0 | 1 | 0 | 0 | 50 | Default |
| 0 | 1 | 0 | 1 | 60 | |
| 0 | 1 | 1 | 0 | 70 | |
| 0 | 1 | 1 | 1 | 80 | |
| 1 | 0 | 0 | 0 | 90 | |
| 1 | 0 | 0 | 1 | 100 | |
| 1 | 0 | 1 | 0 | 110 | |
| 1 | 0 | 1 | 1 | 120 | |
| 1 | 1 | 0 | 0 | 130 | |
| 1 | 1 | 0 | 1 | 140 | |
| 1 | 1 | 1 | 0 | 150 | |
| 1 | 1 | 1 | 1 | 160 | |

### GATE Current Quick Selection

For applications that require different ramp rates during insertion and start-up and operations modes or those where the serial interface is not available, the X80000 provides two external pins, IGQ1 and IGQ0, that allow the system to switch

to different GATE current on-the-fly with pre-selected $I_{GATE}$ currents.

The IGQ1 and IGQ0 pins can be used to select from one of four set values.

| IGQ1 PIN | IGQ0 PIN | CONTENTS |
|---|---|---|
| 0 | 0 | Defaults to gate current set by IG3:IG0 bits |
| 0 | 1 | Gate Current is 10µA |
| 1 | 0 | Gate Current is 70µA |
| 1 | 1 | Gate Current is 150µA |

Typically, the delay from IGQ1 and IGQ0 selection to a change in the GATE pin current is less than 1 µsecond.

### *Drain Sense and Power Good Indicator*

The X80000 provides a drain sense and power good indicator circuit. The $\overline{PWRGD}$ signal asserts LOW when there is no overvoltage, no undervoltage, and no overcurrent condition, the Gate voltage exceeds VDD-1V, and the voltage at the DRAIN pin is less $V_{EE}+V_{DRAIN}$.

As shown in Figure 30, this circuit block contains a drain sense voltage trip point ($\Delta V_{DRAIN}$) and a gate voltage trip point ($\Delta V_{GATE}$), two comparators, and internal voltage references. These provide both a drain sense and a gate sense circuit to determine the whether the FET has turned on as requested. If so, the power good indicator ($\overline{PWRGD}$) goes active.

The drain sense circuit checks the DRAIN pin. If the voltage on this pin is greater that 1V above $V_{EE}$, then a fault condition exists.

The gate sense circuit checks the GATE pin. If the voltage on this pin is less than $V_{EE}$ - 1V, then a fault condition exists.

The $\overline{PWRGD}$ signal asserts (Logic LOW) only when all of the below conditions are true:

- there is no overvoltage or no undervoltage condition, (i.e. undervoltage < $V_{EE}$ < overvoltage.)
- There is no overcurrent condition (i.e. $V_{EE} - V_{SENSE} < V_{OC}$.)
- The FET is turned on (i.e. $V_{DRAIN} < V_{EE} + 1V$ and $V_{GATE} > V_{DD} - 1V$).

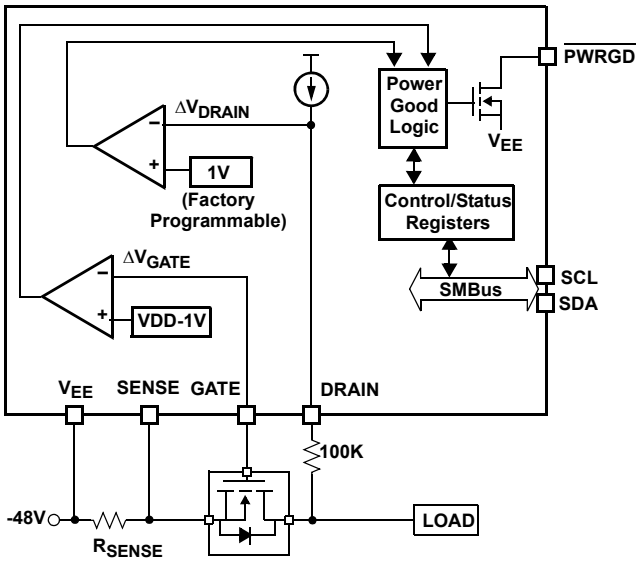



**FIGURE 30. DRAIN SENSE AND POWER GOOD INDICATOR**

### *Power On Reset and System Reset With Delay*

Application of power to the X80000 activates a Power On Reset circuit that pulls the $\overline{RESET}$ pin active. This signal, if used, provides several benefits.

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.
- It prevents communication to the EEPROM during unstable power conditions, greatly reducing the likelihood of data corruption on power up.

The SPOR/RESET circuit is activated when all voltages are within specified ranges and the following time-out conditions are met: $\overline{PWRGD}$ and $\overline{V1GOOD}$, $\overline{V2GOOD}$, $\overline{V3GOOD}$, and $\overline{V4GOOD}$. The SPOR/RESET circuit will then wait 100ms and assert the $\overline{RESET}$ pin. The SPOR delay may be changed by setting the TPOR bits in register CR2. The delay can be set to 100 ms, 500 ms, 1 second, or 5 seconds.

**TABLE 11. SPOR RESET DELAY OPTIONS**

| TPOR1 | TPOR0 | $t_{SPOR}$ DELAY BEFORE $\overline{RESET}$ ASSERTION |
|---|---|---|
| 0 | 0 | 100 miliseconds (default) |
| 0 | 1 | 500 miliseconds |
| 1 | 0 | 1 second |
| 1 | 1 | 5 seconds |

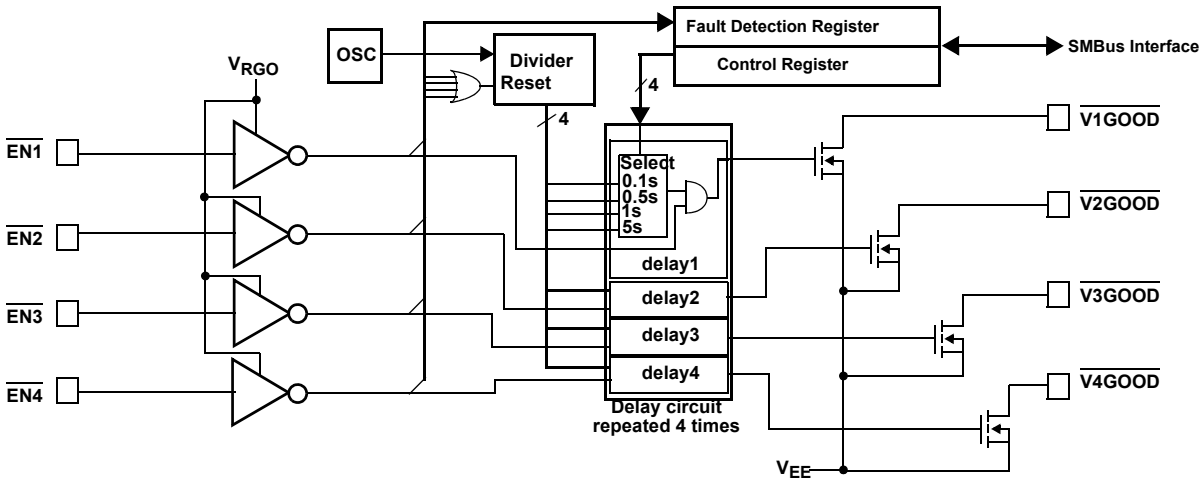



**FIGURE 32. VOLTAGE ENABLE CONTROL AND $\overline{\text{VGOOD}}$ OUTPUTS**

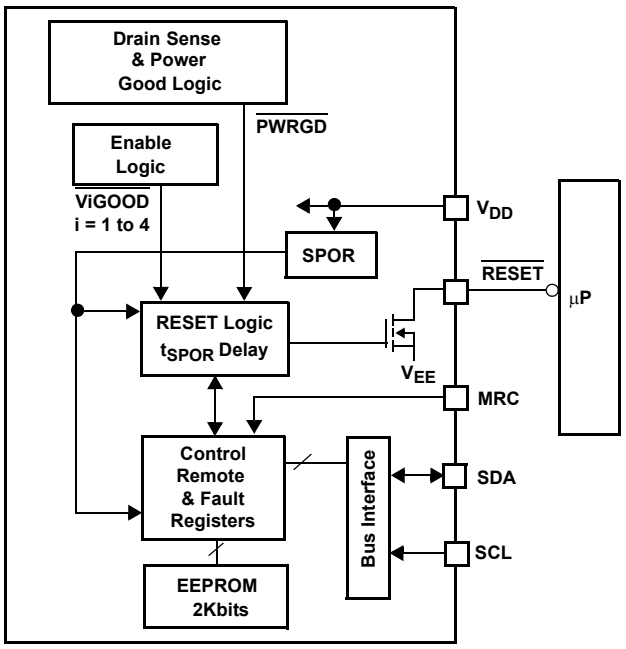



**FIGURE 31. POWER ON/SYSTEM RESET AND DELAY (BLOCK DIAGRAM)**

### *Quad Voltage Monitoring*

X80000 monitors 4 voltage enable inputs. When the $\overline{\text{ENi}}$ (i=1-4) input is detected to be below the input threshold, the output $\overline{\text{ViGOOD}}$ (i = 1 to 4) goes active. The $\overline{\text{ViGOOD}}$ signal is asserted after a delay of 100ms. This delay can be changed on each $\overline{\text{ViGOOD}}$ output individually with bits in register CR3. The delay can be 100ms, 500ms, 1s and 5s. The $\overline{\text{ViGOOD}}$ signal remains active low until $\overline{\text{ENi}}$ rises above threshold.

Once the $\overline{\text{PWRGD}}$ signal is asserted, the power sequencing of the DC-DC modules can commence. $\overline{\text{RESET}}$ will go active 100ms after all $\overline{\text{ViGOOD}}$ (i=1 to 4) outputs are asserted. This delay time can be changed by setting bits in register CR2 (See Figure 32).

As shown in Figure 32, this circuit block contains four separate voltage enable inputs, a time delay circuit, and an output driver.

**TABLE 12. ViGOOD OUTPUT TIME DELAY OPTIONS**

| TiD1 | TiD0 | $t_{DELAYi}$ |
|---|---|---|
| 0 | 0 | 100ms |
| 0 | 1 | 500ms |
| 1 | 0 | 1 secs |
| 1 | 1 | 5 secs |

where i is the ith voltage enable (i = 1 to 4).

### *Manual Reset and Remote Shutdown*

The manual reset option allows a hardware reset of either the Gate control or the $\overline{\text{PWRGD}}$ indicator. These can be used to recover the system in the event of an abnormal operating condition.

The remote shutdown feature of the X80000 allows smart power control remotely through the SMBus. The host system can either override the control of the FET, thus turning it off, or it can remove the override. Removing the override restarts the power up sequence.

The X80000 has two manual reset pins: $\overline{\text{MRH}}$ (manual reset hot side) and MRC (manual reset cold side). The $\overline{\text{MRH}}$ signal is used as a manual reset for the GATE pin. This pin is used to initiate Soft Reinsert. When $\overline{\text{MRH}}$ is pulled LOW the GATE pin will be pulled LOW. It also clears the Remote Shutdown Register (RSR) and the $\overline{\text{FAR}}$ signal. When the $\overline{\text{MRH}}$ pin goes

HIGH, it removes the override signal and the gate will turn on based on the selected gate control mechanism.

**TABLE 13. MANUAL RESET OF THE HOT SIDE (GATE SIGNAL)**

| MRH | GATE PIN | REQUIREMENTS |
|---|---|---|
| 1 | Operational | When $\overline{MRH}$ is HIGH the Manual Reset (Hot) function is disabled and the device operates normally |
| 0 | OFF | $\overline{MRH}$ must be held LOW minimum of 5µsecs to turn of the GATE |

The MRC signal is used as a manual reset for the $\overline{PWRGD}$ signal. This pin is used to initiate a Soft Restart. When the MRC is pulled HIGH, the $\overline{PWRGD}$ signal is pulled HIGH. When MRC pin goes LOW, the $\overline{PWRGD}$ pin goes low using the MRC pin has no affect on the FET gate control, so the FET remains on.

**TABLE 14. MANUAL RESET OF THE COLD SIDE ($\overline{PWRGD}$ SIGNAL)**

| MRC | PWRGD | Requirements |
|---|---|---|
| 1 | HIGH | MRC must be held HIGH minimum of 5µsecs to set $\overline{PWRGD}$ HIGH |
| 0 | Operational | When MRC is LOW the MRC function is disabled and the device operates normally |

### *Fault Detection*

The X80000 contains a Fault Detection Register (FDR) that provides the user the status of the causes for a $\overline{RESET}$ pin active (See Table 17).

At power-up, the FDR is defaulted to all “0”. The system needs to initialize the register to all “1” before the actual monitoring can take place. In the event that any one of the monitored sources fail, the corresponding bit in the register changes from a “1” to a “0” to indicate the failure (ViGOOD sources set the bit LOW when the ViGOOD goes LOW indicating a “good” status). When a RESET is detected by the main controller, the controller should read of the FDR and note the cause of the fault. After reading the register, the controller can reset the register bit back to all “1” in preparation for future monitored conditions.

### *Remote Shutdown*

The gate of the external MOSFET can be remotely shutdown by using a software command sequence. A byte write of ‘10101010’ (AAh) data to the Remote Shutdown Register (RSR) will shutdown the gate and the gate will be pulled low.

Activating the $\overline{MRH}$ pin or a writing 00h into the RSR will turn off the override signal and the gate will turn on based on the gate control mechanism.

The RSR powers up with ‘0’s in the register and its contents are volatile.

### *Flexible Power Sequencing of Multiple Power Supplies*

The X80000 provides several circuits such as multiple voltage enable pins, programmable delays, and a power good signals that can be used to set up flexible power sequencing schemes for downstream DC-DC supplies. Below are two examples:

1. Power Up of DC-DC Supplies In Parallel Sequencing Using Programmable Delays on Power Good (See Figure 33 and Figure 34).

   Several DC-DC power supplies and their respective power up start times can be controlled using the X80000 such that each of the DC-DC power supplies will start up following the issue of the $\overline{PWRGD}$ signal. The $\overline{PWRGD}$ signal is fed into the $\overline{ENi}$ inputs to the X80000. When $\overline{PWRGD}$ is valid, the internal voltage enable inputs issue $\overline{ViGOOD}$ signals after a time delay. The $\overline{ViGOOD}$ signals control the $\overline{ON}$/OFF pins of the DC-DC supplies. In the factory default condition, each DC/DC converter is instructed to turn on 100ms after the $\overline{PWRGD}$ goes active. However, each $\overline{ViGOOD}$ delay is individually selectable as 100ms, 500ms, 1s and 5s. The delay times are changed via the SMBus during calibration of the system.
2. Power Up of DC-DC Supplies Via Relay Sequencing Using Power Good and Voltage Enables (see Figure 35 and Figure 36).

   Several DC-DC power supplies and their respective power up start times can be controlled using the X80000 such that each of the DC-DC power supplies will start in a relay sequencing fashion. The 1st DC-DC supply will power up when $\overline{PWRGD}$ is LOW after a 100ms delay. Subsequent DC-DC supplies will power up after the prior supply has reached its operating voltage. One way to do this is by using an external CPU Supervisor (for example the Intersil X40430) to monitor the DC-DC output. When the DC/DC voltage is good, the supervisor output signals the X80000 $\overline{EN1}$ input to sequence the next supply. An opto-coupler is recommended in this connection for isolation. This configuration ensures that each subsequent DC-DC supply will power up after the preceding DC-DC supplys voltage output is valid. Again, the X80000 offers programmable delays for each voltage enable input that is selectable via the SMBus during calibration of the system.

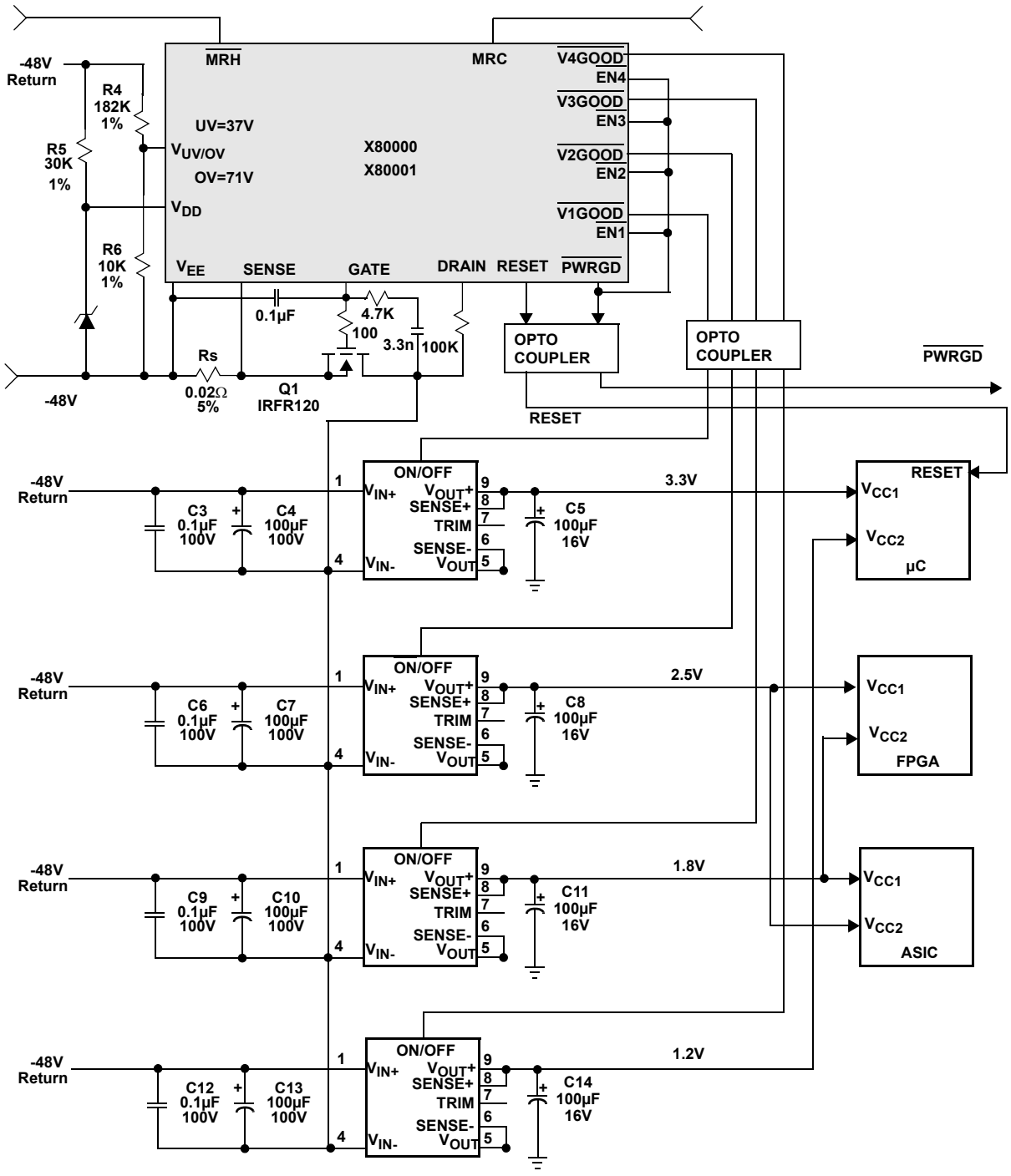



FIGURE 33. TYPICAL APPLICATION OF HOTSWAP AND DC-DC PARALLEL POWER SEQUENCING

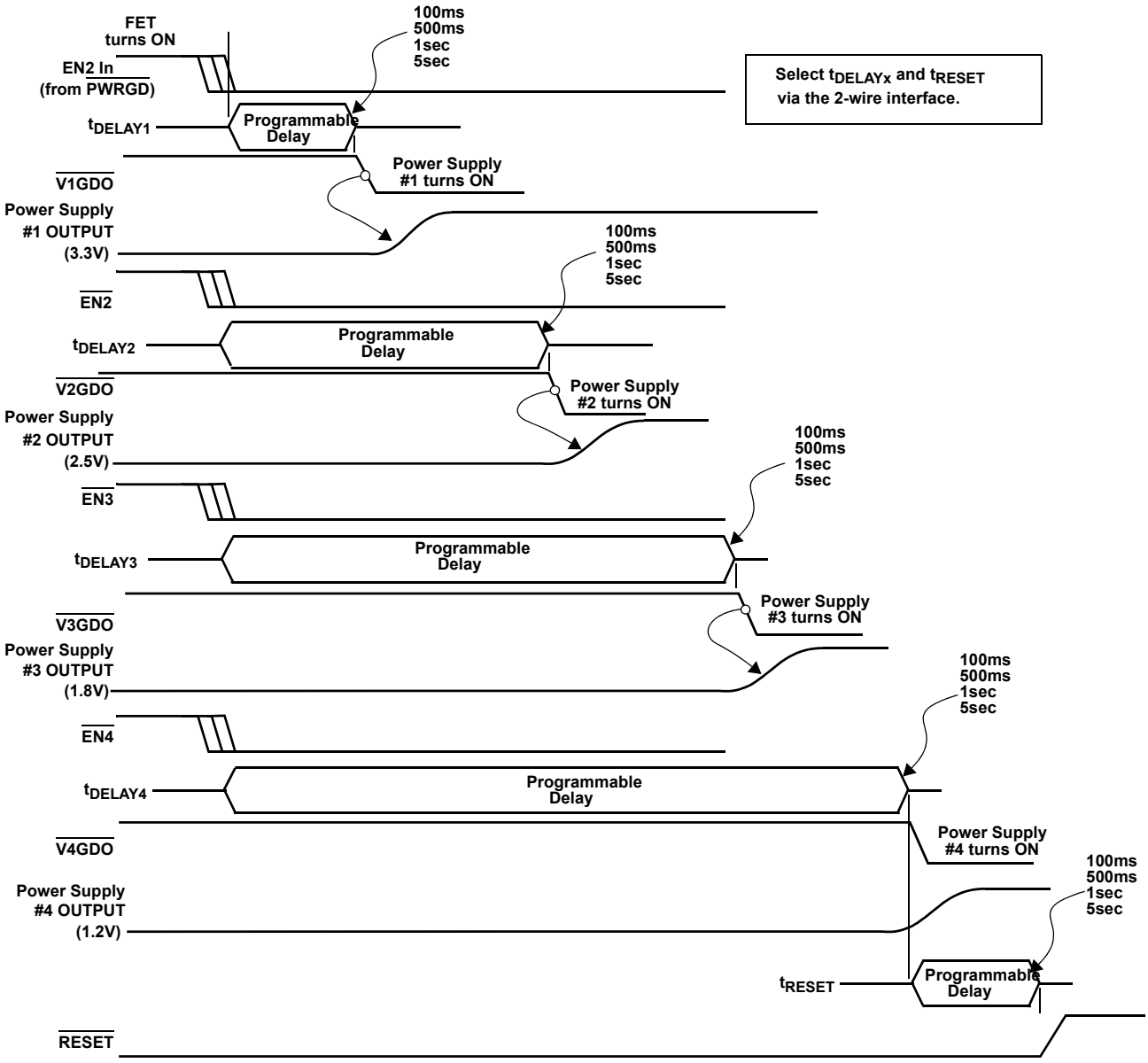



**FIGURE 34. PARALLEL SEQUENCING OF DC-DC SUPPLIES (TIMING)**

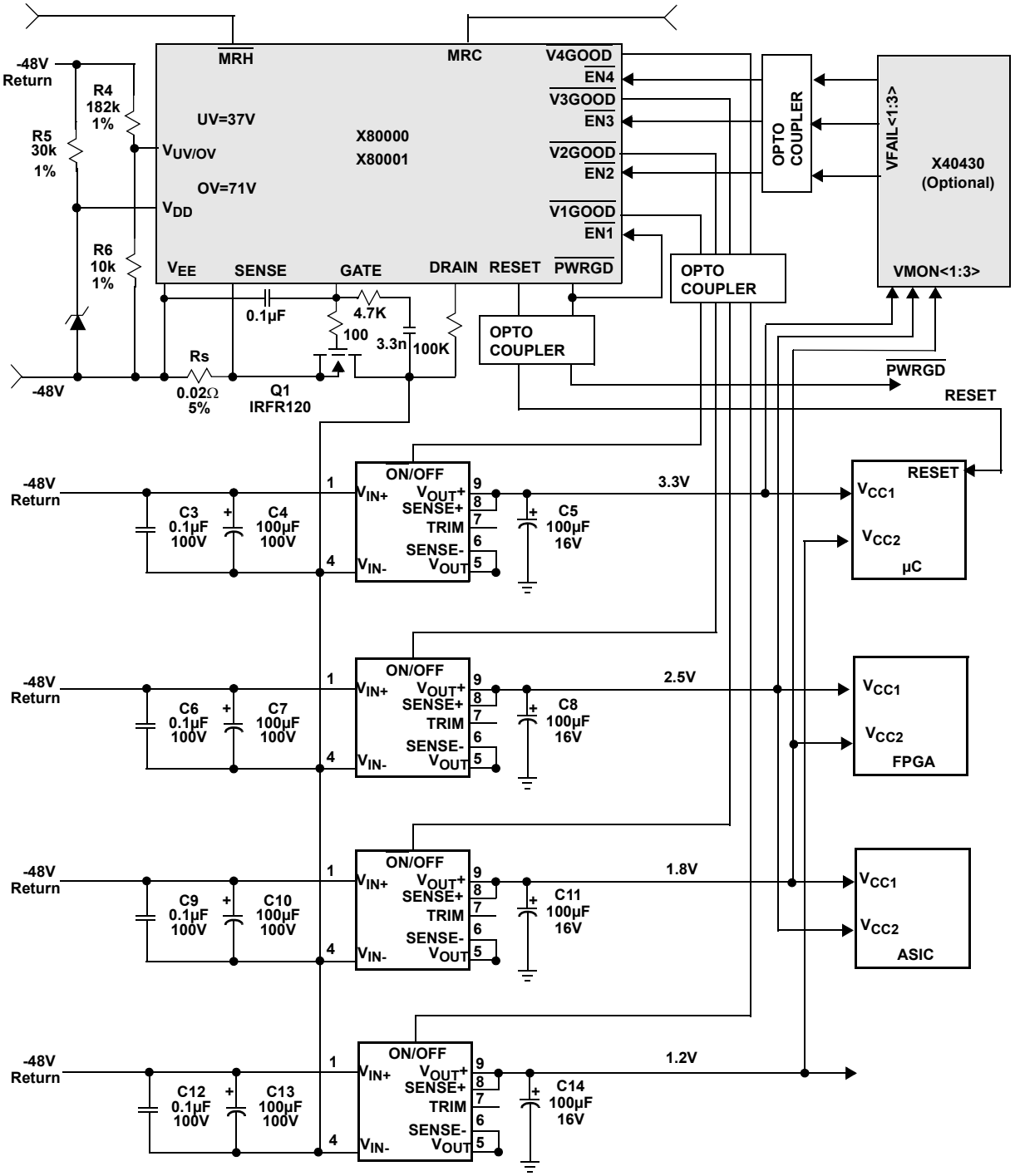



FIGURE 35. TYPICAL APPLICATION OF HOTSWAP AND DC-DC RELAY SEQUENCING

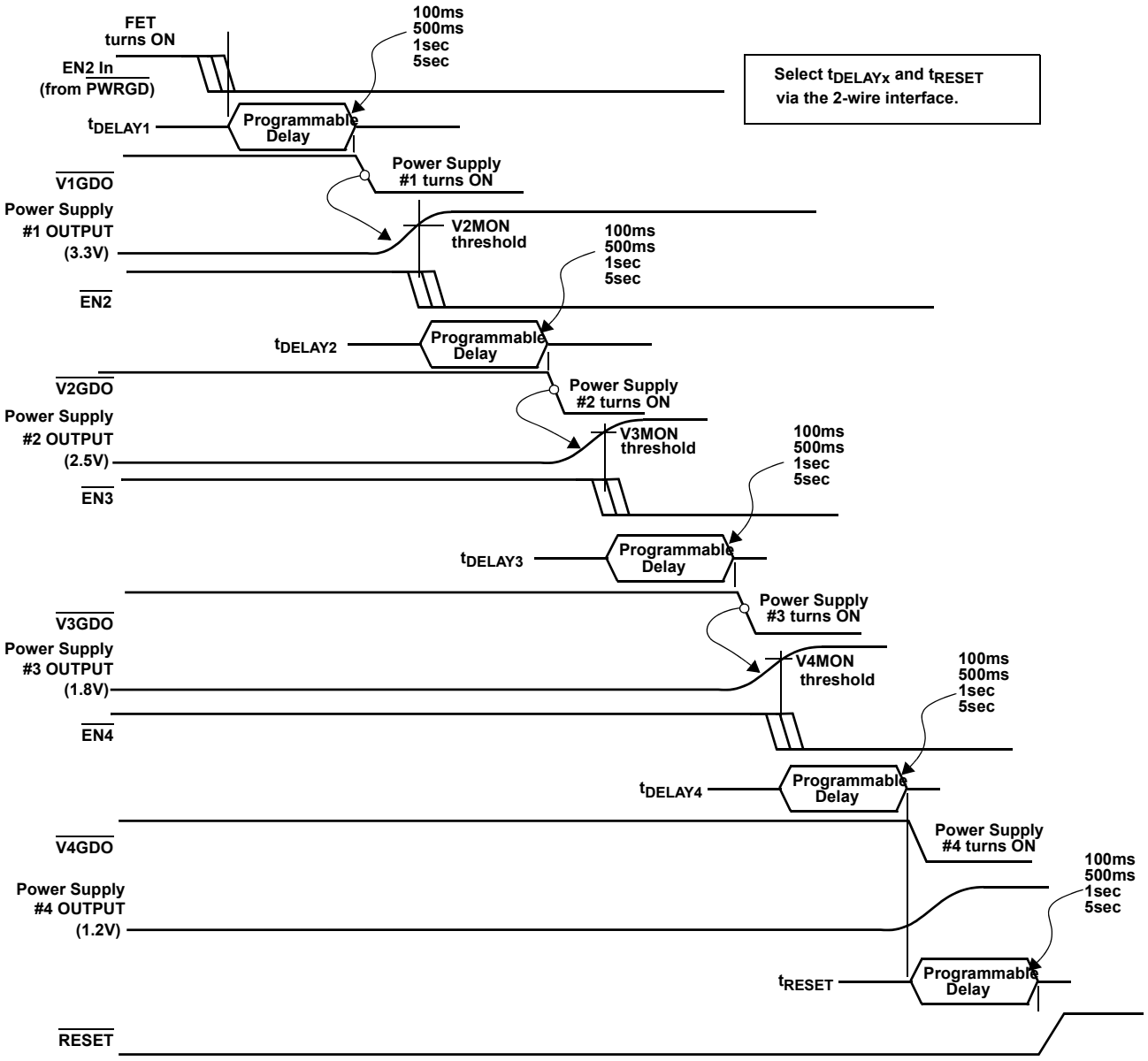



**FIGURE 36. RELAY SEQUENCING OF DC-DC SUPPLIES (TIMING)**

## *Control Registers and Memory*

The user addressable internal control, status and memory components of the X80000 can be split up into four parts:

- Control Register (CR)
- Fault Detection Register (FDR)
- Remote Shutdown Register (RSR)
- EEPROM array

### *Registers*

The Control Registers, Remote Shutdown Register and Fault Detection Register are summarized in Table 15. Changing bits in these registers change the operation of the device or clear fault conditions. Reading bits from these registers provides information about device configuration or fault conditions. Reads and writes are done through the SMBus serial port. It is important to remember that, in most cases, the SMBus serial port must be isolated between the X80000, which is referenced to -48V, and the system controller, which is referenced to ground.

All of the Control Register bits are nonvolatile (except for the WEL bit), so they do not change when power is removed.

The values of the Register Block can be read at any time by performing a random read (see Serial Interface) at the specific byte address location. Only one byte is read by each register read operation.

Bits in the registers can be modified by performing a single byte write operation directly to the address of the register and only one data byte can change for each register write operation.

**TABLE 15. REGISTER ADDRESS MAP**

| BYTE ADDR. | REGISTER NAME | DESCRIPTION | BIT | | | | | | | | MEMORY TYPE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 00H | CR0 | Control Register 0 | WEL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Volatile |
| 01H | CR1 | Control Register 1 | WPEN | 0 | 0 | BP1 | BP0 | NR2 | NR1 | NR0 | EEPROM |
| 02H | CR2 | Control Register 2 | IG3 | IG2 | IG1 | IG0 | TPOR1 | TPOR0 | TSC1 | TSC0 | EEPROM |
| 03H | CR3 | Control Register 3 | T4D1 | T4D0 | T3D1 | T3D0 | T2D1 | T2D0 | T1D1 | T1D0 | EEPROM |
| 04H | CR4 | Control Register 4 | VS1 | VS0 | F1 | F0 | 0 | 0 | 0 | 0 | EEPROM |
| 05H | RSR (Note 1) | Remote Shutdown Register | AAh: Override FET control and shutdown the FET<br>00h: Turn off override<br>(All other data combinations to RSR are reserved.) | | | | | | | | Volatile |
| FF | FDR | Fault Detection Register | FOV | FUV1/2 | FOC | FAR_ STAT | V40S | V30S | V20S | V10S | Volatile |
| (1) This register is write only | | | | | | | | | | | |

**TABLE 16. FAULT DETECTION BITS SUMMARY**

| SYMBOL | LOCATION(S) | | CONTROL FUNCTION/ STATUS INDICATION | DESCRIPTION |
|---|---|---|---|---|
| | REGISTER | BITS | | |
| FAR_STAT | FDR | 4 | Retry Violation | FAR_STAT = 0 : Failure After retry detected (must be preset to 1). |
| FOC | FDR | 5 | Overcurrent Violation | FOC = 0 : Over current detected (must be preset to 1). |
| FOV | FDR | 7 | Overvoltage Violation | FOV = 0 : Over voltage detected (must be preset to 1). |
| FUV1/2 | FDR | 6 | Undervoltage Violation | FUV1/2 = 0 : Under voltage detected (must be preset to 1). |
| V1OS | FDR | 0 | 1st Voltage Good | V1OS = 0 : $\overline{\text{V1GOOD}}$ pin has been asserted (must be preset to 1). |
| V2OS | FDR | 1 | 2nd Voltage Good | V2OS = 0 : $\overline{\text{V2GOOD}}$ pin has been asserted (must be preset to 1). |
| V3OS | FDR | 2 | 3rd Voltage Good | V3OS = 0 : $\overline{\text{V3GOOD}}$ pin has been asserted (must be preset to 1). |
| V4OS | FDR | 3 | 4th Voltage Good | V4OS = 0 : $\overline{\text{V4GOOD}}$ pin has been asserted (must be preset to 1). |

**TABLE 17. HARDWARE/SOFTWARE CONTROL AND FAULT DETECTION BITS SUMMARY**

| SYMBOL | LOCATION(S) | | CONTROL FUNCTION/ STATUS INDICATION | DESCRIPTION |
|---|---|---|---|---|
| | REGISTER | BITS | | |
| **SOFTWARE CONTROL BITS** | | | | |
| F0<br>F1 | CR4 | 5:4 | Insertion Current Filter | F1=0, F0=0 ; $t_{NF}$ = 0<br>F1=0, F0=1 ; $t_{NF}$ = 5µs<br>F1=1, F0=0 ; $t_{NF}$ = 10µs<br>F1=1, F0=1 ; $t_{NF}$ = 20µs |
| IG0<br>IG1<br>IG2<br>IG3 | CR2 | 7:4 | Gate Current Select | See Table 10. |
| NR0<br>NR1<br>NR2 | CR1 | 2:0 | Retry Sequence Options | See Table 6. |
| T1D0<br>T1D1 | CR3 | 1:0 | $\overline{\text{V1GOOD}}$ Time Delay | TiD1=0, TiD0=0 : $\overline{\text{ViGOOD}}$ delay = 100ms<br>TiD1=0, TiD0=1 : $\overline{\text{ViGOOD}}$ delay = 500ms<br>TiD1=1, TiD0=0 : $\overline{\text{ViGOOD}}$ delay = 1s<br>TiD1=1, TiD0=1 : $\overline{\text{ViGOOD}}$ delay = 5s |
| T2D0<br>T2D1 | CR3 | 3:2 | $\overline{\text{V2GOOD}}$ Time Delay | |
| T3D0<br>T3D1 | CR3 | 5:4 | $\overline{\text{V3GOOD}}$ Time Delay | |
| T4D0<br>T4D1 | CR3 | 7:6 | $\overline{\text{V4GOOD}}$ Time Delay | |
| TPOR0<br>TPOR1 | CR2 | 3:2 | $\overline{\text{RESET}}$ delay time | TPOR1=0, TPOR0=0 : $\overline{\text{RESET}}$ delay = 100ms<br>TPOR1=0, TPOR0=1 : $\overline{\text{RESET}}$ delay = 500ms<br>TPOR1=1, TPOR0=0 : $\overline{\text{RESET}}$ delay = 1s<br>TPOR1=1, TPOR0=1 : $\overline{\text{RESET}}$ delay = 5s |
| TSC0<br>TSC1 | CR2 | 1:0 | Overcurrent Retry Delay Time | TSC1=0, TSC0=0 ; $t_{SC\_RETRY}$ = 100ms<br>TSC1=0, TSC0=1 ; $t_{SC\_RETRY}$ = 500ms<br>TSC1=1, TSC0=0 ; $t_{SC\_RETRY}$ = 1s<br>TSC1=1, TSC0=1 ; $t_{SC\_RETRY}$ = 5s |
| VS0<br>VS1 | CR4 | 7:6 | Insertion Overcurrent Limit | VS1=0, VS0=0 ; Insertion Overcurrent Limit = 1X<br>VS1=0, VS0=1 ; Insertion Overcurrent Limit = 2X<br>VS1=1, VS0=0 ; Insertion Overcurrent Limit = 3X<br>VS1=1, VS0=1 ; Insertion Overcurrent Limit = 4X |
| WEL | CR0 | 7 | Write Enable | WEL = 1 enables write operations to the control registers and EEPROM.<br>WEL = 0 prevents write operations. |
| WPEN | CR1 | 7 | Write Protect | WPEN = 1 (and WP pin HIGH) prevents writes to the control registers and the EEPROM. |
| BP1<br>BP0 | CR1 | 4:3 | EEPROM Block Protect | BP1=0, BP0=0 : No EEPROM memory protected.<br>BP1=0, BP0=1 : Upper 1/4 of EEPROM memory protected<br>BP1=1, BP0=0 : Upper 1/2 of EEPROM memory protected.<br>BP1=1, BP0=1 : All of EEPROM memory protected. |
| **HARDWARE SELECT BITS** | | | | |
| IGQ0<br>IGQ1 | Input pins | | Gate Current Select | IGQ1=0, IGQ0=0 : $I_{GATE}$ = set by IG0-IG3<br>IGQ1=0, IGQ0=1 : $I_{GATE}$ = 10µA<br>IGQ1=1, IGQ0=0 : $I_{GATE}$ = 70µA<br>IGQ1=1, IGQ0=1 : $I_{GATE}$ = 150µA |
| BATTON | Input pin | | Main or Battery | BATTON = 0 ; Undervoltage Threshold = $V_{UV1}$<br>BATTON = 1 ; Undervoltage Threshold = $V_{UV2}$ |

## Memory

The X80000 contains a 2kbit EEPROM memory array. This array can contain information about manufacturing location and dates, board configuration, fault conditions, service history, etc. Access to this memory is through the SMBus serial port. Read and write operations are similar to those of the control registers, but a single command can write up to 16 bytes at one time. A single read command can return the entire contents of the EEPROM memory.

### Register and Memory Protection

In order to reduce the possibility of inadvertent changes to either a control register of the contents of memory, several protection mechanisms are built into the X80000. These are a Write Enable Latch, Block Protect bits, a Write Protect Enable bit and a Write Protect pin.

### WEL: Write Enable Latch

A write enable latch (WEL) bit controls write accesses to the nonvolatile registers and the EEPROM memory array in the X80000. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address (registers or memory) will be ignored. The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the control register 0 (CR0). It is important to write only 00h or 80h to the CR0 register.

Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again.

Note, a write to FDR or RSR does not require that WEL=1.

### BP1 and BP0: Block Protect Bits

The Block Protect Bits, BP1 and BP0, determines which blocks of the memory array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of four segments of the array.

| BP1 | BP0 | PROTECTED ADDRESSES (SIZE) | ARRAY LOCK |
|---|---|---|---|
| 0 | 0 | None (Default) | None (Default) |
| 0 | 1 | C0h - FFh (64 bytes) | Upper 1/4 |
| 1 | 0 | 80h - FFh (128 bytes) | Upper 1/2 |
| 1 | 1 | 00h - FFh (256 bytes) | All |

### WPEN: Write Protect Enable

The Write Protect pin and Write Protect Enable bit in the CR1 register control the Programmable Hardware Write Protect feature. Hardware Protection is enabled when the WP pin is HIGH and WPEN bit is HIGH and disabled when WP pin is LOW or the WPEN bit is LOW. When the chip is Hardware Write Protected, non-volatile writes to all control registers (CR1, CR2, CR3, and CR4) are disabled including BP bits, the WPEN bit itself, and the blocked sections in the memory Array. Only the section of the memory array that are not block protected can be written.

**TABLE 18. WRITE PROTECT CONDITIONS**

| WEL | WP | WPEN | MEMORY ARRAY NOT BLOCK PROTECTED | MEMORY ARRAY BLOCK PROTECTED | WRITES TO CR1, CR2, CR3, CR4 | PROTECTION |
|---|---|---|---|---|---|---|
| LOW | X | X | Writes Blocked | Writes Blocked | Writes Blocked | Hardware |
| HIGH | LOW | X | Writes Enabled | Writes Blocked | Writes Enabled | Software |
| HIGH | HIGH | LOW | Writes Enabled | Writes Blocked | Writes Enabled | Software |
| HIGH | HIGH | HIGH | Writes Enabled | Writes Blocked | Writes Blocked | Hardware |

## Bus Interface Information

### Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

### Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (See Figure 37).

### Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH, followed by a HIGH to LOW transition of SCL. The stop condition is also used to place the device into the Standby power mode after a read sequence.

### Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (See Figure 38).

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for the Slave Address Byte when the Device Identifier and/or Select bits are incorrect.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

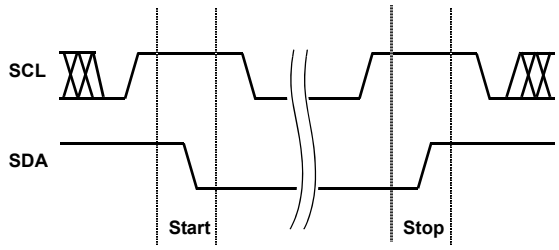



FIGURE 37. VALID START AND STOP CONDITIONS

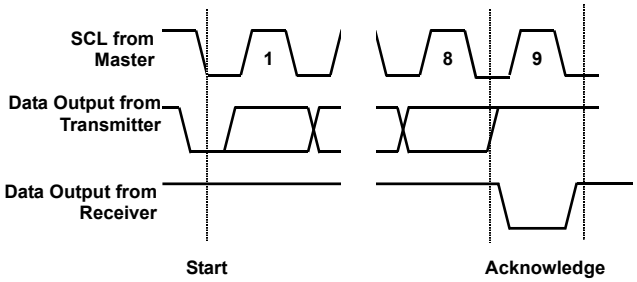



FIGURE 38. ACKNOWLEDGE RESPONSE FROM RECEIVER

## Device Addressing

### Addressing Protocol Overview

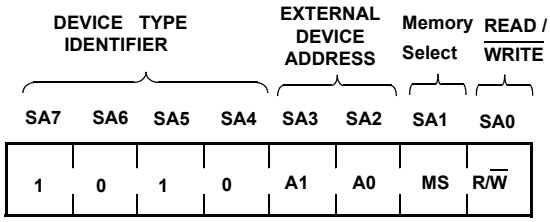
Depending upon the operation to be performed on each of these individual parts, a 1, 2 or 3 Byte protocol is used. All operations however must begin with the Slave Address Byte being clocked into the SMBus port on the SCL and SDA pins. The Slave address selects the part of the device to be addressed, and specifies if a Read or Write operation is to be performed.

### Slave Address Byte

Following a START condition, the master must output a Slave Address Byte. This byte consists of three parts:

- The Device Type Identifier which consists of the most significant four bits of the Slave Address (SA7 - SA4). The Device Type Identifier MUST be set to 1010 in order to select the device.
- The next two bits (SA3 - SA2) are slave address bits. The bits received via the SMBus are compared to A0 and A1 pins and must match or the communication is aborted.
- The next bit, SA1, selects the device memory sector. There are two addressable sectors: the memory array and the control, fault detection and remote shutdown registers.
- The Least Significant Bit of the Slave Address (SA0) Byte is the R/W bit. This bit defines the operation to be performed.

When the R/W bit is “1”, then a READ operation is selected. A “0” selects a WRITE operation (Refer to Figure 39).




| INTERNAL ADDRESS (SA1) | INTERNALLY ADDRESSED DEVICE |
|---|---|
| 0 | EEPROM Array |
| 1 | Control Register,<br>Fault Detection Register,<br>Remote Shutdown Register |

| BIT SA0 | OPERATION |
|---|---|
| 0 | WRITE |
| 1 | READ |

**FIGURE 39. SLAVE ADDRESS FORMAT**

### *Serial Write Operations*

In order to perform a write operation to either a Control Register or the EEPROM array, the Write Enable Latch (WEL) bit must first be set.

Writes to the WEL bit do not cause a high voltage write cycle, so the device is ready for the next operation immediately after the stop condition.

#### Byte Write

For a write operation, the device requires the Slave Address Byte and a Word Address Byte. This gives the master access to any one of the words in the array. After receipt of the Word Address Byte, the device responds with an acknowledge, and awaits the next eight bits of data. After receiving the 8 bits of the Data Byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance.

A write to a protected block of memory will suppress the acknowledge bit.

#### Page Write

The device is capable of a page write operation (See Figure 40). It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to ‘0’ on the same page (See Figure 41).

This means that the master can write 16 bytes to the page starting at any location on that page. If the master begins writing at location 10, and loads 12 bytes, then the first 6 bytes are written to locations 10 through 15, and the last 6 bytes are written to locations 0 through 5. Afterwards, the address counter would point to location 6 of the page that was just written. If the master supplies more than 16 bytes of data, then new data overwrites the previous data, one byte at a time.

The master terminates the Data Byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle.

#### Stop and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be effected.

#### Acknowledge Polling

The disabling of the inputs during high voltage cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master’s byte load operation, the device initiates the internal high voltage cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation (See Figure 44).

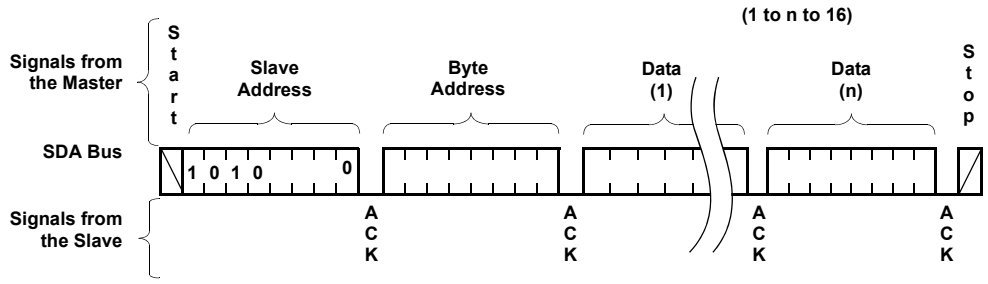



FIGURE 40. PAGE WRITE OPERATION

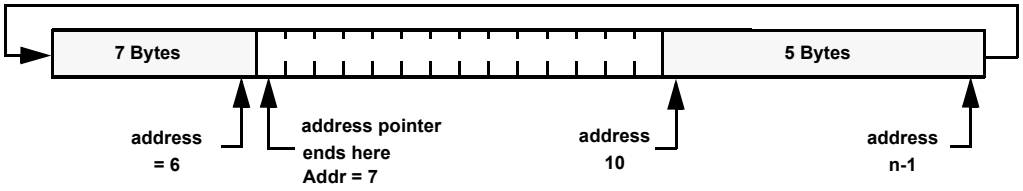



FIGURE 41. WRITING 12 BYTES TO A 16-BYTE PAGE STARTING AT LOCATION 10

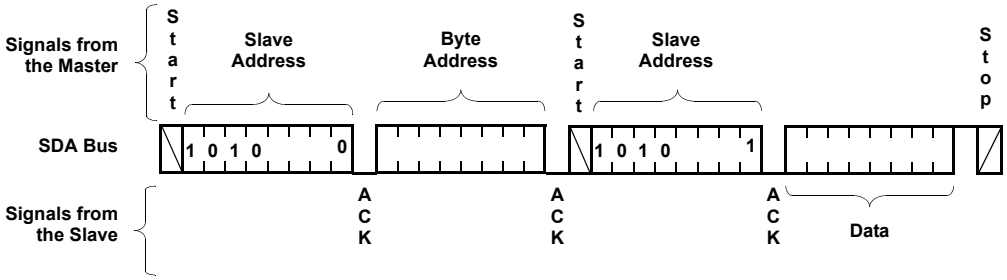



FIGURE 42. RANDOM ADDRESS READ SEQUENCE

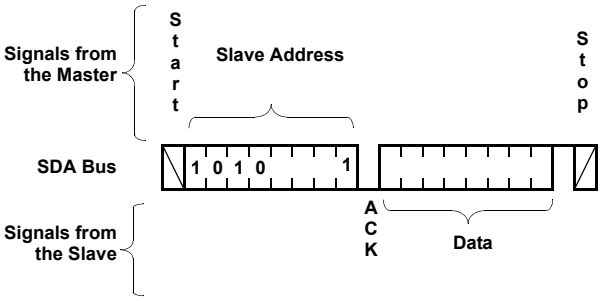



FIGURE 43. CURRENT ADDRESS READ SEQUENCE

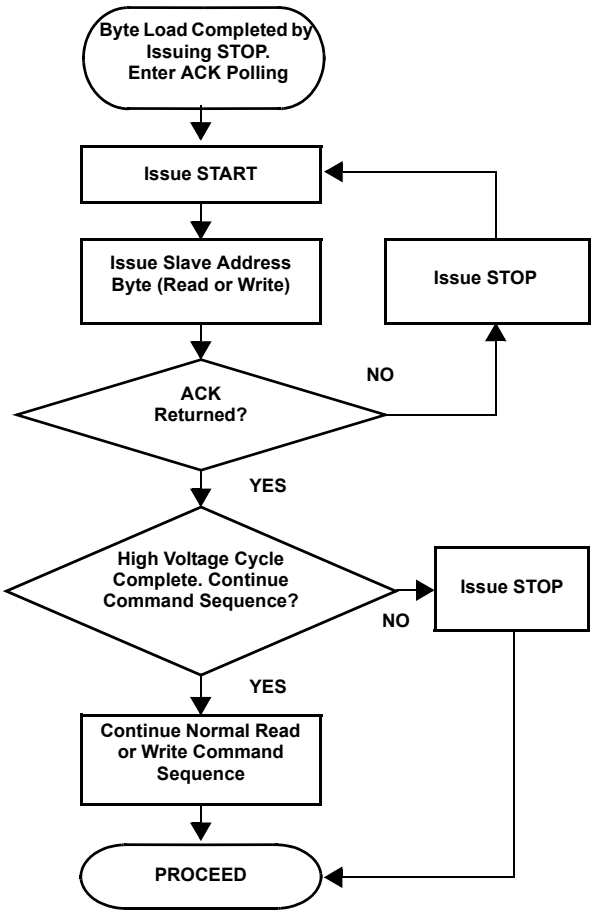



**FIGURE 44. ACKNOWLEDGE POLLING SEQUENCE**

### *Serial Read Operations*

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

#### Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. See Figure 42 for the address, acknowledge, and data transfer sequence.

#### Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power up, the address of the address counter is undefined, requiring a read or write operation for initialization.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. See Figure 43 or the address, acknowledge, and data transfer sequence.

### *Operational Notes*

The device powers-up in the following state:

- The device is in the low power standby state.
- The WEL bit is set to ‘0’. In this state, it is not possible to write to the device.
- SDA pin is the input mode.

### *Data Protection*

The following circuitry has been included to prevent inadvertent writes:

- The WEL bit must be set to allow write operations.
- The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.

## *Packaging Information*

**32-Lead Very Very Thin Quad Flat No Lead Package**
**7mm x 7mm Body with 0.65mm Lead Pitch**