TFT-LCD Power Supply with VCOM Amplifier

Product Data

VPA2000

Features

- 2A high efficiency boost regulator with integrated switch for AVDD
- 1.2V low-power regulator for DisplayPort TCON
- 2.5V, 300mA LDO for DisplayPort TCON
- Built-in high speed VCOM buffer
- External 2x charge pump for VGH
- Negative regulator for VGL
- Over-current, over-voltage, and over-temperature protection
- Built-in soft start
- Reset output for DisplayPort TCON
- QFN-24, 4x4mm, Pb-free (RoHS compliant) package

Applications

- DisplayPort devices
- TFT-LCD display panels for notebooks
- TFT-LCD display panels for monitors

Description

The VPA2000 is a 6-output power management IC for TFT-LCD panels. It is integrated into a 24 lead 4x4mm QFN package to provide a small-footprint, low-temperature, and low-cost solution.

The current mode control dc-dc step-up switching regulator (boost) is designed to deliver the AVDD source driver voltage with high efficiency. The 1.2MHz switching frequency allows for a small external inductor to meet PCB area and height requirements.

The negative gate drive voltage (VGL) is regulated by the on-board linear regulator. A built-in high speed VCOM buffer provides the voltage to drive the capacitive backplane of the TFT-LCD panel. Both VGL and VCOM output voltages can be adjusted by an external resistor divider.

A simple, low-cost, external 2x charge pump supplies the positive gate drive voltage (VGH). The internal 2.5V fixed output LDO and 1.2V fixed output charge pump supply the core voltages for the timing controller (TCON). The 1.2V charge pump dissipates approximately 80% less power than a traditional LDO solution.

Block Diagram

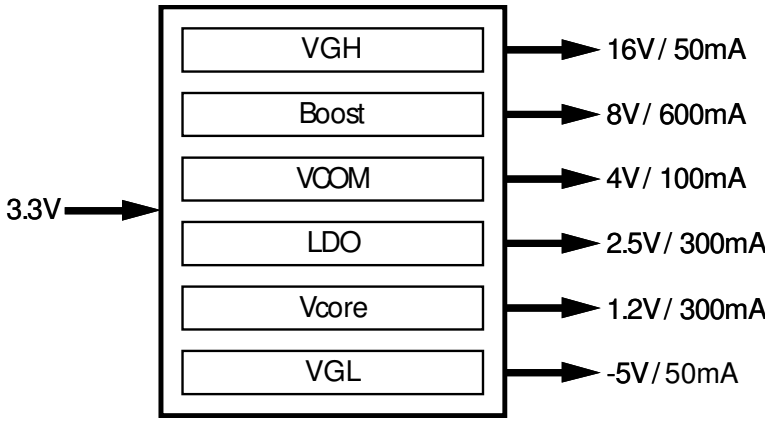

Figure 1. VPA2000 Block Diagram

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Revision History

March 2010 – Rev 1.0: Initial Version

ABSOLUTE MAXIMUM RATINGS

Table 1. Absolute Maximum Ratings Summary

PIN	MAXIMUM RATING [NOTE 1]
Input Voltage, VIN1, VIN2 to GND	-0.3V to 6V
SWN, INP1, INN1, OUT1, VGLREG, AVDD to GND	-0.3V to +24V
ON to GND	-0.3V to +27V
All other pins to GND	-0.3V to VIN+0.3V
Operating Ambient Temperature Range	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Junction Temperature	-40°C to +125°C
Lead Temperature (10 seconds)	+260°C
Maximum Power Dissipation	Internally limited [Note 2]

[Note 1] Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Note 2] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)}-T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Table 2. Package Thermal Resistivity

PACKAGE	THERMAL RESISTIVITY (Θ_{JA}) [NOTE 3]
QFN-24 4mm x 4mm	43.2 °C/W

[Note 3] This thermal rating was calculated based on JEDEC standard conditions (EIA-JESD 51-2 for natural convection & JESD 51-6 for forced convection). The board type is 2S2P recommended by JEDEC (4-layers: 2 oz copper surface traces/ 1 oz copper buried planes, 4" x 4.5" board size). Actual thermal resistivity will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables.

SPECIFICATION TABLE

V_{IN} = 2.7V to 4.0V. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 3. General Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
V_{IN}	Operating input voltage range		◙	2.7		4.0	V
I_{Q_VIN}	V_{IN} quiescent current	V_{IN} = 2.7V to 4.0V			3		mA

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

V_{IN} = 2.7V to 4.0V; C_{IN} = 10µF, C_{AVDD} = 22µF. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 4. Step-up Switching Regulator (Boost) Specification

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
A_{VDD}	Output voltage range					16	V
V_{FBB}	FBB reference voltage	Measure V_{COMP}, V_{FBB} = V_{COMP}		1.188	1.2	1.212	V
	Line regulation	I_{AVDD} = 100mA, V_{IN} = 3V to 4V			0.2		%
	Load regulation	I_{AVDD} = 50mA to 200mA, A_{VDD} = 8V			0.2		%
	Overall accuracy (Line, Load, Temperature)		◙	-3		3	%
I_{FBB_LEAK}	FBB pin input leakage current	V_{FBB} = 0.5V to 1.5V	◙	-100		100	nA
$R_{DS(ON)}$	N-channel switch ON-resistance	V_{IN} = 3.3V			0.2	0.35	Ω
I_{CL}	N-channel switch current limit	V_{FBB} = 1.1V, V_{RLIM} = V_{IN}	◙	1.8	2.35	2.8	A
I_{SW_LEAK}	SWN pin leakage current	V_{FBB} = 1.4V, V_{SWN} = 20V	◙		0.1	1	µA
f_{OSC}	Switching frequency				1.2		MHz
D_{MAX}	Maximum duty cycle		◙	86		93	%
t_{MIN}	Minimum on-time				50		ns
g_m	Error amplifier transconductance				1600		µS
I_{SS}	COMP soft start source current	During soft start			2		µA
OVP	AVDD over-voltage trip point	Measure at AVDD pin Vin = 3.3V	◙	18	19.5	21	V
	AVDD trip point hysteresis				1.7		V
V_{FBB_FAULT}	FBB fault trip point	Measure at FBB pin	◙	0.95	1	1.05	V

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

VIN = 2.7V to 4.0V; C_{LDO} = 1µF. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 5. Low Voltage Linear Regulator

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
I_{OUT_MAX}	Maximum LDO output current	3.0V < V_{IN} < 4.0V		300			mA
		2.7V < V_{IN} ≤ 3.0V		150			mA
	Output voltage setpoint accuracy		◙	-4		4	%
	Output voltage line regulation	V_{IN} = 2.7V to 4.0V			0.3		%
	Output voltage load regulation	I_{LDO} = 0 to 300mA			0.3		%
V_{DO}	Output dropout voltage	I_{LDO} = 300mA [Note 5]	◙			500	mV
I_{SC}	Short circuit current	V_{LDO} = 0V, V_{IN} = 3.3V		300		600	mA
PSRR	Power supply rejection ratio	Freq = 120Hz			70		dB

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

[Note 5] LDO dropout voltage is the minimum input to output differential voltage to keep the output voltage as a 2% reduction from a nominal level measured at V_{IN} = V_{LDO}+1V.

V_{IN} = 2.7V to 4.0V; C_{GL} = 1µF; C_{VGLREG} = 0.1µF. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 6. Negative High Voltage Linear Regulator / Controller

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
V_{FBVGL_OS}	FBVGL offset voltage		◙	-15		15	mV
	Output voltage line regulation	V_{IN} = 3.0V to 3.6V			0.2		%
	Output voltage load regulation	I_{GL} = 0 to 20mA			0.3		%
V_{DO}	Output dropout voltage	I_{GL} = 10mA [Note 6][Note 7]			500		mV
I_{OUT_MAX}	Maximum output current	V_{VGLREG} = 4V, V_{FBVGL} = 0.1V		30			mA
$R_{DS(ON)}$	N-channel switch ON-resistance	I_{VGLREG} = 10mA			20		Ω

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

[Note 6] Guaranteed by design, not 100% production tested.

[Note 7] Negative linear regulator dropout voltage is the minimum A_{VDD} to |V_{GL}| differential voltage to keep |V_{GL}| as a 2% reduction from a nominal level measured at V_{ADDD}=|V_{GL}|+2V.

V_{IN} = 2.7V to 4.0V; C_{REF} = 0.1µF. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 7. Reference Output

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
V_{REF}	Output voltage				1.2		V
	Output voltage accuracy	V_{IN} = 3.0V to 3.6V	◙	-3		3	%
	Output voltage line regulation	V_{IN} = 3.0V to 4.0V	◙			0.2	%
	Output voltage load regulation	I_{REF} = 50 to 100µA	◙			0.3	%
I_{REF_SINK}	V_{REF} pin sink current	V_{IN} = 1.8V		10			µA
I_{REF_SOURCE}	V_{REF} pin source current		◙	200			µA

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

V_{IN} = 2.7V to 4.0V; A_{VDD} = 6.5V to 16V; C_{OUT1} = 1µF. Unless otherwise specified, all specifications are tested under T_A = 25°C. The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 8. VCOM Buffer

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
V_{AVDD}	A_{VDD} input range	V_{COM} = A_{VDD}/2	◙	6.5		16	V
I_{AVDD}	A_{VDD} supply current				0.5	0.85	mA
V_{OS}	Input offset voltage	I_{COM} = 0mA V_{INP1} = 1.8V to A_{VDD}-1.8V	◙	-12		12	mV
		I_{COM} = +50mA V_{INP1} = 1.8V to A_{VDD}-1.8V	◙	-75	-50		mV
		I_{COM} = -50mA V_{INP1} = 1.8V to A_{VDD}-1.8V	◙		50	75	mV
I_{BIAS}	Input bias current	A_{VDD} = 6.5V to 18V	◙	-200		200	nA
V_{CM}	Common mode input range	A_{VDD} = 6.5V to 18V	◙	0		A_{VDD}	V
CMRR	Common mode rejection ratio	V_{INP1} = 1.8V to A_{VDD}-1.8V		60	75		dB
PSRR	Power supply rejection ratio	A_{VDD} = 6.5V to 16V, V_{INP1} = 3.25V		60	75		dB
V_{OH}	Output voltage swing HIGH	I_{SOURCE} = 50mA, A_{VDD} = 10V	◙	9			V
		I_{SOURCE} = 1mA, A_{VDD} = 10V	◙	9.9			V
V_{OL}	Output voltage swing LOW	I_{SINK} = 50mA	◙			1	V
		I_{SINK} = 1mA	◙			0.1	V
I_{SC}	Output short circuit current	V_{COM} = 0V, A_{VDD} = 10V	◙		100	170	mA
		V_{COM} = A_{VDD}, A_{VDD} = 10V	◙	-170	-100		mA
		V_{COM} = 0V, A_{VDD} = 16V	◙			200	mA
		V_{COM} = A_{VDD}, A_{VDD} = 16V	◙	-200			mA
g_m	Transconductance	V_{INP1}-V_{INN1} = ±40mV			1000		mS

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

V_{IN} = 2.7V to 4.0V; C_{FLY} = 0.22µF, C_{OUT} = 4.7µF. Unless otherwise specified, all specifications are tested under T_A = 25°C. The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 9. VCORE Charge Pump

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
I_{OUT_MAX}	Maximum output current	3.0V < V_{IN} < 4.0V		300			mA
		2.7V < V_{IN} ≤ 3.0V		150			mA
	Output voltage setpoint accuracy		◙	-3		3	%
f_{OSC}	Switching frequency		◙	2.0	2.4	2.8	MHz
I_{CL}	Maximum output current (over-current protection)	V_{CORE} = 0.6V, V_{IN} = 3.3V		300		600	mA
I_{SC}	Short circuit current (folded back current)	V_{CORE} = 0V, V_{IN} = 3.3V			80		mA
V_{DO}	Charge pump dropout voltage	I_{CORE} = 300mA [Note 8]	◙		200	300	mV
R_{eq}	Equivalent series resistance	V_{IN} = 3.0V, I_{OUT} = 300mA [Note 6]			0.6	1	Ω

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

[Note 6] Guaranteed by design, not 100% production tested.

[Note 8] Minimum input voltage is measured when output voltage is reduced by 2% as compared to the nominal condition under full load. Dropout is calculated as $V_{IN(MIN)}$/2 - V_{CORE}.

V_{IN} = 2.7V to 4.0V; CLKIN = 1.2MHz. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 10. UVLO and Thermal Protection Circuits

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
V_{UVLO}	Undervoltage lockout circuit	V_{IN} rising			2.4		V
V_{UVLO_TH}	Undervoltage hysteresis	V_{IN} = 3.0V to 3.6V			100		mV
T_{SD}	Thermal shutdown	Temperature rising [Note 6]			150		°C
T_{SD_TH}	Thermal shutdown hysteresis	V_{IN} = 3.0V to 4.0V [Note 6]			15		°C

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

[Note 6] Guaranteed by design, not 100% production tested.

V_{IN} = 2.7V to 4.0V. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 11. ON Output

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
V_{MAX}	ON pin maximum voltage (OFF state)		◙	27			V
V_{MIN}	ON pin low voltage	I_{ON} = 1mA	◙		0.5	1	V
$R_{DS(ON)}$	ON-pin drain to source resistance (ON state)					1	kΩ

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

V_{IN} = 2.7V to 4.0V; C_{DLY} = 0.1µF. Unless otherwise specified, all specifications are tested under T_A = 25°C.
The ◙ denotes specifications that apply for T_A = -40°C to +85°C. [Note 4]

Table 12. Reset Output

SYMBOL	PARAMETER	CONDITIONS	◙	MIN	TYP	MAX	UNITS
$R_{DS(ON)}$	RSTOUT ON-resistance	V_{IN}=3.3V			100	150	Ω
V_{DLY}	DLY threshold voltage	V_{DLY} increasing		1.176	1.20	1.224	V
V_{TH_R}	V_{TH} threshold voltage	V_{TH} increasing		1.176	1.20	1.224	V
V_{TH_F}	V_{TH} threshold	V_{TH} decreasing		1.127	1.15	1.173	V
t_{DELAY}	RSTOUT delay time	After V_{TH}>1.2V			100		ms
I_{DLY}	DLY source current	V_{DLY} = 0V			2		mA
R_{DLY}	DLY pin pull down impedance	V_{IN}=V_{DLY}=3.3V, V_{TH}=0V			2		kΩ

[Note 4] Specifications over the -40°C to +85°C operation ambient temperature are guaranteed by design, characterization and statistical correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

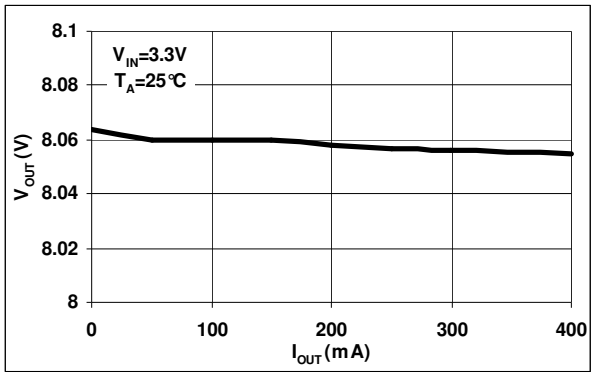

Figure 2. Boost 8V Output Voltage vs. Output Current

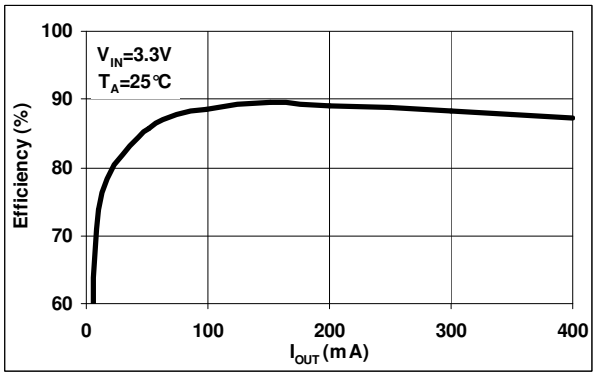

Figure 3. Boost 8V Output Efficiency vs. Output Current

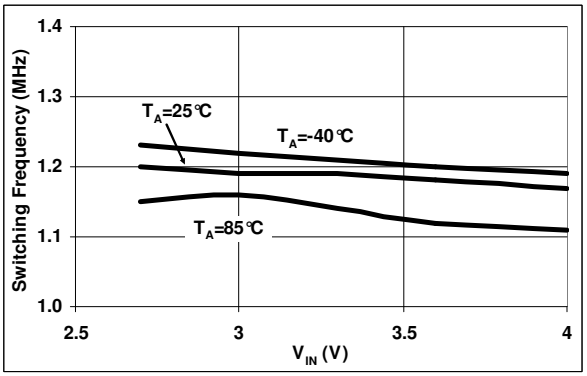

Figure 4. Boost Switching Frequency vs. Input Voltage

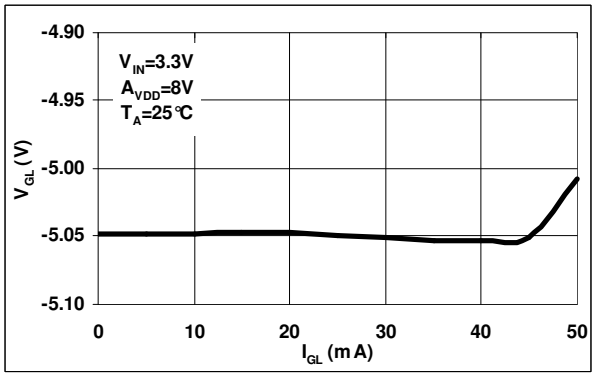

Figure 5. V_{GL} Output Voltage vs. Output Current

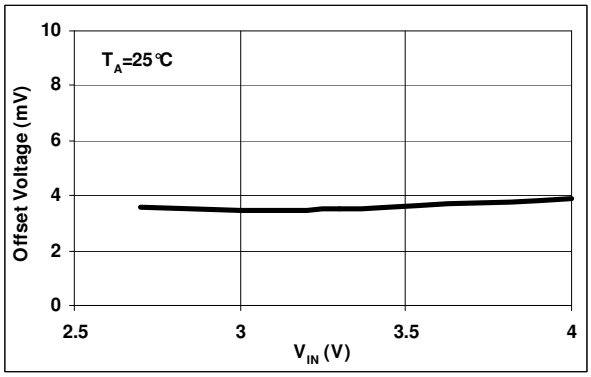

Figure 6. V_{GL} Input Offset Voltage vs. Input Voltage

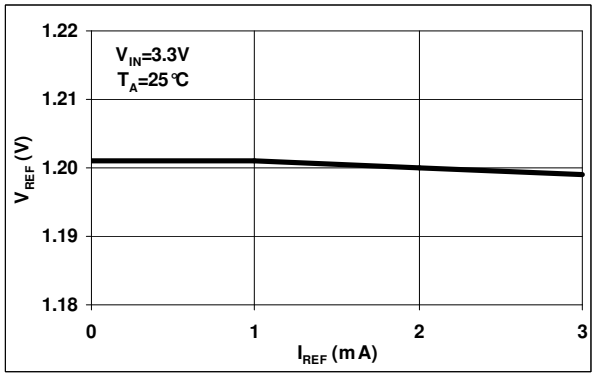

Figure 7. V_{REF} Output Voltage vs. Output Current

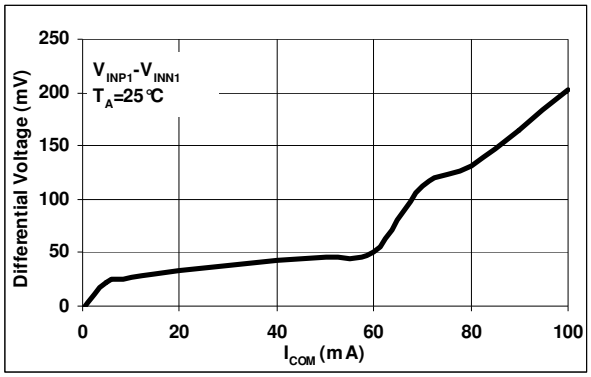

Figure 8. V_{COM} Input Differential Voltage vs. Output Current (Sourcing Current)

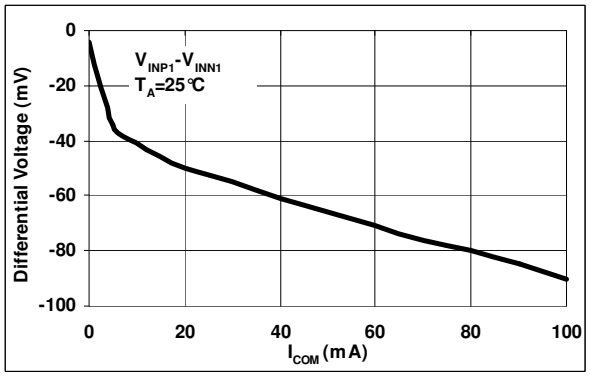

Figure 9. V_{COM} Input Differential Voltage vs. Output Current (Sinking Current)

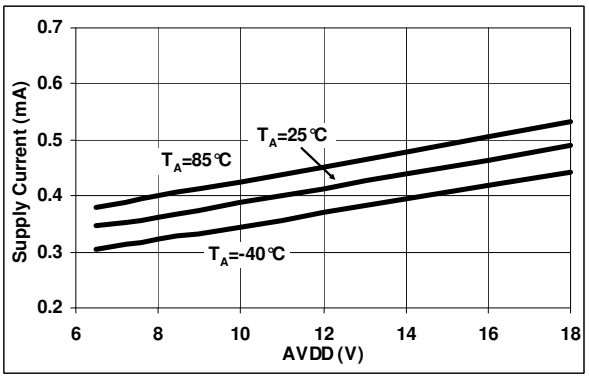

Figure 10. V_{COM} Supply Current vs. AVDD Supply Voltage

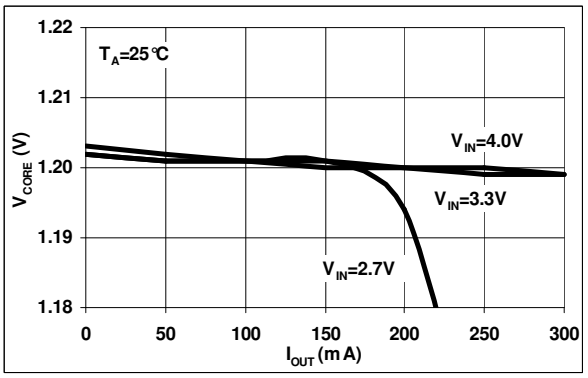

Figure 11. V_{CORE} Output Voltage vs. Output Current

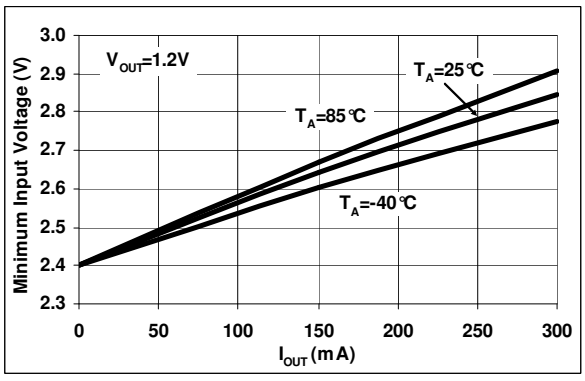

Figure 12. V_{CORE} Minimum Input Voltage vs. Output Current

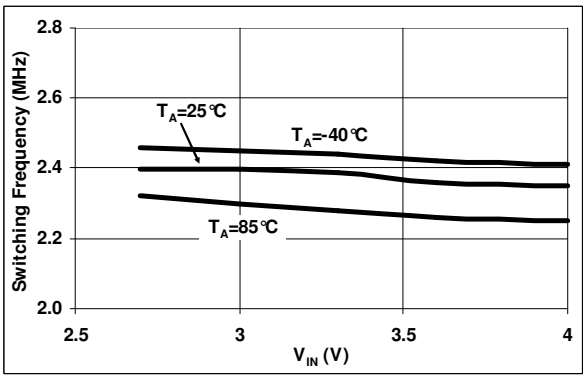

Figure 13. V_{CORE} Switching Frequency vs. Input Voltage

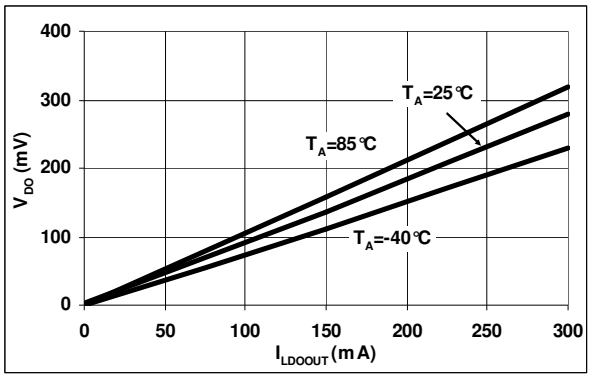

Figure 14. LDO Dropout Voltage vs. Output Current

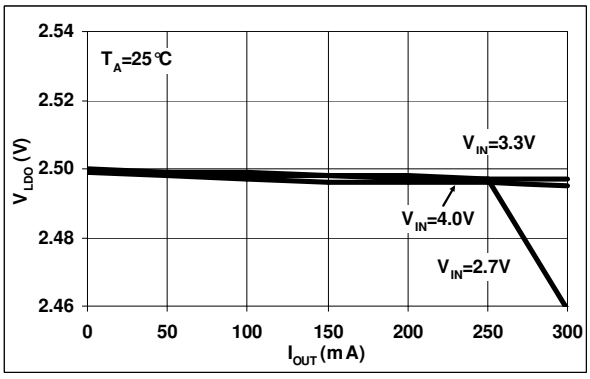

Figure 15. LDO Output Voltage vs. Output Current

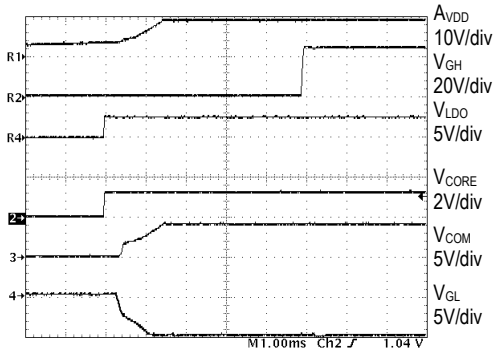

Figure 16. Power Up Sequence
(Typical Application Circuit with VGH set to 3x A_{VDD})

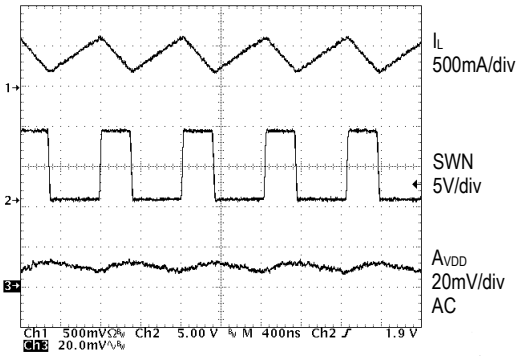

Figure 17. Boost Switching Waveform at I_{OUT} = 100mA

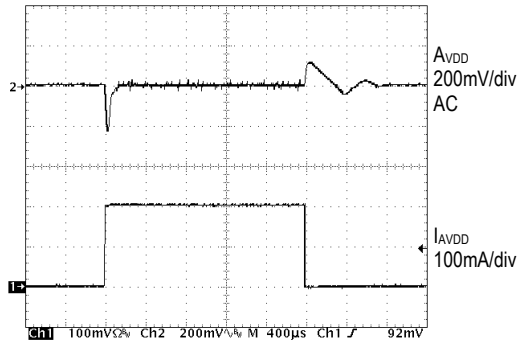

Figure 18. Boost Load Transient Response
for I_{AVDD} = 0 to 200mA

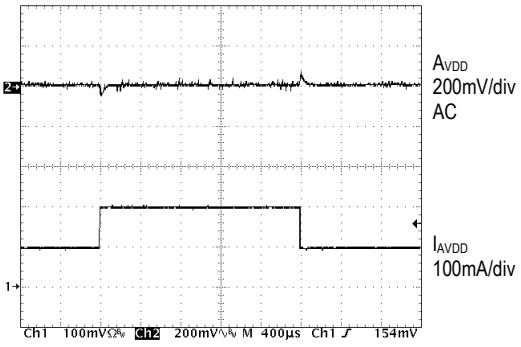

Figure 19. Boost Load Transient Response
for I_{AVDD} = 100mA to 200mA

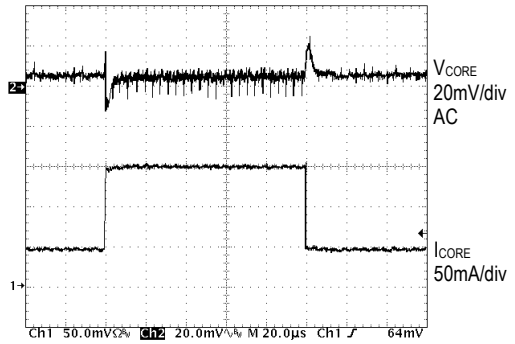

Figure 20. V_{CORE} Load Transient Response for I_{CORE} = 50mA to 150mA

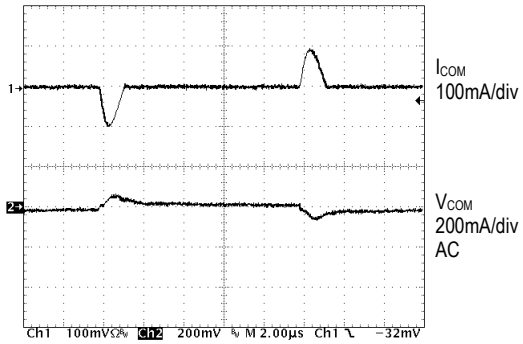

Figure 21. V_{COM} Load Transient Response for I_{COM} = 100mA Capacitive Load

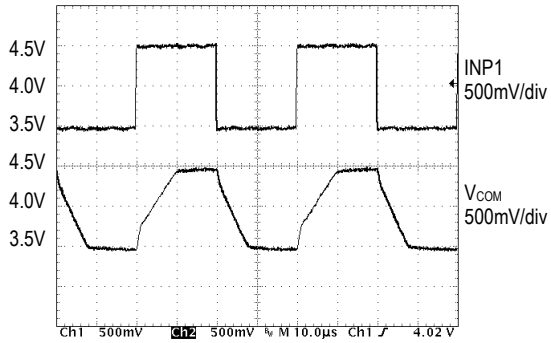

Figure 22. VCOM Large Signal Response

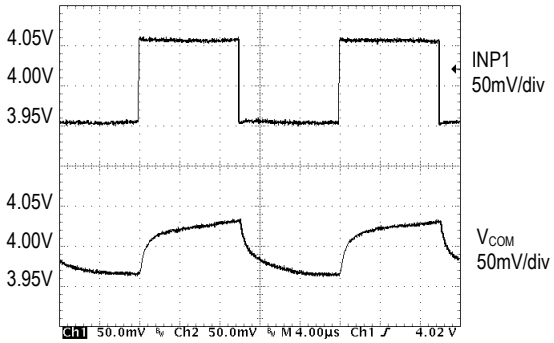

Figure 23. VCOM Small Signal Response

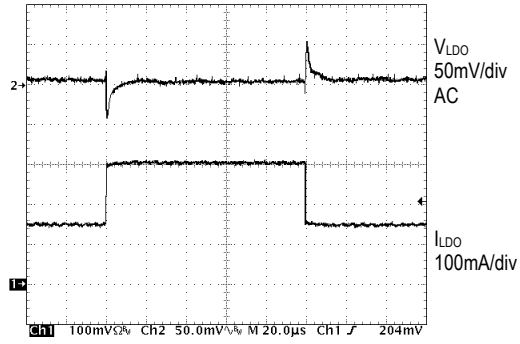

Figure 24. LDO Load Transient Response for I_{LDO} = 150mA to 300mA

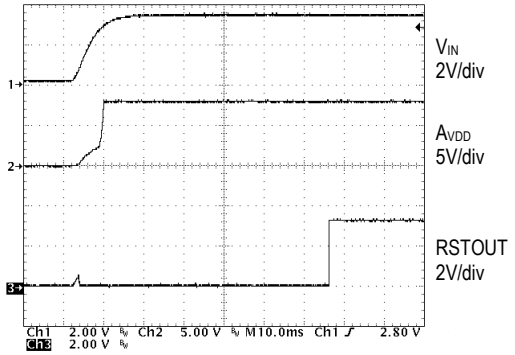

Figure 25. RSTOUT Function Waveforms

PIN CONFIGURATION & DESCRIPTION

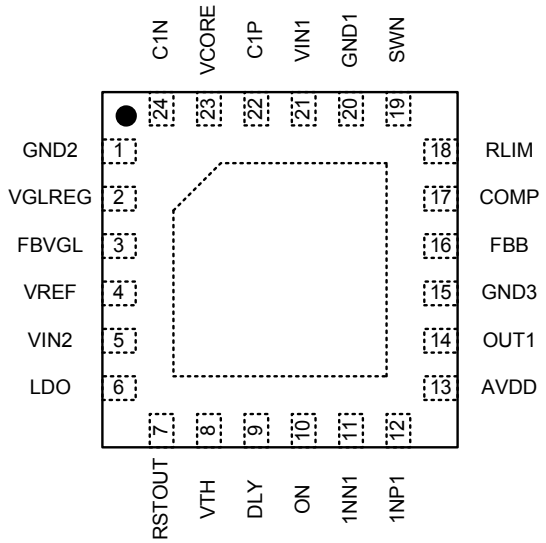

Figure 26. VPA2000 Pin Configuration (Top View)

Table 13. Pin Descriptions

NUMBER	LABEL	I/O	DESCRIPTION
1	GND2		Ground connections for VCORE. Connect this pin to ground.
2	VGLREG	Output	Output of the linear regulator for negative gate driver voltage.
3	FBVGL	Input	Feedback path for the negative regulator. Connect a resistor between this pin and V_{GL} as well as a resistor between this pin and VREF pin. Values of these resistors define output voltage V_{GL}.
4	VREF	Output	Output of the internal reference block.
5	VIN2	Input	Power supply input voltage. Place a decoupling 1µF capacitor next to this pin.
6	LDO	Output	Output of the internal 2.5V LDO supplies the I/O voltage of DP TCON.
7	RSTOUT	Output	Power on reset output. When all voltage outputs are within their appropriate regulation window this output switches High. This is an open drain output. Connect a resistor from this pin to VIN or any voltage source lower than VIN.
8	VTH	Input	Input to the Reset comparator. Place a resistor from V_{IN} to this pin as well as a resistor from this pin to ground.
9	DLY		Place a capacitor from this pin to ground. This pin sets a delay for RSTOUT output switching to High.
10	ON	Output	Driver output for an external P-channel MOSFET or PNP. This signal can be used to delay A_{VDD} or V_{GH} to allow negative output V_{GL} to rise first.
11	INN1	Input	Negative input for the internal VCOM buffer. Connect to OUT1 for unity gain configuration.
12	INP1	Input	Positive input for the internal VCOM buffer. Connect through a resistor divider to A_{VDD}.
13	AVDD	Input	Connect to the output of the boost regulator. This voltage is used to power VCOM buffer.
14	OUT1	Output	Output of the VCOM driver.
15	GND3		Ground connections for the IC.
16	FBB	Input	Feedback pin for the A_{VDD}. Connect this pin to the output through a resistor divider.
17	COMP		Loop compensation for the boost regulator. This pin is an output of an internal transconductance amplifier. Connecting an external RC network from this pin to ground ensures loop stability for the boost regulator.
18	RLIM		Connect this pin to V_{IN} to set the maximum peak current level for the boost switch.

NUMBER	LABEL	I/O	DESCRIPTION
19	SWN		Connection for the drain terminal of the boost power switch.
20	GND1		Ground connections for the boost switch. Route the boost output capacitors ground returns to this pin with the smallest loop area possible. Connect this pin to ground.
21	VIN1	Input	Power supply input voltage. Place a decoupling 4.7µF capacitor next to this pin.
22	C1P		Positive terminal of flying capacitor required by the charge pump.
23	VCORE	Output	Output of the built-in charge pump. This pin supplies 1.2V for the core voltage of DP TCON.
24	C1N		Negative terminal of flying capacitor required by the charge pump.
-	PAD		Thermal pad. Connect this pad to ground. Use thermal vias and large copper area for improved thermal performance.

FUNCTIONAL DIAGRAM

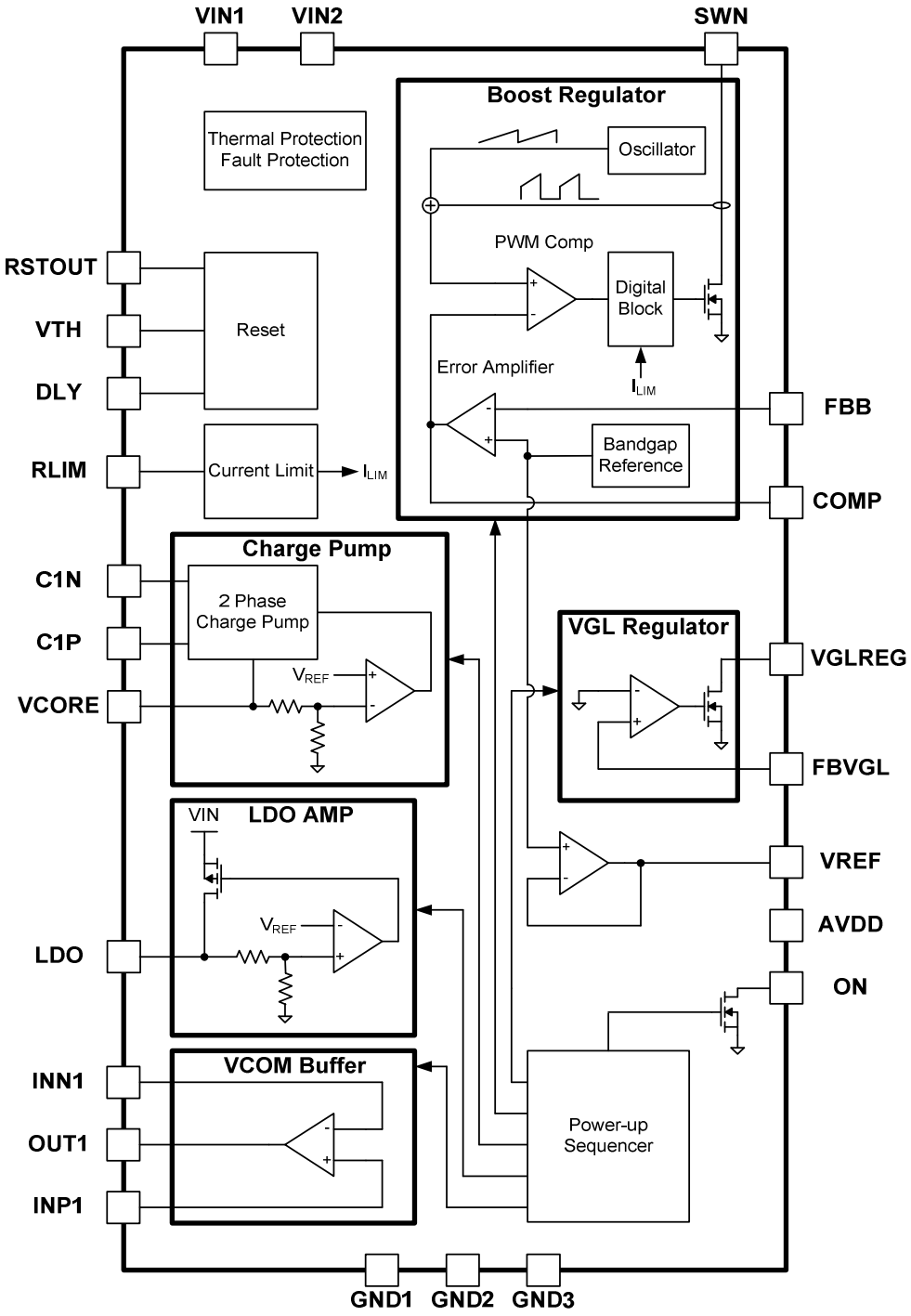

Figure 27. VPA2000 Functional Diagram

THEORY OF OPERATION

Description

The VPA2000 is a complete power solution for TFT-LCD panels and display port timing controllers. It contains a boost regulator, a negative voltage regulator, a VCOM buffer, a 2.5V fixed output LDO, a 1.2V fixed output charge pump, and an external 2x charge pump.

Boost Regulator

The VPA2000 boost regulator is designed to generate the A_{VDD} voltage for the source drivers in the TFT-LCD panel. Its current mode control architecture with fixed 1.2MHz switching frequency provides fast transient response and reduces the number of external components for compensation.

When the internal power N-channel MOSFET (connected to SWN pin) is turned on, current starts to flow from V_{IN} to ground, and the inductor current starts to ramp up and stores the energy.

The ramping current is sensed and is added with the slope compensation ramp. When the ramp current reaches its control level, the MOSFET is turned off, and the energy stored in the inductor will feed to the output (A_{VDD}). The MOSFET on-off ratio (duty cycle) is varied by the input to output ratio and can be calculated with the following equation during continuous conduction mode (CCM):

$$D = 1 - \frac{V_{IN}}{A_{VDD}} \quad [1]$$

The output voltage A_{VDD} is set by an external resistor divider R7 and R8. A_{VDD} can be calculated with equation:

$$A_{VDD} = 1.2V \times \left(1 + \frac{R7}{R8}\right) \quad [2]$$

The boost regulator has a built-in over-voltage protection (OVP) to prevent the output voltage from exceeding 20V. Always connect the boost output (A_{VDD}) to AVDD pin to activate the OVP function and enable the VCOM buffer.

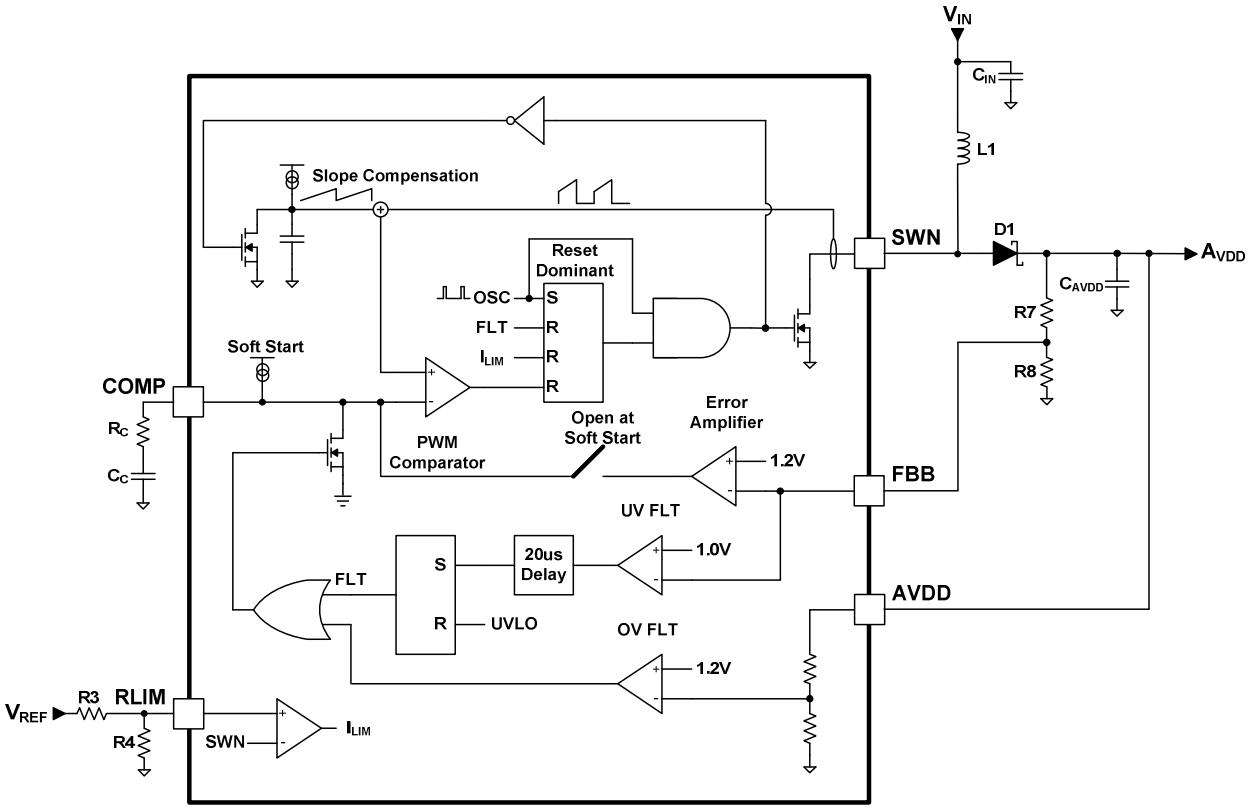

Figure 28. VPA2000 Boost Regulator Block Diagram

If over-voltage is detected during normal operation, the power N-channel MOSFET will turn off, and it will turn on again when output voltage drops below the comparator hysteretic level. On the other hand, if over-voltage is detected during power up, the boost regulator will shut down.

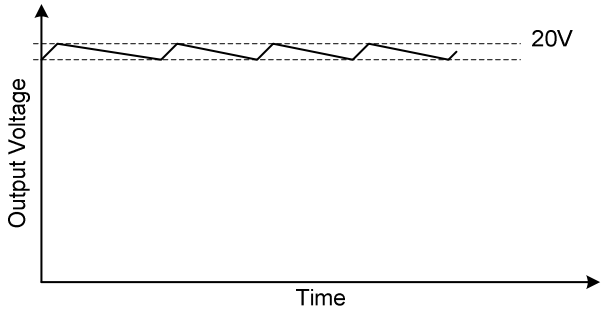

Figure 29. Over-voltage Protection

Besides over-voltage protection, the boost regulator has an over-current protection to prevent excess current from flowing into the power N-channel MOSFET. When the inductor peak current is beyond the current limit level, the N-channel MOSFET will shut down. Thus, during over-current, the output voltage will be lower than the programmed output voltage. Connecting the RLIM pin to V_{IN} will set the current limit level to its default value 2.35A. The current limit level can be adjusted lower by placing a resistor divider from V_{REF} pin to ground, see Figure 28 for details. Therefore, I_{LIM} is calculated as:

$$I_{LIM} = 2.35 \times V_{REF} \times \frac{R4}{R3 + R4} (A) \quad [3]$$

where V_{REF} = 1.2V. For example, to set the current limit level to 1A, choose R4 = 4.99kΩ, so R3 will be 9.09kΩ.

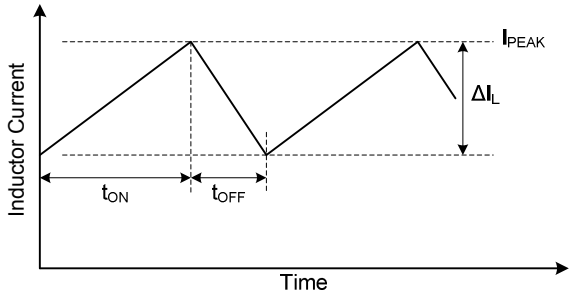

Figure 30. Inductor Current Waveforms

For stability, connect a 4.99kΩ resistor, R_C, in series with a 6.8nF capacitor, C_C, from COMP pin to ground.

The average inductor current is proportional to the boost regulator output current. As the output current decreases, the inductor current will eventually reach zero, and if the output current is further decreased, the boost regulator will operate in discontinuous conduction mode (DCM). The output current level that results in DCM is approximately:

$$I_{OUT} < \frac{1}{2} \times \left(\frac{V_{IN} \times D \times (1-D)}{f_{SW} \times L} \right) \quad [4]$$

where f_{SW} is the switching frequency of the boost regulator.

When the output current level is reduced even further, the boost converter will skip pulses randomly in order to maintain the output regulation. The pulse skipping feature is inherent to the boost regulator, and it improves the light-load efficiency due to the reduction of switching losses.

Negative Linear Regulator

The negative linear regulator provides the negative output voltage (VGL) with a 2-phase operation. During the first phase, when V_{SWN} is equal to A_{VDD}, the flying capacitors C_{GLFLY} and C_{VGLREG} are charged up. During the second phase, when V_{SWN} is equal to 0V, it level shifts C_{GLFLY}, and C_{GLFLY} and C_{GL} are now connected in parallel. Thus, C_{GL} charges up to a negative voltage.

The voltage across C_{GLFLY} and C_{VGLREG} is controlled by the N-channel MOSFET, and V_{GL} is set by the external resistor divider R9 and R10 with the following equation:

$$V_{GL} = -1.2V \times \frac{R9}{R10} \quad [5]$$

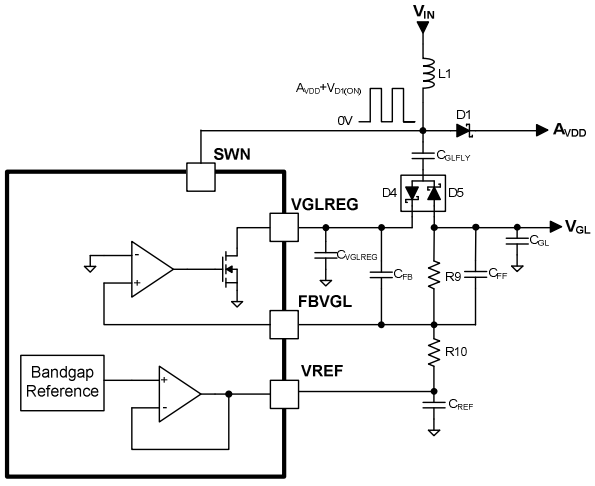

Figure 31. Negative Linear Regulator Block Diagram

VCOM Buffer

The VPA2000 VCOM buffer is an operational transconductance amplifier. Since the stability of the amplifier is improved with larger capacitive loads, it becomes an ideal power supply for the backplane of TFT-LCD panels. Connect INN1 pin to OUT1 pin to configure the VCOM buffer as a unity gain amplifier. To adjust the output voltage of the VCOM buffer, connect a resistor divider on pin INP1 from A_{VDD} to GND, as shown in Figure 39. Therefore,

$$V_{COM} = A_{VDD} \times \frac{R6}{R5 + R6} \quad [6]$$

Low Dropout Linear Regulator (LDO)

The VPA2000 LDO provides a 2.5V fixed output with maximum 300mA current. It is designed to supply the I/O voltage for display port timing controllers. To ensure stability, a minimum 1.0µF output capacitor with ESR < 0.5Ω is required for the LDO. Ceramic capacitors are the best choice for their low ESR range on the order of mΩ. Higher output capacitance will help to reduce the output ripple.

The LDO has a short-circuit current protection which limits the current to be 600mA during a short-circuit condition.

VCORE Charge Pump

The VCORE output is a 0.5x regulated charge pump with fixed 1.2V output voltage, designed as a low cost replacement for buck regulators. The charge pump operates at constant frequency with 50% duty cycle. During the first phase, flying capacitor C_{FLY} is placed in series with output capacitor $C_{OUT.}$ The input current charges both the flying capacitor and the output capacitor, and supplies the output load. During the second phase, the output capacitor and the flying capacitor are placed in parallel, and both capacitors are discharged to supply the output load. Since V_{IN} conducts to V_{OUT} with 50% duty cycle, the average input current is equal to 50% of the output current. As a result, it dissipates approximately 80% less power than a standard LDO.

To regulate the output voltage, the error amplifier controls the input P-channel MOSFET gate driver voltage, which controls the amount of current flowing into the flying capacitor during the charging phase. Thus, the flying capacitor's differential voltage is charged up to be equal to the output voltage.

The value of C_{FLY} should be 0.22µF. To ensure stability over its operating current range, a 4.7µF or larger output capacitor is required. Higher output capacitance will help to reduce the output ripple and will have better transient response performance.

The charge pump has over-current protection which ensures the maximum output current is limited to 600mA during over current and 80mA during a short-circuit condition.

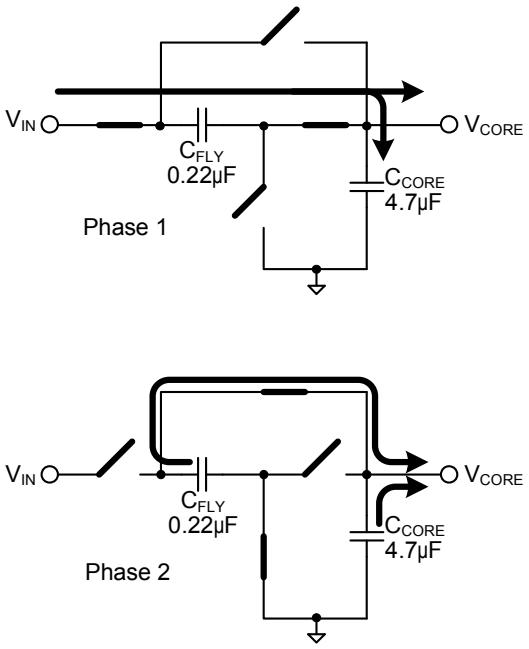

Figure 32. 0.5x Charge Pump 2 Phase Operation

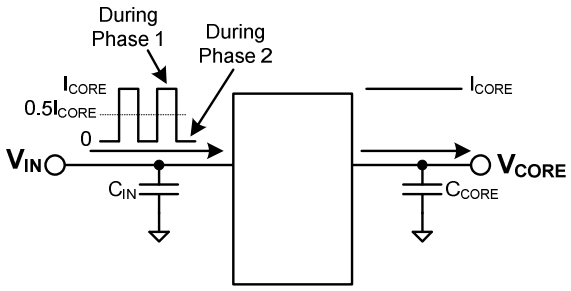

Figure 33. Input Current flowing Diagram

External 2x Charge Pump

A low cost external 2x charge pump is used to supply the positive gate driver voltage (VGH). The output voltage of V_{GH} is ($2xA_{VDD} – V_{D3(ON)}$) with a 2-phase operation. During the first phase when V_{SWN} is equal to 0V, flying capacitor C_{GHFLY} is charged up to ($A_{VDD} – V_{D2(ON)}$) while C_{GH1} is charged up to ($A_{VDD} – V_{D2(ON)} – V_{D3(ON)}$) . During the second phase, when V_{SWN} is equal to A_{VDD}, it level shifts V_{GHFLY} by ($A_{VDD} + V_{D1(ON)}$). The level-shifted voltage then charges up C_{GH1} to ($2xA_{VDD} – V_{D3(ON)}$) assuming $V_{D1(ON)} = V_{D2(ON)}$.

V_{GH} is powered up simultaneously with A_{VDD}. If V_{GH} is needed to startup after A_{VDD}, a pre-biased PNP transistor Q1 and an output capacitor C_{GH2} should be added as shown in Figure 34.

The ON pin is an N-channel MOSFET open drain output, it switches to LOW 3.4ms after A_{VDD} reaches regulation and V_{GL} is enabled. Otherwise, it is floating. A detailed power-up sequencing waveform is shown in Figure 37.

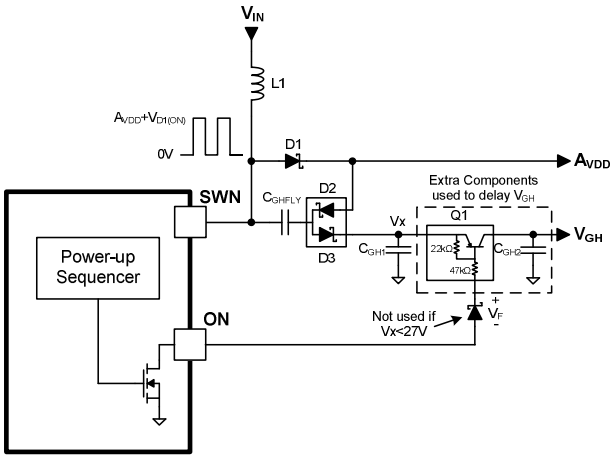

Figure 34. External 2x Charge Pump Block Diagram

The ON pin operating voltage is 27V. If the voltage applied to the Vx node is greater than 27V, an extra zener diode should be placed in series with the ON pin to prevent damage to the ON pin. For example, if 36V is applied to Vx, a 10V zener diode should be used.

Reset Output

The RSTOUT pin is an open drain output. Connect a resistor from this pin to V_{LDO} for a typical application or any voltage source lower than V_{IN}. When the voltage at the V_{TH} pin is lower than 1.2V, RSTOUT stays Low. When the voltage at V_{TH} pin is higher than 1.2V, the DLY pin starts to source 2µA into the external capacitor, C_{DLY}. As soon as the voltage at the V_{DLY} pin is higher than 1.2V, the RSTOUT will stay High.

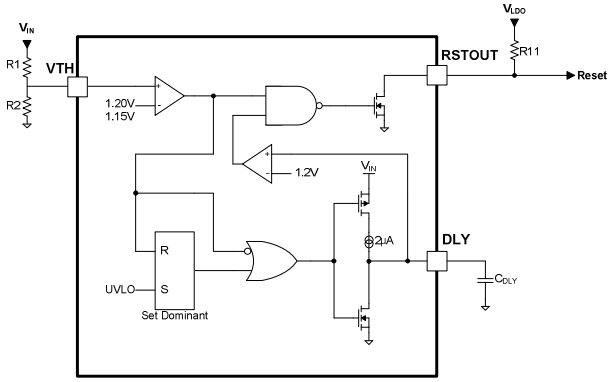

Figure 35. Reset Output Block Diagram

The charging time to charge up CDLY to 1.2V is calculated by this equation:

$$t_{DLY} = C_{DLY} \times \frac{1.2V}{2\mu A} \quad [7]$$

For example, if C_{DLY} is 0.1µF, the delay time T_D will be 60ms.

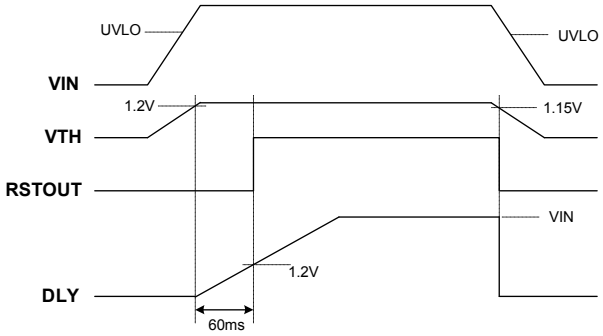

Figure 36. Reset Output Timing Diagram

Power Up Sequence

All of the output voltages will be enabled after the input voltage exceeds the UVLO level. A_{VDD} and V_{GL} will start to rise 300µs after they are enabled. The ON pin is an open-drain output, and it will pull low after 3.4ms, and can be used to delay the V_{GH} output. Refer to Figure 37 for an illustration.

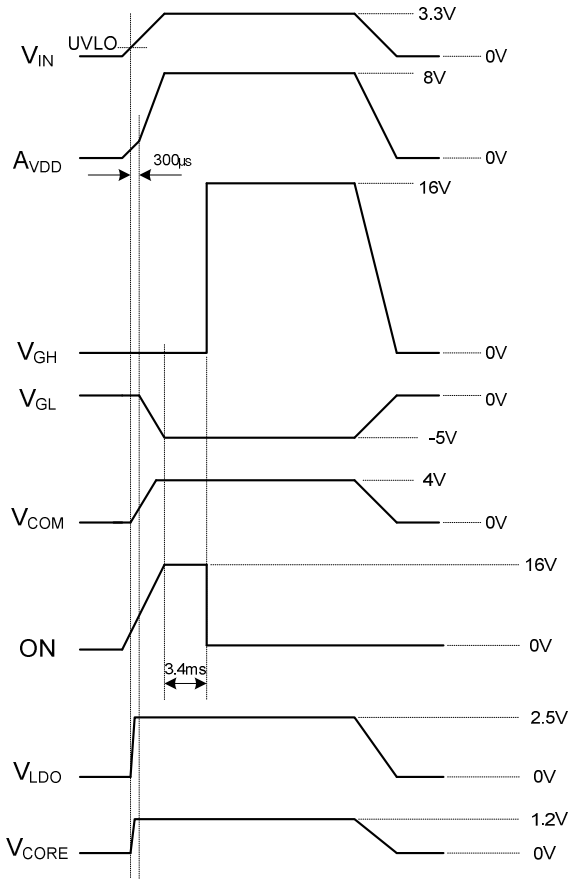

Figure 37. Power Up Sequence

Over-temperature Protection

When the junction temperature of the VPA2000 reaches 150°C, the over-temperature protection will activate and shut down the device. It will resume to its previous operating condition when the junction temperature falls below 135°C.

DESIGN EXAMPLE

To design a boost converter with V_{IN}=3.3V, V_{OUT}=8V, I_{OUT}=400mA, and assume the efficiency is 85%. Refer to Figure 39, choose R8=4.99kΩ. Use equation [2] to calculate R7. Thus, R7=28kΩ.

Inductor Selection

The value of the inductor will affect the boost converter efficiency and output voltage ripple. A 4.7µH inductor works for most applications.

The inductor current ripple should be around 40% of the inductor current for a good compromise between the size of inductor, cost, and power loss. Thus, the minimum inductor value is calculated with the following equation:

$$L_{MIN} = 0.85 \times \left(\frac{V_{IN}}{A_{VDD}}\right)^2 \times \left(\frac{A_{VDD} - V_{IN}}{f_{SW} \times I_{OUT}}\right) \times \left(\frac{1}{0.4}\right) \quad [8]$$

where f_{SW} is the boost converter switching frequency which is 1.2MHz. Therefore, L_{MIN}=4.25µH, so choose a 4.7µH inductor.

Vendors usually provide inductor DC current value, I_{DC} and inductor saturated current value, I_{SAT}. Choose the inductor that offers both ratings at higher than the inductor peak current level. Use the following equation to calculate the inductor peak current:

$$I_P = \left(\frac{A_{VDD} \times I_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{0.85}\right) \times \left(1 + \frac{0.4}{2}\right) \quad [9]$$

The calculated peak current level is 1.37A. The boost converter current limit level should be higher than the inductor peak current level. Connect RLIM pin to V_{IN} to set the current limit level to 2.35A (default value).

Diode Selection

A Schokkty diode should be chosen to reduce the power loss of the diode. The diode current rating should be higher than the output current level, and the reverse breakdown voltage should be higher than the output voltage.

Input Capacitor Selection

A 10µF or greater value input capacitor should be used. Place a 4.7µF and 1µF capacitor close to the VIN1 pin and VIN2 pin, respectively, to bypass the input voltage. Ceramic capacitors should be chosen for their low ESR, which greatly reduces the input voltage ripple.

Output Capacitor Selection

The value of output capacitor helps to reduce output voltage ripple as well as to stabilize the boost converter. A total of 20µF output capacitance is suitable for most applications.

The output voltage ripple is affected by the ESR of the output capacitor (ΔV_{ESR}) as well as the variations in the charge stored in the output capacitors (ΔV_C). However, since ceramic capacitor ESR is fairly low, the output voltage ripple is mainly affected by ΔV_C, and the estimated output voltage ripple is:

$$\Delta V_C = \left(1 - \frac{V_{IN}}{A_{VDD}}\right) \times \left(\frac{I_{OUT}}{f_{SW} \times C}\right) \quad [10]$$

Table 14. VPA2000 Components Selection

	CIRCUIT 1	CIRCUIT 2	CIRCUIT 3
V_{IN}	3.3V	3.3V	3.3V
A_{VDD}	9.7V	12V	16V
I_{OUT}	400mA	200mA	200mA
L	4.7µH	6.8µH	5.6µH
C_{AVDD}	20µF	20µF	20µF

LAYOUT GUIDELINES

To optimize the device performance, follow these layout guidelines:

1. Place the inductor and diode as close as possible to Pin19 (SWN).
2. Pin20 (GND1) is the power ground of the boost converter. Return the boost output capacitors' ground connections to this pin while minimizing the loop area created from pin 19 through the diode D1, through the output capacitors, and back to pin 20.
3. Separate all grounds on the top layer and connect all ground connections through vias to the ground plane.
4. Locate all feedback resistor dividers close to the feedback pins. Keep the traces from feedback pins to the resistor dividers as short as possible.
5. Keep the traces from SWN to C_{GHFLY} to D2 and D3 short.
6. Keep the traces from SWN to C_{GLFLY} to D4 and D5 short.
7. Place output capacitors C_{OUT1}, C_{LDO}, and C_{VCORE} close to their respective output pins.
8. Keep all input decoupling capacitors close to the input pins and return their ground connections directly to the appropriate ground pin.

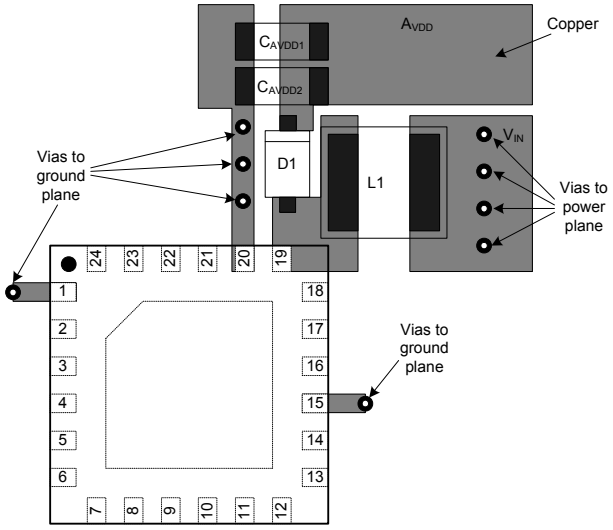

Figure 38. Optimized Layout for Boost Converter

APPLICATION

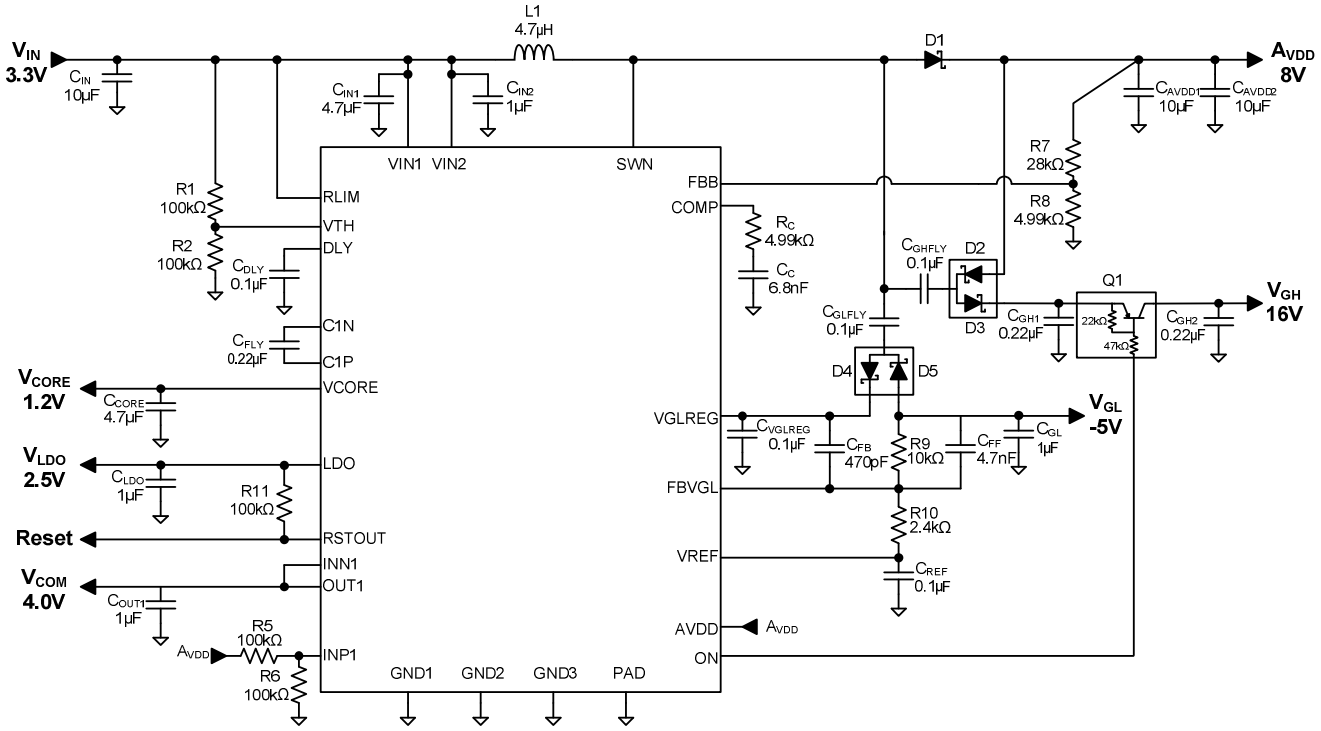

Figure 39. VPA2000 Typical Application Circuit

PACKAGE OUTLINE DRAWING

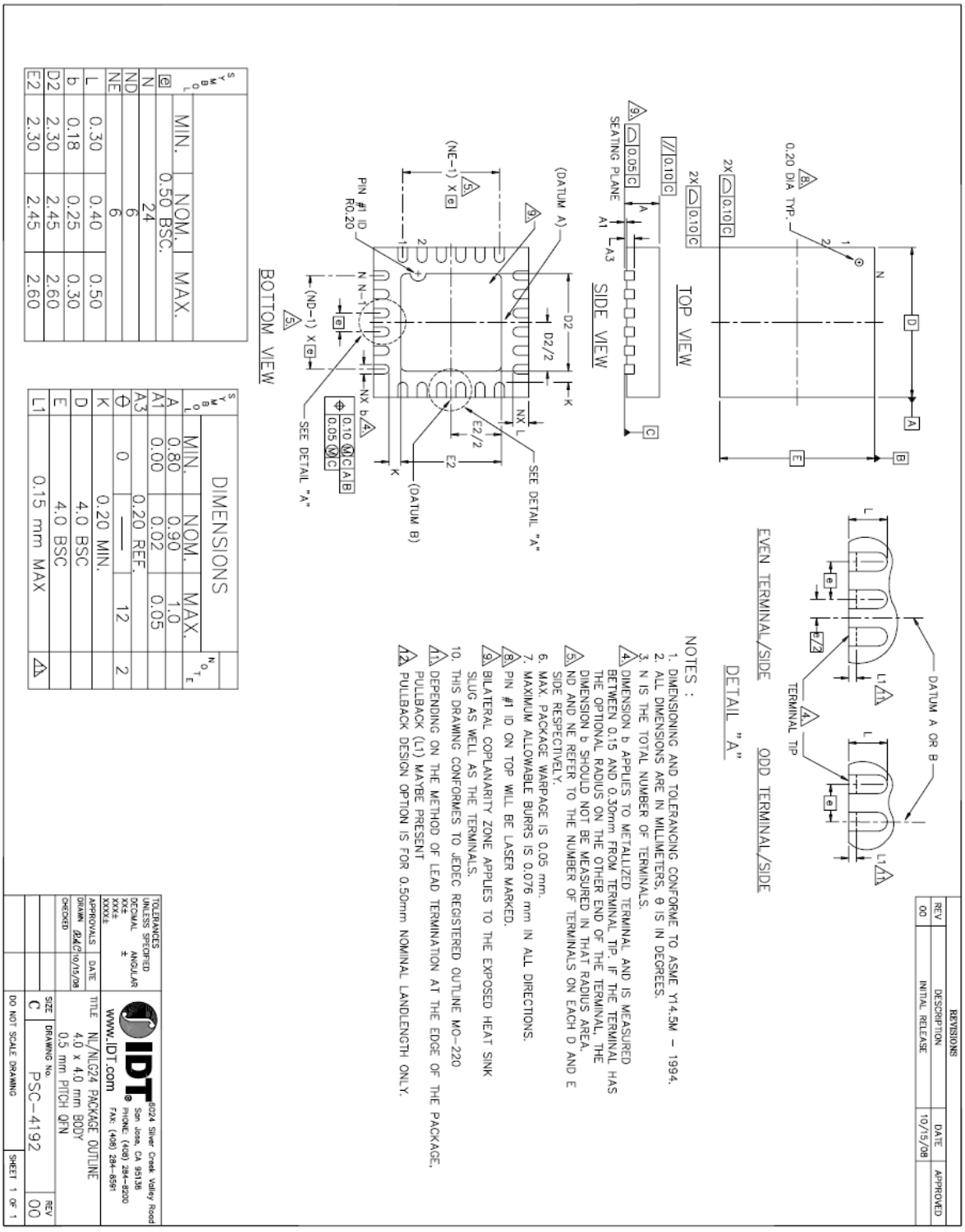

Figure 40. Package Outline Drawing

ORDERING GUIDE

Table 15. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
VPA2000NLGI	VPA2000NLGI	24-QFN 4x4mm	-40°C to +85°C	Tape or Canister	25
VPA2000NLGI8	VPA2000NLGI	24-QFN 4x4mm	-40°C to +85°C	Tape and Reel	2,500

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