DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
V850E/PHC3

V850E/PHC3
32-Bit Single-Chip Microcontroller

DESCRIPTION

With its high performance V850E CPU core and its compact feature set the V850E/PHC3 is especially suited for embedded control applications.
The V850E/PHC3 devices provide an excellent combination of general purpose peripheral functions like serial communication interfaces, timers/counters, measurement and control functions, with dedicated motor control timers and full CAN network support.
Thus equipped, the V850E/PHC3 product is ideally suited for automotive control applications, such as electric power steering (EPS). It is also an excellent choice for other embedded applications where a combination of sophisticated peripheral functions and CAN network support is required.

FEATURE

- 32-bit RISC CPU incl. single-precision FPU
- Internal flash memory: 480 KB
- Internal RAM: 32 KB
- Data Flash: 32 KB
- Operating Clocks
  CPU Frequency: 80 MHz
  MainOsc: operates on 16MHz crystal
  2 x PLL: ratio 5, 2
- Timers
  10 ch 16-bit general purpose timer/counter
  2 ch 16-bit timer for Motor Control
  2 ch 16-bit general purpose timer/counter with encoder function
- A/D Converter: 2 x 10 channels
  10 bit resolution
- CAN Interface: 2 channel (AFCAN)
- Serial Interfaces: 6 channels
  - synchronous: 2 channels (CSIB)
  - synchronous with FIFO: 2 channels (CSIE)
  - asynchronous: 2 channels (UARTC)
- DMA: 10 channels
- Auxiliary Frequency Output
- I/O lines: 76 + 5 input only
- Clock Monitor
- Power Save Mode: HALT
- On Chip Debug: N-Wire
- Power supply:
  3.3V +/- 0.3V and 1.5V +/- 10%
- Temperature range: -40°C to +125°C
- Package: 144 pin LQFP

ORDERING INFORMATION

Product Name	Product Family	Package	Flash	Data Flash	RAM
μPD70F3485GJ(A2)-GAE	V850E/PHC3	144 pin LQFP	480 KB	32 KB	32 KB

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Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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1. Electrical Target Specification

1.1 Absolute Maximum Ratings

T_a = 25°C
V_{SS15} = CV_{SS}= V_{SS30} = $AV_{SS0,1}$ = 0V

Table 1-1: Absolute Maximum Ratings

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD15}			-0.5 to +2.0	V
	CV_{DD}			-0.5 to +2.0	V
	V_{DD30}			-0.5 to +4.6	V
	AV_{DD}			-0.5 to +4.6	V
Input voltage	V_I	The pin X1 is excluded.		-0.5 to V_{DD30}+0.3 [a]	V
Analog input voltage	V_{IN}	ANI00 to ANI09 ANI10 to ANI19		-0.3 to AV_{DD}+0.3 [a]	V
A/D Converter	$AV_{REF0,1}$			-0.3 to AV_{DD}+0.3 [a]	V
High level output current	I_{OH}	For 1 pin	1 pin	-4.0	mA
		Total of all pins [b]	Total	-75	mA
Low level output current	I_{OL}	For 1 pin	1 pin	4.0	mA
		Total of all pins [b]	Total	75	mA
Operating ambient temperature	T_a	Normal operating mode (Package) [c]		-40 to +125	°C
		Flash programming mode, when flash memory is written. (Package) [c]		-40 to +125	°C
Storage temperature	T_{stg}	In tray.		-65 to +125	°C
		Off tray, mounted but not powered.		-65 to + 150	°C

a. Please do not exceed absolute maximum rating (max. +4.6V) of each power supply voltage.
b. Total sum of all input and output currents of all pins. Please observe addtionally the Table 1-7 on page 11, footnotes b. and c.
c. Measured on JEDEC 4 layer PCB.

Cautions: 1. Do not directly connect output (or I/O) pins of IC products to each other, or to V_{DD}, V_{SS}, and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

1.2 Pin Capacitance

T_a = 25°C
$V_{DD15} = CV_{DD} = V_{DD30} = AV_{DD} = V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS0,1}$ = 0V

Table 1-2: Pin Capacitance

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc=1MHz			15	pF
Input/output capacitance	C_{IO}	All pins are at 0V excluding the pin that is measured.			15	pF
Output capacitance	C_O				15	pF

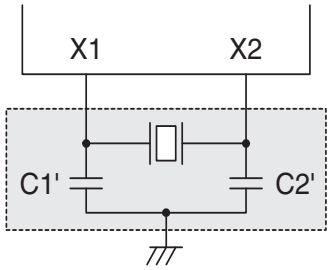
1.3 Operation Conditions

Table 1-3: Operating Conditions

Internal system clock frequency	Operating Temperature		Power Supply Voltage
80MHz	T_a = -40 to +125°C	Normal operating mode	$V_{DD15} = CV_{DD}$ = 1.5V±0.15V $V_{DD30} = AV_{DD}$ = 3.3V±0.3V

1.4 Oscillator Characteristics

Figure 1-1: Oscillator Recommendations



Remark: Values of capacitors C1' and C2' depend on used crystal and must be specified in cooperation with the crystal manufacturer.

Cautions:
1. **External clock input is prohibited.**
2. **Wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.**
   - **Place the oscillation circuit as close as possible to X1 and X2 pins.**
   - **Keep the wiring length as short as possible.**
   - **Do not cross the wiring with the other signal lines.**
   - **Do not route the wiring near a signal line through which a high fluctuating current flows.**
   - **Always make the ground point of the oscillator capacitor the same potential as CV_{SS15}.**
   - **Do not ground the capacitor to a ground pattern through which a high current flows.**
   - **Do not fetch signals from the oscillator.**

Table 1-4: Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	fosc			16		MHz
Oscillation stabilization time	t_{OST}	The oscillation stabilization time depends on the crystal and circuit and must be specified in cooperation with the crystal manufacturer. Ensure that all conditions and tolerances of all components are considered for determination of oscillation stabilization time: Resistance value Capacity value Voltage Temperature Manufacturing range	n/a	n/a	n/a	
PLL lockup time	PSTC	Internal digital counter, counting with fosc (fx=fosc) frequency.		2^{14}/fx		s

1.5 DC Characteristics

1.5.1 Input/Output Level

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V

Table 1-5: Input/Output Level

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	DDI, DMS, DCK	$0.7 \cdot V_{DD30}$		$V_{DD30}+0.3$	V
		P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11	$0.7 \cdot V_{DD30}$		$V_{DD30}+0.3$	V
		$\overline{DRST}$	$0.75 \cdot V_{DD30}$		$V_{DD30}+0.3$	V
		MODE0, MODE1, $\overline{RESET}$	$0.8 \cdot V_{DD30}$		$V_{DD30}+0.3$	V
Input voltage, low	V_{IL}	DDI, DMS, DCK	-0.5		$0.3 \cdot V_{DD30}$	V
		P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11,	-0.5		$0.3 \cdot V_{DD30}$	V
		$\overline{DRST}$	-0.5		$0.3 \cdot V_{DD30}$	V
		MODE0, MODE1, $\overline{RESET}$	-0.5		$0.2 \cdot V_{DD30}$	V
Output voltage, high	V_{OH}	I_{OH}=-2.5 mA [a]	V_{DD30}-1.0			V
		I_{OH}=-0.1 mA	V_{DD30}-0.4			V
Output voltage, low	V_{OL}	I_{OL}=2.5mA [a]			0.8	V
		I_{OL}=0.1mA			0.4	V
Build in pull down resistor	R_L	$\overline{DRST}$ pin only	10	50	120	KΩ

a. Max ± 2.5 mA x 12 of output current simultaneously. Only the output port pins have to be considered.

1.5.2 Pin Leakage Current

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V

Table 1-6: Pin Leakage Current

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH}	$V_I = V_{DD30}$	All pins except ANI00 to ANI09, ANI10 to ANI19			10.0	µA
		$V_I = AV_{DD}$ ANI00 to ANI09, ANI10 to ANI19	ANI00 to ANI09, ANI10 to ANI19 -40°C < Ta ≤ 90°C			1.0	µA
			ANI00 to ANI09, ANI10 to ANI19 +90°C < Ta ≤ 95°C			1.2	µA
			ANI00 to ANI09, ANI10 to ANI19 +95°C < Ta ≤ 125°C			3.0	µA
Input leakage current, low	I_{LIL}	V_I = 0 V	All pins except ANI00 to ANI09, ANI10 to ANI19			-10.0	µA
		V_I = 0 V	ANI00 to ANI09, ANI10 to ANI19			-1.0	µA
Output leakage current, high	I_{LOH}	$V_O = V_{DD30}$	All pins			10.0	µA
Output leakage current, low	I_{LOL}	V_O = 0 V	All pins			-10.0	µA

1.5.3 Operation and HALT Mode Supply Current

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V

Table 1-7: Power Supply Current

Parameter	Conditions		Symbol	TYP.[a]	MAX.	Unit
Supply current	Normal Operation mode	V_{DD15}, CV_{DD} f_{CPU} = 80MHz	I_{DD15}	130	245	mA
		V_{DD30}[b, c]	I_{DD30}		21	mA
	Flash programming mode	V_{DD15}, CV_{DD} f_{CPU} = 80MHz	I_{DDF15}	140	265	mA
		V_{DD30}[b, c]	I_{DDF30}		46	mA
	Halt mode	V_{DD15}, CV_{DD} f_{CPU} = 80MHz	I_{DDH15}	122	227	mA

a. The typical value is a reference value at T_a = 25 °C, V_{DD15} = 1.5 V and V_{DD30} = 3.3 V

b. No external loads considered (C_L = 0 pF). External loads cause additional pin currents. Pin current for each pin can be calculated according to following formular:

I_{pin} [mA] = 0.0057[V] × C_L[pF] × f [MHz]

$I_{DD30\_total} = \Sigma (I_{pin}) + I_{DD30}$

Where C_L is the onboard load capacitance and f is the average pin toggle frequency. Load-dependent pin currents must be summed up and added to I_{DD30}. The maximum value for I_{DD30_total} must not exceed 75mA.

Example:
Only the pin A, B and C may operate in output mode, with the following conditions.
pin A: 8 MHz toogle frequency, on board load capacity C_{LA} = 30 pF
pin B: 2 MHz toogle frequency, on board load capacity C_{LB} = 40 pF
pin C: 1 MHz toogle frequency, on board load capacity C_{LC} = 50 pF

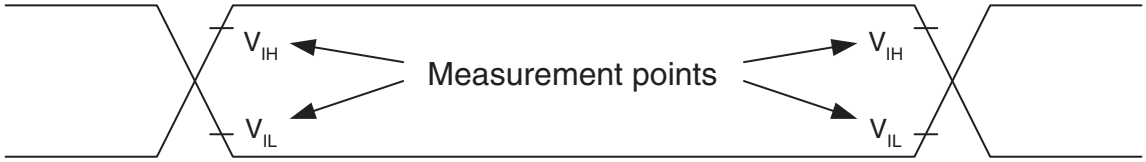
I_{DD30_total}, the V_{DD30} supply current (in normal operation mode), is then calculated as follows:

$I_{DD30\_total} = I_{pin\_A} + I_{pin\_B} + I_{pin\_C} + I_{DD3}$
= (0.0057 × 30 × 8) mA + (0.0057 × 40 ×2) mA+ (0.0057 × 50 × 1) mA + 21 mA
= 23.109 mA

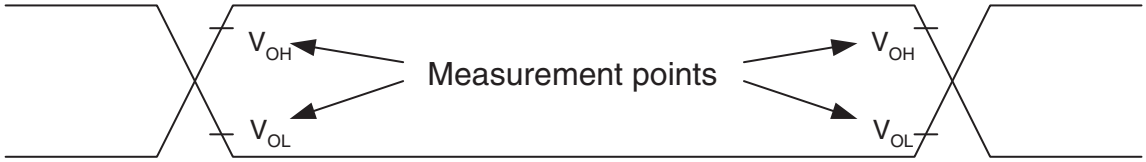
c. Stationary DC load currents of the port pins (I_{OH}/I_{OL}) are not included (e.g. current which flows through external pull-down / pull-up resistors). Ensure that the sum of V_{DD30} supply current from above calculation formula and stationary DC load current of ports (I_{OH}/I_{OL}) will be less than 75 mA. (refer to **1.1 Absolute Maximum Ratings**)

1.6 AC Characteristics

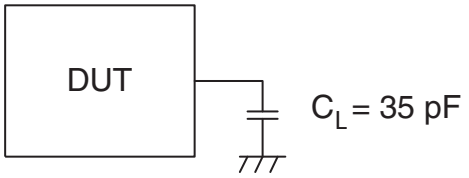
AC Test Input Measurement Points,



AC Test Output Measurement Points



Load Conditions



Caution: If the load capacitance exceeds 35 pF due to the circuit configuration, bring the load capacitance of the device to 35 pF or less by inserting a buffer or by some other means.

1.6.1 Power Supply Turning On / Interception Timing

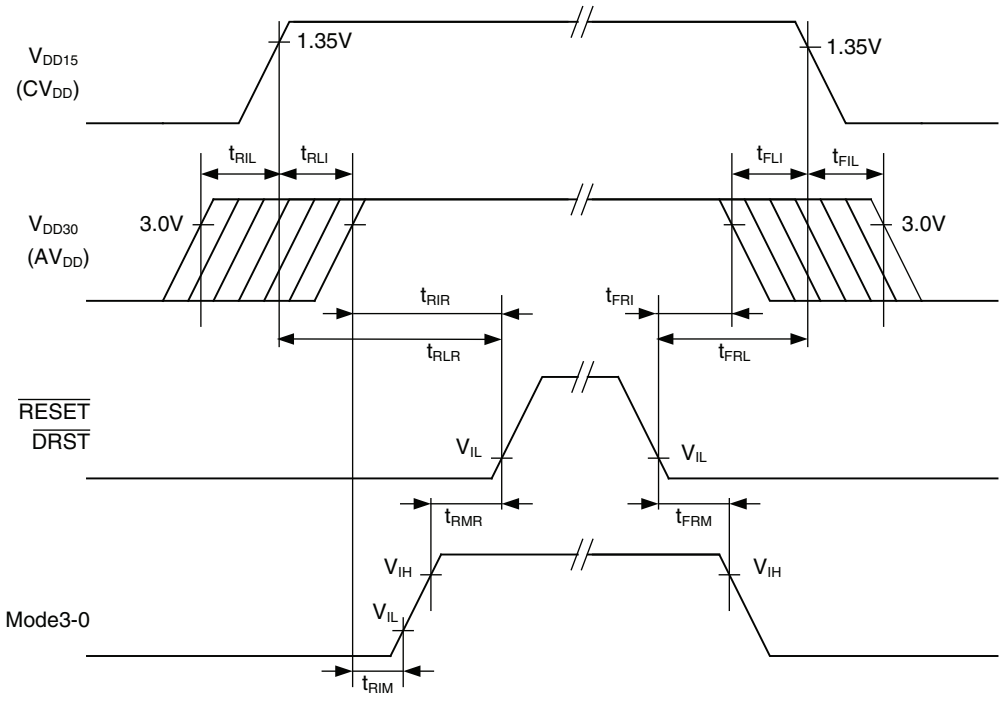
T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V

Table 1-8: Turning On / Interception Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
V_{DD15} to V_{DD30}	t_{RLI}		0	1	s
V_{DD30} to V_{DD15}	t_{RIL}		0	1	s
V_{DD15} to $\overline{RESET}$	t_{RLR}		0.5 + t_{OSC} [a]		ms
V_{DD30} to $\overline{RESET}$	t_{RIR}		0.5 + t_{OSC} [a]		ms
V_{DD30} to MODE1-0	t_{RIM}		0.2		ms
MODE1-0 to $\overline{RESET}$	t_{RMR}		0		ns
$\overline{RESET}$ to MODE1-0	t_{FRM}		0		ns
$\overline{RESET}$ to V_{DD30}	t_{FRI}		500		ns
$\overline{RESET}$ to V_{DD15}	t_{FRL}		500		ns
V_{DD30} to V_{DD15}	t_{FLI}		0	1	s
V_{DD15} to V_{DD30}	t_{FIL}		0	1	s

a. t_{OSC} depends on the external oscillator's stabilization time, crystal type and circuit and should be specified / evaluated in cooperation with the oscillator manufacturer

Figure 1-2: Turning On / Interception Timing



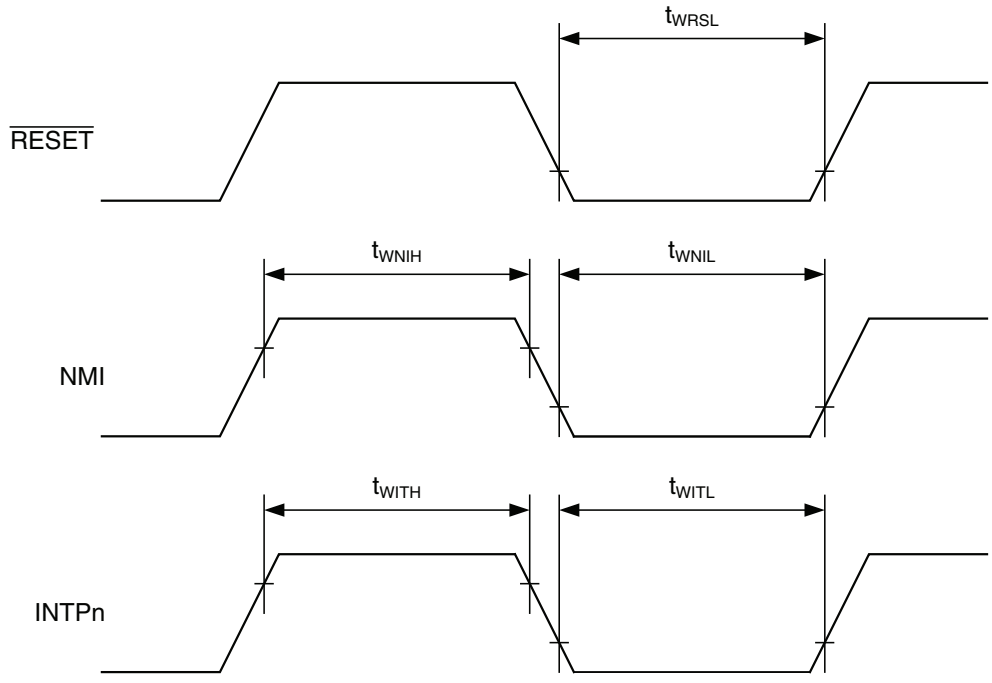
1.6.2 *Reset And Interrupt Timing*

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V

Table 1-9: Reset And Interrupt Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}	except for power on	500		ns
NMI input low level width	t_{WNIL}	(analog filter)	500		ns
NMI input high level width	t_{WNIH}	(analog filter)	500		ns
INTPn input low level width	t_{WITL}	n=0,1 (analog filter)	500		ns
		n=2...12 (digital filter)	Sampling clock × 5T		ns
INTPn input high level width	t_{WITH}	n=0,1 (analog filter)	500		ns
		n=2...12 (digital filter)	Sampling clock × 5T		ns

Figure 1-3: Reset And Interrupt Timing



Remark: n = 0 to 12

1.6.3 Clocked Serial Interface B (CSIB) Characteristics

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V
The load capacity of the output terminal is C_L = 35pF.

Table 1-10: CSIB Characteristics (Master Mode)

CBnCKS2 to CBnCKS0 ≠ 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{CYSKM}	125		ns
$\overline{SCKBn}$ high level width	t_{WSKHM}	$0.5 \cdot t_{CYSKM}$ - 10		ns
$\overline{SCKBn}$ low level width	t_{WSKLM}	$0.5 \cdot t_{CYSKM}$ - 10		ns
SIBn setup time	t_{SSISKM}	20		ns
SIBn hold time	t_{HSKSIM}	10		ns
SOBn delay	t_{DSKSOM}		10	ns
SOBn hold time	t_{HSKSOM}	$0.5 \cdot t_{CYSKM}$ - 10		ns

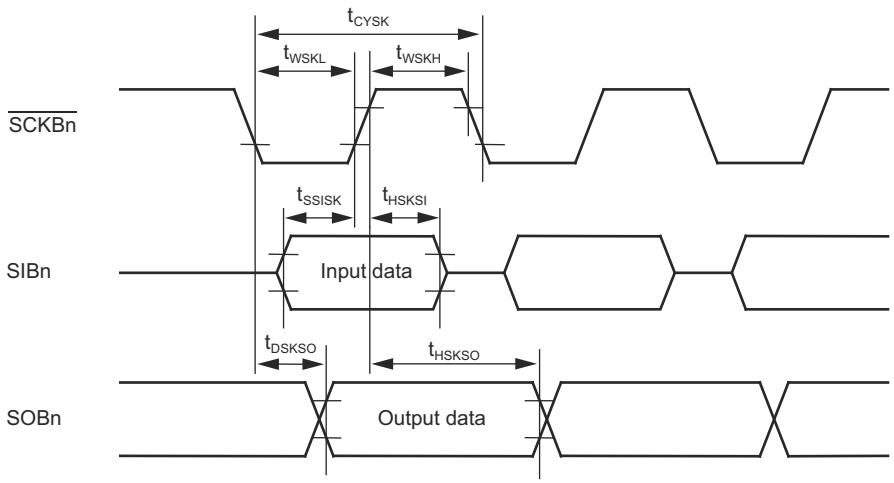
Table 1-11: CSIB Characteristics (Slave Mode)

CBnCKS2 to CBnCKS0 = 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{SCKBn}$ clock cycle time	t_{CYSKS}	125		ns
$\overline{SCKBn}$ high level width	t_{WSKHS}	$0.5 \cdot t_{CYSKS}$ - 10		ns
$\overline{SCKBn}$ low level width	t_{WSKLS}	$0.5 \cdot t_{CYSKS}$ - 10		ns
SIBn setup time	t_{SSISKS}	5		ns
SIBn hold time	t_{HSKSIS}	10		ns
SOBn delay	t_{DSKSOS}		25	ns
SOBn hold time	t_{HSKSOS}	t_{WSKHS}		ns

Remark: n = 0, 1

Figure 1-12: CSIB Master/Slave Mode Timing



1.6.4 Clocked Serial Interface E (CSIE) Timing

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V
The load capacity of the output terminal is C_L = 35pF.

Table 1-13: CSIE Characteristics (Master Mode)

Parameter		Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time		t_{KCY}	31.25		ns
$\overline{SCKEn}$ cycle time		t_{KCYM}	125		ns
$\overline{SCKEn}$ high, low width		t_{KWHM}, t_{KWLM}	$t_{KCYM}/2$ - 10		ns
SIEn input setup time (vs. $\overline{SCKEn}$)		t_{SSIM}	20		ns
SIEn input hold time (vs. $\overline{SCKEn}$)		t_{HSIM}	10		ns
SOEn output delay (vs. $\overline{SCKEn}$)		t_{DSOM}		10	ns
SOEn output hold time (vs. $\overline{SCKEn}$)		t_{HSOM}	$t_{KCYM}/2$ - 10		ns
SCSEnm inactive (High) width	CEnSIT=x CEnOPE=0 CEnMD=x	t_{WSCSB0}	$t_{KCYM}/2$ - 10		ns
	CEnSIT=x CEnOPE=1 CEnMD=x	t_{WSCSB1}	$(CS_{IDLE} + 0.5) \cdot t_{KCYM}$ - 10		ns
SCSEnm setup time (vs. $\overline{SCKEn}$)	CEnSIT=x CEnOPE=0 CEnIDL=x CEnMD=0	t_{SSCSB0}	t_{KCY} - 10		ns
	CEnSIT=x CEnOPE=1 CEnIDL=0 CEnMD=0	t_{SSCSB1}	$CS_{SETUP} \cdot t_{KCYM} + t_{KCY}$ - 10		ns
	CEnSIT=x CEnOPE=1 CEnIDL=1 CEnMD=1	t_{SSCSB2}	$CS_{SETUP} \cdot t_{KCYM} + t_{KCY}$ - 10		ns
SCSEnm hold time (vs. $\overline{SCKEn}$)	CEnSIT=0 CEnOPE=0 CEnMD=x	t_{HSCSB0}	t_{KCY} - 10		ns
	CEnSIT=1 CEnOPE=0 CEnMD=x	t_{HSCSB1}	$t_{KCYM}/2$ - 10		ns
	CEnSIT=0 CEnOPE=1 CEnMD=x	t_{HSCSB2}	$CS_{HOLD} \cdot t_{KCYM}$ - 10		ns
	CEnSIT=1 CEnOPE=1 CEnMD=x	t_{HSCSB3}	$(CS_{HOLD} + 0.5) \cdot t_{KCYM}$ - 10		ns

Table 1-13: CSIE Characteristics (Master Mode)

Parameter		Symbol	MIN.	MAX.	Unit
SCSEnm interframe time	CEnSIT=x CEnOPE=1 CEnMD=x	t_{INTER}	$CS_{INTER} \cdot t_{KCYM}$		ns
	CEnSIT=x CEnOPE=0 CEnMD=x	-	Not Applicable		ns

Remark: n = 0, 1
m = 7 - 0 (n = 0), 3 - 0 (n = 1)
CS_{SETUP},CS_{INTER}: are set by register CEnOPT0
CS_{IDLE},CS_{HOLD}: are set by register CEnOPT1

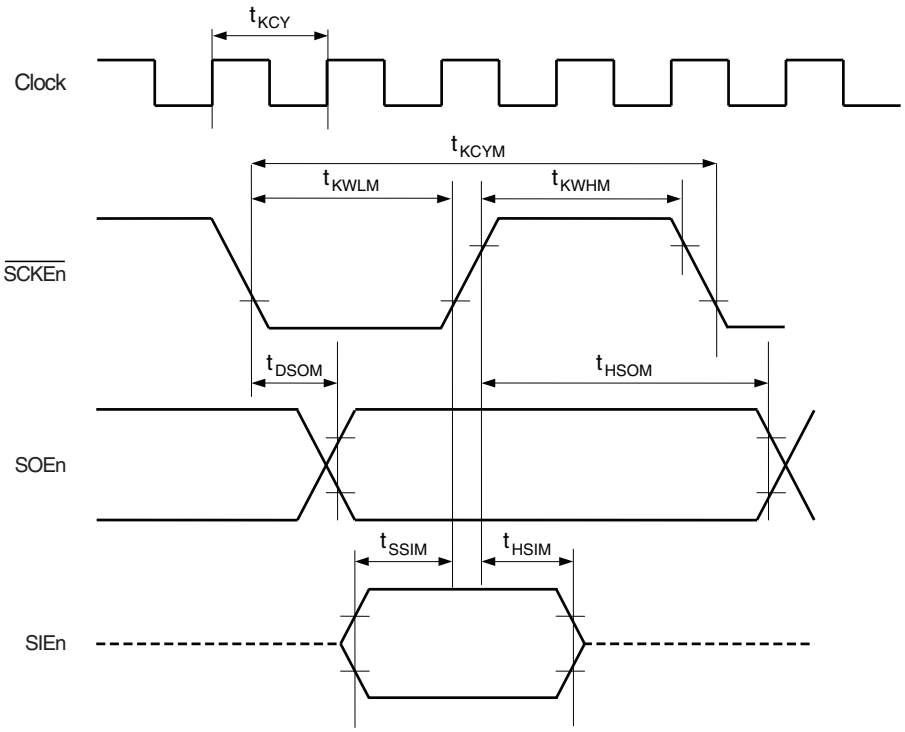
Table 1-14: CSIE Characteristics (Slave Mode)

Parameter	Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time	t_{KCY}	31.25		ns
$\overline{SCKEn}$ cycle time	t_{KCYS}	125		ns
$\overline{SCKEn}$ high, low width	t_{KWHS}, t_{KWLS}	$t_{KCYS}/2$ - 10		ns
SIEn input setup time (vs. $\overline{SCKEn}$)	t_{SSIS}	10		ns
SIEn input hold time (vs. $\overline{SCKEn}$)	t_{HSIS}	$t_{KCY} \cdot 1.5 + 10$		ns
SOEn output delay (vs. $\overline{SCKEn}$)	t_{DSOS}		20	ns
SOEn output hold time (vs. $\overline{SCKEn}$)	t_{HSOS}	$t_{KCYS}/2$ - 10		ns

Remark: n=0, 1

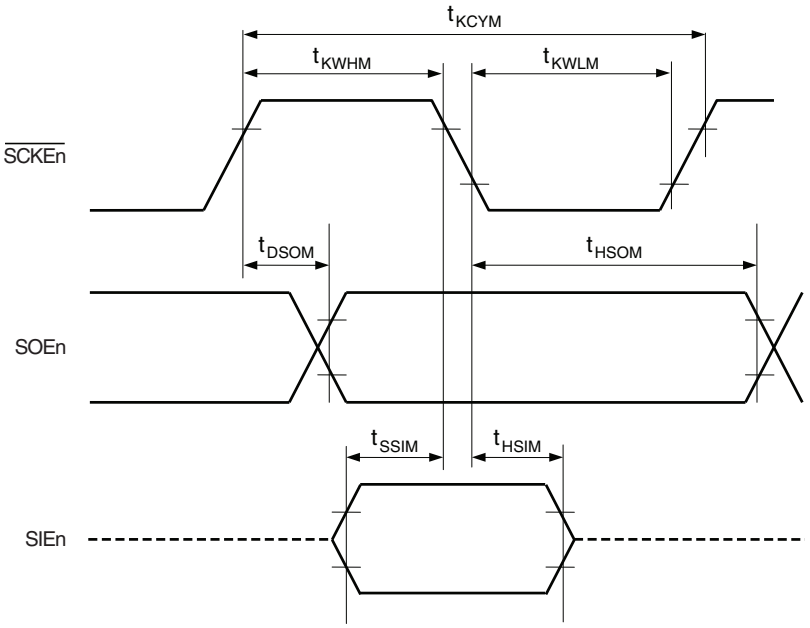
Figure 1-15: CSIEn Timings

(a) [$\overline{SCKEn}$/SIEn/SOEn] Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)



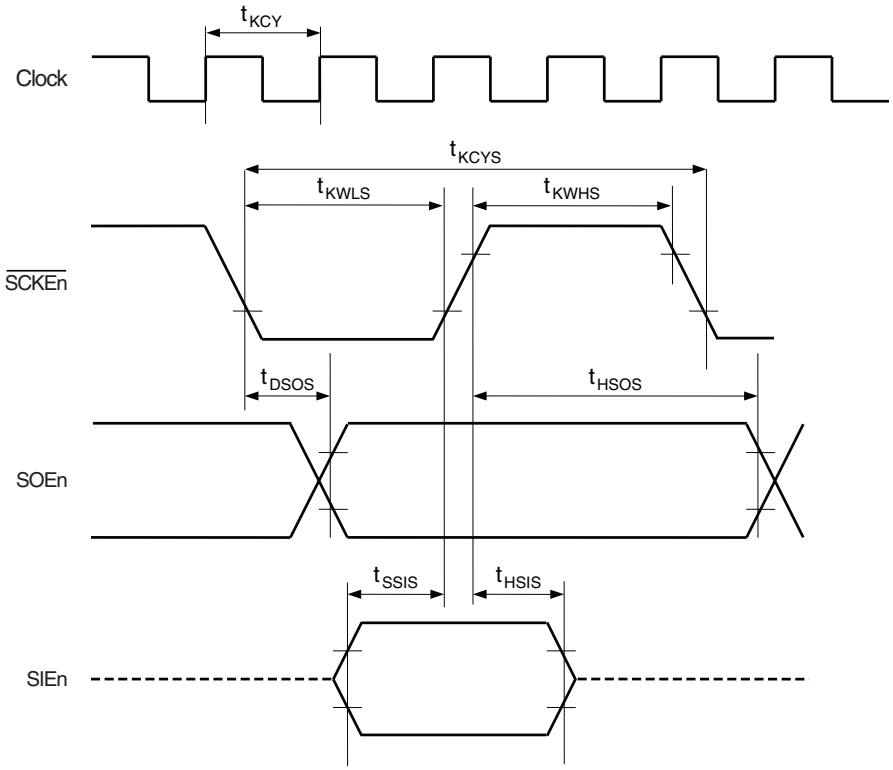
Remark: n = 0, 1

(b) [$\overline{SCKEn}$/SIEn/SOEn] Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)



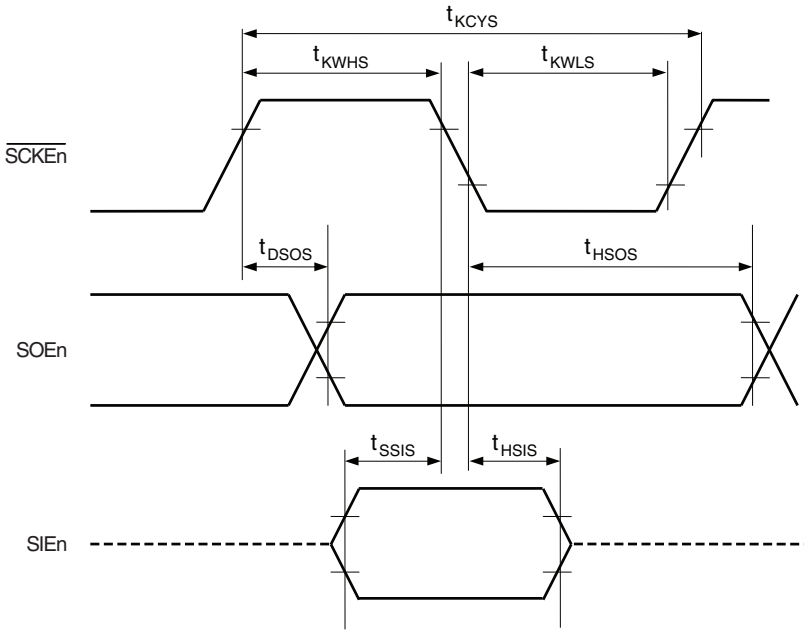
Remark: n = 0, 1

(c) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)



Remark: n = 0, 1

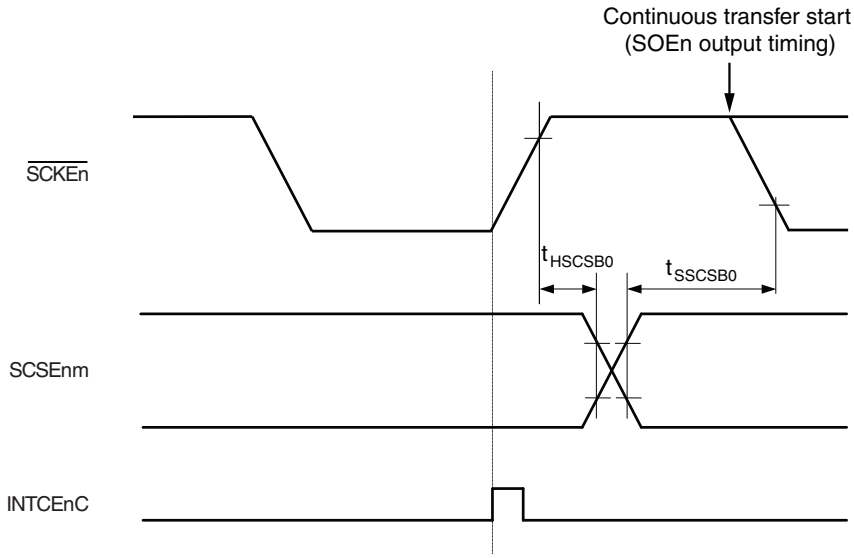
(d) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)



Remark: n = 0, 1

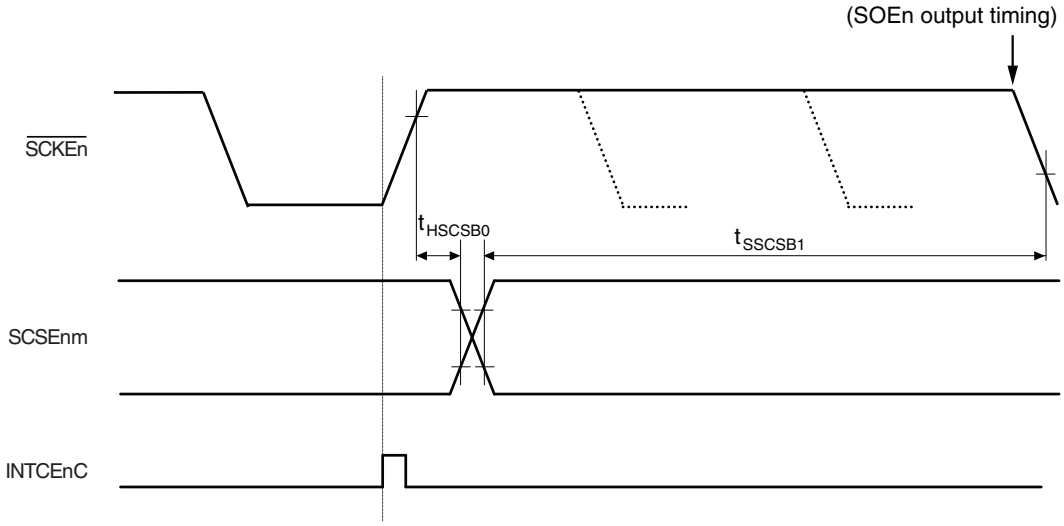
Figure 1-16: CSEn7 - CSEn0 Pin Timings

(e) Only In Master Mode (CEnCTL0:CEnSIT/CEnWE=0/0 & CEnCTL4:CEnOPE=0)



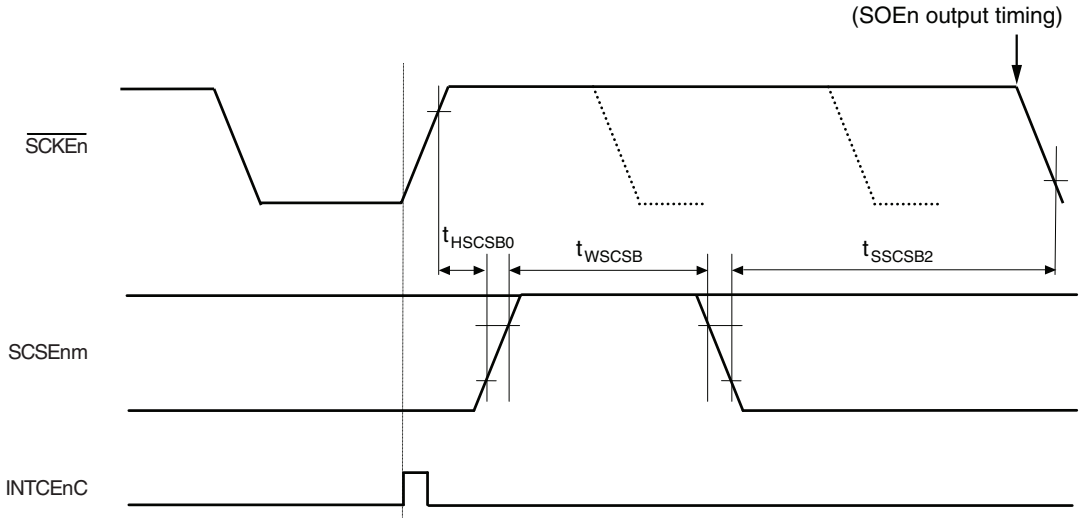
Remark: n = 0, 1
m = 7 - 0 (n = 0), 3 - 0 (n = 1)
INTCEnC: CSIEn transfer end interrupt

(f) Only In Master Mode (CEnCTL0:CEnSIT/CEnWE/CEnCSM=0/1/0 & CEnCTL4:CEnOPE=0)



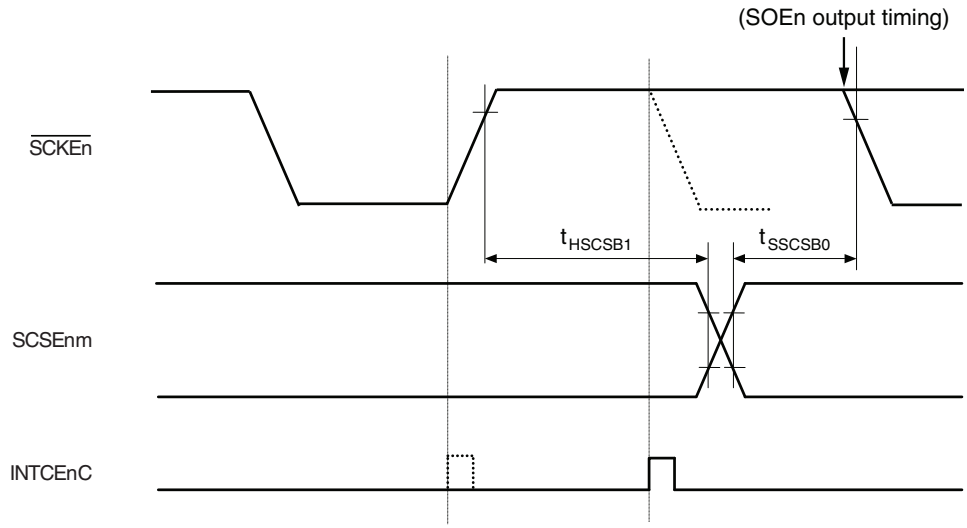
Remark: n = 0, 1
m = 7 - 0 (n = 0), 3 - 0 (n = 1)
INTCEnC: CSIEn transfer end interrupt

(g) Only In Master Mode (CEnCTL0:CEnSIT/CEnWE/CEnCSM=0/1/1 & CEnCTL4:CEnOPE=0)



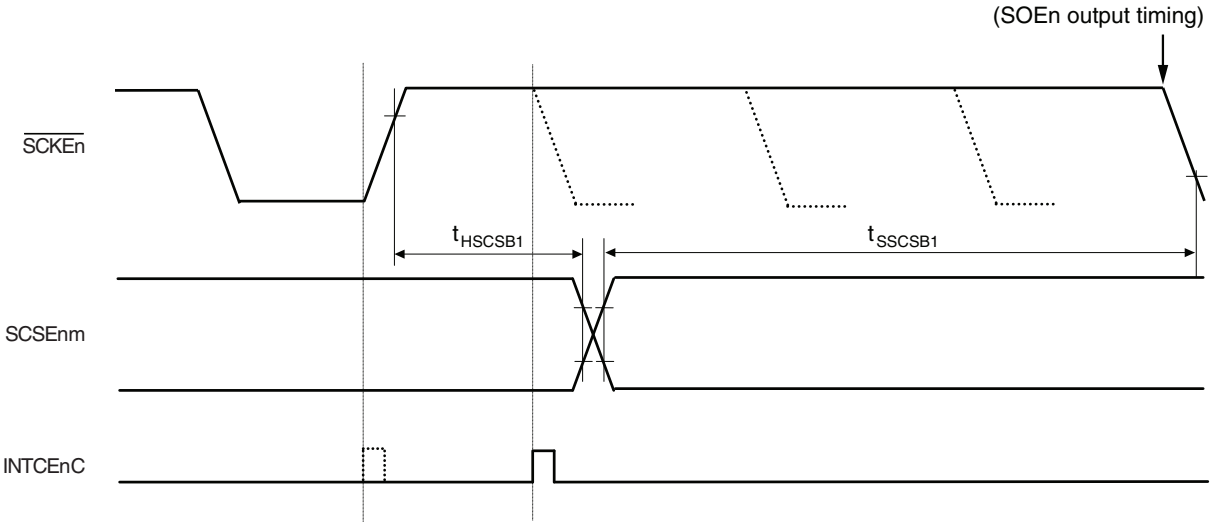
Remark: n = 0, 1
m = 7 - 0 (n = 0), 3 - 0 (n = 1)
INTCEnC: CSIEn transfer end interrupt

(h) Only In Master Mode (CEnCTL0:CEnSITCEnWE/CEnCSM=1/1/0 & CEnCTL4:CEnOPE=0)



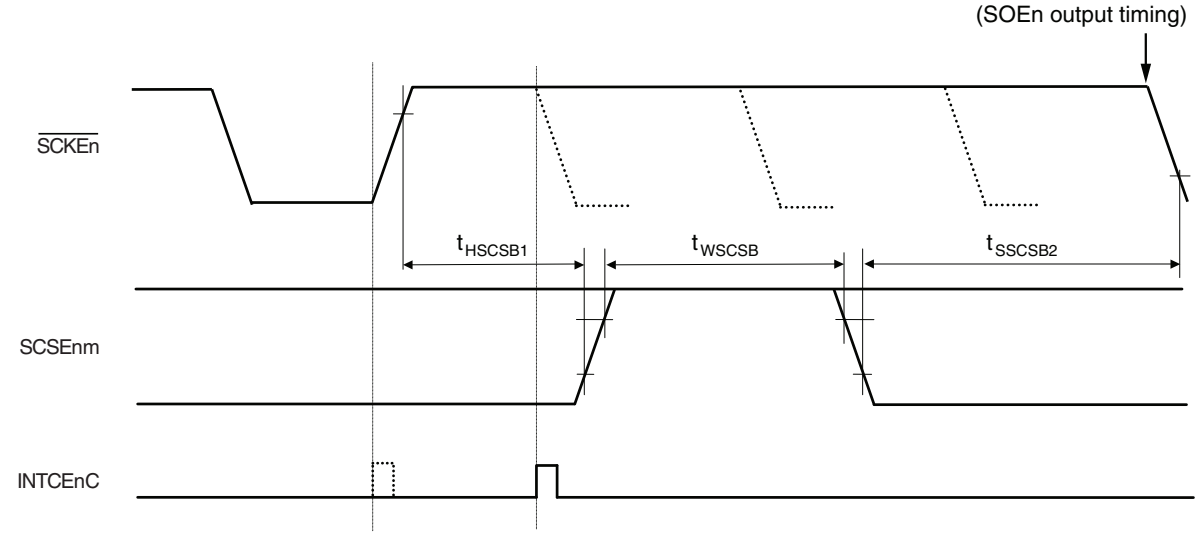
Remark: n = 0, 1
m = 7 - 0 (n = 0), 3 - 0 (n = 1)
INTCEnC: CSIEn transfer end interrupt

(i) Only In Master Mode (CEnCTL0:CEnSIT/CEnWE/CEnCSM=1/1/0 & CEnCTL4:CEnOPE=0)



Remark: n = 0, 1
m = 7 - 0 (n = 0), 3 - 0 (n = 1)
INTCEnC: CSIEn transfer end interrupt

(j) Only In Master Mode (CEnCTL0:CEnSIT/CEnWE/CEnCSM=1/1/1 & CEnCTL4:CEnOPE=0) Or (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE=1)



Remark: n = 0, 1
m = 7 - 0 (n = 0), 3 - 0 (n = 1)
INTCEnC: CSIEn transfer end interrupt

1.6.5 UARTC Timing

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V
The load capacity of the output terminal is C_L = 35pF.

Table 1-17: UARTC Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UARTC}			4	Mbps

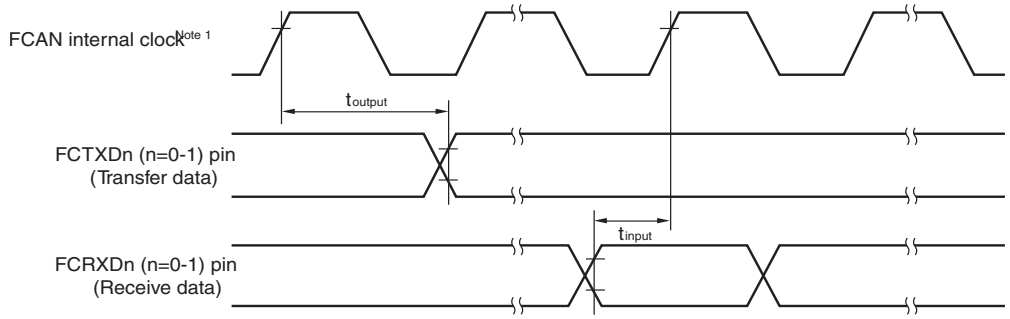
1.6.6 CAN Timing

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V
The load capacity of the output terminal is C_L=35pF.

Table 1-18: CAN Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Internal transmit to receive data delay	t_{node}	$t_{node} = t_{output} + t_{input}$		75	ns

Figure 1-19: CAN Timing



Notes: 1. The FCAN internal clock corresponds to the FCAN macro clock.

Figure 1-20: Internal Delay

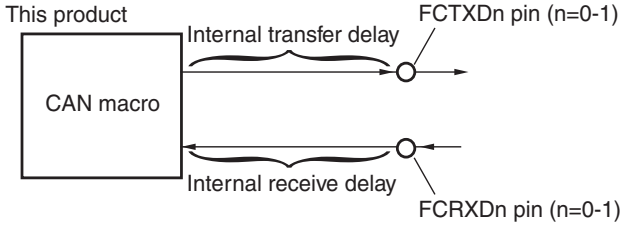


Image figure of internal delay

1.6.7 AD Converter

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD} = AV_{REF0,1}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{DD}$ = 0V

Table 1-21: AD Converter Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution				10		bit
Overall error[a]	TOE				±4	LSB
Quantization error					±0.5	LSB
Conversion time[b]	t_{CONV}		2.0		8.0	µs
Sampling time[c]	t_{SAMP}			$3 \cdot t_{CONV} / 16$		s
Analog input voltage	V_{IAN}		$AV_{SS0,1}$		$AV_{REF0,1}$	V
AV_{REFn} input voltage	$AV_{REF0,1}$	$AV_{REF0,1} = AV_{DD}$			AV_{DD}	V
AV_{REFn} input current	$AI_{REF0,1}$			60	300	µA
AV_{DD} supply current	AI_{DD}				6	mA

a. The quantization error is not included.
b. The conversion time depends on register setting ADMn1. For ADMn1 register setting please refer to the users manual.
c. The sampling time depends on the conversion time and thus from the ADMn1 register seeting. For ADMn1 register setting please refer to the users manual.

1.6.8 Flash Memory Programming Characteristics

(1) Basic Characteristics

T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V
The load capacity of the output terminal is C_L = 35pF.

Table 1-22: Flash Programming Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	f_{CPU}				80	MHz
High Level Input Voltage	V_{IH}	FLMD0	$0.8 \cdot V_{DD30}$		V_{DD30}	
Low Level Input Voltage	V_{IL}	FLMD0	-0.5		$0.2 \cdot V_{DD30}$	
Code Flash	Rewrite count	C_{ERWR}[a]			100	times
	Data retention				15	years
Data Flash	Rewrite count	C_{ERWR}[a]			10000	times
	Data retention				3	years

a. The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: (P: Program(write) E: Erase)
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(2) Serial Writing Operating Conditions

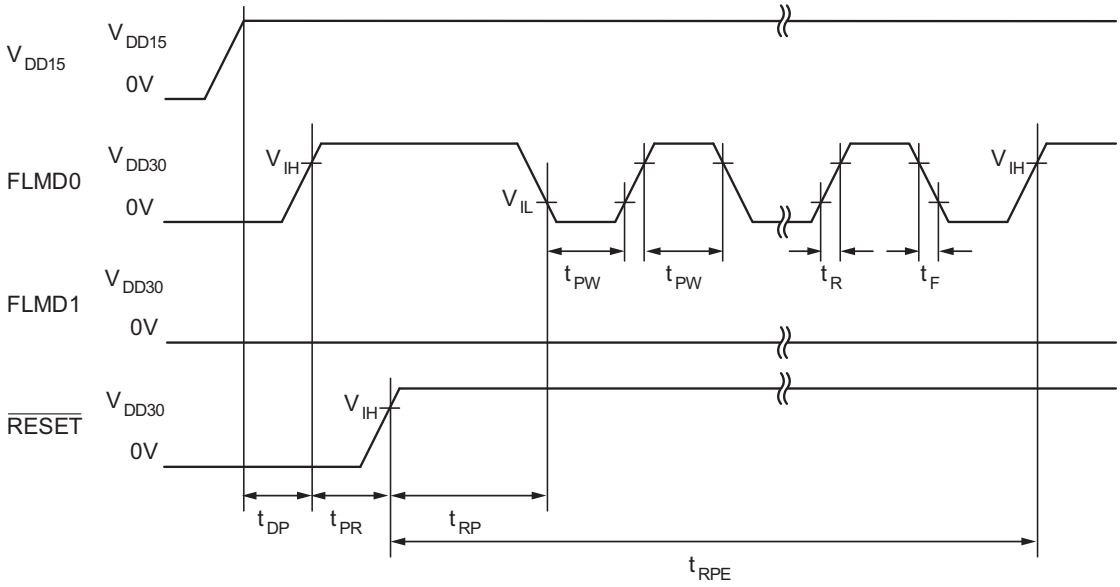
T_a = -40 to +125°C
$V_{DD15} = CV_{DD}$ = 1.5V ± 10%
$V_{DD30} = AV_{DD}$ = 3.3V ± 0.3V
$V_{SS15} = CV_{SS} = V_{SS30} = AV_{SS}$ = 0V
The load capacity of the output terminal is C_L = 35pF.

Table 1-23: Serial Writing Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from V_{DD15})	t_{DP}		1			ms
RESET release (from FLMD0)	t_{PR}	[a]	2			ms
Count start time from $\overline{\text{RESET}}$ to FLMD0	f_{RP}		1.2			ms
Count finish time from $\overline{\text{RESET}}$ to FLMD0	f_{RPE}				10	ms
FLMD0 high / low level width	t_{PW}		10		100	µs
FLMD0 rise / fall time	t_R / t_F				1	µs

a. Turning on timing has to be considered for all power supply voltages, refer to 1.6.1 Power Supply Turning On / Interception Timing

Figure 1-24: Serial Write Operation Timing



2. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to the Joint Industry Standard:

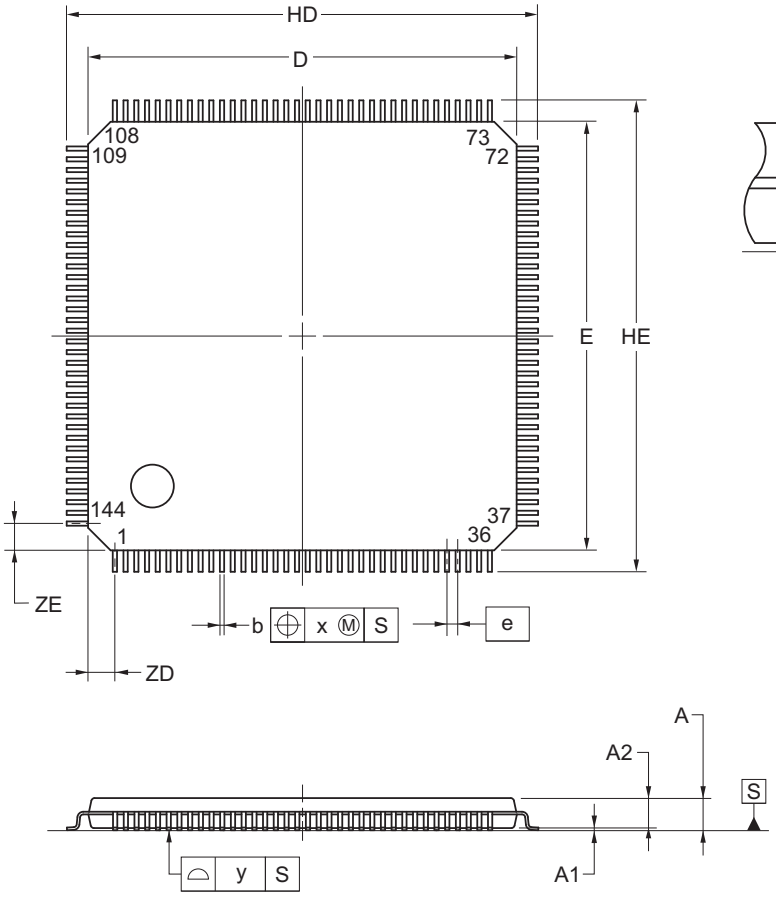
JEDEC J-STD-020C (MSL=3)

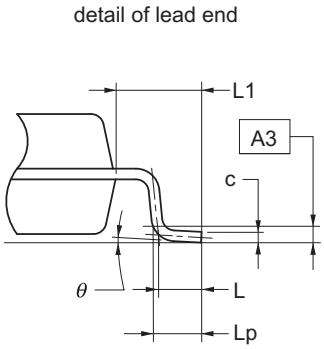
For soldering methods and conditions other than those recommended please consult NEC.

3. Package

3.1 Package Dimension of μPD70F3485GJ(A2)-GAE

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)





(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	20.00±0.20
HD	22.00±0.20
HE	22.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P144GJ-50-GAE-2

4. Revision History

Table 4-1: Revision History

Version	Date	Remarks
1.0	2008/11/21	Initial version
2.0	2010/01/14	Flash memory size of 512 KB splitted into internal flash memory of 480 KB and data flash of 32 KB. µPD70F3485W-CAR (bare die) derivate removed. V_{DD15x}, V_{SS15x} replaced by V_{DD15}, V_{SS15}. CV_{DD15}, CV_{SS15} replaced by CV_{DD}, CV_{SS}. V_{DD3x}, V_{SS3x} replaced by V_{DD30}, V_{SS30}. I_{DD3} replaced by I_{DD30}. Input level VIH/VIL of MODE1 (FLMD0) pin corrected (to same input level as MODE0 pin). Frequency name f_{XX} replaced by f_{CPU} in Table 1-7 conditions. Parameter “Reprogramming” replaced by “Rewrite count C_{ERWR}” in Table 1-22. Reference voltage supply for FLMD0 setup time changed from (unspecific) VDD to VDD15 in Table 1-23 and Figure 1-24.

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