µPD70F4177, 70F4178

– V850E2/FF4-G –

RENESAS MCU

R01DS0167EJ0100
Rev.1.00
Apr 16, 2014

The µPD70F4177 and 70F4178 are 32-bit single-chip microcontrollers from the V850 family. Especially designed for real-time control, a 32-bit CPU, ROM, RAM, interrupt controller, timers, serial interfaces, an A/D converter, a DMA controller, CAN controllers and more are all integrated on a single chip.

Detailed descriptions of the functions of this product are given in the user's manual with the title below. Be sure to read it whenever you incorporate these products in a design.

V850E2/Fx4-G, Hardware: R01UH0366EJ

Application

- Automotive electronics

Contents

Specification Overview

Series name:			FF4-G-256KB	FF4-G-512KB
Part number:			**µPD70F4177**	**µPD70F4178**
Internal memory	Code flash		256 KB	512 KB
	Data flash		32 KB	
	RAM		32 KB	64 KB
	Back RAM		4 KB	
External memory iinterface (MEMC)			not provided	
CPU	CPU system		V850E2S	
	CPU frequency		64 MHz max.	
	System Protection Function (SPF)	MPU	provided	
		SRP	provided	
DMA			8 channels	
Operating clock	Main Oscillator (MainOsc)		4, 5, 6, 8, 10, 12, 16, 20 MHz	
	Low Speed Internal Oscillator (LS IntOsc)		240 kHz typ.	
	High Speed Internal Oscillator (HS IntOsc)		8 MHz typ.	
	Sub-clock Oscillator (SubOsc)		not provided	
	PLL		4, 5, 6, 8, 10, 12, 16, 20 MHz max.	
I/O ports			59	
A/D converter (ADCA)			1 × 10 channels, 10 bits	
Timers	Timer Array Unit B (TAUB), 16 bits		1 unit × 16 channels	
	Timer Array Unit J (TAUJ), 32 bits		1 unit × 4 channels	
	Window Watchdog Timer (WDTA)		2 channels	
	Operating Sytem Timer (OSTM)		1 channel	
Serial interfaces	CAN (FCN)		3 channles (32 messages buffer)	6 channles (32 messages buffer)
	UART I/F (URTE) with LIN Master Controller (LM)		2 channels	
	CSI (CSIG)		2 channels	
	I^2C (IICB)		1 channel	
Interrupts	Maskables	External	9	
		Internal	61	70
	Non-maskable (NMI)	External	1	
		Internal	2	
Other functions	Power-On-Clear (POC)		provided	
	Clock Monitors (CLMA)		provided for MainOsc, HS IntOsc, PLL supervision	
	Key Return (KR)		8 channels	
	On-Chip debug (OCD)		provided	
Voltage supply	System supply		V_{POC} to 5.5 V[a]	
	Port supply		V_{POC} to 5.5 V	
Operating Temperature			–40°C to + 125°C[a]	
Package			80-pin LQFP	

a) Refer to the **Electrial Target Specification**.

Order Information

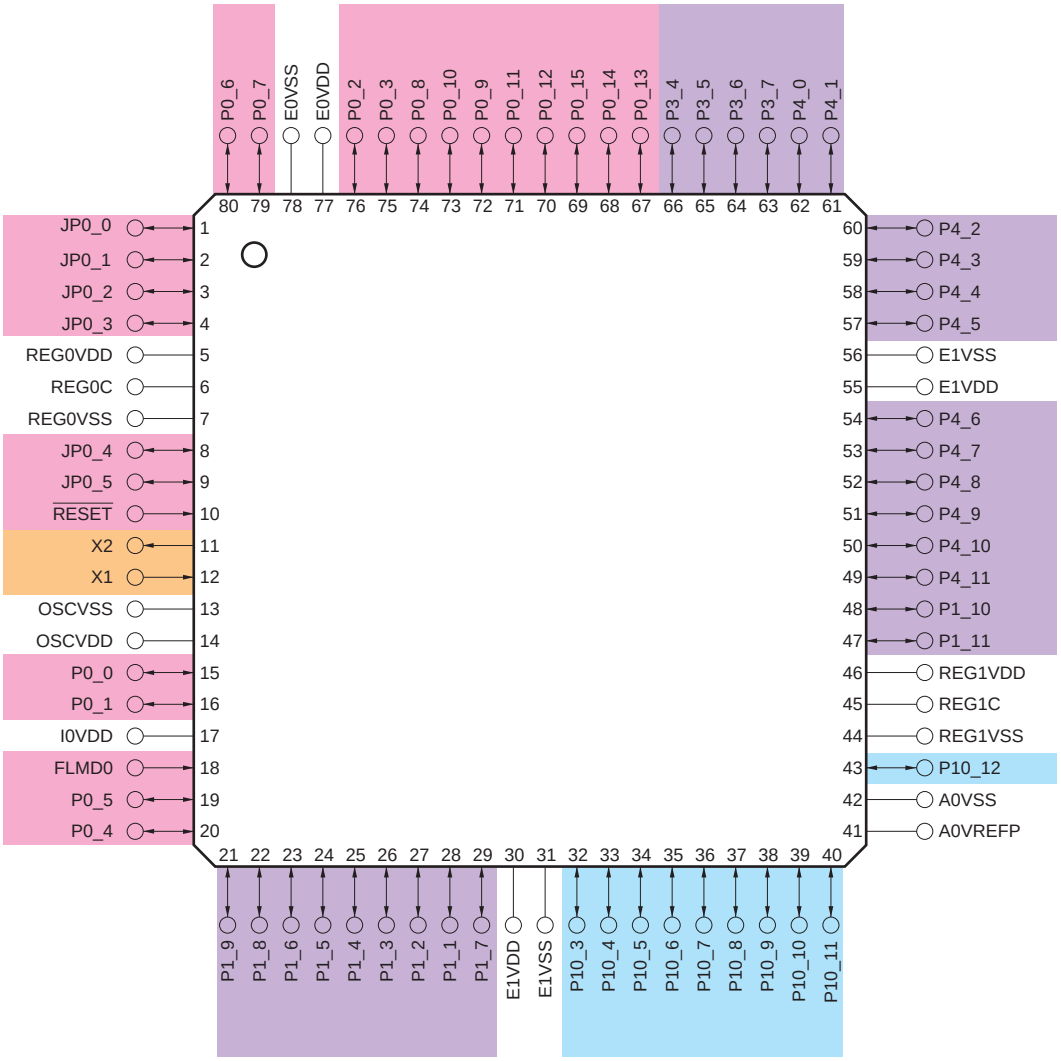
Ordering Code	Package	On-Chip Code Flash	On-chip Local RAM	Quality Level	Remark
µPD70F4177GCA-UEU-AX	80-Pin Plastic LQFP (Fine Pitch; 12 × 12)	256 Kbytes	32 Kbytes	(A)	
µPD70F4177GCA1-UEU-AX				(A1)	
µPD70F4177GCA2-UEU-AX				(A2)	
µPD70F4178GCA-UEU-AX		512 Kbytes	64 Kbytes	(A)	
µPD70F4178GCA1-UEU-AX				(A1)	
µPD70F4178GCA2-UEU-AX				(A2)	

Note 1. The ranges of operating temperature for all of these products are listed below.
(A)-grade product –40 to + 85°C
(A1)-grade product –40 to + 110°C
(A2)-grade product –40 to + 125°C

Note 2. Products with the suffix “-AX” in the ordering codes are lead-free.

Pin Connections (Top View)

80-Pin Plastic LQFP (Fine Pitch; 12 x 12)



Note Pins for the power supply sources

: E0VDD, E1VDD (AWO Port)
: OSCVDD
: E1VDD, E0VDD (ISO0 Port)
: A0VREFP

(1/2)

Pin No.	Name
1	JP0_0/INTP0/TAUJ0I0/TAUJ0O0/DCUTDI
2	JP0_1/INTP1/TAUJ0I1/TAUJ0O1/DCUTDO
3	JP0_2/INTP2/TAUJ0I2/TAUJ0O2/DCUTCK
4	JP0_3/INTP3/TAUJ0I3/TAUJ0O3/DCUTMS
5	REG0VDD
6	REG0C
7	REG0VSS
8	JP0_4/$\overline{\text{DCUTRST}}$
9	JP0_5/NMI/$\overline{\text{DCURDY}}$
10	$\overline{\text{RESET}}$
11	X2
12	X1
13	OSCVSS
14	OSCVDD
15	P0_0/DPIN0/$\overline{\text{CSIG4SSI}}$/ADCA0TRG0/INTP0
16	P0_1/DPIN1/CSIG4DCS/CSIG4SO/INTP1/TAUB0O1/FLMD1
17	I0VDD
18	FLMD0
19	P0_5/FCN0RX/DPIN5/INTP12
20	P0_4/DPIN4/FCN0TX/INTP11
21	P1_9/TAUB0I9/TAUB0O9/INTP3/FCN2TX
22	P1_8/TAUB0I8/TAUB0O8/FCN2RX
23	P1_6/TAUB0I6/TAUB0O6/FCN4TX
24	P1_5/TAUB0I5/TAUB0O5/FCN4RX
25	P1_4/TAUB0I4/TAUB0O4/FCN3TX
26	P1_3/TAUB0I3/TAUB0O3/FCN3RX
27	P1_2/TAUB0I2/TAUB0O2/FCN1TX
28	P1_1/TAUB0I1/TAUB0O1/FCN1RX/FCN0TX
29	P1_7/TAUB0I7/TAUB0O7/FCN0RX
30	E1VDD
31	E1VSS
32	P10_3/ADCA0I3
33	P10_4/ADCA0I4
34	P10_5/ADCA0I5
35	P10_6/ADCA0I6
36	P10_7/ADCA0I7
37	P10_8/ADCA0I8
38	P10_9/ADCA0TRG0/ADCA0I9
39	P10_10/ADCA0TRG1/ADCA0I10
40	P10_11/ADCA0TRG2/ADCA0I11

(2/2)

Pin No.	Name
41	A0VREFP
42	A0VSS
43	P10_12/ADCA0I12
44	REG1VSS
45	REG1C
46	REG1VDD
47	P1_11/TAUB0I11/TAUB0O11/FCN5TX
48	P1_10/TAUB0I10/TAUB0O10/FCN5RX/INTP4
49	P4_11/FCN5TX
50	P4_10/CSIG4RYI/FCN5RX
51	P4_9/CSIG0RY0/FCN4TX
52	P4_8/CSIG4SC/KR0I0/FCN4RX
53	P4_7/INTP4/URTE11RX/CSIG4SO/KR0I1/FCN3TX
54	P4_6/CSIG4SI/URTE11TX/KR0I2/FCN3RX
55	E1VDD
56	E1VSS
57	P4_5/CSIG0SC/KR0I13/FCN2TX
58	P4_4/INTP2/URTE10RX/CSIG0SO/FCN2RX
59	P4_3/CSIG0SI/URTE10TX/FCN1TX
60	P4_2/TAUB0I15/TAUB0O15/FCN1RX
61	P4_1/TAUB0I14/TAUB0O14/FCN0TX
62	P4_0/TAUB0I13/TAUB0O13/FCN0RX
63	P3_7/TAUB0I7/TAUB0O7/CSIG0SI
64	P3_6/TAUB0I6/TAUB0O6/CSIG0DCS/CSIG0SO
65	P3_5/TAUB0I5/TAUB0O5/KR0I4/CSIG0SC
66	P3_4/TAUB0I4/TAUB0O4/KR0I5/CSIG0RYI/CSIG0RYO
67	P0_13/TAUJ0I1/DPIN13/TAUJ0O1/KR0I5/FCN5TX/CSIG0SI
68	P0_14/TAUJ0I2/TAUJ0O2/DPO/KR0I6/FCN5RX/CSIG0DCS/CSIG0SO
69	P0_15/TAUJ0I3/TAUJ0O3/APO/KR0I7/FCN4RX/CSIG0SC
70	P0_12/TAUJ0I0/DPIN12/TAUJ0O0/KR0I0/INTP8/FCN4TX/$\overline{\text{CSIG0SSI}}$
71	P0_11/URTE11RX/DPIN11/FCN2RX
72	P0_9/URTE10RX/DPIN9/FCN2TX/KR0I4/INTP6/TAUB0O6/IICB0SCL
73	P0_10/DPIN10/URTE11TX/FCN3RX
74	P0_8/DPIN8/URTE10TX/KR0I3/FCN3TX/TAUB0O5/IICB0SDA
75	P0_3/DPIN3/CSIG4SC/ADCA0TRG1/INTP3
76	P0_2/DPIN2/CSIG4SI/ADCA0TRG2/INTP2/TAUB0O2
77	E0VDD
78	E0VSS
79	P0_7/URTE11RX/DPIN7/FCN1TX/KR0I2/INTP4
80	P0_6/FCN1RX/DPIN6/URTE11TX/KR0I1/NMI

Internal Block Diagram

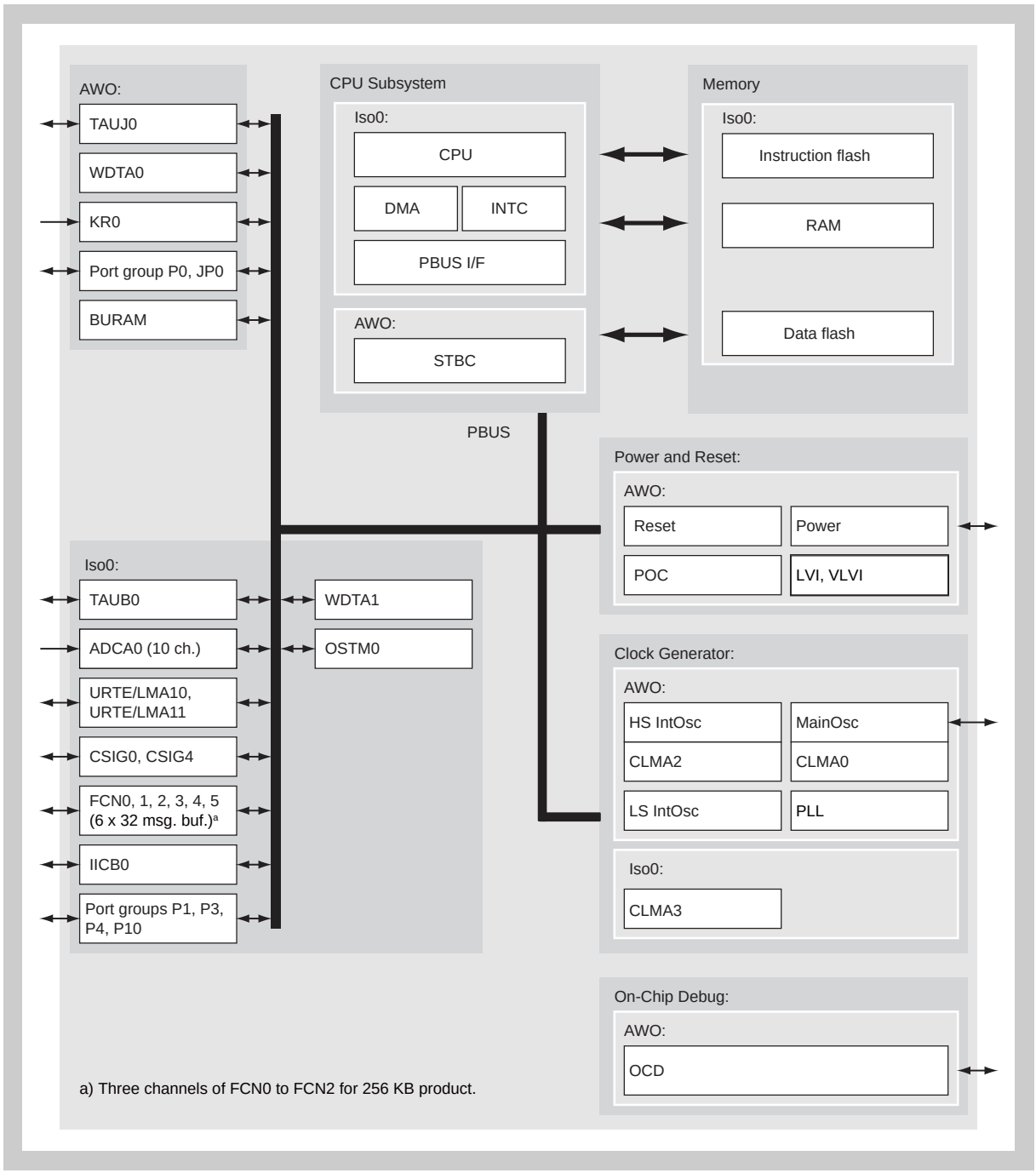


Figure 1-3 Block Diagram of V850E2/FF4-G

Section 1 Overview

1.1 Naming

1.1.1 Alternative Function Pins

Peripheral	Prefix	Function name	Suffix
Short-cut of macro name	Consecutive number for same peripheral module[a]	Peripheral Macro pin naming	Consecutive number for same pin names[a]

a) This is an option that can be omitted if meaning is obvious

Example:

– CSIG0SO, CSIG0SI, CSIG0SC, CSIG0RYI, CSIG0RYO

1.1.2 Power Supply Pins

Function	Prefix	Kind of supply
Symbol	Consecutive number for different functions[a]	VDD or VSS

a) This is an option that can be omitted if meaning is obvious

Example:

– OSCVDD, E0VDD, REG0VSS

Function	Explanation
REG	Internal regulator supply
OSC	Oscillator supply
I0	Flash module supply and ISO0 Internal regulator supply
E	Standard buffer supply
A	Analog module supply (e.g. ADC)

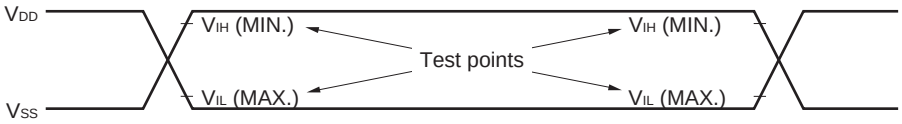
1.2 Pin Groups

Symbol	Pin group supplied by	Related pins / ports
PgE0	E0VDD, E0VSS	Related ports: JP0, P0 Related pins: RESET, FLMD0
PgE1	E1VDD, E1VSS	Related ports: P1, P3, P4
PgOSC	OSCVDD, OSCVSS	Related pins: X1, X2
PgA0	A0VREFP, A0VSS	Related ports: P10

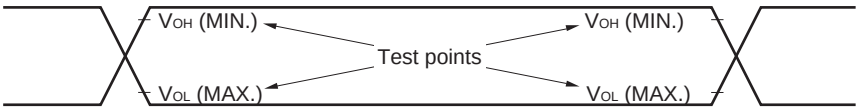
1.3 General Measurement Conditions

1.3.1 AC Characteristic Measurement Condition

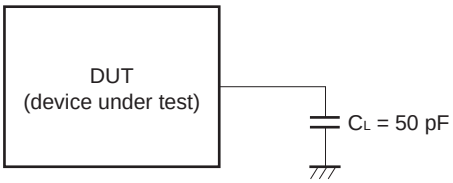
(1) AC test input measurement points



(2) AC test output measurement points



(3) Load conditions



Caution A load capacitance in the circuit configuration exceeding 50 pF can lead to input to the buffers and so on, so ensure that the load capacitance for the device is no greater than 50 pF.

Section 2 Absolute Maximum Ratings

Notes

1. Do not directly connect outputs (or input/outputs) to each other or to VDD, VCC, or GND.
2. Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings.
   The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.
3. In designing the external circuit, ensure that the connections are such that pins which enter the high-impedance state do not conflict with outputs.

2.1 Supply voltages

Table 2-1 VDD Data

Parameter	Symbol	Condition	Ratings	Unit
System	I0VDD		–0.3 to +6.0	V
	OSCVDD		–0.3 to +6.0	V
	REG0VDD		–0.3 to +6.0	V
	REG1VDD		–0.3 to +6.0	V
Ports	E0VDD		–0.3 to +6.0	V
	E1VDD		–0.3 to +6.0	V
ADC0	A0VREFP		–0.3 to +6.0	V

Ta = 25°C

2.2 Port voltages

Table 2-2 Port Input voltage

Parameter	Pin Group[a]	Symbol	Condition	Ratings	Unit
Input voltage[b]	PgE0	V_I	E0VDD ≤ 5.5 V	–0.3 to E0VDD + 0.3	V
	PgE1		E1VDD ≤ 5.5 V	–0.3 to E1VDD + 0.3	V
	PgOSC		OSCVDD ≤ 5.5 V	–0.3 to OSCVDD + 0.3	V
	PgA0			–0.3 to A0VREFP + 0.3	V

a) The column reflects all supplies within the device series. Therefore, not each pin group is available for each product.

b) The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Ta = 25°C

2.3 Port current

Table 2-3 High level port output current

Parameter	Pin Group[a]	Symbol	Condition	Max. spec	Unit
High level output current	PgE0/PgE1	I_{OH}	1 pin	-10	mA
			Total of all PgE0 and PgE1 pins	-60	mA
	PgA0		1 pin	-10	mA
			Total pin	-25	mA

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

Table 2-4 Low level port output current

Parameter	Pin Group[a]	Symbol	Condition	Max. spec	Unit
Low level output current	PgE0/PgE1	I_{OL}	1 pin	10	mA
			Total of all PgE0 and PgE1 pins	60	mA
	PgA0		1 pin	10	mA
			Total pin	25	mA

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

2.4 Thermal characteristics

Table 2-5 Thermal characteristics

Parameter	Symbol	Condition	Ratings	Unit
Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_A	(A) grade products	-40 to +85	°C
		(A1) grade products	-40 to +110	°C
		(A2) grade products	-40 to +125	°C

Section 3 Power supply specification

3.1 Requirements for external power supply connections

3.1.1 Definition of ground supply pins

This specification denotes ground supply pins as:
VSS = OSCVSS = REGnVSS = EnVSS = A0VSS = 0 V

in the further text.
With
- REGnVSS: REG0VSS, REG1VSS
- EnVSS: E0VSS, E1VSS

3.1.2 Definition of power supply pins

This specification denotes power supply pins as:
- EnVDD, I0VDD, REGnVDD, OSCVDD, A0VREFP

in the further text.
With
- EnVDD: E0VDD, E1VDD
- REGnVDD: REG0VDD, REG1VDD

3.2 Power area definitions

The device consists of the following power areas:
- AWO (Always-On area)
- Iso0 (Isolated area 0)

The table below lists the related core and port voltage supply of each power area:

Table 3-1 Power areas supply voltages

Power Area	Supply voltage	Related pins
AWO	Internal regulator supply	REG0VDD, REG0VSS
	Port supply	E0VDD, E0VSS
	Other	OSCVDD, OSCVSS, I0VDD
Iso0	Internal regulator supply	REG1VDD, REG1VSS
	Port supply	E1VDD, E1VSS
	Other	A0VSS, A0VREFP

3.3 Supply voltages

Table 3-2 VDD Data

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	I0VDD		V_{POC}[a]		5.5	V
	OSCVDD		V_{POC}[a]		5.5	V
	REG0VDD		V_{POC}[a]		5.5	V
	REG1VDD		V_{POC}[a]		5.5	V
Port supply voltages	E0VDD		V_{POC}[a]		5.5	V
	E1VDD		V_{POC}[a]		5.5	V
ADC supply voltages	A0VREFP	10-bit resolution	V_{POC}[a]		5.5	V

a) V_{POC}: POC detection voltage
For details on V_{POC}, see section 3.3.3, POC characteristics.

3.3.1 AWO Regulator characteristics

Table 3-3 AWO Regulator characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REG0VDD		V_{POC}[a]		5.5	V
Output voltage	V_{RO}		1.35	1.50	1.65	V
Capacitance of the REG0C pin	REG0C		2.31		6.11	µF
Voltage gradient	RAVS	0 to V_{POC}	0.5		150	V/ms

a) V_{POC}: POC detection voltage
For details on V_{POC}, see section 3.3.3, POC characteristics.

3.3.2 Iso0 Regulator characteristics

Table 3-4 Iso0 regulator characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGnVDD		V_{POC}[a]		5.5	V
Output voltage	V_{ROI}		1.35	1.50	1.65	V
Capacitance on REGnC	REG1C		70	100	130	nF
Voltage gradient	RIVS	0 to V_{POC}	0.18		1800	V/ms

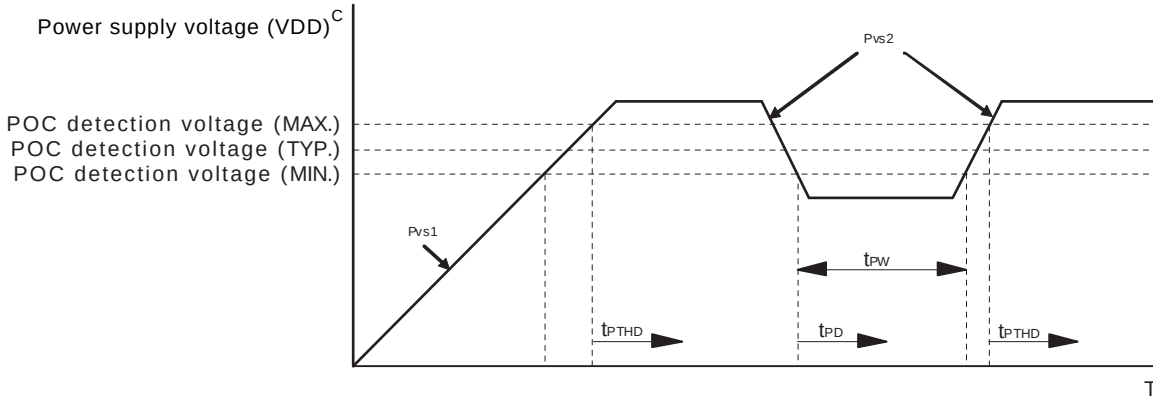
a) POC: POC detection voltage
For details on VPOC, see section 3.3.3, POC characteristics.

3.3.3 POC characteristics

Table 3-5 POC characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
POC detection voltage	V_{POC}		2.75	2.9	3.0	V
Voltage slope 1	P_{VS1}		0.18		1800	V/ms
Voltage slope 2	P_{VS2}		0.0018		1800	V/ms
Response time 1[a]	t_{PTHD}				2	ms
Response time 2[b]	t_{PD}				2	ms
VDD minimum width	t_{PW}		0.2			ms

a) This is the time until de-assertion of the reset signal (POCRES) after detection of the POC detection voltage.
b) This is the time until generation of the reset signal (POCRES) after detection of the POC detection voltage.
c) VDD: REG0VDD



3.4 Power-up/-down sequence of external supply voltages

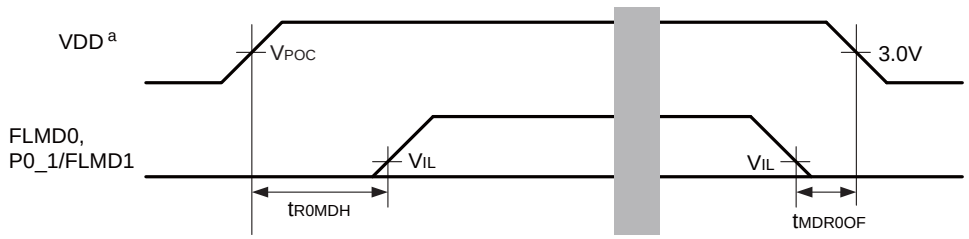
3.4.1 Condition 1

Table 3-6 $\overline{\text{RESET}}$ not used

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
VDD[a] (rise) to FLMD0, P0_1/FLMD1 (≤ V_{IL}) hold time	t_{R0MDH}		2			ms
FLMD0, P0_1/FLMD1 (≤ V_{IL}) to VDD[a] (fall) hold time	t_{MDR0OF}		0			ms

a) VDD: REGnVDD, I0VDD, OSCVDD, EnVDD, A0VREFP

Note n=0, 1



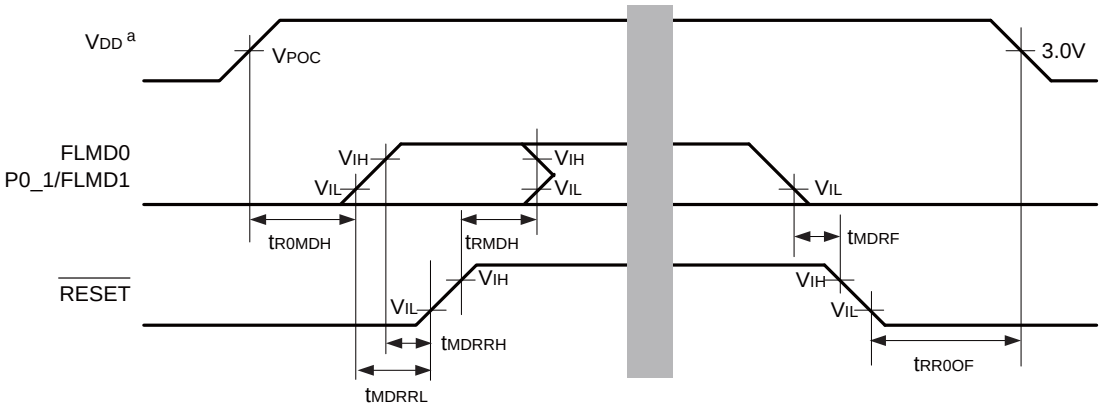
3.4.2 Condition 2

Table 3-7 $\overline{\text{RESET}}$ is used

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V_{DD}[a] (rise) to FLMD0, P0_1/FLMD1 (≤ V_{IL}) hold time	t_{R0MDH}		1			ms
V_{DD}[a] (rise) to $\overline{\text{RESET}}$ (≤ V_{IL}) hold time	t_{R0RR}[b]		2			ms
FLMD0, P0_1/FLMD1 (≥ V_{IH}) to $\overline{\text{RESET}}$ (≤ V_{IL}) setup time	t_{MDRRH}		1			ms
FLMD0, P0_1/FLMD1 (≤V_{IL}) to $\overline{\text{RESET}}$ (≤ V_{IL}) setup time	t_{MDRRL}		1			ms
$\overline{\text{RESET}}$ (≥ V_{IH}) to FLMD0,P0_1/FLMD1 (≥ V_{IH} ≥ V_{IL}) hold time	t_{RMDH}		1			ms
FLMD0,P0_1/FLMD1 (≤ V_{IL}) to $\overline{\text{RESET}}$ (≥ V_{IH}) setup time	t_{MDRF}		0			ms
$\overline{\text{RESET}}$ (≤ V_{IL}) to V_{DD}[a] (fall) hold time	t_{RR0OF}		0			ms

a) VDD: REGnVDD, I0VDD, OSCVDD, EnVDD, A0VREFP
b) Operation is not guaranteed if the value of t_{R0RR} is not fixed or the the $\overline{\text{RESET}}$ flag in the RESF register is not set up.

Note n = 0, 1



3.4.3 Condition 3

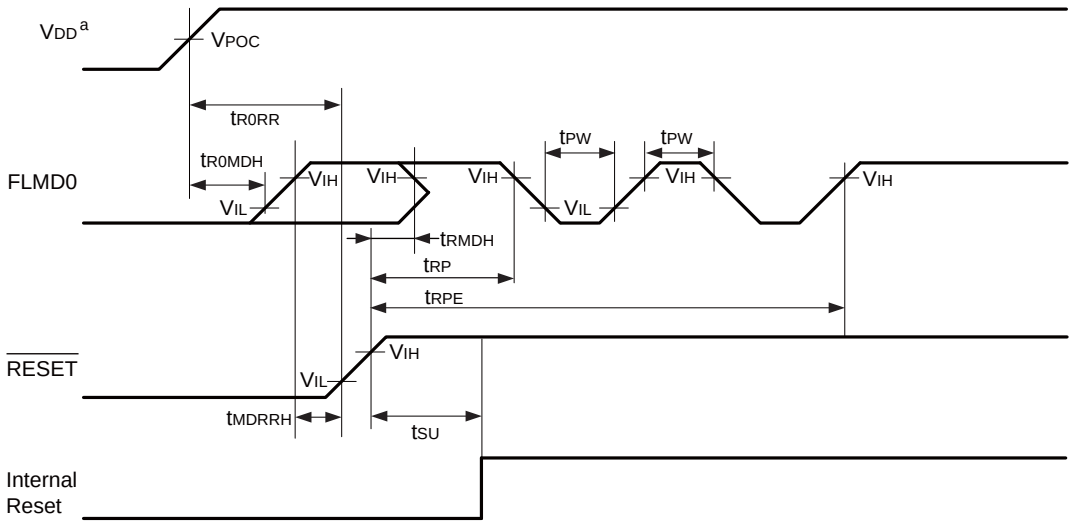
Table 3-8 $\overline{\text{RESET}}$ pin is used in serial programming mode

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V_{DD}[a] (rise) to FLMD0 (≤ V_{IL}) hold time	t_{R0MDH}		1			ms
V_{DD}[a] (rise) to $\overline{\text{RESET}}$ (≤ V_{IL}) hold time	t_{R0RR}[b]		2			ms
$\overline{\text{RESET}}$ (≥ V_{IH}) to FLMD0 (≥ V_{IH}) hold time	t_{RMDH}		1			ms
FLMD0 (≥ V_{IH}) to $\overline{\text{RESET}}$ (≤ V_{IL}) setup time	t_{MDRRH}		1			ms
CPU startup time ($\overline{\text{RESET}}$ (≥ V_{IH}) to Internal reset delay time)	t_{SU}				2.5	ms
$\overline{\text{RESET}}$ (≥ V_{IH}) to FLMD0 pulse input start time	t_{RP}		t_{SU}(max)+ 0.73			ms
$\overline{\text{RESET}}$ (≥ V_{IH}) to FLMD0 pulse input end time	t_{RPE}		0		t_{SU}(max)+10	ms
FLMD0 low/high level width	t_{PW}		0.8			µs

a) VDD: REGnVDD, I0VDD, OSCVDD, EnVDD, A0VREFP

b) Operation is not guaranteed if the value of t_{R0RR} is not fixed or the the $\overline{\text{RESET}}$ flag in the RESF register is not set up.

Note n = 0, 1



Section 4 Clock generator

Refer to section 3.3 Supply vlotages for the condition of Supply voltages.

4.1 CPU clock frequency

Table 4-1 CPU clock frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPU}				64	MHz

4.2 Peripheral clock

Table 4-2 Peripheral clock frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Peripheral clock frequency	f_{PERI}				48[a]	MHz

a) Maximum peripheral clock frequency is different in some macros. Refer to the chapter ‘Clock Selection’ in the UM for details.

4.3 Oscillator characteristics

4.3.1 Main oscillator (MainOsc) characteristics

Table 4-3 Main oscillator (MainOsc) characteristics

Parameter	Symbol	Condition	Ratings	Unit
Main oscillator (MainOsc) clock frequency	f_{MOSC}	Crystal / Ceramic	4, 5, 6, 8, 10, 12, 16, 20	MHz

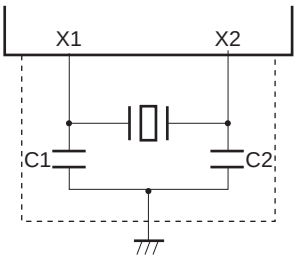


Figure 4-1 Recommended Main Oscillator Circuit (MainOsc)

Cautions

1. External clock input is prohibited.
2. General guidance for PCB layout:
   - Keep the wiring length as short as possible.
   - Do not cross the wiring with other signal lines.
   - Do not route this circuit close to a signal line with high fluctuating current flow.
   - Always make the ground point of the oscillator capacitor the same potential as REG0VSS and OSCVSS.
   - Do not ground the capacitor to a ground pattern with high current flow.
   - Do not tap signals from the oscillator.
3. The values for C1 and C2 depend on the ceramic resonator or crystal oscillator, so choose the values on the basis of discussions with the manufacturer of the resonator or oscillator.

4.3.2 Internal oscillator characteristics

Table 4-4 Internal oscillator characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low speed OSC frequency	f_{RL}	• Other than DEEPSTOP mode • DEEPSTOP mode with PSC0.REGSTP = 0	220.8	240	259.2	kHz
	f_{RLLP}	• DEEPSTOP mode with PSC0.REGSTP = 1	172.0	240	268.0	kHz
High speed OSC frequency	f_{RH}	• Other than DEEPSTOP mode • DEEPSTOP mode, and PSC0.PSC0REGSTP is not set to 1	7.2	8.0	8.8	MHz
		• Other than DEEPSTOP mode • DEEPSTOP mode, and PSC0.PSC0REGSTP is not set to 1 • ACT13M	8.558		17.41	MHz
	f_{RHLP}	• DEEPSTOP mode with PSC0.PSC0REGSTP = 1	5.3	8.0	9.0	MHz
		• DEEPSTOP mode, and PSC0.PSC0REGSTP is not set to 1 • ACT13M	2.534		6.385	MHz

4.4 PLL Characteristics

Table 4-5 PLL characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output frequency[a]	f_{XXn}		20		64	MHz
Lock time	t_{LCKPn}				50	µs
Period jitter	t_{PEJTn}				160	ps
Long term jitter	t_{LTJTn}				2.5	ns

a) Values for the frequency of output from the PLL do not take jitter times and long-term jitter times in the clock from the main oscillator or the PLL into account.

Section 5 I/O specification

Refer to section 3.3 Supply vlotages for the condition of Supply voltages.

5.1 Port Characteristics

5.1.1 PgE0

Table 5-1 PgE0

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}	Schmitt1 (SHMT1)	0.7 E0VDD		E0VDD + 0.3	V
		Schmitt2 (SHMT2)	0.8 E0VDD		E0VDD + 0.3	V
		Schmitt4 (SHMT4) (E0VDD = V_{POC} to 3.0 V)	0.84 E0VDD		E0VDD + 0.3	V
		Schmitt4 (SHMT4) (E0VDD = 3.0 to 5.5 V)	0.8 E0VDD		E0VDD + 0.3	V
Low level input voltage	V_{IL}	Schmitt1 (SHMT1)	-0.3		0.3 E0VDD	V
		Schmitt2 (SHMT2)	-0.3		0.2 E0VDD	V
		Schmitt4 (SHMT4) (E0VDD = V_{POC} to 3.4 V)	-0.3		0.4 E0VDD	V
		Schmitt4 (SHMT4) (E0VDD = 3.4 to 5.5 V)	-0.3		0.5 E0VDD	V
High level output voltage	V_{OH}	I_{OH} = -3 mA[a]	E0VDD - 1.0			V
		I_{OH} = -100 µA	E0VDD - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 3 mA[a]			0.4	V
		I_{OL} = 100 µA			0.4	V
Input hysteresis of Schmitt	V_H	Schmitt1 (SHMT1)	0.3			V
		Schmitt2 (SHMT2)	0.3			V
		Schmitt4 (SHMT4)	0.1			V
Internal pull-up resistor	R_U		15	40	150	kΩ
Internal pull-down resistor	R_D		15	40	150	kΩ
High level input leakage current	I_{LIH}	V_I = E0VDD			0.5	µA
Low level input leakage current	I_{LIL}	V_I = 0 V			-0.5	µA
High level output leakage current	I_{LOH}	V_O = E0VDD			0.5	µA
Low level output leakage current	I_{LOL}	V_O = 0 V			-0.5	µA
Output frequency	f_O				20	MHz
Rise time (output)	t_{KRP}				15	ns
Fall time (output)	t_{KFP}				15	ns

a) As the values for the total current from PgE0 and PgE1, refer to section 2.3 Port current.

5.1.2 PgE1

Table 5-2 PgE1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}					V
		Schmitt1 (SHMT1)	0.7 E1VDD		E1VDD + 0.3	V
		Schmitt4 (SHMT4) (E1VDD = V_{POC} to 3.0 V)	0.84 E1VDD		E1VDD + 0.3	V
		Schmitt4 (SHMT4) (E1VDD = 3.0 to 5.5 V)	0.8 E1VDD		E1VDD + 0.3	V
Low level input voltage	V_{IL}					V
		Schmitt1 (SHMT1)	-0.3		0.3 E1VDD	V
		Schmitt4 (SHMT4) (E1VDD = V_{POC} to 3.4 V)	-0.3		0.4 E1VDD	V
		Schmitt4 (SHMT4) (E1VDD = 3.4 to 5.5 V)	-0.3		0.5 E1VDD	V
High level output voltage	V_{OH}	I_{OH} = -3 mA[a]	E1VDD - 1.0			V
		I_{OH} = -100 µA	E1VDD - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 3 mA[a]			0.4	V
		I_{OL} = 100 µA			0.4	V
Input hysteresis of Schmitt	V_H	Schmitt1 (SHMT1)	0.3			V
		Schmitt4 (SHMT4)	0.1			V
Internal pull-up resistor	R_U		15	40	150	kΩ
Internal pull-down resistor	R_D		15	40	150	kΩ
High level input leakage current	I_{LIH}	V_I = E1VDD			0.5	µA
Low level input leakage current	I_{LIL}	V_I = 0 V			-0.5	µA
High level output leakage current	I_{LOH}	V_O = E1VDD			0.5	µA
Low level output leakage current	I_{LOL}	V_O = 0 V			-0.5	µA
Output frequency	f_O				20	MHz
Rise time (output)	t_{KRP}				15	ns
Fall time (output)	t_{KFP}				15	ns

a) As the values for the total current from PgE0 and PgE1, refer to section 2.3 Port current.

5.1.3 PgA0

Table 5-3 PgA0

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}	CMOS1	0.7 A0VREFP		A0VREFP + 0.3	V
Low level input voltage	V_{IL}	CMOS1	-0.3		0.3 A0VREFP	V
High level output voltage	V_{OH}	I_{OH} = -1 mA[a]	A0VREFP - 1.0			V
		I_{OH} = -100 µA	A0VREFP - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1 mA[a]			0.4	V
		I_{OL} = 100 µA			0.4	V
High level input leakage current	I_{LIH}	V_I = A0VREFP			0.5	µA
Low level input leakage current	I_{LIL}	V_I = 0 V			-0.5	µA
High level output leakage current	I_{LOH}	V_O = A0VREFP			0.5	µA
Low level output leakage current	I_{LOL}	V_O = 0 V			-0.5	µA
Output frequency	f_O				20	MHz
Rise time (output)	t_{KRP}				15.5	ns
Fall time (output)	t_{KFP}				15.5	ns

a) As the values for the total current from PgA0, do not allow V_{OH} to go below -20 mA or V_{OL} to rise above 20mA.

Section 6 Supply current specification

Item	Power[a]	Condition						Object Product	Specification value				Unit
	ISO0	Main OSC	High-speed IntOsc	Low-speed IntOsc	PLL	CPU frequency [HHz]	Peripheral function		Typ.	Max. (A)	Max. (A1)	Max. (A2)	
RUN mode	ON	RUN	RUN	RUN	RUN	64	RUN (32MHz)	µPD70F4177	19	31	34	37	mA
	ON	RUN	RUN	RUN	RUN	64	RUN (32MHz)	µPD70F4178	19	31	34	37	mA
	ON	RUN	RUN	RUN	RUN	48	RUN (48MHz)	µPD70F4177	18	30	33	36	mA
	ON	RUN	RUN	RUN	RUN	48	RUN (48MHz)	µPD70F4178	18	30	33	36	mA
	ON	STOP	RUN	RUN	STOP	8	RUN (8MHz)	µPD70F4177	6	18	20	22	mA
	ON	STOP	RUN	RUN	STOP	8	RUN (8MHz)	µPD70F4178	6	18	20	22	mA
RUN mode (EEPROM emulation)	ON	RUN	RUN	RUN	RUN	64	RUN (32MHz)	µPD70F4177	36	59	62	65	mA
	ON	RUN	RUN	RUN	RUN	64	RUN (32MHz)	µPD70F4178	36	59	62	65	mA
	ON	RUN	RUN	RUN	RUN	48	RUN (48MHz)	µPD70F4177	35	58	61	64	mA
	ON	RUN	RUN	RUN	RUN	48	RUN (48MHz)	µPD70F4178	35	58	61	64	mA
STOP mode	ON	STOP	STOP	STOP	STOP	STOP	STOP	µPD70F4177	1.5	13	15	18	mA
	ON	STOP	STOP	STOP	STOP	STOP	STOP	µPD70F4178	1.5	13	15	18	mA
DEEPSTOP mode (PSC0.REGSTP=1)	OFF	STOP	STOP	RUN	STOP	STOP	STOP	µPD70F4177	0.025	0.220	0.250	0.300	mA
	OFF	STOP	STOP	RUN	STOP	STOP	STOP	µPD70F4178	0.025	0.220	0.250	0.300	mA

a) AWO is always ON.

Note 1. "ON" indicates the state where the power supplies are on.
"OFF" indicates the state where the power supplies are off.

Note 2. The above table does not include currents of port buffers and A/D converter.

Note 3. Typ. values are reference data.

Note 4. Running emulation values are reference data.

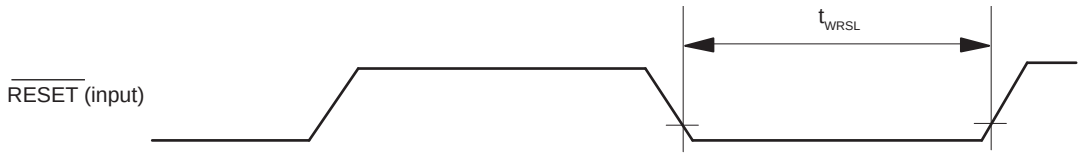
Section 7Peripherals specification

Refer to section 3.3 Supply vlotages for the condition of Supply voltages.

7.1 Reset timing

Table 7-1 Reset timing

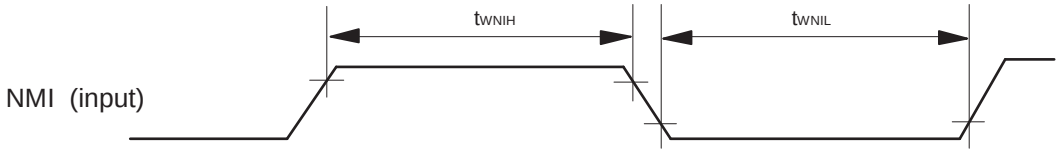
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}	Except power on	450			ns



7.2 NMI timing

Table 7-2 NMI timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}		300			ns
NMI input low level width	t_{WNIL}		300			ns

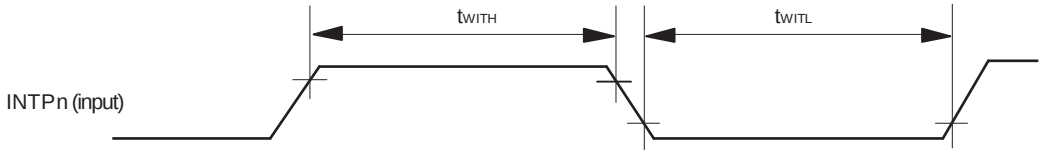


7.3 INTP timing

Table 7-3 INTP timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
INTPn input high level width	t_{WITH}		300			ns
INTPn input low level width	t_{WITL}		300			ns

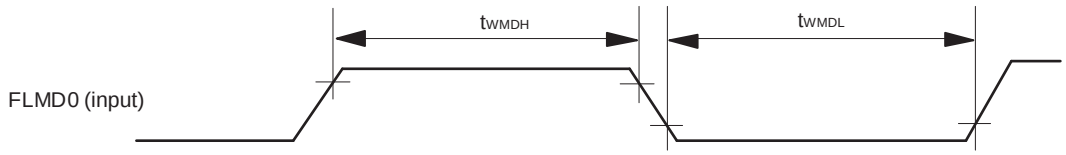
Note n = 0-4,6,8,11,12



7.4 FLMD0 timing

Table 7-4 FLMD0 timing

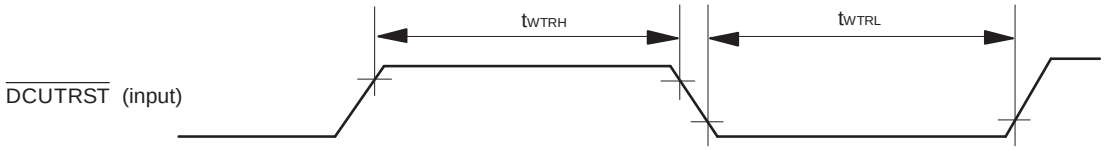
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 input high level width	t_{WMDH}		300			ns
FLMD0 input low level width	t_{WMDL}		300			ns



7.5 $\overline{\text{DCUTRST}}$ timing

Table 7-5 $\overline{\text{DCUTRST}}$ timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{DCUTRST}}$ input high level width	t_{WTRH}		450			ns
$\overline{\text{DCUTRST}}$ input low level width	t_{WTRL}		450			ns

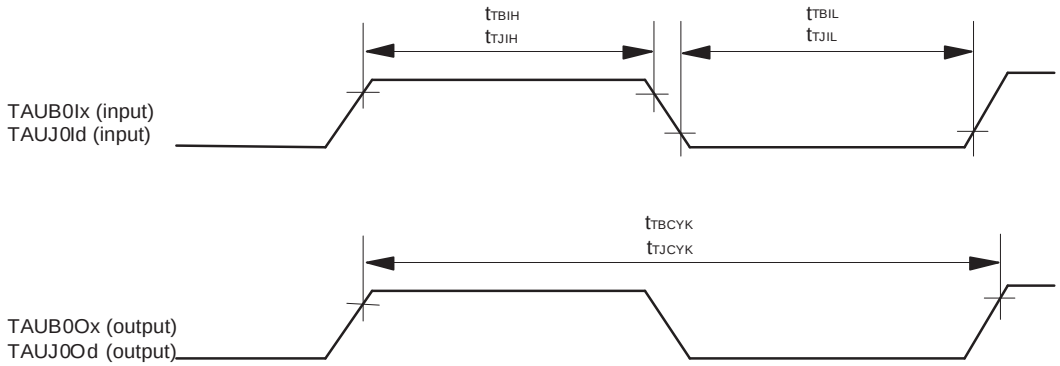


7.6 Timer timing

Table 7-6 Timer timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUB0Ix input high level width	t_{TBIH}	x = 1-11,13-15	a			ns
TAUB0Ix input low level width	t_{TBIL}	x = 1-11,13-15	a			ns
TAUJ0Id input high level width	t_{TJIH}	d=0-3	300			ns
TAUJ0Id input low level width	t_{TJIL}	d=0-3	300			ns
TAUB0Ox output cycle	t_{TBCYK}	x = 1-11,13-15			20	MHz
TAUJ0Od output cycle	t_{TJCYK}	d=0-3			20	MHz

a) This is one from among $2T_{SAMP}$ + 20, $3T_{SAMP}$ + 20, $4T_{SAMP}$ + 20, and $5T_{SAMP}$ + 20.
T_{SAMP} is the period of the sampling clock for the noise canceller.



7.7 CSI timing

7.7.1 CSIG timing (Master mode)

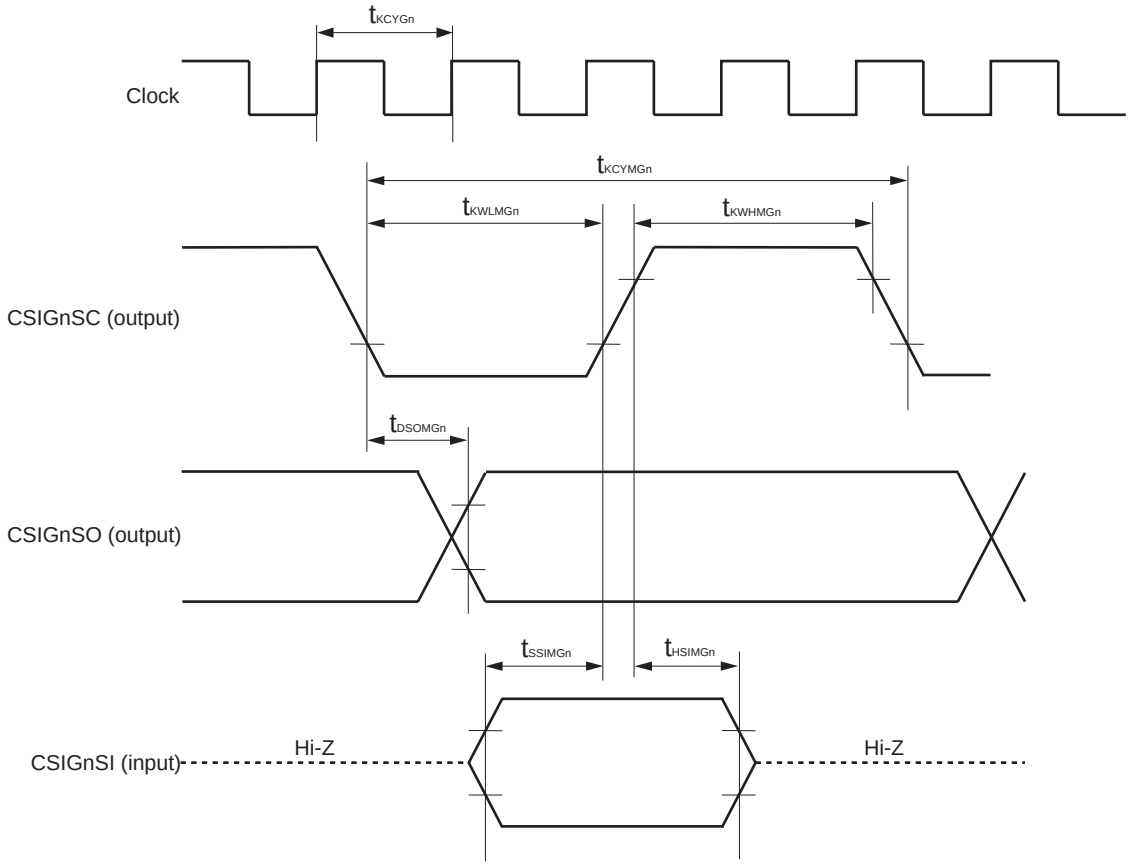
Table 7-7 CSIG timing (Master mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYGn}		20.83			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		$0.5t_{KCYMGn}$ - 10			ns
CSIGnSC low level width	t_{KWLMGn}		$0.5t_{KCYMGn}$ - 10			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSC to CSIGnSO output delay time	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT bit = 0 or 1, CSIGnCTL1.CSIGnHSE bit = 1	$2t_{KCYGn}$ + 25			ns
CSIGnRYI high level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE bit = 1	t_{KCYGn} - 5.0			ns

Note n = 0, 4

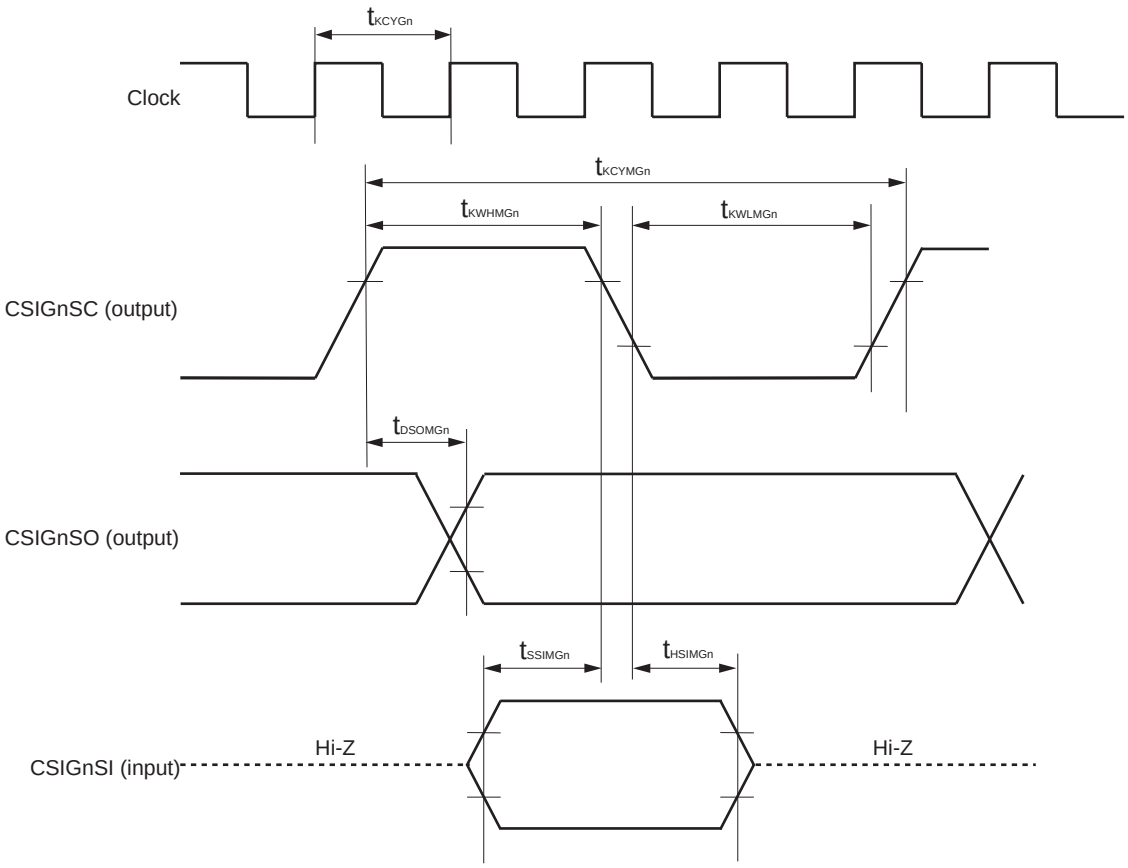
(1) CSIGnSC, CSIGnSO, CSIGnSI pin (master mode)

- CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 0 or
  CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 1



n=0,4

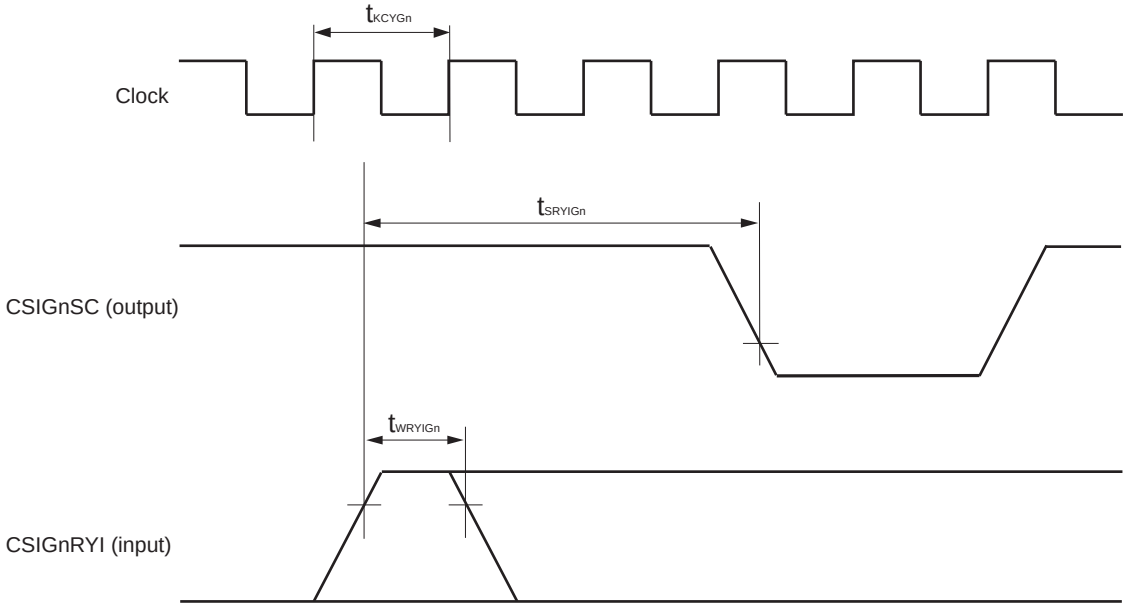
- CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 1 or
  CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 0



n=0,4

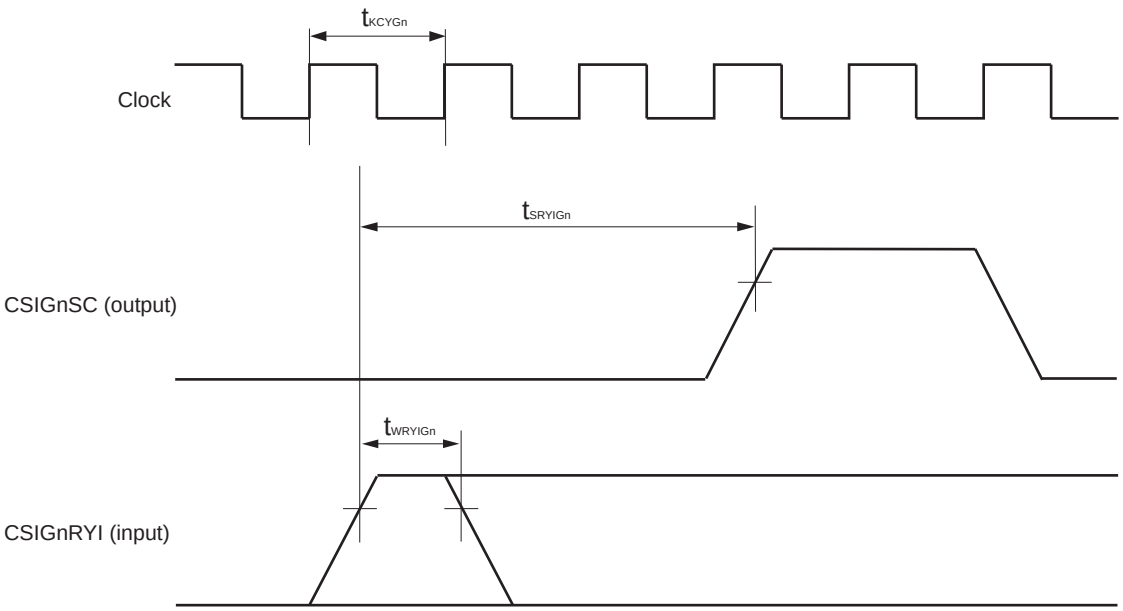
(2) CSIGnRYI pin (master mode)

- CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCTL1.CSIGnSIT bit = 0, CSIGnCTL1.CSIGnHSE bit = 1



n=0,4

- CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCTL1.CSIGnSIT bit = 0, CSIGnCTL1.CSIGnHSE bit = 1



n=0,4

7.7.2 CSIG timing (slave mode)

Table 7-8 CSIG timing (slave mode)

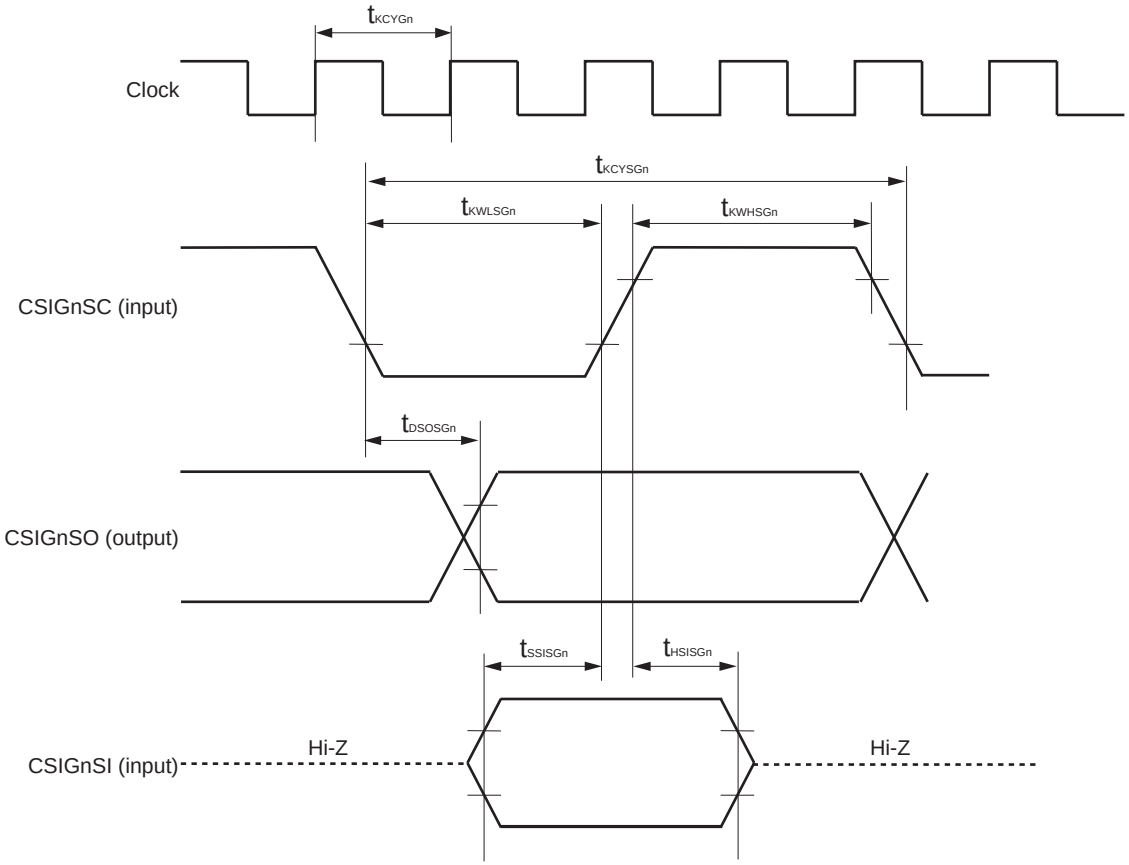
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYGn}		20.83			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		$0.5t_{KCYSGn}$ - 10			ns
CSIGnSC low level width	t_{KWLSGn}		$0.5t_{KCYSGn}$ - 10			ns
CSIGnSI setup time (vs CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs CSIGnSC)	t_{HSISGn}		t_{KCYGn} + 5.0			ns
CSIGnSC to CSIGnSO output delay time	t_{DSOSGn}				35	ns
CSIGnRYO output delay time[a]	t_{SRYOGn}				35	ns
$\overline{\text{CSIGnSSI}}$ setup time (vs CSIGnSC)	$t_{SSSISGn}$		$0.5t_{KCYSGn}$ - 5.0			ns
$\overline{\text{CSIGnSSI}}$ hold time (vs CSIGnSCI)	$t_{HSSISGn}$		t_{KCYSGn} + 5.0			ns

a) Since there is no output mode for CSIG4RYO, the output delay time for CSIG4RYO is not supported.

Note n = 0, 4

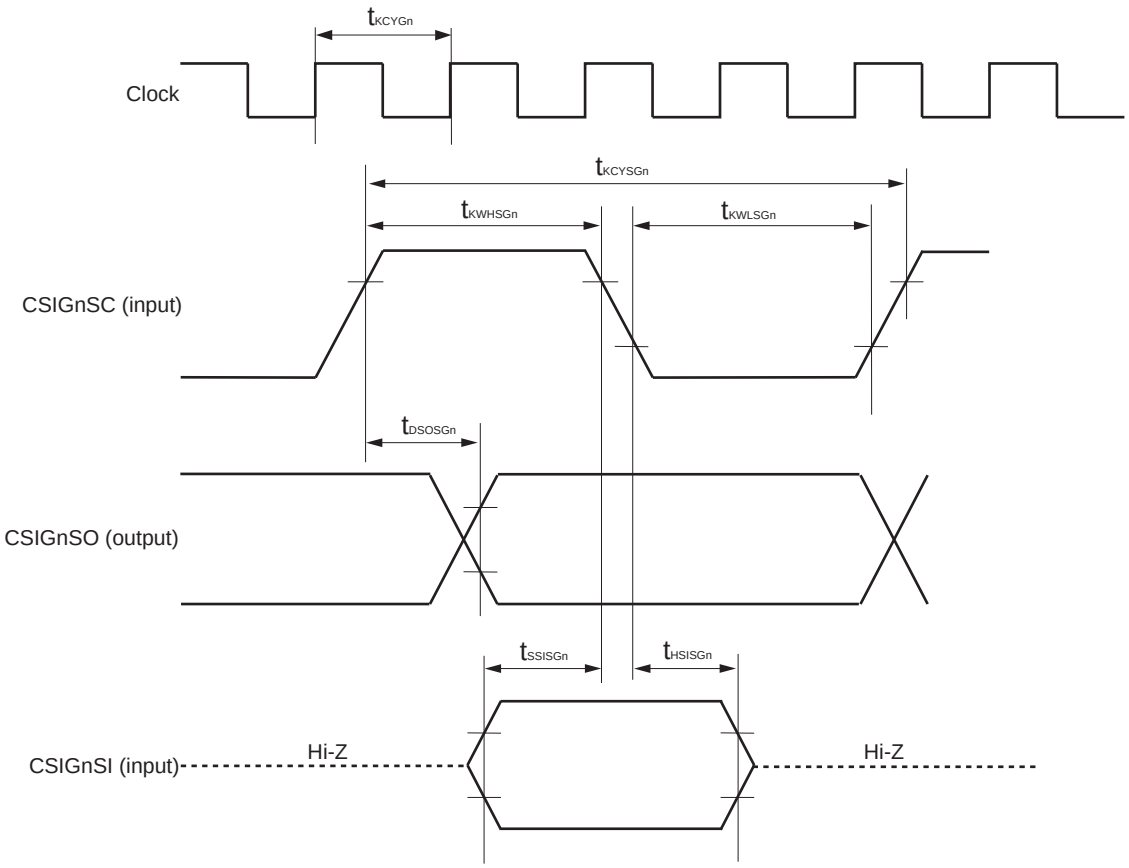
(1) CSIGnSC, CSIGnSO, CSIGnSI pin (slave mode)

- CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 0 or
  CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 1



n = 0,4

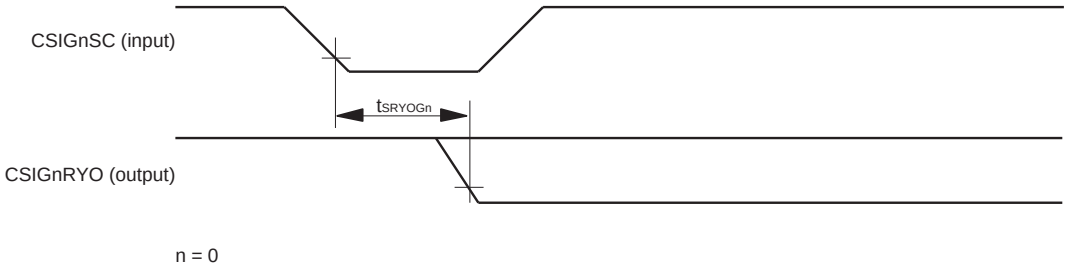
- CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 1 or
  CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 0



n = 0,4

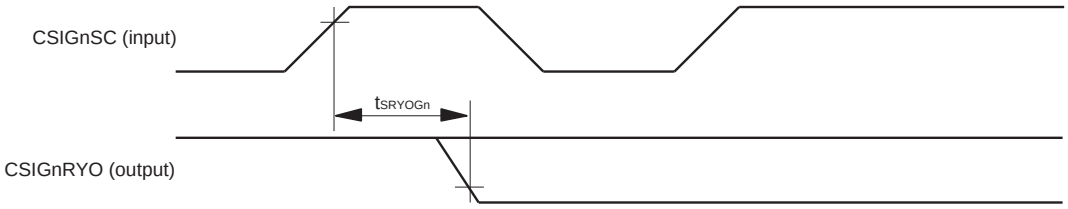
(2) CSIGnRYO pin (slave mode)

- CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 0



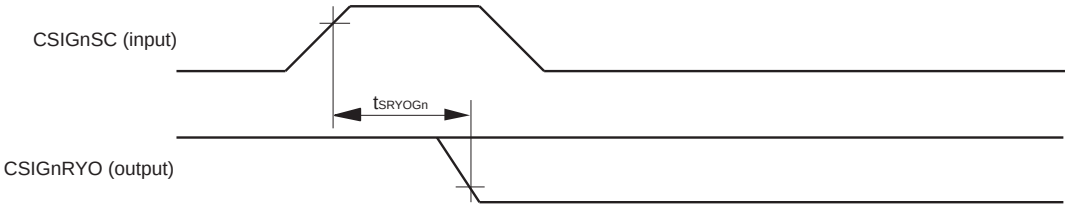
n = 0

- CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 1



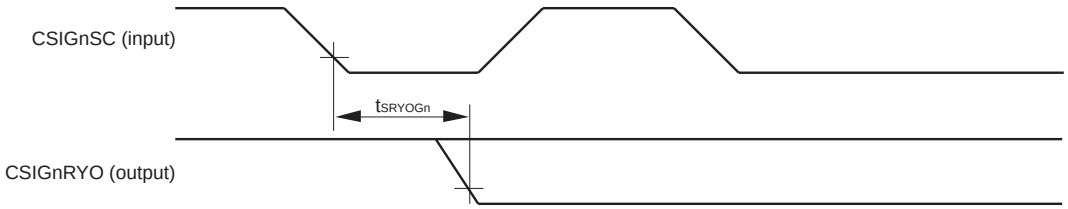
n = 0

- CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 1



n = 0

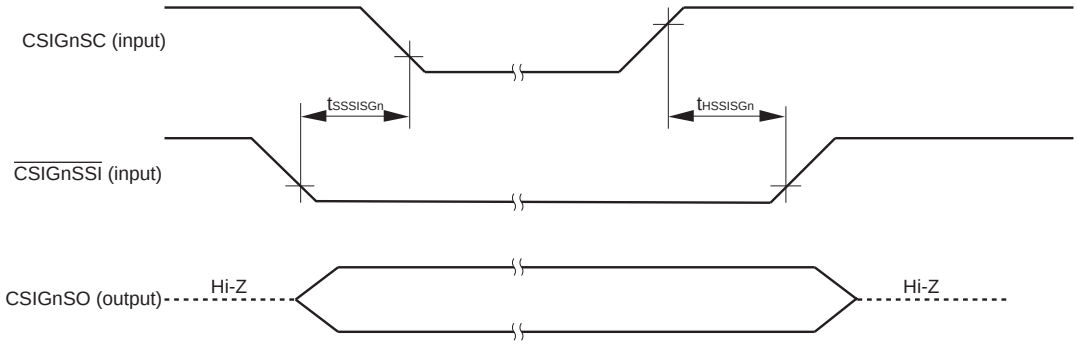
- CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 1



n = 0

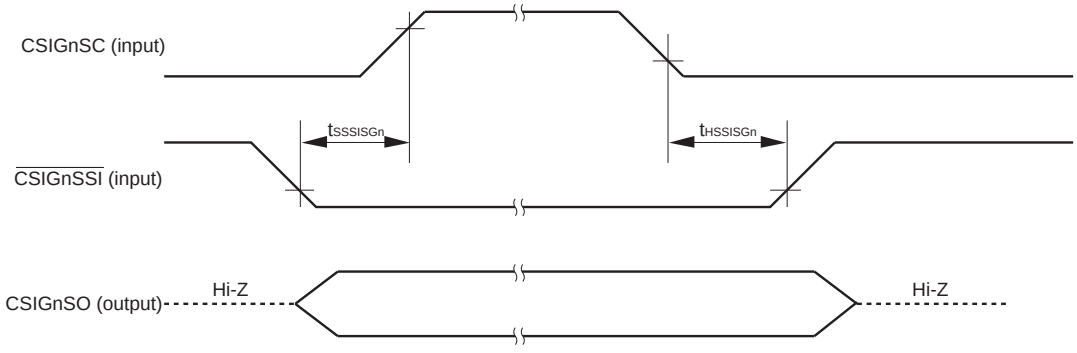
(3) $\overline{\text{CSIGnSSI}}$ pin (slave mode)

- CSIGnCTL1.CSIGnSSE bit =1,
  CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 0 or
  CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 1



n = 0,4

- CSIGnCTL1.CSIGnSSE bit =1,
  CSIGnCTL1.CSIGnCKR bit = 0, CSIGnCFG0.CSIGnDAP bit = 1 or
  CSIGnCTL1.CSIGnCKR bit = 1, CSIGnCFG0.CSIGnDAP bit = 0



n = 0,4

7.8 UARTE timing

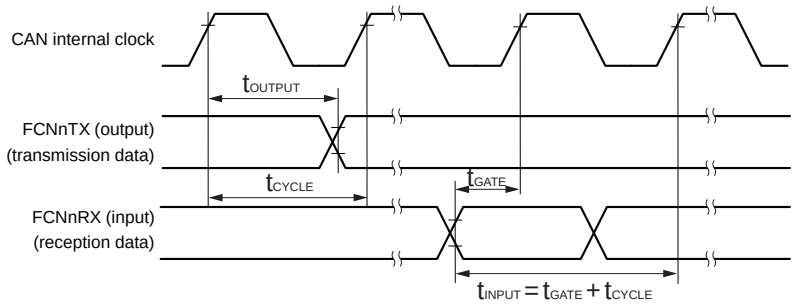
Table 7-9 UARTE timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps

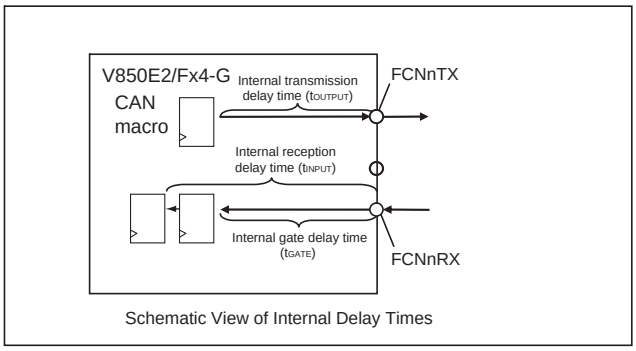
7.9 CAN (FCN) timing

Table 7-10 CAN (FCN) timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time	t_{INTDEL}				37.5	ns
CAN node delay time	t_{NODE}	t_{CYCLE} = 62.5 ns			100	ns



CAN node delay time (t_{NODE}) = Internal transmission delay time (t_{OUTPUT}) + Internal reception delay time (t_{INPUT})
Internal delay time (t_{INTDEL}) = Internal gate delay time (t_{GATE}) + Internal transmission delay time (t_{OUTPUT})



Schematic View of Internal Delay Times

Note µPD70F4178 (512 K): n = 0 to 5, µPD70F4177 (256 K): n = 0 to 2

7.10 I^2C timing

Table 7-11 Normal mode

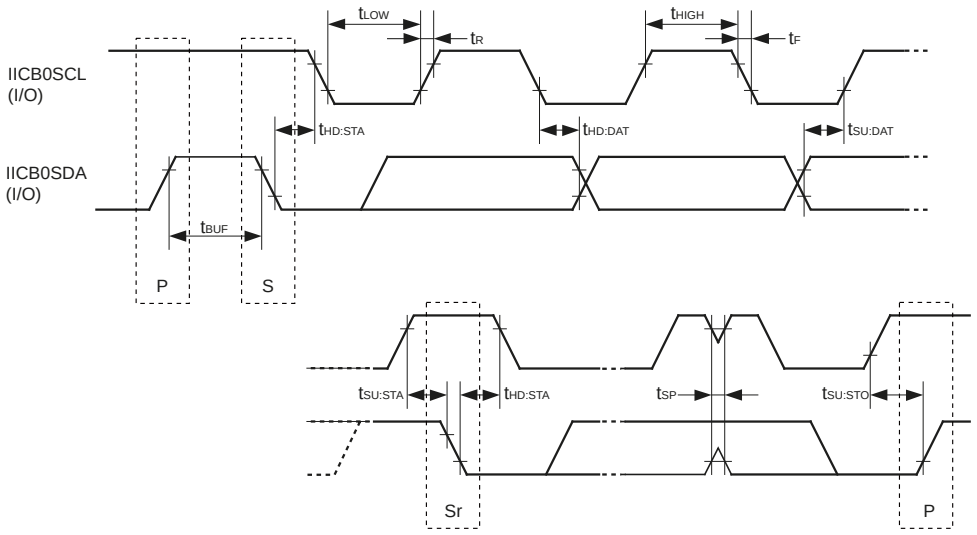
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
IICB0SCL clock frequency	f_{CLK}		0		100	kHz
Bus free time (between stop condition and start condition)	t_{BUF}		4.7			µs
Start/Restart hold time[a]	$t_{HD:STA}$		4			µs
IICB0SCL clock low state hold time	t_{LOW}		4.7			µs
IICB0SCL clock high state hold time	t_{HIGH}		4			µs
Setup time for start/restart condition	$t_{SU:STA}$		4.7			µs
Data hold time	$t_{HD:DAT}$	CBUS compatible	5			µs
		I^2C mode	0			µs
Data setup time	$t_{SU:DAT}$		250			ns
Rising time for IICB0SDA or IICB0SCL	t_R				1000	ns
Falling time for IICB0SDA or IICB0SCL	t_F				300	ns
Setup time of stop condition	$t_{SU:STO}$		4			µs
Capacitive load of all bus lines	C_b				400	pF

a) At the time of a start condition, the first clock pulse is generated after the hold time.

Table 7-12 Fast mode

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
IICB0SCL clock frequency	f_{CLK}		0		400	kHz
Bus free time (between stop condition and start condition)	t_{BUF}		1.3			μs
Start/Restart hold time[a]	$t_{HD:STA}$		0.6			μs
IICB0SCL clock low state hold time	t_{LOW}		1.3			μs
IICB0SCL clock high state hold time	t_{HIGH}		0.6			μs
Setup time for start/restart condition	$t_{SU:STA}$		0.6			μs
Data hold time	$t_{HD:DAT}$	I^2C mode	0		0.9	μs
Data setup time	$t_{SU:DAT}$		100			ns
Rising time for IICB0SDA or IICB0SCL	t_R		20 + 0.1C_b		300	ns
Falling time for IICB0SDA or IICB0SCL	t_F		20 + 0.1C_b		300	ns
Setup time of stop condition	$t_{SU:STO}$		0.6			μs
Pulse width of spikes that can be suppressed by the internal filters	t_{SP}		0		50	ns
Capacitive load of all bus lines	C_b				400	pF

a) At the time of a start condition, the first clock pulse is generated after the hold time.



Note 1. P: Stop condition

Note 2. S: Start condition

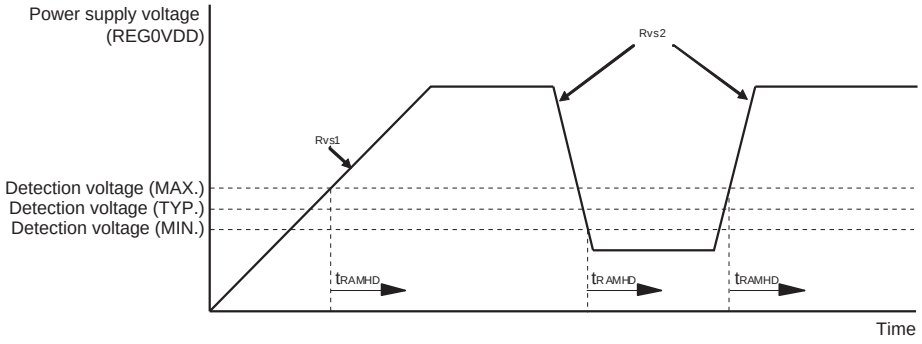
Note 3. Sr: Restart condition

7.11 RAM retention flag characteristics

Table 7-13 RAM retention flag characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{RAMHF}		1.75	1.9	2.0	V
Voltage slope 1	R_{vs1}		0.18		1800.0	V/ms
Voltage slope 2	R_{vs2}		0.0018		1800.0	V/ms
Response time[a]	t_{RAMHD}				2	ms

a) This is the time until setting of the VLVF.VLVF bit after detection of the detection voltage.

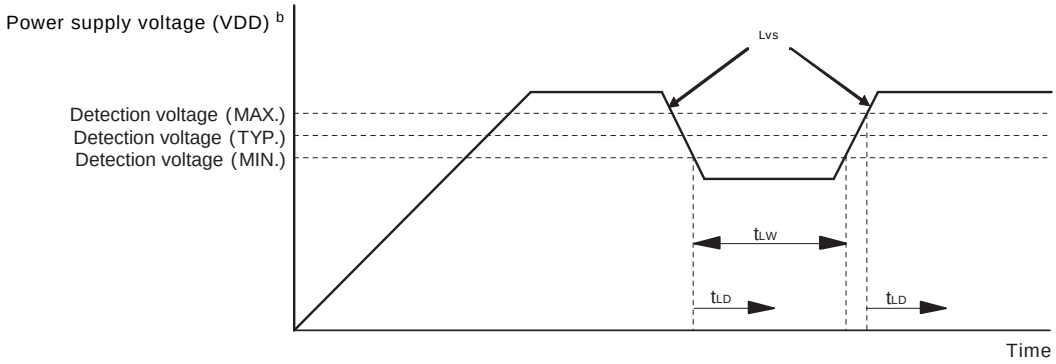


7.12 LVI characteristics

Table 7-14 LVI characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LVI detection voltage	V_{LVI0}	LVICNT.LVICNT[2:0]=001B	3.9	4.0	4.1	V
	V_{LVI1}	LVICNT.LVICNT[2:0]=010B	3.6	3.7	3.8	V
	V_{LVI2}	LVICNT.LVICNT[2:0]=011B	3.4	3.5	3.6	V
Voltage slope	L_{VS}		0.18		1800	V/ms
Response time[a]	t_{LD}				2.0	ms
REG0VDD minimum width	t_{LW}		2			ms

a) This is the time until generation of the interrupt request signal after detection of the detection voltage.
b) VDD : REG0VDD



7.13 A/D Converter characteristics

7.13.1 10-Bit Resolution A/D: ADCA0lm

Table 7-15 10-Bit Resolution A/D: ADCA0lm

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES0}		10	10	10	bit
Conversion time	T_{CON0}		2		10	µs
Overall error[b,c]	TOE0				±3.5	LSB
Non-liniarity error[c]	ILE0				±4.0	LSB
Differencial liniarity error[c]	DLE0				±1.0	LSB
Zero scale error[c]	ZSE0				±3.5	LSB
Full scale error[c]	FSE0				±3.5	LSB
Analog input voltage	V_{AIN0}		A0VSS		A0VREFP	V
Recovery time from power down				110	520	ns
A0VREFP	AI_{DD0}				4	mA
Conversion error by Diagnosis function					± 20[d]	LSB

[a] "Power down" indicates the ADCA0CTL1.ADCA0GPS bit being 0 or the chip being in STOP mode.
[b] This excludes the quantization error (± 0.5 LSB).
[c] This does not include sampling errors introduced by an external resistor and external capacitor.
[d] Conversion error by Diagnosis function may become change after evaluation.

Note m = 3 to 12

7.13.2 Equivalent Circuit of Analog Input Unit (Reference Value)

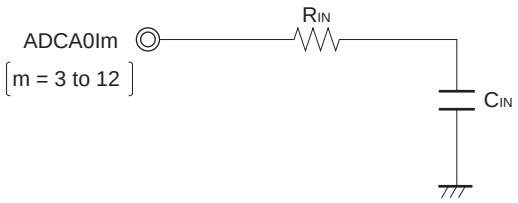


Table 7-16 Equivalent Circuit (Reference Value)

Pin	Condition	RIN (kW)	CIN (pF)
ADCA0Im		1.2	11.9

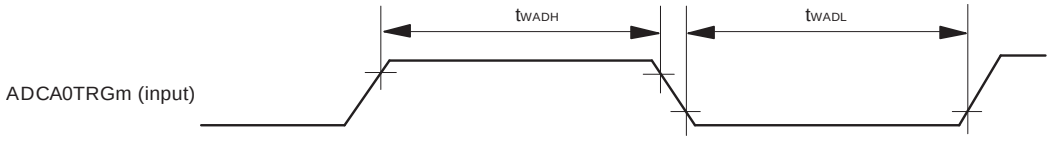
Note The above value is the maximum value for reference (m = 3 to 12).

7.13.3 ADCA0TRGm timing

Table 7-17 ADCA0TRGm timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCA0TRGm input high level width	tWADH		300			ns
ADCA0TRGm input low level width	tWADL		300			ns

Note m = 0 to 2

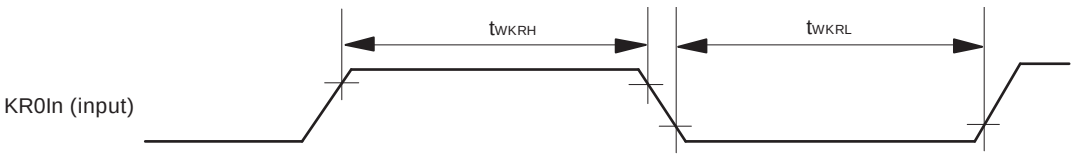


7.14 Key return timing

Table 7-18 Key return timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input high level width	tWKRH		300			ns
KR0In input low level width	tWKRL		300			ns

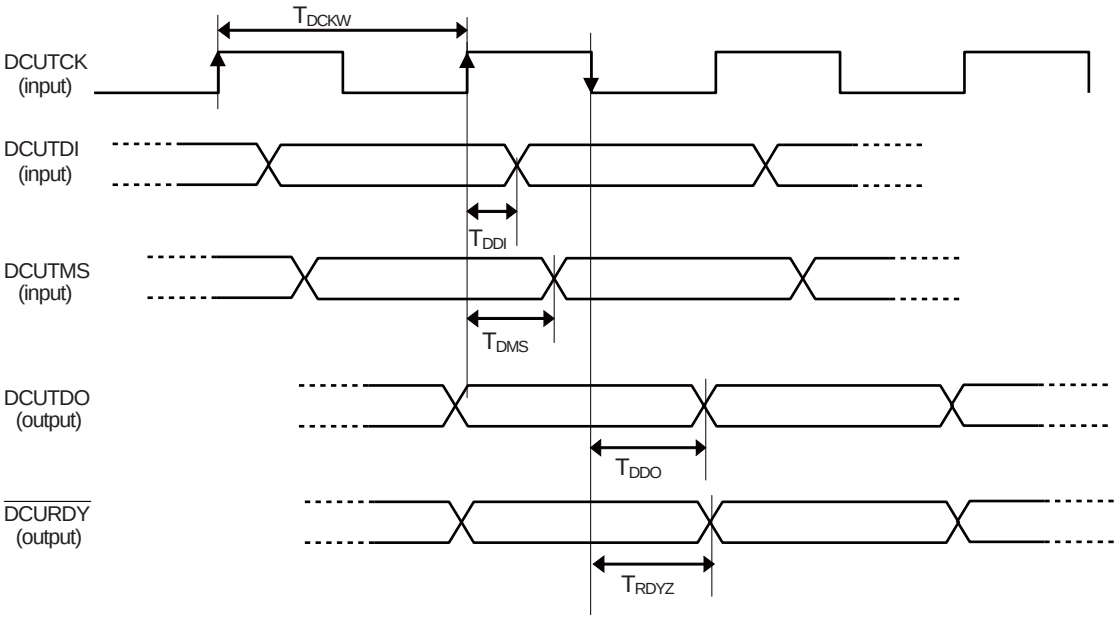
Note n = 0 to 7



7.15 Nexus debugging interface

Table 7-19 JTAG interface (T_A = 0°C to 40°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	T_{DCKW}		50			ns
DCUTDI delay time (↑DCUTCK)	T_{DDI}		3		10	ns
DCUTMS delay time (↑DCUTCK)	T_{DMS}		3		10	ns
DCUTDO delay time (↓DCUTCK)	T_{DDO}		0		25	ns
$\overline{\text{DCURDY}}$ delay time (↓DCUTCK)	T_{RDYZ}		0		25	ns



Section 8 Memory specification

8.1 Code flash specification

Table 8-1 Code flash specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Number of re-writes[a]	C_{WRT}	Data retention 20 years			1000	times
Programming temperature	t_{PRG}	(A) grade products	-40		85	°C
		(A1) grade products	-40		110	°C
		(A2) grade products	-40		125	°C

a) Please contact RENESAS sales office regarding specification other than the above.

Caution Note that for a product as shipped, either erasure followed by programming or programming only counts as one round of programming.
Example (P: programming, E: erasure)
The sequence product shipment → ― → P → E → P → E → P
is considered as reprogramming three times.
The sequence product shipment → E → P → E → P → E → P is considered as reprogramming three times.

8.2 Data flash specification

Table 8-2 Data flash specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Number of re-writes	D_{WRT1}	Data retention 20 years			100000	times
Programming temperature	t_{PRG}	(A) grade products	-40		85	°C
		(A1) grade products	-40		110	°C
		(A2) grade products	-40		125	°C

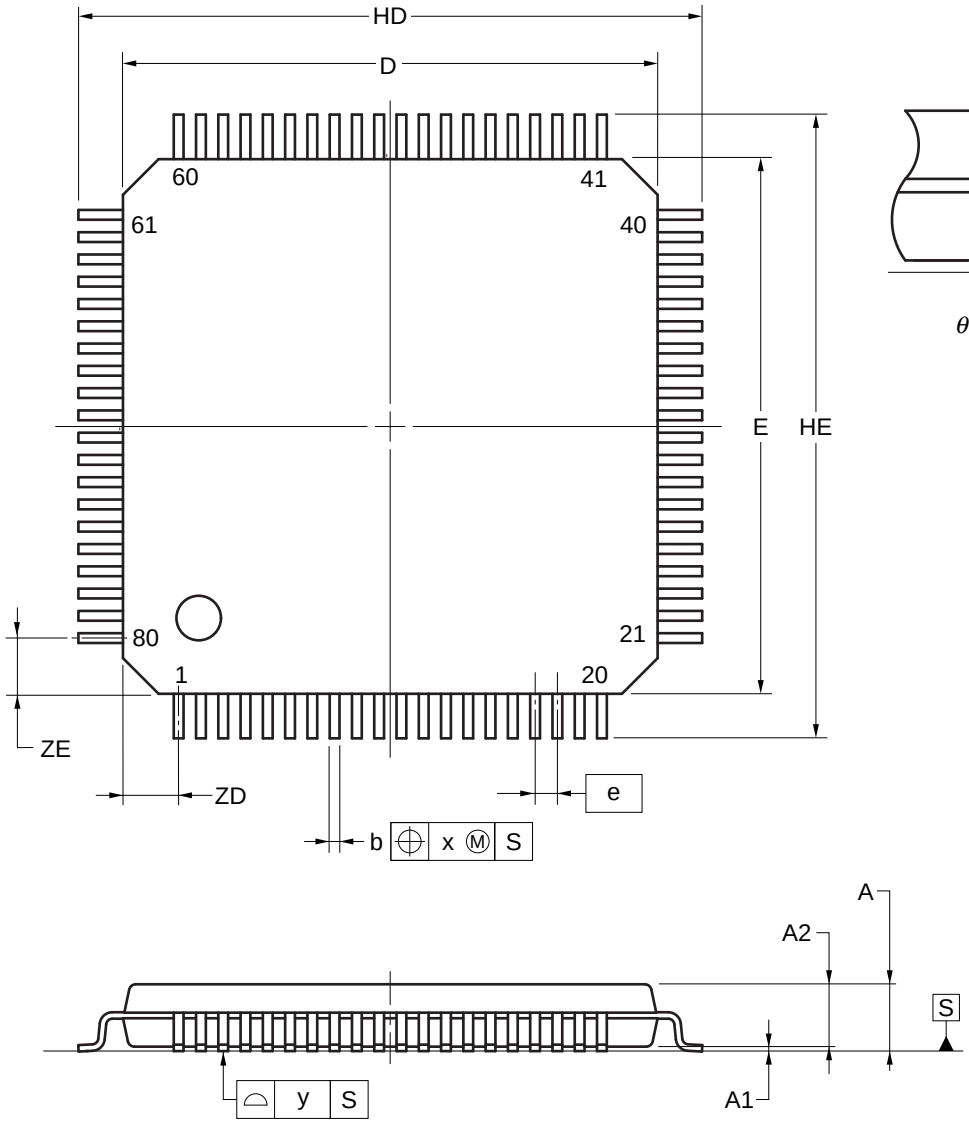
8.3 Serial write operation specification

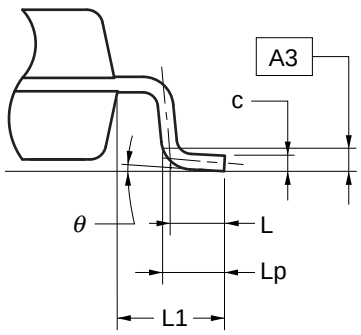
Table 8-3 Serial write operation specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Erase time		per 128 KB			2.1	s
Programming time		per 128 KB			1.92	s

Section 9 Package specification

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)





(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P80GK-50-GAK

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

Revision History	μPD70F4177, 70F4178 Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	2012.03.29	—	First Edition issued
1.00	2014.04.16	4	CAN chanel number fixed for each devices
		4	Correct the interrupts numbers
		4	Supply voltage 4.0 → Vpoc
		9	Modified the layout
		11	A0VDD → A0VREFP
		13	Correct the Port currents
		14	AnVSS → A0VSS, AnVREFP → A0VREFP
		16	Correct the RAVS MIN and MAX voltage gradient
		16	Deleted the figures
		17	Deleted the figures
		17	Vpoc 2.8 → 2.75
		22	Added High speed OSC frequency
		24	Correct the conditions V_{IL}, V_{OH}, V_{OL}
		25	Deleted the CMOS1 description
		25	Correct the conditions V_{IL}, V_{OH}, V_{0L}
		28	Replace the figure
		30	Correct the conditions t_{TBIH}, t_{TBIL}, t_{TBCYK}
		37	Correct the conditions CSIGnSSE,CSIGnCKR and CSIGnDAP
		44	V_{RAMHF} → 1.75
		45	Delete the LVS2 descriptions
		49	Data retention 15 years → 20 years
		49	Programming time 1.9 → 1.92

Notes for CMOS devices

(1) Voltage application wafeform at input pin:

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) Handling of unused input pins:

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) Precaution against ESD:

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) Status before initialization:

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) Power ON/OFF sequence:

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) Input of signal during power off state:

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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