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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD9971

SOUND GENERATOR LSI FOR RINGER MELODIES FOR MOBILE PHONES THAT ARE EQUIPPED WITH 3D POSITIONING SURROUND FUNCTIONS

DESCRIPTION

The μPD9971 is a sound generator LSI for ringer melodies for mobile phones that are equipped with 3D positioning surround functions.

FEATURES

- PCM sound generation method provides realistic sound reproduction
  - Contains 32 kHz sampling Wavetable, it include 128 GM tone and 47 drum set and 32 effect tone.
  - A richer tone is achieved by using 2 Wave a tone.
  - The wave and the parameter can be downloaded, and the sound-making not limited to a fixed tone is possible.
  - Can play up to four melodies because of four MIDI™ ports that are embedded in the sound generator core.
  - The port for a real-time control of MIDI that assumes karaoke and the JAVA®application program is installed.
  - Contains a digital parametric equalizer for equalizing speakers.
  - The function for a low output of the level to always enable the reproduction in the vicinity of the maximum volume is built into.
  - Various sound effects (pitch pipe bend, vibrato, Delay, reverberation, chorus, Doppra, and compressor) can be achieved.
  - Supports MOBILE-XMF.
- Contains real-time-processing 3D positioning surround functions
  - The effect of the sound that the sound source moves three-dimensionally by the digital signal processing can be achieved.
  - The stereophonic effect with the extension can be obtained by the digital signal processing.
  - The programmable solid sound parameter is installed, and the best setting is possible in the case and the speaker arrangement etc. of the cellular phone.
  - When the headphone is used, the stereophonic effect can be obtained.
- Includes a high-performance D/A converter with 16-bit resolution
  - Supports five sampling frequency (fs) modes: 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz
- Provides an audio serial I/O interface (16 bits).
  - The serial data input frequency is variable from 32 fs to 64 fs (during slave mode).
  - Supported formats are right-justified, left-justified, and IIS
- Provides an external serial input/output interface for the sound generator
- Provides stereo line output for audio
- Supports 8-bit parallel interface or 3 or 4-wire serial interface (SPI).
- Output control functions for vibration and LED.
- Built-in PLL, so various types of input clocks can be supported.
- Contains a regulator for digital power supply (DV_{DD}).

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The mark ★ shows major revised points.

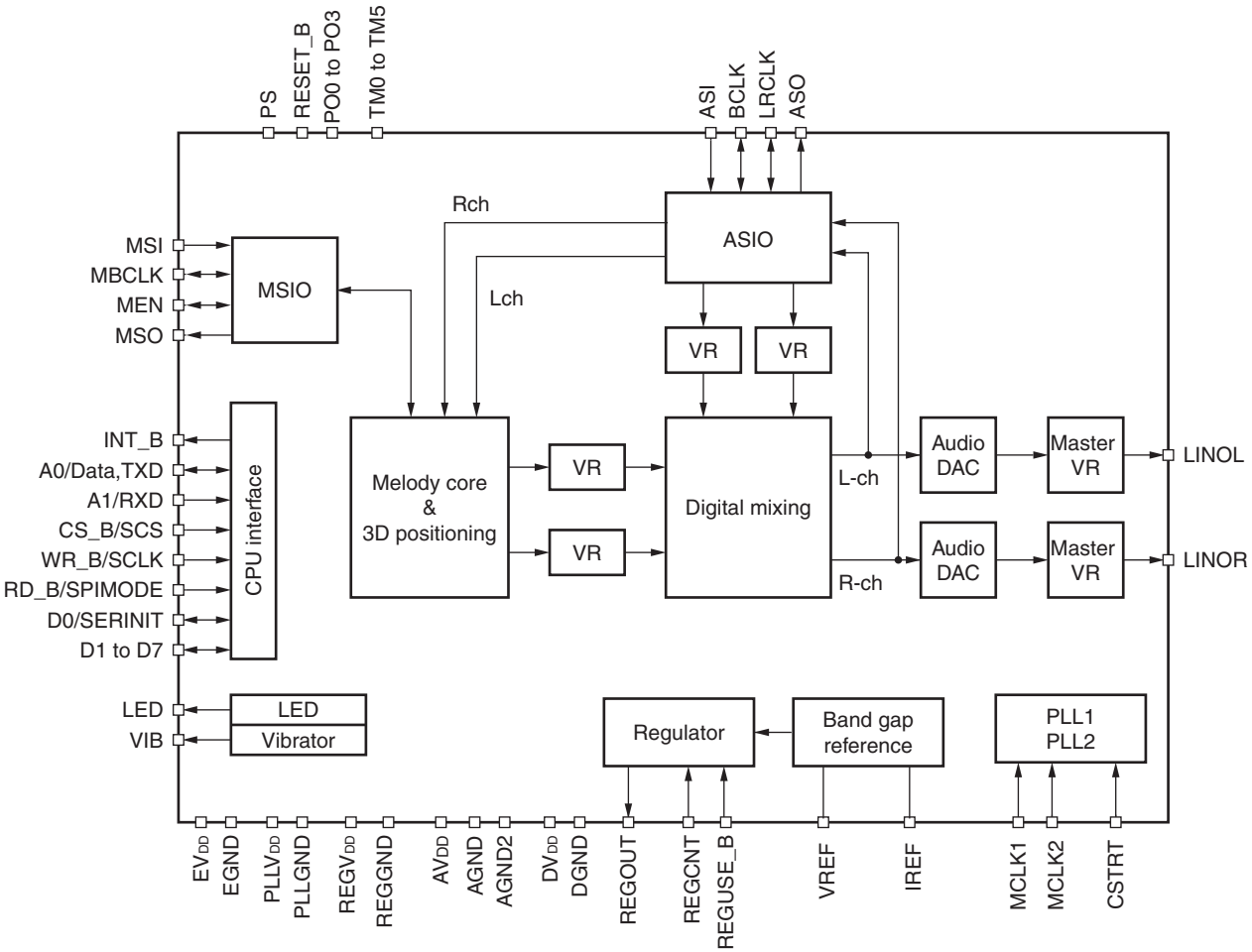
- Power supply voltages
  - I/O power supply (EV_{DD}): 1.7 to 3.3 V
  - Power supply for PLL ($PLLV_{DD}$): 2.7 to 3.3 V
  - Analog power supply (AV_{DD}): 2.7 to 3.3 V
  - Power supply for regulators ($REGV_{DD}$): 2.7 to 3.3 V
  - Digital power supply (DV_{DD}): Internal regulators (External voltage can be applied)
- Operating ambient temperatures: –20 to +85 °C
- 85-pin tape FBGA package (Body size: 6 × 6 mm, Ball pitch: 0.5 mm)

ORDERING INFORMATION

Part number	Package
μPD9971F9-BA3-A	85-pin tape FBGA (6 × 6)

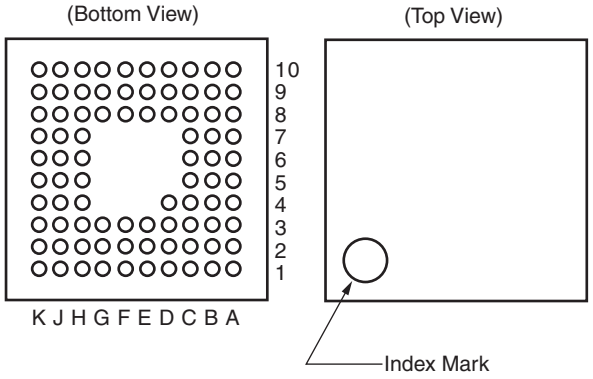
Remark A lead-free product.

BLOCK DIAGRAM



PIN CONFIGURATION

- 85-pin tape FBGA (6 × 6)
  μPD9971F9-BA3-A



Pin No.	Pin Name
1A	Shorted with 1K pin
1B	N.C
1C	LINOL
1D	AGND
1E	AV_{DD}
1F	LINOR
1G	AGND2
1H	PLLGND
1J	$REGV_{DD}$
1K	Shorted with 1A pin
2A	N.C
2B	N.C
2C	TM0
2D	IREF
2E	VREF
2F	TM1
2G	$PLLV_{DD}$
2H	MCLK1
2J	N.C
2K	REGOUT
3A	TM3
3B	TM2

Pin No.	Pin Name
3C	MSO
3D	N.C
3E	N.C
3F	MCLK2
3G	REGGND
3H	$REGV_{DD}$
3J	REGOUT
3K	REGCNT
4A	MSI
4B	TM4
4C	DV_{DD}
4D	N.C (index)
4H	REGUSE_B
4J	PO3
4K	PO2
5A	MEN
5B	MBCLK
5C	DGND
5H	PO0
5J	A1/RXD
5K	DGND
6A	EGND

Pin No.	Pin Name
6B	PS
6C	TM5
6H	PO1
6J	CS_B/SCS
6K	A0/Data, TXD
7A	ASI
7B	ASO
7C	DV_{DD}
7H	DV_{DD}
7J	RD_B/SPIMODE
7K	WR_B/SCLK
8A	LRCLK
8B	BCLK
8C	CSTRT
8D	N.C
8E	N.C
8F	DV_{DD}
8G	EGND
8H	EV_{DD}
8J	D1
8K	D0/SERINIT
9A	N.C

Pin No.	Pin Name
9B	N.C
9C	EV_{DD}
9D	VIB
9E	RESET_B
9F	D7
9G	D5
9H	D3
9J	N.C
9K	N.C
10A	Shorted with 10K pin
10B	N.C
10C	LED
10D	DV_{DD}
10E	INT_B
10F	D6
10G	D4
10H	D2
10J	N.C
10K	Shorted with 10A pin

Remark N.C: Reserved for future use. Leave this pin open.

PIN NAME

A0, A1:	Address
AGND:	Ground for Analog Block
AGND2:	Ground for Analog Block
ASI:	Audio Serial Data Input
ASO:	Audio Serial Data Output
AV_{DD}:	Power Supply for Analog Block
BCLK:	Bit Clock Input/Output
CS_B:	Chip Select
CSTRT:	Clock Select Signal Input from External
D0 to D7:	Data Bus
Data:	Data
DGND:	Ground for Digital Block
DV_{DD}:	Power Supply for Digital Block
EGND:	Ground for I/O Pins
EV_{DD}:	Power Supply for I/O Pins
INT_B:	Interruption
IREF:	Current Reference for Analog Block
LED:	LED Control Output
LINOL:	Line Out (L-ch)
LINOR:	Line Out (R-ch)
LRCLK:	Left Right Clock Input/Output
MBCLK:	Bit Clock for Melody Core
MCLK1:	Clock Input
MCLK2:	Clock Input
MEN:	Frame Clock for Melody Core
MSI:	Data Input for Melody Core
MSO:	Data Output for Melody Core
N.C.:	No Connection
N.C.(index):	No Connection
PLLGND:	Ground for PLL
$PLLV_{DD}$:	Power Supply for PLL
PO0 to PO3:	Peripheral Output
PS:	Parallel/Serial Interface Select
RD_B:	Read
REGCNT:	Regulator Control
REGGND:	Ground for Regulator
REGOUT:	Regulator Output
REGUSE_B:	Regulator Block Enable Signal Input
$REGV_{DD}$:	Power Supply for Regulator
RESET_B:	Reset
RXD:	Serial Data Input
SCLK:	Clock for Serial I/F
SCS:	Chip Select Input for Serial I/F
SERINIT:	Initialization Signal for Serial I/F
SPIMODE:	SPI Mode Select
TM0 to TM2:	Test Mode Input
TM3, TM4:	Test Mode I/O
TM5:	Test Mode Input
TXD:	Serial Data Output
VIB:	Vibration Control Output
VREF:	Voltage Reference for Analog Block
WR_B:	Write

CONTENTS

1. FUNCTIONS

1.1 General Descriptions of Functions

(1) Power supply voltages

Digital I/O power supply:	1.7 to 3.3 V, 1.8 V TYP.
Analog power supply:	2.7 to 3.3 V, 3.0 V TYP.
Power supply for PLL:	2.7 to 3.3 V, 3.0 V TYP.
Power supply for regulators:	2.7 to 3.3 V, 3.0 V TYP.
(Digital power supply:	1.45 to 1.65 V, 1.54 V TYP.)

(2) Operating temperatures

−20 to +85°C

(3) Function blocks

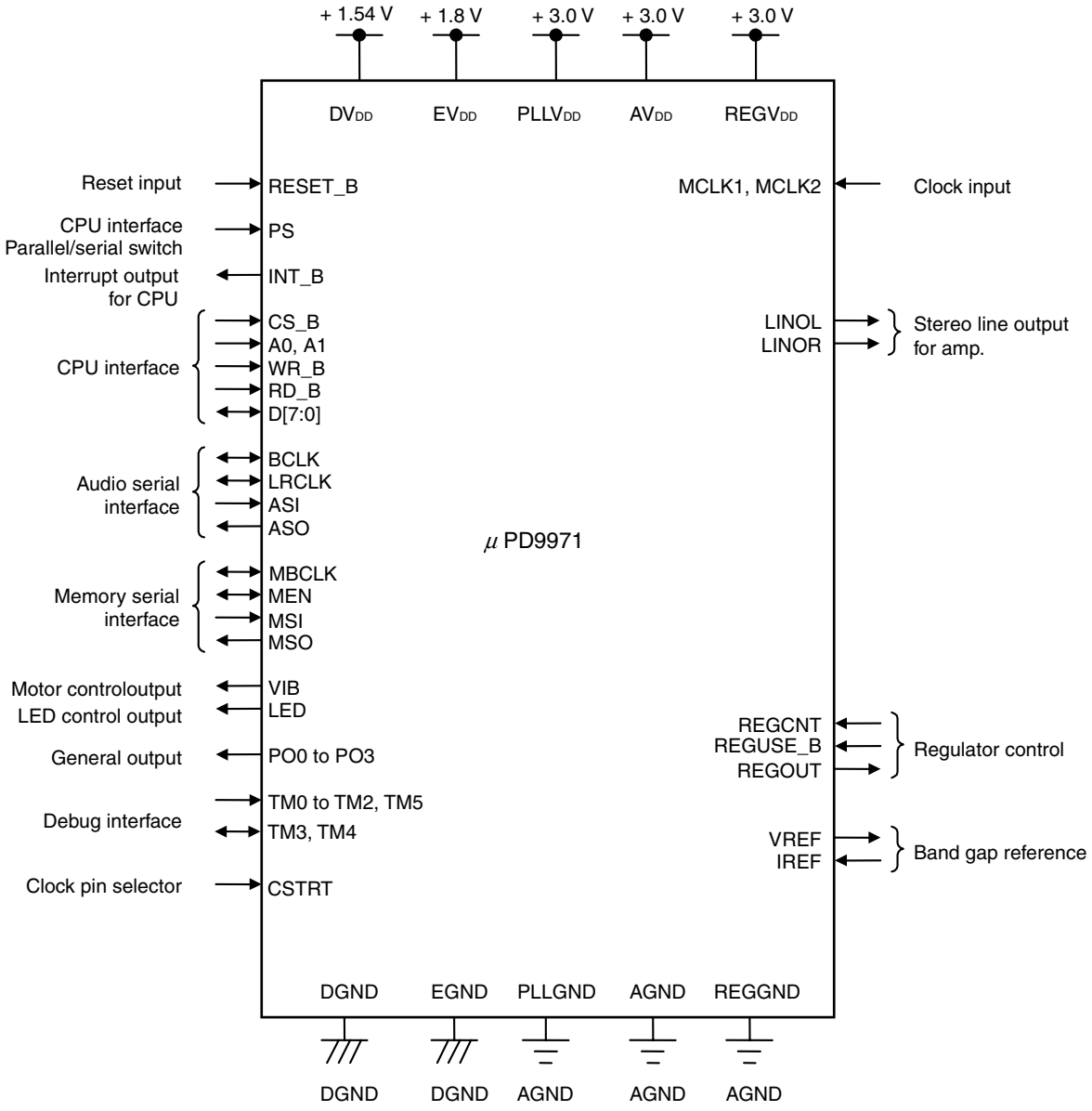
Melody Core:	PCM sound generator core for 128 polyphonic
3D Positioning:	3D positioning surrounds function
Digital Mixing:	Digital mixing circuit
Regulator:	Regulator for digital power supply
PLL1/PLL2:	PLL for sound generator and PLL for audio
Audio DAC:	Stereo 16-bit audio DAC
Band gap:	Circuit generating reference voltage and current for analog circuits
VIB/LED:	Circuit generating control signals for vibration and LED
Master/Digital VR:	Volume circuit

1.2 General Descriptions of Circuits

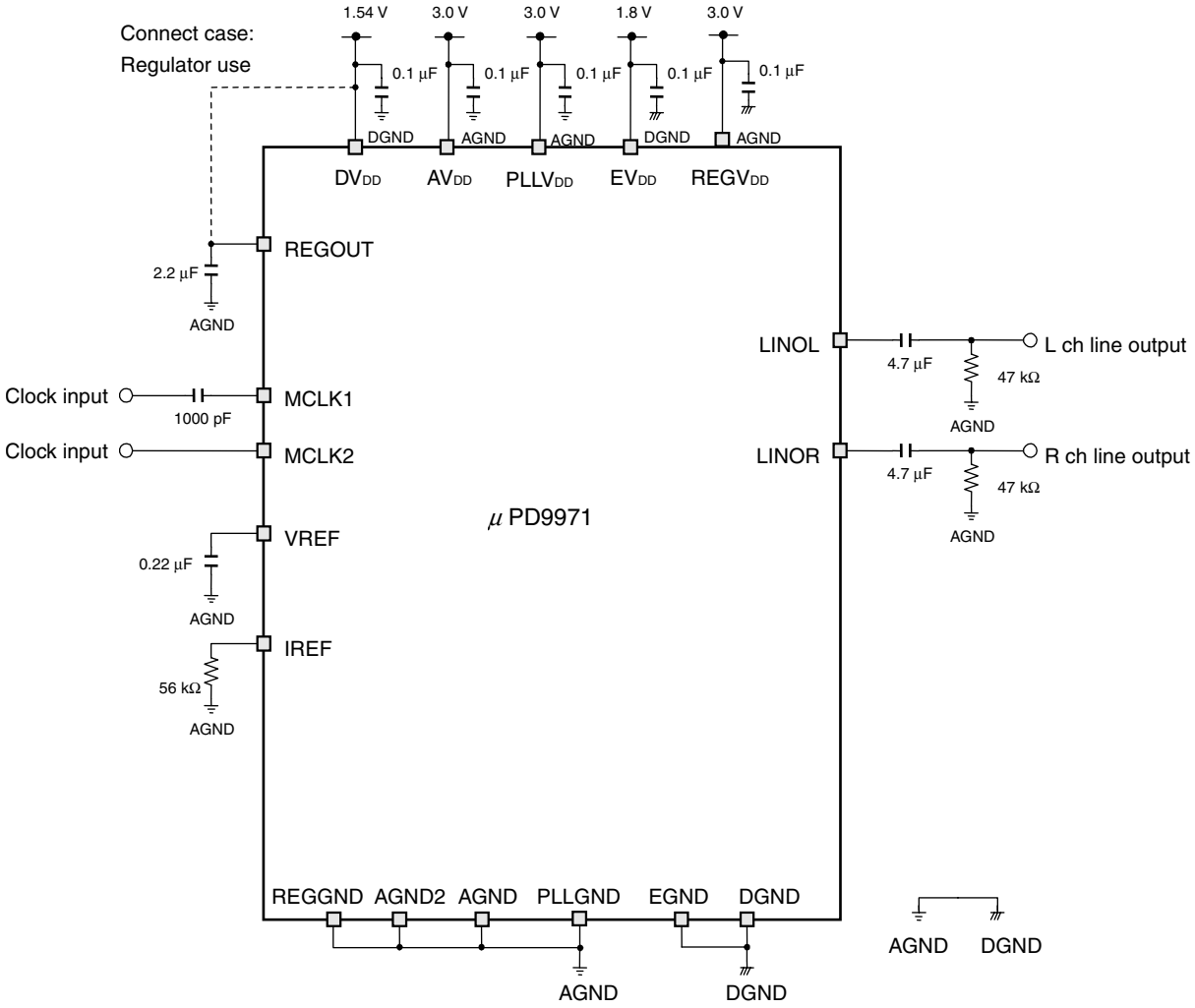
Block	Functions
Melody Core	Up to 128 tones can be produced at the same time. This block contains a PCM sound generator and a sequencer. The sampling frequency is 32 kHz.
3D Positioning	3D positioning surround function
Digital Mixing	Switching or adding sound generator output and audio serial input.
PLL	Generates master clocks for processing internal signals. Input clocks: 3.84 MHz to 15.36 MHz
Audio DAC	16 bits × 2 channels (L-ch and R-ch) Sampling frequencies: 48 kHz, 44.1 kHz, 32 kHz, 16 kHz, and 8 kHz (Default: 32 kHz) The interface supports the master and slave modes. Dynamic range: 90 dBr TYP (for a single block)
Regulator	1.54 V output regulator for digital power supply
VIB/LED	Outputs control signals for VIB and LED.
Master/Digital VR	Master volume: 0 dB to −45 dB/1.5 dB increments Digital volume: +12 dB to −63 dB/1 dB increments

2. PINS FUNCTIONS

2.1 Pin Configuration



2.2 Recommended External Circuit



2.3 Descriptions of Pin Functions

(1) Power supply pins and GND pins

Pin Name	Pin No.	I/O	Functions
DV_{DD}	4C, 7C, 7H, 8F, 10D	–	Power supply for digital blocks When using an internal regulator, connect this pin and the REGOUT pin on the outside of the μPD9971. Be sure to connect a 0.1 μF capacitor between this pin and DGND.
DGND	5C, 5K	–	Ground for digital blocks
EV_{DD}	8H, 9C	–	Power supply for digital I/O Be sure to connect a 0.1 μF capacitor between this pin and EGND.
EGND	6A, 8G	–	Ground for digital I/O
$PLLV_{DD}$	2G	–	Power supply for PLL Be sure to connect a 0.1 μF capacitor between this pin and PLLGND.
PLLGND	1H	–	Ground for PLL
AV_{DD}	1E	–	Power supply for analog blocks Be sure to connect a 0.1 μF capacitor between this pin and AGND.
AGND	1D	–	Ground for analog blocks
AGND2	1G	–	Ground for analog blocks
$REGV_{DD}$	1J, 3H	–	Power supply for regulator band gap reference Be sure to connect a 0.1 μF capacitor between this pin and REGGND.
REGGND	3G	–	Ground for regulators

(2) Clock and system control pins

Pin Name	Pin No.	I/O	Functions
MCLK1	2H	Input	Clock input (3.84 MHz to 15.36 MHz) This is the reference clock input to generate the internal master clock. Be sure to input using capacitive coupling (1000 pF). Connect this pin to GND when the pin is not used.
MCLK2	3F	Input	Clock input (3.84 MHz to 15.36 MHz) This is the reference clock input to generate the internal master clock. This pin is also used for inputting square waves of input level EV_{DD}. Connect this pin to GND when the pin is not used.
CSTRT	8C	Input	Signal input to select clock input from outside **Cautions This pin is valid when the CSTRTEN register is high level. When the CSTRT pin does switching, however, only limited frequencies can be input. Before using this pin, be sure to contact NEC Electronics.** 0: Selects input from MCLK2. 1: Selects input from MCLK1 This pin is pulled down in the μPD9971.
RESET_B	9E	Input	Hardware reset signal input This resets the μPD9971. 0: Resets. 1: Cancels the reset. Registers are initialized to their initial values after a reset.

(3) Host CPU pins and interface pins

(1/2)

Pin Name	Pin No.	I/O	Functions
A0/Data, TXD	6K	I/O	1. Parallel I/F mode (when PS = 0) Host interface address A0 signal input This input pin indicates the internal register address or data during host CPU access. 1: When transferring data 0: When setting the address of the register to be accessed
			2. Serial mode (when PS = 1) Bidirectional TX/RX serial input/output (when PS = 1 and RD_B = 0). In this case, this pin is used as 3-wire SPI mode TX serial data output (when PS = 1 and RD_B = 1). In this case, this pin is used as 4-wire SPI mode
A1/RXD	5J	Input	1. Parallel I/F mode (when PS = 0) Host interface address A1 signal input This input pin selects the access destination register during host CPU access. 1: PCM Sound generator register 0: Register other than PCM sound generator register
			2. Serial I/F mode (when PS = 1) This pin is not used in 3-wire SPI mode (RD_B = 0). This pin inputs receive data in 4-wire SPI mode (RD_B = 1).
CS_B/SCS	6J	Input	1. Parallel I/F mode (when PS = 0) Chip select input for parallel I/F This is the input pin for the host interface select signal. This pin is set as active (low) while the host CPU accesses a register
			2. Serial I/F mode (when PS = 1) Chip select input for serial I/F
RD_B/SPIMODE	7J	Input	1. Parallel I/F mode (when PS = 0) Host read input This pin is set as active (low) while the host CPU reads a register. Do not set this pin and the WR_B pin as active at the same time.
			2. Serial I/F mode (when PS = 1) 3-wire / 4-wire SPI mode selection 0: 3-wire SPI mode. 1: 4-wire SPI mode.
WR_B/SCLK	7K	Input	1. Parallel mode (when PS = 0) Host write input This pin is set as active (low) while the host CPU reads a register. Do not set this pin and the RD_B active pin at the same time.
			2. Serial mode (when PS = 1) Clock for serial I/F at frequencies up to 13 MHz.

(2/2)

Pin Name	Pin No.	I/O	Functions
D0/(SERINT)	8K	I/O	1. Parallel I/F mode (when PS = 0) Bit 0 for 8-bit host data bus When the host CPU accesses μPD9971, address and data I/O is performed. When the CS_B signal in inactive (high), this pin is set to high impedance.
			2. Serial I/F mode (when PS = 1) Initialization signal for serial I/F
D1 to D7	8J, 10H, 9H, 10G, 9G, 10F, 9F	I/O	1. Parallel I/F mode (when PS = 0) Bits 7 -1 for 8-bit host data bus When the host CPU accesses μPD9971, address and data I/O is performed. When the CS_B signal in inactive (high), this pin is set to high impedance.
			2. Serial I/F mode (when PS = 1) This bus is always set to high impedance
INT_B	10E	Output	Interrupt request from PCM sound generator This signal requests interrupts from the μPD9971 to the host CPU. This is used when requesting data transfer or internal status notification.
PS	6B	Input	Parallel/serial I/F mode setting This pin sets the parallel or serial mode of the host CPU interface. 1: Serial I/F mode 0: Parallel I/F mode This pin has an internal pull-down resistor

(4) Audio serial interface pins (ASIO)

Pin Name	Pin No.	I/O	Functions
BCLK	8B	I/O	Bit synchronization clock I/O for audio serial When this pin is not used, connect it to GND.
LRCLK	8A	I/O	Audio serial frame synchronization clock I/O When this pin is not used, connect it to GND.
ASO	7B	Output	Audio serial data output The audio serial data frame size is set via registers. During master mode, either 64 bits or 32 bits can be selected. During slave mode, selections can be made in 2-bit steps within a range from 32 to 64 bits. Leave this pin open when not used.
ASI	7A	Input	Audio serial data input The audio serial data frame size is set via registers. During master mode, either 64 bits or 32 bits can be selected. During slave mode, selections can be made in 2-bit steps within a range from 32 to 64 bits. Leave this pin open when not used. Pull-down is performed internally.

(5) Serial interface dedicated to sound generator core external connection (MSIO)

Pin Name	Pin No.	I/O	Functions
MBCLK	5B	I/O	Bit synchronization clock I/O dedicated to PCM sound generator external connection When this pin is not used, connect it to GND.
MEN	5A	I/O	Frame synchronization clock I/O dedicated to PCM sound generator external connection When this pin is not used, connect it to GND.
MSO	3C	Output	Data output dedicated to PCM sound generator external connection Frame size of serial data is set by using the register. In the master mode, 32, 64, 128, or 256 bits can be selected (when only MSIO is used). In slave mode, selections can be made in 32-bit increments within a range from 32 to 256 bits (when only MSIO is used). When this pin is not used, leave it open.
MSI	4A	Input	Data input dedicated to PCM sound generator external connection Frame size of serial data is set by using the register. In the master mode, 32, 64, 128, or 256 bits can be selected (when only MSIO is used). In the slave mode, selections can be made in 32-bit increments within a range from 32 to 256 bits (when only MSIO is used). When this pin is not used, leave it open. (This pin contains a pull-down register.)

Cautions 1. Data sizes that can be set vary depending on the master mode or the slave mode.
In the master mode, MBFS is only 32, 64, 128, or 256 fs.
In the slave mode, MBFS can be selected within a range from 32 to 256 bits, in 32-fs increments.

2. When MSIO and ASIO are used at the same time, ASIO can be set to the master mode only (BFS = 32 or 64 fs).

(6) External LED pin and motor control output pin

Pin Name	Pin No.	I/O	Functions
LED	10C	Output	External LED control output (The drive capacity is 1 mA when EV_{DD} = 1.8 V.) This pin is the port output pin. Settings are entered by writing values to the port setting register from the host CPU. When this pin is not used, leave it open.
VIB	9D	Output	External motor control output (The drive capacity is 1 mA when EV_{DD} = 1.8 V.) This pin is the port output pin. Settings are entered by writing values to the port setting register from the host CPU. When this pin is not used, leave it open.

(7) Reference voltage/current pins for analog circuits

Pin Name	Pin No.	I/O	Functions
VREF	2E	Output	Reference voltage for analog blocks Be sure to connect a 0.22 μF capacitor between this pin and AGND.
IREF	2D	Input	For generating reference current for analog blocks Be sure to connect a 56 kΩ register between this pin and AGND.

(8) Audio DAC output pins

Pin Name	Pin No.	I/O	Functions
LINOL	1C	Output	Line (L-ch) output
LINOR	1F	Output	Line (R-ch) output

(9) Regulator pins

Pin Name	Pin No.	I/O	Functions
REGOUT	2K, 3J	Output	Regulator output When using regulator output for the digital power supply, connect these pins with DV_{DD} pin outside the μPD9971. Be sure to connect a 2.2 μF capacitor between this pin and REGGND.
REGUSE_B	4H	Input	Regulator block enable signal input pin 0: When the regulator is used 1: When the regulator is not used
REGCNT	3K	Input	Input pin for regulator control 0: Stops the output. 1: Starts the output.

(10) General-purpose external output pins

Pin Name	Pin No.	I/O	Functions
PO0 to PO3	5H, 6H, 4K, 4J	Output	General-purpose external output pins These pins can be used to output control signals to peripheral devices. When they are not used, leave them open.

(11) Test pins

Pin Name	Pin No.	I/O	Functions
TM0 to TM2	2C, 2F, 3B	Input	Input for tests Leave these pins open when using them under normal conditions.
TM3 to TM4	3A, 4B	I/O	Input/output for tests Leave these pins open when using them under normal conditions.
TM5	6C	Input	Input for tests Leave this pin open when using it under normal conditions.

(12) Others

N.C.	Pin No.	I/O	Functions
N.C	1B, 2A, 2B, 2J, 3D, 3E, 8D, 8E, 9A, 9B, 9J, 9L, 10B, 10J	–	Reserved for future use. Leave this pin open.
N.C (index)	4D	–	Reserved for future use. Leave this pin open.

2.4 Connection of Unused Pins

Table 2-1 Connection of Unused Pins

Pin Name	I/O	Recommended Connection
MCLK1	I	Connect to PLLGND.
MCLK2	I	Connect to EGND.
CSTRT	I	Leave open (Internal Pull-down).
A1/RXD	I	Connect to DGND.
D0/SERINIT	I	Connect to DGND.
D1 to D7	I	Connect to DGND.
INT_B	O	Leave open.
LRCLK	I/O	Connect to DGND.
BCLK	I/O	Connect to DGND.
ASI	I	Leave open (Internal Pull-down).
ASO	O	Leave open.
MEN	I/O	Connect to DGND.
MBCLK	I/O	Connect to DGND.
MSI	I	Leave open (Internal Pull-down).
MSO	O	Leave open.
LED	O	Leave open.
VIB	O	Leave open.
LINOL	O	Leave open.
LINOR	O	Leave open.
REGUSE_B	I	Connect to EV_{DD} (when regulator is not used).
REGCNT	I	Connect to EGND (when regulator is not used).
$REGV_{DD}$	Power	Connect to a 3.0 V power supply (regardless of whether the regulator is used or not).
REGOUT	O	Leave open (when the regulator is not used).
PO0 to PO3	O	Leave open.
TM0 to TM2	I	Leave open (Internal Pull-down).
TM3, TM4	I/O	Leave open.
TM5	I	Leave open (Internal Pull-down).

2.5 Pin Statuses

(1/2)

Pin. No	I/O	A/D	Pin Name	Standby Status		RESET_B=0 status		After Reset
				Control Signal	Pin Status	Control Signal	Pin Status	
2F	Input	Digital	TM1		Input		Input	Input
1C	Output	Analog	LINOL	STDAC	Hi-Z	STDAC	Hi-Z	Hi-Z
1D		Analog	AGND					
2D	Output	Analog	IREF	STREF	Hi-Z	STREF	Hi-Z	Hi-Z
2E	Output	Analog	VREF	STREF	Hi-Z	STREF	Hi-Z	Hi-Z
1E		Analog	AV_{DD}					
1F	Output	Analog	LINOR	STDAC	Hi-Z	STDAC	Hi-Z	Hi-Z
1G		Analog	AGND2					
2G		Analog	$PLLV_{DD}$					
2H	Input	Analog	MCLK1	STPLL1, STPLL2	Input	STPLL1, STPLL2	Input	Input
1H		Analog	PLLGND					
3G		Analog	REGGND					
3H		Analog	$REGV_{DD}$					
1J		Analog	$REGV_{DD}$					
2K	Output	Analog	REGOUT	REGCNT	Low	REGCNT	Low	Low
3J	Output	Analog	REGOUT	REGCNT	Low	REGCNT	Low	Low
3F	Input	Analog	MCLK2	STPLL1, STPLL2	Input	STPLL1, STPLL2	Input	Input
3K	Input	Digital	REGCNT		Input		Input	Input
4H	Input	Digital	REGUSE_B		Input		Input	Input
5H	Output	Digital	PO0		Register	RESET_B	Low	Low
4K	Output	Digital	PO2		Register	RESET_B	Low	Low
4J	Output	Digital	PO3		Register	RESET_B	Low	Low
6H	Output	Digital	PO1		Register	RESET_B	Low	Low
5K		Digital	DGND					
5J	Input	Digital	A1/RXD		Input		Input	Input
7H		Digital	DV_{DD}					
6K	I/O	Digital	A0/Data, TXD		Input		Input	Input
6J	Input	Digital	CS_B/SCS		Input		Input	Input
7J	Input	Digital	RD_B/SPIMODE		Input		Input	Input
7K	Input	Digital	WR_B/SCLK		Input		Input	Input
8H		Digital	EV_{DD}					
8K	I/O	Digital	D0/SERINIT		Input	RESET_B	Hi-Z	Input
8J	I/O	Digital	D1		Input	RESET_B	Hi-Z	Input
8G		Digital	EGND					
10H	I/O	Digital	D2		Input	RESET_B	Hi-Z	Input
9H	I/O	Digital	D3		Input	RESET_B	Hi-Z	Input

(2/2)

Pin. No	I/O	A/D	Pin Name	Standby Status		RESET_B=0 status		After Reset
				Control Signal	Pin Status	Control Signal	Pin Status	
8F		Digital	DV_{DD}					
10G	I/O	Digital	D4		Input	RESET_B	Hi-Z	Input
9G	I/O	Digital	D5		Input	RESET_B	Hi-Z	Input
10F	I/O	Digital	D6		Input	RESET_B	Hi-Z	Input
9F	I/O	Digital	D7		Input	RESET_B	Hi-Z	Input
10E	Output	Digital	INT_B		Output	RESET_B	High	High
9E	Input	Digital	RESET_B		Input		Input	Input
10D		Digital	DV_{DD}					
9D	Output	Digital	VIB		Register	RESET_B	Low	Low
10C	Output	Digital	LED		Register	RESET_B	Low	Low
9C		Digital	EV_{DD}					
8C	Input	Digital	CSTRT		Input		Input	Input
8B	I/O	Digital	BCLK	STASI, STASO		RESET_B	Hi-Z	Input
8A	I/O	Digital	LRCLK	STASI, STASO		RESET_B	Hi-Z	Input
7C		Digital	DV_{DD}					
7A	Input	Digital	ASI	STASI, STASO			Input	Input
7B	Output	Digital	ASO	STASI, STASO		RESET_B	Hi-Z	Hi-Z
6B	Input	Digital	PS		Input		Input	Input
6A		Digital	EGND					
6C	Input	Digital	TM5		Input		Input	Input
5B	I/O	Digital	MBCLK	STMSI, STMSO		RESET_B	Hi-Z	Input
5A	I/O	Digital	MEN	STMSI, STMSO		RESET_B	Hi-Z	Input
5C		Digital	DGND					
4C		Digital	DV_{DD}					
4A	Input	Digital	MSI	STMSI, STMSO			Input	Input
4B	I/O	Digital	TM4		Low	RESET_B	Hi-Z	Low
3C	Output	Digital	MSO	STMSI, STMSO		RESET_B	Hi-Z	Hi-Z
3A	I/O	Digital	TM3		Low	RESET_B	Hi-Z	Low
3B	Input	Digital	TM2		Input		Input	Input
2C	Input	Digital	TM0		Input		Input	Input

For pin statuses in ASIO and MSIO blocks, refer to **Table 2-2, Table 2-3**.

Table 2-2 Pin Statuses in ASIO Block

Pin	Pin Function	AMS = 0 (Slave Mode) (STASI, STASO)				AMS = 1 (Master Mode) (STASI, STASO)			
		(0, 0)	(1, 1)	(1, 0)	(0, 1)	(0, 0)	(1, 1)	(1, 0)	(0, 1)
BCLK	Bit synchronization I/O for audio	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
LRCLK	Frame synchronization I/O for audio	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
ASI	Audio serial data input	–	Input	Input	–	–	Input	Input	–
ASO	Audio serial data output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output

Table 2-3 Pin Statuses in MSIO Block

Pin	Pin Function	MMS = 0 (Slave Mode) (STMSI, STMSO)				MMS = 1 (Master Mode) (STMSI, STMSO)			
		(0, 0)	(1, 1)	(1, 0)	(0, 1)	(0, 0)	(1, 1)	(1, 0)	(0, 1)
MBCLK	Bit synchronization I/O for PCM sound generator-core	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
MEN	Frame synchronization I/O for PCM sound generator-core	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
MSI	PCM sound generator-core serial data input	–	Input	Input	–	–	Input	Input	–
MSO	PCM sound generator-core serial data output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output

3. CPU INTERFACE

Two interface modes are available: parallel interface mode, and serial interface mode. The access methods from the host CPU interface are described below.

3.1 Parallel Host CPU Interface

Setting the PS pin to low level enters the parallel I/F mode.

3.1.1 Write access

During write access, data is written to the μPD9971 from the system.

- A0 is used to distinguish between address write cycles and data write cycles.
- A1 is used to distinguish between register access for the sound generator and chip control. (0: For chip control, 1: For the sound generator)
- In the address write cycle, the data write address is assigned to bits D7 to D0.

Caution Be sure to fix the RD_B pin to the high level during address write cycles and data write cycles.

Figure 3-1 Write Access (Single Access)

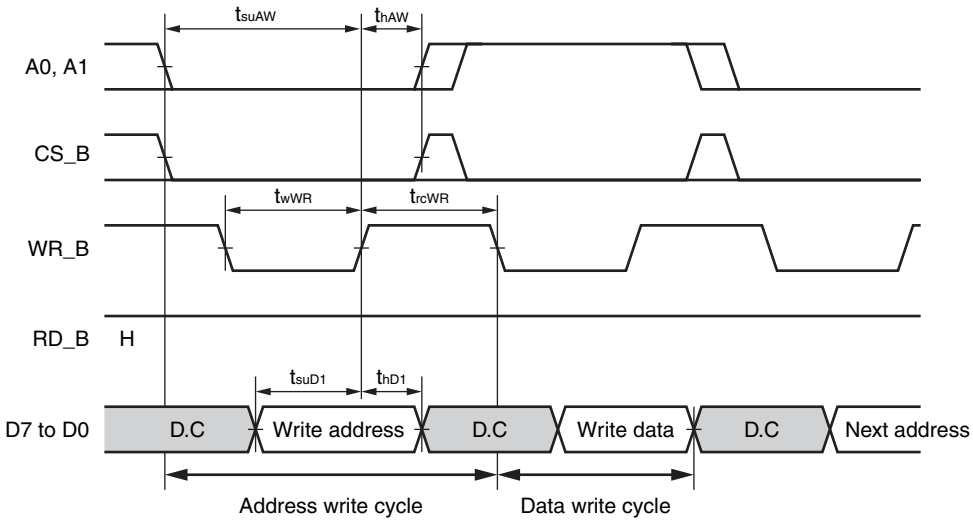
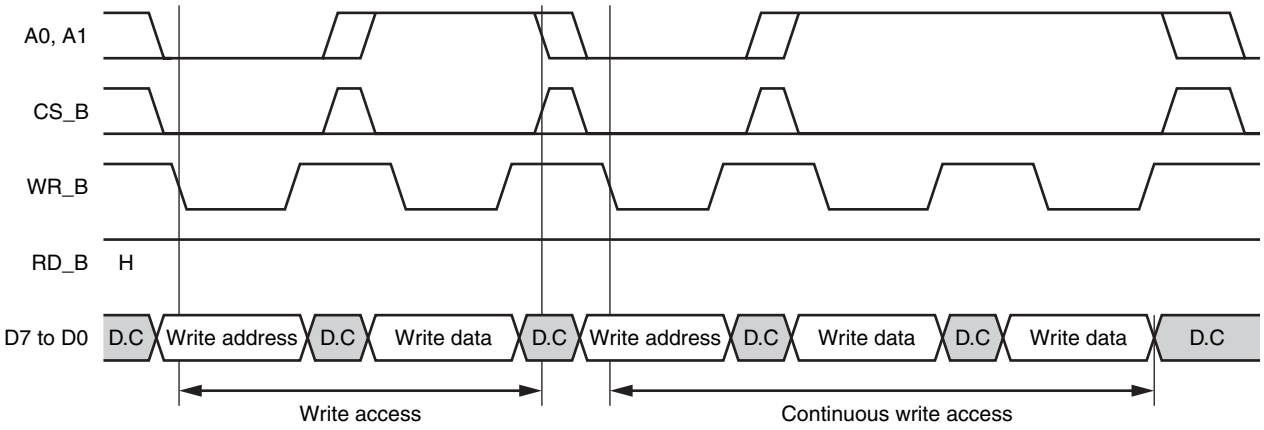


Figure 3-2 Write Access (Continuous Access)



Remark Set the CS_B pin to the low level during the write period. It is not necessary to always set the CS_B pin to the low level during continuous write access.
D.C.: Don't Care

3.1.2 Read access

During read access, data is read from the system by μPD9971. The read access timing is shown below.

- A0 is used to distinguish between address write cycles and data read cycles.
- A1 is used to distinguish between register access for the sound generator and chip control (0: For chip control ,1: For the sound generator)
- Operation is based on the detection of the rising edge of WR_B and RD_B by the system clock.
- In the address write cycle, the write data address is assigned to bits D7 to D0.

Figure 3-3 Read Access (Single Access)

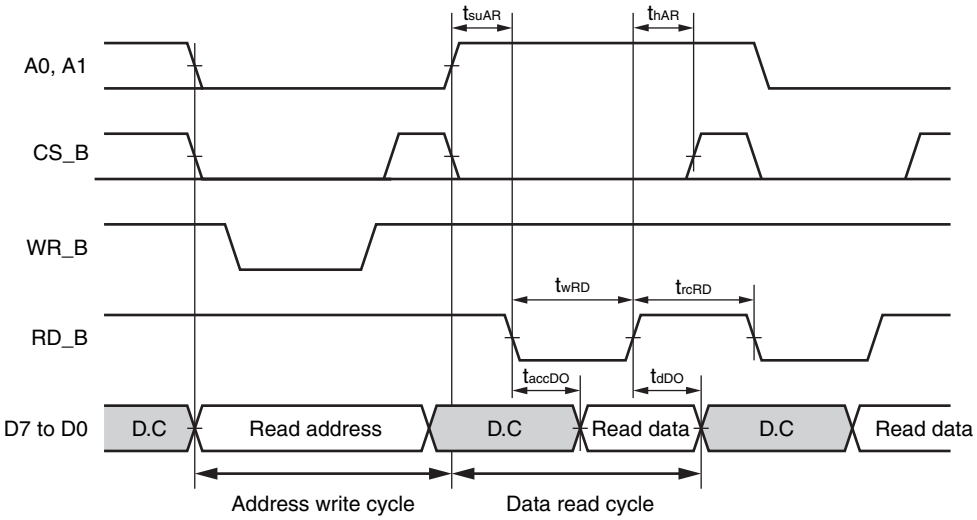
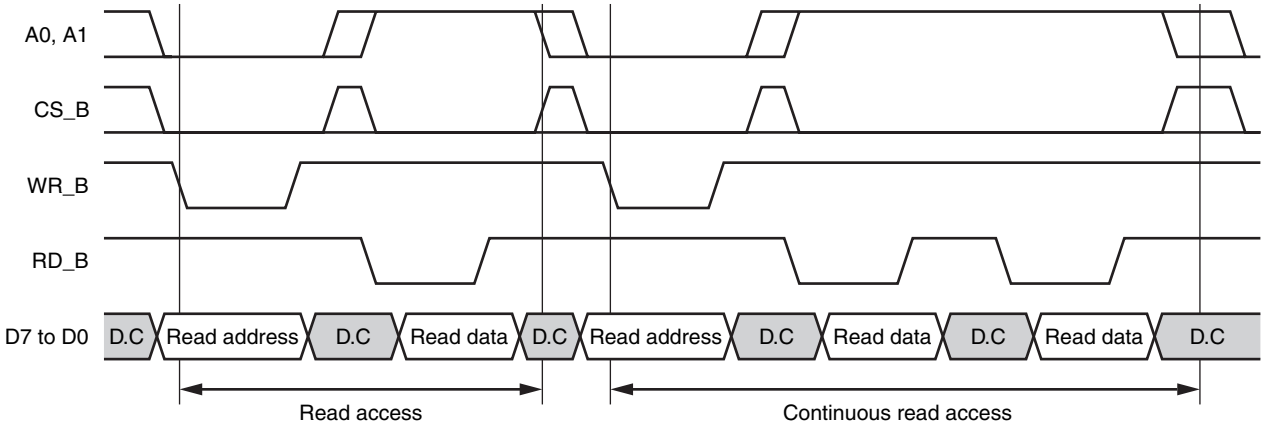


Figure 3-4 Read Access (Continuous Access)



Remark Set the CS_B pin to the low level during the read period. It is not necessary to always set the CS_B pin to the low level during continuous read access.
D.C.: Don't Care

3.2 Serial Host Interface

Setting the PS pin to high level enters the Serial I/F mode. In this mode, there are two communication methods: 3-wire SPI mode and 4-wire SPI mode. The SPIMODE (RD_B) is used to switch the SPI mode.

3.2.1 Pin functions

- The pins used in the serial mode can also be used in the parallel mode.
  The setting of the PS pin validates the serial mode.
  1: Serial mode
  0: Parallel mode (default)

- Switching the modes of the RD_B (SPIMODE) pin leads to the selection of a transfer method--either the 3-wire SPI mode or the 4-wire SPI mode.
  1: 4-wire SPI mode
  0: 3-wire SPI mode

Pin Name		I/O	Functions
Serial	Parallel		
PS	PS	I	Host CPU interface mode select signal input 0: Parallel mode is valid. 1: Serial mode is valid.
SPIMODE	RD_B	I	SPI mode select signal input 0: 3-wire SPI mode 1: 4-wire SPI mode
SCLK	WR_B	I	Serial clock input
SCS	CS_B	I	Chip select signal input
Data, TXD	A0	I/O	In 3-wire SPI mode: Inputs or outputs transmit/receive data. In 4-wire SPI mode: Outputs transmit data.
RXD	A1	I	In 3-wire SPI mode: This pin is not used. In 4-wire SPI mode: This pin inputs receive data.
SERINT	D0	I	Serial reset signal input When SERINT =1 and SCS = 1, an asynchronous reset is triggered in the serial interface circuit.

3.2.2 Serial formats

Total:	16 bits
Read/write control:	1 bit (High: Write, Low: Read)
Address:	7 bits
Data:	8 bits

(1) Register areas

The μPD9971 has two banks: One for the setting of the sound generator core (sound generator bank) and the other for controlling the chip (Control register bank).

Writing a value to a specific address performs switching of these registers. (7CH: Bank Register)

(2) Access formats

The formats below are provided.

1. Normal write access
2. Normal read access
3. Continuous write access (1)
4. Continuous write access (2) for FIFOs

3.2.3 Access formats (3-wire SPI mode)

Figure 3-5 Host CPU Access (During Write/Read Access)

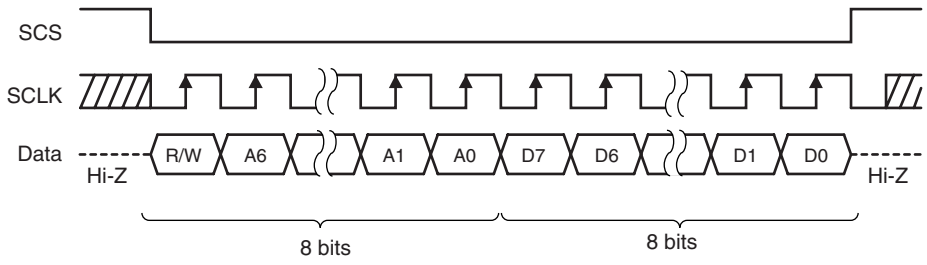
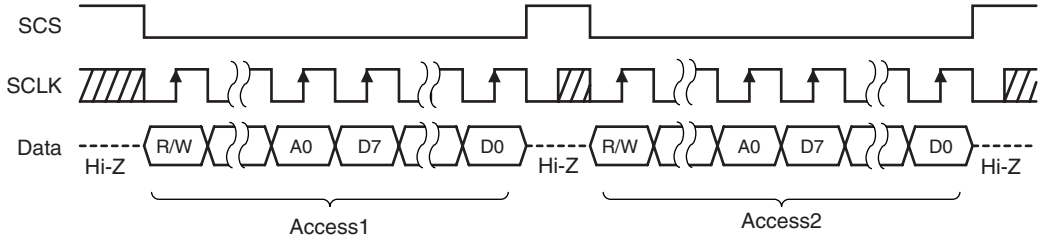
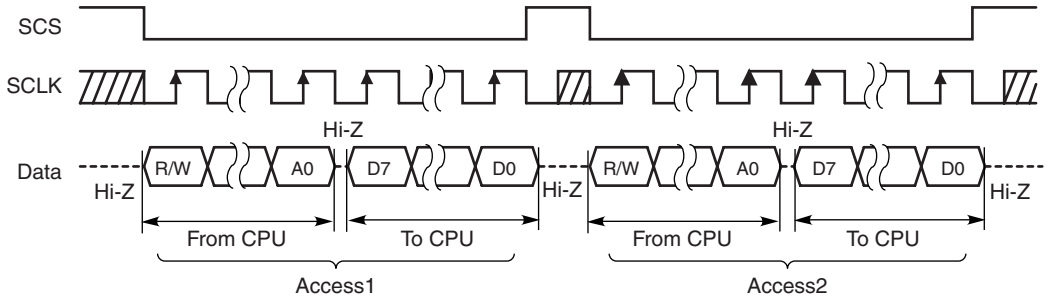


Figure 3-6 Host CPU Access Formats (Continuous Access)

(a) Write Access



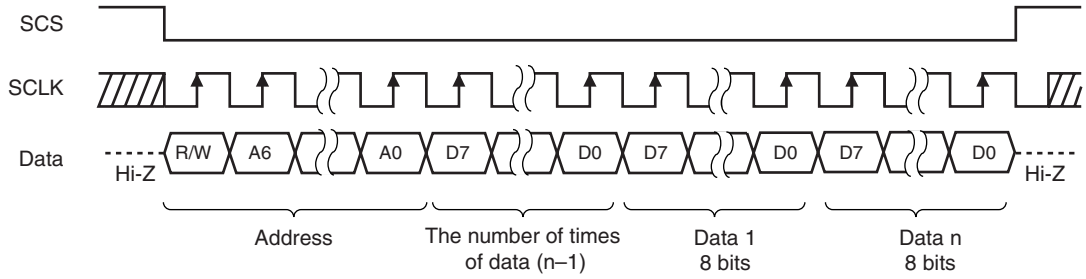
(b) Read Access



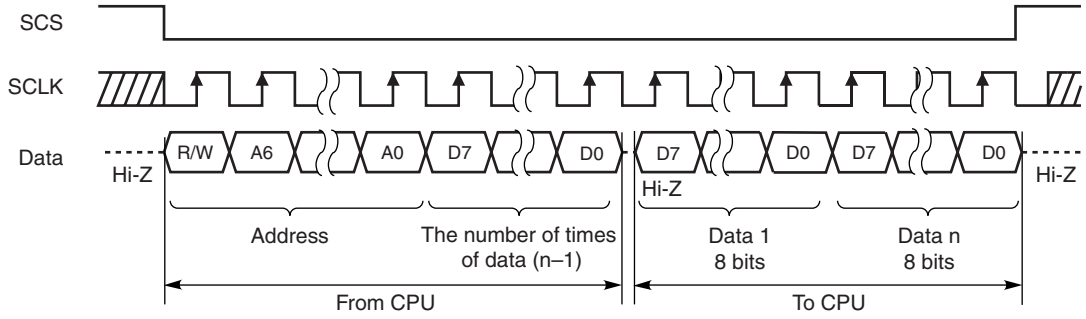
Remark The above formats are used except when accessing FIFOs in the sound generator block.

Figure 3-7 Host CPU Access Formats (Continuous Access)

(a) Write Access



(b) Read Access



Remark The above formats are only used to access FIFOs in the sound generator block.

3.2.4 Access formats (4-wire SPI mode)

Figure 3-8 Host CPU Access Format (Read/Write Access)

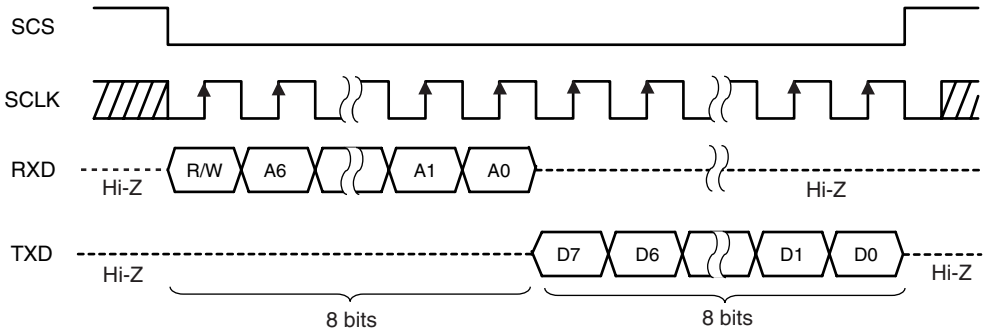
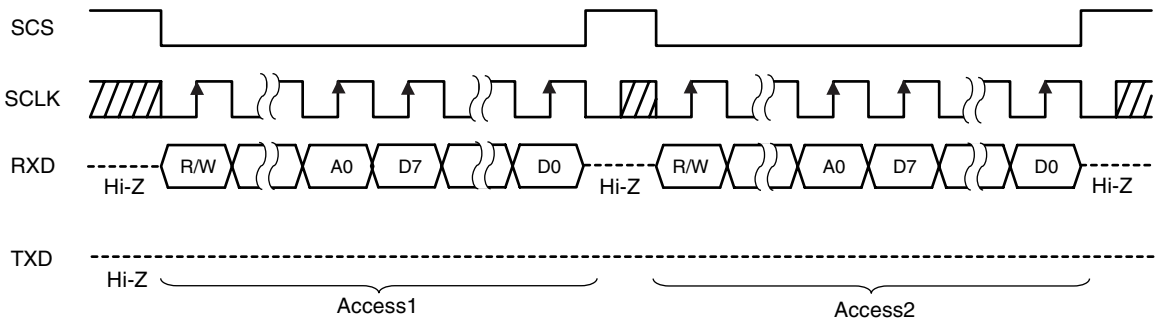
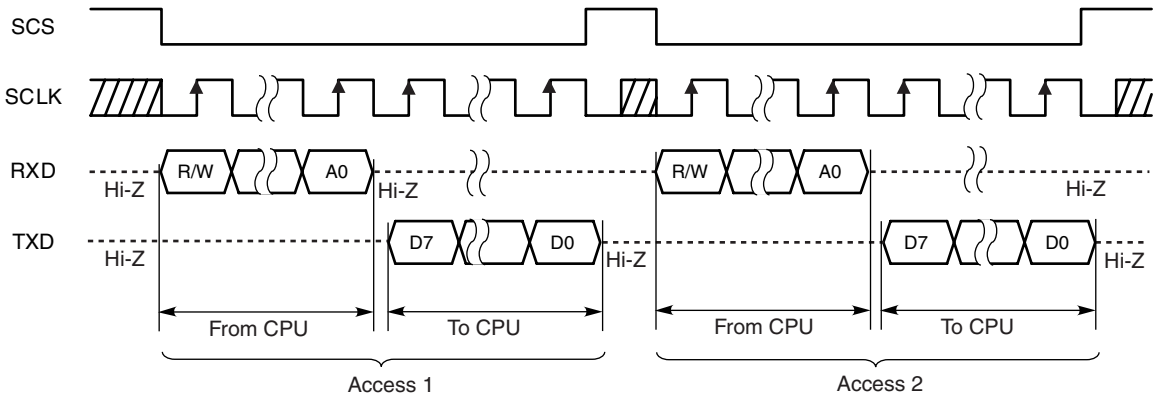


Figure 3-9 Host CPU Access Formats (Continuous Access)

(a) Write access



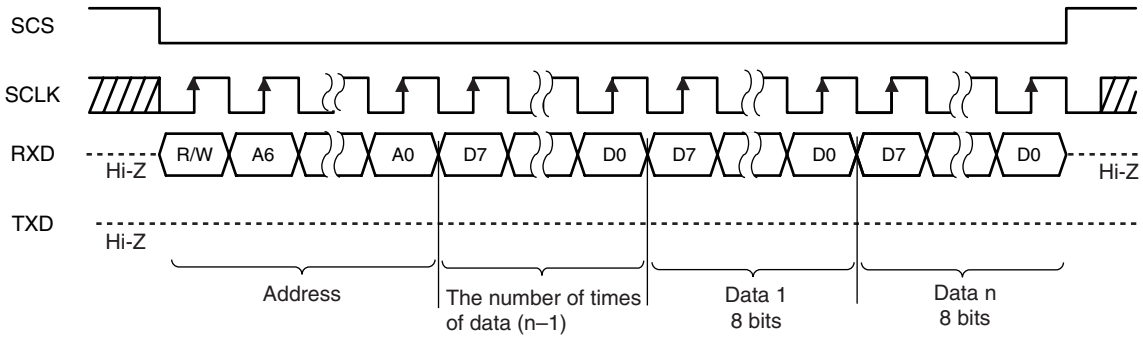
(b) Read access



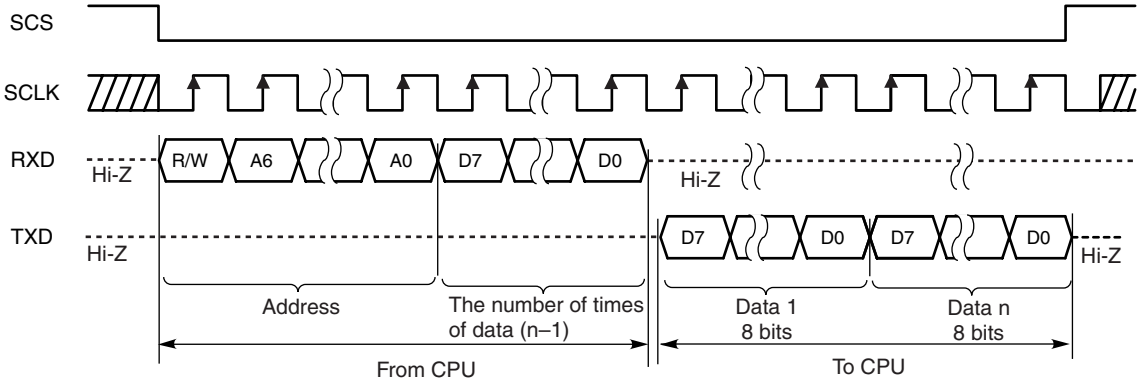
Remark The above formats are used except when accessing FIFOs in the sound generator.

Figure 3-10 Host CPU Access Formats (Continuous Access 2)

(a) Write Access



(b) Read Access



Remark The above formats are used except when accessing FIFOs in the sound generator.

3.2.5 Initialization of serial interface

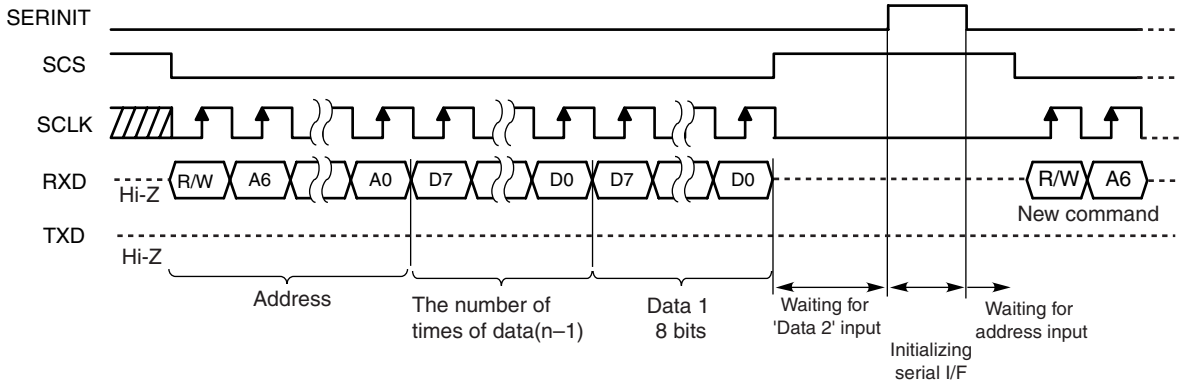
The SERINIT (D0) pin is an initialization signal for the serial I/F and is used for compulsory initialization of the serial I/F during write/read continuous access. (Therefore, this pin is normally used at low level if compulsory initialization is unnecessary)

The compulsory initialization operates only the serial I/F and is asynchronously performed by SCS = 1 and SERINIT = 0. On the other hand the registers in the sound generator and chip control are not initialized. Therefore the serial I/F wait for a new address to be input after initialization.

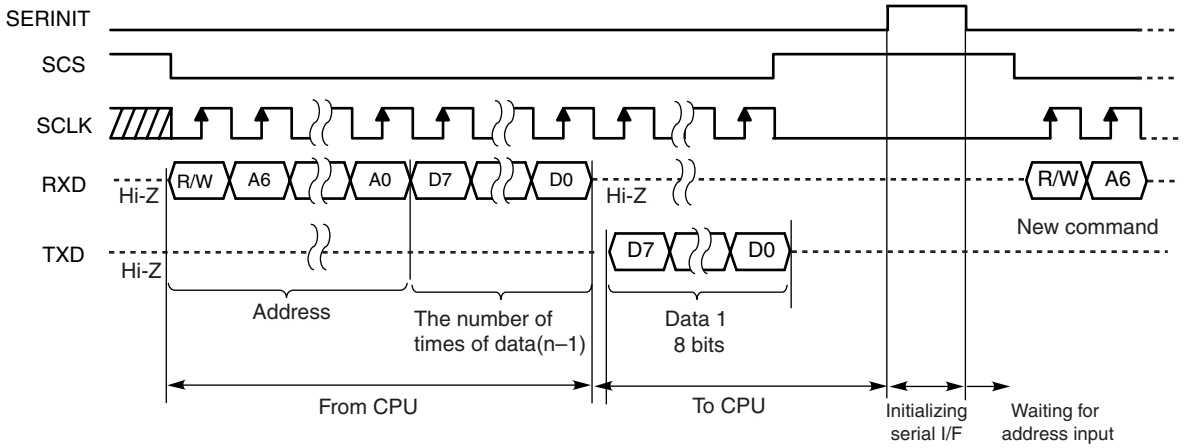
An example of this initialization signal is shown below.

Figure 3-11 Canceling Continuous Access Using SERINT (D0) Pin

(a) Write Access



(b) Read Access



Remark The initialization conditions in 3 / 4 -wire mode are the same.

4. MUSIC SERIAL INTERFACE

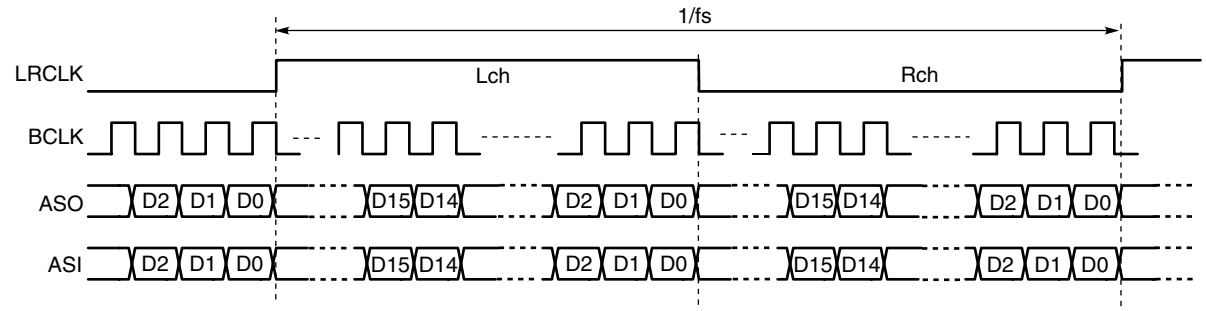
4.1 Audio Serial Interface (ASIO)

When LRCLK = 0 in the SEL_ASI register, L-ch data is assigned during the high-level period of LRCLK and R-ch data is assigned during the low-level period of LRCLK. For IIS format, this is reversed, in which case LRCLK =1 should be set.

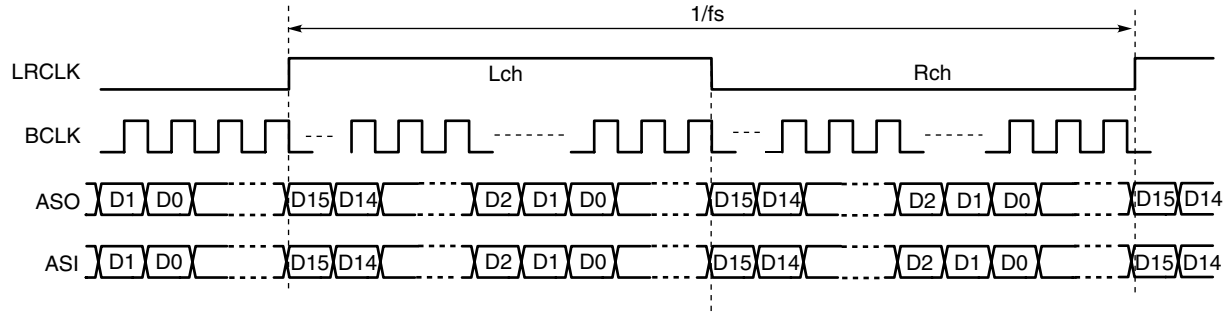
Within each of these periods, the format can be switched among right justified, left justified, and IIS format. Selection of master mode or slave mode is also enabled. The number of data bits per frame can be set via the BFS [4:0] bits in the SEL_FS register. The serial input/output timing is shown below.

Figure 4-1 Audio Serial Interface Timing

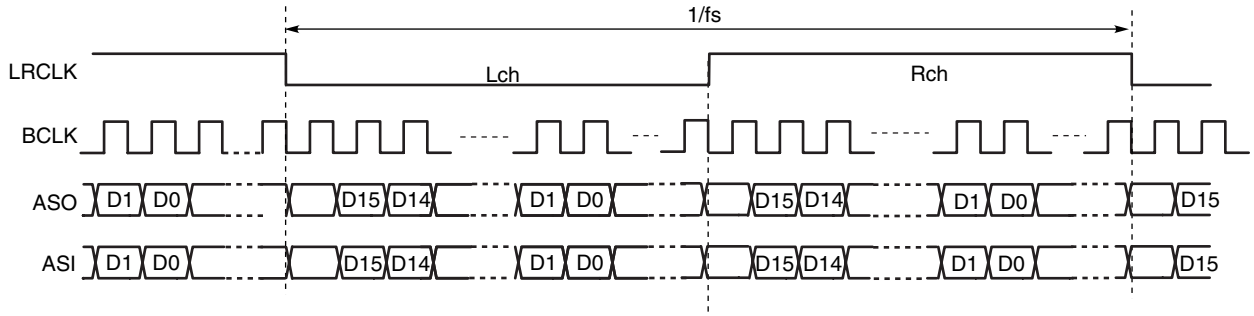
(a) Right-Justified Format



(b) Left-Justified Format



(c) IIS Format



Cautions 1. The IIS format is left justified with one empty bit and sets L-ch to low level and R-ch to high level. Do not specify other settings when selecting IIS mode (ASIM =1 in SEL_ASI register). When selecting LR mode (ASIM = 0 in SEL_ASI register), left or right justification can be selected in combination with normal or reversed left-right format.

2. The number of data bits per frame can be set via BFS [4:0] bits in the SEL_FS register. In master mode, either 64 bits or 32 bits can be selected. In slave mode, any value between 32 bits and 64 bits can be selected in two bits increments. After a reset is cleared, the default frame configuration setting 64 bits in total (32 bit for L-ch and 32 bits for R-ch).

4.2 Serial Interface Dedicated to Sound Generator Core External Connection (MSIO)

This is a serial interface dedicated to the connection between the sound generator core embedded in the μPD9971 and external application chips. Effects have so far been processed in the sound generator core. With this interface, however, external application chips can control effects. Regarding data formats, only the IIS format is supported.

The figures below show the timing of serial input/output. Mode settings, bit-width settings, and the use of inverted bit-clocks can be achieved by the changing of registers.

Figure 4-2 Frame Synchronous Mode (SMEN = 0), Normal MBCLK (SMBCLK = 0), Bit Width 128 (MBFS = 128), and 8 Channels (MCH = 8)

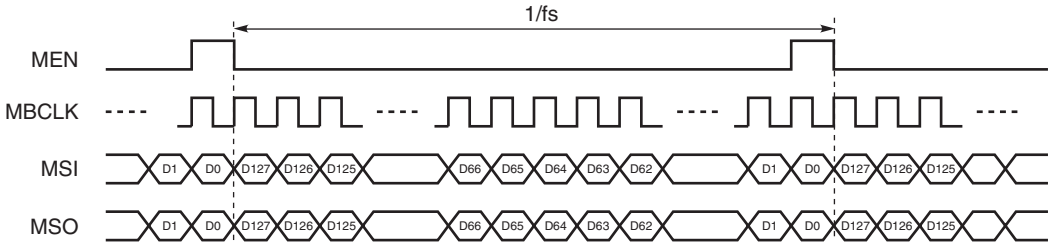


Figure 4-3 Frame Synchronous Mode (SMEN = 0), Inverted MBCLK (SMBCLK = 1), Bit Width 128 (MBFS = 128), and 8 Channels (MCH = 8)

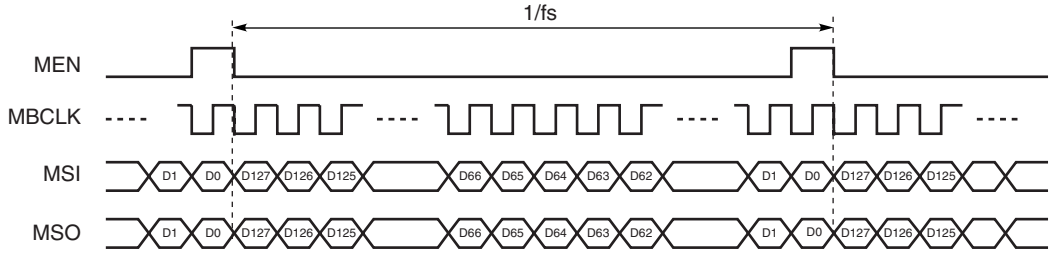
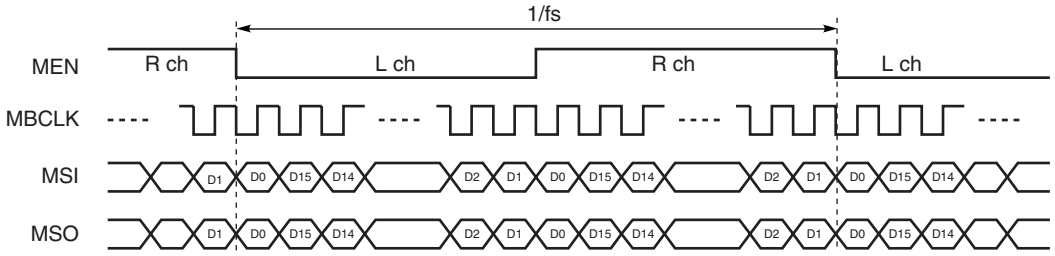


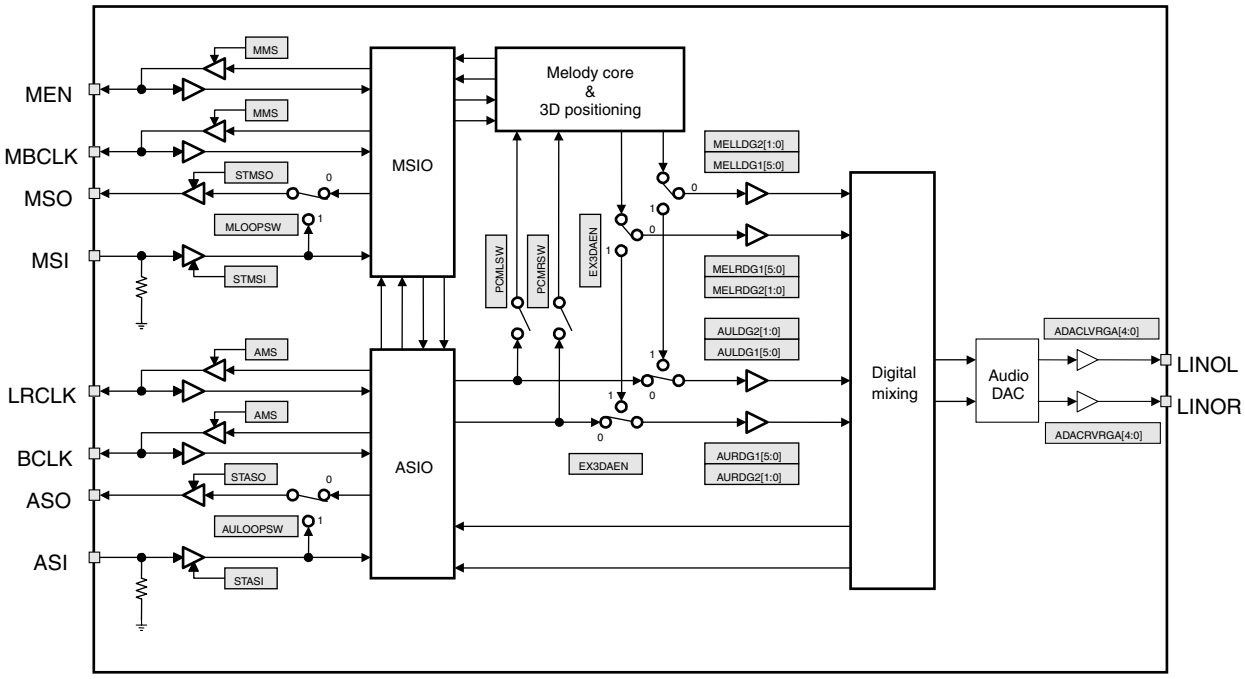
Figure 4-4 LR Stereo Mode (SMEN = 1), Inverted MBCLK (SMBCLK = 1), Bit Width 32 (MBFS = 32), and 2 Channels (MCH = 2)



Cautions 1. Data sizes that can be set vary depending on the master mode or the slave mode.
In the master mode, MBFS is only 32, 64, 128, or 256 fs.
In the slave mode, MBFS can be selected within a range from 32 to 256 bits, in 32 fs increments.
2. When MSIO and ASIO are used at the same time, ASIO can be set to the master mode only (BFS = 32 or 64 fs).

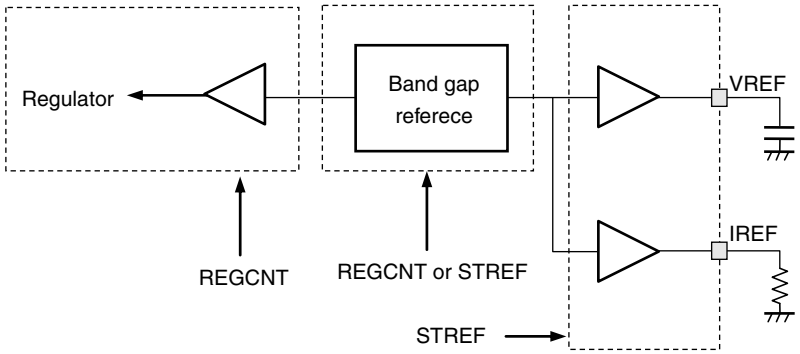
5. BLOCK FUNCTIONS

Figure 5-1 Details Of Signal Paths



5.1 Reference Voltage and Current Source Block

Figure 5-2 Voltage and Current Source



This block has the following functions:

- Generates reference voltage by using a band gap and supplies the voltage to analog circuits, PLL, and the regulator.
- Generates reference current by using the reference voltage as well as an external resistor and supplies the current to PLL, the regulator, and all analog circuits.
- Receives power supply from AV_{DD}.

The standby control of this block is controlled by the STNBY register.

To assert the internal regulator, reference voltage supplied from a part of this block is required. The REGCNT pin controls the supply of the reference voltage. Thus, when using the regulator, be sure to supply 3.0 V power to both $REGV_{DD}$ and AV_{DD}.

The normal mode is set within 5 ms after this block is started (standby is released).

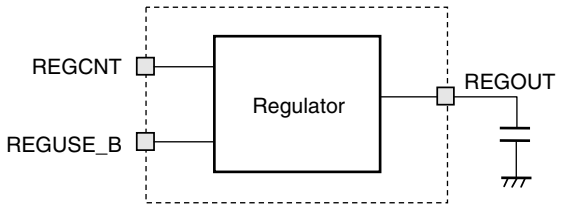
Cautions 1. Be sure to connect a 0.22 μF (± 20 %) capacitor between the VREF pin and AGND. Since capacitors with the above capacitance affect the analog characteristics of the μPD9971, place the capacitor as close as possible to the VREF pin. Do not connect any other capacitors to the VREF pin.

2. Be sure to connect a 56 kΩ (± 5 %) resistor between the IREF pin and AGND. Do not connect any other resistors to the IREF pin.

3. Note that output may be unstable if another analog block is started before this block is set to the normal mode.

5.2 Regulator Block

Figure 5-3 Regulator



This block has the following functions:

- Generates fixed voltage with the regulator and supplies current to the power supply DV_{DD} pin for digital circuits.
- Requires a short between the regulator output REGOUT pin and the DV_{DD} pin, which must be done at the outside of the μPD9971, when the regulator is used.
- Sets the regulator output to the low level when the regulator is not used.
- Receives power supply from $REGV_{DD}$.
- Requires a supply of 3.0 V power to $REGV_{DD}$ to check that the regulator is not used, even when the regulator is not used.

This block can be used when the REGUSE_B pin is set to the low level (DGND). When this block is not used, set the REGUSE_B pin to the high level (EV_{DD}).

While the REGUSE_B pin is set to the low level, this block starts supplying current if the REGCNT pin is set to the high level, and stops it if the REGCNT pin is set to the low level.

Table 5-1 Setting Of Pins When Regulator Is Used/Is Not Used

Pin	Pin Status	
	When regulator is not used	When regulator is used
$REGV_{DD}$	3.0 V external power supply	3.0 V external power supply
REGOUT	Left open (Output: Low)	Shorted with DV_{DD}
DV_{DD}	Connected to 1.54 V external power supply	Shorted with REGOUT
REGCNT	Shorted with DGND	High: Regular standby is canceled.
		Low: Regular standby
REGUSE_B	Shorted with EV_{DD}	Shorted with DGND

Cautions 1. Be sure to connect a 2.2 μF (± 20 %) capacitor between the REGOUT pin and AGND. Since capacitors with the above capacitance affect the noise characteristics of the regulator, place the capacitor as close as possible to the REGOUT pin. Do not connect any other capacitors to the REGOUT pin.

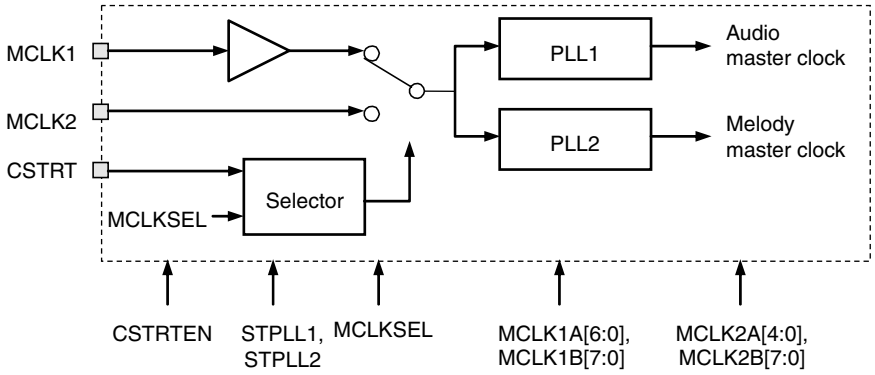
2. Be sure to connect a 0.1 μF (± 20 %) capacitor between the $REGV_{DD}$ pin and AGND.

3. Note that output may be unstable if a digital block is started before this block is set to the normal mode.

4. To charge the capacitor connected to the REGOUT pin, about 350 mA of through current flows into the capacitor for about 50 μs. when the regulator is started. Contact NEC Electronics if charging causes problems.

5.3 PLL Block

Figure 5-4 PLL



This block has the following functions:

- Divides or multiplies clocks input from the outside (which is done by the setting of registers) and generates the sound generator master clock as well as the audio master clock.
- Selects either the MCLK1 or MCLK2 pin as the clock input pin by using an internal register MCLKSEL or an external pin CSTRT. (Selection using the CSTRT pin is a special mode. Normally, use the MCLKSEL register.)
- Requires a setting, CSTRTEN bit = high, for validating the selection using the CSTRT pin.
- Inputs the MCLK2 pin to the EV_{DD} level because the pin uses external digital signals as clocks.
- Receives power supply from $PLLV_{DD}$.

This block generates the audio master clock when the STPLL1 bit is set to the high level, and the sound generator block master clock when the STPLL2 bit is set to the high level. Each master clock requires the setting of a division ratio by MCLK1A, MCLK1B, MCLK2A, and MCLK2B registers. The setting has to be performed in accordance with the input frequency and the sampling frequency.

When the CSTRTEN bit is set to the low level, and when the MCLKSEL bit is set to the low level, the MCLK1 pin is selected as the clock input pin. In this case, if the MCLKSEL bit is set to the high level, the MCLK2 pin is selected.

When the CSTRTEN bit is set to the high level, and when a specific division ratio is set, a special mode in which clock input pins are switched by an external pin CSTRT is enabled. For details of the special mode, contact NEC Electronics.

Normally, use the MCLKSEL register to perform the switching.

Table 5-2 SWITCHING OF CLOCKS BY REGISTERS

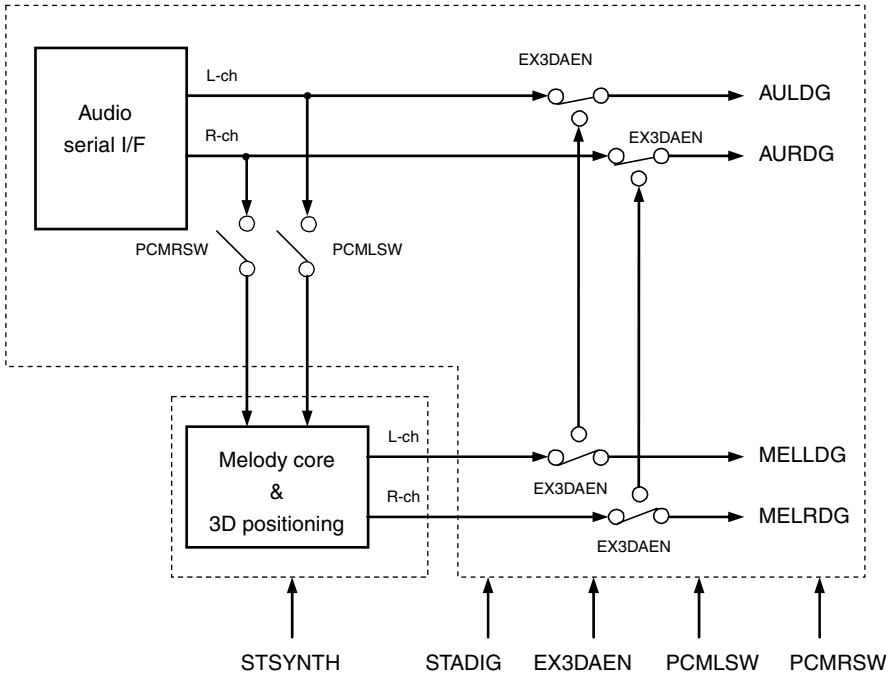
CSTRTEN	MCLKSEL	CSTRT	Clock Selection
Low	High	Don't care	Selects MCLK2 as clock input pin.
Low	Low	Don't care	Selects MCLK1 as clock input pin.
High	Don't care	High	Selects MCLK1 as clock input pin. (Fixed at 15.36 MHz.)
High	Don't care	Low	Selects MCLK2 as clock input pin. (Fixed at 12.00 MHz.)

Cautions 1. For this block to operate, the reference voltage source and reference current source blocks must be set to the normal mode.

2. The reference voltage source and reference current source blocks are set to the normal mode in 5 ms after the standby is released.

5.4 Sound Generator Core (Sound Generator/3D Positioning/Equalizer) Interface Block

Figure 5-5 Sound Generator Core



This block has the following functions:

- Can perform surround processing of PCM data input from ASI, when the sampling frequency is 32 kHz.
- Needs to be set to the expansion 3DA mode (the EX3DAEN bits = high) to perform surround processing of PCM data input from ASI, when the sampling frequency is 44.1 kHz.
- Switches the output destination of surround-processed data from the MELLDG or MELRDG block to the AULDG or AURDG block, when the expansion 3DA mode is selected.
- Receives power supply from DV_{DD}.

In this block, the audio serial interface operates when STADIG = high.
In this block, the sound generator core block operates when STSYNTH = high.

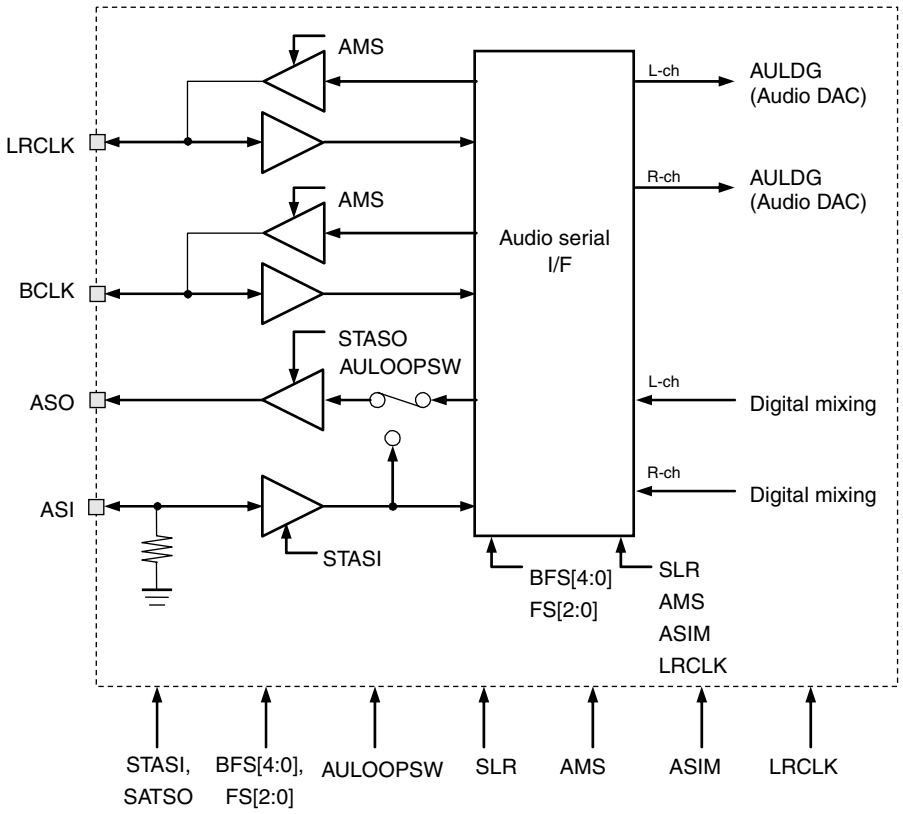
The table below shows the selection and addition of audio data that goes through surround processing.

Table 5-3 Selection of Data Going Through Surround Processing

Block	Set Address	Adjustable Range
PCMLSW	0BH	Mute, ASI input
PCMRSW	0BH	Mute, ASI input

5.5 Audio Serial Interface Block (ASIO)

Figure 5-6 Audio Serial Interface



This block has the following functions:

- Converts serial data input from ASI into parallel data, and outputs the data to the Audio DAC block.
- Converts parallel data input from the Digital Mixing block into serial data, and outputs the data from ASO.
- Selects a sampling frequency from among 8, 16, 32 (default), 44.1, and 48 kHz according to the register setting.
- Can change the frequency of BCLK (default: 64 fs) by setting the register.
- Can perform loop back between ASI and ASO by setting the register.
- Can select the right-justified (default) or left-justified data format by setting the register.
- Can select the slave (default) or master mode by setting the register.
- Can select the LR (default) or IIS mode by setting the register.
- Can invert LRCLK by setting the register.
- Receives power supply from DV_{DD}.

This block operates according to the STASI and STASO register settings. For details, refer to **Table 5-4**.

Table 5-4 Pin Statuses In ASIO Block

Pin	Pin Function	AMS = 0 (Slave Mode)				AMS = 1 (Master Mode)			
		(STASI, STASO)				(STASI, STASO)			
		(0, 0)	(1, 1)	(1, 0)	(0, 1)	(0, 0)	(1, 1)	(1, 0)	(0, 1)
BCLK	Bit synchronization I/O for audio	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
LRCLK	Frame synchronization I/O for audio	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
ASI	Audio serial data input	–	Input	Input	–	–	Input	Input	–
ASO	Audio serial data output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output

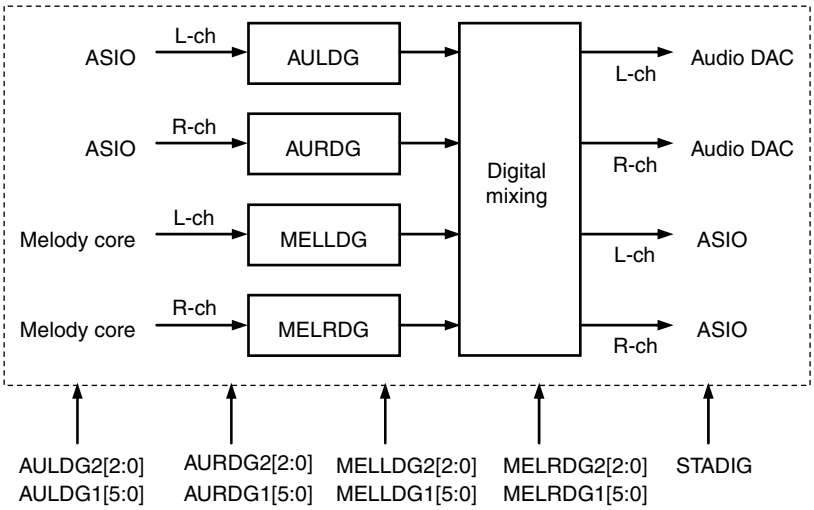
Cautions 1. For this block to operate, the PLL block has to be operating.

2. Set the LRCLK and SLR registers to the high level when selecting the IIS mode.

3. To perform surround processing of data input from ASI, set the sampling frequency at 32 or 44.1 kHz.

5.6 Audio Playback and Digital Gain Adjustment Block

Figure 5-7 Audio Playback and Digital Gain Adjustment Block



This block has the following functions:

- Performs digital gain adjustment for sampling stereo linear PCM formats of 8, 16, 32, 44.1, and 48 kHz that are digitally input from the audio serial interface.
- Performs digital gain adjustment for the sampling stereo linear PCM format of 32 kHz that is digitally input from the sound generator.
- Digitally mixes the signals that have gone through the above gain adjustment.
- Outputs the digitally mixed signals to the Audio DAC and audio serial interface blocks.
- Receives power supply from DV_{DD}.

This block operates when the STADIG register is set to the high level. In the gain adjustment block, multiplying the each digital input signal by a coefficient performs gain adjustment. Performing gradual change of gains realizes soft mute functions that minimize unusual noise.

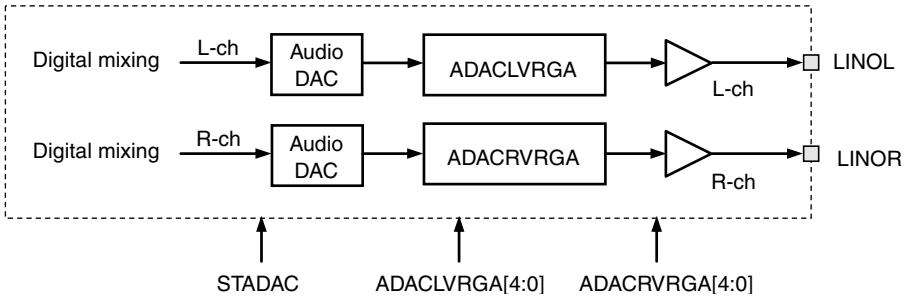
Table 5-5 Digital Gain Adjustment

Block	Set Address	Adjustable Range
AULDG	13H	Mute, +12 dB to 0 dB to −63 dB in 1 dB increments
AURDG	14H	Mute, +12 dB to 0 dB to −63 dB in 1 dB increments
MELLDG	11H	Mute, +12 dB to 0 dB to −63 dB in 1 dB increments
MELRDG	12H	Mute, +12 dB to 0 dB to −63 dB in 1 dB increments

Caution For this block to operate, PLL has to be operating stably.

5.7 Audio Playback Analog Block

Figure 5-8 Audio Playback Analog Block



This block has the following functions:

- Performs D/A conversion of digital signals that are output from the Digital Mixing block (the conversion is done in Audio DAC), and then performs analog gain adjustment for the output analog signals.
- Outputs the signals that have gone through the gain adjustment from the LINEOL and LINEOR pins (line output).
- Receives power supply from AV_{DD}.

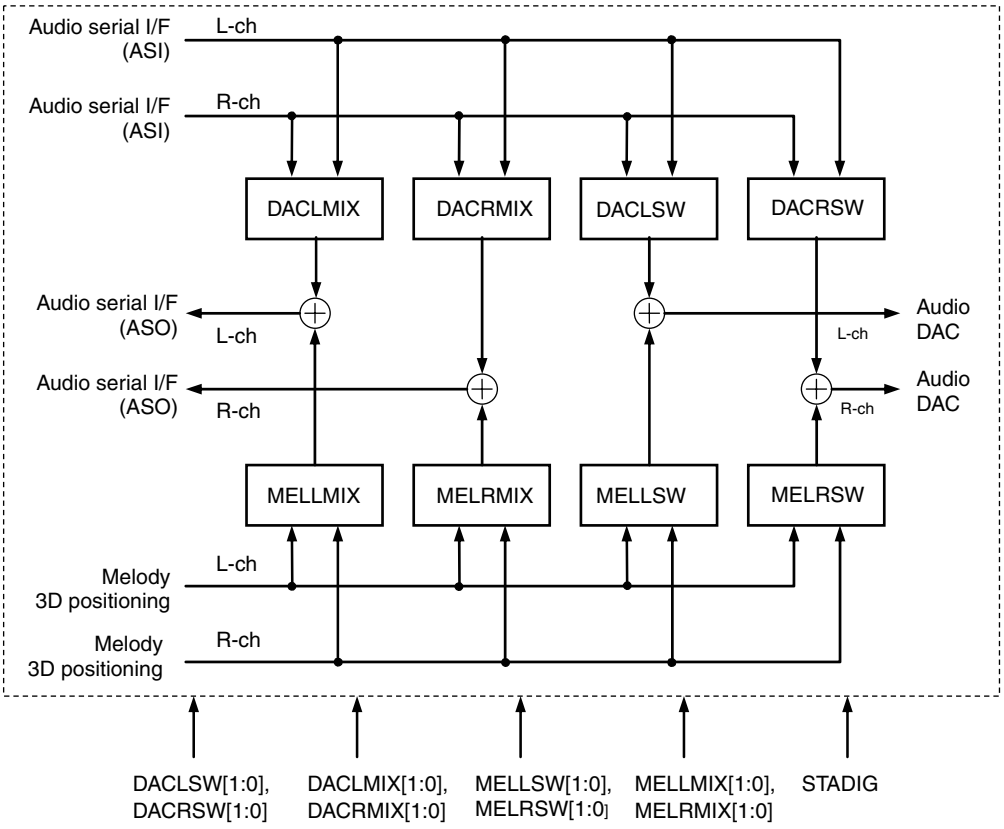
This block operates when the STADAC bit is set to the high level. In the gain adjustment block, gain adjustment for audio DAC output is performed in analog circuits. L-ch and R-ch gains can be set individually.

Table 5-6 Analog Gain Adjustment

Block	Set Address	Adjustable Range
ADACLVRGA	17H	Mute, 0 dB to –45 dB in 1.5 dB increments
ADACRVRGA	18H	Mute, 0 dB to –45 dB in 1.5 dB increments

5.8 Digital Mixing Block

Figure 5-9 Digital Mixing Block



This block has the following functions:

- Mixes digital signals input from the audio serial interface and output from the sound generator. (The mixing can be performed only when the fs = 32 kHz.)
- Outputs the mixed digital data to the ASIO and Audio DAC blocks.
- Equipped with selectors to select channels. The selector names and the selectable channels are as follows: Through (L-ch → L-ch and R-ch → R-ch); Channel inversion (L-ch → R-ch and R-ch → L-ch); Monaural (L-ch → L-ch + R-ch and R-ch → L-ch + R-ch); Mute (L-ch → no output and R-ch → no output). In the case of the monaural selector, first, the L-ch and R-ch are divided by two then added.
- Receives power supply from DV_{DD}.

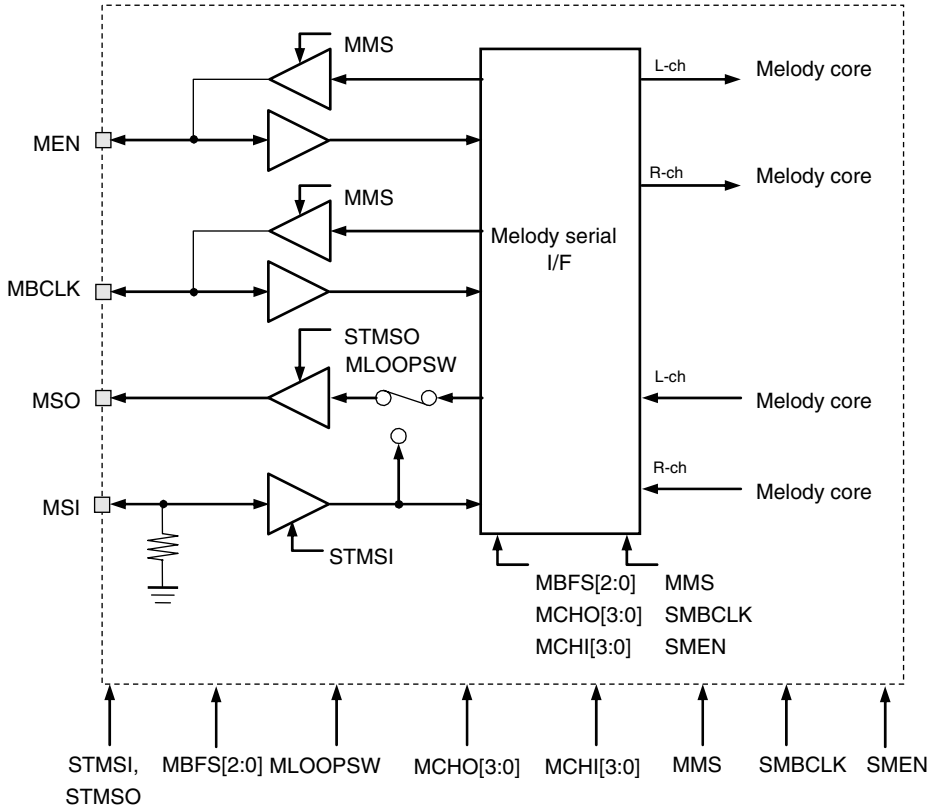
This block operates when the STADIG bit is set to the high level.

Table 5-7 Selector Setting

Block	Initial Setting	Path to be Set
DACLSW	Through	Path between ASI and Audio DAC
DACRSW	Through	Path between ASI and Audio DAC
MELLSW	Through	Path between sound generator and Audio DAC
MELRSW	Through	Path between sound generator and Audio DAC
DACLMIX	Mute	Path between ASI and ASO
DACRMIX	Mute	Path between ASI and ASO
MELLMIX	Mute	Path between sound generator and ASO
MELRMIX	Mute	Path between sound generator and ASO

5.9 Serial Interface Dedicated to Sound Generator Core External Connection (MSIO)

Figure 5-10 Serial Interface Dedicated to Sound generator Core External Connection



This block has the following functions:

- Converts serial data input from MSI into parallel data, and outputs the parallel data to the sound generator core block.
- Converts parallel data input from the sound generator core block into serial data, and outputs the serial data from MSO.
- Has a fixed sampling frequency of 32 kHz.
- Can change the frequency of MBCLK (default: 64 fs) by setting the register.
- Can set the number of valid data items in MSI input data and MSO output data individually by setting the register.
- Can perform data loop back between MSI and MSO by setting the register.
- Can select the slave (default) or master mode by setting the register.
- Can select the frame synchronous (default) or LR stereo mode by setting the register.
- Can invert the MBCLK bit clock by setting the register.
- Receives power supply from DV_{DD}.

This block operates according to the STMSI and STMSO register settings. For details, refer **Table 5-8.**

Table 5-8 Pin Statuses in MSIO Block

Pin	Pin Function	MMS = 0 (Slave Mode)				MMS = 1 (Master Mode)			
		(STMSI, STMSO)				(STMSI, STMSO)			
		(0, 0)	(1, 1)	(1, 0)	(0, 1)	(0, 0)	(1, 1)	(1, 0)	(0, 1)
MBCLK	Bit synchronization I/O for PCM sound generator-core	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
MEN	Frame synchronization I/O for PCM sound generator-core	Input (Internal: Low)	Input	Input	Input	Low	Output	Output	Output
MSI	PCM sound generator-core serial data input	–	Input	Input	–	–	Input	Input	–
MSO	PCM sound generator-core serial data output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output

Cautions 1. As in the case of ASIO, MSIO can operate in the slave or master mode.
When ASIO and MSIO are used at the same time, the frame signals in the μPD9971 need to be integrated. Accordingly, ASIO can be used in the master mode only.

2. Below are the restrictions that are applied depending on use conditions.

(1)When only ASIO set to the master mode is used, the setting value of BFS must be only 64 fs or 32 fs.

(2)When only MSIO set to the master mode is used, the setting value of MBSF must be selected from among 32 fs, 64 fs, 128 fs, and 256 fs.

(3)When both ASIO and MSIO are used, ASIO can be used only if it is set to the master mode.

(4)In all of the above cases, the setting of invalid values to BFS or MBFS results in the application of default values.

6. REGISTERS (CONTROL REGISTER BANK)

Below are the descriptions of registers of the Control register bank. It is not possible to write to registers except those specified in the table below.

Table 6-1 Chip Control Registers

Add.	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function	Reg Name
00H	R/W	STADIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STADAC	STREF	00H	LSI Standby	STNBY
01H	R/W	0	MCLK1A[6:0]							1CH	Master clock 1	MCLK1A
02H	R/W	MCLK1B[7:0]								80H	Master clock1	MCLK1B
03H	R/W	0	0	0	MCLK2A[4:0]					02H	Master clock2	MCLK2A
04H	R/W	MCLK2B[7:0]								2AH	Master clock2	MCLK2B
05H	R/W	0	0	0	0	0	0	CSTRTEN	MCLKSEL	00H	Clock switching	MCLKSEL
06H	R/W									xx	Reserved	Reserved
07H	R/W	BFS[4:0]					FS[2:0]			00H	FS,BCLK select	SEL_FS
08H	R/W	0	0	EX3DAEN	AULOOPSW	SLR	AMS	ASIM	LRCLK	00H	ASI	SEL_ASI
09H	R/W	DACLMIX[1:0]		DACRMIX[1:0]		DACLSW[1:0]		DACRSW[1:0]		F0H	Mixing path1	MIXING1
0AH	R/W	MELLMIX[1:0]		MELRMIX[1:0]		MELLSW[1:0]		MELRSW[1:0]		F0H	Mixing path2	MIXING2
0BH	R/W	0	0	0	0	0	PCMLSW	0	PCMRSW	00H	Mixing path3	MIXING3
0CH	R/W									xx	Reserved	Reserved
0DH	R/W	0	0	0	0	0	0	VIB	LED	00H	LED,VIB control output	LEDVIB
0EH	R/W	0	0	0	0	POUT3	POUT2	POUT1	POUT0	00H	Port output external output	POUT
0FH	R/W										Reserved	Reserved
10H	R/W	0	0	0	0	SLOPE[1:0]		AUSMUTE	MELSMUTE	00H	Soft mute	SMUTE
11H	R/W	MELLDG2[1:0]		MELLDG1[5:0]						FFH	ADAC digital gain/path	MELLDG
12H	R/W	MELRDG2[1:0]		MELRDG1[5:0]						FFH	ADAC digital gain/path	MELRDG
13H	R/W	AULDG2[1:0]		AULDG1[5:0]						FFH	ADAC digital gain/path	AULDG
14H	R/W	AURDG2[1:0]		AURDG1[5:0]						FFH	ADAC digital gain/path	AURDG
15H	R/W										Reserved	Reserved
16H	R/W										Reserved	Reserved
17H	R/W	0	0	0	ADACLVRGA[4:0]					1FH	ADAC analog gain	ADACLVR
18H	R/W	0	0	0	ADACRVRGA[4:0]					1FH	ADAC analog gain	ADACRVR
20H	R/W	0	0	0	0	0	0	STMSI	STMSO	00H	LSI standby for MSIO	STNBY2
21H	R/W	0	MBFS[2:0]			MLOOPSW	MMS	SMEN	SMBCLK	10H	MSIO	SEI_MSIO1
22H	R/W	MCHI[3:0]				MCHO[3:0]				33H	MSIO	SEL_MSIO2
3FH	R	1	0	1	1	VER[3:0]				xx	LSI version[Note]	LSIVER
7CH	R/W	0	0	0	0	0	0	BANK1	BANK0	00H	BANK exchange	BANK

Note Serial mode only, **Remark** xx: Undefined

6.1 Standby Setting (STNBY)

This register performs the setting for standby.

Address: 00H, register name: STNBY, block: whole block, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
STADIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STADAC	STREF

6.1.1 STADIG

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for audio digital block
1	ON		Normal operation

6.1.2 STPLL2

During the standby mode, clock signals output from PLL2 are not supplied.

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for PLL2
1	ON		Normal operation

6.1.3 STPLL1

During the standby mode, clock signals output from PLL1 are not supplied.

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for PLL1
1	ON		Normal operation

6.1.4 STASI

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for ASI (audio serial interface input)
1	ON		Normal operation

6.1.5 STASO

LRCLK and BCLK operate in the standby mode only when both the STASI and STASO bits have been set for standby. For details, refer to **Table 5-4 Pin Statuses In ASIO Block**

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for ASO (audio serial interface output)
1	ON		Normal operation

6.1.6 STSYNTH

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for sound generator block (Synthesizer)
1	ON		Normal operation

6.1.7 STADAC

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for Audio DAC block
1	ON		Normal operation

6.1.8 STREF

During the standby mode, the reference voltage and reference current are not supplied to PLL not to all of the analog blocks. Make sure that the ON mode is selected when the μPD9971 is used.

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for reference voltage/reference current in the analog block
1	ON		Normal operation

6.2 Master Clock Switching (MCLK1A, MCLK1B, MCLK2A, and MCLK2B)

These registers are for the settings for the master clocks, refer to **6.3.2 (2) Setting the master clock PLL2 for Sound generators**.

Address: 01H, register name: MCLK1A, block: PLL1, access: R/W, initial value: 1CH

D7	D6	D5	D4	D3	D2	D1	D0
0	MCLK1A[6:0]						

Address: 02H, register name: MCLK1B, block: PLL1, access: R/W, initial value: 80H

D7	D6	D5	D4	D3	D2	D1	D0
MCLK1B[7:0]							

Address: 03H, register name: MCLK2A, block: PLL2, access: R/W, initial value: 02H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	MCLK2A[4:0]				

Address: 04H, register name: MCLK2B, block: PLL2, access: R/W, initial value: 2AH

D7	D6	D5	D4	D3	D2	D1	D0
MCLK2B[7:0]							

6.2.1 MCLK1A[6:0]

Data	Mode	Initial Value	Description
MCLK1A[6:0]		1Ch	Sets PLL1 used for generating the audio master clock.

6.2.2 MLCK1B[7:0]

Data	Mode	Initial Value	Description
MCLK1B[7:0]		80h	Sets PLL1 used for generating the audio master clock.

6.2.3 MCLK2A[4:0]

Data	Mode	Initial Value	Description
MCLK2A[4:0]		02h	Sets PLL2 used for generating the sound generator master clock.

6.2.4 MCLK2B[7:0]

Data	Mode	Initial Value	Description
MCLK2B[7:0]		2Ah	Sets PLL2 used for generating the sound generator master clock.

6.3 Selecting Input Clock (MCLKSEL)

This register selects the clock input pin.

Address: 05H, register name: MCLKSEL, block: PLL, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CSTRTEN	MCLKSEL

6.3.1 MCLKSEL

Be sure to leave the clock selection pin (CSTRT) open or fix it to the low level (a pull-down resister is contained) when clock input pins are switched by registers.

Data	Mode	Initial Value	Description
0	MCLK1 input	0	Selects MCLK1 as the clock input pin.
1	MCLK2 input		Selects MCLK2 as the clock input pin.

6.3.2 CSTRTEN

Use the MCLKSEL register for normal switching (In this case, the default setting is CSTRTEN = 0.).

Data	Mode	Initial Value	Description
0	CSTRT invalidation	0	Uses the MCLKSEL register for switching clock input pins.
1	CSTRT validation		Uses the CSTRT pin for switching clock input pins.

(1) Setting the master clock PLL1 for audio blocks

When clock input pins are switched by the CTSRT pin, only limited frequencies can be used. The relationships between the frequencies and the pins are as follows: 15.36 MHz for MCLK1 and 12.00 MHz for MCLK2.

Table 6-2 When Switching Is Not Done By the CSTRT Pin (CSTRTEN = 0)

Input Frequency [MHz]	MCLK1A		MCLK1B		Error [%]	Master Frequency (Except Frequency for Sound generator) [MHz]
	Dec.	HEX	Dec.	HEX		
3.840	20	14H	128	80H	0.0000	24.57600
5.376 (default)	28	1CH	128	80H	0.0000	24.57600
12.000	75	4BH	154	9AH	0.2604	24.64000
12.600	81	51H	158	9EH	0.0072	25.57778
13.000	64	40H	121	79H	0.0086	24.57813
14.400	75	4BH	128	80H	0.0000	24.57600
15.360	96	60H	154	9AH	0.2604	24.64000

Table 6-3 When Switching Is Done By the CSTRT Pin (CSTRTEN = 1)

Input Frequency [MHz]	MCLK1A		MCLK1B		Error [%]	Master Frequency for Sound generator [MHz]
	Dec.	HEX	Dec.	HEX		
MCLK1 = 15.36 MHz MCLK2 = 12.00 MHz	75	4BH	154	9AH	0.2604	24.64000

(2) Setting the master clock PLL2 for Sound generators

When clock input pins are switched by the CSTRT pin, only limited frequencies can be used. The relationships between the frequencies and the pins are as follows: 15.36 MHz for MCLK1 and 12.00 MHz for MCLK2.

Table 6-4 When Switching Is Not Done By The CSTRT Pin (CSTRTEN = 0).

Input Frequency [MHz]	MCLK2A		MCLK2B		Error [%]	Master Frequency for Sound generator [MHz]
	Dec.	HEX	Dec.	HEX		
3.840	2	02H	59	3BH	0.4255	113.2800
5.376 (default)	2	02H	42	2AH	0.0851	112.8960
12.000	5	05H	47	2FH	0.0000	112.8000
12.600	5	05H	45	2DH	0.5319	113.4000
13.000	5	05H	44	2CH	1.4184	114.4000
14.400	6	06H	47	2FH	0.0000	112.8000
15.360	6	06H	44	2CH	0.1418	112.6400

Table 6-5 When Switching Is Done By The CSTRT Pin (CSTRTEN = 1).

Input Frequency [MHz]	MCLK2A		MCLK2B		Error [%]	Master Frequency for Sound generator [MHz]
	Dec.	HEX	Dec.	HEX		
MCLK1 = 15.36 MHz MCLK2 = 12.00 MHz	25	19H	234	EAH	0.4255	112.3200

6.4 FS Switching and BCLK Switching for ASIO (SEL_FS)

This register sets the ASI sampling rate and the frequency of BCLK.

Address: 07H, register name: SEL_FS, block: ASIO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
BFS[4:0]					FS[2:0]		

6.4.1 FS[2:0]

Data	Mode	Initial Value	Description
000b	32 kHz	000b	Sets ASIO sampling rate at 32 kHz.
001b	44.1 kHz		Sets ASIO sampling rate at 44.1 kHz.
010b	48 kHz		Sets ASIO sampling rate at 48 kHz.
100b	8 kHz		Sets ASIO sampling rate at 8 kHz.
101b	16 kHz		Sets ASIO sampling rate at 16 kHz.

Caution Do not set data items other than the above.
When MSIO is used (STMSI or STMSO = 1), the sampling rate is forcedly set at 32 kHz (the default value).

6.4.2 BFS[4:0]

Data	Mode	Initial Value	Description
00h	64 fs	00H	Sets BCLK frequency at 64 fs (This can be done in master mode.).
01h	62 fs		Sets BCLK frequency at 62 fs.
02h	60 fs		Sets BCLK frequency at 60 fs.
03h	58 fs		Sets BCLK frequency at 58 fs.
04h	56 fs		Sets BCLK frequency at 56 fs.
05h	54 fs		Sets BCLK frequency at 54 fs.
06h	52 fs		Sets BCLK frequency at 52 fs.
07h	50 fs		Sets BCLK frequency at 50 fs.
08h	48 fs		Sets BCLK frequency at 48 fs.
09h	46 fs		Sets BCLK frequency at 46 fs.
0Ah	44 fs		Sets BCLK frequency at 44 fs.
0Bh	42 fs		Sets BCLK frequency at 42 fs.
0Ch	40 fs		Sets BCLK frequency at 40 fs.
0Dh	38 fs		Sets BCLK frequency at 38 fs.
0Eh	36 fs		Sets BCLK frequency at 36 fs.
0Fh	34 fs		Sets BCLK frequency at 34 fs.
10h	32 fs		Sets BCLK frequency at 32 fs (This can be done in master mode.).
18h	80 fs		Sets BCLK frequency at 80 fs.
1Ch	120 fs		Sets BCLK frequency at 120 fs.

Caution In the master mode (AMS = 1), only 64 fs (00H) and 32 fs (10H) can be set. If any other value is set, 64 fs is forcedly selected.
When MSIO and ASIO are used at the same time, ASIO is set to the master mode (BFS = 32 or 64 fs) only.

6.5 ASIO Mode Setting (SEL_ASI)

This register performs the setting for ASIO.

Address: 08H, register name: SEL_ASI, block: ASIO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	EX3DAEN	AULOOPSW	SLR	AMS	ASIM	LRCLK

6.5.1 EX3DAEN

Data	Mode	Initial Value	Description
0	OFF	0	Normal operation
1	ON		Reference clock (44.1 kHz) for 3DA surround

6.5.2 AULOOPSW

Data	Mode	Initial Value	Description
0	Normal mode	0	Normal operation
1	Loop back		Loop back mode for ASIO (ASI to ASO)

6.5.3 SLR

Data	Mode	Initial Value	Description
0	SR	0	Right-justified format for ASIO data
1	SL		Left-justified format for ASIO data

6.5.4 AMS

Data	Mode	Initial Value	Description
0	Slave	0	ASIO slave mode
1	Master		ASIO master mode

Caution When MSIO and ASIO are used at the same time, ASIO is forcedly set to the master mode (AMS = 1).

6.5.5 ASIM

Data	Mode	Initial Value	Description
0	LR	0	ASIO LR mode
1	IIS		ASIO IIS mode

6.5.6 LRCLK

Data	Mode	Initial Value	Description
0	L-ch	0	L-channel data when LRCLK is at high level.
1	R-ch		R-channel data when LRCLK is at high level.

Caution Set SLR = 1 and LRCLK = 1 when IIS mode is selected.
In slave mode (AMS = 0), external clock input is required.

6.6 Digital Mixing Path (ASI Input Data) Selection (MIXING1)

This register performs mixing setting (ASI to ASO or DAC).

Address: 09H, register name: MIXING1, block: Selector mixer, access: R/W, initial value: F0H

D7	D6	D5	D4	D3	D2	D1	D0
DACLMIX[1:0]		DACRMIX[1:0]		DACLSW[1:0]		DACLSW[1:0]	

6.6.1 DACLMIX[1:0]

Data	Mode	Initial Value	Description
00b	Through	11b	Outputs ASI L-ch input data to ASO L-ch.
01b	Cross		Outputs ASI R-ch input data to ASO L-ch (LR inverted).
10b	Monaural		Outputs ASI L/R-ch mixed input data to ASO L-ch (LR added and monaural).
11b	Mute		Mutes output from ASI L-ch input data to ASO L-ch.

6.6.2 DACRMIX[1:0]

Data	Mode	Initial Value	Description
00b	Through	11b	Outputs ASI R-ch output data to ASO R-ch.
01b	Cross		Outputs ASI L-ch output data to ASO R-ch (LR inverted).
10b	Monaural		Outputs ASI L/R-ch mixed output data to ASO R-ch (LR added and monaural).
11b	Mute		Mutes output from ASI R-ch output data to ASO R-ch.

6.6.3 DACLSW[1:0]

Data	Mode	Initial Value	Description
00b	Through	00b	Outputs ASI L-ch output data to DAC path L-ch.
01b	Cross		Outputs ASI R-ch output data to DAC path L-ch (LR inverted).
10b	Monaural		Outputs ASI L/R-ch mixed output data to DAC path L-ch (LR added and monaural).
11b	Mute		Mutes output from ASI L-ch output data to DAC path L-ch.

6.6.4 DACRSW[1:0]

Data	Mode	Initial Value	Description
00b	Through	00b	Outputs ASI R-ch output data to DAC path R-ch.
01b	Cross		Outputs ASI L-ch output data to DAC path R-ch (LR inverted).
10b	Monaural		Outputs ASI L/R-ch mixed output data to DAC path R-ch (LR added and monaural).
11b	Mute		Mutes output from ASI L/R-ch output data to DAC path R-ch.

6.7 Digital Mixing Path (Sound Generator Output Data) Selection (MIXING2)

This register performs mixing setting (sound generator to ASO or DAC).

Address: 0AH, register name: MIXING2, block: Selector mixer, access: R/W, initial value: F0H

D7	D6	D5	D4	D3	D2	D1	D0
MELLMIX[1:0]		MELRMIX[1:0]		MELLSW[1:0]		MELRSW[1:0]	

6.7.1 MELLMIX[1:0]

Data	Mode	Initial Value	Description
00b	Through	11b	Outputs sound generator L-ch output data to ASO L-ch.
01b	Cross		Outputs sound generator R-ch output data to ASO L-ch (LR inverted).
10b	Monaural		Outputs sound generator L/R-ch mixed output data to ASO L-ch (LR added and monaural).
11b	Mute		Mutes output from sound generator L-ch output data to ASO L-ch.

6.7.2 MELRMIX[1:0]

Data	Mode	Initial Value	Description
00b	Through	11b	Outputs sound generator R-ch output data to ASO R-ch.
01b	Cross		Outputs sound generator L-ch output data to ASO R-ch (LR inverted).
10b	Monaural		Outputs sound generator L/R-ch mixed output data to ASO R-ch (LR added and monaural).
11b	Mute		Mutes output from sound generator R-ch output data to ASO R-ch.

6.7.3 MELLSW[1:0]

Data	Mode	Initial Value	Description
00b	Through	00b	Outputs sound generator L-ch output data to DAC path L-ch.
01b	Cross		Outputs sound generator R-ch output data to DAC path L-ch (LR inverted).
10b	Monaural		Outputs sound generator mixed L/R-ch output data to DAC path L-ch (LR added and monaural).
11b	Mute		Mutes output from sound generator L-ch output data to DAC path L-ch.

6.7.4 MELRSW[1:0]

Data	Mode	Initial Value	Description
00b	Through	00b	Outputs sound generator R-ch output data to DAC path R-ch.
01b	Cross		Outputs sound generator L-ch output data to DAC path R-ch (LR inverted).
10b	Monaural		Outputs sound generator L/R-ch mixed output data to DAC path R-ch (LR added and monaural).
11b	Mute		Mutes output from sound generator L/R ch output data to DAC path R-ch.

6.8 Digital Mixing Path (ASI to Sound Generator) Selection (MIXING3)

This register performs mixing setting (sound generator to the ASO path).

Address: 0BH, register name: MIXING3, block: Selector mixer, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	PCMLSW	0	PCMRSW

6.8.1 PCMLSW

Data	Mode	Initial Value	Description
0	Mute	0	Mutes.
1	Through		Selects data (L-ch) from ASI.

6.8.2 PCMRSW

Data	Mode	Initial Value	Description
0	Mute	0	Mutes.
1	Through		Selects data (R-ch) from ASI.

6.9 VIB and LED Settings (LEDVIB)

This register performs setting for VIB and LED.

Address: 0DH, register name: LEDVIB, block: VB, LED, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	VIB	LED

6.9.1 VIB

Data	Mode	Initial Value	Description
0	OFF	0	Performs low-level output from LED pin.
1	ON		Performs high-level output from LED pin.

6.9.2 LED

Data	Mode	Initial Value	Description
0	OFF	0	Performs low-level output from LED pin.
1	ON		Performs high-level output from LED pin.

Remark For both VIB and LED, the register value is output to the output pin (LSI pin).

6.10 Setting of General-Purpose Output Pins (POUT)

This register performs setting for POUT.

Address: 0EH, register name: POUT, block: PO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	POUT3	POUT2	POUT1	POUT0

6.10.1 POUT0 to POUT3

Data	Mode	Initial Value	Description
0	LOW	0	Performs low-level output from the corresponding pin from PO0 to PO3.
1	HIGH		Performs high-level output from the corresponding pin from PO0 to PO3.

Remark While STADIG is set to standby mode, the POUT output retains the data value.

6.11 Audio Soft Mute Control (SMUTE)

This register controls soft mute.

Address: 10H, register name: SMUTE, block: Audio , access: R/W, initial value: 00h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SLOPE[1:0]		AUSMUTE	MELSMUTE

6.11.1 SLOPE[1:0]

Data	Mode	Initial Value	Description
00b	8 ms	00b	Sets soft mute cancel time at 8 ms (from –63 dB to 0 dB).
01b	16 ms		Sets soft mute cancel time at 16 ms (from –63 dB to 0 dB).
10b	24 ms		Sets soft mute cancel time at 24 ms (from –63 dB to 0 dB).
11b	32 ms		Sets soft mute cancel time at 32 ms (from –63 dB to 0 dB).

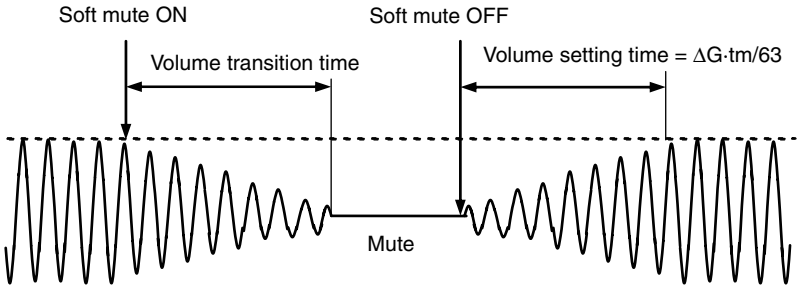
6.11.2 AUSMUTE

Data	Mode	Initial Value	Description
0	OFF	0	Soft mute control is not provided for ASIO input data.
1	ON		Soft mute control is provided for ASIO input data.

6.11.3 MELSMUTE

Data	Mode	Initial Value	Description
0	OFF	0	Soft mute control is not provided for sound generator output.
1	ON		Soft mute control is provided for sound generator output.

Figure 6-1 Soft Mute Operation



Remark ΔG: Gain setting difference
tm: Volume setting time

6.12 Digital Volume (Sound generator Output L-ch) Setting for Audio DAC (MELLDG)

This register performs setting for digital gain (sound generator output L-ch).

Address: 11H, register name: MELLDG, block: Digital volume, access: R/W, initial value: FFH

D7	D6	D5	D4	D3	D2	D1	D0
MELLDG2[1:0]		MELLDG1[5:0]					

6.12.1 MELLDG2[1:0]

Data	Mode	Initial Value	Description
MELLDG2[1:0]		11b	Performs setting for digital gain (sound generator output L-ch)

6.12.2 MELLDG1[5:0]

Data	Mode	Initial Value	Description
MELLDG1[5:0]		111111b	Performs setting for digital gain (sound generator output L-ch)

Remark The setting value is derived from the sum of the corresponding gain setting values in Digital gain settings 1 and 2 (Refer to **Table 6-6 Digital Gain Settings 1, Table 6-7 Digital Gain Settings 2**).

6.13 Digital Volume (Sound generator Output R-ch) Setting for Audio DAC (MELRDG)

This register performs setting for digital gain (sound generator output R-ch).

Address: 12H, register name: MELRDG, block: Digital volume, access: R/W, initial value: FFH

D7	D6	D5	D4	D3	D2	D1	D0
MELRDG2[1:0]		MELRDG2[5:0]					

6.13.1 MELRDG2[1:0]

Data	Mode	Initial Value	Description
MELRDG2[1:0]		11b	Performs setting for digital gain (sound generator output R-ch)

6.13.2 MELRDG1[5:0]

Data	Mode	Initial Value	Description
MELRDG1[5:0]		111111b	Performs setting for digital gain (sound generator output R-ch)

Remark The setting value is derived from the sum of the corresponding gain setting values in Digital Gain Settings 1 and 2 (Refer to **Table 6-6 Digital Gain Settings 1, Table 6-7 Digital Gain Settings 2**).

6.14 Digital Volume (ASI Input L-ch) Setting for Audio DAC (AULDG)

This register performs setting for digital gain (sound generator output L-ch).

Address: 13H, register name: AULDG, block: Digital volume, access: R/W, initial value: FFH

D7	D6	D5	D4	D3	D2	D1	D0
AULDG2[1:0]		AULDG1[5:0]					

6.14.1 AULDG2[1:0]

Data	Mode	Initial Value	Description
AULDG2[1:0]		11b	Performs setting for digital gain (ASI input L-ch)

6.14.2 AULDG1[5:0]

Data	Mode	Initial Value	Description
AULDG1[5:0]		111111b	Performs setting for digital gain (ASI input L-ch)

Remark The setting value is derived from the sum of the corresponding gain setting values in Digital gain settings 1 and 2 (Refer to **Table 6-6 Digital Gain Settings 1, Table 6-7 Digital Gain Settings 2**).

6.15 Digital Volume (ASI Input R-ch) Setting for Audio DAC (AURDG)

This register performs setting for digital gain (ASI input R-ch).

Address: 14H, register name: AURDG, block: Digital volume, access: R/W, initial value: FFH

D7	D6	D5	D4	D3	D2	D1	D0
AURDG2[1:0]		AURDG1[5:0]					

6.15.1 AURDG2[1:0]

Data	Mode	Initial Value	Description
AURDG2[1:0]		11b	Performs setting for digital gain (ASI input R-ch)

6.15.2 AURDG1[5:0]

Data	Mode	Initial Value	Description
AURDG1[5:0]		111111b	Performs setting for digital gain (ASI input R-ch)

Remark The setting value is derived from the sum of the corresponding gain setting values in Digital Gain Settings 1 and 2((Refer to **Table 6-6 Digital Gain Settings 1, Table 6-7 Digital Gain Settings 2**).

Example When +10 dB is set: (+12 dB) + (–2 dB) → 82H
When 0 dB is set: (0 dB) + (0 dB) → 00H
When –20 dB is set: (0 dB) + (–20 dB) → 14H
When –60 dB is set: (0 dB) + (–60 dB) → 3H

Table 6-6 Digital Gain Settings 1

----DG2[1:0]	Gain
00b	0dB
01b	+6dB
10b	+12dB
11b	Mute (initial value)

Table 6-7 Digital Gain Settings 2

----DG1[5:0]	Gain Setting Value
000000b	0 dB
000001b	–1 dB
000010b	–2 dB
000011b	–3 dB
000100b	–4 dB
000101b	–5 dB
000110b	–6 dB
000111b	–7 dB
001000b	–8 dB
001001b	–9 dB
001010b	–10 dB
001011b	–11 dB
001100b	–12 dB
001101b	–13 dB
001110b	–14 dB
001111b	–15 dB
010000b	–16 dB
010001b	–17 dB
010010b	–18 dB
010011b	–19 dB
010100b	–20 dB
010101b	–21 dB
010110b	–22 dB
010111b	–23 dB
011000b	–24 dB
011001b	–25 dB
011010b	–26 dB
011011b	–27 dB
011100b	–28 dB
011101b	–29 dB
011110b	–30 dB
011111b	–31 dB

----DG1[5:0]	Gain Setting Value
100000b	–32 dB
100001b	–33 dB
100010b	–34 dB
100011b	–35 dB
100100b	–36 dB
100101b	–37 dB
100110b	–38 dB
100111b	–39 dB
101000b	–40 dB
101001b	–41 dB
101010b	–42 dB
101011b	–43 dB
101100b	–44 dB
101101b	–45 dB
101110b	–46 dB
101111b	–47 dB
110000b	–48 dB
110001b	–49 dB
110010b	–50 dB
110011b	–51 dB
110100b	–52 dB
110101b	–53 dB
110110b	–54 dB
110111b	–55 dB
111000b	–56 dB
111001b	–57 dB
111010b	–58 dB
111011b	–59 dB
111100b	–60 dB
111101b	–61 dB
111110b	–62 dB
111111b	–63 dB

6.16 Setting of Analog Master Volume (L-ch) for Audio DAC (ADACLVR)

This register performs setting for analog gain (L-ch).

Address: 17H, register name: ADACLVR, block: Master volume, access: R/W, initial value: 1FH

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ADACLVRGA[4:0]				

6.16.1 ADACLVRGA[4:0]

Data	Mode	Initial Value	Description
ADACLVRGA[4:0]		11111b	Performs setting for analog gain (Audio DAC output L-ch).

6.17 Setting of Analog Master Volume (R-ch) for Audio DAC (ADACRVR)

Performs setting for analog gain (R-ch).

Address: 18H, register name: ADACRVR, block: Master volume, access: R/W, initial value: 1FH

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ADACRVRGA[4:0]				

6.17.1 ADACRVRGA[4:0]

Data	Mode	Initial Value	Description
ADACRVRGA[4:0]		11111b	Performs setting for analog gain (Audio DAC output R-ch).

Table 6-8 Analog Gain Settings 1

----VRGA[4:0]	Gain Setting Value
00000b	0 dB
00001b	–1.5 dB
00010b	–3.0 dB
00011b	–4.5 dB
00100b	–6.0 dB
00101b	–7.5 dB
00110b	–9.0 dB
00111b	–10.5 dB
01000b	–12.0 dB
01001b	–13.5 dB
01010b	–15.0 dB
01011b	–16.5 dB
01100b	–18.0 dB
01101b	–19.5 dB
01110b	–21.0 dB
01111b	–22.5 dB

----VRGA[4:0]	Gain Setting Value
10000b	–24.0 dB
10001b	–25.5 dB
10010b	–27.0 dB
10011b	–28.5 dB
10100b	–30.0 dB
10101b	–31.5 dB
10110b	–33.0 dB
10111b	–34.5 dB
11000b	–36.0 dB
11001b	–37.5 dB
11010b	–39.0 dB
11011b	–40.5 dB
11100b	–42.0 dB
11101b	–43.5 dB
11110b	–45.0 dB
11111b	Mute (initial value)

6.18 Setting of LSI Standby (MSIO) (STNBY2)

This register performs setting for standby.

MEN and MBCLK are set to standby only when both STMSI and STMSO bits are set to standby. For details, refer to **Table 2-3 Pin Statuses in MSIO Block.**

Address: 20H, register name: STNBY2, block: MSIO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	STMSI	STMSO

6.18.1 STMSO

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for MSO (external sound generator connection serial interface input)
1	ON		Normal operation

6.18.2 STMSI

Data	Mode	Initial Value	Description
0	Stand-by	0	Standby for MSO (external sound generator connection serial interface input)
1	ON		Normal operation

6.19 Setting of MSIO Mode (SEL_MSIO1)

This register performs setting for MSIO.

Address: 21H, register name: SEl_MSIO1, block: MSIO, access: R/W, initial value: 10H

D7	D6	D5	D4	D3	D2	D1	D0
0	MBFS[2:0]			MLOOPSW	MMS	SMEN	SMBCLK

6.19.1 SMBCLK

Data	Mode	Initial Value	Description
0	Normal	0	Sets bit clock MBCLK to normal.
1	Inverted		Sets bit clock MBCLK to invert.

6.19.2 SMEN

Data	Mode	Initial Value	Description
0	Frame synchronization mode	0	Sets MEN to frame synchronization mode.
1	Stereo mode		Sets MEN to LR stereo mode.

Remark In LR stereo mode, R-ch data is stored in the high cycle of the MEN signal, and L-ch data in the Low cycle.

6.19.3 MMS

Data	Mode	Initial Value	Description
0	Slave	0	MSIO slave mode
1	Master		MSIO master mode

Remark When slave mode (MMS = 0) is set, an external clock is required.

6.19.4 MLOPSW

Data	Mode	Initial Value	Description
0	Normal mode	0	Normal operation
1	Loop back		Loop back mode for MSIO (MSI to MSO)

6.19.5 MBF[2:0]

Data	Mode	Initial Value	Description
00H	32 fs	01H	Sets MBCLK frequency at 32 fs (This can be done in master mode.).
01H	64 fs		Sets MBCLK frequency at 64 fs (This can be done in master mode.).
02H	96 fs		Sets MBCLK frequency at 96 fs.
03H	128 fs		Sets MBCLK frequency at 128 fs (This can be done in master mode.).
04H	160 fs		Sets MBCLK frequency at 160 fs.
05H	192 fs		Sets MBCLK frequency at 196 fs.
06H	224 fs,		Sets MBCLK frequency at 224 fs.
07H	256 fs		Sets MBCLK frequency at 256 fs (This can be done in master mode.).

Cautions 1. In master mode (MMS = 1), only 32, 64, 128, and 256 fs can be set. If any other value is set, 64 fs is forcedly selected.

2. When MSIO and ASIO are used at the same time, ASIO is set to the master mode (BFS = 32 or 64 fs) only.

6.20 FS Switching and BCLK Switching in Audio Serial Interface (SEL_FS)

This register performs setting for the effective channel count of MSI and MSO.

Address: 22H, register name: SEL_MSIO2, block: MSIO, access: R/W, initial value: 33H

D7	D6	D5	D4	D3	D2	D1	D0
MCHI[3:0]				MCHO[3:0]			

6.20.1 MCHI[3:0]

Data	Mode	Initial Value	Description
00H	1 ch	03H	Sets frame effective channel for MSI input data to 1 ch.
01H	2 ch		Sets frame effective channel for MSI input data to 2 ch.
02H	3 ch		Sets frame effective channel for MSI input data to 3 ch.
03H	4 ch		Sets frame effective channel for MSI input data to 4 ch.
04H	5 ch		Sets frame effective channel for MSI input data to 5 ch.
05H	6 ch		Sets frame effective channel for MSI input data to 6 ch.
06H	7 ch		Sets frame effective channel for MSI input data to 7 ch.
07H	8 ch		Sets frame effective channel for MSI input data to 8 ch.
08H	9 ch		Sets frame effective channel for MSI input data to 9 ch.
09H	10 ch		Sets frame effective channel for MSI input data to 10 ch.
0AH	11 ch		Sets frame effective channel for MSI input data to 11 ch.
0BH	12 ch		Sets frame effective channel for MSI input data to 12 ch.
0CH	13 ch		Sets frame effective channel for MSI input data to 13 ch.
0DH	14 ch		Sets frame effective channel for MSI input data to 14 ch.
0EH	15 ch		Sets frame effective channel for MSI input data to 15 ch.
0FH	16 ch		Sets frame effective channel for MSI input data to 16 ch.

6.20.2 MCHO[3:0]

Data	Mode	Initial Value	Description
00H	1 ch	03H	Sets frame effective channel for MSO output data to 1 ch.
01H	2 ch		Sets frame effective channel for MSO output data to 2 ch.
02H	3 ch		Sets frame effective channel for MSO output data to 3 ch.
03H	4 ch		Sets frame effective channel for MSO output data to 4 ch.
04H	5 ch		Sets frame effective channel for MSO output data to 5 ch.
05H	6 ch		Sets frame effective channel for MSO output data to 6 ch.
06H	7 ch		Sets frame effective channel for MSO output data to 7 ch.
07H	8 ch		Sets frame effective channel for MSO output data to 8 ch.
08H	9 ch		Sets frame effective channel for MSO output data to 9 ch.
09H	10 ch		Sets frame effective channel for MSO output data to 10 ch.
0AH	11 ch		Sets frame effective channel for MSO output data to 11 ch.
0BH	12 ch		Sets frame effective channel for MSO output data to 12 ch.
0CH	13 ch		Sets frame effective channel for MSO output data to 13 ch.
0DH	14 ch		Sets frame effective channel for MSO output data to 14 ch.
0EH	15 ch		Sets frame effective channel for MSO output data to 15 ch.
0FH	16 ch		Sets frame effective channel for MSO output data to 16 ch.

6.21 Setting of LSI Version (LSIVER)

This register shows the LSI version. This register is read only. It is impossible to write to the register.

Address: 3FH, register name: LSIVER, block: test, access: R, initial value: Undefined

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	VER[3:0]			

6.21.1 VER[3:0]

Data	Mode	Initial Value	Description
VER [3:0]			Reads LSI version.

6.22 Setting of Bank in Serial Interface Mode (BANK)

This register performs setting for bank switching.

Address: 7CH, register name: BANK, block: CPU I/F, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BANK[1:0]	

6.22.1 BANK[1:0]

A1 Pin	Data	Initial Value	Description
*	00h	00H	Accesses to addresses from 00H to 7FH of registers of Control register bank (in serial I/F).
*	01h		Accesses to addresses from 80H to FFH of registers of Control register bank (in serial I/F).
*	02h		Accesses to addresses from 00H to 7FH of sound generator registers (in serial I/F).
*	03h		Accesses to addresses from 80H to FFH of sound generator registers (in serial I/F).

The bank switching in parallel interface mode is shown in the table below.

A1 Pin	Data	Initial Value	Description
0	*	0	Accesses to addresses from 00H to FFH of registers of Control register bank.
1	*		Accesses to addresses from 00H to FFH of sound generator registers.

Caution Be sure to set 0 for addresses from D7 to D2.
BANK switching is effective only in serial interface mode (PS = 1).

7. POWER STARTUP PROCEDURE

The μPD9971 has five internal power-supply units: Power supply for regulators ($REGV_{DD}$), power supply for internal digital circuits (DV_{DD}), power supply for PLL1 and PLL2 ($PLLV_{DD}$), power supply for internal analog circuits (AV_{DD}), and power supply for level shifter blocks in I/O circuits (EV_{DD}).

When internal regulator output pin REGOUT is connected to power supply pin DV_{DD}, REGOUT can be used as power supply for the internal digital circuits.

7.1 Wakeup Sequence

7.1.1 When a regulator is not used

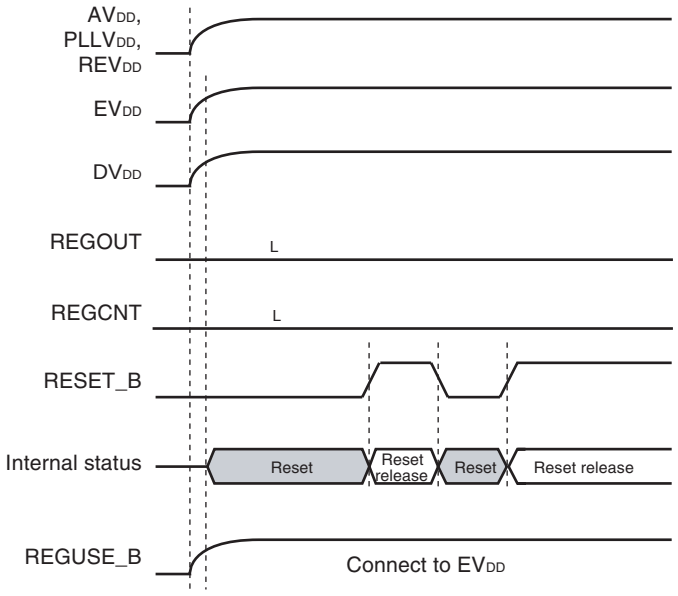
<1> Short REGUSE_B with EV_{DD} beforehand. (Fix REGUSE_B to high level.) Short REGCNT pin with DGND beforehand, too.

<2> With RESET_B pin set to low level, turn on DV_{DD} (with 1.54 V), $REGV_{DD}$, AV_{DD}, $PLLV_{DD}$ (with 3.0 V each), and EV_{DD} (with 1.8 to 3.0 V). It is recommended that all of power supplies be turned on at the same time. Avoid turning on the power supplies while RESET_B pin is set to high level because this may lead to the flow of a through current into bus lines of the CPU.

<3> Wait until power supply voltage reaches the specified voltage.

<4> Release hardware reset. To release it, set RESET_B pin to high level instead of low level.

Figure 7-1 Wakeup Sequence (When A Regulator Is Not Used)



7.1.2 When a regulator is used

<1> Short REGUSE_B with DGND beforehand. (Fix REGUSE_B to low level.)
Set REGCNT pin to low level beforehand, too.

<2> With RESET_B pin set to low level, turn on $REGV_{DD}$, AV_{DD}, $PLLV_{DD}$ (with 3.0 V each), and EV_{DD} (with 1.8 to 3.0 V). It is recommended that all of the power supplies be turned on at the same time.

<3> Wait until power supply voltage reaches to the specified voltage.

★ <4> Set REGCNT pin to high level to supply current to the digital power supply.

<5> Release hardware reset. To release it, set RESET_B pin to high level instead of low level.

Figure 7-2 Wakeup Sequence 1 (When A Regulator Is Used)

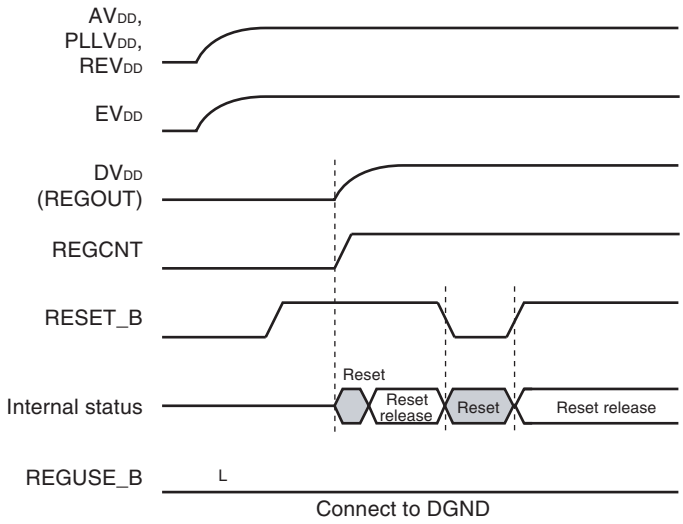
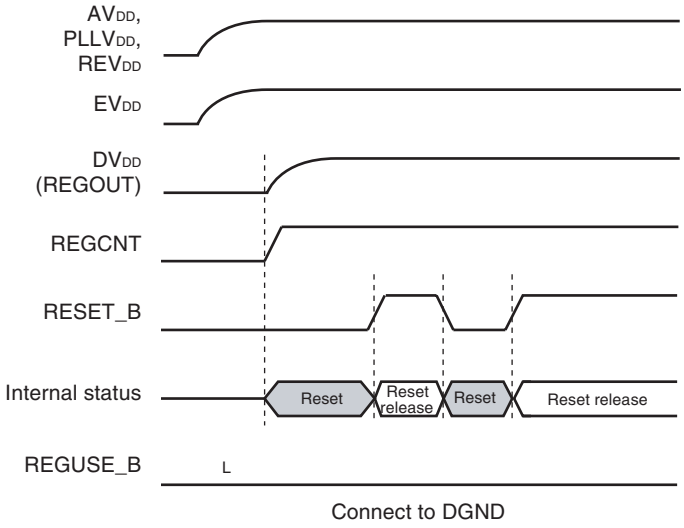


Figure 7-3 Wakeup Sequence 2 (When A Regulator Is Used)



7.2 Shutdown Sequence

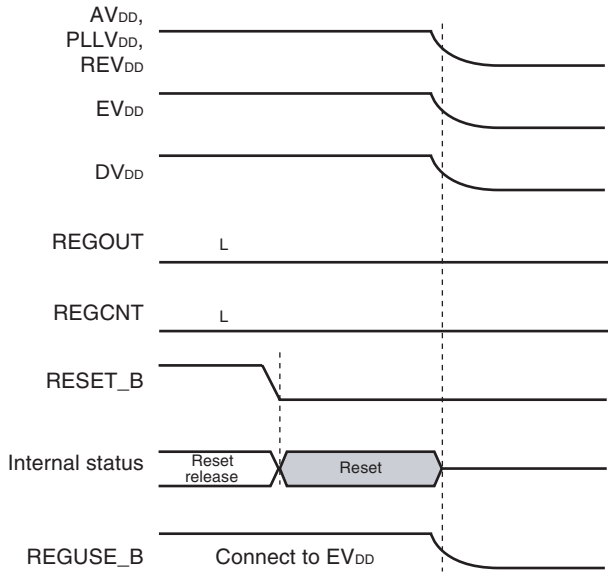
7.2.1 When a regulator is not used

<1> Set hardware reset. (Set RESET_B pin to low level instead of high level.)

<2> With RESET_B pin set to low level, turn off DV_{DD} (with 1.54 V), $REGV_{DD}$, AV_{DD}, $PLLV_{DD}$ (with 3.0 V each), and EV_{DD} (with 1.8 to 3.0 V). It is recommended that all of the power supplies be turned off at the same time. Even though turning off power without RESET_B pin set to the low level does not lead to failures of μPD9971, this should be avoided because this may lead to the flow of through current into bus lines of the CPU.

<3> After shutdown is performed, status of the RESET_B pin is undefined.

Figure 7-4 Shutdown Sequence (When A Regulator Is Not Used)



7.2.2 When a regulator is used

<1> Set hardware reset. (Set RESET_B pin to low level instead of high level.)

<2> Set REGCNT pin to low level to stop the supply of current to the digital power source.

★ <3> With RESET_B pin set to low level, turn off $REGV_{DD}$, AV_{DD}, $PLLV_{DD}$ (with 3.0 V each), and EV_{DD} (with 1.8 to 3.0 V). It is recommended that all of the power supplies be turned off at the same time.

Figure 7-5 Shutdown Sequence 1 (When A Regulator Is Used)

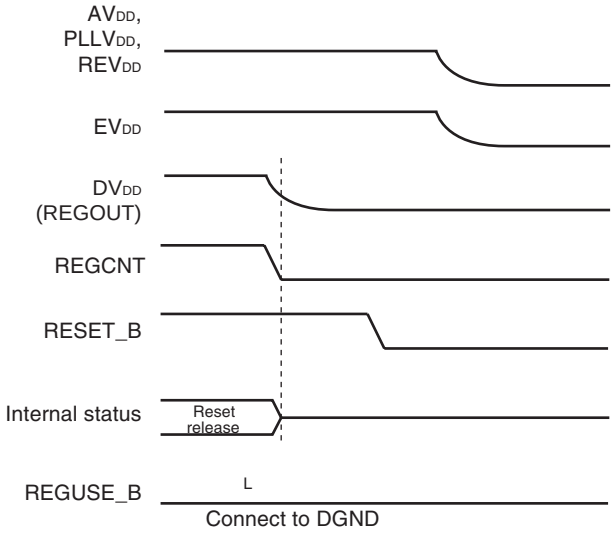
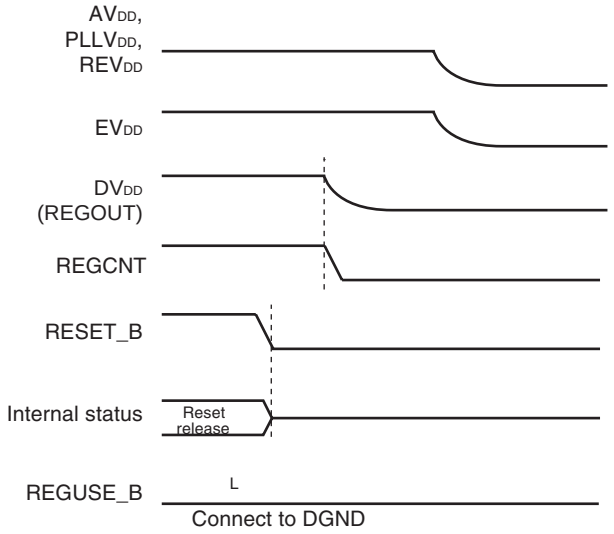


Figure 7-6 Shutdown Sequence 2 (When A Regulator Is Used)



7.3 Power Saving Functions

The μPD9971 includes 2 power saving functions (standby modes): The software power saving function controlled by command input (in standby mode) and the hardware power saving function is controlled by the core power supply.

Note that when these functions are enabled, all contents written to registers and memory are erased. (Rewrite is required after power saving is canceled.)

7.3.1 Hardware power saving function

For hardware power saving, follow the steps below.

<1> With RESET_B pin set to low level, turn off DV_{DD}, $REGV_{DD}$, AV_{DD}, and $PLLV_{DD}$.

<2> When a regulator is used (when REGUSE_B = low), set REGCNT pin to low level instead of high level.

<3> Continue supplying EV_{DD} since it is used to protect the CPU bus lines.

<4> Be sure to fix RESET_B pin to low level during hardware power saving operation.

Follow the steps described below to return to normal operation.

<1> When a regulator is used (when REGUSE_B = low), set REGCNT pin to high level instead of low level.

<2> With RESET_B pin set to low level, turn on DV_{DD} (with 1.5 V), $REGV_{DD}$, AV_{DD}, and $PLLV_{DD}$ (with 3.0 V each).

<3> Set RESET_B pin to high level.

★ **Cautions When the power is on/off with RESET_B pin set to high level, the output value and I/O control of each register and pin are unstable because the initialization of μPD9971 is not completed until initialization (RESET_B = low) is performed. Therefore, pay attention to the statuses of D0 to D7 pins, LED pin, VIB pin, PO0 to PO3 pins, and INT pin until they are initialized.**
Note that through current may flow into the bus lines of the CPU.

7.3.2 Software power saving function

The software power saving function of the μPD9971 is realized as follows: The controlling of registers 00H and 20H achieves the standby state of each block.

In this state, power is supplied to all blocks, and each register value is retained because RESET_B is set to high level.

When the internal regulator is used, setting REGCNT pin to low level can reduce the regulator output to GND, drastically reducing the leakage current of digital power supply.

Caution When either of the functions is performed, a certain wait time is required for rebooting after PLL and reference voltage blocks are initialized or their power is reduced (STREF, STPLL1, and STPLL2 = low).

8. SETTING SEQUENCE

In serial I/F mode (PS pin = 1), two operations--"switching to the sound generator bank" and "switching to the Control register bank"--are required. The former means setting the bank register to the sound generator bank while the bank register is assigned to Control register bank. Latter means setting the bank register to the Control register bank while the bank register is assigned to the sound generator bank.

These operations are not required when PS = 0 (parallel interface mode).

8.1 Power Up Sequence

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A, MCLK1B, MCLK2A, MCLK2B
5	Setting of ASIO sampling frequency	FS, BFS
6	Setting of MSIO mode	MBFS, MMS, SMEN, SMBCLK, MCHI, MCHO
7	Canceling VREF standby	STREF
8	Canceling PLL standby	STPLL1 and STPLL2 (5 ms after STREF standby is canceled)
9	Canceling function block standby	STSYNTH, STADIG, STADAC…
10	Internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

8.2 Basic Sequence for Switching Among Operation Modes

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when PS pin = 1)	BANK
2	Setting of digital volume mute	MELLDG, MELRDG, AULDG, AURDG
3	Setting of analog volume mute	ADACLVRGA, ADACRVRGA
4	Setting of standby state	STPLL1, STPLL2, STREF, STSYNTH, …
5	Setting of sampling frequency	FS, BFS
6	Setting of path (3DA)	EX3DAEN, PCMLSW, PCMRSW
7	Setting of path (digital mixing)	DACLSW, DACRSW, DACLMIX, DACRMIX, MELLSW, MELRSW, MELLMIX, MELRMIX
8	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
9	Setting of MSIO mode	MBFS, MMS, SMEN, SMBCLK, MCHI, MCHO
10	Switching to Sound generator bank (when PS pin = 1)	BANK
11	Setting of 3DA/surround function	
12	Switching to Control register bank (when PS pin = 1)	BANK
13	Canceling VREF standby	STREF
14	Canceling PLL standby	STPLL1 and STPLL2 (5 ms after STREF standby is canceled)
15	Canceling function block standby	STSYNTH, STADIG, STADAC…
16	Internal clock is valid.	5 ms after the STPLL1 and STPLL2 standby is canceled
17	Canceling the analog volume mute	ADACLVRGA, ADACRVRGA
18	Canceling the digital volume mute	MELLDG, MELRDG, AULDG, AURDG

Cautions 1. In slave mode, the clock input of LRCLK and BCLK is required.

2. Both, the setting for a mute performed after a phased decrease in volume by the digital volume (soft mute) and the phased increase in volume after a mute is canceled are a sequence for eliminating an audible change in sound that may occur due to single-frame operation errors in the digital data that occur during switching.

To make this function effective, the following settings are required: AUSMUTE = 1 and MELSMUTE = 1.

3. When the soft mute is not used, a phased decrease/increase in volume has to be performed by the analog volume of the path to be used, instead.

4. Since the STADIG signal is also used to reset arithmetic operations such as digital filter operations, a reset must be performed during mode switching.

8.2.1 Mute setting

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when the PS pin = 1)	BANK
2	Setting of digital volume mute	MELLDG, MELRDG, AULDG, AURDG
3	Setting of analog volume mute	ADACLVRGA, ADACRVRGA

8.2.2 Standby setting/cancel

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when the PS pin = 1)	BANK
2	Setting of digital volume mute	MELLDG, MELRDG, AULDG, AURDG
3	Setting of analog volume mute	ADACLVRGA, ADACRVRGA
4	Setting of standby state	STPLL1, STPLL2, STREF, STSYNTH, …
5	Canceling VREF standby	STREF
6	Canceling PLL standby	STPLL1 and STPLL2 (5 ms after the STREF standby is canceled)
7	Canceling function block standby	STSYNTH, STADIG, STADAC, …
8	The internal clock is valid.	5 ms after the STPLL1 and STPLL2 standby is canceled
9	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
10	Canceling digital volume mute	MELLDG, MELRDG, AULDG, AURDG

8.2.3 FS switching

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when the PS pin = 1)	BANK
2	Setting of digital volume mute	MELLDG, MELRDG, AULDG, AURDG
3	Setting of analog volume mute	ADACLVRGA, ADACRVRGA
4	Setting of standby state	STPLL1, STPLL2, STREF, STSYNTH, …
5	Setting of sampling frequency	FS, BFS
6	Setting of MSIO mode	MBFS, MMS, SMEN, SMBCLK, MCHI, MCHO
7	Canceling VREF standby	STREF
8	Canceling PLL standby	STPLL1 and STPLL2 (5 ms after the STREF standby is canceled)
9	Canceling function block standby	STSYNTH, STADIG, STADAC, …
10	The internal clock is valid.	5 ms after the STPLL1 and STPLL2 standby is canceled
11	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
12	Canceling digital volume mute	MELLDG, MELRDG, AULDG, AURDG

8.2.4 Path switching

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when the PS pin = 1)	BANK
2	Setting of digital volume mute	MELLDG, MELRDG, AULDG, AURDG
3	Setting of analog volume mute	ADACLVRGA, ADACRVRGA
4	Setting of standby state	STPLL1, STPLL2, STREF, STSYNTH, …
5	Setting of path (digital mixing)	DACLSW, DACRSW, DACLMIX, DACRMIX, MELLSW, MELRSW, MELLMIX, MELRMIX
6	Canceling VREF standby	STREF
7	Canceling PLL standby	STPLL1 and STPLL2 (5 ms after STREF standby is canceled)
8	Canceling function block standby	STSYNTH, STADIG, STADAC, …
9	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled
10	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
11	Canceling digital volume mute	MELLDG, MELRDG, AULDG, AURDG

8.2.5 3DA/surround switching

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when the PS pin = 1)	BANK
2	Setting of digital volume mute	MELLDG, MELRDG, AULDG, AURDG
3	Setting of analog volume mute	ADACLVRGA, ADACRVRGA
4	Setting of standby state	STPLL1, STPLL2, STREF, STSYNTH, …
5	Switching to sound generator bank (when PS pin = 1)	BANK
6	Setting of 3DA/surround function	
7	Switching to Control register bank (when PS pin = 1)	BANK
8	Setting of path (3DA)	EX3DAEN, PCMLSW, PCMRSW
9	Setting of path (digital mixing)	DACLSW, DACRSW, DACLMIX, DACRMIX, MELLSW, MELRSW, MELLMIX, MELRMIX
10	Canceling VREF standby	STREF
11	Canceling the PLL standby	STPLL1 and STPLL2 (5 ms after the STREF standby is canceled)
12	Canceling function block standby	STSYNTH, STADIG, STADAC, …
13	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled
14	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
15	Canceling digital volume mute	MELLDG, MELRDG, AULDG, AURDG

8.2.6 ASIO mode setting

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when PS pin = 1)	BANK
2	Setting of digital volume mute	MELLDG, MELRDG, AULDG, AURDG
3	Setting of analog volume mute	ADACLVRGA, ADACRVRGA
4	Setting of standby state	STPLL1, STPLL2, STREF, STSYNTH, …
5	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
6	Canceling VREF standby	STREF
7	Canceling PLL standby	STPLL1 and STPLL2 (5 ms after STREF standby is canceled)
8	Canceling function block standby	STSYNTH, STADIG, STADAC, …
9	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled
10	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
11	Canceling digital volume mute (soft mute)	MELLDG, MELRDG, AULDG, AURDG

8.3 Setting Sequence Examples

Examples of the setting sequence are given below.

In the examples, the input clock is set provided that MCLK = 12 MHz.

8.3.1 Sound generator-DAC-line output

8.3.2 Sound generator-ASO output (master mode)

8.3.3 Sound generator-ASO output (slave mode)

8.3.4 ASI-DAC-line output

8.3.5 ASI-ASO output

8.3.6 ASI-EQ-DAC-line output (fs = 32 kHz)

8.3.7 ASI-EQ-DAC-line output (fs = 44.1 kHz)

8.3.8 ASI-EQ-ASO output (fs = 32 kHz)

8.3.9 ASI-EQ-ASO output (fs = 44.1 kHz)

8.3.1 Sound generator-DAC-line output (Clock: MCLK2 = 12 MHz)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when the regulator is used) REGCNT pin: From low to high (when the regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after the setting of REGCNT when the regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 32 kHz, BFS: 64 fs
6	Switching to sound generator bank (when the PS pin = 1)	BANK
7	Setting of 3DA/surround function	
8	Switching to Control register bank (when the PS pin = 1)	BANK
9	Setting of soft mute	MELSMUTE = 1
10	Setting of path (digital mixing)	MELLSW: Through, MELRSW: Through
11	Canceling VREF standby	STREF = 1
12	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after the STREF standby is canceled)
13	Canceling function block standby	STSYNTH = STADIG = STADAC = 1
14	Internal clock is valid.	5 ms after the STPLL1 and STPLL2 standby is canceled

(2) Switching to the sound generator bank (when the PS pin = 1)

(3) Setting of the sound generator

(4) Transferring data to the sound generator

(5) Canceling the mute

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when the PS pin = 1)	BANK
2	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
3	Canceling digital volume mute	MELLDG, MELRDG

8.3.2 Sound generator-ASO output (Clock: MCLK2 = 12 MHz, in the master mode)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when the regulator is used) REGCNT pin: From low to high (when the regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after the setting of REGCNT when the regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 32 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS = 1, ASIM, LRCLK, SLR
7	Switching to sound generator bank (when the PS pin = 1)	BANK
8	Setting of 3DA/surround function	
9	Switching to Control register bank (when the PS pin = 1)	BANK
10	Setting of soft mute	MELSMUTE = 0
11	Setting of path (digital mixing)	DACLMIX: Mute, DACRMIX: Mute, MELLMIX: Through, MELRMIX: Through, EX3DAEN = 0
12	Canceling VREF standby	STREF = 1
13	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after the STREF standby is canceled)
14	Canceling function block standby	STSYNTH = STADIG = STASI = STASO = 1
15	Internal clock is valid.	5 ms after the STPLL1 and STPLL2 standby is canceled

(2) Switching to the sound generator bank (when the PS pin = 1)

(3) Setting of the sound generator

(4) Transferring data to the sound generator

(5) Canceling the mute

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when the PS pin = 1)	BANK
2	Canceling digital volume mute	MELLDG, MELRDG

8.3.3 Sound generator-ASO output (Clock: MCLK2 = 12 MHz, in the slave mode)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 32 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS = 0, ASIM, LRCLK, SLR
7	Switching to sound generator bank (when PS pin = 1)	BANK
8	Setting of 3DA/surround function	
9	Switching to Control register bank (when PS pin = 1)	BANK
10	Setting of soft mute	MELSMUTE = 0
11	Setting of path (digital mixing)	DACLMIX: Mute, DACRMIX: Mute, MELLMIX: Through, MELRMIX: Through, EX3DAEN = 0
12	Canceling VREF standby	STREF = 1
13	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after STREF standby is canceled)
14	Canceling function block standby	STSYNTH = STADIG = STASI = STASO = 1
15	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

(2) Switching to the sound generator bank (when the PS pin = 1)

(3) Setting of the sound generator

(4) Transferring data to the sound generator

(5) Canceling the mute

Step	Item	Target registers, pins, etc.
1	Switching to Control register bank (when PS pin = 1)	BANK
2	Canceling digital volume mute	MELLDG, MELRDG

8.3.4 ASI-DAC-line output (Clock: MCLK2 = 12 MHz)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 32 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
7	Setting of soft mute	AUSMUTE = 1
8	Setting of path (digital mixing)	DACLSW: Through, DACRSW: Through
9	Canceling VREF standby	STREF = 1
10	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after STREF standby is canceled)
11	Canceling function block standby	STSYNTH = STADIG = STADAC = STASI = STASO = 1
12	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

(2) Transmitting music data

(3) Canceling mute

Step	Item	Target registers, pins, etc.
1	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
2	Canceling digital volume mute	AULDG, AURDG

8.3.5 ASI-ASO output (Clock: MCLK = 12 MHz)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 32 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
7	Setting of soft mute	AUSMUTE = 0
8	Setting of path (digital mixing)	DACLSW: Through, DACRSW: Through
9	Canceling VREF standby	STREF = 1
10	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after STREF standby is canceled)
11	Canceling function block standby	STSYNTH = STADIG = STADAC = STASI = STASO = 1
12	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

(2) Transmitting music data

(3) Canceling mute

Step	Item	Target registers, pins, etc.
1	Canceling digital volume mute	AULDG, AURDG

8.3.6 ASI-surround-DAC-line output (Clock: MCLK2 = 12 MHz, fs = 32 kHz)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 32 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
7	Setting of soft mute	MELSMUTE = 1
8	Switching to sound generator bank (when PS pin = 1)	BANK
9	Setting of 3D surround function	
10	Switching to Control register bank (when PS pin = 1)	BANK
11	Setting of path (equalizer)	EX3DAEN = 0, PCMLSW = PCMRSW = 1
12	Setting of path (digital mixing)	MELLSW: Through, MELRSW: Through
13	Canceling VREF standby	STREF = 1
14	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after STREF standby is canceled)
15	Canceling function block standby	STSYNTH = STADIG = STADAC = STASI = STASO = 1
16	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

(2) Transmitting music data

(3) Canceling mute

Step	Item	Target registers, pins, etc.
1	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
2	Canceling digital volume mute	MELLDG, MELRDG

8.3.7 ASI-surround-DAC-line output (Clock: MCLK2 = 12 MHz, fs = 44.1 kHz)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 44.1 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
7	Setting of soft mute	AUSMUTE = 1
8	Switching to sound generator bank (when PS pin = 1)	BANK
9	Setting of 3D surround function	
10	Switching to Control register bank (when PS pin = 1)	BANK
11	Setting of path (equalizer)	EX3DAEN = 1, PCMLSW = PCMRSW = 1
12	Setting of path (digital mixing)	DACLSW: Through, DACRSW: Through
13	Canceling VREF standby	STREF = 1
14	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after STREF standby is canceled)
15	Canceling function block standby	STSYNTH = STADIG = STADAC = STASI = STASO = 1
16	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

(2) Transmitting music data

(3) Canceling mute

Step	Item	Target registers, pins, etc.
1	Canceling analog volume mute	ADACLVRGA, ADACRVRGA
2	Canceling digital volume mute	AULDG, AURDG

8.3.8 ASI-surround-ASO output (Clock: MCLK2 = 12 MHz, fs = 32 kHz)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 32 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
7	Setting of soft mute	AUSMUTE = MELSMUTE = 0
8	Switching to sound generator bank (when PS pin = 1)	BANK
9	Setting of 3D surround function	
10	Switching to Control register bank (when PS pin = 1)	BANK
11	Setting of path (equalizer)	EX3DAEN = 0, PCMLSW = PCMRSW = 1
12	Setting of path (digital mixing)	DACLMIX: Mute, DACRMIX: Mute, MELLMIX: Through, MELRMIX: Through
13	Canceling VREF standby	STREF = 1
14	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after STREF standby is canceled)
15	Canceling function block standby	STSYNTH = STADIG = STASI = STASO = 1
16	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

(2) Transmitting music data

(3) Canceling mute

Step	Item	Target registers, pins, etc.
1	Canceling digital volume mute	MELLDG, MELRDG

8.3.9 ASI-surround-ASO output (Clock: MCLK2 = 12 MHz, fs = 44.1 kHz)

(1) Power on

Step	Item	Target registers, pins, etc.
1	Setting of regulator	REGUSE_B pin: Fixed to low (when regulator is used) REGCNT pin: From low to high (when regulator is used)
2	Canceling hardware reset	RESET_B pin: From low to high
3	Setting of PLL (setting of CSTRT and MCLKSEL)	CSTRT pin, MCLKSEL, and CSTRTEN (1 ms after setting of REGCNT when regulator is used)
4	Setting of PLL (input frequency)	MCLK1A = 4BH, MCLK1B = 9AH, MCLK2A = 05H, MCLK2B = 2FH
5	Setting of sampling frequency	FS: 44.1 kHz, BFS: 64 fs
6	Setting of ASIO mode	MS, ASIM, LRCLK, SLR
7	Setting of soft mute	AUSMUTE = MELSMUTE = 0
8	Switching to sound generator bank (when PS pin = 1)	BANK
9	Setting of 3D surround function	
10	Switching to Control register bank (when PS pin = 1)	BANK
11	Setting of path (equalizer)	EX3DAEN = 1, PCMLSW = PCMRSW = 1
12	Setting of path (digital mixing)	DACLMIX: Mute, DACRMIX: Mute, MELLMIX: Through, MELRMIX: Through
13	Canceling VREF standby	STREF = 1
14	Canceling PLL standby	STPLL1 = STPLL2 = 1 (5 ms after STREF standby is canceled)
15	Canceling function block standby	STSYNTH = STADIG = STASI = STASO = 1
16	The internal clock is valid.	5 ms after STPLL1 and STPLL2 standby is canceled

(2) Transmitting music data

(3) Canceling mute

Step	Item	Target registers, pins, etc.
1	Canceling digital volume mute	AULDG, AURDG

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	DV_{DD}	For digital ports	–0.3 to +2.0	V
	EV_{DD}	For I/O pins	–0.3 to +4.0	V
	$REGV_{DD}$	For regulators	–0.3 to +4.0	V
	$PLLV_{DD}$	For PLL	–0.3 to +4.0	V
	AV_{DD}	For analog ports	–0.3 to +4.0	V
Input voltage	V_I	$V_I/V_O < EV_{DD} + 0.5$ V	–0.3 to +4.0	V
Output voltage	V_O		–0.3 to +4.0	V
Power dissipation	P_D	$T_j = 125°C$	800	mW
Storage temperature	T_{stg}		–50 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

9.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating voltage	DV_{DD}		1.425		1.65	V
	EV_{DD}		1.71	1.8	3.3	V
	$REGV_{DD}$		2.7	3.0	3.3	V
	$PLLV_{DD}$		2.7	3.0	3.3	V
	AV_{DD}		2.7	3.0	3.3	V
Input voltage	V_I		0		EV_{DD}	V
Operating ambient temperature	T_A		–20		+85	°C

9.3 Capacitance

(T_A = +25°C, DV_{DD} = 0 V, EV_{DD} = 0 V, Analog pins are excluded.)

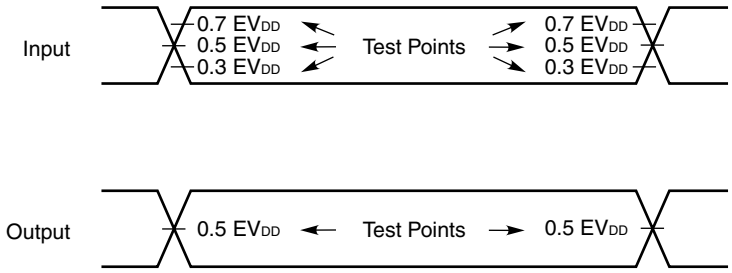
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz, pins other than those tested: 0 V		10		pF
Output capacitance	C_O			10		pF
I/O capacitance	C_{IO}			10		pF

9.4 DC Characteristics

(T_A = –20 to +85°C, The range of EV_{DD} does not exceed the range of the recommended operating condition)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IHN}		0.7 EV_{DD}		EV_{DD}	V
Low level input voltage	V_{ILN}		0		0.3 EV_{DD}	V
High level output voltage	V_{OH}	I_{OH} = –1 mA (LED or VIB = –1.5 mA)	0.7 EV_{DD}			V
Low level output voltage	V_{OL}	I_{OL} = +1 mA (LED or VIB = +1.5 mA)			0.3 EV_{DD}	V
High level input leakage current	I_{LHN}	V_I = EV_{DD}	0		10	μA
Low level input leakage current	I_{LLN}	V_I = 0 V	–10		0	μA
High-impedance leakage current	I_{zI}	0 V ≤ V_I ≤ EV_{DD}	0		–10	μA

Common ratings for switching characteristics



9.5 AC Characteristics

Unless otherwise specified, the ranges of T_A = –20 to +85°C, DV_{DD} and EV_{DD} conform to the recommended operating conditions.

9.5.1 Clock

Timing requirements

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MCLK1/MCLK2 input frequency	f_{CLKIN}	V_{CLKIN1} = 0.5V_{p-p} V_{CLKIN2} = EV_{DD} V_{p-p}	3.84		15.36	MHz
MCLK1 input level	V_{CLKIN1}	f_{CLKIN} = 3.84 MHz to 15.36 MHz[Note 1]	0.5		**Note 2**	V_{p-p}
MCLK2 input level	V_{CLKIN2}	f_{CLKIN} = 3.84 MHz to 15.36 MHz	0.7 EV_{DD}		EV_{DD}	
PLL lockup time	t_{LPLL}				2.0	ms

Notes 1. MCLK1 input to be used as PLL input should have capacitive coupling (1000 pF).

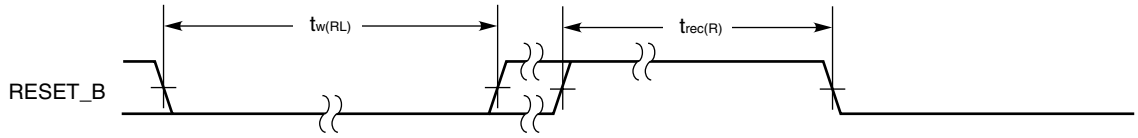
2. The maximum input level for MCLK1 should not exceed the power supply ($PLLV_{DD}$) potential.

9.5.2 Reset

Timing requirements (EV_{DD} = 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RESET_B low level width	$t_{w(RL)}$		225			ns
RESET_B recovery time	$t_{rec(R)}$		225			ns

Reset timing



9.5.3 Parallel CPU interface

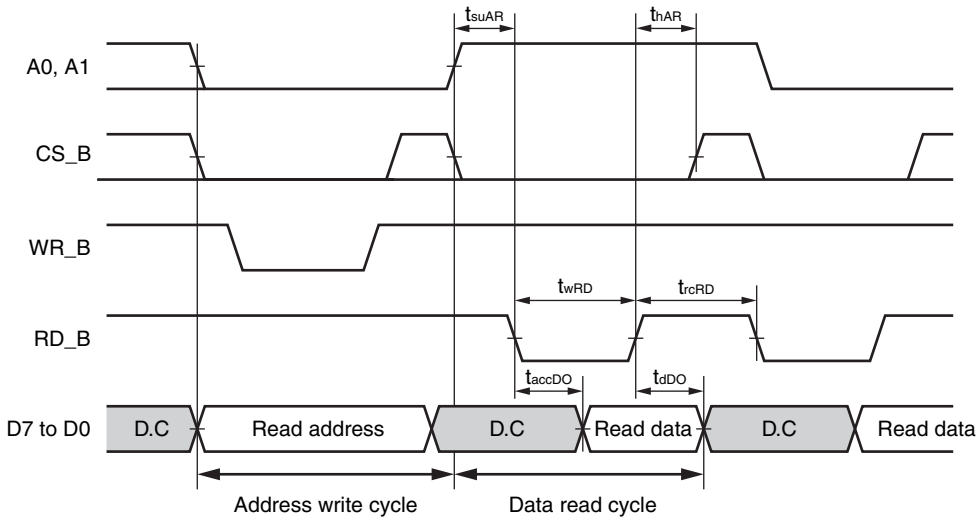
Timing requirements (EV_{DD} = 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RD_B width	t_{wRD}		100			ns
WR_B width	t_{wWR}		40			ns
RD_B recovery time	t_{rcRD}	During read access to the sound generator register	30			ns
WR_B recovery time	t_{rcWR}	During write access to registers of control register bank	80			ns
Data setup time	t_{suDI}	WR_B↑	50			ns
Data hold time	t_{hDI}	WR_B↑	0			ns
A, CS_B setup time	t_{suAW}	WR_B↑	50			ns
A, CS_B hold time	t_{hAW}	WR_B↑	0			ns
A, CS_B setup time	t_{suAR}	RD_B↓	0			ns
A, CS_B hold time	t_{hAR}	RD_B↑	0			ns

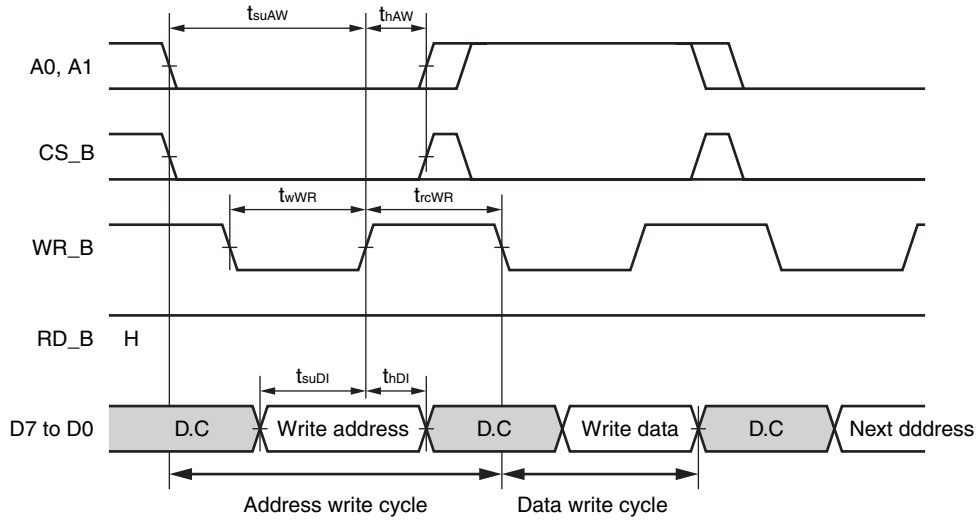
Switching characteristics (EV_{DD} = 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data access time 1	t_{accDO}	RD_B↓, I_{sink} = 1 mA			100	ns
Data hold time 1	t_{dDO}	RD_B↑, I_{sink} = 1 mA	0		30	ns

Parallel interface read timing



Parallel interface write timing

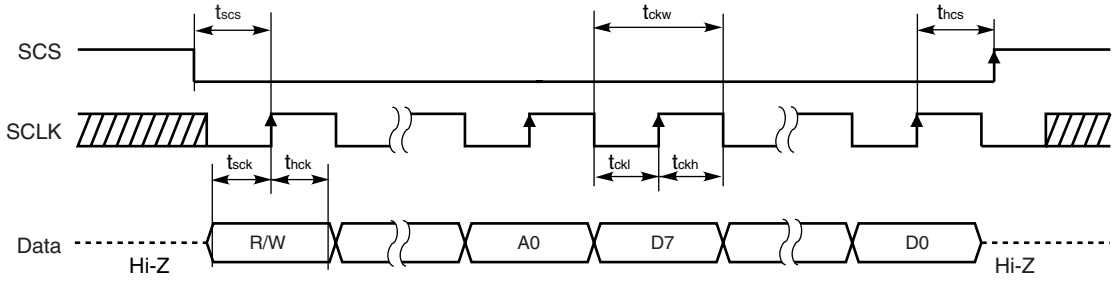


9.5.4 Serial CPU interface mode (Common to the 3-wire SPI mode and 4-wire SPI mode)

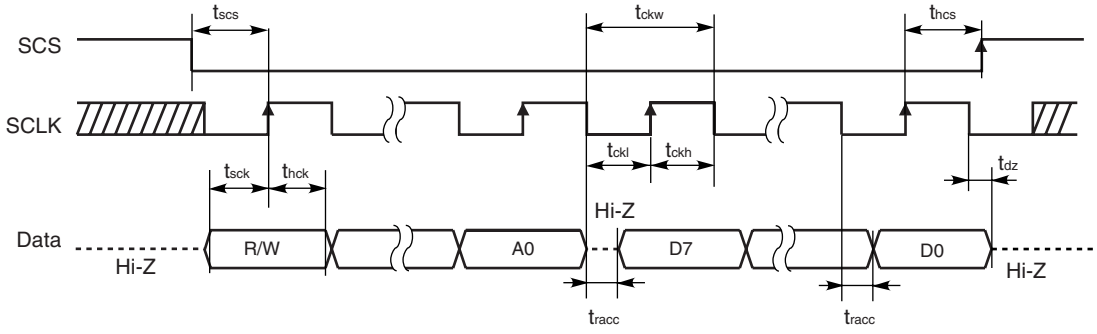
Timing requirements (EV_{DD} = 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLK cycle timeperiod	t_{ckw}		100			ns
SCLK high level width	t_{ckh}		50			ns
SCLK low level width	t_{ckl}		50			ns
Data setup time	t_{sck}	SCLK↑	20			ns
Data hold time	t_{hck}	SCLK↑	10			ns
SCS setup time	t_{scs}	SCLK↑	20			ns
SCS hold time	t_{hcs}	SCLK↑	20			ns
Data delay time	t_{racc}	Time until SCLK↓ data is output	5		20	ns
SCS recovery time	t_{csacc}	From SCS↑ to SCS↓	1			sclk
Data delay time	t_{dz}	Time until SCLK↓ data change to Hi-z	0		20	ns
SERINIT hold time	$t_{hcsINIT}$	SERINIT↑	80			ns
SCS setup time	t_{dhh}	SERINT↑	0			ns
SERINIT width	$t_{whSERINIT}$		20			ns
SCS hold time	t_{dll}	SERINT↓	0		20	ns

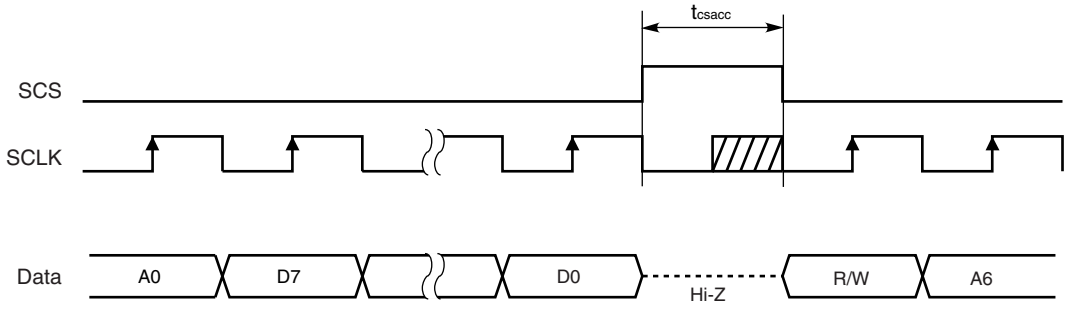
Serial interface write timing



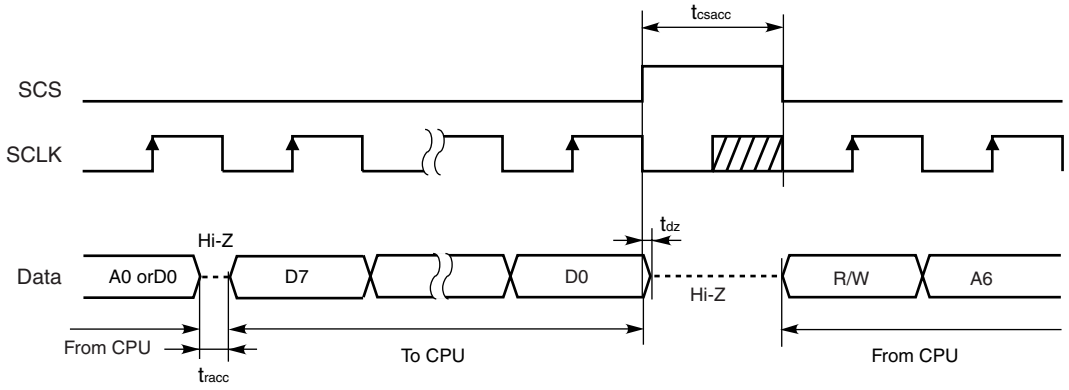
Serial interface read timing



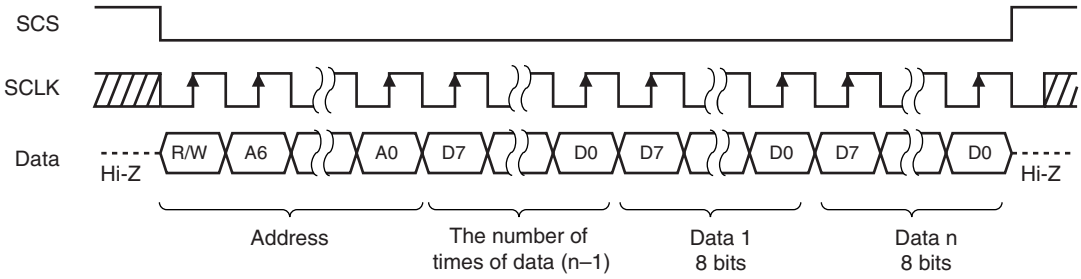
Serial interface write timing (continuous access)



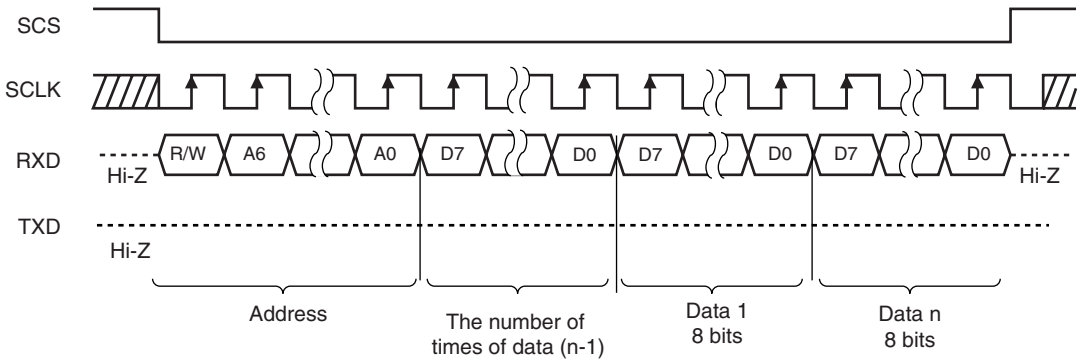
Serial interface read timing (continuous access)



3-wire SPI mode (host CPU write access format (continuous access 3)



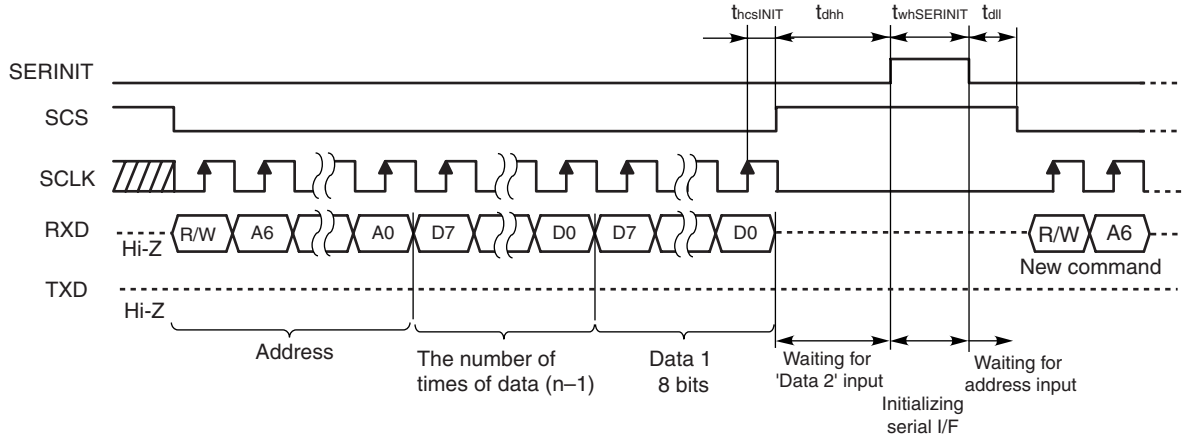
4-wire SPI mode (host CPU write access format (continuous access)



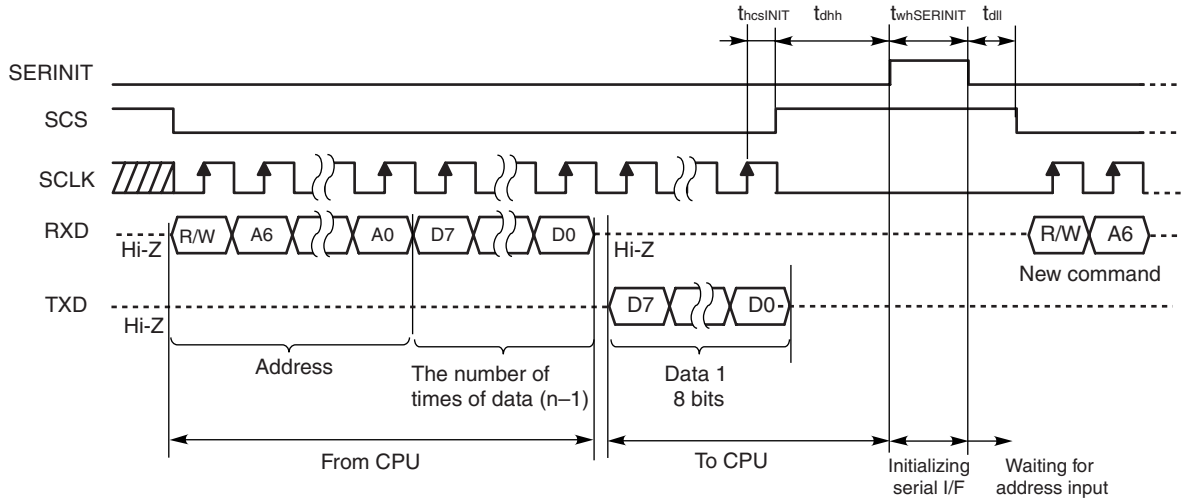
Initialization signal (SERINIT) timing

With this timing at the SERINIT/D0 pin, continuous access can be canceled

Write access



Read access



9.5.5 Audio serial interface (ASIO)

Timing requirements (EV_{DD} = 1.8 V)

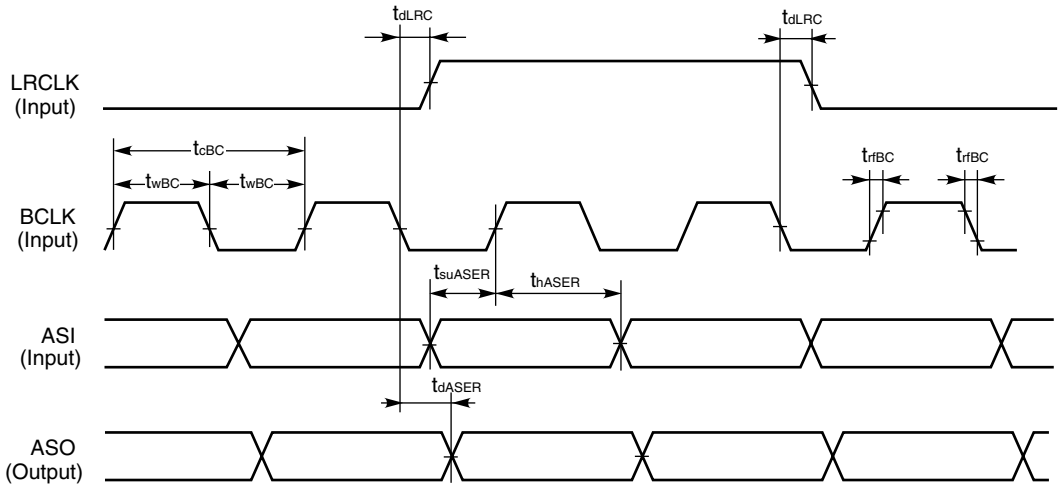
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASI input setup time	t_{suASER}	BCLK↑	50			ns
ASI input hold time	t_{hASER}	BCLK↑	50			ns

Switching characteristics (EV_{DD} = 1.8 V)

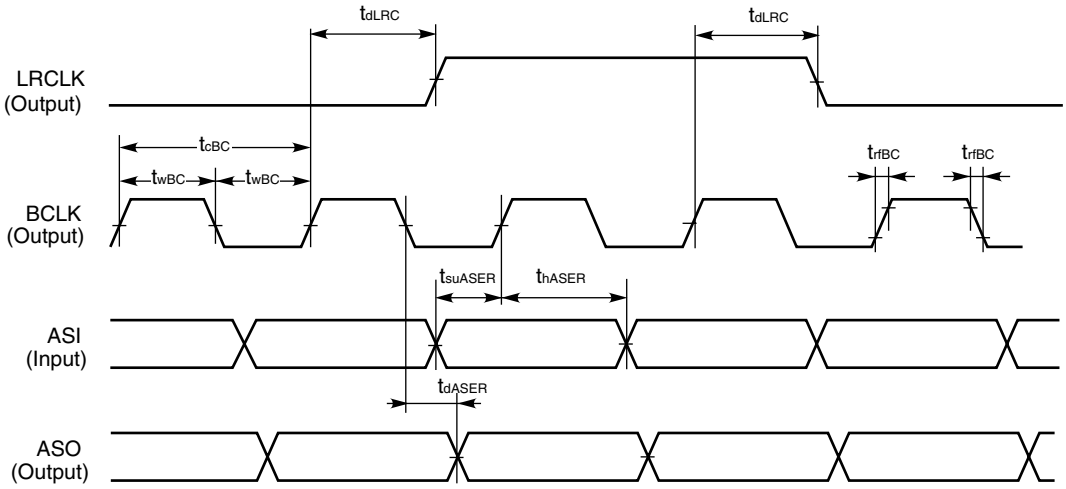
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LRCLK cycle time	t_{dLRC}			1/fs		ns
BCLK cycle time	t_{cBC}			1/(fs × 64)		ns
BCLK high-/low-level width	t_{wBC}			t_{cBC}/2		ns
BCLK rise/fall time	t_{rfBC}	In the slave mode			20	ns
LRCLK output delay time	t_{dLRC}	BCLK↓ (in the master mode)			50	ns
LRCLK output delay time	t_{dLRC}	BCLK↑ (in the slave mode)	50			ns
ASO output delay time	t_{dASER}	BCLK↓	–37.5		80	ns

The configuration of each frame depends on the settings of the BFS register.

Audio serial mode timing (master mode)



Audio serial mode timing (slave mode)



9.5.6 Serial interface dedicated to sound generator core external connection (MSIO)

Timing requirement

(EV_{DD} = 1.8 V)

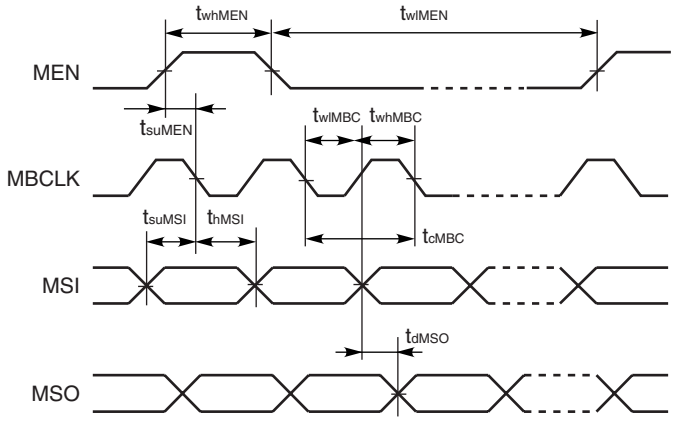
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
MSI setup time	t_{suMSI}	BCLK↑	50			ns
MSI input hold time	t_{hMSI}	BCLK↑	50			ns

Switching characteristics

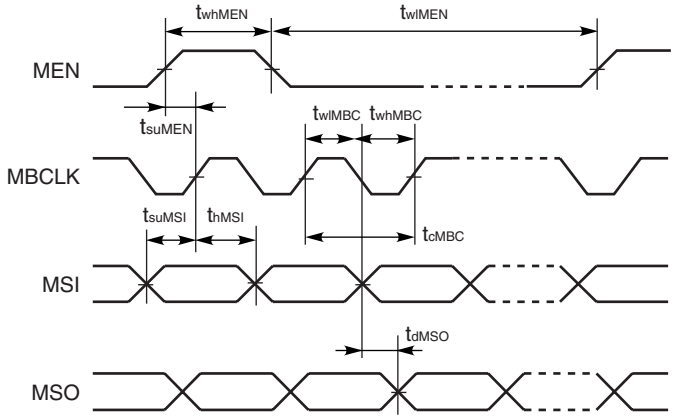
(EV_{DD} = 1.8 V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
MEN cycle time	t_{cMEN}			1/fs		ns
MEN high level width	t_{whMEN}		1			clk
MEN low level width	t_{wlMEN}		1			clk
MBCLK cycle time	t_{cMBC}	x = 32 to 256		1/(x*fs)		ns
MBCLK high level width	t_{whMBC}			t_{cMBC}/2		ns
MBCLK low level width	t_{wlMBC}			t_{cMBC}/2		ns
MBCLK rise/fall time	t_{rfMBC}	In the slave mode			20	ns
MEN setup time	t_{suMEN1}	MBCLK↓ (MBCLK normal mode)	50			ns
MEN setup time	tS_{uMEN2}	MBCLK↑ (MBCLK inversion mode)	50			ns
MSO output delay time	t_{dMSO1}	MBCLK↑ (MBCLK reverse mode)	−37.5		+50	ns
MSO output delay time	$t_{dMSO}2$	MBCLK↓ (MBCLK inversion mode)	−37.5		+50	ns

Clock normal (SMBCLK = 0) mode



Clock inversion (SMBCLK =1) mode



9.6 Analog Characteristics

Unless otherwise specified, the following conditions must be met.

D/A converter input level: V_{IN} = 0 dBFS (The full-scale input of the D/A converter is defined as 0 dBFS.)
D/A converter input frequency : f_{IN} = 997 Hz
Ambient temperature: T_A = 25°C
Power supply voltage: AV_{DD} = 3.0 V
Sampling frequency: fs = 48 kHz
Output load: R_L = 10 kΩ

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum output level	V_O	Volume = 0 dB	1.8	2.0	–	V_{p-p}
Gain error 1	GE_{max}	volume = 0 dB, 0 dBr = 2.0 V_{p-p}	–1	0	+1	dBr
Gain error 2	GE_{min}	Volume = –45 dB, value relative to G_{Emax} reference	–47	–45	–43	dB
Gain adjustment resolution	G_{step}	Volume = differential error when 0 to –45 dB is set,	1	1.5	2	dB
THD	THD	Volume = 0 dB, Input = –3 dBFS@997 Hz, f = 20kHz	–	–80	–74	dB
Frequency characteristics	GF	Volume = 0 dB, Input = –10 dBm@997 Hz, Output at 997 Hz is used as 0 dB reference.	–1	0	+1	dB
Dynamic range	SND	Volume = 0 dB, INPUT = –60 dBFS, f = 20 Hz, A-weighting filter	80	86	–	dB

9.6.1 Analog block characteristics (reference values)

(1) Audio DAC characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Resolution	RESda			16		bit
Output voltage	VOFSda	When 0 dBFS is output		2.0		V_{p-p}
Absolute gain	Gda	0 dB input	−0.5	0	+0.5	dBr
Frequency characteristics	GRda	−20 dBFS at 997 Hz, 100 to 15 kHz	−0.5	0	+0.5	dBr
Dynamic range	SNDda	Input = −60 dBFS, A-weighting filter	83	89		dB
THD	THDda	Input = −3 dBFS, 997 Hz			−80	dB

(2) Master volume + line output amplifier characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Gain error maximum value	Gvmax	0 dBr = 2.0 Vp-p when 997 Hz and 0 dB are set.	−0.1	0	+0.1	dBr
Gain error minimum value	Gvmin	When 997 Hz and −45 dB are set	−47	−45	−43	dB
Gain adjustment resolution	Gstep	Differential error when 20 kHz to 15 kHz and 0 dB to −45 dB are set	1.0	1.5	2.0	dB
Minimum load resistance			10k			Ω
Maximum load capacitance					20	pF
Maximum output level	SNvo	Input = 2.0 V_{p-p} when 997 Hz and 0 dB are set.		2.0		V_{p-p}
Mute level	ML	When 997 Hz and Mute are set	60			dB
Frequency characteristics	FCvo	0.2 V_{p-p} at 997 Hz. When 0 dB is set, the frequency is 100 kHz to 15 kHz.	−0.5	0	+0.5	dBr
Dynamic range	SNvo	Input = −60 dB, A-weighting filter			83	dB
THD	THDvo	Input = 2.0 Vp-p at 997 Hz			−86	dB

(3) Band gap reference characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	VRO		1.2	1.3	1.4	V
Rise time	VRUP	Capacitance of 0.22 μF		2	5	ms

(4) Regulator characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Current consumption	REG_{idd}	When the output current is 0 mA		(50)		μA
Output voltage	REG_{vo}			1.54		V
Output current	REG_{io}			150		mA
Power up time	REG_{ton}	90% of the output voltage when the output voltage is maximum			(1)	ms
Power down time	REG_{toff}	Output voltage of 0.5 V when the output voltage is maximum			(1)	ms

10. CURRENT CONSUMPTION

Unless otherwise specified, the following conditions must be met.

Sound source master clock: 112 MHz
D/A converter input level: V_{IN} = 0 dBFS (The full scale input of the D/A converter is defined as 0 dBFS.)
D/A converter input frequency: f_{IN} = 997 Hz
Ambient temperature: T_A = 25°C
Power supply voltage: DV_{DD} = 1.54 V, EV_{DD} = 1.8 V, $PLLV_{DD}$ = AV_{DD} = $REGV_{DD}$ = 3.0 V
Sampling frequency: fs = 48 kHz
Output load: R_L = 10 kΩ

The above current values are reference values derived from the μPD9970.

They may be changed without prior notice.

The current value of the EV_{DD} pin is a reference value measured when no loads are applied. It varies depending on external environments such as loads and clock rates.

(1/2)

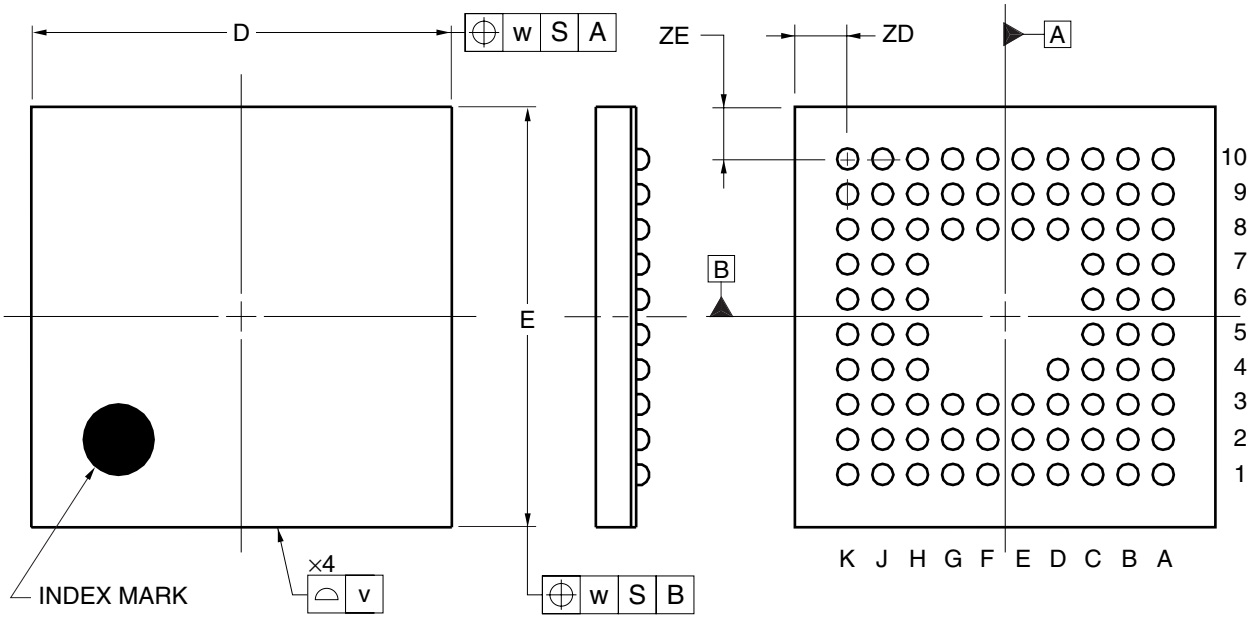
Parameter	Symbol	Conditions	Power Supply Pin	MIN	TYP	MAX	Unit
Current consumption during output from sound generator to DAC	I_{DD1}	MIDI playback, 3DA is on, EQ is on, stereo line output, and no regulators are used (REGUSE_B = EV_{DD})	DV_{DD}			120	mA
			AV_{DD}			12	mA
			$PLLV_{DD}$			9	mA
			$REGV_{DD}$		0.5		μA
			EV_{DD}			3	mA
Current consumption during output from sound generator to ASO	I_{DD2}	MIDI playback, 3DA is on, EQ is on, ASO data output, and no regulators are used (REGUSE_B = EV_{DD})	DV_{DD}			120	mA
			AV_{DD}			2	mA
			$PLLV_{DD}$			9	mA
			$REGV_{DD}$		0.5		μA
			EV_{DD}			3	mA
Current consumption during output from ASI to DAC	I_{DD3}	Audio playback, sound generator is off, 3DA is off, EQ is off, stereo line output, and no regulators are used (REGUSE_B = EV_{DD})	DV_{DD}			10	mA
			AV_{DD}			12	mA
			$PLLV_{DD}$			9	mA
			$REGV_{DD}$		0.5		μA
			EV_{DD}			3	mA
Current consumption during output from ASI to ASO	I_{DD4}	Audio loop back, sound generator is off, 3DA is off, EQ is off, ASO data output, and no regulators are used (REGUSE_B = EV_{DD})	DV_{DD}			10	mA
			AV_{DD}			2	mA
			$PLLV_{DD}$			9	mA
			$REGV_{DD}$		0.5		μA
			EV_{DD}			3	mA

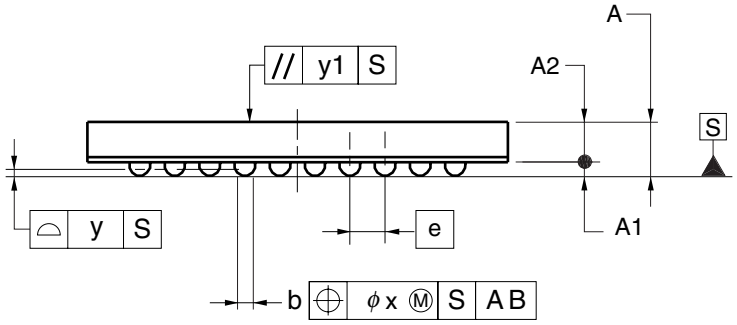
(2/2)

	Parameter	Symbol	Conditions	Power Supply Pin	MIN	TYP	MAX	Unit
	Software standby current 1	I_{STB1}	Software standby current (except EVDD) when all signals are stopped REGCNT = 0 REGUSE_B = EV_{DD}	DV_{DD}		0		μA
				AV_{DD}		0.5		μA
				$PLLV_{DD}$		0.5		μA
				$REGV_{DD}$		0.5		μA
	Software standby current 2	I_{STB2}	Software standby current (except EVDD) when all signals are stopped REGCNT = 0 REGUSE_B = EV_{DD}	DV_{DD}		0		μA
				AV_{DD}		0.5		μA
				$PLLV_{DD}$		0.5		μA
				$REGV_{DD}$		0.5		μA
★	Hardware standby current	I_{STBH}	EVDD current at the time of reset (RESET_B = low)	EV_{DD}		0.2	5	μA

11. PACKAGE DRAWING

85-PIN TAPE FBGA (6x6)





(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.10
E	6.00±0.10
v	0.15
w	0.20
e	0.50
A	0.83±0.10
A1	0.18±0.05
A2	0.65
b	0.32±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P85F9-50-BA3

12. RECOMMENDED SOLDERING CONDITIONS

The μPD9971 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

- **μPD9971F9-BA3-A: 85-pin tape FBGA (6 × 6)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°Cor below, Time: 60 sec. max. (at 220°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours) Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Products packed in a medium other than a heat-resistance tray (such as a magazine, taping, and non-heat-resistance tray) cannot be baked.	IR60-107-2

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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