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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD9930

LINEAR CODEC FOR DIGITAL CELLULAR TELEPHONE

The μPD9930 is a +3 V single power operation, low power consumption linear CODEC LSI developed for digital cellular telephone use.

CODEC has a wide dynamic use.

This IC also features a microphone/receiver amplifier, a tone generator, DAI (Digital Audio Interface: conforming to GSM11.10), and a power-saving function. These functions can be controlled by microcontroller.

In addition, 21 mW (TYP.) low power consumption is enabled during 3 V operation.

FEATURES

- +3 V single power supply
- Low power consumption
  In operation: 7 mA (TYP.) (V_{DD} = 3 V)
  In stand-by mode: 50 μA (TYP.) (V_{DD} = 3 V)
- CODEC
  - 13-bit precision linear coding
  - Transmission level can be controlled by microcontroller.
- Analog input/output funciton
  - Low noise microphone amplifier
  - High output receiver amplifier
    Piezo-electric receiver can be directly driven.
    Gain canbe controlled by microcontroller.
  - On-chip amplifier for accessory input/output
- Tone generator
  - Frequency, generating pattern and gain can be controlled by microcontroller.
  - DTMF generation function
  - Various service tone generation function
  - GSM triple tone generation function
  - Desired tone frequency can be registered (0.3 to 3.4 kHz)
- DAI
  - Conforming to GSM11.10
  - Test mode can be set by terminal or microcontroller command.
- Stand-by mode
  - Rise time at time of stand-by clearing: 30.5 ms (TYP.)
- Master clock generation PLL (external clock input: 8 kHz)
- Tone interrupt pattern output function
- Ringer output function

ORDERING INFORMATION

Part Number	Package
μPD9930G-22	44-pin plastic QFP (10 × 10 mm)

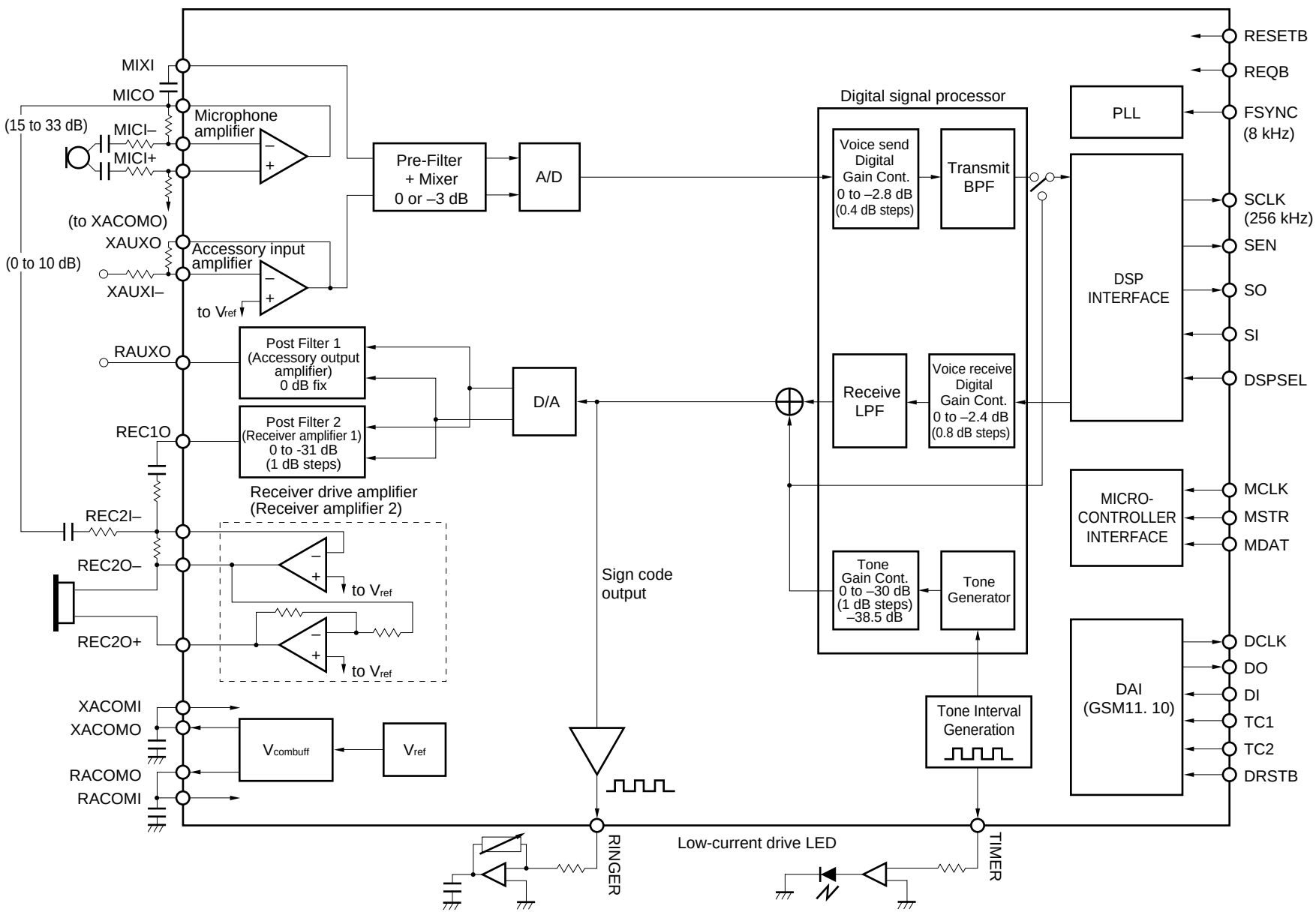
The information in this document is subject to change without notice.

Document No. S11616EJ2V0DS00 (2nd edition)
(Previous No. IC-3342)
Date Published November 1996 N
Printed in Japan

The mark ★ shows major revised points.

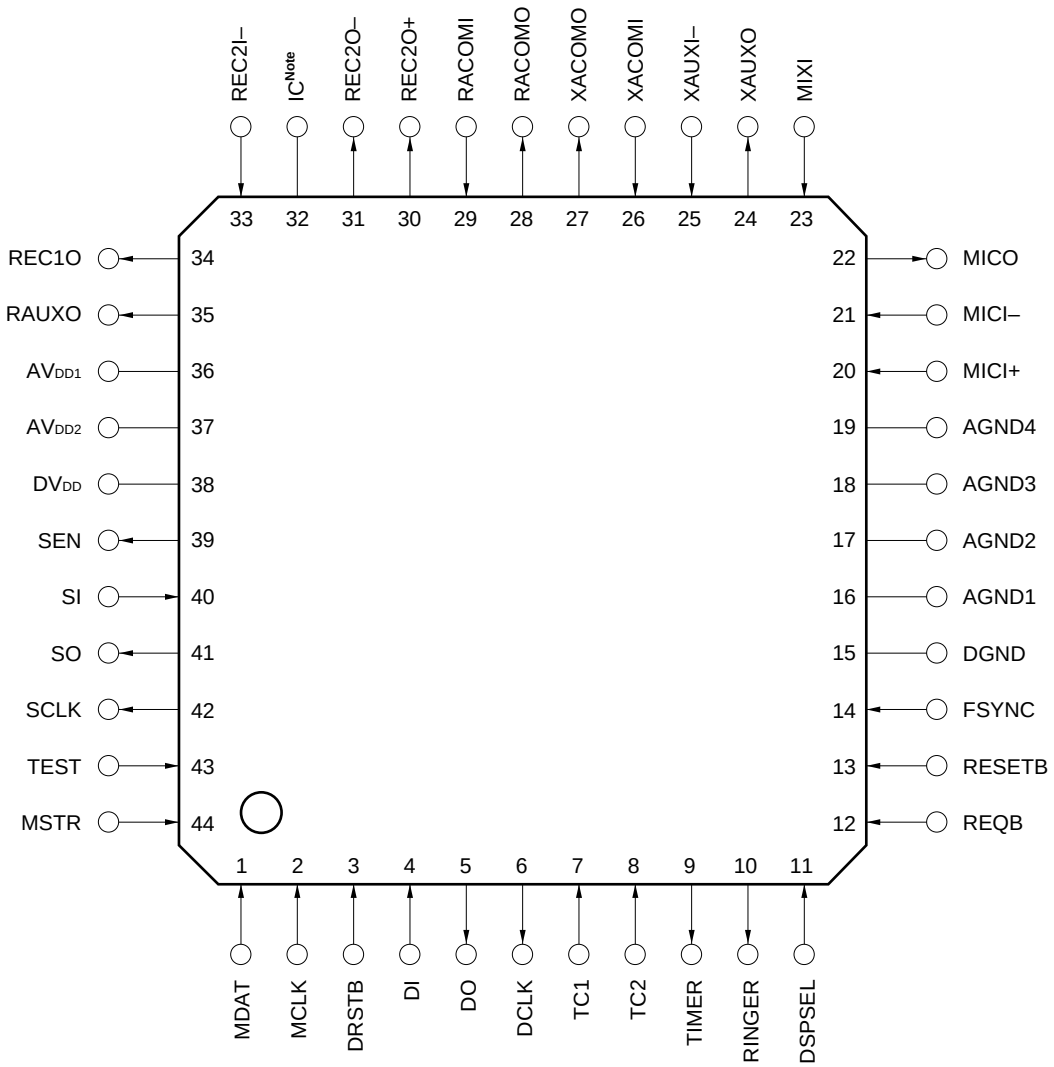
Phase-out/Discontinued

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

44-pin plastic QFP (10 x 10 mm)



Note Internal connection; leave unconnected

Pin Name

AGND1-AGND4	: Analog Ground
AV_{DD1}, AV_{DD2}	: Analog Power Supply
DCLK	: DAI (Digital Audio Interface) Clock Output
DGND	: Digital Ground
DI	: DAI Serial Input
DO	: DAI Serial Output
DRSTB	: DAI Reset
DSPSEL	: Digital Signal Processor Select
DV_{DD}	: Digital Power Supply
FSYNC	: Frame Synchronization Signal Input
IC	: Internally Connected
MCLK	: Microcontroller Synchronous Clock
MDAT	: Microcontroller Serial Data
MICI+	: Microphone Amplifier Input Non-Inverted
MICI–	: Microphone Amplifier Input Inverted
MICO	: Microphone Amplifier Output
MIXI	: Mixer Input
MSTR	: Microcontroller Strobe
RACOMI	: Receive Common Reference Voltage Input
RACOMO	: Receive Common Reference Voltage Output
RAUXO	: Receive Auxiliary Amplifier Output
REC1O	: Receive Amplifier 1 Output
REC2I–	: Receive Amplifier 2 Input Inverted
REC2O+	: Receive Amplifier 2 Output Non-Inverted
REC2O–	: Receive Amplifier 2 Output Inverted
REQB	: Request
RESETB	: Reset
RINGER	: Ringer
SCLK	: Serial Data Synchronous Clock Output
SEN	: Serial Data Output Enable
SI	: Serial Data Input
SO	: Serial Data Output
TC1, TC2	: DAI Mode Control
TEST	: Test
TIMER	: Timer
XACOMI	: Transmit Common Reference Voltage Input
XACOMO	: Transmit Common Reference Voltage Output
XAUXI–	: Transmit Auxiliary Amplifier Input Inverted
XAUXO	: Transmit Auxiliary Amplifier Output

CONTENTS

1. PIN FUNCTIONS

1.1 LIST OF PIN FUNCTIONS

Table 1-1 List of Pin Functions (1/2)

Pin No.	Pin Name	Input/Output	Function
1	MDAT	Input	Microcontroller interface serial input
2	MCLK	Input	Microcontroller interface clock input
3	DRSTB	Input	DAI (Digital Audio Interface) reset input This is reset at low level. Internally pulled high.
4	DI	Input	DAI serial input Internally pulled high.
5	DO	Output	DAI serial output Hi-Z in normal operation (TC1 = TC2 = low level)
6	DCLK	Output	DAI clock output (104 kHz) Hi-Z in normal operation
7	TC1	Input	DAI mode control Selection of test mode specified by GSM11.10 in combination with TC1 and TC2 L: Low level H: High level TC1 and TC2 pins are internally pulled down.
8	TC2	Input	
9	TIMER	Output	Timer output. Output of rectangular wave synchronized with tone intermittent pattern.
10	RINGER	Output	Ringer tone output. Output of rectangular wave synchronized with tone frequency.
11	DSPSEL	Input	Selection of DSP interface input/output timing mode. Connect to V_{DD} or GND. (V_{DD} = mode 1, GND = mode 2)
12	REQB	Input	Input of DSP interface data transmit request signal. Serial data can be input/output at low level.
13	RESETB	Input	System reset input. This is reset at low level. Initializes all control registers. Reset when turning power on.
14	FSYNC	Input	Send/receive frame synchronization signal (8 kHz) input
★ 15	DGND	—	Digital ground. Connect to a digital ground line near μPD9930 pins.
16	AGND1	—	Analog ground. Connect to an analog ground line near μPD9930 pins.
17	AGND2	—	
18	AGND3	—	
19	AGND4	—	
20	MICI+	Input	Microphone amplifier non-inverted input
21	MICI–	Input	Microphone amplifier inverted input
22	MICO	Output	Microphone amplifier output. Connect microphone amplifier gain adjust resistor. Outputs sidetone signal to REC2I- pin.
23	MIXI	Input	Pre-filter + mixer input
24	XAUXO	Output	Accessory input amplifier output. Connect accessory input amplifier gain adjust resistor.

TC2	TC1	Test mode specification
L	L	Normal operation
L	H	Speech encoder test mode
H	L	Speech decoder test mode
H	H	Acoustic device test mode

Table 1-1 List of Pin Functions (2/2)

Pin No.	Pin Name	Input/Output	Function
25	XAUXI–	Input	Accessory input amplifier inverted input
26	XACOMI	Input	Voice send internal reference voltage input
27	XACOMO	Output	Voice send internal reference voltage (1.2 V) output
28	RACOMO	Output	Voice receive internal reference voltage (1.2 V) output
29	RACOMI	Input	Voice receive internal reference voltage input
30	REC2O+	Output	Receiver amplifier 2 non-inverted output
31	REC2O–	Output	Receiver amplifier 2 inverted output
32	IC	—	Internal connection; leave unconnected
33	REC2I–	Input	Receiver amplifier 2 inverted input Connect sidetone gain adjust resistor.
34	REC1O	Output	Receiver amplifier 1 output
35	RAUXO	Output	Accessory output amplifier output
36	AV_{DD1}	—	Analog power. Connect to an analog power supply line near μPD9930 pins.
37	AV_{DD2}	—	
★ 38	DV_{DD}	—	Digital power. Connect to a digital power supply line near μPD9930 pins.
39	SEN	Output	DSP interface enable signal output
40	SI	Input	DSP interface serial input
41	SO	Output	DSP interface serial output
42	SCLK	Output	DSP interface clock output (256 kHz)
43	TEST	Input	Set at high level
44	MSTR	Input	Microcontroller interface strobe signal input

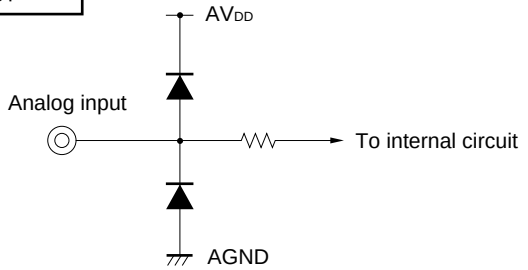
★ **Caution Short-circuit the XACOMI and XACOMO pins at a location as close to the pins of the μPD9930 as possible. Connect a capacitor (chip capacitor or electrolytic capacitor) between this short-circuited portion and analog ground.**

The same applies to the RACOMI and RACOMO pins.

The transmission/reception level is determined by these reference pins. Therefore, make sure that these pins are not affected by noise or fluctuation of ground potential due to current.

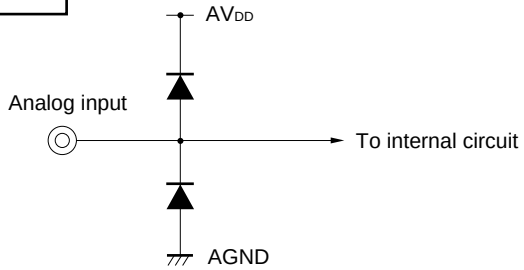
1.2 PIN EQUIVALENT CIRCUIT

Type 1



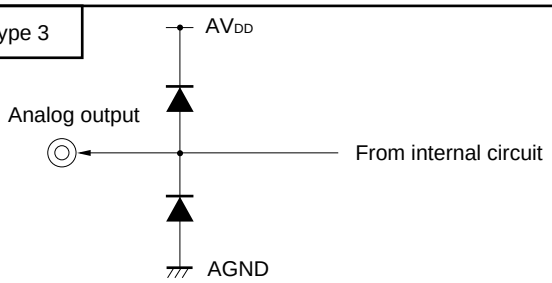
Pin Name MICI+, MICI–, XAUXI–, REC2I–

Type 2



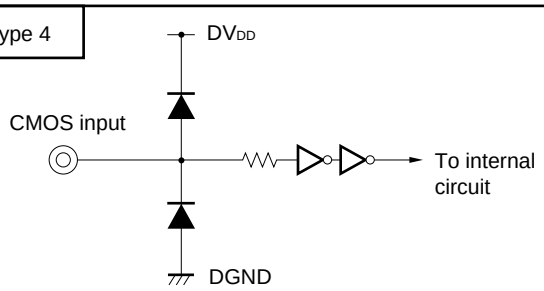
Pin Name MIXI, XACOMI, RACOMI

Type 3



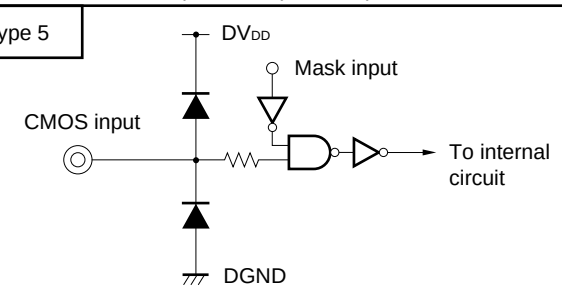
Pin Name MICO, XAUXO, XACOMO, RACOMO, REC2O+, REC2O–, REC1O, RAUXO

Type 4



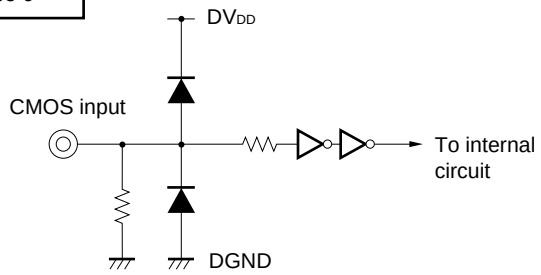
Pin Name MDAT, MCLK, DSPSEL, REQB, RESETB, FSYNC, TEST, MSTR

Type 5



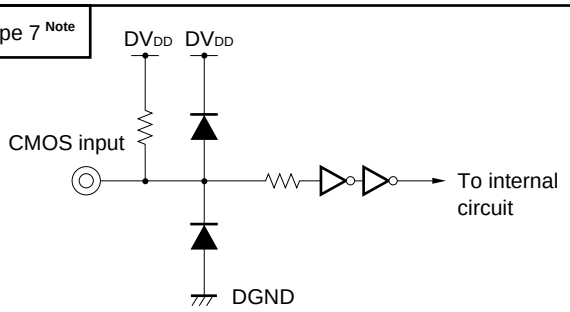
Pin Name SI

Type 6 [Note]



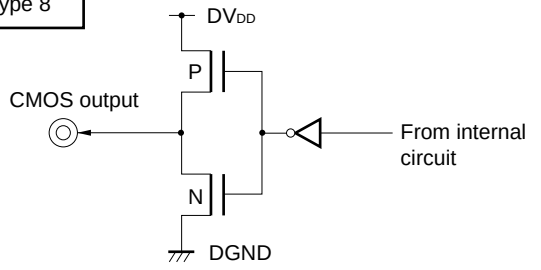
Pin Name TC1, TC2

Type 7 [Note]



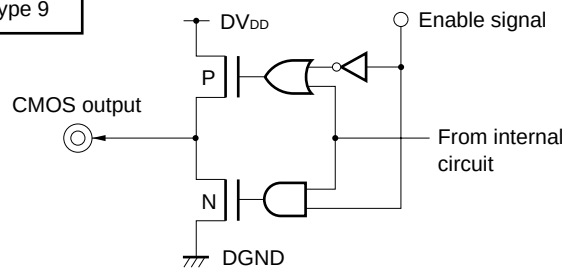
Pin Name DRSTB, DI

Type 8



Pin Name TIMER, RINGER, SEN, SO, SCLK

Type 9



Pin Name DO, DCLK

Note In normal mode, set the output of drive IC side to high impedance for reducing power consumption.

★ 2. BLOCK FUNCTIONS

2.1 CODEC

2.1.1 Audio Codec

Audio analog signal and linear code conversion.

- Input/output format: 16 bits (2's complement)
- Accuracy: 13 bits

2.1.2 Audio Analog Input

Includes microphone input and accessory input.

(1) Microphone amplifier

Amplifiers differential input signals from the microphone to the required gain.

(2) Accessory input amplifier

Amplifiers the accessory input signal to the required gain.

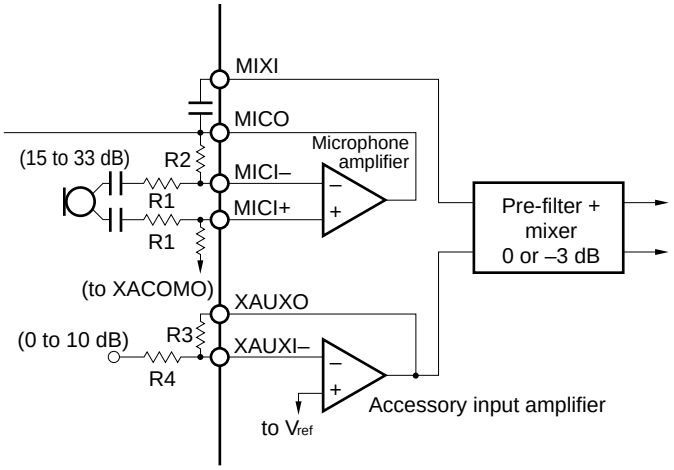
(3) Pre-filter + mixer

Selects the output signal of microphone amplifier and accessory input amplifier, and inputs these to A/D converter after controlled gain.

Table 2-1 Analog Input Function

Function \ Amplifier	Microphone Amplifier	Accessory Input Amplifier	Pre-filter + Mixer
Gain setting method	External resistor	External resistor	Microcontroller command
Gain setting range	15 to 33 dB $20 \log \frac{R2}{R1}$ (dB)	0 to 10 dB $20 \log \frac{R3}{R4}$ (dB)	0 or –3 dB
Minimum resistive load	50 kΩ (Including gain setting resistance)	300 kΩ (Including gain setting resistance)	—
Maximum capacitive load	20 pF	20 pF	—
Maximum output level	0.6 $V_{0\text{-}p}$	0.6 $V_{0\text{-}p}$	—

Figure 2-1 Analog Input Block



2.1.3 Audio Analog Output

Includes receiver output and accessory output. Sidetone addition is also possible.

(1) Post filter 2 (receiver amplifier 1)

This circuit adjusts the gain of D/A differential output signal (volume control), and then converts it to single output signal.

(2) Receiver drive amplifier (receiver amplifier 2)

This is differential output amplifier that can directly drive a piezo-electric receiver (when using a dynamic receiver, an additional external amplifier is necessary). The sidetone is added in this circuit.

(3) Post filter 1 (accessory output amplifier)

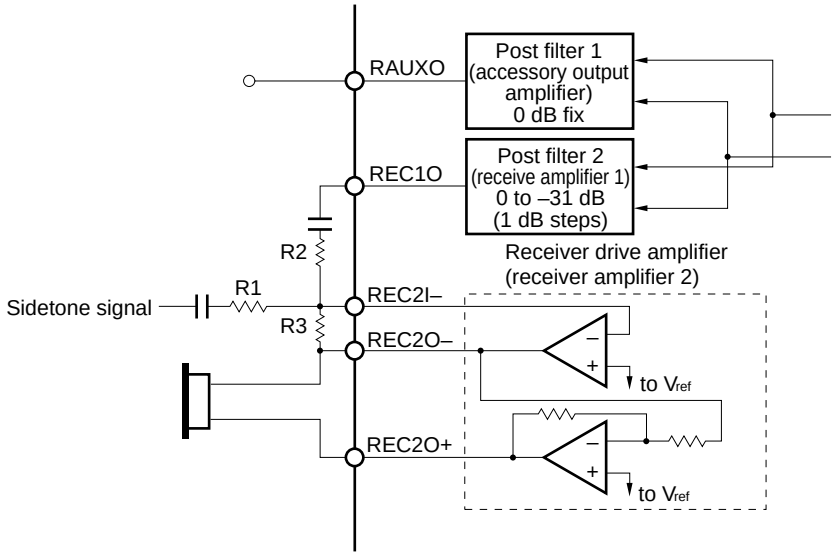
This circuit converts D/A differential output signal to single output signal. Connected to the earphone of the head set (capacitance load), etc.

Table 2-2 Analog Output Functions

Function \ Amplifier	Receiver Amplifier 1	Receiver Amplifier 2	Accessory Output Amplifier
Gain setting method	Microcontroller command	External resistor	—
Gain setting range	0 to –31 dB (1 dB steps)	Voice receive signal gain: $-\infty$ to + 10 dB $20 \log \frac{R3}{R2}$ (dB) + 6 dB[Note] Sidetone signal gain: $-\infty$ to + 3 dB $20 \log \frac{R3}{R1}$ (dB) + 6 dB[Note]	—
Minimum resistive load	100 kΩ	2 kΩ	100 kΩ
Maximum capacitive load	20 pF	60 nF	100 pF
Maximum output level	0.6 $V_{0\text{-}p}$	4 $V_{p\text{-}p}$ (Differential output)	0.6 $V_{0\text{-}p}$

Note Conversion result (single output → differential output)

Figure 2-2 Analog Output Block

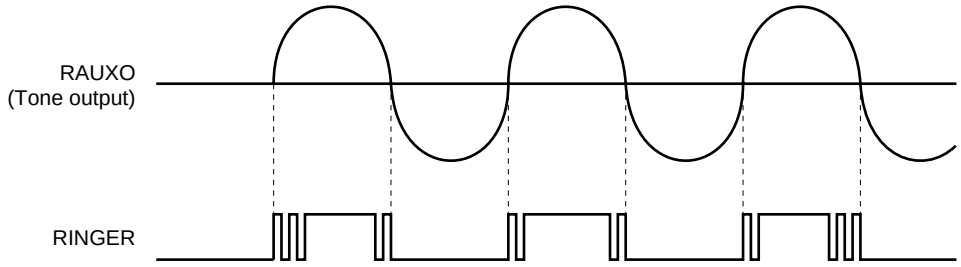


2.1.4 Audio Digital Accessory Output

(1) Ringer output (RINGER pin)

- Outputs rectangular waves of the same signal frequency as tone signal frequency.
- The output is controlled by turning off power to the output buffer with a control register.

Figure 2-3 RINGER Output

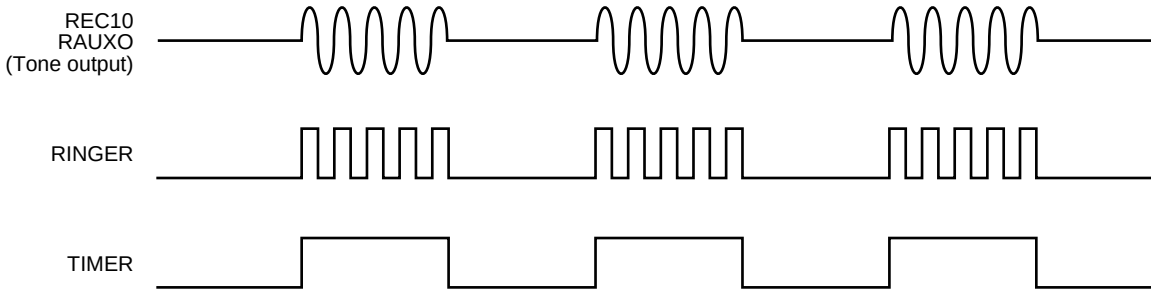


The RINGER signal tends to bounce when the tone output (RAUXO) signal crosses its zero level, and this tendency increases as the tone output gain decreases (lower than 0 dB).
When using RINGER pin, tune the tone output gain by TNGCR (Tone gain control register) to 0 dB.

(2) Timer (tone interval) output (TIMER pin)

Outputs rectangular waves of the same pattern as the tone signal interrupt pattern. This is used to make the LED blink in synchronization with the ringer tone.

Figure 2-4 Digital Accessory Output Waveform



2.1.5 Audio Digital Signal Processor

Send signal digital BPF processing, receive signal digital LPF processing, transmission level (digital gain) control, and tone generation processing.

(1) Voice send signal digital gain fine adjustment function

Performs gain fine adjustment for voice send signal by digital coefficient multiplication. Together with prefilter gain adjustment, fine adjustment is possible at a width of 5.8 dB.

(2) Voice receive signal digital gain fine adjustment function

Performs fine adjustment of gain for voice receive signal by digital coefficient multiplication.

(3) Tone generation function

Generates single-tone and dual-tone audible signals. Tone frequency, interrupt pattern, gain, generation/stop can be controlled by microcontroller command. GSM triple tone can be generated by special command.

Table 2-3 Digital Gain Control Functions

	Voice Send Signal Gain Control	Voice Receive Signal Gain Control	Tone Gain Control
Gain setting method	Microcontroller command	Microcontroller command	Microcontroller command
Gain setting range	0 to –2.8 dB (0.4 dB steps)	0 to –2.4 dB (0.8 dB steps)	0 to –30 dB (1 dB steps), –38.5 dB

2.1.6 Power Up/Down Control

The μPD9930 includes a power down function for reducing power consumption. Power down control is by the two methods described below.

(1) Input/output amplifier power up/down control

Power up/down for both the input and output amplifiers can be controlled.

When the power down function is used for all input amplifiers, both pre-filter and A/D enter the power down state.

When the power down function is used for the accessory output amplifier and the receiver 1 amplifier, the D/A also enters power down state.

(2) Stand-by mode

Low power consumption can be realized in the mode in which all chip operation is stopped. The stand-by mode is set by power down command. Operation restarts by power up command.

The following control registers are used to enable the control described above.

Control Method	Registers Used
Power up/down control of input/output amplifier (not including receiver amplifier 2)	Input/output amplifier control register (AMPCR)
Power up/down control of receiver amplifier 2	Send analog gain/receiver amplifier 2 control register (TXGCR)
Set/clear of standby mode	Power up control command (PUPCMD) Power down control command (PDWCMD)

An outline diagram of power down control is shown in **Figure 2-5**.

Figure 2-5 Power Down Control

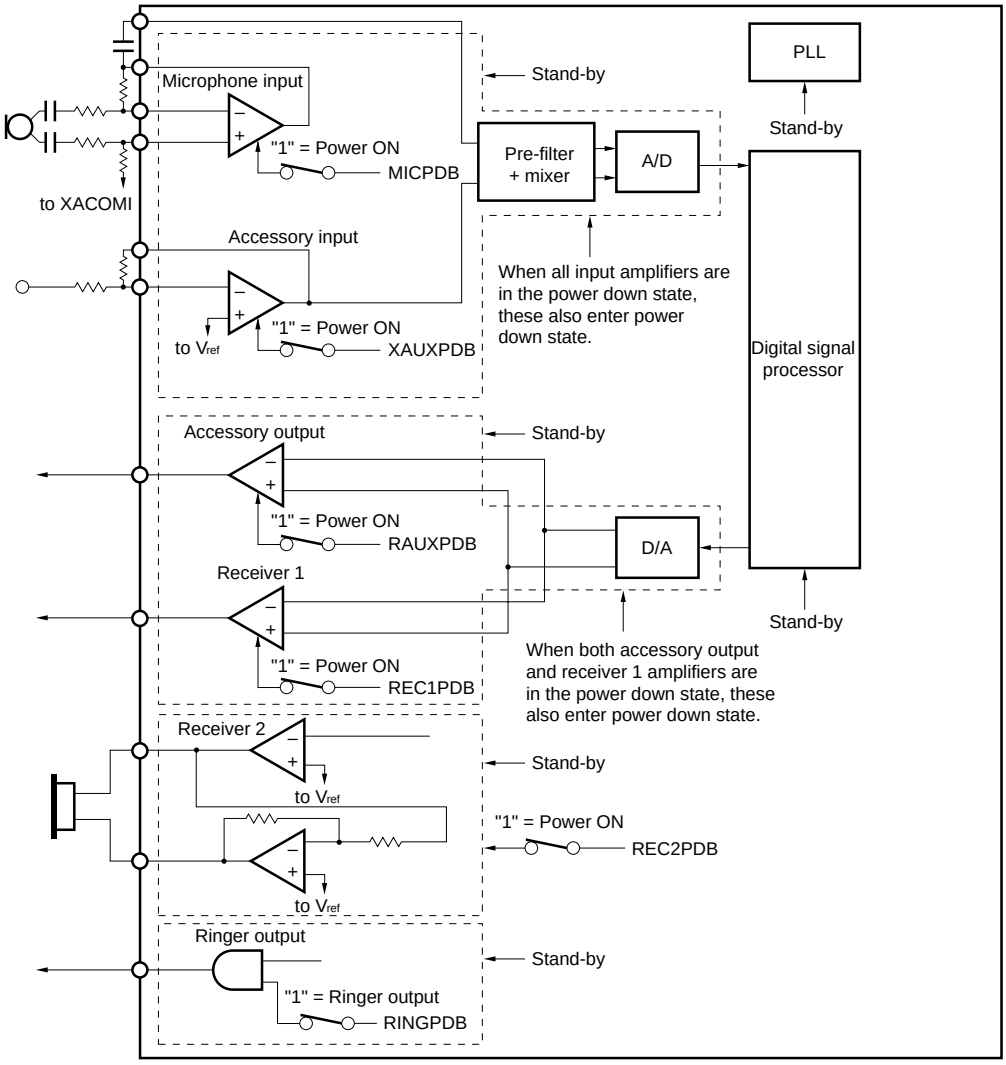
Register address			AMPCR				
0	0	0	MICPDB	XAUXPDB	REC1PDB	RAUXPDB	RINGPDB

Register address					TXGCR		
0	0	0	1	1	0	REC2PDB	TXAG

Power up command								HEX[Note]	
								M	L
0	1	1	1	1	0	—	—	78H	1EH

Power down command								HEX[Note]	
								M	L
0	1	1	1	0	0	—	—	70H	0EH

Note M: HEX value with MSB first L: HEX value with LSB first



Caution MICPDB and XAUXPDB cannot enter the power up state at the same time (MICPDB = XAUXPDB = "1").

(3) Input/output amplifier control register (AMPCR)

This is a 5-bit register for power up/down control of each input/output amplifier (not including receiver amplifier 2), and for ringer output ON/OFF control.

Remark For information on power up/down control of receiver amplifier 2, refer to **4.1.1 Voice Send Analog Gain/ Receiver Amplifier 2 Control Register (TXGCR)**.

Figure 2-6 Input/Output Amplifier Control Register

Register address			AMPCR				
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	MICPDB	XAUXPDB	REC1PDB	RAUXPDB	RINGPDB

MICPDB	Microphone amplifier power control
0	Power down
1	Power up

XAUXPDB	Accessory input amplifier power control
0	Power down
1	Power up

REC1PDB	Receiver amplifier 1 power control
0	Power down
1	Power up

RAUXPDB	Accessory output amplifier power control
0	Power down
1	Power up

RINGPDB	Ringer output control
0	Sets output at low level.
1	Output enable

Remarks 1. In the stand-by mode, all amplifiers enter the power down state regardless of input/output control register settings. However, register contents are held unless reset or written, so when the stand-by mode is cleared by power up command, the command prior to the stand-by mode is resumed.

2. The microphone and accessory amplifiers cannot enter the power up (D4 = D3 = "1") state at the same time.

Table 2-4 Function Specification by Input/Output Amplifier Control Register

Register address			AMPCR					Microphone amplifier	Accessory input amplifier	Receiver amplifier 1	Accessory output amplifier	Ringer output	HEX[Note]		Remarks
D7	D6	D5	D4	D3	D2	D1	D0						M	L	
0	0	0	0	0	0	0	0	X	X	X	X	Stop	00H	00H	At reset
			0	0	0	0	1	X	X	X	X	Output	01H	80H	
			0	0	0	1	0	X	X	X	O	Stop	02H	40H	
			0	0	0	1	1	X	X	X	O	Output	03H	C0H	
			0	0	1	0	0	X	X	O	X	Stop	04H	20H	
			0	0	1	0	1	X	X	O	X	Output	05H	A0H	
			0	0	1	1	0	X	X	O	O	Stop	06H	60H	
			0	0	1	1	1	X	X	O	O	Output	07H	E0H	
			0	1	0	0	0	X	O	X	X	Stop	08H	10H	
			0	1	0	0	1	X	O	X	X	Output	09H	90H	
			0	1	0	1	0	X	O	X	O	Stop	0AH	50H	
			0	1	0	1	1	X	O	X	O	Output	0BH	D0H	
			0	1	1	0	0	X	O	O	X	Stop	0CH	30H	
			0	1	1	0	1	X	O	O	X	Output	0DH	B0H	
			0	1	1	1	0	X	O	O	O	Stop	0EH	70H	
			0	1	1	1	1	X	O	O	O	Output	0FH	F0H	
			1	0	0	0	0	O	X	X	X	Stop	10H	08H	
			1	0	0	0	1	O	X	X	X	Output	11H	88H	
			1	0	0	1	0	O	X	X	O	Stop	12H	48H	
			1	0	0	1	1	O	X	X	O	Output	13H	C8H	
			1	0	1	0	0	O	X	O	X	Stop	14H	28H	
			1	0	1	0	1	O	X	O	X	Output	15H	A8H	
			1	0	1	1	0	O	X	O	O	Stop	16H	68H	
			1	0	1	1	1	O	X	O	O	Output	17H	E8H	

Note M: HEX value with MSB first
L: HEX value with LSB first

Remark O: Power up X: Power down

(4) Power up/down command (PUPCMD/PDWCMD)

The stand-by mode is set and cleared by the following two special commands. When resetting, the stand-by mode is set.

Figure 2-7 Power Down Command (Sets to stand-by mode)

	D7	D6	D5	D4	D3	D2	D1	D0
PDWCMD	0	1	1	1	0	0	X	X

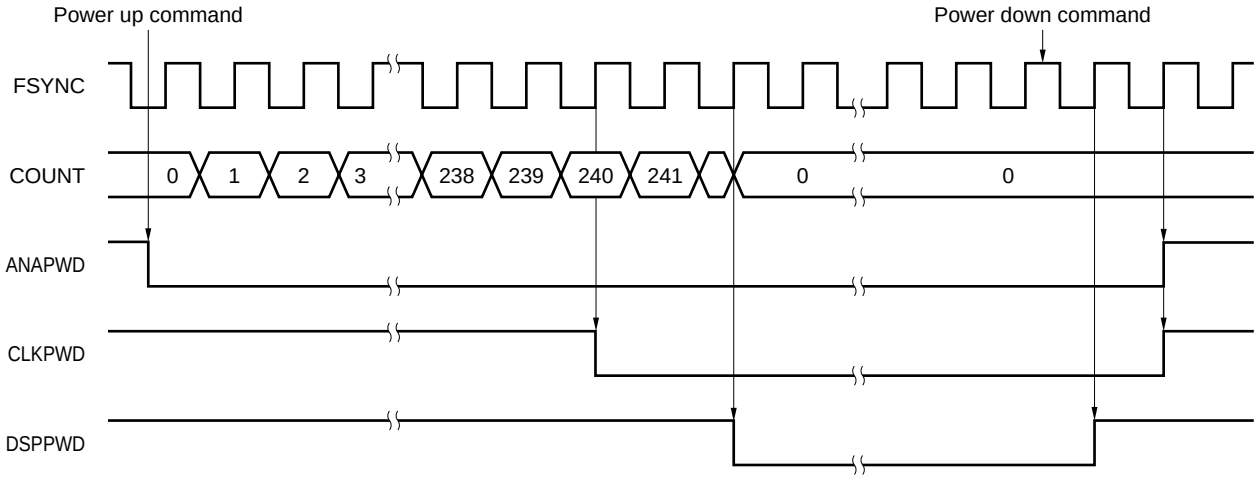
Remark X: Don't Care

Figure 2-8 Power Up Command (Clears stand-by mode)

	D7	D6	D5	D4	D3	D2	D1	D0
PUPCMD	0	1	1	1	1	0	X	X

Remark X: Don't Care

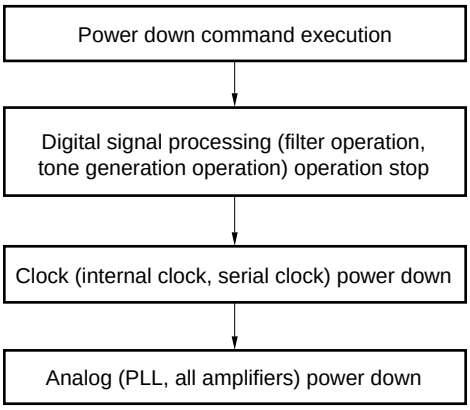
Power up/down timing



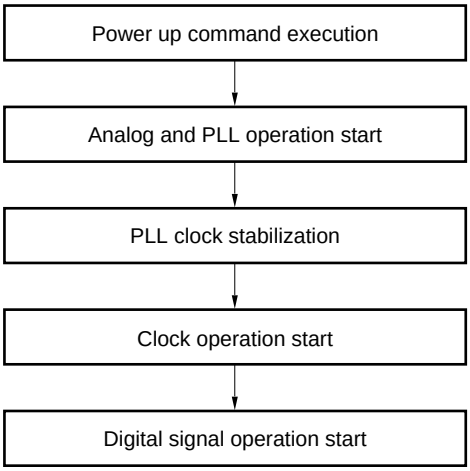
Remarks COUNT: Internal counter (counts with an 8-kHz internal clock)
ANAPWD: Analog power down (power down when high)
CLKPWD: Clock power down (power down when high)
DSPPWD: Signal processing power down (power down when high)

(5) Power up/down sequence

(a) Power down sequence



(b) Power up sequence



Remarks 1. The DSP interface serial input/output operation does not stop or start when switching to power up/down.

2. Rising time from standby mode to normal operation mode is about 30.5 ms after execution of the power up command.

3. FSYNC can be stopped at power down. However, input of the FSYNC clock is necessary during operation and in the above sequence.

2.1.7 Microcontroller Interface

The μPD9930 can control internal functions by microcontroller command. A clock synchronous serial I/O is incorporated to receive command.

A clocked serial interface is provided to receive microcontroller commands. A microcontroller connection example is shown in **Figure 2-9**. 8-bit length data is received by the serial clock (MCLK), serial input (MDAT), and strobe input (MSTR) lines[Note].

The timing chart is shown in **Figure 2-10**. By reading data to the internal shift register and setting MSTR to high level at the MCLK rising point, it is latched to the internal control register. Data transfer must be made with LSB first.

Note When 8 bits or more (9 MCLK clocks or more) data is input, the last 8-bit which is input immediately before the active edge of MSTR is recognized as a control command.

Figure 2-9 Example of Connection with Microcontroller

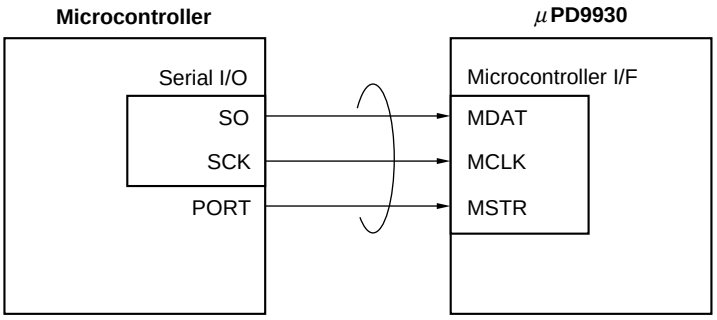
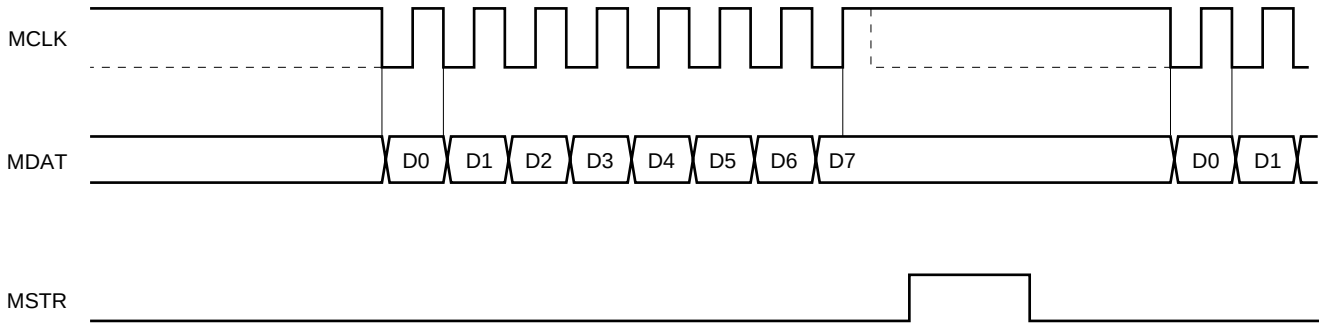


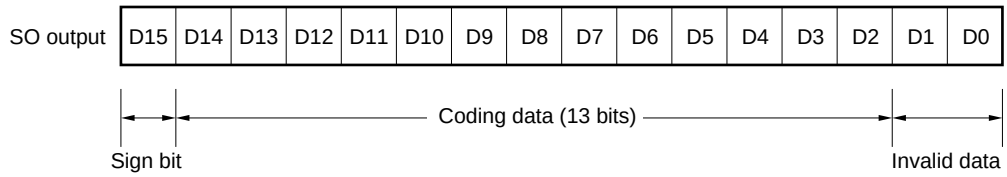
Figure 2-10 Microcontroller Interface Timing Chart



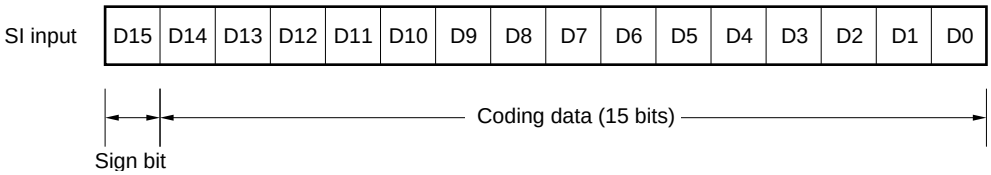
2.1.8 DSP Interface

A clock synchronous serial I/O is built-in to exchange voice send/receive coding data with an external DSP. 16-bit data is transferred at 8 kHz by the serial clock (SCLK = 256 kHz), serial input (SI), serial output (SO), and enable output (SEN) lines. The REQB is a terminal for allowing/inhibiting data transmission. There are two modes for data input and output timing, and either can be selected by the DSPSEL terminal. Select the mode matching the DSP serial interface input/output timing. Data format is as follows: Both SO output and SI input are in 2's complement format with MSB first.

Figure 2-11 Data Format in DSP Interface



Remark A full code is output when the SO pin is +3.17 dBm0 (A/D 1.2 V_{p-p}).



Remark When a full code is input to the SI pin, the accessory output is 1.2 V_{p-p}.

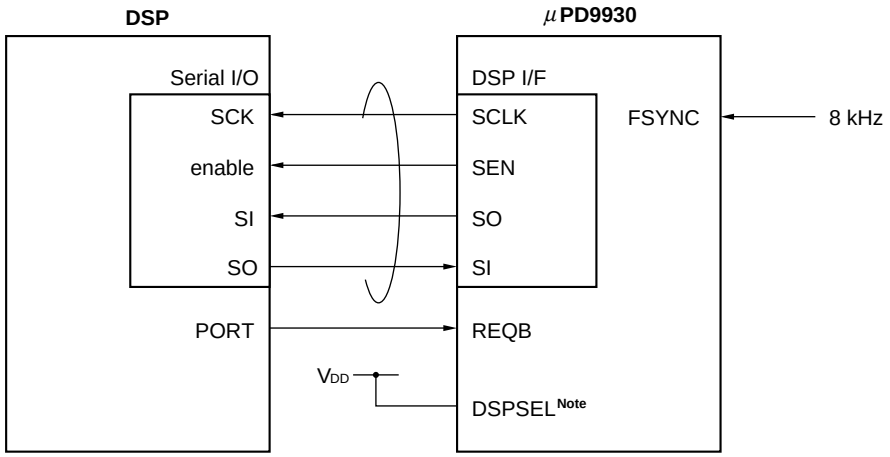
Table 2-5 DSP Input/Output Timing Mode Selection

Pin input	Mode
DSPSEL	
H	MODE1
L	MODE2

Table 2-6 Allowing Data Transmission

REQB pin Input	Data Transmission
L	Data transmission is allowed. Enable signal (SEN) is output at rising edge of FSYNC (8 kHz), and data input/output is started.
H	Enable signal is not output and data are not input or output.

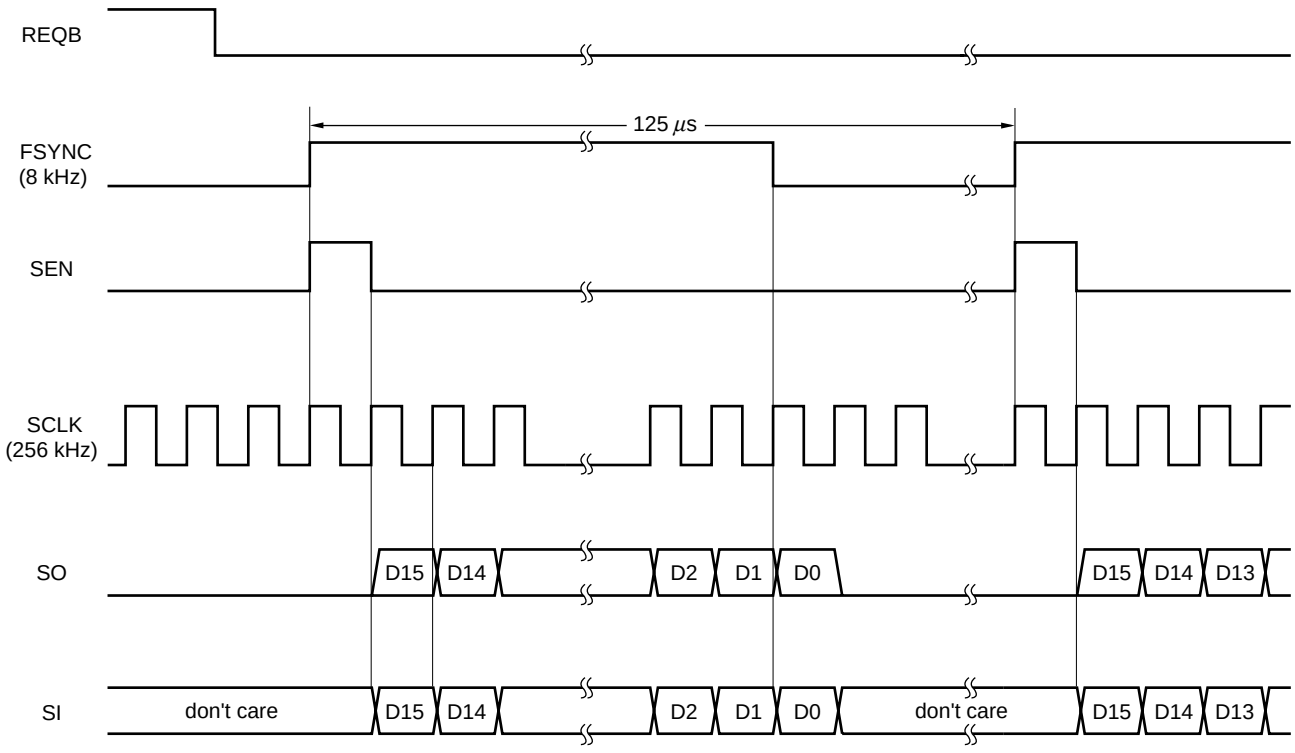
Figure 2-12 Example of Connection with DSP (Mode 1)



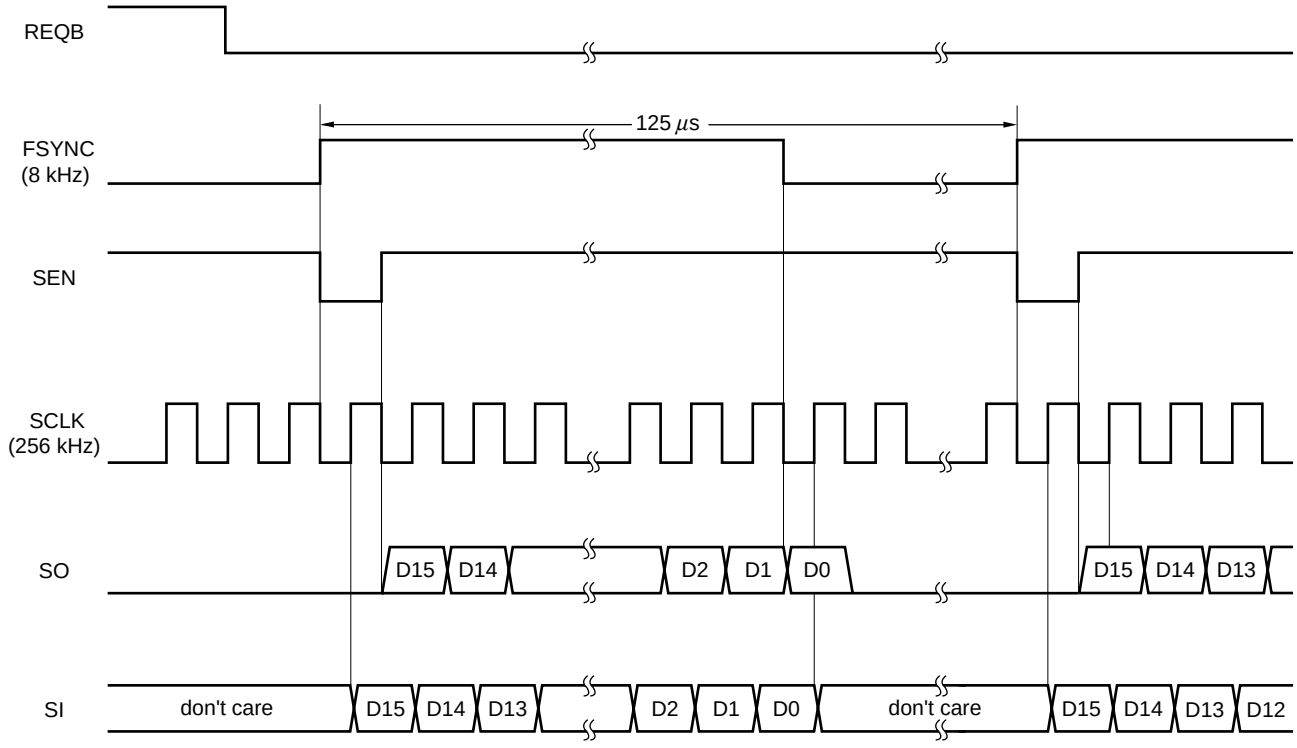
Note When using with mode 2, connect DSPSEL to GND.

Figure 2-13 DSP Interface Timing Chart

(a) Mode 1 (DSPSEL = V_{DD})



(b) Mode 2 (DSPSEL = GND)



2.1.9 DAI (Digital Audio Interface)

Has a on-chip circuit enabling DAI functions specified in GSM11.10. The receive system has a on-chip LPF only. If a BPF is necessary, it should be mounted externally. System configuration at the time of DAI test mode is shown in **Figure 2-15**. The DAI terminal is connected to the system simulator via the pin 25 DSUB socket. The test mode can be selected by terminals TC1 or TC2, or by microcontroller command. DAI mode should be set after completing power-up operation (30.5 ms after executing power-up command).

When changing the modes from DAI to normal, either of the following operations should be executed.

- After specifying normal mode, input the DAI reset signal (DRSTB = low).
- Input reset signal (RESETB = low).

When specifying by command, test control register mode specification bits (ITC1, ITC2) are used (Refer to **4.4.1 Test Control Register (TSTCR)**.).

Timing for each mode is shown in **Figures 2-16** through **2-20**.

For operation at the time of each mode, refer to **Figure 4-13 Test Mode Operation**.

Table 2-7 DAI Test Mode Specification

TC2 (ITC2)	TC1 (ITC1)	Test mode specification	Function
0	0	Normal operation[Note]	Normal operation. This mode is set at system reset (when RESETB = low) regardless of status of TC1 and TC2.
0	1	Speech encoder test mode	Outputs data input from DI pin to DSP (speech encoder) from SO pin. Input is started at rising edge of first FSYNC (8-kHz external clock input) after execution of mode specification, and outputting data to DSP is started at next rising edge of FSYNC.
1	0	Speech decoder test mode	Outputs speech decoder output data input from SI pin from DO pin. Inputting data from DSP is started at rising edge of first FSYNC (8-kHz external clock input) after execution of mode specification, and data is output from DO pin at next rising edge of FSYNC.
1	1	Acoustic device, A/D, D/A test mode	Outputs audio data converted into digital signal from DO pin. Also inputs audio data input from DI pin to D/A converter. Inputting/outputting data is started at rising edge of first FSYNC (8-kHz external clock input) after execution of mode specification. At this time, clock output to DSP (SCLK) is stopped.

Note In the normal mode, do not set DRSTB to low level (during low period, serial interface with DSP is disabled). As well, set the output pins of driver IC to high-impedance state, because DRSTB input pin is connected with a pull-up resistor.

Remark Analog loop back mode and DAI test mode cannot be specified at the same time.

DAI test mode is set with TC1, TC2 (or ITC1, ITC2) and DRSTB pins. DAI test mode is entered at the rising edge of the DRSTB signal when both TC1 and TC2 pins (or ITC1 and ITC2 pins) are set as shown in **Figure 2-14**.

Figure 2-14 Latch Timing of TC1, TC2 (or ITC1, ITC2)

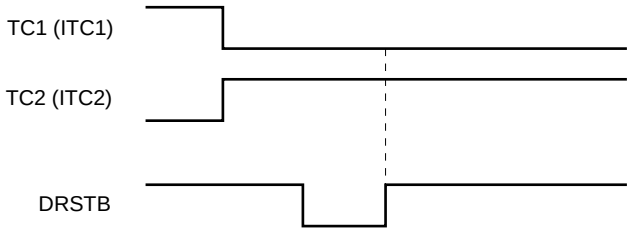
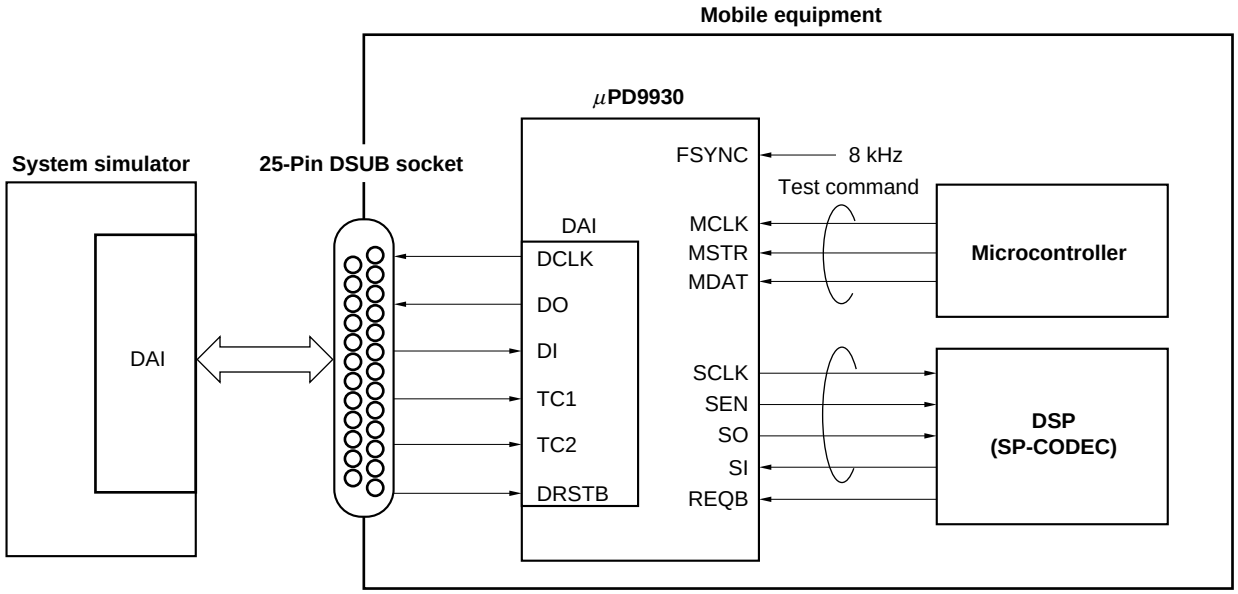


Figure 2-15 Example of System Configuration at Time of DAI Test Mode



Remark In the acoustic device test mode, REQB is ignored (both high and low levels). When DSPSEL = V_{DD} (mode 1), SCLK and SEN are fixed to low, and when DSPSEL = GND (mode 2), fixed to high.

Phase-out/Discontinued

Figure 2-16 Speech Encoder Test Mode (DSP Interface = MODE 1) (TC1 = 1, TC2 = 0)

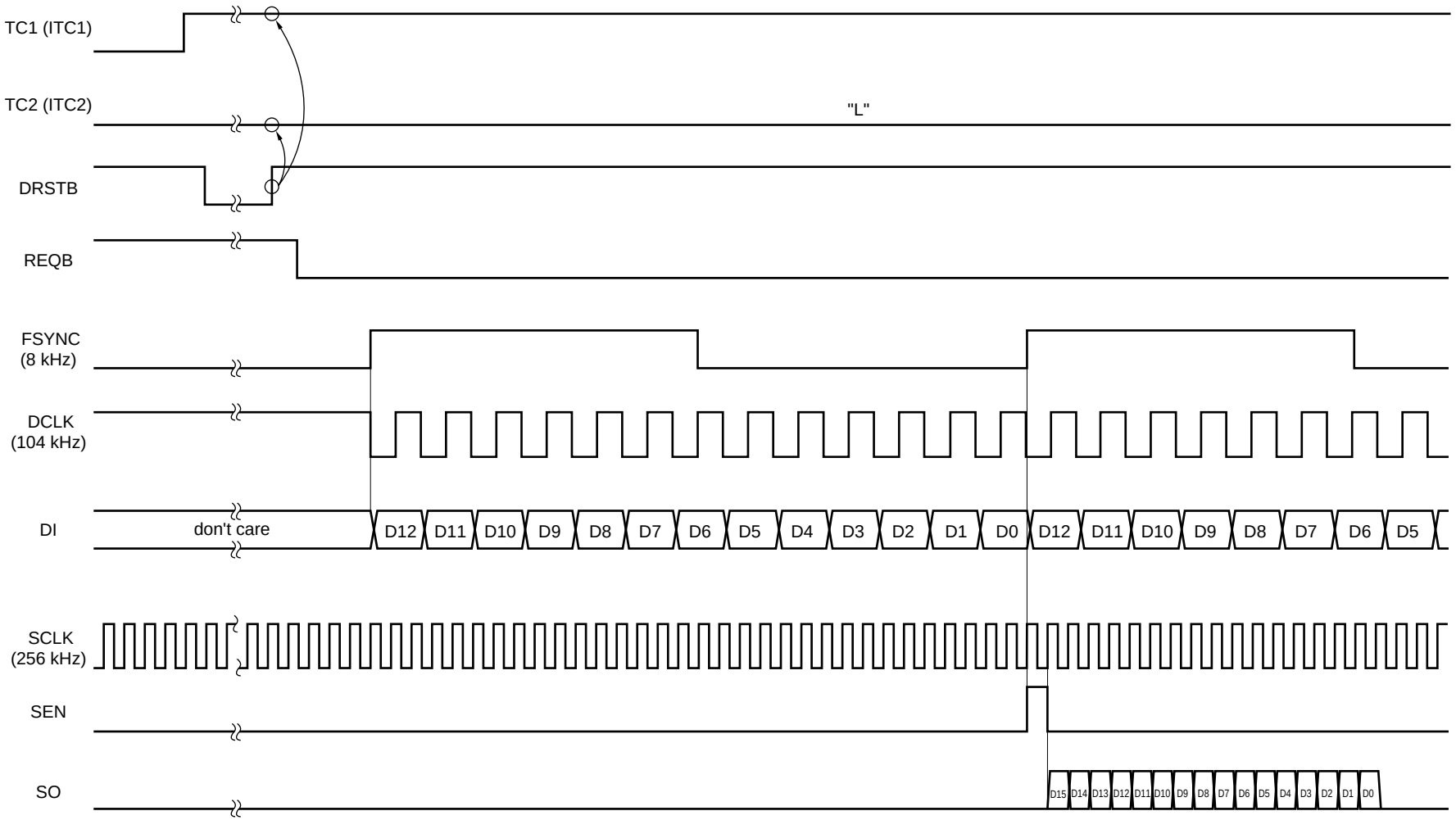


Figure 2-17 Speech Encoder Test Mode (DSP Interface = Mode 2) (TC1 = 1, TC2 = 0)

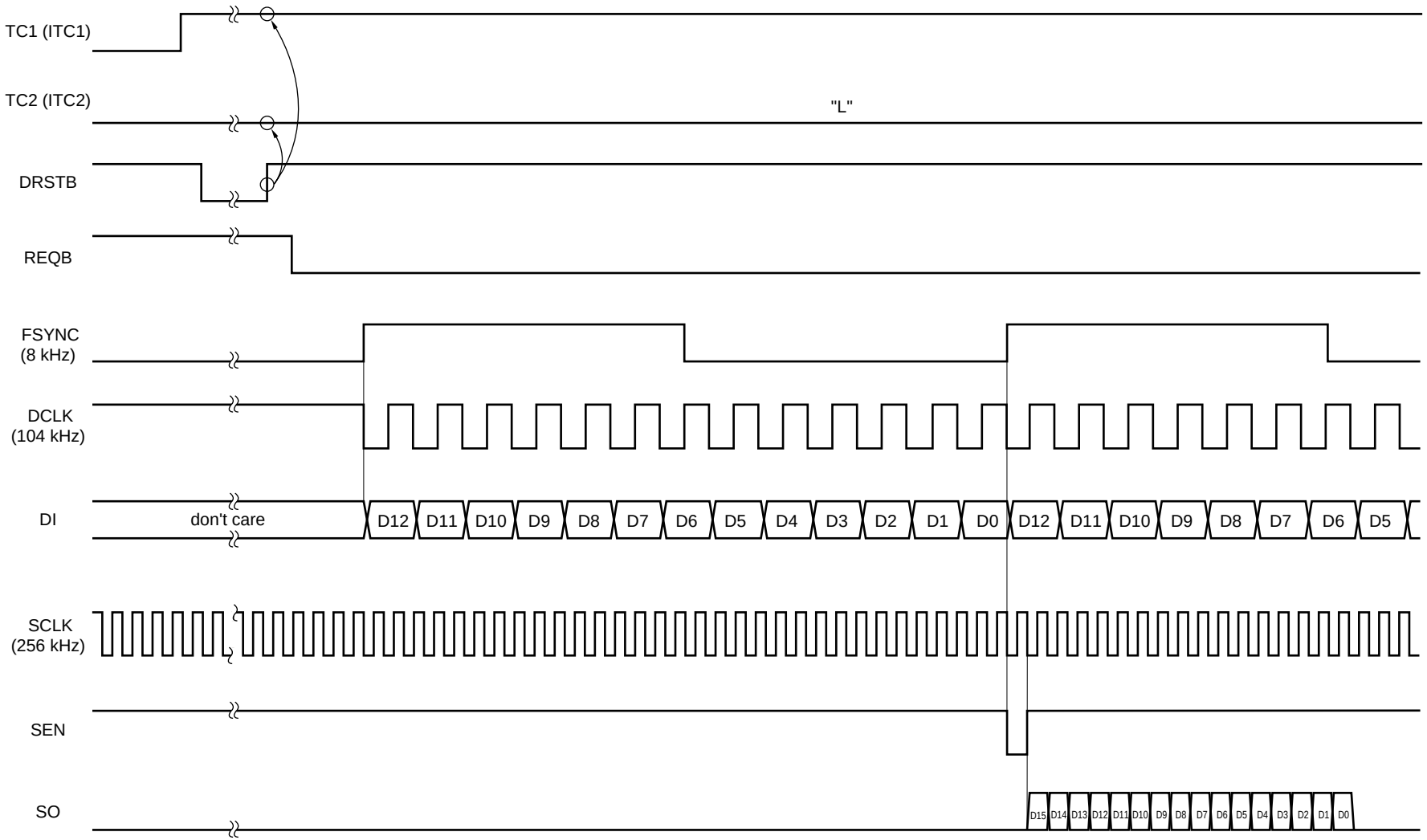


Figure 2-18 Speech Decoder Test Mode (DSP Interface = Mode 1) (TC1 = 0, TC2 = 1)

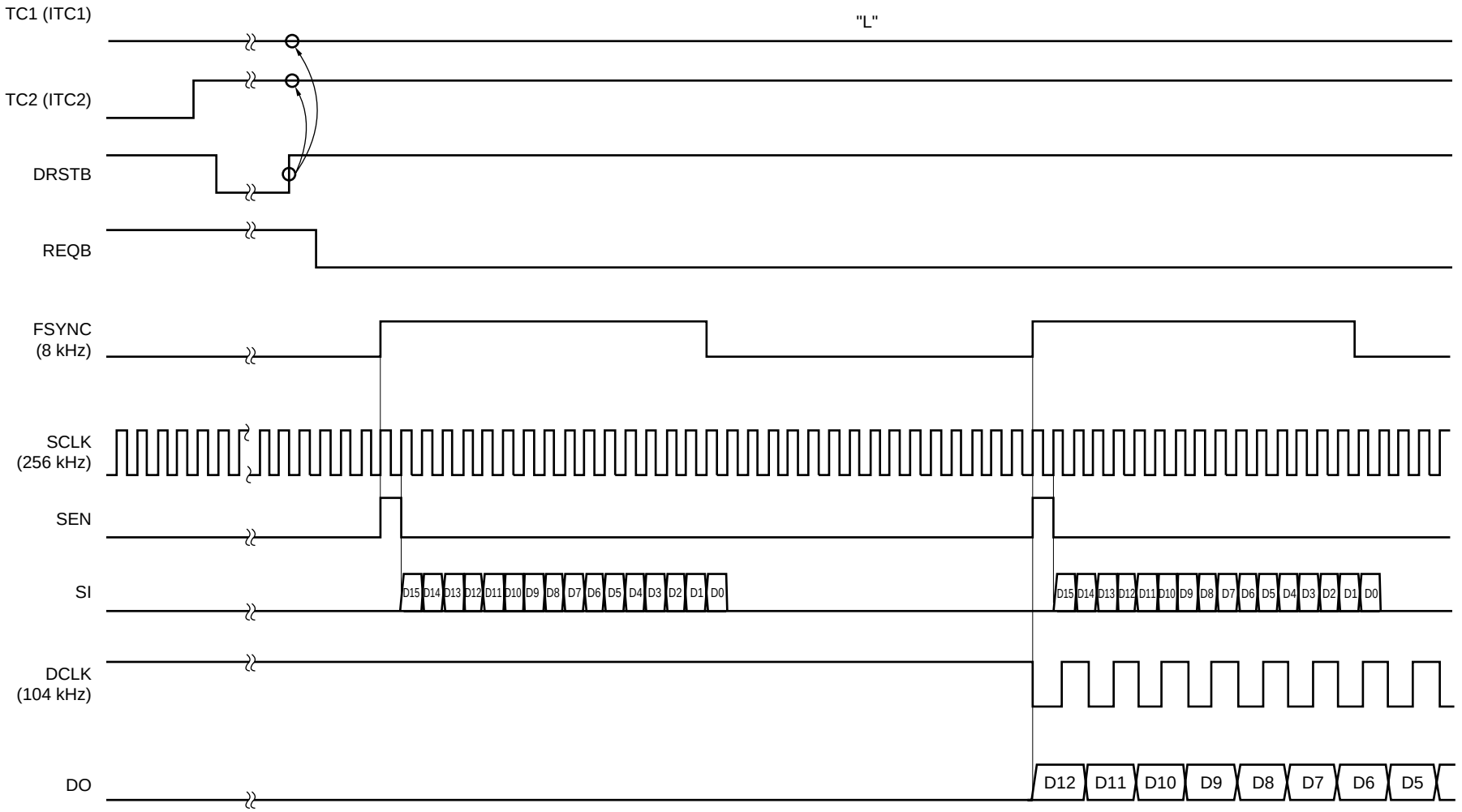


Figure 2-19 Speech Decoder Test Mode (DSP Interface = Mode 2) (TC1 = 0, TC2 = 1)

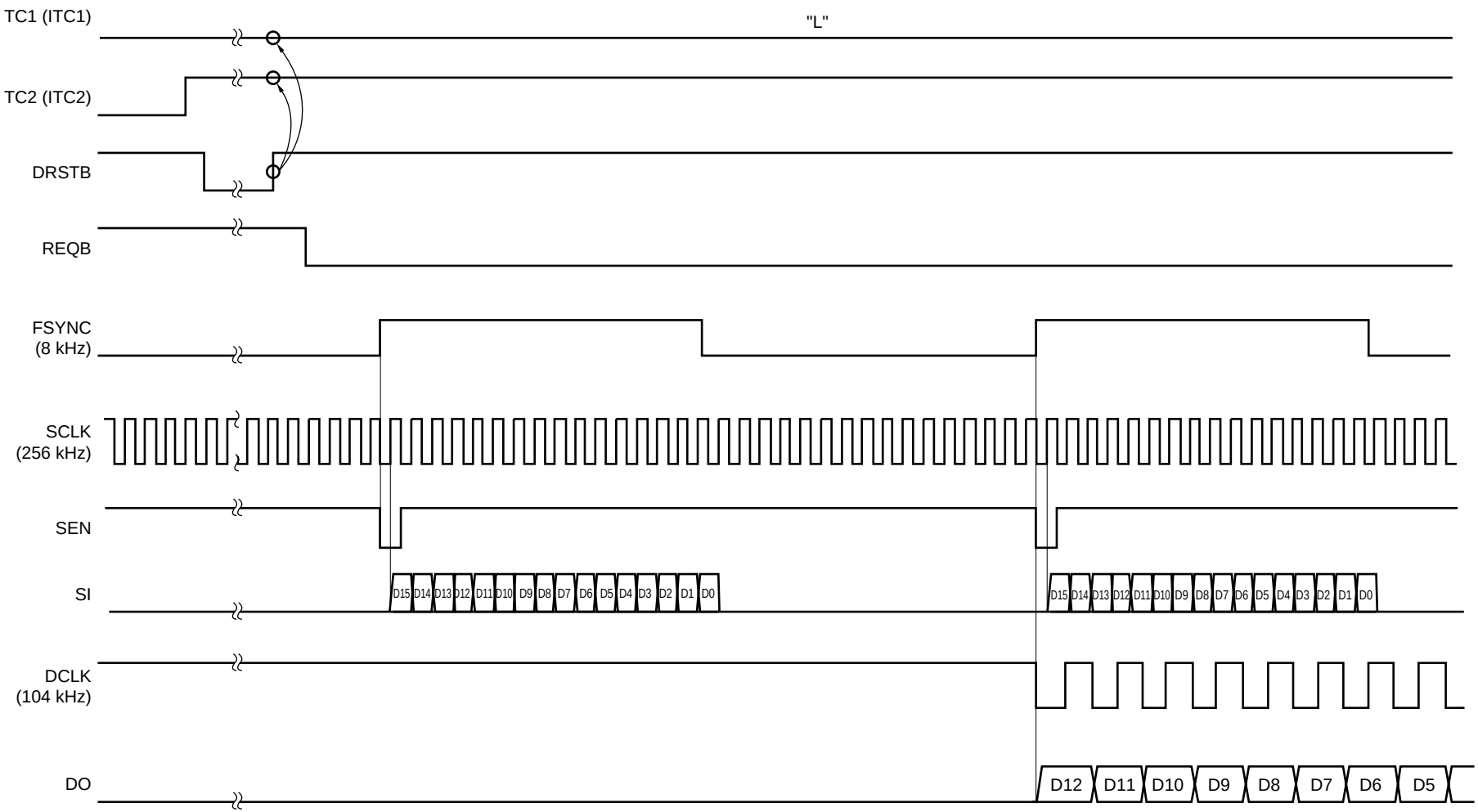
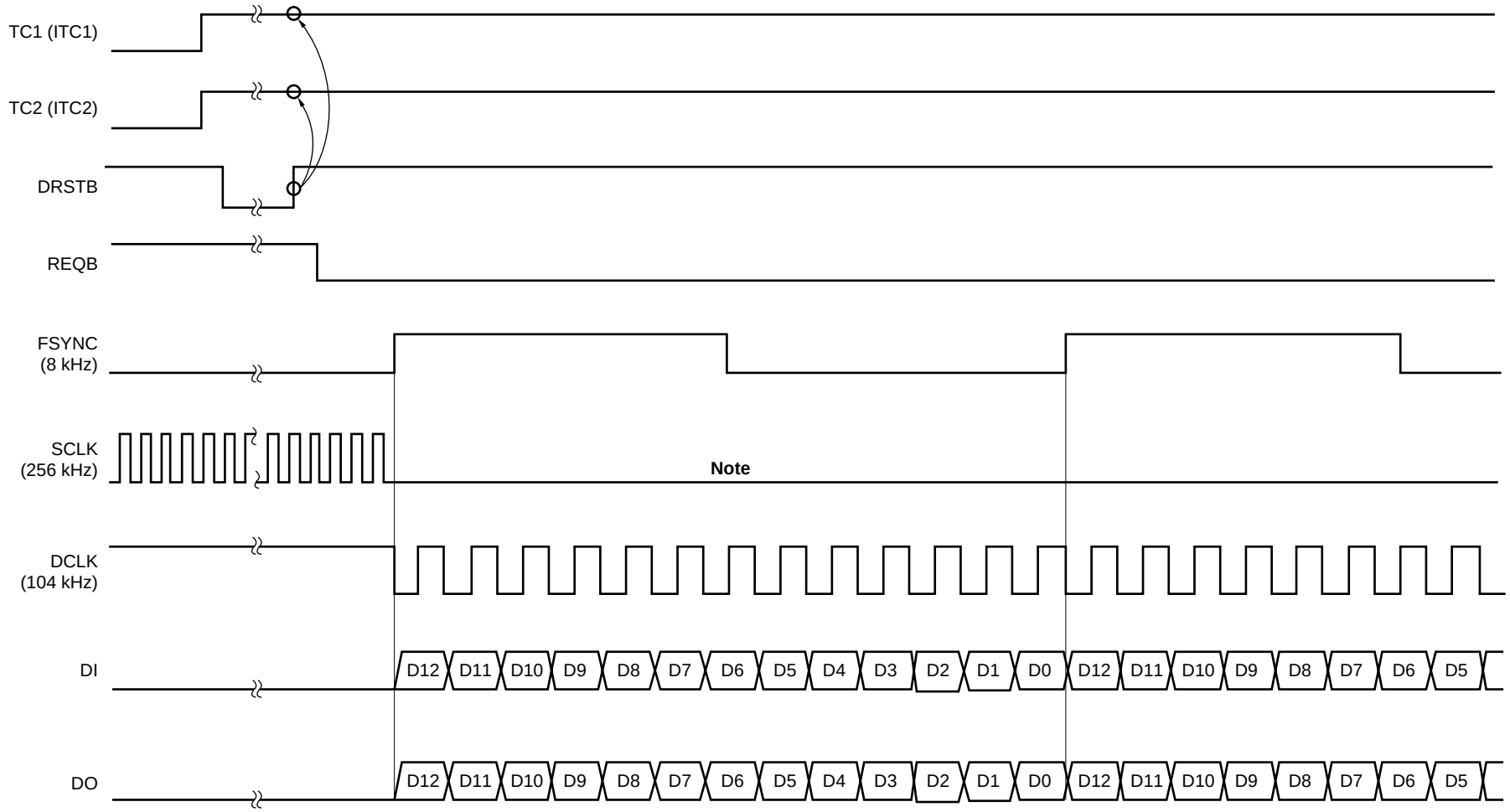


Figure 2-20 Acoustic Device Test Mode (DSP Interface = Mode 1) (TC1 = 1, TC2 = 1)

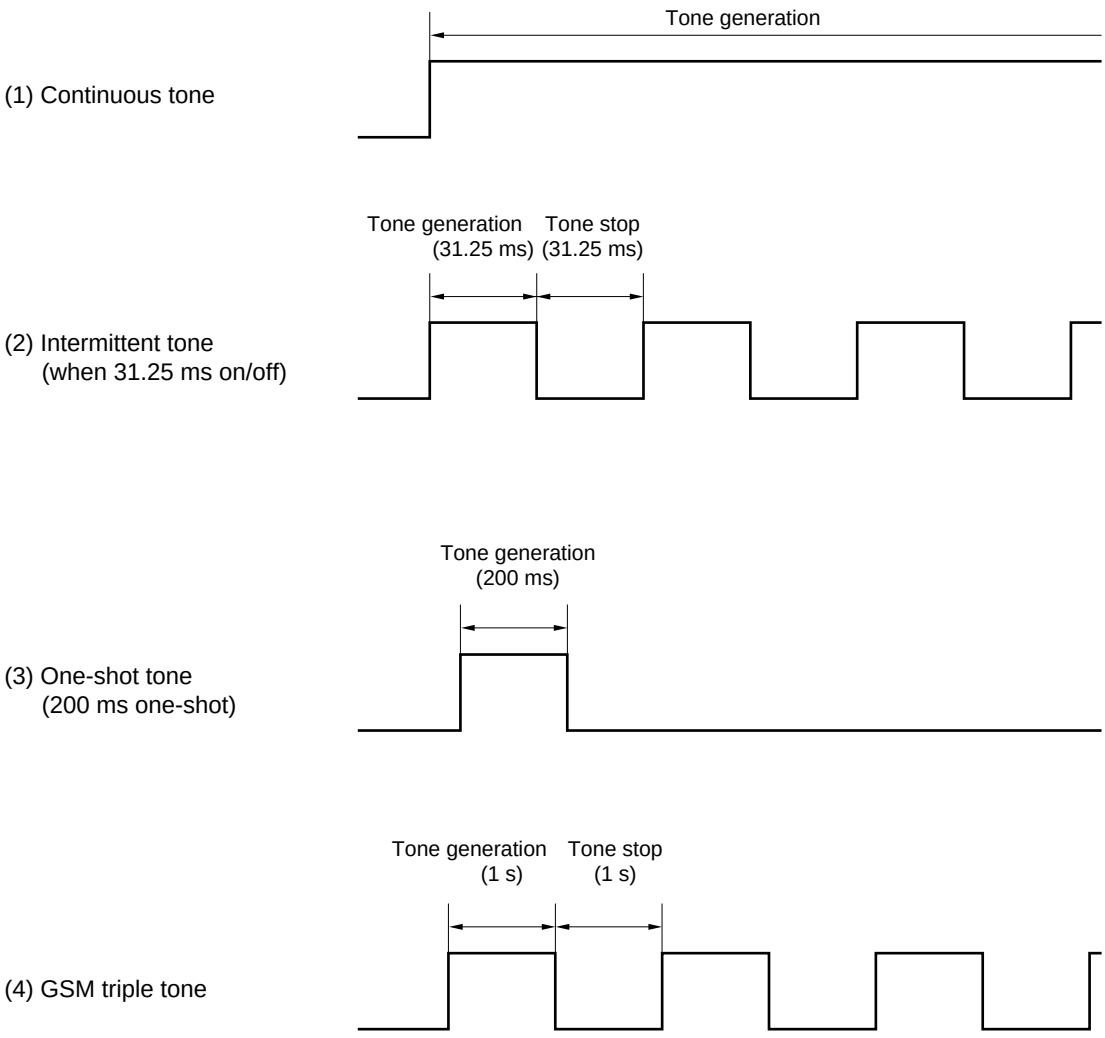


Note In DSP Interface = Mode 2, SCLK is fixed to high.

3. TONE INTERVAL OUTPUT FUNCTION (TIMER TERMINAL)

When a tone is generated, an interval signal that indicates the tone intermittent state is output. The function is used, for example, to make the LED blink in synchronization with the ringer tone.

Figure 3-1 Tone Interval Output Waveform



★ 4. INTERNAL CONTROL FUNCTIONS

The μPD9930 can control internal functions by commands from a microcontroller. Commands consist of 8-bit data (D7 to D0) consisting of register address and setting data, and are written in the following internal registers.

Register name	Control
(1) Voice send analog gain/receiver amplifier 2 control register (TXGCR) (2) Voice receive analog gain control register (RXGCR) (3) Voice send/receive digital gain control register (DGGSR)	Voice send/receive gain control
(4) Digital signal processing control register (DSPCR)	Digital input/output control
(5) Tone frequency selection register (FRQSR) (6) Expanded tone register (EXPR1/EXPR2) (7) Tone control register (TONCR) (8) Tone gain control register (TNGCR)	Tone control
(9) Input/output amplifier control register (AMPCR) (10) Power up control command (PUPCMD) (11) Power down control command (PDWCMD)	Power up/down control
(12) Test control register (TSTCR)	Test mode control

Remarks 1. In the case of registers (1), (2), and (9) to (11), written contents are executed instantly.

2. For registers (3) to (8) and (12), since fetch execution is made by the internal clock (125 μs interval), keep 125 μs or more interval for write-in to the same register.
If the write-in to the same register is executed continuously, the previous command may be ignored.

3. Even when in the stand-by mode, write-in to each internal register is possible (can be held), but the command written in the register is executed only after clearing the stand-by mode.

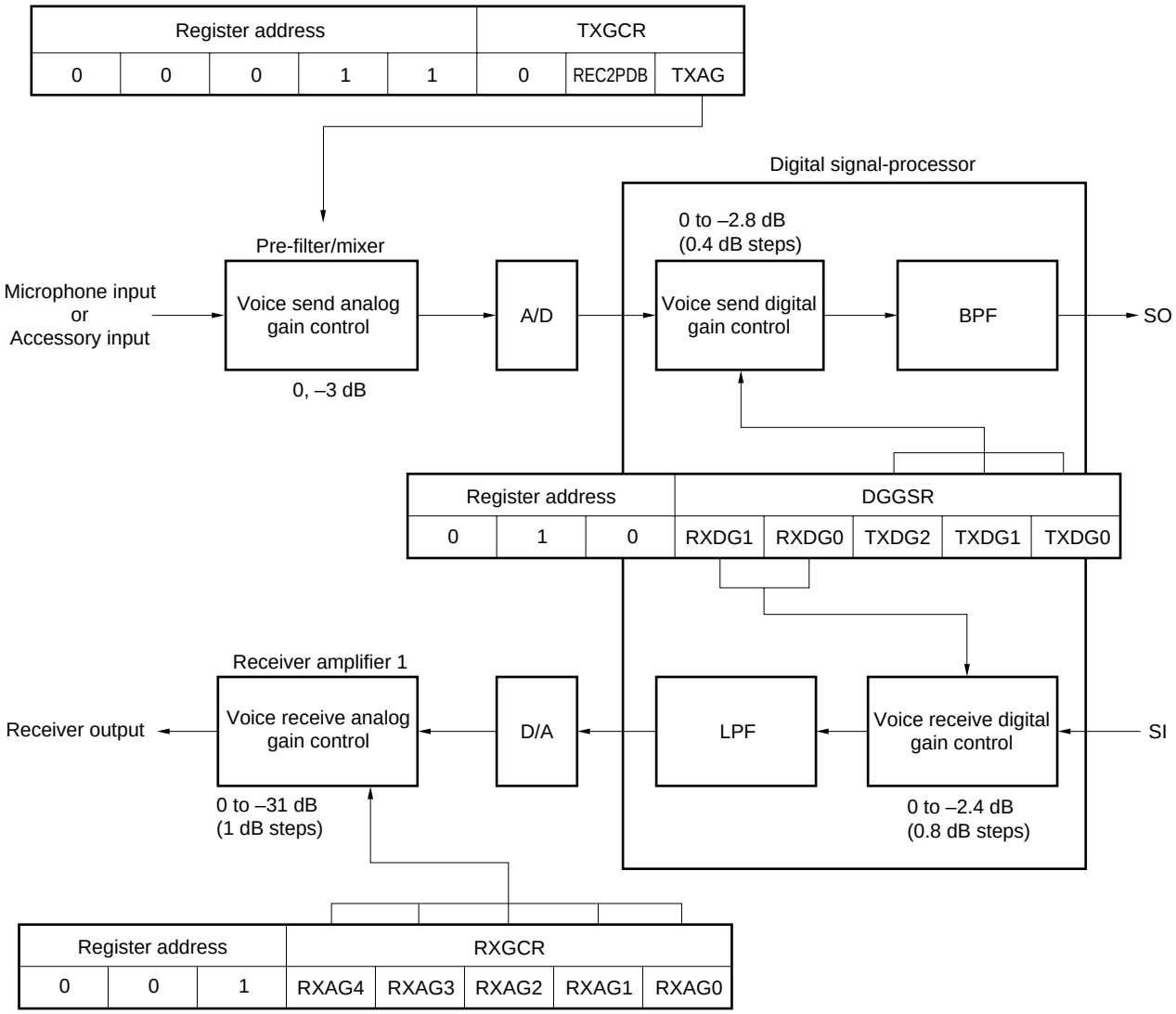
4.1 SEND/RECEIVE GAIN CONTROL

An outline of send/receive gain control is shown in **Figure 4-1**.

With the μPD9930, the following send and receive gain control is possible.

Send/receive gain control		Register used
Voice send gain control	Pre-filter analog gain adjustment (0, –3 dB)	Voice send analog gain/receiver amplifier 2 control register (TXGCR)
	Digital gain fine adjustment (0 to –2.8 dB, 0.4 dB steps)	Voice send/receive digital gain control register (DGGSR)
Voice receive gain control	Receiver amplifier 1 analog gain adjustment (volume control) (0 to –31 dB, 1 dB steps)	Voice receive analog gain control register (RXGCR)
	Digital gain fine adjustment (0 to –2.4 dB, 0.8 dB steps)	Voice send/receive digital gain control register (DGGSR)

Figure 4-1 Send/Receive Gain Control



4.1.1 Voice Send Analog Gain/Receiver Amplifier 2 Control Register (TXGCR)

This register controls pre-filter gain. It also controls receiver amplifier 2 power up/down as shown in Table 4-1 (Refer to **2.1.6 Power Up/Down Control**).

When power is down, the contents of the register area retained. After power is up, control continues as before power was down.

Figure 4-2 Voice Send Analog Gain/Receiver Amplifier 2 Control Register

Register address					TXGCR		
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	REC2PDB	TXAG

REC2PDB	Receiver amplifier 2 power up/down specification
0	Power down
1	Power up

TXAG	Pre-filter analog gain specification
0	Sets to 0 dB
1	Sets to –3 dB

Table 4-1 Function Specification by Send Analog Gain/Receiver Amplifier 2 Control Register

Register address					TXGCR			Receiver amplifier 2	Voice send analog gain	HEX[Note]		Remarks
D7	D6	D5	D4	D3	D2	D1	D0			M	L	
0	0	0	1	1	0	0	0	Power down	0 dB	18H	18H	At reset
					0	0	1	Power down	–3 dB	19H	98H	
					0	1	0	Power up	0 dB	1AH	58H	
					0	1	1	Power up	–3 dB	1BH	D8H	

Note M: HEX value with MSB first
L: HEX value with LSB first

4.1.2 Voice Receive Analog Gain Control Register (RXGCR)

This is a 5-bit register for controlling the analog gain (volume) of receiver amplifier 1.

Figure 4-3 Voice Receive Analog Gain Control Register

Register address			RXGCR				
D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	RXAG4	RXAG3	RXAG2	RXAG1	RXAG0

RXAG4 to RXAG0	Receiver amplifier 1 gain specification
00000 to 11111	0 to –31 dB (1 dB steps)

Table 4-2 Function Specifications by Voice Receive Analog Gain Control Register

Register address			RXGCR					Voice receive analog gain	HEX[Note]		Remarks
D7	D6	D5	D4	D3	D2	D1	D0		M	L	
0	0	1	0	0	0	0	0	0 dB	20H	04H	
			0	0	0	0	1	–1 dB	21H	84H	
			0	0	0	1	0	–2 dB	22H	44H	
			0	0	0	1	1	–3 dB	23H	C4H	
			0	0	1	0	0	–4 dB	24H	24H	
			0	0	1	0	1	–5 dB	25H	A4H	
			0	0	1	1	0	–6 dB	26H	64H	
			0	0	1	1	1	–7 dB	27H	E4H	
			0	1	0	0	0	–8 dB	28H	14H	
			0	1	0	0	1	–9 dB	29H	94H	
			0	1	0	1	0	–10 dB	2AH	54H	
			0	1	0	1	1	–11 dB	2BH	D4H	
			0	1	1	0	0	–12 dB	2CH	34H	
			0	1	1	0	1	–13 dB	2DH	B4H	
			0	1	1	1	0	–14 dB	2EH	74H	
			0	1	1	1	1	–15 dB	2FH	F4H	
			1	0	0	0	0	–16 dB	30H	0CH	
			1	0	0	0	1	–17 dB	31H	8CH	
			1	0	0	1	0	–18 dB	32H	4CH	
			1	0	0	1	1	–19 dB	33H	CCH	
			1	0	1	0	0	–20 dB	34H	2CH	
			1	0	1	0	1	–21 dB	35H	ACH	
			1	0	1	1	0	–22 dB	36H	6CH	
			1	0	1	1	1	–23 dB	37H	ECH	
			1	1	0	0	0	–24 dB	38H	1CH	
			1	1	0	0	1	–25 dB	39H	9CH	
			1	1	0	1	0	–26 dB	3AH	5CH	
			1	1	0	1	1	–27 dB	3BH	DCH	
			1	1	1	0	0	–28 dB	3CH	3CH	
			1	1	1	0	1	–29 dB	3DH	BCH	
			1	1	1	1	0	–30 dB	3EH	7CH	
			1	1	1	1	1	–31 dB	3FH	FCH	At reset

Note M: HEX value with MSB first
L: HEX value with LSB first

4.1.3 Voice Send/Receive Digital Gain Control Register (DGGSR)

This is a 5-bit register for adjusting the gain of the digital signal processor. The gain of the send system and receive system can be fine-adjusted independently.

Figure 4-4 Send/Receive Digital Gain Control Register

Register address			DGGSR				
D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	RXDG1	RXDG0	TXDG2	TXDG1	TXDG0

RXDG1 to RXDG0	Receive digital gain specification
00 to 11	0 to –2.4 dB (0.8 dB steps)

TXDG2 to TXDG0	Send digital gain specification
000 to 111	0 to –2.8 dB (0.4 dB steps)

Table 4-3 Function Specifications by Voice Send/Receive Digital Gain Control Register

Register address			DGGSR					Voice receive digital gain	Voice send digital gain	HEX[Note]		Remarks
D7	D6	D5	D4	D3	D2	D1	D0			M	L	
0	1	0	0	0	0	0	0	0 dB	0 dB	40H	02H	At reset
			0	0	0	0	1	0 dB	–0.4 dB	41H	82H	
			0	0	0	1	0	0 dB	–0.8 dB	42H	42H	
			0	0	0	1	1	0 dB	–1.2 dB	43H	C2H	
			0	0	1	0	0	0 dB	–1.6 dB	44H	22H	
			0	0	1	0	1	0 dB	–2.0 dB	45H	A2H	
			0	0	1	1	0	0 dB	–2.4 dB	46H	62H	
			0	0	1	1	1	0 dB	–2.8 dB	47H	E2H	
			0	1	0	0	0	–0.8 dB	0 dB	48H	12H	
			0	1	0	0	1	–0.8 dB	–0.4 dB	49H	92H	
			0	1	0	1	0	–0.8 dB	–0.8 dB	4AH	52H	
			0	1	0	1	1	–0.8 dB	–1.2 dB	4BH	D2H	
			0	1	1	0	0	–0.8 dB	–1.6 dB	4CH	32H	
			0	1	1	0	1	–0.8 dB	–2.0 dB	4DH	B2H	
			0	1	1	1	0	–0.8 dB	–2.4 dB	4EH	72H	
			0	1	1	1	1	–0.8 dB	–2.8 dB	4FH	F2H	
			1	0	0	0	0	–1.6 dB	0 dB	50H	0AH	
			1	0	0	0	1	–1.6 dB	–0.4 dB	51H	8AH	
			1	0	0	1	0	–1.6 dB	–0.8 dB	52H	4AH	
			1	0	0	1	1	–1.6 dB	–1.2 dB	53H	CAH	
			1	0	1	0	0	–1.6 dB	–1.6 dB	54H	2AH	
			1	0	1	0	1	–1.6 dB	–2.0 dB	55H	AAH	
			1	0	1	1	0	–1.6 dB	–2.4 dB	56H	6AH	
			1	0	1	1	1	–1.6 dB	–2.8 dB	57H	EAH	
			1	1	0	0	0	–2.4 dB	0 dB	58H	1AH	
			1	1	0	0	1	–2.4 dB	–0.4 dB	59H	9AH	
			1	1	0	1	0	–2.4 dB	–0.8 dB	5AH	5AH	
			1	1	0	1	1	–2.4 dB	–1.2 dB	5BH	DAH	
			1	1	1	0	0	–2.4 dB	–1.6 dB	5CH	3AH	
			1	1	1	0	1	–2.4 dB	–2.0 dB	5DH	BAH	
			1	1	1	1	0	–2.4 dB	–2.4 dB	5EH	7AH	
			1	1	1	1	1	–2.4 dB	–2.8 dB	5FH	FAH	

Note M: HEX value with MSB first
L: HEX value with LSB first

4.2 DIGITAL INPUT/OUTPUT CONTROL

An outline of digital input/output control is shown in **Figure 4-5**.

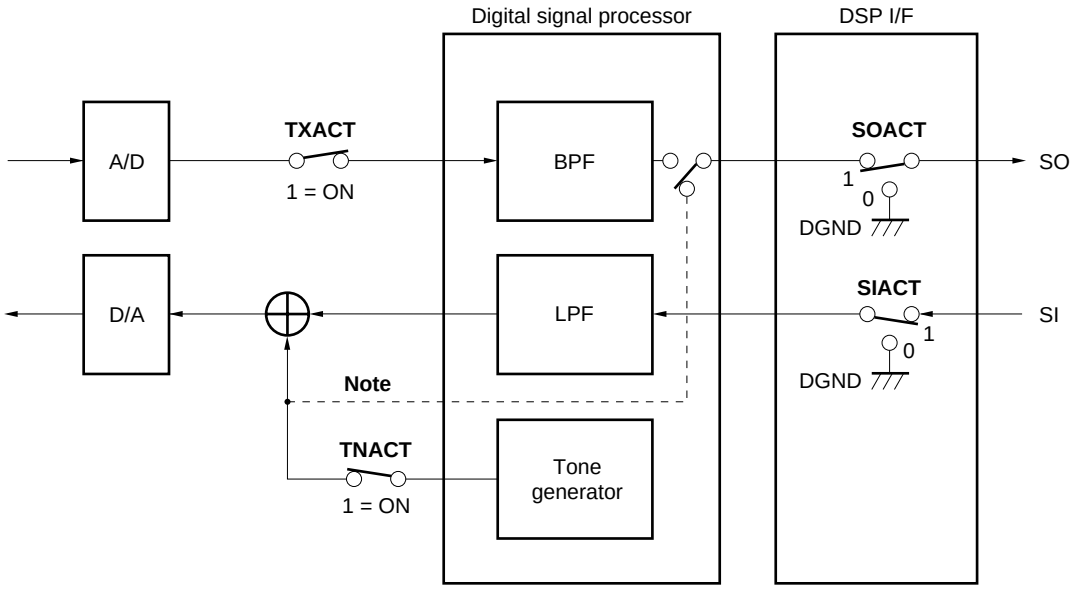
The μPD9930 can control input and output of the digital signal processor as follows.

Digital input/output control	Registers used
Voice send data BPF operation processing execution/stop	Digital signal processing control register (DSPCR)
Connection and disconnection to tone output Voice send/ receive system	
Serial output terminal (SO) control	
Serial input terminal (SI) control	

Caution You must not connect nor disconnect tone output voice send/receive system in the tone operation. It causes malfunction.

Figure 4-5 Digital Input/Output Control

Register address				DSPCR			
0	1	1	0	TXACT	TNACT	SOACT	SIACT



Note Connected when TXACT = 0 and TNACT = 1.

4.2.1 Digital Signal Processing Control Register (DSPCR)

This is a 4-bit register for controlling digital signal processor input/output.

Figure 4-6 Digital Signal Processing Control Register

Register address				DSPCR			
D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	TXACT	TNACT	SOACT	SIACT

TXACT	Voice send data processing control
0	Stops voice send data digital BPF processing.
1	Executes voice send data digital BPF processing.

TNACT	Tone output control
0	Disconnects tone output from voice send/receive systems.
1	Connects tone output to voice send/receive systems.

SOACT	DSP interface output control
0	Sets serial output (SO) at low level[Note].
1	Outputs send data (or tone data) to the serial output (SO).

SIACT	DSP interface input control
0	Sets serial input (SI) at low level[Note].
1	Inputs receive data to serial input (SI).

Note Test Control Register can set serial input/output terminal at low level, too (refer to **4.4.1 Test Control Register (TSTCR)**).

Caution Before specification of SOACT bit, be sure to write "0" for SIOOFF bit of Test Control Register. If "0" isn't written for SIOOFF bit, serial output terminal is set at low level, regardless of SOACT bit.

Table 4-4 Function Specification by Digital Signal Processing Control Register

Register address				DSPCR				Serial output control	Control of output to D/A	HEX[Note]		Remarks
D7	D6	D5	D4	D3	D2	D1	D0			M	L	
0	1	1	0	0	0	0	0	**Note 2**	**Note 3**	60H	06H	At reset
				0	0	0	1	**Note 2**	Voice receive signal output	61H	86H	
				0	0	1	0	Inhibiting command		—	—	
				0	0	1	1	Inhibiting command		—	—	
				0	1	0	0	**Note 2**	Tone output	64H	26H	
				0	1	0	1	**Note 2**	Voice receive signal + tone output	65H	A6H	
				0	1	1	0	Tone output	Tone output	66H	66H	
				0	1	1	1	Tone output	Voice receive signal + tone output	67H	E6H	
				1	0	0	0	Inhibiting command		—	—	
				1	0	0	1	Inhibiting command		—	—	
				1	0	1	0	Voice send signal output	**Note 3**	6AH	56H	
				1	0	1	1	Voice send signal output	Voice receive signal output	6BH	D6H	
				1	1	0	0	Inhibiting command		—	—	
				1	1	0	1	Inhibiting command		—	—	
				1	1	1	0	Voice send signal output	Tone output	6EH	76H	
				1	1	1	1	Voice send signal output	Voice receive signal + tone output	6FH	F6H	

Notes 1. M: HEX value with MSB first
L: HEX value with LSB first

2. Stops voice send data processing and serial output.

3. Stops voice receive data serial input and tone output.

4.3 TONE CONTROL

An outline diagram of the tone generator is shown in **Figure 4-7**. Tone generation is by the tone 1 oscillation circuit and the tone 2 oscillation circuit.

The tone 1 oscillation circuit generates high group frequency for DTMF and four types of single tones (tone 1 frequency).

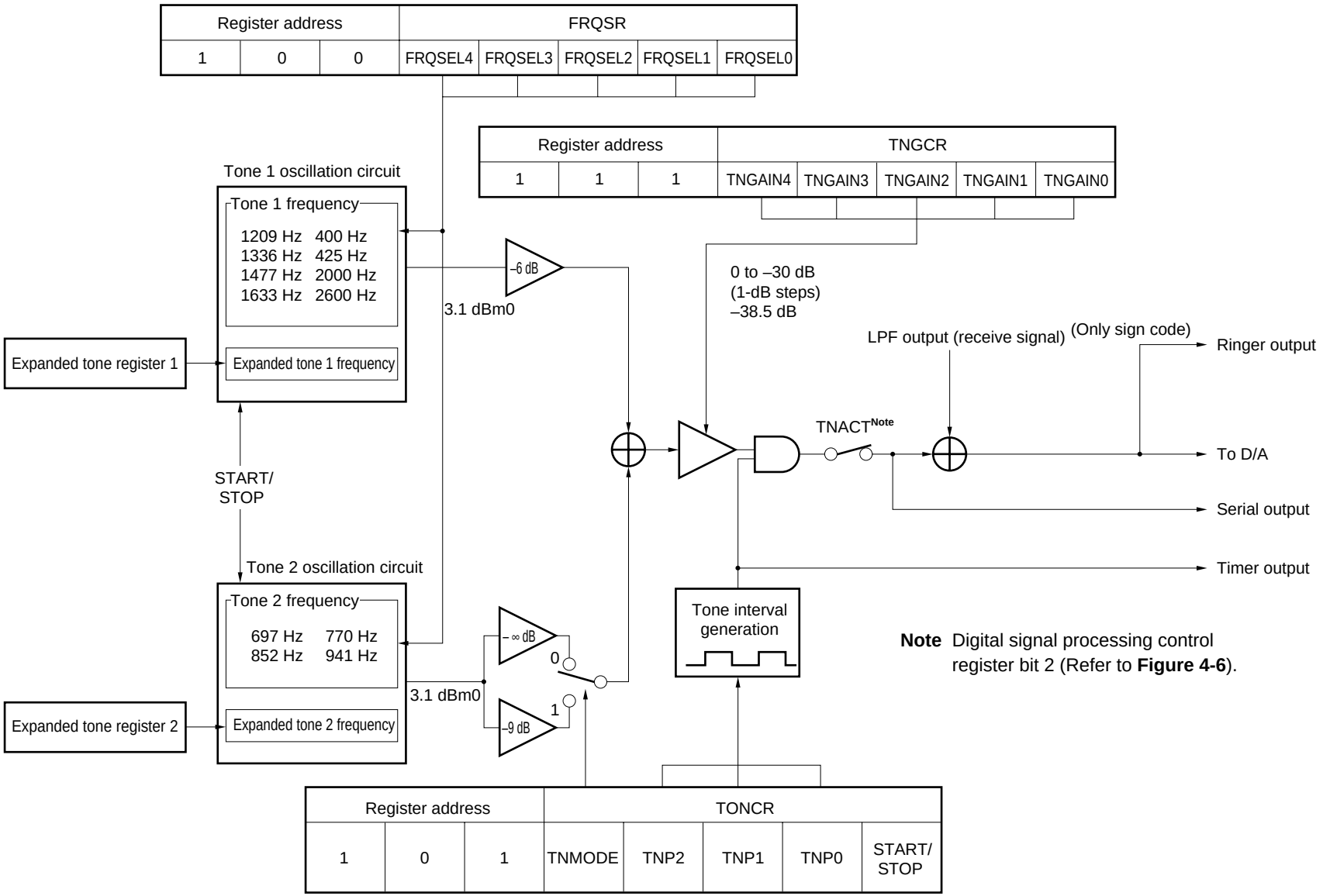
The tone 2 oscillation circuit generates low group frequency (tone 2 frequency) for DTMF. Dual tone is output by adding tone 1 frequency.

In addition to registered tones, other frequencies can be registered. Also, GSM triple tone can be generated by special command. Examples of tone generation are shown in **Figure 4-8**.

Tone control items are shown below.

Tone control			Registers used
Tone frequency	Registered tone	Specification of DTMF	Tone frequency selection register (FRQSR)
		Single tone: 400 Hz, 425 Hz, 2 kHz, 2.6 kHz	
		Selection of GSM triple tone	Tone control register (TONCR)
	User registration tone	Registration of desired tone in 0.3 to 3.4 kHz range. (Single tone, dual tone)	Tone frequency selection register (FRQSR) Expanded tone register 1 (EXPR1) Expanded tone register 2 (EXPR2)
Generation pattern	Registered pattern	31.25 ms intermittence, 200 ms intermittence, 250 ms intermittence, 500 ms intermittence, 1s intermittence, 200 ms one-shot tone	Tone control register (TONCR)
	Desired pattern	Interrupted at desired interval by START/STOP command	
Gain	Control of tone output gain 0 to –30 dB (1 dB steps), –38.5 dB		Tone gain control register (TNGCR)

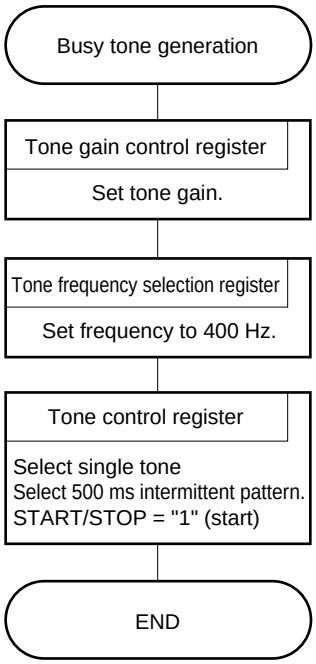
Figure 4-7 Tone Control



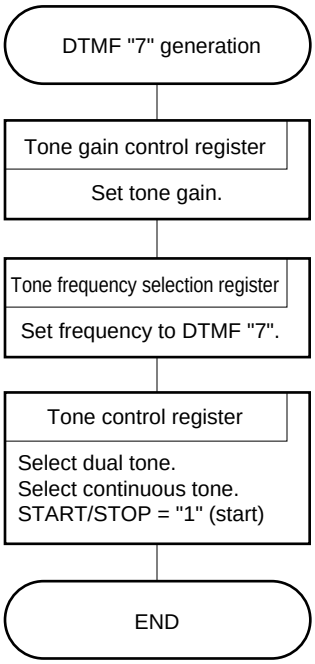
Note Digital signal processing control register bit 2 (Refer to **Figure 4-6**).

Figure 4-8 Tone Generation Examples

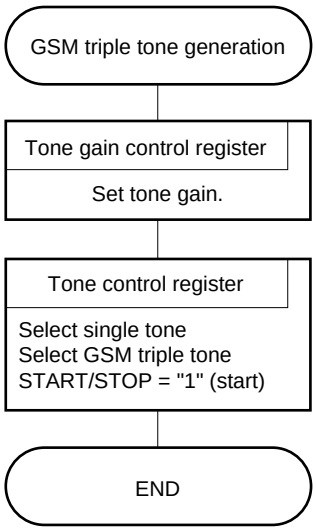
(a) When generating a busy tone (400 Hz single tone, 500 ms intermittence)



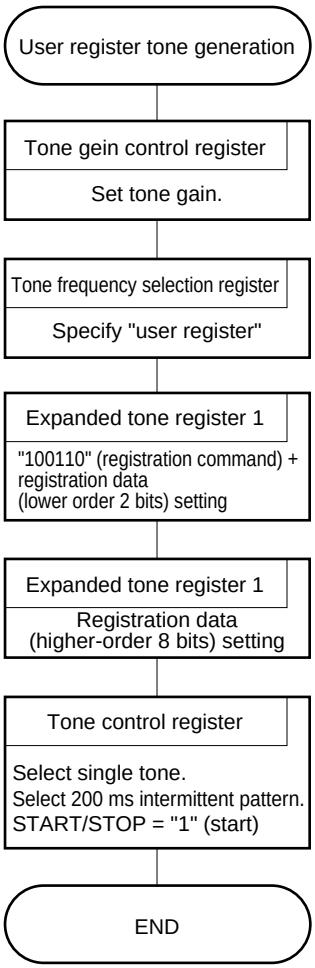
(b) When generating DTMF "7" with continuous tone



(c) When generating GSM triple tone



(d) When generating 200 ms intermittent user register tone (480 Hz single tone; coefficient = 0111011100B)



4.3.1 Tone Frequency Selection Register (FRQSR)

This is a 5-bit register for specifying tone 1 (high group frequency for DTMF and four types of single tones) and tone 2 (low group frequency for DTMF) frequency combinations.

Figure 4-9 Tone Frequency Selection Register

Register address			FRQSR				
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

FRQSEL4 to FRQSEL0	Tone frequency selection
00000 to 10100	Refer to **Table 4-5 Function Specification by Tone Frequency Selection Register**.

Write operation in this register is instantaneously executed and retained when a command is received, but change of tone generation or generating tone is executed only when "1" is written for START/STOP control bit of the tone control register (refer to **Figure 4-11 Tone Control Register**).

When a user registration tone is selected, the tone specified by the expanded tone register (refer to **Figure 4-10 Expanded Tone Frequency Registration Procedure**) is generated.

Caution Do not input a command that sets a tone oscillation frequency after inputting a tone oscillation command (writing "1" to the START/STOP control bit of the tone control register).

Table 4-5 Function Specification by Tone Frequency Selection Register

Register address			FRQSR					DTMF function	Tone 1 frequency	Tone 2 frequency	HEX[Note 1]		Remarks
D7	D6	D5	D4	D3	D2	D1	D0				M	L	
1	0	0	0	0	0	0	0	DTMF “1”	1209 Hz	697 Hz	80H	01H	
			0	0	0	0	1	DTMF “2”	1336 Hz	697 Hz	81H	81H	
			0	0	0	1	0	DTMF “3”	1477 Hz	697 Hz	82H	41H	
			0	0	0	1	1	DTMF “A”	1633 Hz	697 Hz	83H	C1H	
			0	0	1	0	0	DTMF “4”	1209 Hz	770 Hz	84H	21H	
			0	0	1	0	1	DTMF “5”	1336 Hz	770 Hz	85H	A1H	
			0	0	1	1	0	DTMF “6”	1477 Hz	770 Hz	86H	61H	
			0	0	1	1	1	DTMF “B”	1633 Hz	770 Hz	87H	E1H	
			0	1	0	0	0	DTMF “7”	1209 Hz	852 Hz	88H	11H	
			0	1	0	0	1	DTMF “8”	1336 Hz	852 Hz	89H	91H	
			0	1	0	1	0	DTMF “9”	1477 Hz	852 Hz	8AH	51H	
			0	1	0	1	1	DTMF “C”	1633 Hz	852 Hz	8BH	D1H	
			0	1	1	0	0	DTMF “*”	1209 Hz	941 Hz	8CH	31H	
			0	1	1	0	1	DTMF “0”	1336 Hz	941 Hz	8DH	B1H	
			0	1	1	1	0	DTMF “#”	1477 Hz	941 Hz	8EH	71H	
			0	1	1	1	1	DTMF “D”	1633 Hz	941 Hz	8FH	F1H	
			1	0	0	0	0		400 Hz[Note 2]	Indefinite value	90H	09H	
			1	0	0	0	1		425 Hz[Note 2]	Indefinite value	91H	89H	
			1	0	0	1	0		2 kHz[Note 2]	Indefinite value	92H	49H	
			1	0	0	1	1		2.6 kHz[Note 2]	Indefinite value	93H	C9H	At reset
			1	0	1	0	0		User registration	User registration	94H	29H	
			1	0	1	0	1	Inhibiting command			—	—	
			1	0	1	1	0	Inhibiting command			—	—	
			1	0	1	1	1	Inhibiting command			—	—	

Notes 1. M: HEX value with MSB first
L: HEX value with LSB first

2. This is single tone. When specifying this tone, be sure to specify the tone control register in the single tone mode (refer to **Figure 4-11 Tone Control Register**).

Remark For DTMF tone generation, specify the tone control register in the dual tone mode (refer to **Figure 4-11 Tone Control Register**). If the register is specified in the single tone mode, only the high group tone (tone 1 frequency) is generated.

4.3.2 Expanded Tone Registers (EXPR1, EXPR2)

(1) Expanded Tone Frequency Registration Procedure

The μPD9930 can register desired tone frequencies (expanded tone frequencies) in 0.3 to 3.4 kHz range. Expanded tone register 1 (EXPR1) is for registering expanded tone 1 frequency (high group frequency for DTMF and single tone). Expanded tone register 2 (EXPR2) is for registering expanded tone 2 frequency (low frequency for DTMF). The frequency must be specified by 10-bit coefficient (2's complement).

Registration of single tone is done with EXPR1 (single-tone generation is impossible by EXPR2) (refer to **Figure 4-10 (a)**).

When registering dual tone, set high group in EXPR1 and low group in EXPR2.

Write operation in this register can be executed by continuously writing the expanded tone registration command and expanded tone data command (refer to **Figure 4-10**).

Once registered, the frequency is valid until reset or updated.

Figure 4-10 Expanded Tone Frequency Registration Procedure

(a) Expanded tone 1 frequency registration procedure

<1> Set expanded tone 1 registration command in EXPR1.

Expanded tone 1 registration command

	D7	D6	D5	D4	D3	D2	D1	D0
EXPR1	1	0	0	1	1	0	EA1	EA0

<2> Set higher-order 8 bits of expanded tone coefficient (expanded tone 1 data command) in EXPR1.

Expanded tone 1 data command

	D7	D6	D5	D4	D3	D2	D1	D0
EXPR1	EA9	EA8	EA7	EA6	EA5	EA4	EA3	EA2

Remark EA9 to EA0: Tone 1 frequency 10-bit coefficient

(b) Expanded tone 2 frequency registration procedure

<1> Set expanded tone 2 registration command in EXPR2.

Expanded tone 2 registration command

	D7	D6	D5	D4	D3	D2	D1	D0
EXPR2	1	0	0	1	1	1	EB1	EB0

<2> Set higher-order 8 bits of expanded tone coefficient (expanded tone 2 data command) in EXPR2.

Expanded tone 2 data command

	D7	D6	D5	D4	D3	D2	D1	D0
EXPR2	EB9	EB8	EB7	EB6	EB5	EB4	EB3	EB2

Remark EB9 to EB0: Tone 2 frequency 10-bit coefficient

Caution After executing the expanded tone registration command, the next command is written as expanded tone data, so continuously execute the expanded tone data command.

(2) Expanded Tone Data Determination Method

The coefficient E of the tone frequency fe (0.3 to 3.4 kHz) to be generated is determined by the following formula.

$E = \cos(2\pi\, fe/fs)$ fs = 8 kHz

Coefficient E: Sign bit 1 bit + 9 bits below the decimal point (Coefficient: 2's complement)

Example When specifying 400 Hz single tone

$\cos(2\pi \times 400/8000) = \cos(\pi \times 0.1)$
$= \cos(0.3141592653.....)$
$= 0.951056516.....$
$= (0.11110011X)\ b$ (Higher-order 9 bits are determined.)

Next, the least significant bit is determined.

When $(0.111100110)\ b = 0.94921875$
$2\pi\, fe' \times fs = \cos^{-1}(0.94921875) = 0.320052983$
$fe' = 0.320052983 \times fs/(2\pi)$
$fe' = 407.504115$
When $(0.111100111)\ b = 0.951071875$
$2\pi\, fe'' \times fs = \cos^{-1}(0.951071875) = 0.314109559$
$fe'' = 0.314109559 \times fs/(2\pi)$
$fe'' = 399.524415$

Since fe" is nearest to 400 Hz, the coefficient to be registered is (0.111100111) b = (1E7) H.

0	1	1	1	1	0	0	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EA9	EA8	EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0

The error of oscillation frequency by rounding 10-bit coefficient is below ±5 Hz (MAX. at 300 Hz → ±1.7 %) for all frequencies.

About ±1.67 % near 300 Hz (±5 Hz)
About ±1.00 % near 500 Hz (±5 Hz)
About ±0.40 % near 1 kHz (±5 Hz)
About ±0.25 % near 2 kHz (±5 Hz)
About ±0.16 % near 3 kHz (±5 Hz)

Coefficient is negative number in fe > 2.0 kHz.

4.3.3 Tone Control Register (TONCR)

This is a 5-bit register for controlling single tone/dual tone specification, generation pattern selection, and generation and stopping.

Figure 4-11 Tone Control Register

Register address			TONCR				
D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	TNMODE	TNP2	TNP1	TNP0	START /STOP

TNMODE	Single tone/dual tone specification	Remarks
0	Single tone mode	At reset
1	Dual tone mode	

TNP2	TNP1	TNP0	Generation pattern selection	Remarks
0	0	0	Continuous tone generation	At reset
0	0	1	31.25 ms tone, 31.25 ms no tone repeated	
0	1	0	200 ms tone, 200 ms no tone repeated	
0	1	1	250 ms tone, 250 ms no tone repeated	
1	0	0	500 ms tone, 500 ms no tone repeated	
1	0	1	1 s tone, 1s no tone repeated	
1	1	0	GSM triple tone generated[Note 1]	
1	1	1	200 ms interval tone generated (one shot tone)	

START/STOP	Tone generation/stop control	Remarks
0	Stop ("1" → "0", "0" → "0" both valid) [Note 2]	At reset
1	Validation of tone ferquency selection register setting data, start of generation ("1"→ "1", "0" → "1" both valid)	

Notes 1. 950 Hz tone 333 ms, 1400 Hz tone 333 ms, 1800 Hz tone 333 ms, 1 s no tone repeated.

2. Do not input a command that sets a tone oscillation frequency after inputting a tone oscillation command (writing "1" to the START/STOP control bit of the tone control register).

Remark When the regeneration pattern is specified as "110", it becomes GSM triple tone command, so tone generation forcibly enters single tone mode.

Tone generation and change of a tone that is being generated is executed only when "1" is written for START/STOP control bit (D0 bit) (refer to **Figure 4-11** and **Table 4-6**).

Table 4-6 Function Specification by Tone Control Register

Register address			TONCR					Tone control conditions	HEX[Note]	
D7	D6	D5	D4	D3	D2	D1	D0		M	L
1	0	1	X	X	X	X	0	Tone stop	A0H	05H
			0	0	0	0	1	Continuous single tone generation	A1H	85H
			0	0	0	1	1	31.25 ms intermittent single tone generation	A3H	C5H
			0	0	1	0	1	200 ms intermittent single tone generation	A5H	A5H
			0	0	1	1	1	250 ms intermittent single tone generation	A7H	E5H
			0	1	0	0	1	500 ms intermittent single tone generation	A9H	95H
			0	1	0	1	1	1 s intermittent single tone generation	ABH	D5H
			0	1	1	0	1	GSM triple tone generation	ADH	B5H
			0	1	1	1	1	200 ms one-shot single tone generation	AFH	F5H
			1	0	0	0	1	Continuous dual tone generation	B1H	8DH
			1	0	0	1	1	31.25 ms intermittent dual tone generation	B3H	CDH
			1	0	1	0	1	200 ms intermittent dual tone generation	B5H	ADH
			1	0	1	1	1	250 ms intermittent dual tone generation	B7H	EDH
			1	1	0	0	1	500 ms intermittent dual tone generation	B9H	9DH
			1	1	0	1	1	1 s intermittent dual tone generation	BDH	BDH
			1	1	1	1	1	200 ms one-shot dual tone generation	BFH	FDH

Note M: HEX value with MSB first L: HEX value with LSB first

Remark X: Don't care

4.3.4 Tone Gain Control Register (TNGCR)

This is a 5-bit register for controlling the tone output gain.

Figure 4-12 Tone Gain Control Register

Register address			TNGCR				
D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	TNGAIN4	TNGAIN3	TNGAIN2	TNGAIN1	TNGAIN0

TNGAIN4 to TNGAIN0	Tone gain selection (Refer to **Table 4-7 Function Specification by Tone Gain Control Register**).
00000 to 11111	0 to –30 dB (1 dB steps), –38.5 dB

Table 4-7 Function Specification by Tone Gain Control Register

Register address			TNGCR					Tone gain	HEX[Note]		Remarks
D7	D6	D5	D4	D3	D2	D1	D0		M	L	
1	1	1	0	0	0	0	0	0 dB	E0H	07H	
			0	0	0	0	1	–1 dB	E1H	87H	
			0	0	0	1	0	–2 dB	E2H	47H	
			0	0	0	1	1	–3 dB	E3H	C7H	
			0	0	1	0	0	–4 dB	E4H	27H	
			0	0	1	0	1	–5 dB	E5H	A7H	
			0	0	1	1	0	–6 dB	E6H	67H	
			0	0	1	1	1	–7 dB	E7H	E7H	
			0	1	0	0	0	–8 dB	E8H	17H	
			0	1	0	0	1	–9 dB	E9H	97H	
			0	1	0	1	0	–10 dB	EAH	57H	
			0	1	0	1	1	–11 dB	EBH	D7H	
			0	1	1	0	0	–12 dB	ECH	37H	
			0	1	1	0	1	–13 dB	EDH	B7H	
			0	1	1	1	0	–14 dB	EEH	77H	
			0	1	1	1	1	–15 dB	EFH	F7H	
			1	0	0	0	0	–16 dB	F0H	0FH	
			1	0	0	0	1	–17 dB	F1H	8FH	
			1	0	0	1	0	–18 dB	F2H	4FH	
			1	0	0	1	1	–19 dB	F3H	CFH	
			1	0	1	0	0	–20 dB	F4H	2FH	At reset
			1	0	1	0	1	–21 dB	F5H	AFH	
			1	0	1	1	0	–22 dB	F6H	6FH	
			1	0	1	1	1	–23 dB	F7H	EFH	
			1	1	0	0	0	–24 dB	F8H	1FH	
			1	1	0	0	1	–25 dB	F9H	9FH	
			1	1	0	1	0	–26 dB	FAH	5FH	
			1	1	0	1	1	–27 dB	FBH	DFH	
			1	1	1	0	0	–28 dB	FCH	3FH	
			1	1	1	0	1	–29 dB	FDH	BFH	
			1	1	1	1	0	–30 dB	FEH	7FH	
			1	1	1	1	1	–38.5 dB	FFH	FFH	

Note M: HEX value with MSB first
L: HEX value with LSB first

4.4 TEST MODE CONTROL

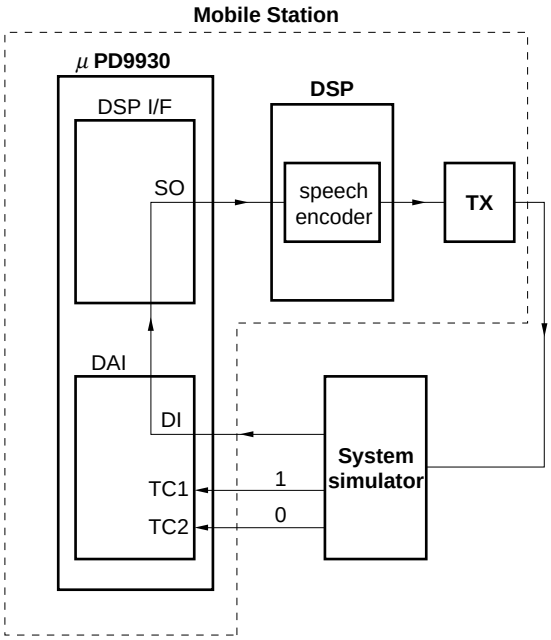
The μPD9930 has the following test functions.

Test function		Registers used
DAI test function	This test function is stipulated in GSM11.10. Test mode selection can be controlled by external terminal (TC1 or TC2) or internal register (ITC1, ITC2).	Test control register (TSTCR)
Analog loopback function	Send data after BPF processing is input to LPF.	
DSP interface input/ output control function	SO, SI, SCLK and SEN terminals can be set at low level.	

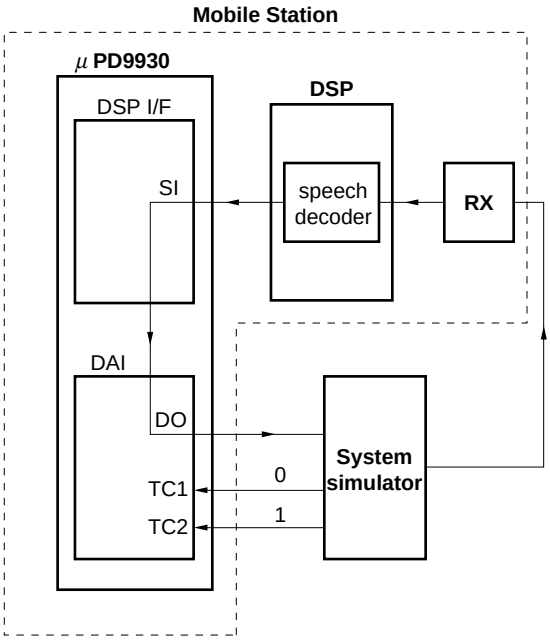
An outline of test mode control is shown in **Figure 4-13**.

Figure 4-13 Test Mode Operation

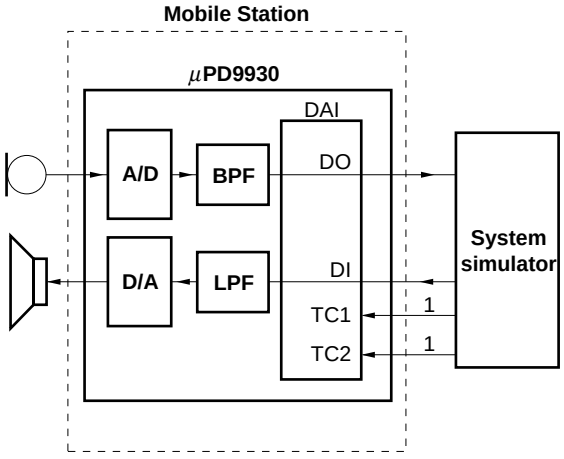
(a) DAI (speech encoder test mode)



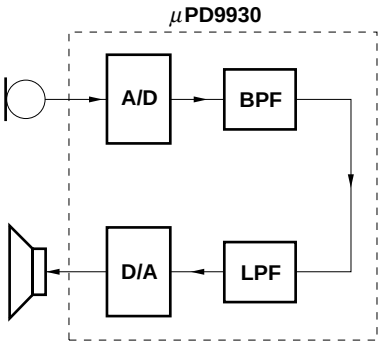
(b) DAI (speech decoder test mode)



(c) DAI (A/D, D/A test mode)



(d) Analog loopback mode



4.4.1 Test Control Register (TSTCR)

This is a 5-bit control register for selecting the test mode.

ITC1, ITC2 become valid at the rising edge of DRSTB. For the precautions when using DAI, refer to **2.1.9 DAI (Digital Audio Interface)**.

Figure 4-14 Test Control Register

Register address			TSTCR				
D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	TCMODE	ITC2	ITC1	LOOPBK	SIOOFF

TCMODE	DAI test mode control method selection	Remarks
0	Specification of test mode by external terminals TC1 and TC2	At reset
1	Specification of test mode by test control registers ITC1 and ITC2	

ITC2	ITC1	DAI test mode specification	Remarks
0	0	Normal operation	At reset
0	1	Speech encoder test mode	
1	0	Speech decoder test mode	
1	1	Acoustic device, A/D, D/A test mode	

LOOPBK	Analog loopback specification	Remarks
0	Normal operation	At reset
1	Analog loopback	

SIOOFF	DSP interface input/output terminal control	Remarks
0	Normal operation	
1	Setting of terminals SO, SI, SCLK, and SEN to low level	At reset

Remark The analog loopback mode and the DAI test mode cannot be specified at the same time.

5. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, DGND = AGND1 to AGND4 = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	AV_{DD1}, AV_{DD2}, DV_{DD}	–0.3 to +5.5	V
Analog Input Voltage	V_{AIN}	All analog input pins	–0.3 to V_{DD} +0.3	V
Digital Input Voltage	V_{DIN}	All digital input pins	–0.3 to V_{DD} +0.3	V
Analog Output Pin Applied Voltage	V_{AOUT}	All analog output pins	–0.3 to V_{DD} +0.3	V
Digital Output Pin Applied Voltage	V_{DOUT}	All digital output pins	–0.3 to V_{DD} +0.3	V
Operating Ambient Temperature	T_A		–30 to +85	°C
Storage Temperature	T_{stg}		–65 to +150	°C

Cautions 1. Connect the AGND1 through AGND4 pins and DGND pin to an analog ground line near μPD9930 pins. Connect the DV_{DD}, AV_{DD1}, AV_{DD2} pins to an analog power supply line near μPD9930 pins.

2. Do not connect output (and bidirectional) pins each other. Do not connect output (or bidirectional) pins directly to the V_{DD}, V_{CC}, or GND line. However, open drain pin and open collector pin can be directly connected to V_{DD}, V_{CC}, or GND line. If timing design is made so that no signal conflict occurs, three-state pins can also be connected directly to three-state pins of external circuit.

3. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

RECOMMENDED OPERATING RANGE (T_A = –30 to +85°C)

(1) DC Condition

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}	AV_{DD1}, AV_{DD2}, DV_{DD}	2.7	3.0	3.6	V
High Level Input Voltage	V_{IH}	All digital input pins	0.7 V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}	All digital input pins	0		0.3 V_{DD}	V
Analog Input Voltage	V_{IA}	All analog input pins	0.6		1.8	V
Microphone Input						
Analog Input Voltage	V_{MIC}	Differential: MICI+, MICI–			1.2	V_{p-p}
Gain Setting Range	G_{MIC}	Set with external resistor	15		33	dB
Load Resistance	RL_{MIC}	Includes gain setting resistance	50			kΩ
Load Capacitance	CL_{MIC}				20	pF
Accessory Input						
Analog Input Voltage	V_{AUXI}	XAUXI–			1.2	V_{p-p}
Gain Setting Range	G_{AUXI}	Set with external resistor	0		10	dB
Load Resistance	RL_{AUXI}	Includes gain setting resistance	300			kΩ
Load Capacitance	CL_{AUXI}				20	pF
Pre-filter + Mixer Input						
Analog Input Voltage	V_{MIXI}	MIXI			1.2	V_{p-p}
Accessory Output						
Load Resistance	RL_{AUXO}		100			kΩ
Load Capacitance	CL_{AUXO}				100	pF
Receiver 1 Output						
Load Resistance	RL_{REC1}		100			kΩ
Load Capacitance	CL_{REC1}				20	pF
Receiver 2 Output						
Analog Input Voltage	V_{REC2}	REC2I-			1.2	V_{p-p}
Gain Setting Range	G_{REC2}	Set with external resistor	– ∞		+10	dB
Load Resistance	RL_{REC2}	60 nF series	2			kΩ
Load Capacitance	CL_{REC2}	2 kΩ series			60	nF
Reference Voltage Output						
Load Capacitance	CL_{ACOM}	XACOMO, RACOMO	0.2		10	μF

(2) Frame Signal (FSYNC) and Reset Signal (RESETB)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FSYNC Frequency	fs		7.995	8.000	8.005	kHz
FSYNC High Level Width	t_{WHS}		2.0			μs
FSYNC Low Level Width	t_{WLS}		2.0			μs
FSYNC Rise Time	t_r				20	ns
FSYNC Fall Time	t_f				20	ns
RESETB Low Level Width	t_{RSL}		260			ns

(3) Microcontroller Interface

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MCLK Cycle Time	t_{MCY}		240			ns
MCLK High Level Width	t_{MCH}		100			ns
MCLK Low Level Width	t_{MCL}		100			ns
MCLK Rise Time	t_{MR}				20	ns
MCLK Fall Time	t_{MF}				20	ns
★ MDAT Setup Time to MSTR ↑	t_{SUMDA}		50			ns
MDAT Hold Time from MCLK ↑	t_{HMDA}		50			ns
MSTR High Level Width	t_{WMST}		320			ns
MCLK Setup Time to MSTR ↑	t_{SUMCK}		0			ns
MSTR Setup Time to MCLK ↑	t_{SUMST}		100			ns

(4) DSP Interface

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SI Setup Time to SCLK ↓	t_{SUSI}		200			ns
SI Hold Time from SCLK ↓	t_{HSI}		200			ns

(5) DAI

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DI Setup Time to DCLK ↑	t_{SUDI}		200			ns
DI Hold Time from DCLK ↑	t_{HDI}		200			ns
TC1, TC2 Rise Time	t_{TR}		50			ns
TC1, TC2 Fall Time	t_{TF}		50			ns
DRSTB Low Level Width	t_{DRSL}		130			μs
DRSTB Rise Time	t_{DRR}				20	ns
DRSTB Fall Time	t_{DRF}				20	ns
DAI Mode Setting Time 1	t_{TCF}		60			ms
DAI Mode Setting Time 2	t_{TCR}		260			μs
REQB Low Level Width	t_{DRQL}		130			μs
REQB High Level Width	t_{DRQH}		130			μs
REQB Rise Time	t_{DRQR}				20	ns
REQB Fall Time	t_{DRQF}				20	ns

CAPACITANCE (T_A = 25°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Digital Output Pin Capacitance	C_{OD}	f = 1 MHz			20	pF
Digital Input Pin Capacitance	C_{ID}	f = 1 MHz			20	pF

DC CHARACTERISTICS (T_A = 25°C, V_{DD} = 2.7 to 3.6 V (GND standard))

(1) Current Consumption

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current in Normal Mode	I_{DD1}	Microphone input (1020 Hz: –10 dBm0) Accessory input: Power down serial input (1020 Hz: –10 dBm0) Accessory output: Power up Receiver 1, 2: Power up		7.0	9.0	mA
Circuit Current in DAI Operation	I_{DD2}	Microphone input (1020 Hz: –10 dBm0) Accessory input: Power down serial input (1020 Hz: –10 dBm0) Accessory output: Power up Receiver 1, 2: Power up		7.5	10.0	mA
Circuit Current in Standby Mode	I_{DD3}	DI, DRSTB, TC1, TC2: Open FSYNC: 8 kHz Other digital input pins: 0 or V_{DD}		50	100	μA

(2) Digital Part

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Digital Input Leak Current	I_{LH}	$V_I = V_{DD}$			1.0	μA
	I_{LL}	V_I = 0	–1.0			μA
Pull-Up/Down Current	I_{IL}	V_{DD} = 3.3 V, 0 ≤ V_I ≤ V_{DD}			100	μA
Low Level Output Voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = –2.0 mA	2.4			V

(3) Analog Part

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Pre-filter + Mixer						
Volume Range	G_{PRF}		–3		0	dB
Volume Accuracy	ΔG_{PRF}	Volume 0 dB standard	–3.2	–3.0	–2.8	dB
Cross-Talk 1 between Input Channels	CT_{IN1}	Microphone input amplifier: Power down MICI = 1.2 V_{p-p} XAUXI– = 0 V_{p-p} Accessory input gain setting: 0 dB			–45	dB
Cross-Talk 2 between Input Channels	CT_{IN2}	Accessory input amplifier: Power down MICI = 0 V_{p-p} XAUXI– = 1.2 V_{p-p} Accessory input gain setting: 0 dB			–45	dB
Accessory Output						
Maximum Output Voltage	V_{AMAX}				1.2	V_{p-p}
Receiver 1 Output						
Maximum Output Voltage	V_{R1MAX}				1.2	V_{p-p}
Volume Range	G_{REC1}		–31		0	dB
★ Volume Accuracy	ΔG_{REC1}	Volume: 0 to –16 dB	–1.5	–1.0	–0.5	dB
		Volume[Note]: –17 to –31 dB	–2.0	–1.0	0.0	dB
Receiver 2 Output						
Maximum Output Voltage	V_{R2MAX}	Distortion factor 4 % (MAX.)			4	V_{p-p}
Reference Voltage Output						
Output Voltage	V_{ACOM}	XACOMO, RACOMO		1.2		V

Note Simple decrease in the gain due to drop of volume is guaranteed.

(4) Tone Generator

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Signal Level	V_{TN1}	Tone 1	–2.93		–2.73	dBm0
	V_{TN2}	Tone 2	–5.93		–5.73	
Frequency Deviation	ΔF_{TN}	0.3 to 3.4 kHz	–5		+5	Hz
Distortion Factor	TNSD	Accessory output	30			dB
Tone Volume Range	G_{TN}		–38.5		0	dB
Tone Volume Accuracy	ΔG_{TN}	Volume: 0 to –30 dB (1 dB steps)	–1.4	–1.0	–0.8	dB

AC CHARACTERISTICS

(1) DSP Interface (T_A = –30 to +85°C, V_{DD} = 2.7 to 3.6 V, C_L = 100 pF)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLK Cycle Time	t_{SCY}			3906		ns
SCLK High Level Width	t_{SCH}			1953		ns
SCLK Low Level Width	t_{SCL}			1953		ns
SCLK Rise Time	t_{SR}				20	ns
SCLK Fall Time	t_{SF}				20	ns
★ SCLK Delay Time from FSYNC ↑	t_{DSCLK}				1.0	μs
SEN ↑ Delay Time from FSYNC ↑	t_{DSENR}				80	ns
SEN ↓ Delay Time from SCLK ↑: Mode 1 SEN ↓ Delay Time from SCLK ↓: Mode 2	t_{DSENF}				80	ns
SO Output Delay Time from SCLK ↑: Mode 1 SO Output Delay Time from SCLK ↓: Mode 2	t_{DSO}				40	ns

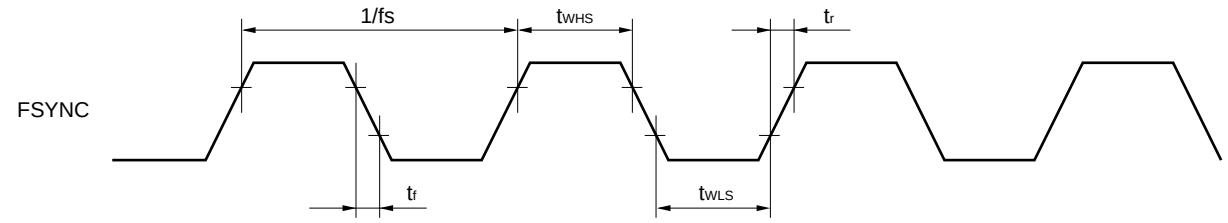
(2) DAI (T_A = –30 to +85°C, V_{DD} = 2.7 to 3.6 V, C_L = 100 pF)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DCLK Cycle Time	t_{DCY}			9615		ns
DCLK High Level Width	t_{DCH}			4808		ns
DCLK Low Level Width	t_{DCL}			4808		ns
DCLK Rise Time	t_{DR}				20	ns
DCLK Fall Time	t_{DF}				20	ns
DCLK Delay Time from FSYNC ↑	t_{DDCLK}				200	ns
DO Output Delay Time from DCLK ↓	t_{DDO}				200	ns

(3) Others (Digital Output) (T_A = –30 to +85°C, V_{DD} = 2.7 to 3.6 V, C_L = 100 pF)

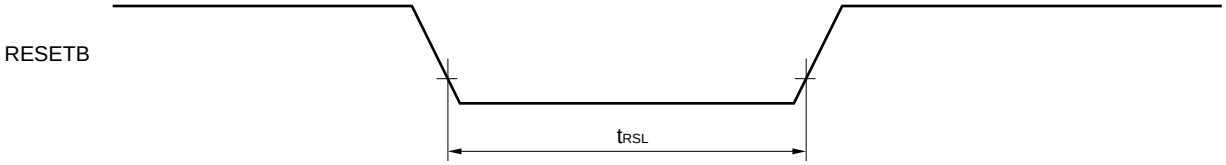
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TIMER/RINGER Rise Time	t_{DDR}	TIMER pin and RINGER pin			50	ns
TIMER/RINGER Fall Time	t_{DDF}	TIMER pin and RINGER pin			50	ns

Frame signal (FSYNC)



Remark During normal operation or the power up/down sequence, be sure to input the frame signal.

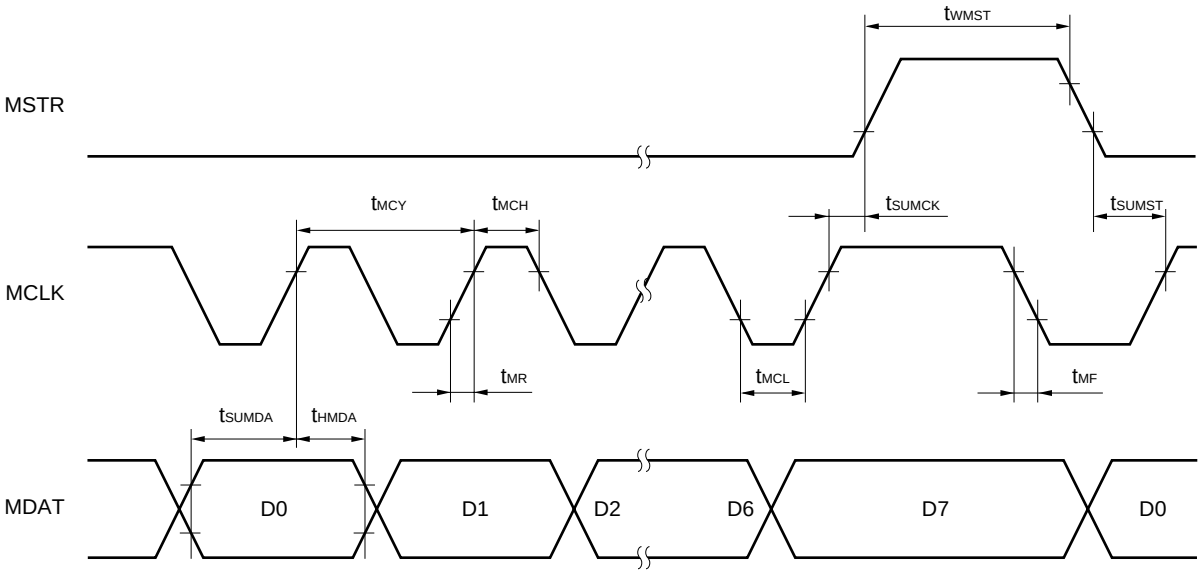
Reset signal (RESETB)



Remarks 1. The reset signal is input as it is without shaping, so take full precautions against noise.

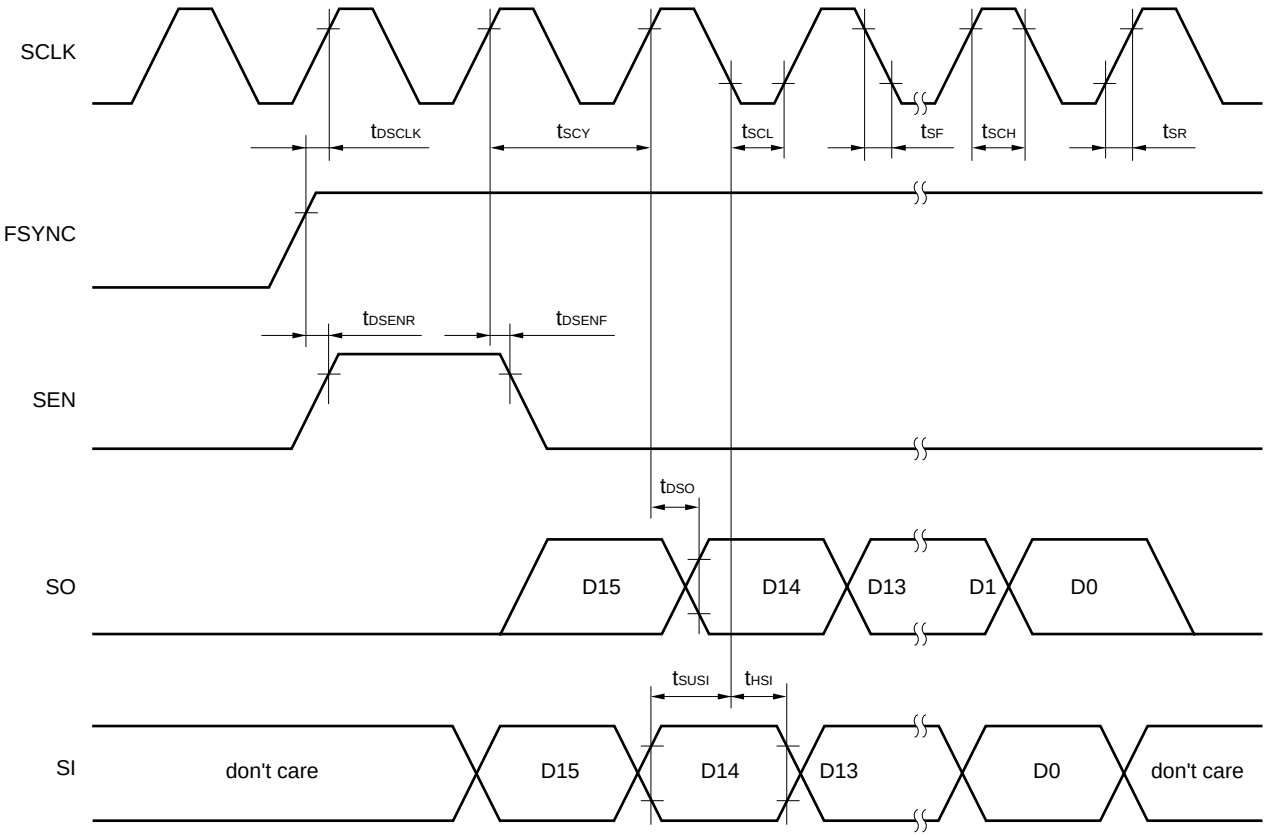
2. A power on reset circuit is not incorporated, so be sure to set RESET to low after turning the power on.

★ **Microcontroller interface timing**

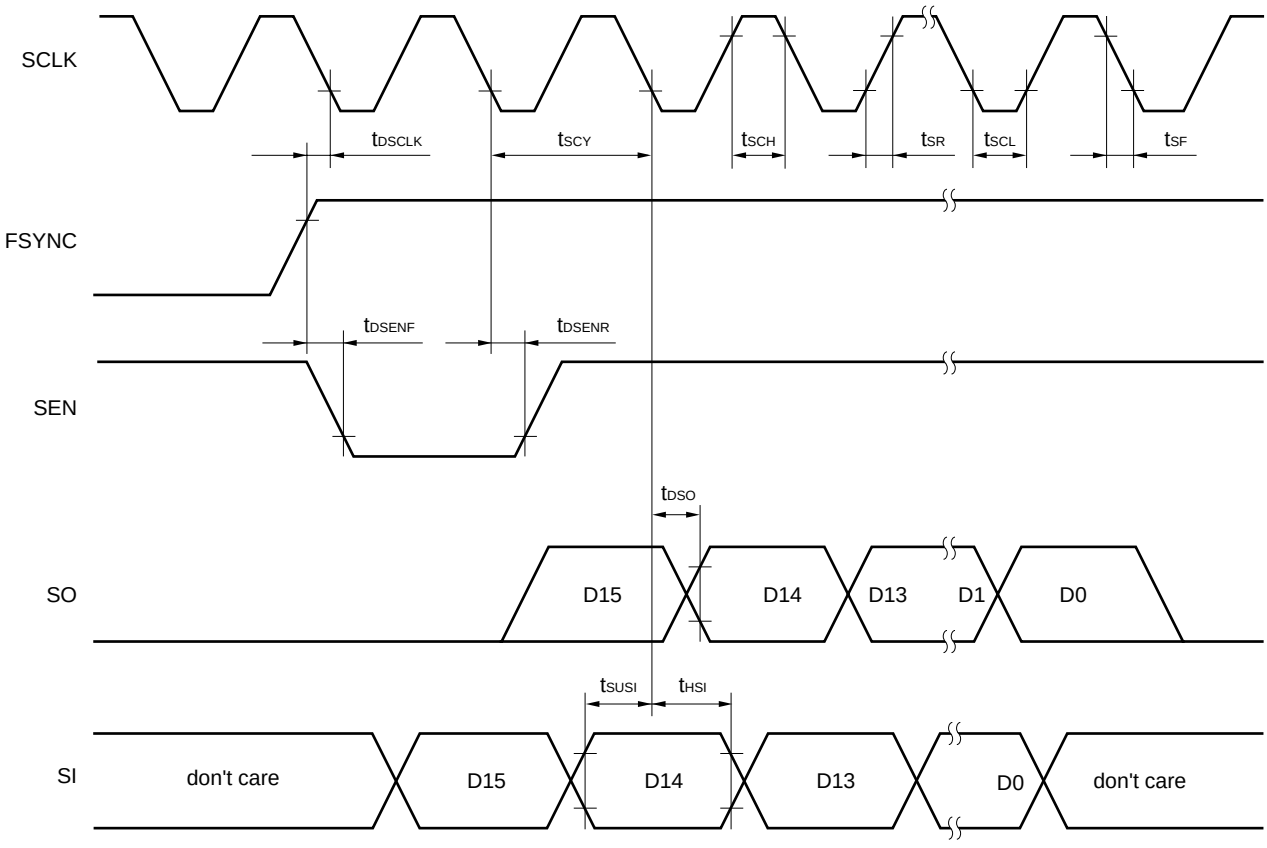


Remark D0 to D7: Microcontroller command (LSB first)

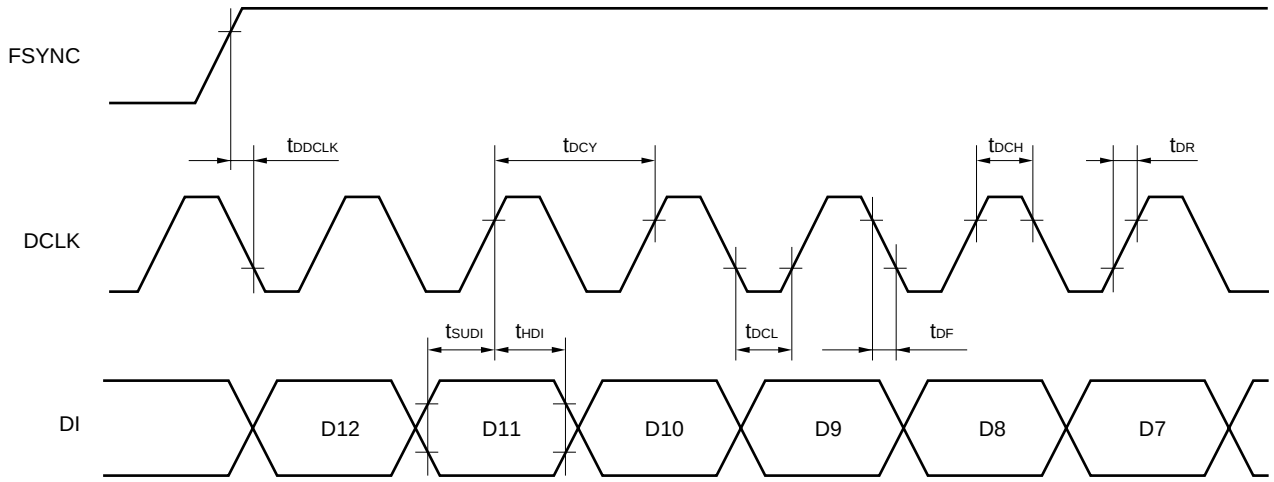
DSP interface timing (mode 1)



DSP interface timing (mode 2)

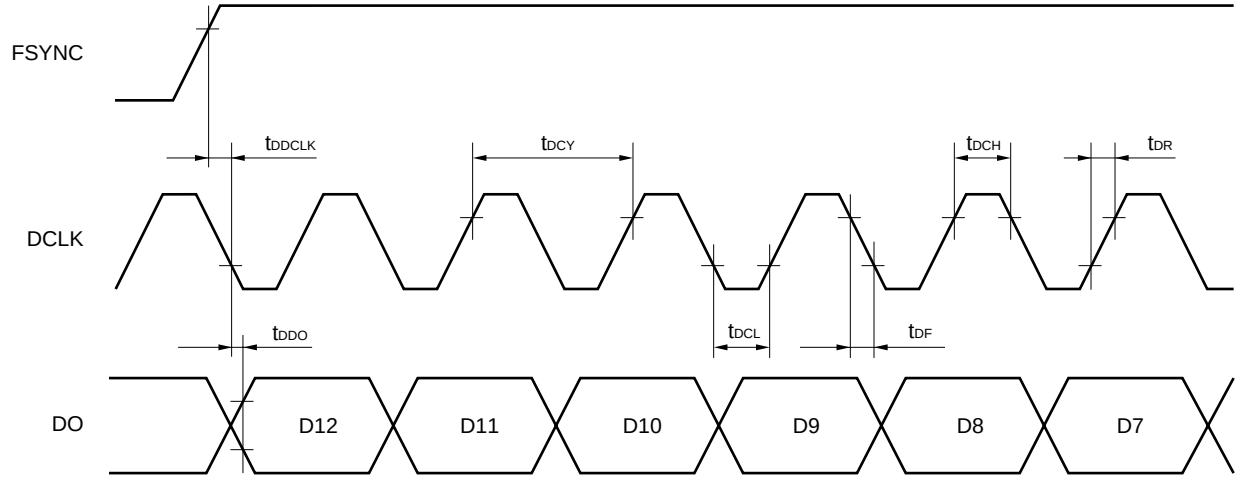


DAI input timing



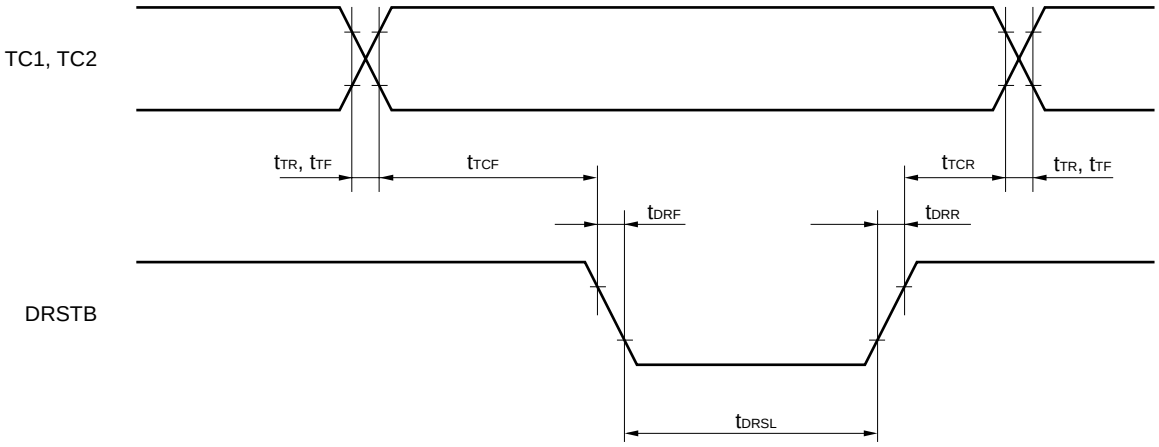
Remark D12 to D0: Input data (MSB first)

DAI output timing

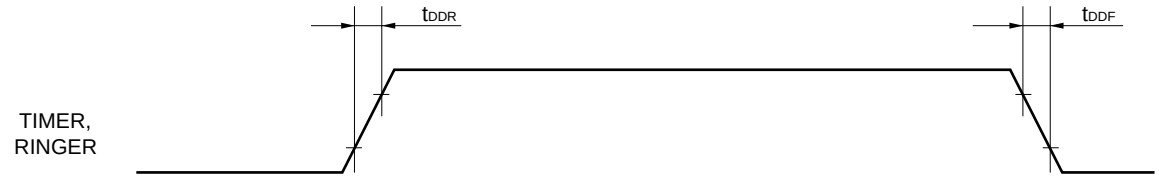


Remark D12 to D0: Output data (MSB first)

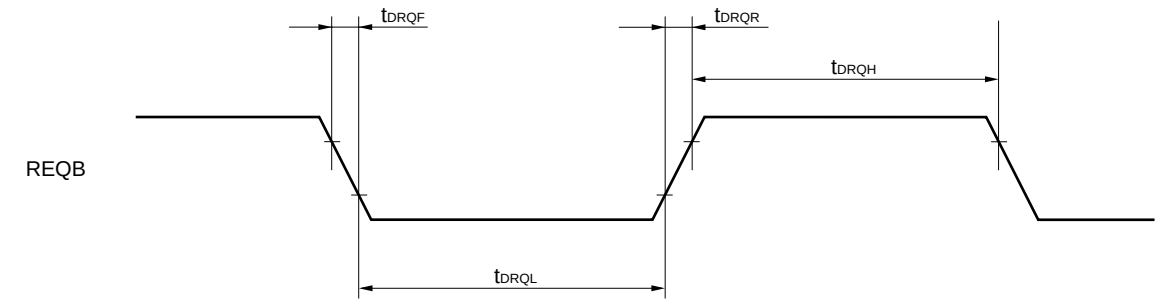
TC1, TC2, DRSTB input timing



TIMER, RINGER output timing



REQB input timing



TRANSMISSION CHARACTERISTICS

Transmission characteristics are as indicated below unless otherwise specified.

- Analog input
  Analog input signal (–10 dBm0, 1020 Hz) → accessory input part
  Accessory input: Set gain 0 dB
  Microphone input: Power down
  Pre-filter + mixer: Set gain 0 dB
- Analog output
  Analog output signal → accessory output part
  Receiver output: Power down
- Digital gain set
  Send and receive: 0 dB
- Digital input signal level: 0 dBm0
- T_A = 25°C, V_{DD} = 2.7 to 3.6 V (GND standard)

(1) Send/Receive Zero Transmission Level (0 dBm0 level)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Send Zero Transmission Level	V_{0TLPX}	600 Ω standard		–8.4		dBm
Receive Zero Transmission Level	V_{0TLPR}	600 Ω standard		–8.4		dBm

(2) Gain Characteristics

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Send Gain Deviation	G_X		–0.5		+0.5	dB
Receive Gain Deviation	G_R		–0.5		+0.5	dB
Send Gain Deviation Temperature Power Fluctuation	ΔG_X		–0.4		+0.4	dB
Receive Gain Deviation Temperature Power Fluctuation	ΔG_R		–0.4		+0.4	dB

(3) Transmission Loss Level

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Send Transmission Loss Level	G_{TX}	+3 to –40 dBm0	–0.4		+0.4	dB
		–40 to –50 dBm0	–0.6		+0.6	dB
		–50 to –55 dBm0	–1.2		+1.2	dB
Receive Transmission Loss Level	G_{TR}	+3 to –40 dBm0	–0.4		+0.4	dB
		–40 to –50 dBm0	–0.6		+0.6	dB
		–50 to –55 dBm0	–1.2		+1.2	dB

(4) Transmission Gain Frequency Characteristics

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Send Transmission Gain Frequency Characteristics	G_{RX1}	60 Hz			–23	dB
	G_{RX2}	200 Hz	–2.5		0	dB
	G_{RX3}	0.3 to 3.0 kHz	–0.3		+0.3	dB
	G_{RX4}	3.2 kHz	–0.65		+0.3	dB
	G_{RX5}	3.4 kHz	–0.8		0	dB
	G_{RX6}	4.0 kHz			–14	dB
	G_{RX7}	4.6 kHz or more			–28	dB
Receive Transmission Gain Frequency Characteristics	G_{RR3}	0.3 to 3.0 kHz	–0.3		+0.3	dB
	G_{RR4}	3.2 kHz	–0.65		+0.3	dB
	G_{RR5}	3.4 kHz	–0.8		0	dB
	G_{RR6}	4.0 kHz			–14	dB
	G_{RR7}	4.6 kHz or more			–28	dB

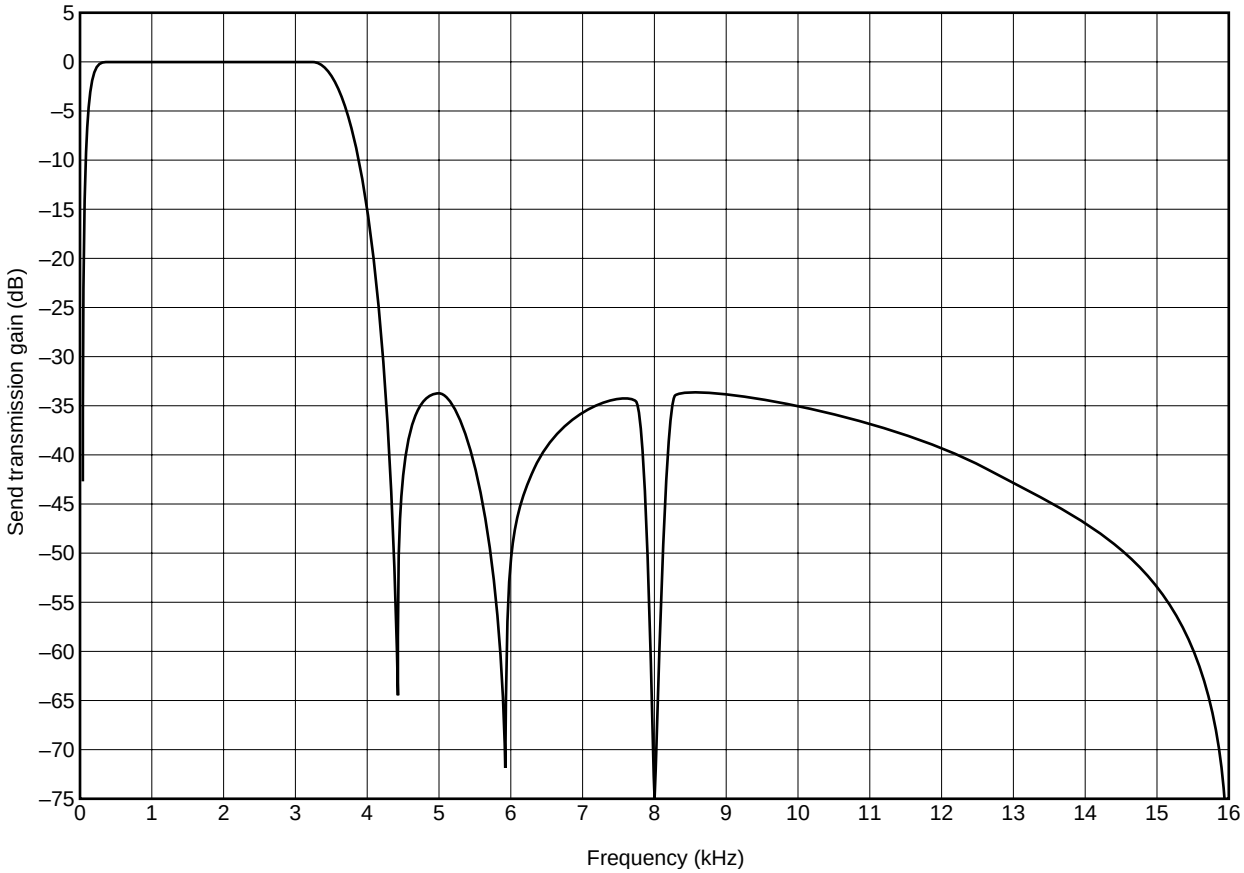
(5) Noise Characteristics

	Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	Send Noise	N_{XC}	Microphone power down, XAUXI– → ACOM, gain 0 dB, C message filter			25	dBrnc0
						–65	dBm0c
★	Receive Noise	N_{RC1}	C message filter, input +0 code from SI			25	dBrnc0
						–65	dBm0c
	Single Frequency Noise	N_{SF}	Send input → Receive output			–50	dBm0
	Cross-Talk between Send and Receive Channels	CT_{TR}	No sidetone pass, microphone power down input 0 dBm0 and 1020 Hz from XAUXI– input +0 code from SI			–60	dB
	Cross-Talk between Receive and Send Channels	CT_{RT}	No sidetone pass, microphone power down XAUXI– → ACOM input 0 dBm0 and 1020 Hz from SI			–60	dB
	Power Supply Voltage Variation Rejection	PSRR	V_{DD} ±100 mV_{0-p} signal application f = 0 to 3.4 kHz	30			dB

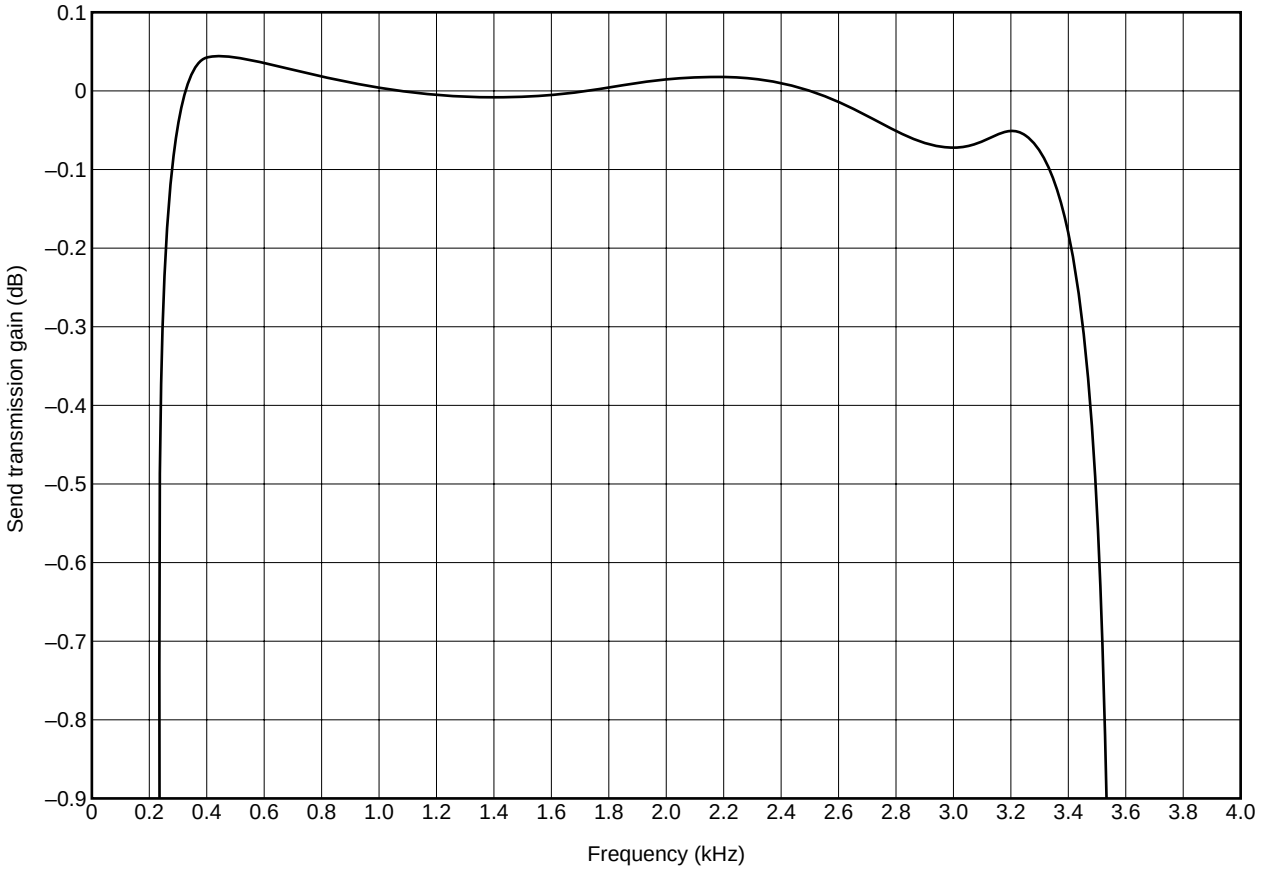
(6) Distortion Factor Characteristics

	Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★	Send Channel Total Power Distortion Factor	SD_X	0 to –10 dBm0		35			dB
			–40 dBm0		25			
			–45 dBm0		20			
★	Receive Channel Total Power Distortion Factor	SD_R	0 to –10 dBm0		35			dB
			–40 dBm0		25			
			–45 dBm0		20			
	Absolute Delay	D_A	XAUXI– → RAUXO				550	μs
	Delay Distortion Frequency Characteristics	D_O	XAUXI– → RAUXO	500 Hz			1.40	ms
				600 Hz			0.70	
				1 kHz			0.20	
				2.6 kHz			0.20	
				2.8 kHz			1.40	

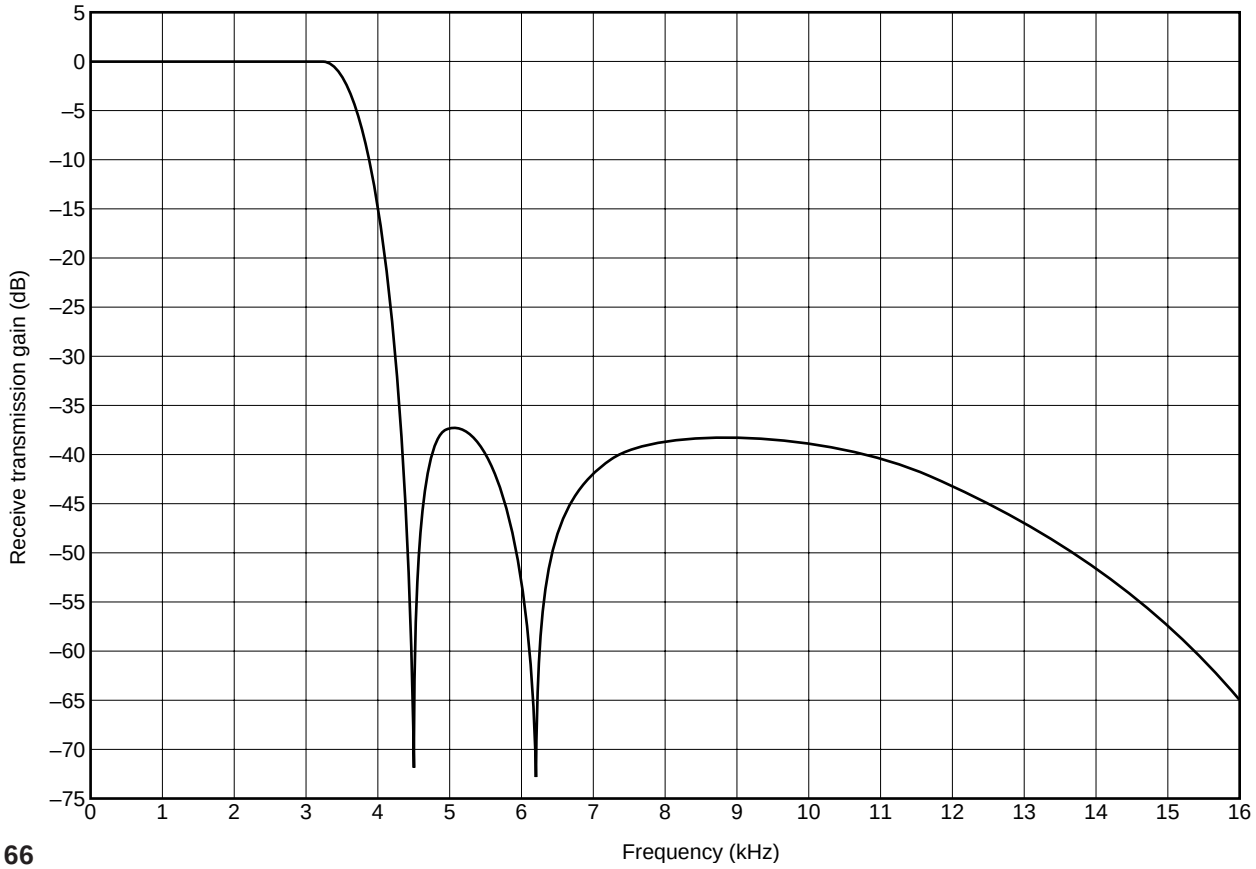
Send Transmission Gain Frequency Characteristics 1 (G_{RX})



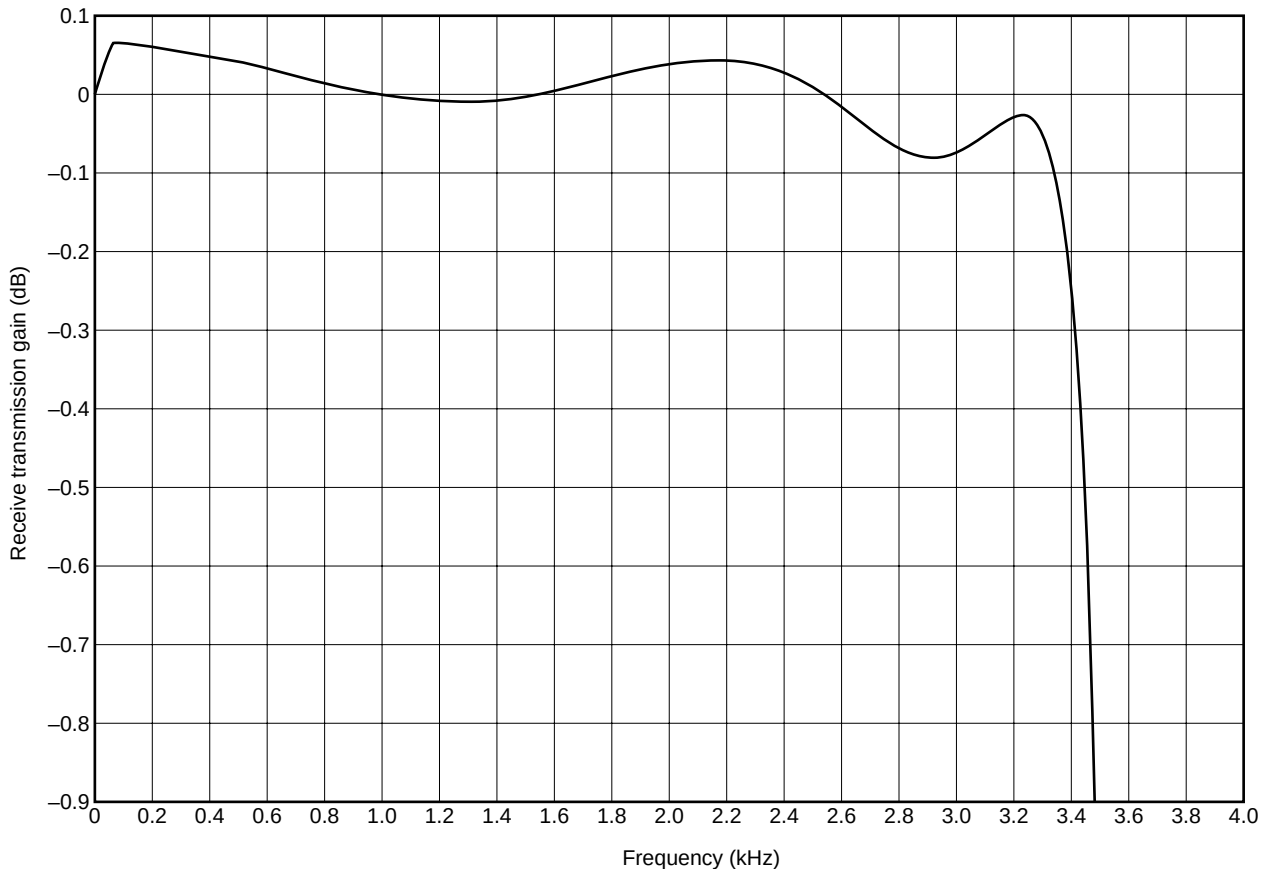
Send Transmission Gain Frequency Characteristics 2 (G_{RX})



Receive Transmission Gain Frequency Characteristics 1 (G_{RR})



Receive Transmission Gain Frequency Characteristics 2 (G_{RR})



★ Send/receive zero transmission level (0 dBm0 level) is explained below for your reference.

(a) Send zero transmission level

Analog output signal level at which the digital input signal level of the D/A converter becomes 0 dBm0.

(b) Receive zero transmission level

Analog input signal level at which the digital output signal level of the A/D converter becomes 0 dBm0.

(c) Analog signal level (dBm)

The conversion expression of the amplitude voltage of a signal and an analog signal level is as follows:

$X = 10 \log W$

X: analog signal level (dBm)

W: analog signal power (mW)

$W = (V^2/R) \times 10^3$

V: effective value of analog signal (AC) (Vrms)

R: resistance (Ω)

With the μPD9930, the signal voltage (effective value) can be calculated if R = 600 Ω and X = –8.4 dBm are substituted.

W = 0.1445 (mW)

V = 0.294 (Vrms)

To calculate $V_{0\text{-}p}$, multiply the signal voltage (effective value) by $\sqrt{2}$.

$V_{0\text{-}p}$ = 0.416 (V)

(d) Digital signal level (dBm0)

Signal level where the level of the full swing of the digital output value of the A/D converter and the digital input value of the D/A converter is considered to be 3.17 dBm0 (the amplitude of the analog signal is 1.2 $V_{p\text{-}p}$ where the gain of the microphone input or accessory input is 0 dB).

<Level diagram>

This diagram indicates the range in which adjustments can be made by using each amplifier and gain control function.

Example: Input level at which digital output of linear codec is –10 dBm0 is –33 dBm.

(Conditions)

Microphone amplifier gain during microphone input: 15 dB

Analog gain control: 0 dB

Digital gain control: 0 dB

Output level at which digital input of linear codec is –10 dBm0 is –18.4 dBm.

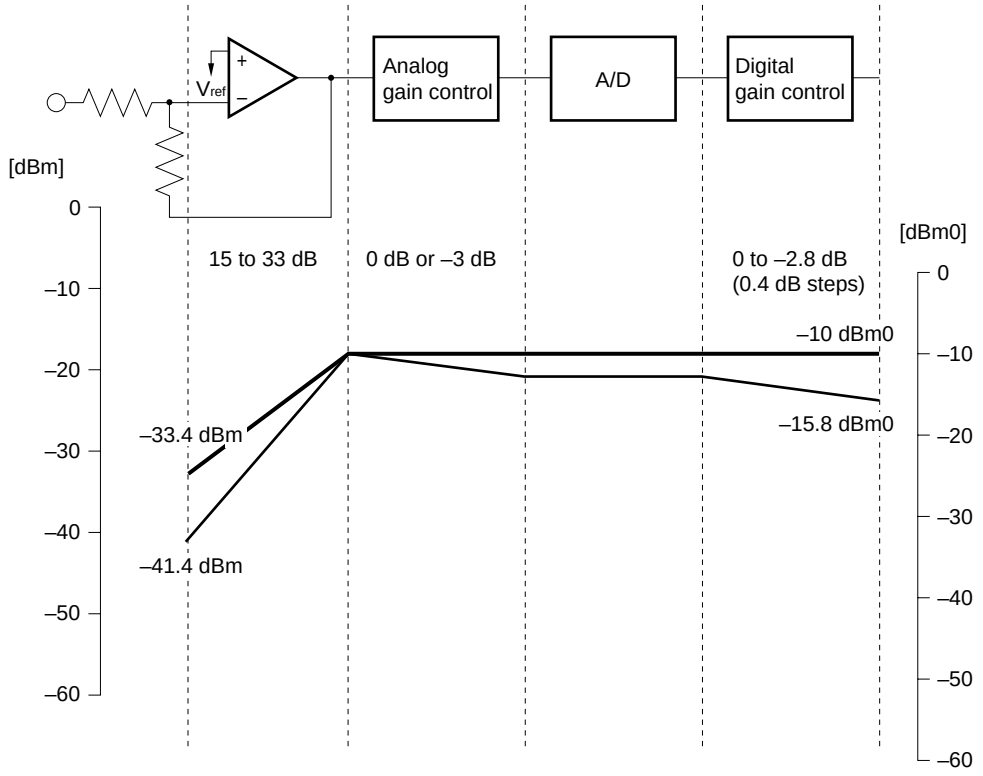
(Conditions)

During receiver output

Analog gain control: 0 dB

Digital gain control: 0 dB

★ **Voice send level diagram (microphone input)**

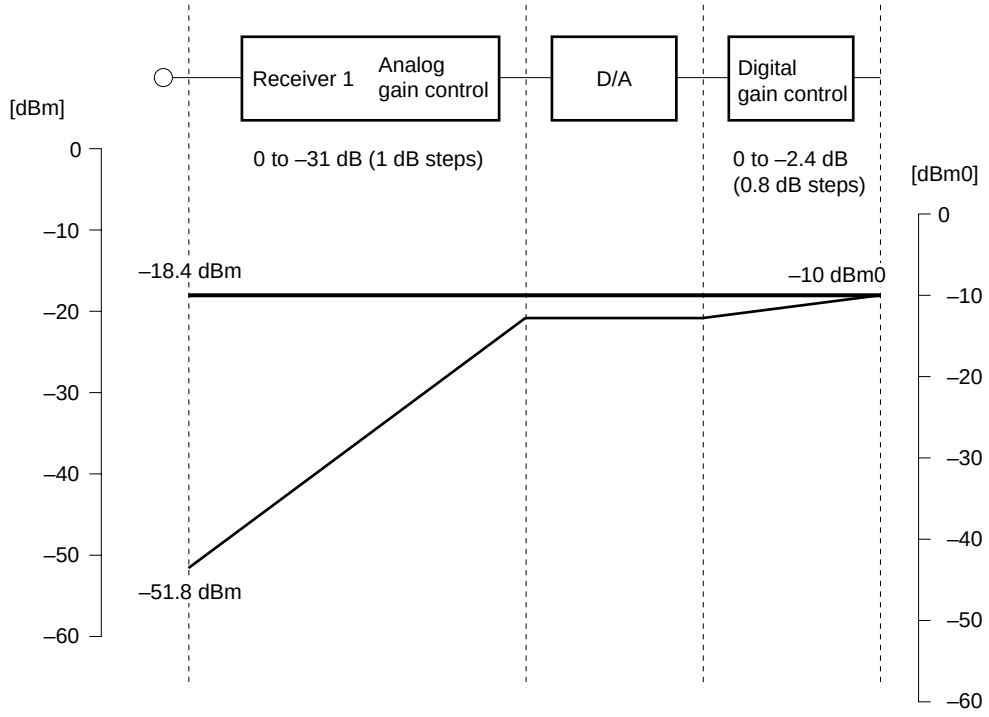


Remarks 1. Thick line: Indicates case where gain of microphone amplifier is set to 15 dB, gain of analog gain control to 0 dB, and gain of digital gain control to 0 dB.

Thin line: Indicates case where gain of microphone amplifier is set to 33 dB, gain of analog gain control to –3 dB, and gain of digital gain control to –2.8 dB.

2. Overload level: 3.17 dBm0.

★ **Voice receive level diagram (receiver output)**

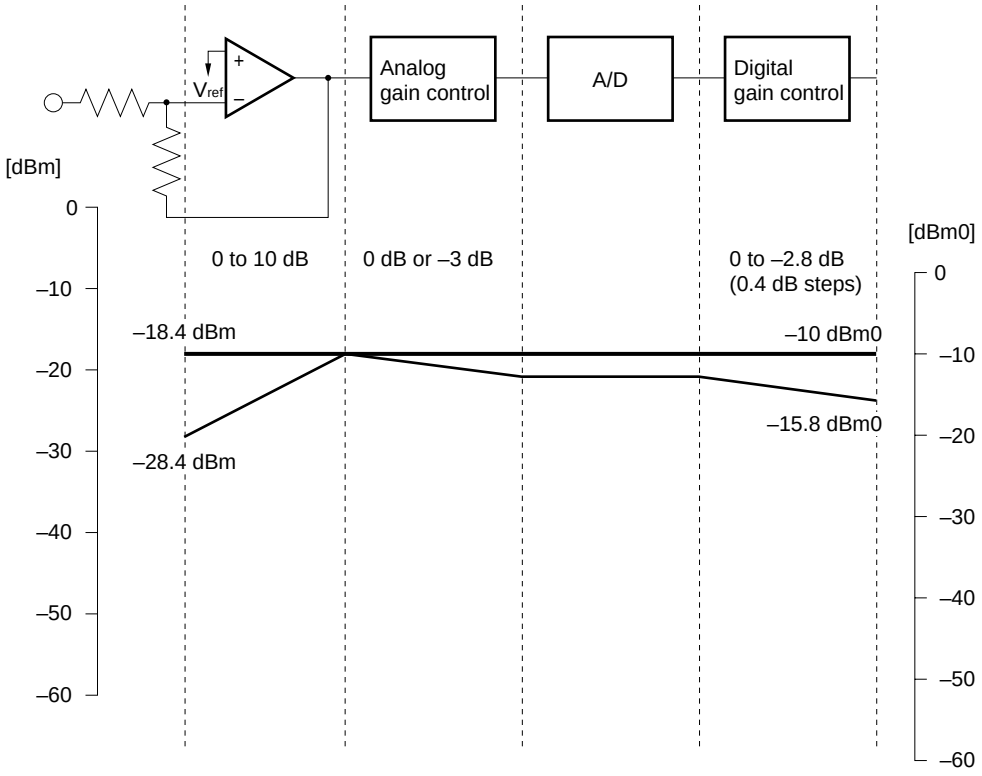


Remarks 1. Thick line: Indicates case where gain of analog gain control is set to 0 dB and gain of digital gain control to 0 dB.

Thin line: Indicates case where gain of analog gain control is set to –31 dB and gain of digital gain control to –2.4 dB.

2. Overload level: 3.17 dBm0.

★ **Voice send level diagram (accessory input)**

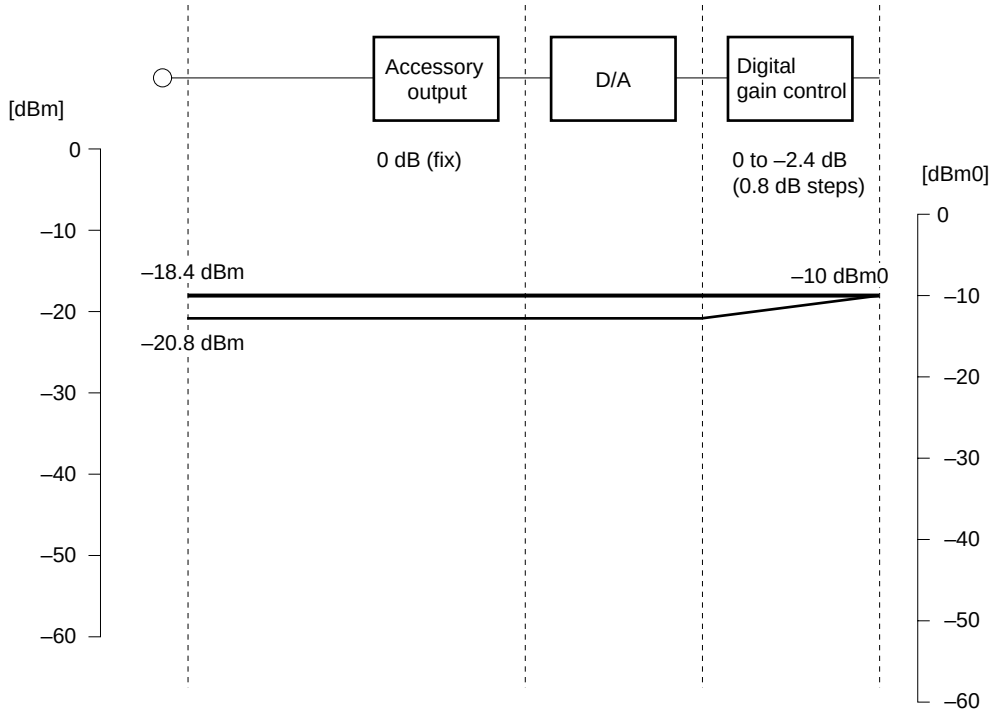


Remarks 1. Thick line: Indicates case where gain of microphone amplifier is set to 0 dB, gain of analog gain control to 0 dB, and gain of digital gain control to 0 dB.

Thin line: Indicates case where gain of microphone amplifier is set to 10 dB, gain of analog gain control to –3 dB, and gain of digital gain control to –2.8 dB.

2. Overload level: 3.17 dBm0.

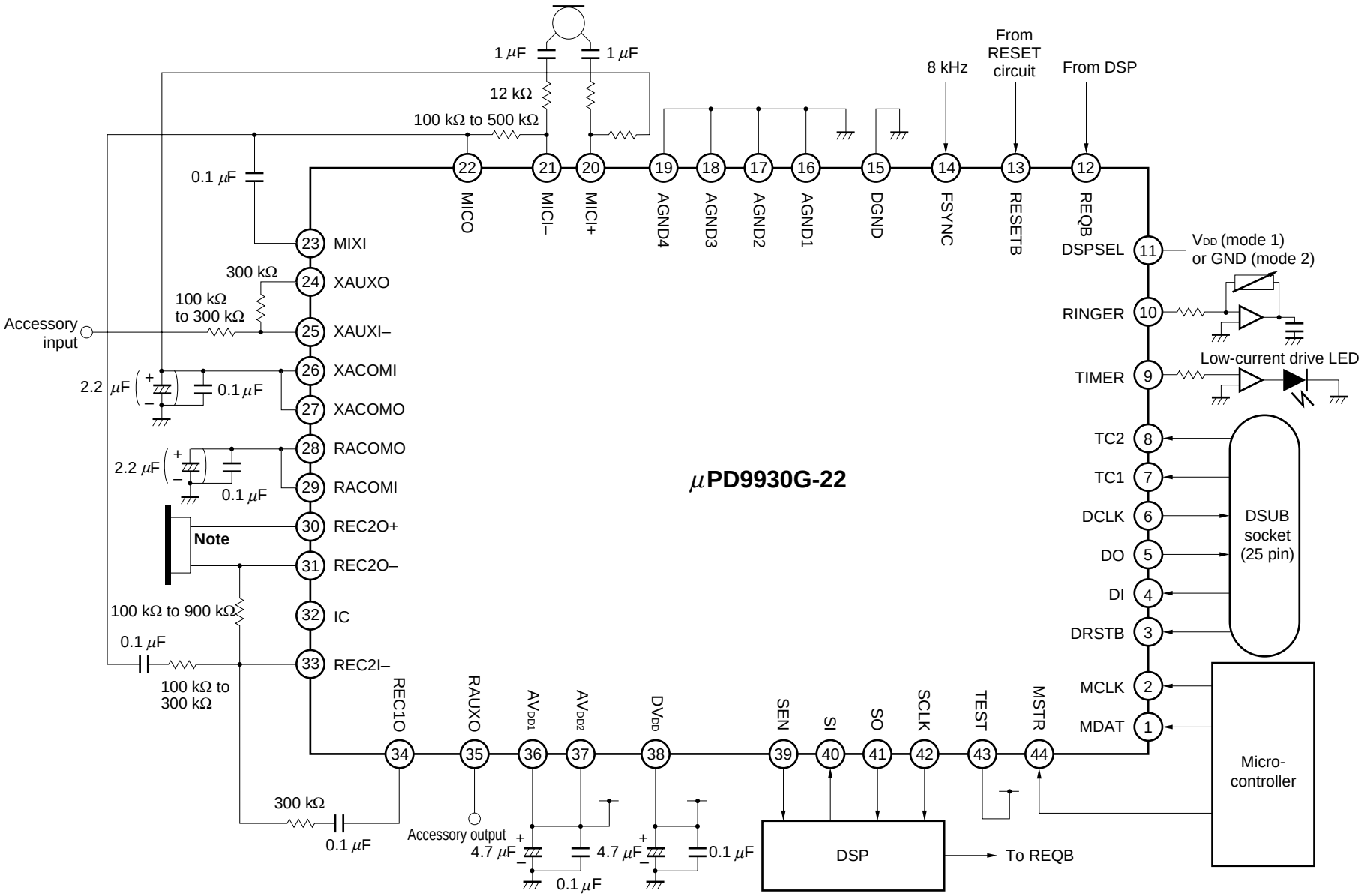
★ **Voice receive level diagram (accessory output)**



Remarks 1. Thick line: Indicates case where gain of digital gain control is set to 0 dB.
Thin line: Indicates case where gain of digital gain control is set to –2.4 dB.

2. Overload level: 3.17 dBm0.

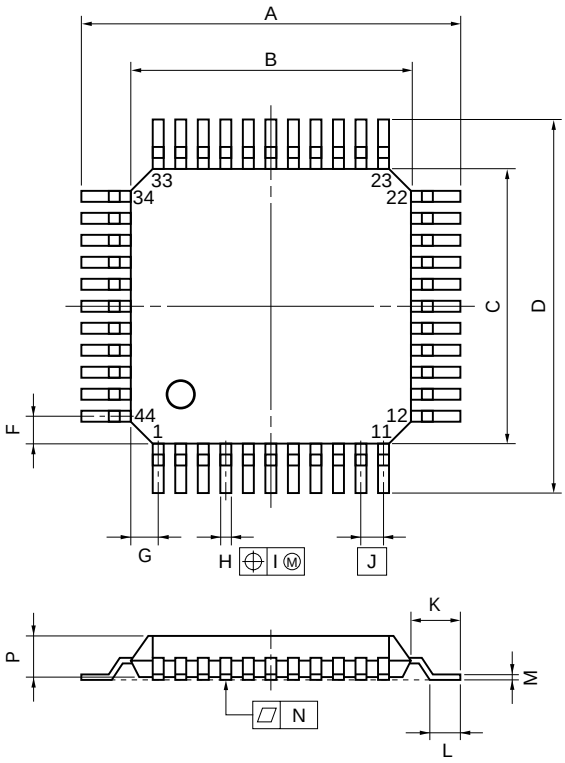
6. APPLIED CIRCUIT EXAMPLE

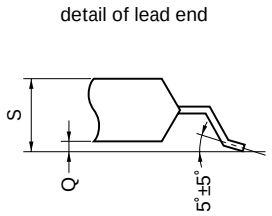


Note When connecting a dynamic receiver, use a drive amplifier.

7. PACKAGE DRAWINGS

44 PIN PLASTIC QFP (□10)





P44G-80-22-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	1.0±0.2	$0.039^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	1.45±0.1	$0.057^{+0.005}_{-0.004}$
Q	0.05±0.05	0.002±0.002
S	1.65 MAX.	0.065 MAX.

★ 8. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD9930.

For more details, refer to our document "Semiconductor Device Mounting Technology Manual" (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μPD9930G-22: 44-pin plastic QFP (10 x 10 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235°C or below, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 7 days (10 hours pre-baking is required at 125°C afterwards)	IR35-107-2
VPS	Peak temperature of package surface: 215°C or below, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 7 days (10 hours pre-baking is required at 125°C afterwards)	VP15-107-2
Wave soldering	Soldering bath temperature: 260°C or below, Reflow time: 10 seconds or below, Number of reflow processes: 1 Preheating temperature: 120°C MAX. (package surface temperature) Exposure limit[Note]: 7 days (10 hours pre-baking is required at 125°C afterwards)	WS60-107-1
Partial heating method	Terminal temperature: 300°C or below, Time: 3 seconds or below (Per one side of the device).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25°C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The export of this product from Japan is prohibited without governmental license. To export or re-export this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.