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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD98502

NETWORK CONTROLLER

The μPD98502 network controller is an LSI for network terminal applications such as ADSL systems. The controller integrates a VR4120A™ MIPS™ RISC CPU core, memory interface, PCI, and other network interface functions such as ATM, Ethernet™, and USB on one chip.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

μPD98502 User's Manual: S15543E

FEATURES

- Includes high performance MIPS based 64-bit RISC processor VR4120A
- Can perform RTOS and network middleware (M/W) on the chip
- Includes interface for PROM and flash ROM used for storing boot program
- Includes 32-bit RISC controller in ATM Cell Processor
- Software SAR processing by RISC controller affords flexibility for specification update
- Supports CBR/VBR/UBR service classes
- Include 2-channel 10/100-Mbps Ethernet controllers compliant to IEEE802.3, IEEE 802.3u and IEEE802.3x
- Can directly connect external Ethernet PHY device through 3.3 V MII interface
- Includes USB full speed function controller compliant to USB specification 1.1
- Supports operation conforming to the USB Communication Device Class Specification
- Can directly connect 64-Mbit and 128-Mbit SDRAM as external memory
- Includes 32-bit 33-MHz PCI Bus Master compliant to PCI Specification Rev. 2.2
- Includes 8-bit 16.5/25/33-MHz UTOPIA level 2 interface compliant to ATM Forum af-phy-0039
- Includes boundary scan function (JTAG) compliant to IEEE 1149.1
- Include UART and Micro Wire™ interfaces
- Include 2-ch general purpose timers
- Using advanced CMOS technology
- Power supply 2.5V(Core)/3.3V(I/O)
- Package 500-pin T-BGA

ORDERING INFORMATION

Part Number	Package
μPD98502N7-H6	500-pin tape BGA (Heat spreader type) (40 × 40)

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The mark ★ shows major revised points.

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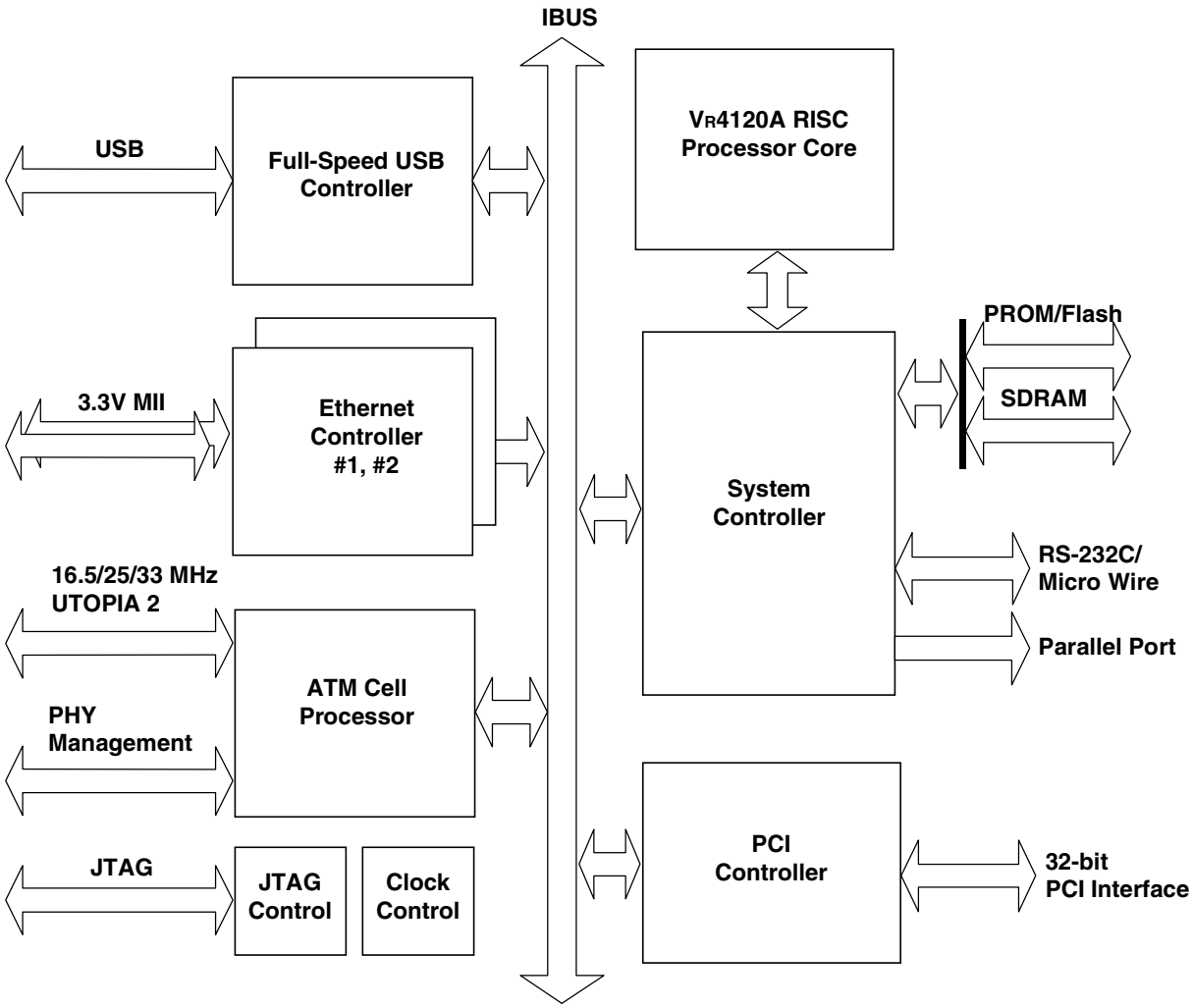
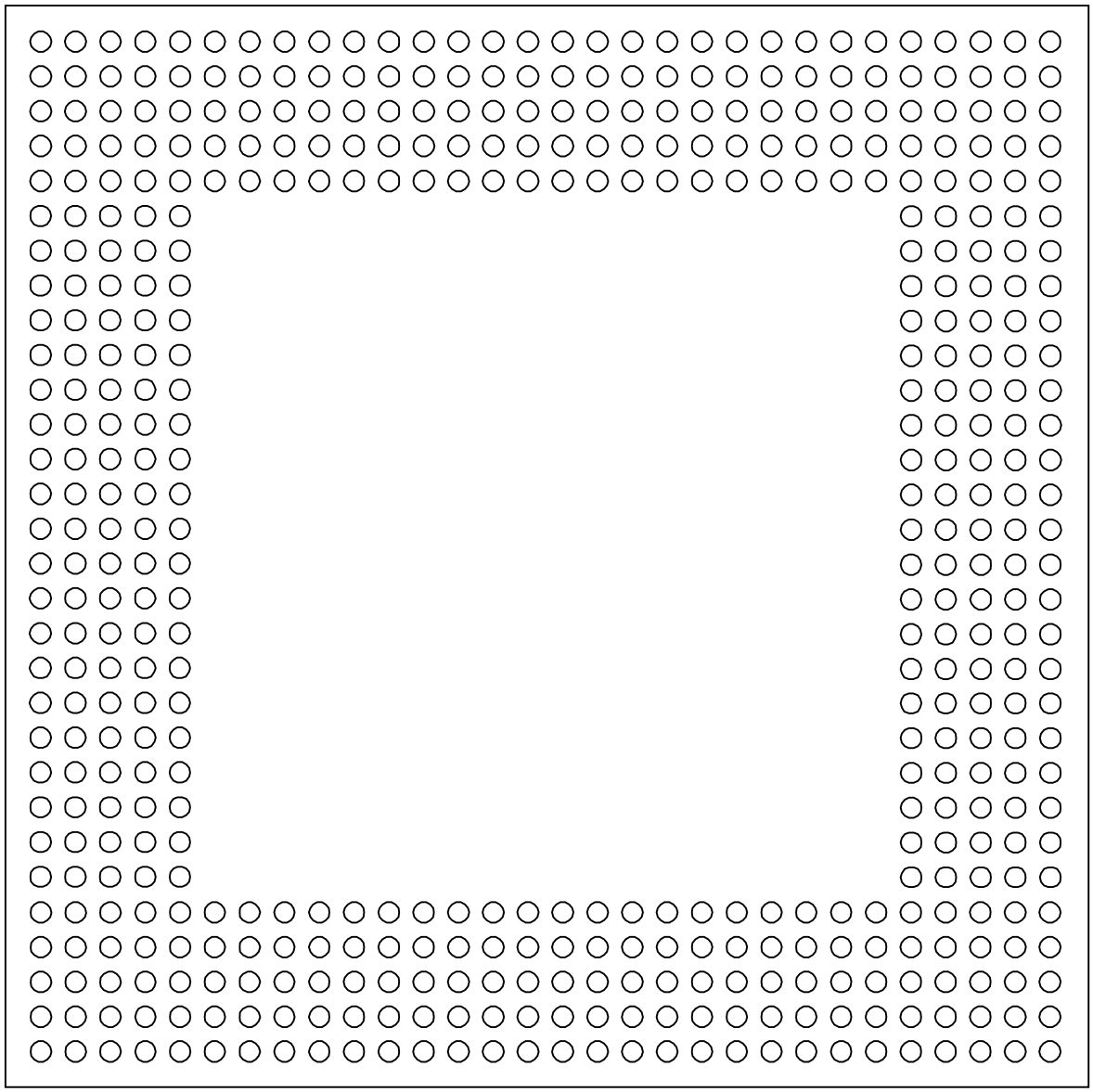
INTERNAL BLOCK DIAGRAM



PIN CONFIGURATION (Bottom View)

• 500-pin tape BGA (Heat spreader type) (40 × 40)
μPD98502N7-H6

Index Mark



PIN TABLE

(1/3)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	SMA13	B10	URSDO	C19	IC-PDnR	D28	PGTO2_B	F27	GND
A2	SMD0	B11	RMSL1	C20	IC-OPEN	D29	PRQI1_B	F28	GND
A3	SMD4	B12	MWDO	C21	JDI	D30	PAD0	F29	PAD5
A4	SMD7	B13	POM3	C22	GND	E1	GND	F30	PAD6
A5	SMD19	B14	POM5	C23	USBDM	E2	SDRAS_B	G1	SMA8
A6	SMD22	B15	EVDD	C24	IC-OPEN	E3	SMA0	G2	SMA15
A7	SRMCS_B	B16	IC-OPEN	C25	PUDGND	E4	SMA10	G3	SDCLK1
A8	URDSR_B	B17	IC-OPEN	C26	IVDD	E5	GND	G4	EVDD
A9	URDCD_B	B18	IC-PUpR★	C27	PMODE	E6	EVDD	G5	SDCAS_B
A10	URDTR_B	B19	IC-OPEN	C28	PGTO3_B	E7	SMD16	G26	PAD1
A11	MWSK	B20	GND	C29	PGTO1_B	E8	GND	G27	PAD3
A12	MWDI	B21	IC-PDn	C30	PRQI0_B	E9	EVDD	G28	EVDD
A13	EXNMI_B	B22	JDO	D1	SDWE_B	E10	GND	G29	PAD7
A14	POM6	B23	GND	D2	SMA1	E11	RMSL0	G30	PAD8
A15	EXINT_B	B24	USBDP	D3	SMA11	E12	GND	H1	SMA4
A16	IVDD	B25	PUDVD	D4	IVDD	E13	POM0	H2	SMA7
A17	IC-PUpR★	B26	IC-OPEN	D5	SMD3	E14	GND	H3	SMA9
A18	IC-PDnR	B27	PUMD_B★	D6	SMD6	E15	POM7	H4	IVDD
A19	IC-OPEN	B28	PHINT_B	D7	EVDD	E16	GND	H5	GND
A20	IC-OPEN	B29	PRSTO_B	D8	IVDD	E17	GND	H26	GND
A21	IC-PDn	B30	PGTO0_B	D9	URCLK	E18	IC-OPEN	H27	IVDD
A22	JCK	C1	SMA2	D10	IVDD	E19	GND	H28	PCBE0_B
A23	JMS	C2	GND	D11	GND	E20	IC-PDn	H29	PAD9
A24	EVDD	C3	SMA16	D12	IVDD	E21	GND	H30	GND
A25	EVDD	C4	SMD2	D13	POM1	E22	EVDD	J1	SMA18
A26	PUAVD	C5	GND	D14	IVDD	E23	GND	J2	SMA3
A27	GND	C6	SMD18	D15	IC-PDnR	E24	USBCLK	J3	SMA5
A28	IC-OPEN	C7	SMD21	D16	BIG	E25	EVDD	J4	SMA6
A29	GND	C8	SRMOE_B	D17	IVDD	E26	GND	J5	EVDD
A30	PSERI_B	C9	GND	D18	IC-OPEN	E27	PRQI3_B	J26	EVDD
B1	SMA12	C10	URRTS_B	D19	IVDD	E28	PRQI2_B	J27	PAD10
B2	SMA14	C11	EVDD	D20	IC-OPEN	E29	PAD2	J28	PAD11
B3	SMD1	C12	MWCS	D21	IVDD	E30	PAD4	J29	PAD12
B4	SMD5	C13	POM2	D22	JRSTB_B	F1	SMA17	J30	PAD13
B5	SMD17	C14	POM4	D23	IVDD	F2	SDCKE1	K1	SMD31
B6	SMD20	C15	ENDCEN	D24	PUAGND	F3	SDCS_B	K2	SMA20
B7	SMD23	C16	GND	D25	PUSTBY	F4	GND	K3	SMA19
B8	URCTS_B	C17	IC-PDnR	D26	PARBN	F5	EVDD	K4	IVDD
B9	URSDI	C18	IC-OPEN	D27	IVDD	F26	EVDD	K5	GND

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
K26	GND	P5	GND	V4	IVDD	AB3	IC-PUp	AF2	MICRS
K27	IVDD	P26	GND	V5	GND	AB4	IC-PDn	AF3	MIMCLK
K28	PAD14	P27	IVDD	V26	PAD26	AB5	EVDD	AF4	MITD3
K29	PAD15	P28	PAD16	V27	PAD25	AB26	EVDD	AF5	GND
K30	EVDD	P29	PAD17	V28	PAD24	AB27	IC-OPEN	AF6	EVDD
L1	SDCLK0	P30	PAD18	V29	GND	AB28	IC-OPEN	AF7	MI2TE
L2	GND	R1	EVDD	V30	PSCLK	AB29	GND	AF8	GND
L3	SDCKE0	R2	SMD12	W1	IC-PUp	AB30	RST_B	AF9	EVDD
L4	SMD30	R3	SMD9	W2	IVDD	AC1	IC-PUp	AF10	GND
L5	EVDD	R4	SMD10	W3	IC-PUp	AC2	MIRD3	AF11	UDRD1
L26	PCBE1_B	R5	SMD11	W4	IVDD	AC3	GND	AF12	GND
L27	GND	R26	EVDD	W5	GND	AC4	IVDD	AF13	UDRAD2
L28	PAR	R27	PAD19	W26	GND	AC5	GND	AF14	GND
L29	PSERO_B	R28	PAD20	W27	IVDD	AC26	GND	AF15	UDTAD3
L30	PER_B	R29	GND	W28	PAD28	AC27	IVDD	AF16	UDTD7
M1	EVDD	R30	PAD21	W29	EVDD	AC28	IC-OPEN	AF17	GND
M2	SMD28	T1	SMD8	W30	PAD27	AC29	IC-OPEN	AF18	EVDD
M3	SMD29	T2	GND	Y1	IC-OPEN	AC30	PINT_B	AF19	GND
M4	IVDD	T3	CLKUSL1	Y2	PSDGND	AD1	MIRD2	AF20	UMWR_B
M5	GND	T4	CLKUSL0	Y3	PSAGND	AD2	MIRD1	AF21	GND
M26	GND	T5	EVDD	Y4	PSAVD	AD3	MIRCLK	AF22	EVDD
M27	IVDD	T26	PAD22	Y5	PSDVD	AD4	MIRER	AF23	GND
M28	PSTP_B	T27	IVDD	Y26	PAD31	AD5	MIRDV	AF24	GND
M29	PDSEL_B	T28	GND	Y27	PME_B	AD26	GND	AF25	EVDD
M30	EVDD	T29	PAD23	Y28	PRQO_B	AD27	EVDD	AF26	GND
N1	SMD24	T30	PCBE3_B	Y29	PAD30	AD28	IC-PDnR	AF27	GND
N2	SMD25	U1	CLKSL	Y30	PAD29	AD29	IC-OPEN	AF28	IC-PDnR
N3	GND	U2	GND	AA1	IC-OPEN	AD30	GND	AF29	IC-PDnR
N4	SMD26	U3	IC-PUp	AA2	PSTBY	AE1	MIRD0	AF30	IC-PDnR
N5	SMD27	U4	IVDD	AA3	PSMD_B★	AE2	GND	AG1	MIMD
N26	PTRY_B	U5	GND	AA4	IVDD	AE3	MITER	AG2	GND
N27	PIRY_B	U26	GND	AA5	GND	AE4	IVDD	AG3	MITD2
N28	GND	U27	IVDD	AA26	GND	AE5	EVDD	AG4	IVDD
N29	PFRA_B	U28	PIDSEL	AA27	IVDD	AE26	EVDD	AG5	MI2COL
N30	PCBE2_B	U29	GND	AA28	PGTI_B	AE27	IC-PDnR	AG6	IVDD
P1	SMD13	U30	EVDD	AA29	GND	AE28	IC-PDnR	AG7	MI2CRS
P2	SMD14	V1	SCLK	AA30	EVDD	AE29	IC-PDnR	AG8	IVDD
P3	SMD15	V2	GND	AB1	IC-OPEN	AE30	IC-PDnR	AG9	UDRSC
P4	IVDD	V3	IC-PUp	AB2	GND	AF1	MITE	AG10	IVDD

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
AG11	UDRD0	AH3	MICOL	AH25	EVDD	AJ17	UDTD5	AK9	UDRD5
AG12	IVDD	AH4	MI2RD0	AH26	IVDD	AJ18	GND	AK10	UDRD2
AG13	UDRAD1	AH5	MI2MD	AH27	UMAD8	AJ19	UMRDY_B	AK11	UDRCLK
AG14	IVDD	AH6	MI2TER	AH28	UMAD7	AJ20	GND	AK12	UDRAD3
AG15	UDTAD2	AH7	MI2TD3	AH29	UMAD3	AJ21	EVDD	AK13	UDRAD0
AG16	UDTAD0	AH8	GND	AH30	UMAD1	AJ22	UMD13	AK14	UDTE_B
AG17	IVDD	AH9	UDRCLV	AJ1	MITD0	AJ23	UMD9	AK15	UDTAD4
AG18	UDTD1	AH10	UDRD4	AJ2	MI2MCLK	AJ24	UMD7	AK16	UDTCLK
AG19	IVDD	AH11	UDTCLV	AJ3	MI2RD1	AJ25	UMD4	AK17	UDTD6
AG20	UMMD	AH12	IC-OPEN	AJ4	GND	AJ26	UMD1	AK18	UDTD3
AG21	IVDD	AH13	EVDD	AJ5	MI2RER	AJ27	GND	AK19	UDTD0
AG22	UMD10	AH14	UDTSC	AJ6	GND	AJ28	GND	AK20	UMRST_B
AG23	IVDD	AH15	EVDD	AJ7	MI2TD1	AJ29	UMAD6	AK21	UMRD_B
AG24	UMD2	AH16	UDTAD1	AJ8	UDRE_B	AJ30	UMAD4	AK22	UMD14
AG25	UMAD11	AH17	UDTD4	AJ9	UDRD6	AK1	MI2RD3	AK23	UMD12
AG26	UMAD9	AH18	UDTD2	AJ10	UDRD3	AK2	MI2RD2	AK24	UMD8
AG27	IVDD	AH19	UMINT_B	AJ11	UDRAD4	AK3	MI2RCLK	AK25	UMD6
AG28	UMAD2	AH20	UMSL_B	AJ12	IC-OPEN	AK4	MI2RDV	AK26	UMD3
AG29	UMAD0	AH21	UMD15	AJ13	GND	AK5	MI2TCLK	AK27	UMD0
AG30	IVDD	AH22	UMD11	AJ14	GND	AK6	MI2TD2	AK28	UMAD10
AH1	MITCLK	AH23	GND	AJ15	IVDD	AK7	MI2TD0	AK29	IC-PUp
AH2	MITD1	AH24	UMD5	AJ16	GND	AK8	UDRD7	AK30	UMAD5

Special pin name description:

IC-PDn: Pull Down
IC-PDnR: Pull Down with Resistor
IC-PUp: Pull Up
IC-PUpR: Pull Up with Resistor

Remark In this document, XXX_B stands for active low pin.

CONTENTS

1. PIN FUNCTIONS

Symbol of I/O column indicates following status in this section.

I : Input
O : Output
I/O : Bidirection
I/OZ : Bidirection (Include Hi-Z state)
OZ : Output (Include Hi-Z state)
OD : Output (Open drain)

1.1 Power Supply

Pin Name	Pin No.	I/O	Active Level	Function
GND	A27, A29, B20, B23, C2, C5, C9, C16, C22, D11, E1, E5, E8, E10, E12, E14, E16, E17, E19, E21, E23, E26, F4, F27, F28, H5, H26, H30, K5, K26, L2, L27, M5, M26, N3, N28, P5, P26, R29, T2, T28, U2, U5, U26, U29, V2, V5, V29, W5, W26, AA5, AA26, AA29, AB2, AB29, AC3, AC5, AC26, AD26, AD30, AE2, AF5, AF8, AF10, AF12, AF14, AF17, AF19, AF21, AF23, AF24, AF26, AF27, AG2, AH8, AH23, AJ4, AJ6, AJ13, AJ14, AJ16, AJ18, AJ20, AJ27, AJ28			GND (0 V)
IVDD	A16, C26, D4, D8, D10, D12, D14, D17, D19, D21, D23, D27, H4, H27, K4, K27, M4, M27, P4, P27, T27, U4, U27, V4, W2, W4, W27, AA4, AA27, AC4, AC27, AE4, AG4, AG6, AG8, AG10, AG12, AG14, AG17, AG19, AG21, AG23, AG27, AG30, AH26, AJ15			Internal logic core power supply (+2.5 V)
EVDD	A24, A25, B15, C11, D7, E6, E9, E22, E25, F5, F26, G4, G28, J5, J26, K30, L5, M1, M30, R1, R26, T5, U30, W29, AA30, AB5, AB26, AD27, AE5, AE26, AF6, AF9, AF18, AF22, AF25, AH13, AH15, AH25, AJ21			External (I/O) power supply (+3.3 V)

1.2 System PLL Power Supply

	Pin Name	Pin No.	I/O	Active Level	Function
★	PSAGND	Y3			Analog ground (0 V)
★	PSAVD	Y4			Analog power supply (+2.5 V)
★	PSDGND	Y2			Digital ground (0 V)
★	PSDVD	Y5			Digital power supply (+2.5 V)

1.3 USB PLL Power Supply

	Pin Name	Pin No.	I/O	Active Level	Function
★	PUAGND	D24			Analog ground (0 V)
★	PUAVD	A26			Analog power supply (+2.5 V)
★	PUDGND	C25			Digital ground (0 V)
★	PUDVD	B25			Digital power supply (+2.5 V)

1.4 System Control Interface

Pin Name	Pin No.	I/O	Active Level	Function
SCLK	V1	I		System clock (33 MHz)
CLKSL	U1	I		Clock select (L: 100 MHz/H: 66 MHz) for VR4120A and SDRAM
★ PSMD_B	AA3	I	L	System PLL mode control (L: normal, H: through) Note
PSTBY	AA2	I	H	System PLL standby mode control (L: active, H: standby)
★ PUMD_B	B27	I	L	USB PLL mode control (L: normal, H: through) Note
PUSTBY	D25	I	H	USB PLL standby mode control (L: active, H: standby)
BIG	D16	I	H	VR4120A big endian mode
ENDCEN	C15	I		Endian converter enable
EXINT_B	A15	I	L	External interrupt
EXNMI_B	A13	I	L	External non-maskable interrupt
RST_B	AB30	I	L	System reset
RMSL0, RMSL1	E11, B11	I		ROM access bus width select (RMSL1/0 = L/L: 32-bit, L/H: 16-bit, H/L: 8-bit)

★ **Note** PSMD_B and PUMD_B pins shall be connected to GND.

1.5 Memory Interface

Pin Name	Pin No.	I/O	Active Level	Function
SDCLK0, SDCLK1	L1, G3	O		SDRAM clock
SDCKE0, SDCKE1	L3, F2	O	H	SDRAM clock enable
SDCS_B	F3	O	L	Chip select
SDRAS_B	E2	O	L	Row address strobe
SDCAS_B	G5	O	L	Column address strobe
SDWE_B	D1	O	L	Write enable
SRMCS_B	A7	O	L	PROM/FLASH chip select
SRMOE_B	C8	O	L	PROM/FLASH output enable
SMA0 - SMA20	E3, D2, C1, J2, H1, J3, J4, H2, G1, H3, E4, D3, B1, A1, B2, G2, C3, F1, J1, K3, K2	O		Memory address
SMD0 - SMD31	A2, B3, C4, D5, A3, B4, D6, A4, T1, R3, R4, R5, R2, P1, P2, P3, E7, B5, C6, A5, B6, C7, A6, B7, N1, N2, N4, N5, M2, M3, L4, K1	I/O		Memory data

1.6 PCI Interface

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Pin Name	Pin No.	I/O	Active Level	Function
PSCLK	V30	I		PCI clock (33 MHz)
★ PARBN	D26	I	H	PCI arbiter enable NIC Mode : Not available (Connect to GND) Host Mode : Control for Internal Bus Arbiter High -> Enable Low -> Disable
PMODE	C27	I		PCI mode select (L: host, H: NIC)
★ PIDSEL	U28	I	H	Initialization device select NIC Mode : Available Host Mode : Not Available (Connect to GND)
PDSEL_B	M29	I/OZ	L	Device select
PER_B	L30	I/OZ	L	Parity error
PFRA_B	N29	I/OZ	L	Cycle frame
★ PHINT_B	B28	I	L	PCI host interrupt NIC Mode : Not available (Connect to EVDD) Host Mode : Available
★ PINT_B	AC30	O	L	Interrupt_A NIC Mode : Available Host Mode : Not Available (Leave open)
PIRY_B	N27	I/OZ	L	Initiator ready
★ PME_B	Y27	OD	L	Power management event NIC Mode : Available Host Mode : Not Available (Leave open)
★ PRSTO_B	B29	O	L	PCI system reset out NIC Mode : Not Available (Leave open) Host Mode : Available
★ PSERI_B	A30	I	L	System error in NIC Mode : Not available (Connect to EVDD) Host Mode : Available
★ PSERO_B	L29	O	L	System error out NIC Mode : Available Host Mode : Not Available (Leave open)
PTRY_B	N26	I/OZ	L	Target ready
PSTP_B	M28	I/OZ	L	Stop request from target
PCBE[0:3]_B	H28, L26, N30, T30	I/OZ	L	Bus command and byte enable
★ PRQO_B	Y28	O	L	Bus request out NIC Mode : Available Host Mode : Not Available (Leave open)
★ PRQI[0:3]_B	C30, D29, E28, E27	I	L	Bus request in NIC Mode : Not available (Connect to EVDD) Host Mode : Available
★ PGTI_B	AA28	I	L	Bus grant in NIC Mode : Available Host Mode : Not available (Connect to EVDD)

(2/2)

Pin Name	Pin No.	I/O	Active Level	Function
★ PGTO[0:3]_B	B30, C29, D28, C28	O	L	Bus grant out NIC Mode : Not Available (Leave open) Host Mode : Available
PAR	L28	I/OZ		Parity of address/data
PAD0 - PAD31	D30, G26, E29, G27, E30, F29, F30, G29, G30, H29, J27, J28, J29, J30, K28, K29, P28, P29, P30, R27, R28, R30, T26, T29, V28, V27, V26, W30, W28, Y30, Y29, Y26	I/OZ		PCI address and data

1.7 ATM Interface

1.7.1 UTOPIA Management Interface

Pin Name	Pin No.	I/O	Active Level	Function
UMMD	AG20	O		Management mode select
UMINT_B	AH19	I	L	Interrupt from PHY
UMRD_B	AK21	O	L	Management read enable
UMRDY_B	AJ19	I	L	Management data ready
UMRST_B	AK20	O	L	PHY reset
UMSL_B	AH20	O	L	PHY select
UMWR_B	AF20	O	L	Management write enable
UMAD0 - UMAD11	AG29, AH30, AG28, AH29, AJ30, AK30, AJ29, AH28, AH27, AG26, AK28, AG25	O		PHY address
UMD0 - UMD15	AK27, AJ26, AG24, AK26, AJ25, AH24, AK25, AJ24, AK24, AJ23, AG22, AH22, AK23, AJ22, AK22, AH21	I/O		Management data

1.7.2 UTOPIA Data Interface

Pin Name	Pin No.	I/O	Active Level	Function
CLKUSL0, CLKUSL1	T4, T3	I		UTOPIA clock select (CLKUSL1/0 = L/L: 33 MHz, H/L: 25 MHz, L/H: 16.5 MHz)
UDRCLK	AK11	O		Receive clock
UDRCLV	AH9	I	H	Receive cell available
UDRE_B	AJ8	O	L	Receive enable
UDRSC	AG9	I	H	Receive cell start
UDRAD0 - UDRAD4	AK13, AG13, AF13, AK12, AJ11	O		Receive PHY address
UDRD0 - UDRD7	AG11, AF11, AK10, AJ10, AH10, AK9, AJ9, AK8	I		Receive data
UDTCLK	AK16	O		Transmit clock
UDTCLV	AH11	I	H	Transmit cell available
UDTE_B	AK14	O	L	Transmit enable
UDTSC	AH14	O	H	Transmit cell start position
UDTAD0 - UDTAD4	AG16, AH16, AG15, AF15, AK15	O		Transmit PHY address
UDTD0 - UDTD7	AK19, AG18, AH18, AK18, AH17, AJ17, AK17, AF16	O		Transmit data

1.8 Ethernet Interface

1.8.1 Ethernet Interface (Channel 1)

Pin Name	Pin No.	I/O	Active Level	Function
MIMCLK	AF3	O		MII management clock
MIMD	AG1	I/O		MII management data
MICOL	AH3	I		Collision
MICRS	AF2	I		Carrier sense
MIRCLK	AD3	I		Receive clock (2.5 MHz/25 MHz)
MIRDV	AD5	I		Receive data valid
MIRER	AD4	I		Receive error
MIRD0 - MIRD3	AE1, AD2, AD1, AC2	I		Receive data
MITCLK	AH1	I		Transmit clock (2.5 MHz/25 MHz)
MITE	AF1	O		Transmit enable
MITER	AE3	O		Transmit error
MITD0 - MITD3	AJ1, AH2, AG3, AF4	O		Transmit data

1.8.2 Ethernet Interface (Channel 2)

Pin Name	Pin No.	I/O	Active Level	Function
MI2MCLK	AJ2	O		MII management clock
MI2MD	AH5	I/O		MII management data
MI2COL	AG5	I		Collision
MI2CRS	AG7	I		Carrier sense
MI2RCLK	AK3	I		Receive clock (2.5 MHz/25 MHz)
MI2RDV	AK4	I		Receive data valid
MI2RER	AJ5	I		Receive error
MI2RD0 - MI2RD3	AH4, AJ3, AK2, AK1	I		Receive data
MI2TCLK	AK5	I		Transmit clock (2.5 MHz/25 MHz)
MI2TE	AF7	O		Transmit enable
MI2TER	AH6	O		Transmit error
MI2TD0 - MI2TD3	AK7, AJ7, AK6, AH7	O		Transmit data

1.9 USB Interface

Pin Name	Pin No.	I/O	Active Level	Function
★ USBCLK	E24	I		External USB clock (12 MHz)
USBDM	C23	I/O		USB data(–)
USBDP	B24	I/O		USB data(+)

1.10 UART Interface

Pin Name	Pin No.	I/O	Active Level	Function
★ URCLK	D9	I		UART external clock (18.432 MHz)
URCTS_B	B8	I	L	UART clear to send
URDCD_B	A9	I	L	UART data carrier detect
URDSR_B	A8	I	L	UART data set ready
URDTR_B	A10	O	L	UART data terminal ready
URRTS_B	C10	O	L	UART data request to send
URSDI	B9	I		UART serial data input
URSDO	B10	O		UART serial data output

1.11 Micro Wire Interface

Pin Name	Pin No.	I/O	Active Level	Function
MWCS	C12	O		Micro Wire chip select
MWDI	A12	I		Micro Wire data in
MWDO	B12	O		Micro Wire data out
MWSK	A11	O		Micro Wire sampling clock out

1.12 Parallel Port Interface

Pin Name	Pin No.	I/O	Active Level	Function
POM0 - POM7	E13, D13, C13, B13, C14, B14, A14, E15	O		Parallel port signal output

1.13 Boundary SCAN Interface

Pin Name	Pin No.	I/O	Active Level	Function
JCK	A22	I		B-SCAN clock
JDI	C21	I		B-SCAN input-data
JDO	B22	OZ		B-SCAN output-data
JMS	A23	I		B-SCAN mode select
JRSTB_B	D22	I	L	B-SCAN reset

1.14 I.C. – open

Pin Name	Pin No.	I/O	Active Level	Function
★ IC-OPEN	A19, A20, A28, B16, B17, B19, B26, C18, C20, C24, D18, D20, E18, Y1, AA1, AB1, AB27, AB28, AC28, AC29, AD29, AH12, AJ12	O		Leave open

1.15 I.C.– pull down

Pin Name	Pin No.	I/O	Active Level	Function
IC-PDn	A21, B21, E20, AB4	I		Connect to GND

1.16 I.C. – pull down with resistor

Pin Name	Pin No.	I/O	Active Level	Function
IC-PDnR	A18, C17, C19, D15, AD28, AE27, AE28, AE29, AE30, AF28, AF29, AF30	I/O		Connect to GND via pull-down resistor

1.17 I.C. – pull up

Pin Name	Pin No.	I/O	Active Level	Function
IC-PUp	U3, V3, W1, W3, AB3, AC1, AK29	I		Connect to EVDD

★ 1.18 I.C. – pull up with resistor

Pin Name	Pin No.	I/O	Active Level	Function
IC-PUpR	A17, B18	I/O		Connect to EVDD via pull-up resistor

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

	Parameter	Symbol	Conditions	Rating	Unit
	Supply voltage	IV_{DD}	Internal logic core	−0.5 to +3.6	V
		EV_{DD}	I/O buffer	−0.5 to +4.6	V
	Input/output voltage	V_{I1}/V_{O1}	LVTTL-level pin	−0.5 to +4.6	V
		V_{I2}/V_{O2}	PCI I/O buffer	−0.5 to +4.6	V
		V_{I3}/V_{O3}	USB I/O buffer	−0.5 to +3.6	V
★	Output current	I_{O1}	LVTTL-level pin; I_{OL}= 9 mA	30	mA
★		I_{O2}	PCI I/O buffer	30	mA
		I_{O3}	USB I/O buffer; I_{OL}= 18 mA	55	mA
	Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Supply voltage	IV_{DD}		2.3	2.5	2.7	V
★		EV_{DD}		3.15	3.3	3.45	V
	Low-level input voltage	V_{IL1}	LVTTL-level pin	0		0.8	V
		V_{IL2}	PCI I/O buffer	0		$0.3EV_{DD}$	V
★		V_{IL3}	USB I/O buffer, refer to **(10) USB interface parameters** (Single-end operation)			0.8	V
	High-level input voltage	V_{IH1}	LVTTL-level pin	2.0			V
		V_{IH2}	PCI I/O buffer	$0.5EV_{DD}$		EV_{DD}	V
★		V_{IH3}	USB I/O buffer, refer to **(10) USB interface parameters** (Single-end operation)	2.0			V
★	USB differential input voltage	V_{IDF}	USB I/O buffer, refer to **(10) USB interface parameters** (Differential operation)	0.2			V
	Operating ambient temperature	T_A		0		70	°C

DC Characteristics (IV_{DD} = 2.5 ±0.2 V; EV_{DD} = 3.3 ±0.15 V; T_A = 0 to +70°C)

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
★	Supply current	II_{DD}				1310	mA
★		EI_{DD}				132	mA
	Input leakage current	I_{LI}	V_I = EV_{DD} or GND			±10	μA
	Off state output current	I_{OZ}	V_O = V_{DD} or GND			±10	μA
	Low-level output voltage	V_{OL1}	LVTTL-level pin; I_{OL} = 9 mA			0.4	V
		V_{OL2}	PCI I/O buffer			0.1EV_{DD}	V
★		V_{OL3}	USB I/O buffer, refer to **(10) USB interface parameters**			0.3	V
	High-level output voltage	V_{OH1}	LVTTL-level pin; I_{OL} = 9 mA	2.4			V
		V_{OH2}	PCI I/O buffer	0.1EV_{DD}			V
★		V_{OH3}	USB I/O buffer, refer to **(10) USB interface parameters**	2.8		EV_{DD}	V

★ **Capacitance (T_A = 25°C, V_{DD} = 0 V)**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_I	f_C = 1 MHz,	4		8	pF
Output Capacitance	C_O	Unmeasured pins returned to	4		8	pF
I/O Capacitance	C_{IO}	0 V	4		8	pF

Pin Classifications

Input pins

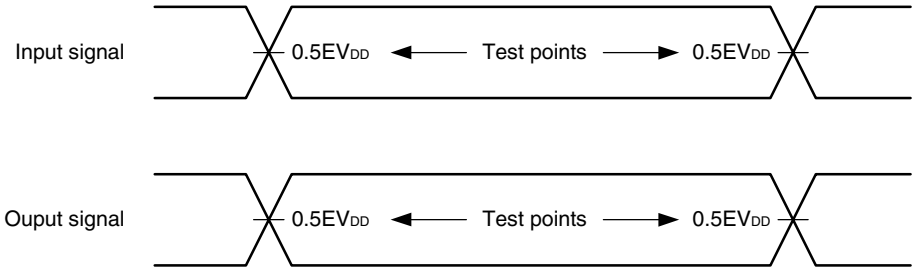
Type		Pin Names	Number of Pins
LVTTL-level pin	V_{I1}, V_{IL1}/V_{IH1}	SCLK, CLKSL, PSMD, PSTBY, PUMD, PUSTBY, BIG, ENDCEN, EXINT_B, EXNMI_B, RMSL[1:0], SMD[31:0], UMINT_B, UMRDY_B, UMD[15:0], UDRCLV, UDRSC, UDRD[7:0], UDTCLV, USBCLK, URCLK, URSDI, MWDI, URCTS_B, URDCD_B, URDSR_B, JCK, JDI, JMS, JRSTB_B, MIRCLK, MIMD, MICOL, MICRS, MIRDV, MIRER, MIRD[3:0], MITCLK, MI2RCLK, MI2MD, MI2COL, MI2CRS, MI2RDV, MI2RER, MI2RD[3:0], MI2TCLK	106
PCI I/O buffer	V_{I2}, V_{IL2}/V_{IH2}	PARBN, PMODE, PSERI_B, PHINT_B, PRQI[3:0]_B, PAD[31:0], PCBE[3:0]_B, PFRA_B, PDSEL_B, PTRY_B, PIRY_B, PSTP_B, PAR, PER_B, PIDSEL, RST_B, PGTI_B, PSCLK	55
USB I/O buffer	V_{I3}, V_{IL3}/V_{IH3}, V_{IDF}	USBDP, USBDM	2

Output pins

Type			Pin Names	Number of Pins
LVTTL-level pins	I_{O1}	V_{O1}, V_{OL1}/V_{OH1}	SDCLK0, SDCLK1, SDCKE0, SDCKE1, SDCS_B, SDRAS_B, SDCAS_B, SDWE_B, SRMCS_B, SRMOE_B, SMA[20:0], SMD[31:0], UMMD, UMRD_B, UMRST_B, UMSL_B, UMWR_B, UMAD[11:0], UMD[15:0], UDRCLK, UDRE_B, UDRAD[4:0], UDTCLK, UDTE_B, UDTSC, UDTAD[4:0], UDTD[7:0], URSDO, URDTR_B, URRTS_B, MWSK, MWCS, MWDO, POM[7:0], JDO, MIMCLK, MIMD, MITE, MITER, MITD[3:0], MI2MCLK, MI2MD, MI2TE, MI2TER, MI2TD[3:0]	150
PCI I/O buffer	I_{O2}	V_{O2}, V_{OL2}/V_{OH2}	PRSTO_B, PGTO[3:0]_B, PAD[31:0], PCBE[3:0]_B, PFRA_B, PDSEL_B, PTRY_B, PIRY_B, PSTP_B, PAR, PER_B, PINT_B, PSERO_B, PME_B, PRQO_B	52
USB I/O buffer	I_{O3}	V_{O3}, V_{OL3}/V_{OH3}	USBDP, USBDM	2

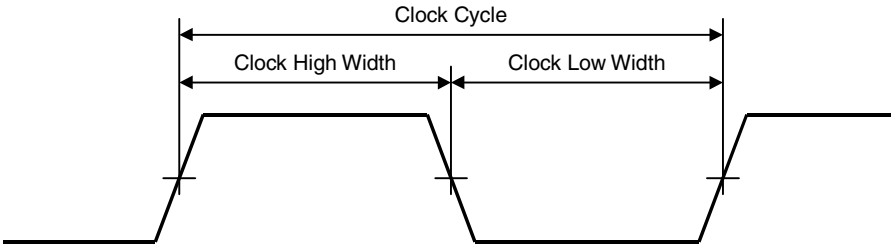
AC Characteristics (IV_{DD} = 2.5 ±0.2 V; EV_{DD} = 3.3 ±0.15 V; T_A = 0 to +70°C)

★ **(1) AC test waveform**



(2) Clock parameters

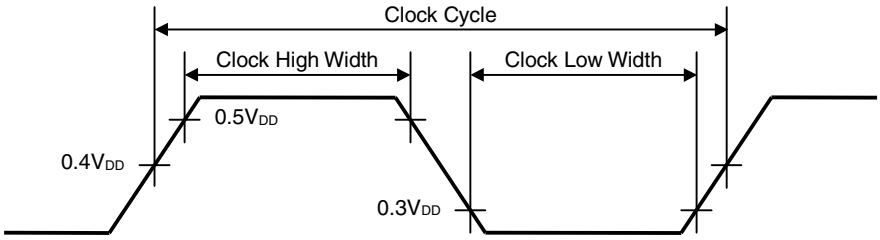
Clock timing (except PCI clock)



Clock input parameters (except PCI clock)

	Parameter	Symbol	Conditions	Min.	Max.	Unit
	SCLK input cycle	t_{CYSCK}		30.00	33.00	ns
	SCLK input high width	t_{WHSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
	SCLK input low width	t_{WLSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
	MITCLK input cycle	t_{CYMTK}		40.00	400.00	ns
	MITCLK input high width	t_{WHMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
	MITCLK input low width	t_{WLMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
	MIRCLK input cycle	t_{CYMRK}		40.00	400.00	ns
	MIRCLK input high width	t_{WHMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
	MIRCLK input low width	t_{WLMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
	MI2TCLK input cycle	t_{CY2TK}		40.00	400.00	ns
	MI2TCLK input high width	t_{WH2TK}		0.4 × t_{CY2TK}	0.6 × t_{CY2TK}	ns
	MI2TCLK input low width	t_{WL2TK}		0.4 × t_{CY2TK}	0.6 × t_{CY2TK}	ns
	MI2RCLK input cycle	t_{CY2RK}		40.00	400.00	ns
	MI2RCLK input high width	t_{WH2RK}		0.4 × t_{CY2RK}	0.6 × t_{CY2RK}	ns
	MI2RCLK input low width	t_{WL2RK}		0.4 × t_{CY2RK}	0.6 × t_{CY2RK}	ns
	USBCLK input cycle	t_{CYUBK}		83.1	84.6	ns
	USBCLK input high width	t_{WHUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
	USBCLK input low width	t_{WLUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
★	JCK input cycle	t_{CYJCK}		150.00	1000.00	ns
	JCK input high width	t_{WHJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns
	JCK input low width	t_{WLJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns

★ **Clock timing (PCI clock)**



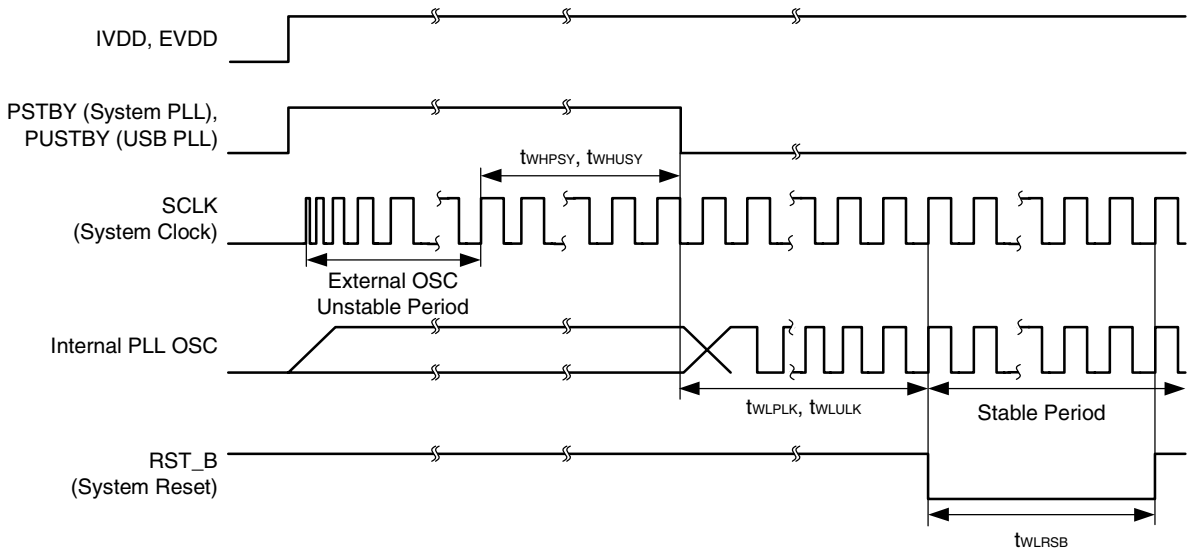
★ **Clock input parameters (PCI clock)**

Parameter	Symbol	Conditions	Min.	Max.	Unit
PSCLK input cycle	t_{CYpCK}		30.00	60.00	ns
PSCLK input high width	t_{WHpCK}		0.4 × t_{CYSCK}		ns
PSCLK input low width	t_{WLpCK}		0.4 × t_{CYSCK}		ns

Clock output parameters

Parameter	Symbol	Conditions	Min.	Max.	Unit
SDCLK0 output cycle	t_{CYSK0}	Load 50 pF	10.00	15.00	ns
SDCLK0 output high width	t_{WHSK0}	Load 50 pF	0.4 × t_{CYSK0}	0.6 × t_{CYSK0}	ns
SDCLK0 output low width	t_{WLSK0}	Load 50 pF	0.4 × t_{CYSK0}	0.6 × t_{CYSK0}	ns
SDCLK1 output cycle	t_{CYSK1}	Load 50 pF	10.00	15.00	ns
SDCLK1 output high width	t_{WHSK1}	Load 50 pF	0.4 × t_{CYSK1}	0.6 × t_{CYSK1}	ns
SDCLK1 output low width	t_{WLSK1}	Load 50 pF	0.4 × t_{CYSK1}	0.6 × t_{CYSK1}	ns
UDTCLK output cycle	t_{CYUTK}	Load 50 pF	30.00/40.00/ 60.00		ns
UDTCLK output high width	t_{WHUTK}	Load 50 pF	0.4 × t_{CYUTK}		ns
UDTCLK output low width	t_{WLUTK}	Load 50 pF	0.4 × t_{CYUTK}		ns
UDRCLK output cycle	t_{CYURK}	Load 50 pF	30.00/40.00/ 60.00		ns
UDRCLK output high width	t_{WHURK}	Load 50 pF	0.4 × t_{CYURK}		ns
UDRCLK output low width	t_{WLURK}	Load 50 pF	0.4 × t_{CYURK}		ns
MIMCLK output cycle	t_{CYMCK}	Load 50 pF	420.00		ns
MIMCLK output high width	t_{WHMCK}	Load 50 pF	0.4 × t_{CYMCK}		ns
MIMCLK output low width	t_{WLMCK}	Load 50 pF	0.4 × t_{CYMCK}		ns
MI2MCLK output cycle	t_{CYM2K}	Load 50 pF	420.00		ns
MI2MCLK output high width	t_{WHM2K}	Load 50 pF	0.4 × t_{CYM2K}		ns
MI2MCLK output low width	t_{WLM2K}	Load 50 pF	0.4 × t_{CYM2K}		ns

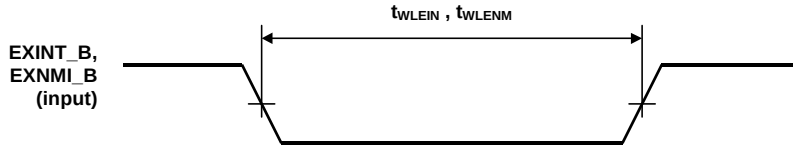
★ **(3) Reset, PLL parameters**



Parameter	Symbol	Conditions	Min.	Max.	Unit
RST_B Input Low Level Width	t_{WLRSB}		240	4000 Note	ns
PSTBY Hold High Level Width	t_{WHPSY}		1		μs
PSTBY Lookup Time	t_{WLPLK}	Load 50 pF		1000	μs
PUSTBY Hold High Level Width	t_{WHUSY}		1		μs
PUSTBY Lookup Time	t_{WLULK}	Load 50 pF		1000	μs

Note If RST_B is applied longer, operation of the μPD98502 will start anyhow. Therefore it shall be made sure, that other logic is also out of RESET state after 4 μs, even if RST_B is applied for longer period.

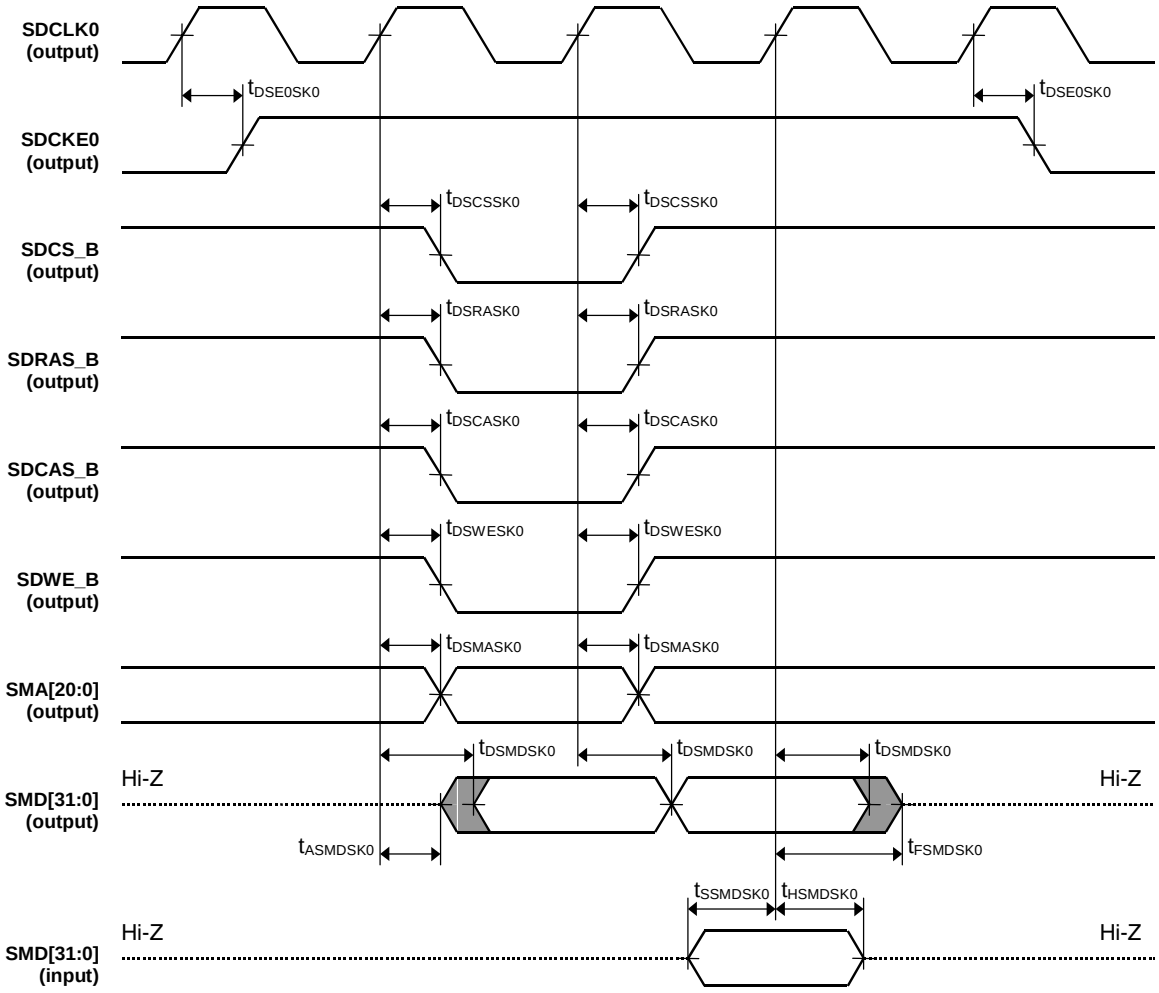
(4) Interrupt interface parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
EXINT_B input low width	t_{WLEIN}		$4 \times t_{CYSK0/1}$		ns
EXNMI_B input low width	t_{WLENM}		$4 \times t_{CYSK0/1}$		ns

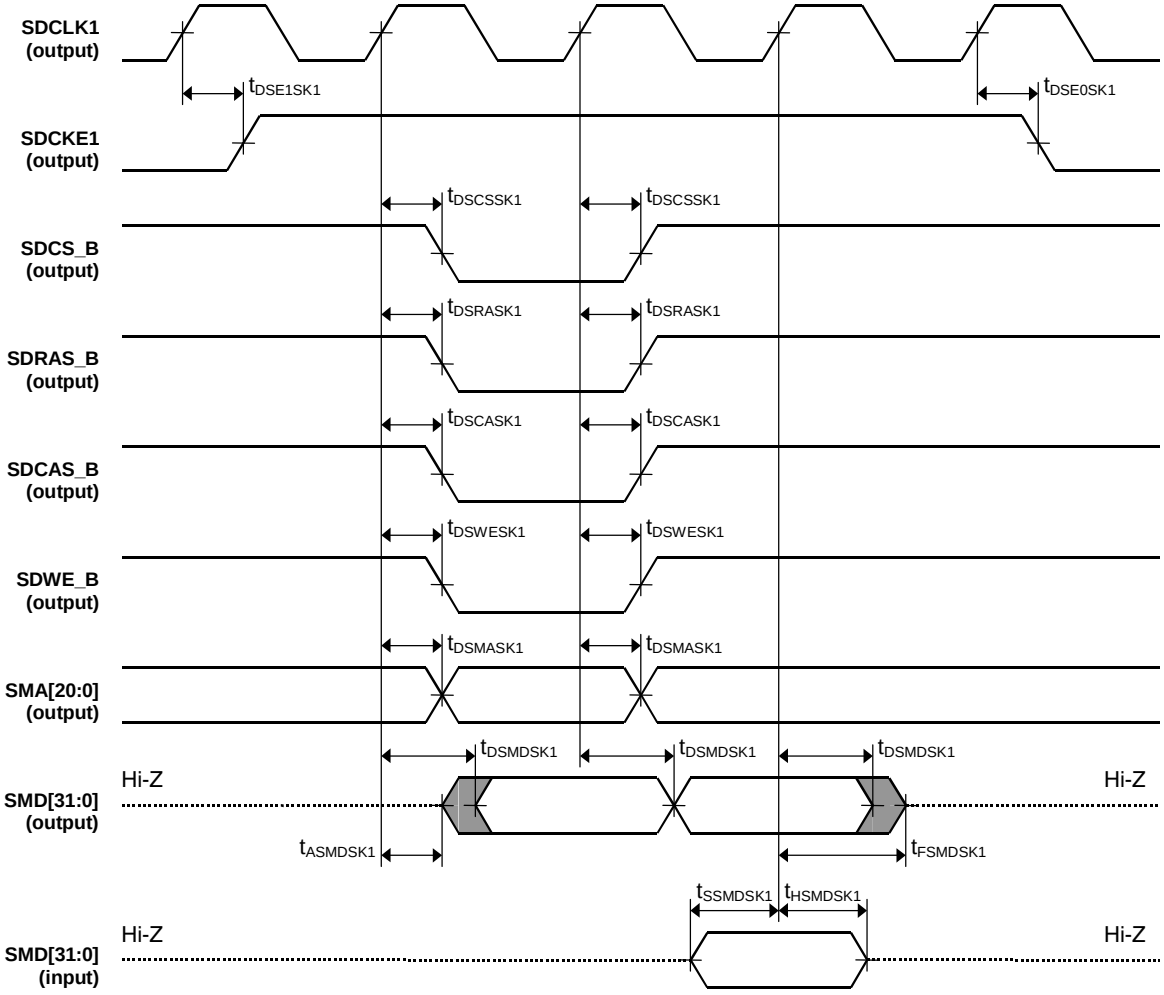
(5) Memory interface parameters

(a) SDCLK0 memory interface parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
SDCKE0 output delay from SDCLK0	$t_{DSE0SK0}$	Load 50 pF	1.0	8.0	ns
SDCS_B output delay from SDCLK0	$t_{DSCSSK0}$	Load 50 pF	1.0	8.0	ns
SDRAS_B output delay from SDCLK0	$t_{DSRASK0}$	Load 50 pF	1.0	8.0	ns
SDCAS_B output delay from SDCLK0	$t_{DSCASK0}$	Load 50 pF	1.0	8.0	ns
SDWE_B output delay from SDCLK0	$t_{DSWESK0}$	Load 50 pF	1.0	8.0	ns
SMA[20:0] output delay from SDCLK0	$t_{DSMASK0}$	Load 50 pF	1.0	8.0	ns
SMD[31:0] output floating to active delay from SDCLK0	$t_{ASMDSK0}$	Load 50 pF	1.0		ns
SMD[31:0] output delay from SDCLK0	$t_{DSMDSK0}$	Load 50 pF	1.0	8.0	ns
SMD[31:0] output active to floating delay from SDCLK0	$t_{FSMDSK0}$	Load 50 pF		8.0	ns
SMD[31:0] input setup to SDCLK0	$t_{SSMDSK0}$		4.0		ns
SMD[31:0] input hold from SDCLK0	$t_{HSMDSK0}$		1.00		ns

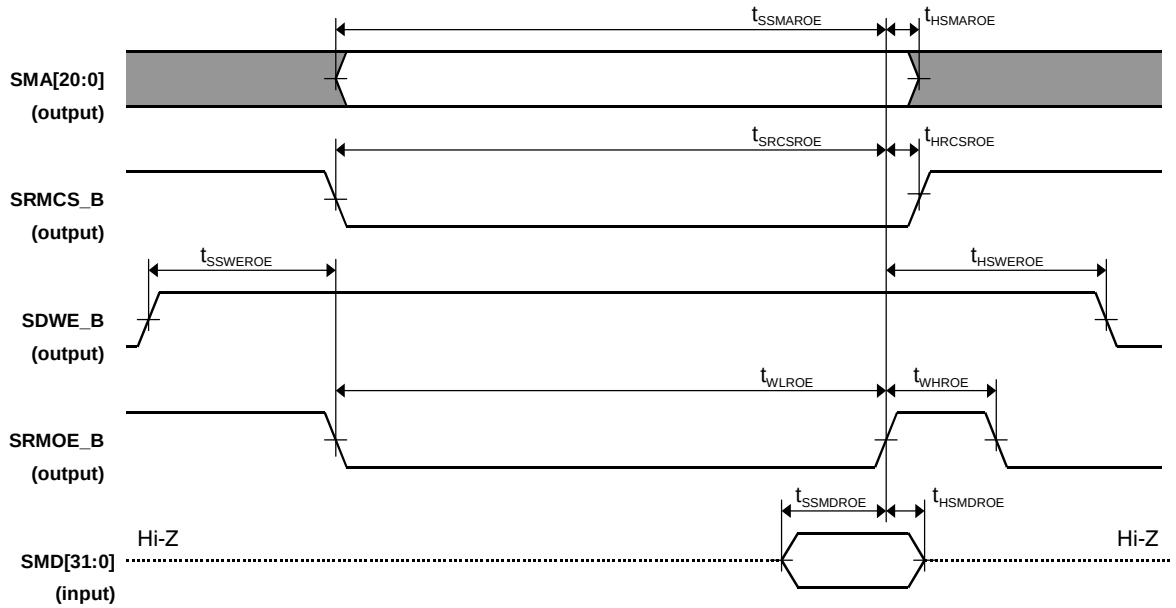
(b) SDCLK1 memory interface parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
SDCKE1 output delay from SDCLK1	$t_{DSE1SK1}$	Load 50 pF	1.0	8.0	ns
SDCS_B output delay from SDCLK1	$t_{DSCSSK1}$	Load 50 pF	1.0	8.0	ns
SDRAS_B output delay from SDCLK1	$t_{DSRASK1}$	Load 50 pF	1.0	8.0	ns
SDCAS_B output delay from SDCLK1	$t_{DSCASK1}$	Load 50 pF	1.0	8.0	ns
SDWE_B output delay from SDCLK1	$t_{DSWESK1}$	Load 50 pF	1.0	8.0	ns
SMA[20:0] output delay from SDCLK1	$t_{DSMASK1}$	Load 50 pF	1.0	8.0	ns
SMD[31:0] output floating to active delay from SDCLK1	$t_{ASMDSK1}$	Load 50 pF	1.0		ns
SMD[31:0] output delay from SDCLK1	$t_{DSMDSK1}$	Load 50 pF	1.0	8.0	ns
SMD[31:0] output active to floating delay from SDCLK1	$t_{FSMDSK1}$	Load 50 pF		8.0	ns
SMD[31:0] input setup to SDCLK1	$t_{SSMDSK1}$		4.0		ns
SMD[31:0] input hold from SDCLK1	$t_{HSMDSK1}$		1.0		ns

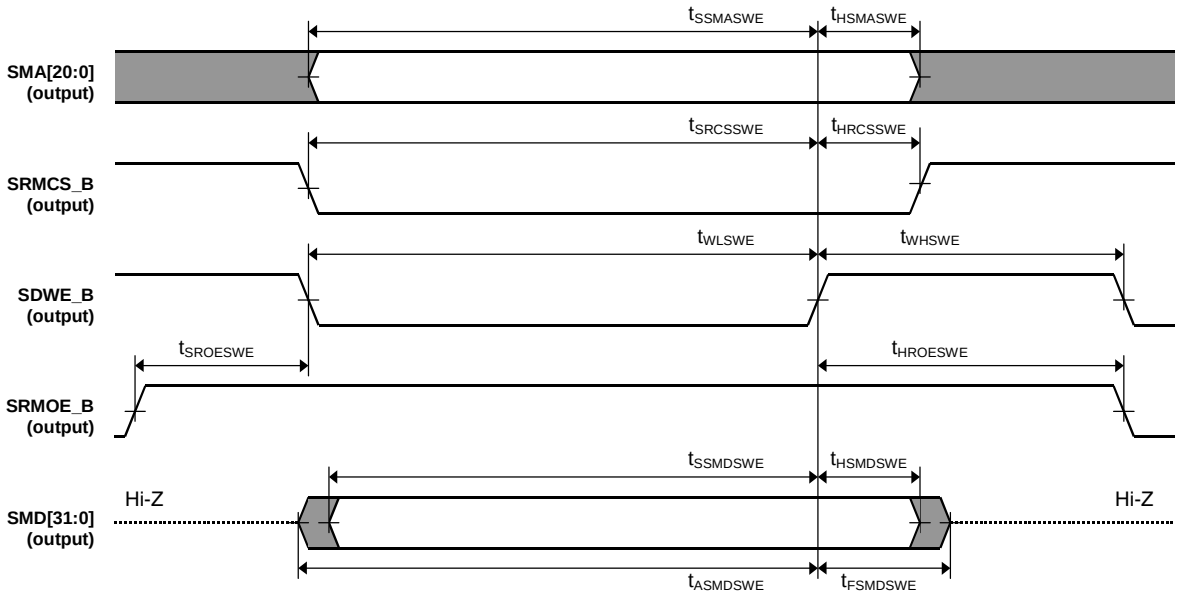
(6) Flash ROM interface parameters

(a) Flash ROM interface read cycle parameters



	Parameter	Symbol	Conditions	Min.	Max.	Unit
★	SMA[20:0] setup to SRMOE_B	$t_{SSMAROE}$	Load 50 pF	$5 \times t_{CYSK0/1} - 8$		ns
★	SMA[20:0] hold from SRMOE_B	$t_{HSMAROE}$	Load 50 pF		$t_{CYSK0/1} - 8$	ns
★	SRMCS_B setup to SRMOE_B	$t_{SRCSROE}$	Load 50 pF	$5 \times t_{CYSK0/1} - 8$		ns
★	SRMCS_B hold from SRMOE_B	$t_{HRCSROE}$	Load 50 pF		5	ns
★	SDWE_B setup time to SRMOE_B	$t_{SSWEROE}$	Load 50 pF	$2 \times t_{CYSK0/1} - 8$		ns
★	SDWE_B hold time from SRMOE_B	$t_{HSWEROE}$	Load 50 pF	$4 \times t_{CYSK0/1} - 8$		ns
★	SRMOE_B low pulse width	t_{WLROE}	Load 50 pF	$5 \times t_{CYSK0/1} - 8$		ns
★	SRMOE_B high pulse width	t_{WHROE}	Load 50 pF	$1 \times t_{CYSK0/1} - 8$		ns
	SMD[31:0] setup to SRMOE_B	$t_{SSMDROE}$		10		ns
	SMD[31:0] hold from SRMOE_B	$t_{HSMDROE}$		0		ns

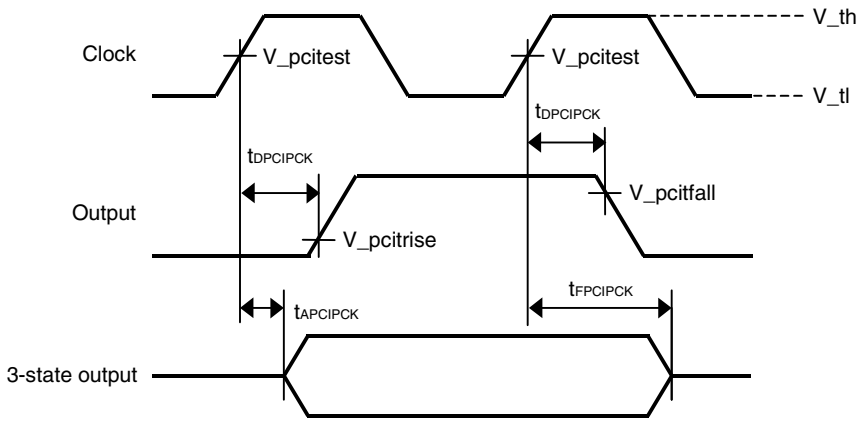
(b) Flash ROM interface write cycle parameters



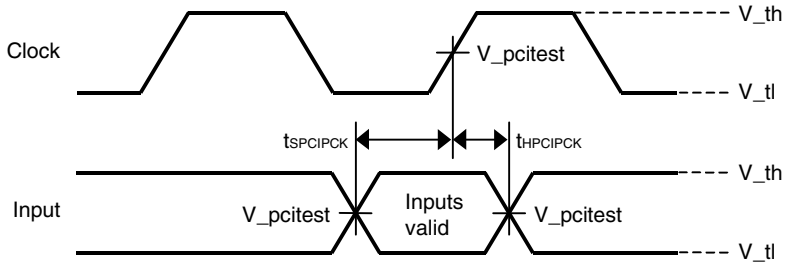
	Parameter	Symbol	Conditions	Min.	Max.	Unit
	SMA[20:0] setup to SDWE_B	$t_{SSMASWE}$	Load 50 pF	$4 \times t_{CYSK0/1} - 8$		ns
★	SMA[20:0] hold from SDWE_B	$t_{HSMASWE}$	Load 50 pF	2.0		ns
	SRMCS_B setup to SDWE_B	$t_{SRCSSWE}$	Load 50 pF	$4 \times t_{CYSK0/1} - 8$		ns
★	SRMCS_B hold from SDWE_B	$t_{HRCSSWE}$	Load 50 pF	2.0		ns
	SRMOE_B setup time to SDWE_B	$t_{SROESWE}$	Load 50 pF	$4 \times t_{CYSK0/1} - 8$		ns
	SRMOE_B hold time from SDWE_B	$t_{HROESWE}$	Load 50 pF	$2 \times t_{CYSK0/1} - 8$		ns
	SDWE_B low pulse width	t_{WLSWE}	Load 50 pF	$3 \times t_{CYSK0/1} - 8$		ns
	SDWE_B high pulse width	t_{WHSWE}	Load 50 pF	$7 \times t_{CYSK0/1} - 8$		ns
	SMD[31:0] setup to SDWE_B	$t_{SSMDSWE}$	Load 50 pF	$4 \times t_{CYSK0/1} - 8$		ns
	SMD[31:0] hold from SDWE_B	$t_{HSMDSWE}$	Load 50 pF		$1 \times t_{CYSK0/1} + 8$	ns
	SMD[31:0] output Hi-Z to valid delay	$t_{ASMDSWE}$	Load 50 pF	$4 \times t_{CYSK0/1} - 8$		ns
	SMD[31:0] output valid to Hi-Z delay	$t_{FSMDSWE}$	Load 50 pF		$1 \times t_{CYSK0/1} + 8$	ns

(7) PCI interface parameters

Output timing measurement conditions



Input timing measurement conditions



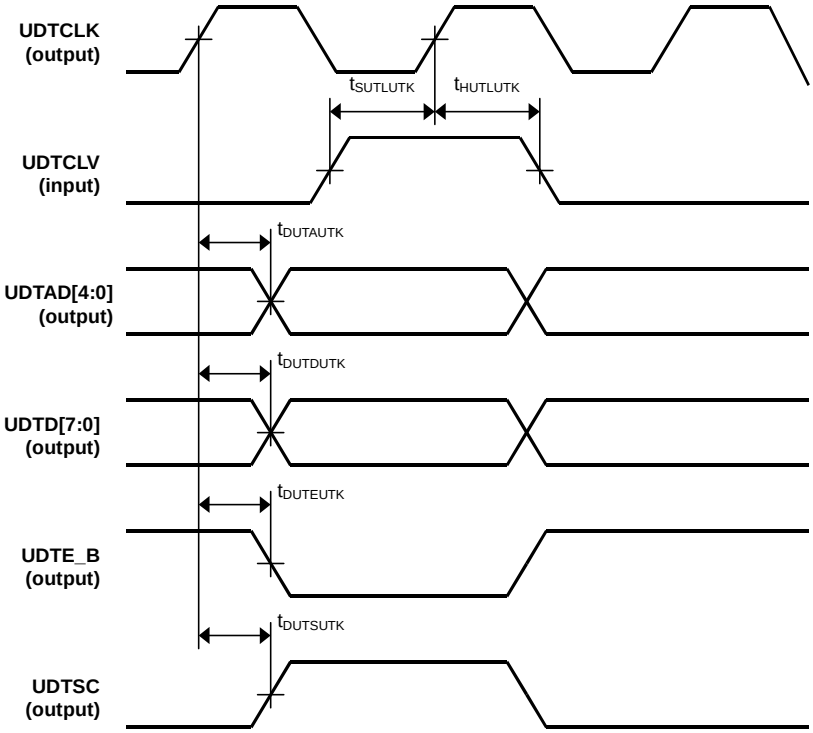
Symbol	Voltage Level	Unit
V_th	$0.6EV_{DD}$	V
V_tl	$0.2EV_{DD}$	V
V_pcitest	$0.4EV_{DD}$	V
V_pcitrise	$0.285EV_{DD}$	V
V_pcitfall	$0.615EV_{DD}$	V

Parameter	Symbol	Conditions	Min.	Max.	Unit
PCI output delay	$t_{DPCIPCK}$	Load 10 pF	2	12	ns
PCI active delay	$t_{APCIPCK}$	Load 10 pF	2		ns
PCI floating delay	$t_{FPCIPCK}$	Load 10 pF		28	ns
PCI setup time	$t_{SPCIPCK}$		7		ns
PCI hold time	$t_{HPCIPCK}$		0		ns

(8) ATM interface parameters

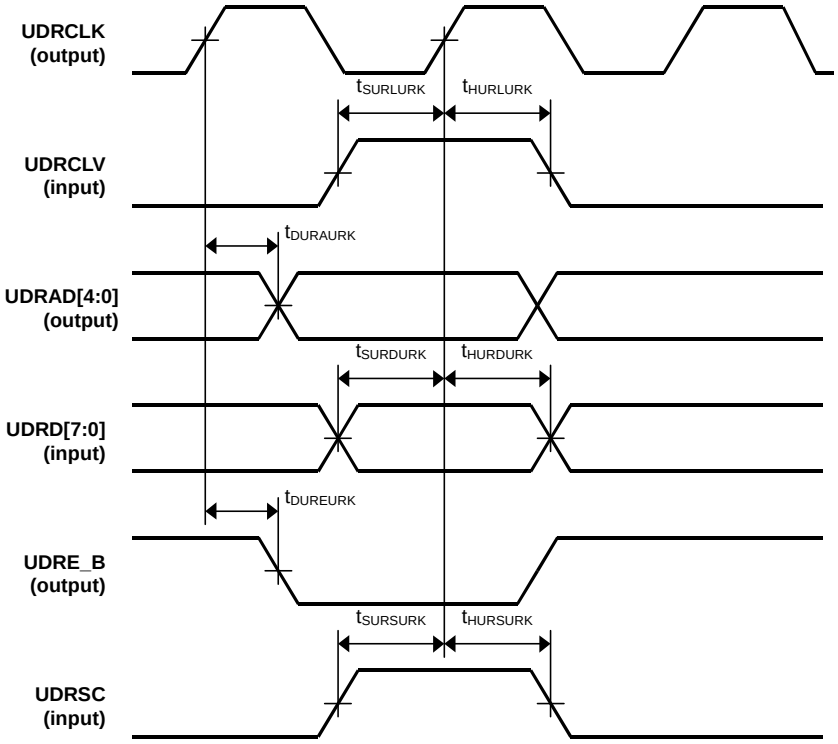
(a) UTOPIA2 interface parameters

Data transmission parameters



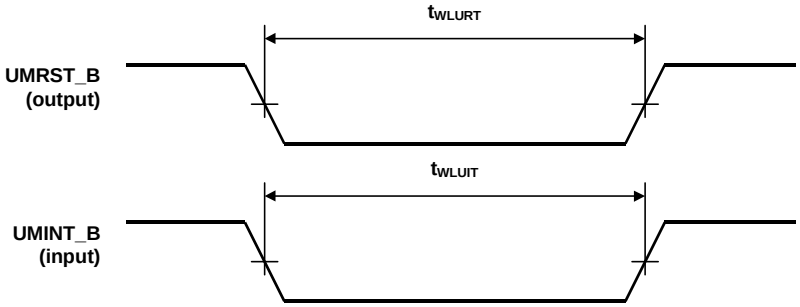
Parameter	Symbol	Conditions	Min.	Max.	Unit
UDTCLV setup time	$t_{SUTLUTK}$		8		ns
UDTCLV hold time	$t_{HUTLUTK}$		1		ns
UDTAD[4:0] output delay	$t_{DUTAUTK}$	Load 50 pF	1	15	ns
UDTD[7:0] output delay	$t_{DUTDUTK}$	Load 50 pF	1	15	ns
UDTE_B output delay	$t_{DUTEUTK}$	Load 50 pF	1	15	ns
UDTSC output delay	$t_{DUTSUTK}$	Load 50 pF	1	15	ns

Data reception parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
UDRCLV setup time	$t_{SURLURK}$		8		ns
UDRCLV hold time	$t_{HURLURK}$		1		ns
UDRAD[4:0] output delay	$t_{DURAURK}$	Load 50 pF	1	15	ns
UDRD[7:0] setup time	$t_{SURDURK}$		8		ns
UDRD[7:0] hold time	$t_{HURDURK}$		1		ns
UDRE_B output delay	$t_{DUREURK}$	Load 50 pF	1	15	ns
UDRSC setup time	$t_{SURSURK}$		8		ns
UDRSC hold time	$t_{HURSURK}$		1		ns

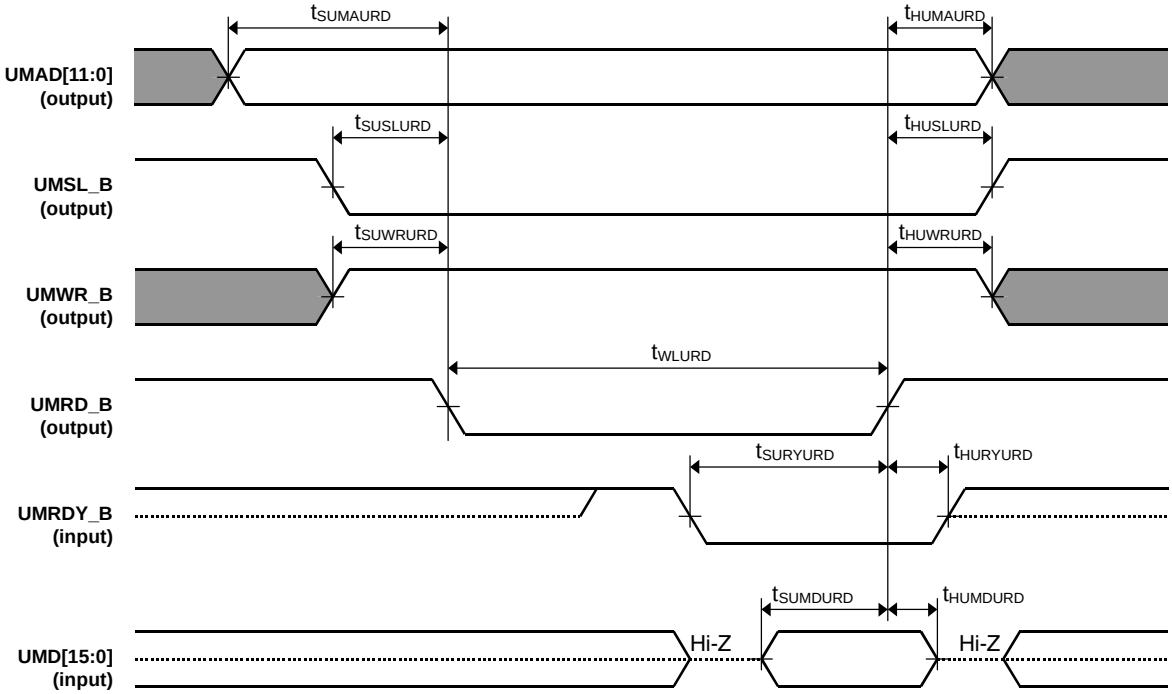
(b) UTOPIA management interface parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
UMRST_B low pulse width	t_{WLURT}		$3 \times t_{CYSCK}$		ns
UMINT_B low pulse width	t_{WLUIT}		$3 \times t_{CYSCK}$		ns

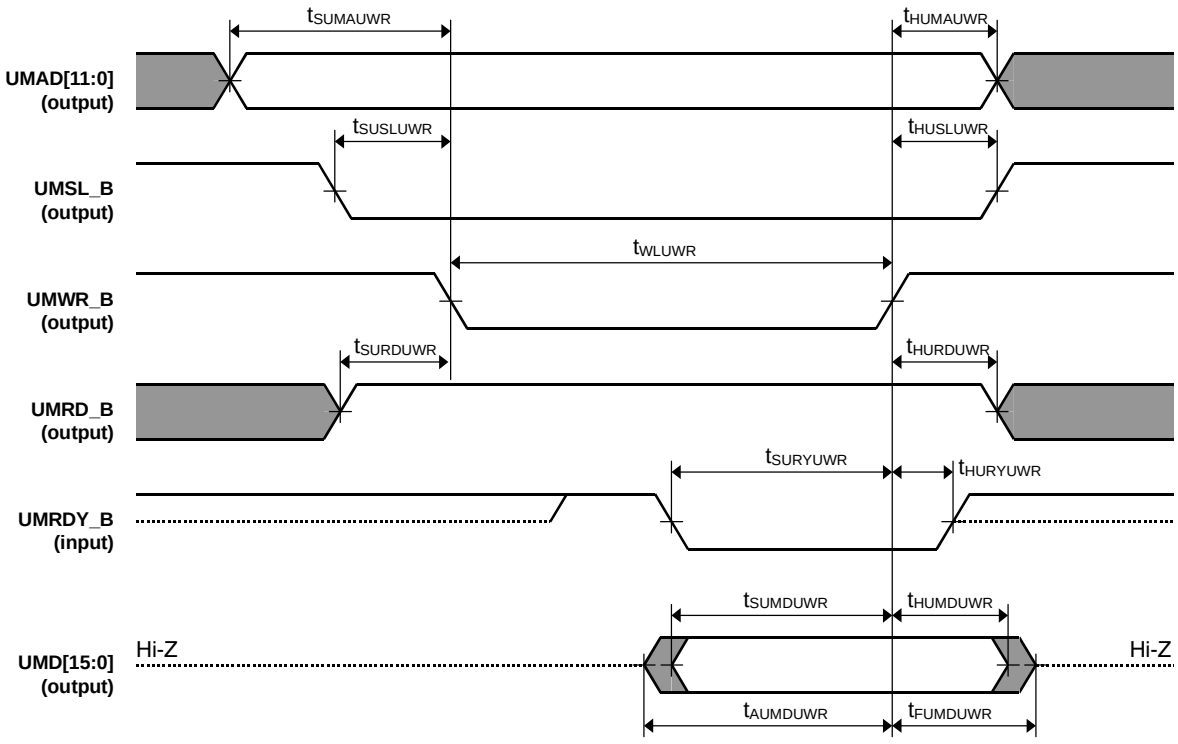
(c) Intel Mode

Read cycle parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
UMAD[11:0] setup to UMRD_B	$t_{SUMAURD}$	Load 50 pF	10		ns
UMAD[11:0] hold from UMRD_B	$t_{HUMAURD}$	Load 50 pF	4		ns
UMSL_B setup to UMRD_B	$t_{SUSLURD}$	Load 50 pF	5		ns
UMSL_B hold from UMRD_B	$t_{HUSLURD}$	Load 50 pF	0		ns
UMWR_B setup to UMRD_B	$t_{SUWRURD}$	Load 50 pF	5		ns
UMWR_B hold from UMRD_B	$t_{HUWRURD}$	Load 50 pF	0		ns
UMRD_B low pulse width	t_{WLURD}	Load 50 pF	50		ns
UMRDY_B setup to UMRD_B	$t_{SURYURD}$		25		ns
UMRDY_B hold from UMRD_B	$t_{HURYURD}$		10		ns
UMD[15:0] setup to UMRD_B	$t_{SUMDURD}$		10		ns
UMD[15:0] hold from UMRD_B	$t_{HUMDURD}$		15		ns

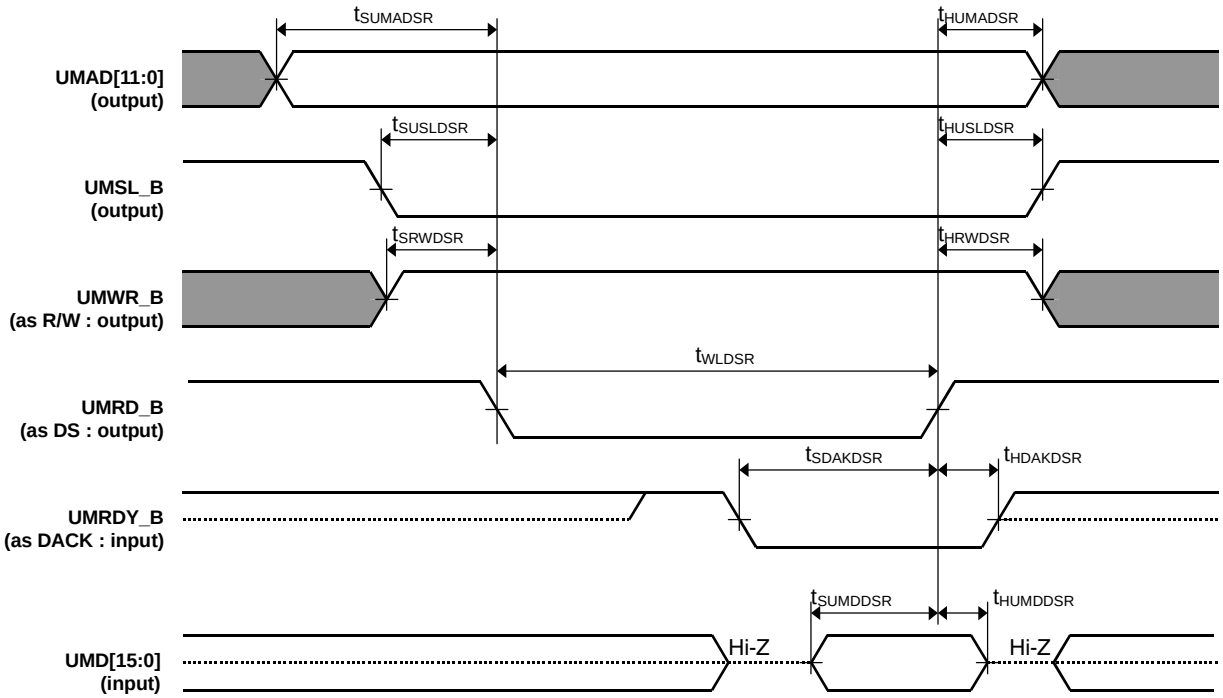
Write cycle parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
UMAD[11:0] setup to UMWR_B	$t_{SUMAUWR}$	Load 50 pF	10		ns
UMAD[11:0] hold from UMWR_B	$t_{HUMAUWR}$	Load 50 pF	4		ns
UMSL_B setup to UMWR_B	$t_{SUSLUWR}$	Load 50 pF	5		ns
UMSL_B hold from UMWR_B	$t_{HUSLUWR}$	Load 50 pF	0		ns
UMRD_B setup to UMWR_B	$t_{SURDUWR}$	Load 50 pF	5		ns
UMRD_B hold from UMWR_B	$t_{HURDUWR}$	Load 50 pF	0		ns
UMWR_B low pulse width	t_{WLUWR}	Load 50 pF	50		ns
UMRDY_B setup to UMWR_B	$t_{SURYUWR}$		25		ns
UMRDY_B hold from UMWR_B	$t_{HURYUWR}$		10		ns
UMD[15:0] setup to UMWR_B	$t_{SUMDUWR}$		15		ns
UMD[15:0] hold from UMWR_B	$t_{HUMDUWR}$		4		ns
UMD[15:0] active time to UMWR_B	$t_{AUMDUWR}$	Load 30 pF	15		ns
UMD[15:0] floating time from UMWR_B	$t_{FUMDUWR}$	Load 30 pF	4		ns

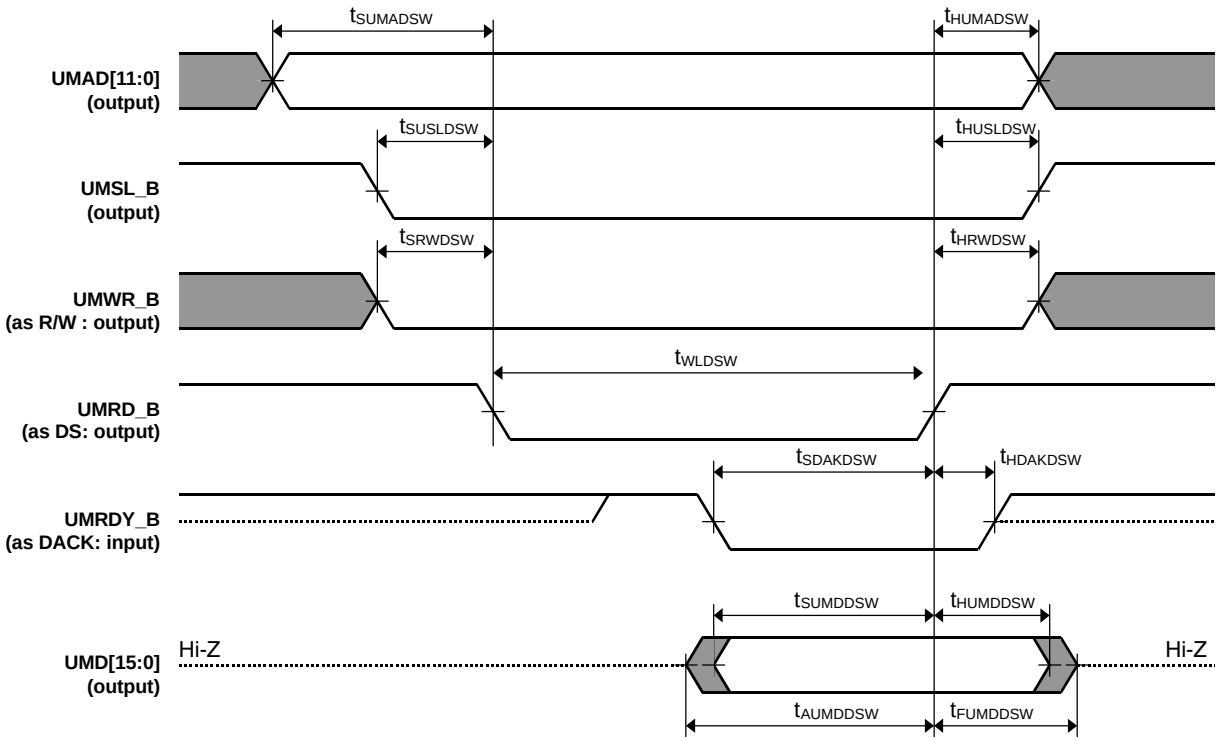
(d) Motorola Mode

Read cycle parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
UMAD[11:0] setup to DS	$t_{SUMADSR}$	Load 50 pF	10		ns
UMAD[11:0] hold from DS	$t_{HUMADSR}$	Load 50 pF	4		ns
UMSL_B setup to DS	$t_{SUSLDSR}$	Load 50 pF	5		ns
UMSL_B hold from DS	$t_{HUSLDSR}$	Load 50 pF	0		ns
R/W setup to DS	t_{SRWDSR}	Load 50 pF	5		ns
R/W hold from DS	t_{HRWDSR}	Load 50 pF	0		ns
DS low pulse width	t_{WLDSR}	Load 50 pF	50		ns
DACK setup to DS	$t_{SDAKDSR}$		25		ns
DACK hold from DS	$t_{HDAKDSR}$		10		ns
UMD[15:0] setup to DS	$t_{SUMDDSR}$		10		ns
UMD[15:0] hold from DS	$t_{HUMDDSR}$		15		ns

Write cycle parameters

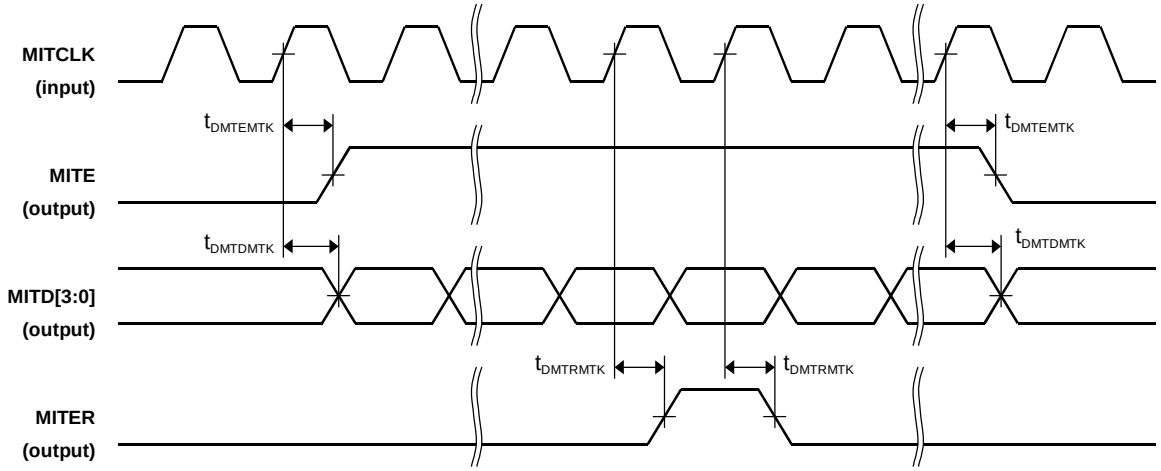


Parameter	Symbol	Conditions	Min.	Max.	Unit
UMAD[11:0] setup to DS	$t_{SUMADSW}$	Load 50 pF	10		ns
UMAD[11:0] hold from DS	$t_{HUMADSW}$	Load 50 pF	4		ns
UMSL_B setup to DS	$t_{SUSLDSW}$	Load 50 pF	5		ns
UMSL_B hold from DS	$t_{HUSLDSW}$	Load 50 pF	0		ns
R/W setup to DS	t_{SRWDSW}	Load 50 pF	5		ns
R/W hold from DS	t_{HRWDSW}	Load 50 pF	0		ns
DS low pulse width	t_{WLDSW}	Load 50 pF	50		ns
DACK setup to DS	$t_{SDAKDSW}$		25		ns
DACK hold from DS	$t_{HDAKDSW}$		10		ns
UMD[15:0] setup to DS	$t_{SUMDDSW}$		15		ns
UMD[15:0] hold from DS	$t_{HUMDDSW}$		4		ns
UMD[15:0] active time to DS	$t_{AUMDDSW}$	Load 30 pF	15		ns
UMD[15:0] floating time from DS	$t_{FUMDDSW}$	Load 30 pF	4		ns

(9) Ethernet interface parameters

(a) Ethernet interface 1

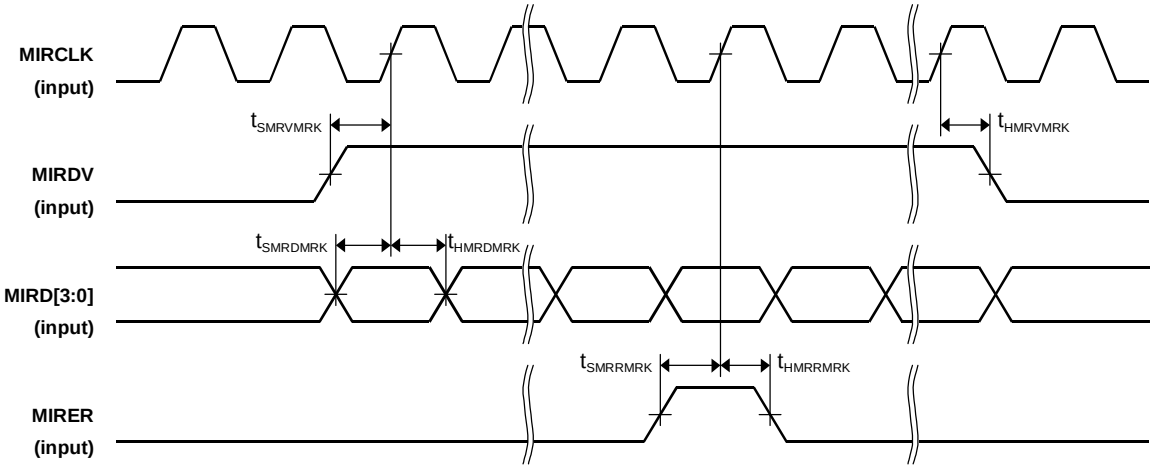
MII data transmission parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
MITE output delay	$t_{DMTEMTK}$	Load 50 pF	0	20 Note	ns
MITD[3:0] output delay	$t_{DMTDMTK}$	Load 50 pF	0	20 Note	ns
MITER output delay	$t_{DMTRMTK}$	Load 50 pF	0	20 Note	ns

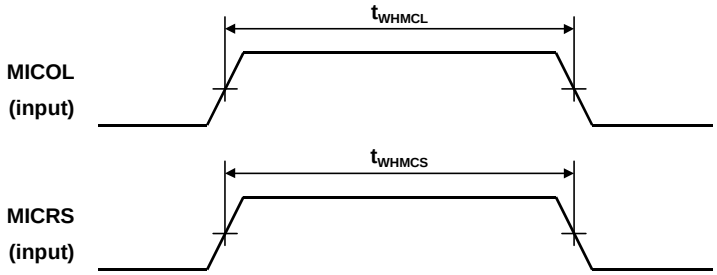
Note In the MII specification, maximum output delay is specified as 25 ns.

MII data reception parameters



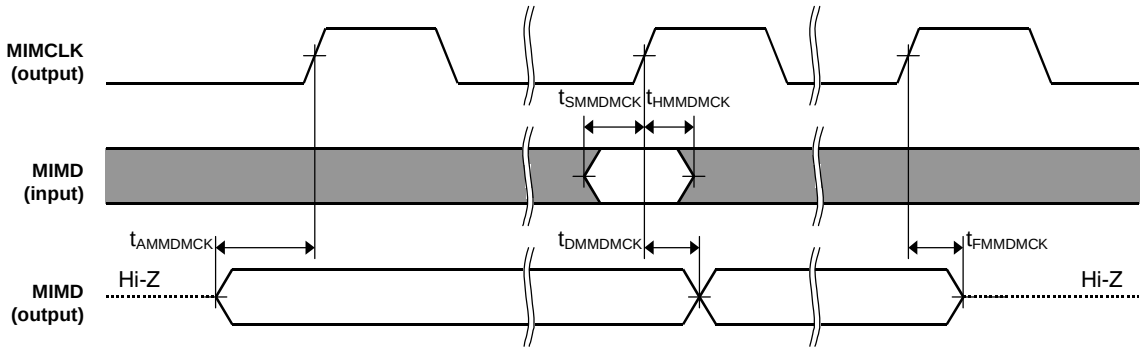
Parameter	Symbol	Conditions	Min.	Max.	Unit
MIRDV setup time	$t_{SMRVMRK}$		10		ns
MIRDV hold time	$t_{HMRVMRK}$		10		ns
MIRD[3:0] setup time	$t_{SMRDMRK}$		10		ns
MIRD[3:0] hold time	$t_{HMRDMRK}$		10		ns
MIRER setup time	$t_{SMRRMRK}$		10		ns
MIRER hold time	$t_{HMRRMRK}$		10		ns

MII interface signal parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
MICOL high pulse width	t_{WHMCL}		$2 \times t_{CYMTK}$		ns
MICRS high pulse width	t_{WHMCS}		$2 \times t_{CYMTK}$		ns

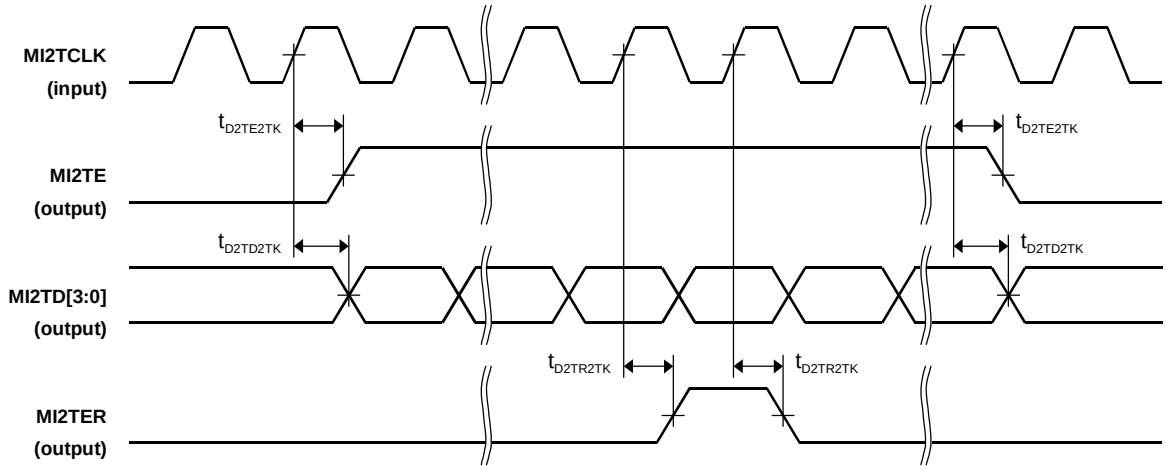
MII management interface parameters



	Parameter	Symbol	Conditions	Min.	Max.	Unit
	MIMD setup to MIMCLK	$t_{SMMDMCK}$		20		ns
	MIMD hold from MIMCLK	$t_{HMMDMCK}$		0		ns
	MIMD active delay from MIMCLK	$t_{AMMDMCK}$	Load 50 pF	10		ns
★	MIMD output delay from MIMCLK	$t_{DMMDMCK}$	Load 50 pF	10	30	ns
★	MIMD floating delay from MIMCLK	$t_{FMMDMCK}$	Load 50 pF	10		ns

(b) Ethernet Interface 2

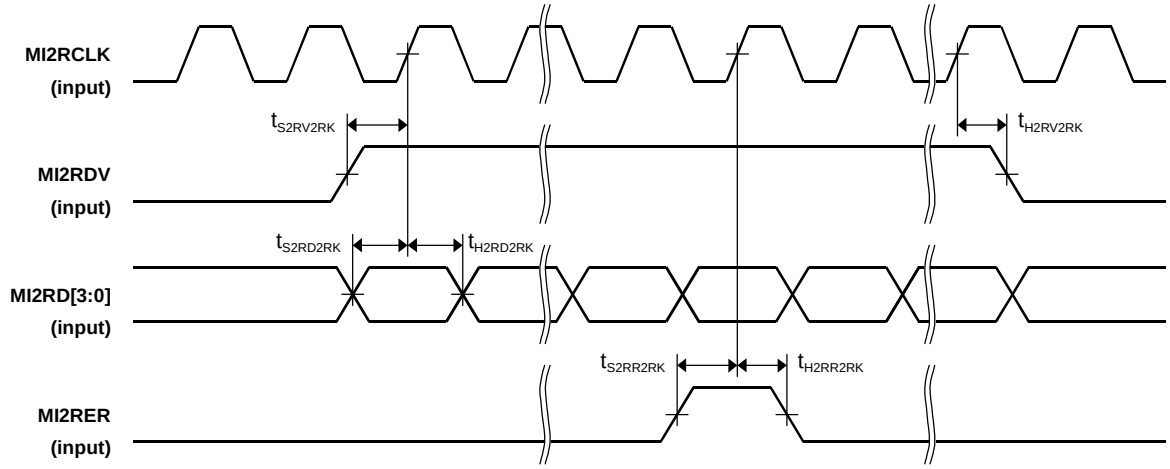
MII data transmission parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
MI2TE output delay	$t_{D2TE2TK}$	Load 50 pF	0	20 Note	ns
MI2TD[3:0] output delay	$t_{D2TD2TK}$	Load 50 pF	0	20 Note	ns
MI2TER output delay	$t_{D2TR2TK}$	Load 50 pF	0	20 Note	ns

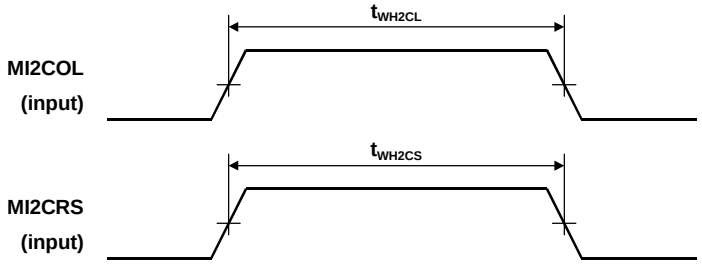
Note In the MII specification, maximum output delay is specified as 25 ns.

MII data reception parameters



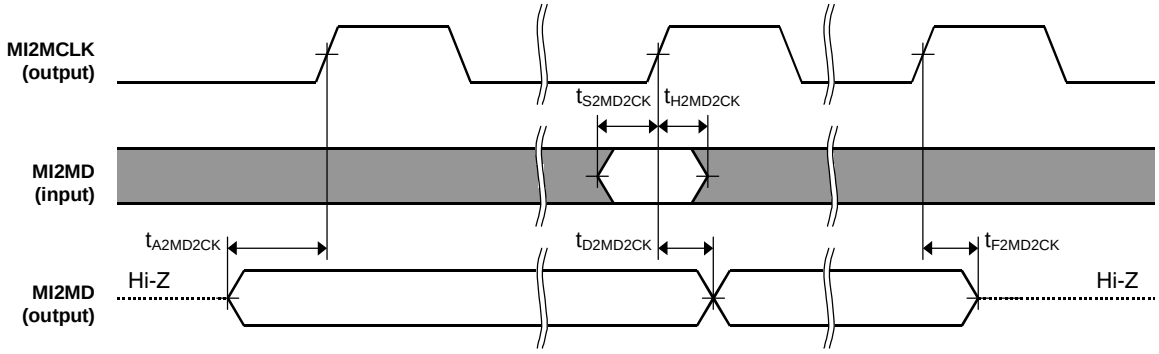
Parameter	Symbol	Conditions	Min.	Max.	Unit
MI2RDV setup time	$t_{S2RV2RK}$		10		ns
MI2RDV hold time	$t_{H2RV2RK}$		10		ns
MI2RD[3:0] setup time	$t_{S2RD2RK}$		10		ns
MI2RD[3:0] hold time	$t_{H2RD2RK}$		10		ns
MI2RER setup time	$t_{S2RR2RK}$		10		ns
MI2RER hold time	$t_{H2RR2RK}$		10		ns

MII interface signal parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
MI2COL high pulse width	t_{WH2CL}		$2 \times t_{CY2TK}$		ns
MI2CRS high pulse width	t_{WH2CS}		$2 \times t_{CY2TK}$		ns

MII management interface parameters

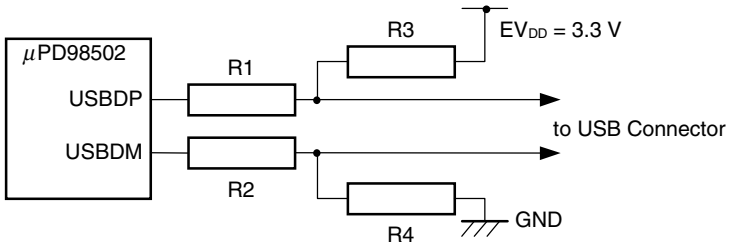


	Parameter	Symbol	Conditions	Min.	Max.	Unit
	MI2MD setup to MI2MCLK	$t_{S2MD2CK}$		20		ns
	MI2MD hold from MI2MCLK	$t_{H2MD2CK}$		0		ns
	MI2MD active delay from MI2MCLK	$t_{A2MD2CK}$	Load 50 pF	10		ns
★	MI2MD output delay from MI2MCLK	$t_{D2MD2CK}$	Load 50 pF	10	30	ns
★	MI2MD floating delay from MI2MCLK	$t_{F2MD2CK}$	Load 50 pF	10		ns

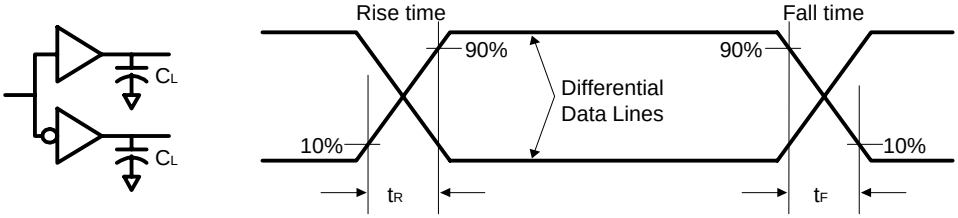
(10) USB interface parameters

★ **External circuitry**

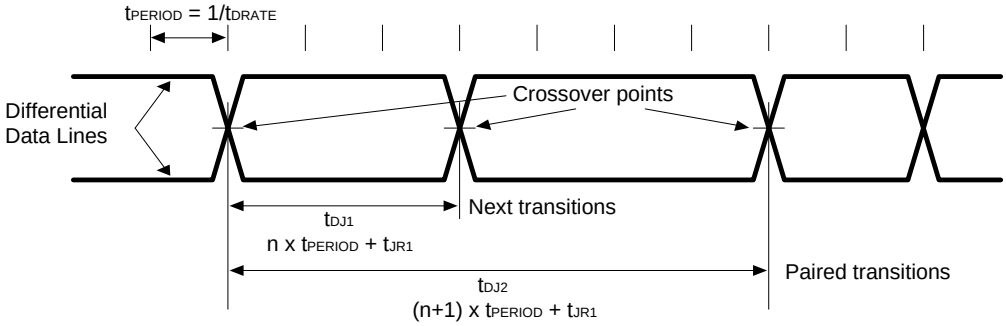
The USB line I/O signals (refer to **chapter 1.9 USB interface**) need 4 external resistors to adjust the output impedance (R1 and R2 = 22 Ω each), to code the full speed USB mode (R3 = 1.5 kΩ) and to protect the output driver of the USBDM pin (R4 = 51 kΩ). The following figure shows a typical connection diagram.



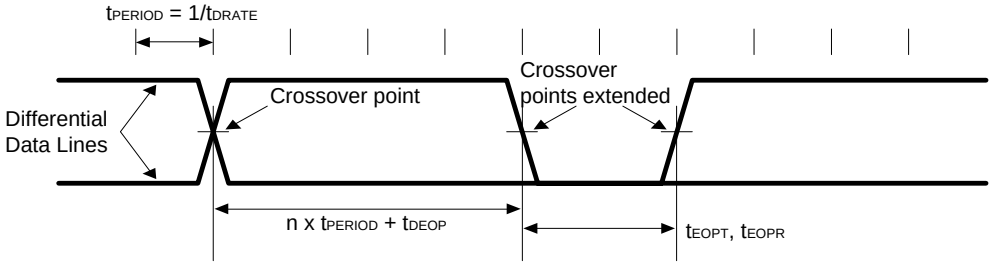
Data signal rise and fall time



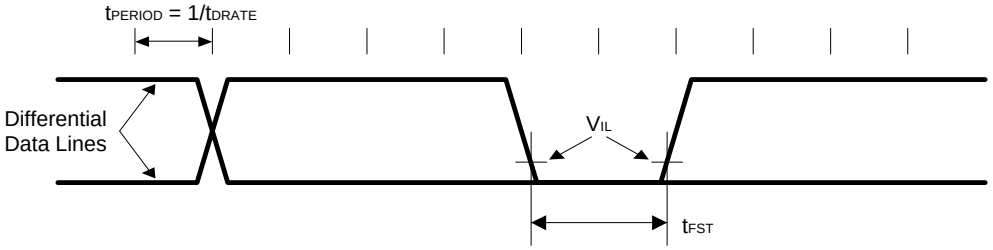
Differential data jitter



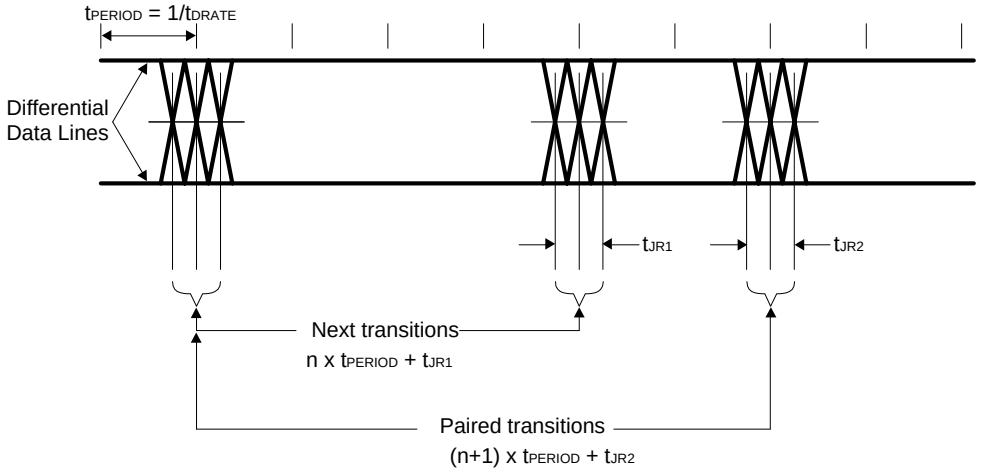
Differential-to-EOP transition skew and EOP width



Differential transition interval width



Receiver jitter tolerance

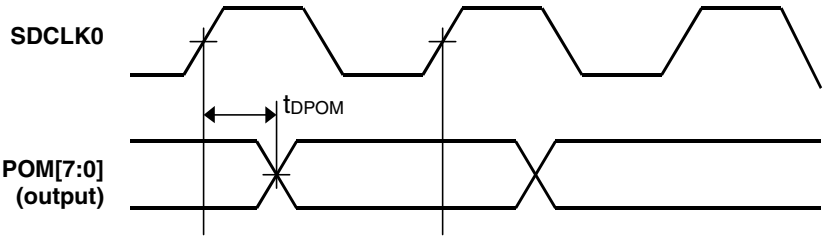


USB interface parameters (USBDM and USBDP)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Rise time	t_R		1	20	ns
Fall time	t_F		1	20	ns
Differential rise and fall time matching	t_{FRFM}	t_R/t_F	90	111.11	%
Full-speed data rate	t_{DRATE}		11.97	12.03	Mbps
Source jitter total (including frequency tolerance):					
To next transition	t_{DJ1}		−3.5	+3.5	ns
For paired transitions	t_{DJ2}		−4	+4	ns
Source jitter for differential transition to SE0 transition	t_{DEOP}		−2	+5	ns
Receiver jitter:					
To next transition	t_{JR1}		−18.5	+18.5	ns
For paired transitions	t_{JR2}		−9	+9	ns
Source SE0 interval of EOP	t_{EOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{EOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

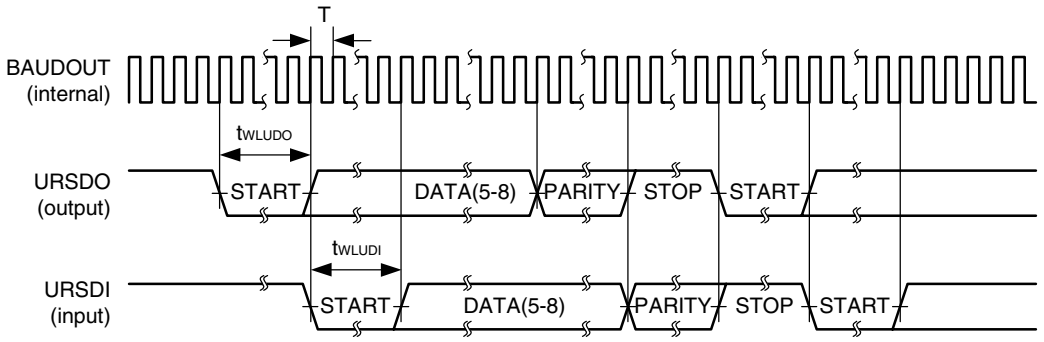
(11) Parallel port interface parameters

★



Parameter	Symbol	Conditions	Min.	Max.	Unit
POM[7:0] output delay	t_{DPOM}	Load 50 pF	0.0	8.0	ns

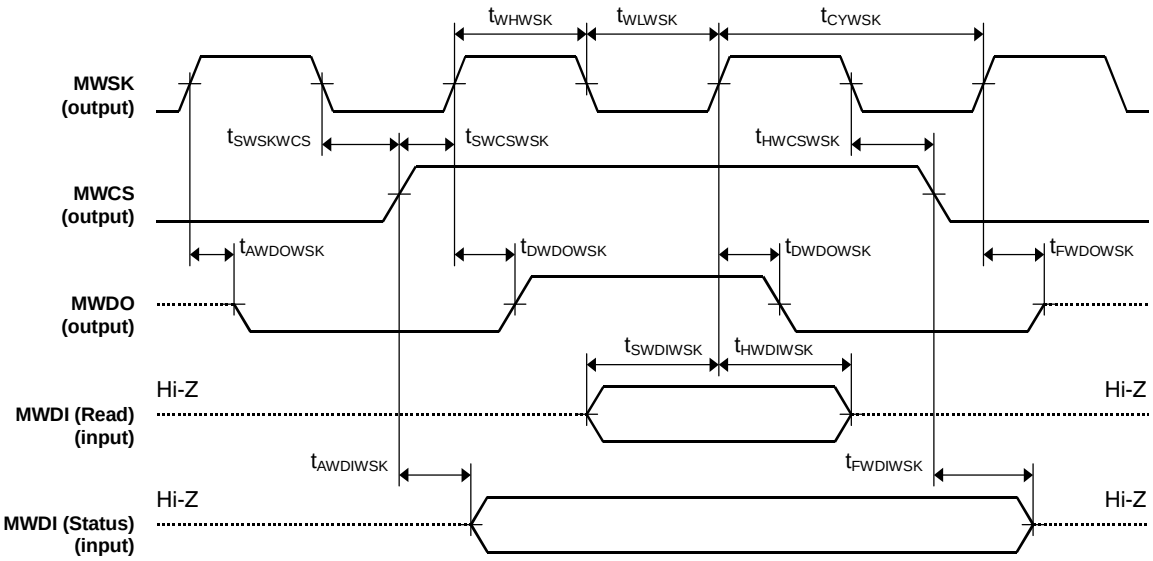
★ **(12) UART interface parameters**



Remark The BAUDOUT is equal to the 16X of transmisson baud rate (1/T = 16 × Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

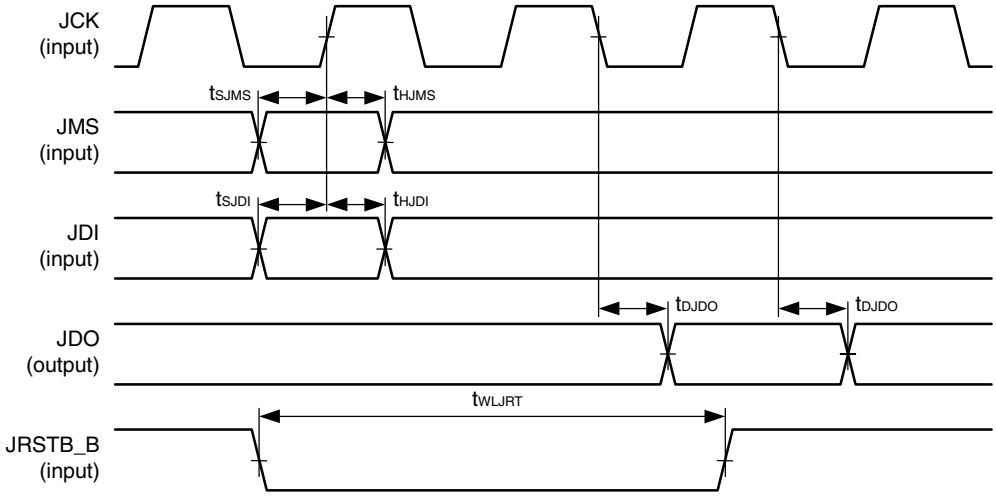
Parameter	Symbol	Conditions	Min.	Max.	Unit
URCLK input frequency	t_{CYUCK}			18.432	MHz
URSDO low level width	t_{WLUDO}		16 × T		ns
URSDI low level width	t_{WLUDI}		16 × T		ns

(13) Micro Wire interface parameters



Parameter	Symbol	Conditions	Min.	Max.	Unit
MWSK clock frequency	t_{CYWSK}	Load 50 pF	400 × t_{CYSK0}		ns
MWSK high time	t_{WHWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK low time	t_{WLWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK setup to MWCS	$t_{SWSKWCS}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS setup to MWSK	$t_{SWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS hold from MWSK	$t_{HWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWDO output active to floating delay from MWSK	$t_{AWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO output delay from MWSK	$t_{DWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO output floating to active delay from MWSK	$t_{FWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDI setup to MWSK	$t_{SWDIWSK}$		10 × t_{CYSK0}		ns
MWDI hold from MWSK	$t_{HWDIWSK}$		10 × t_{CYSK0}		ns
MWCS to status time from MWSK	$t_{AWDIWSK}$			100 × t_{CYSK0}	ns
MWCS to MWDO in 3-state	$t_{FWDIWSK}$			40 × t_{CYSK0}	ns

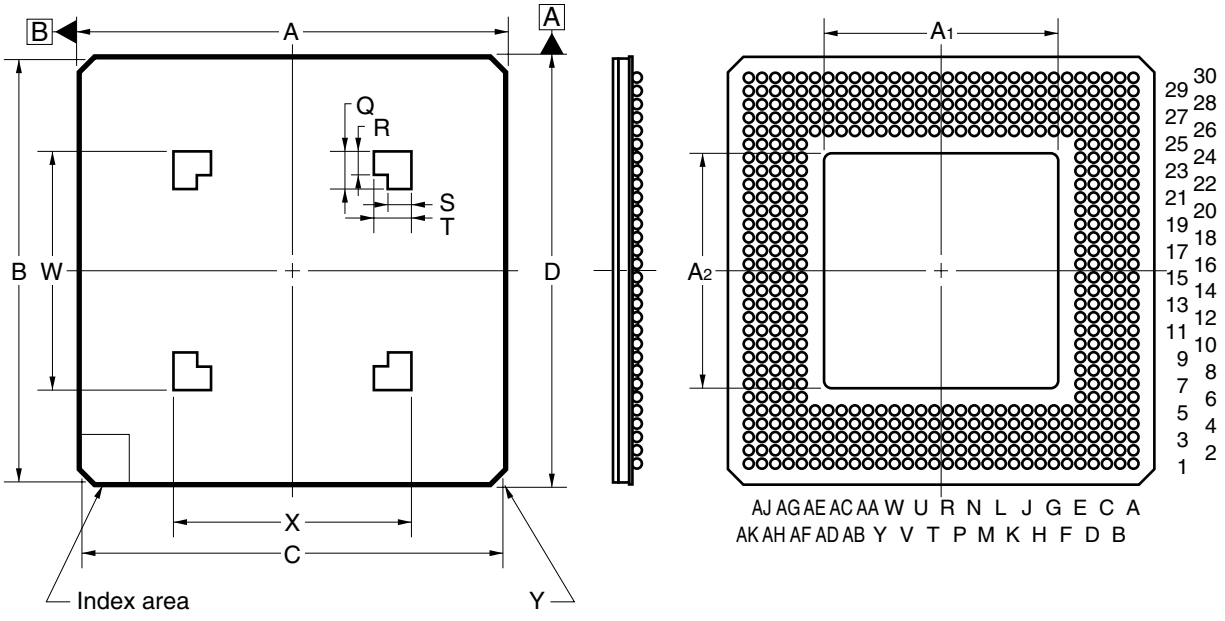
(14) JTAG boundary scan parameters

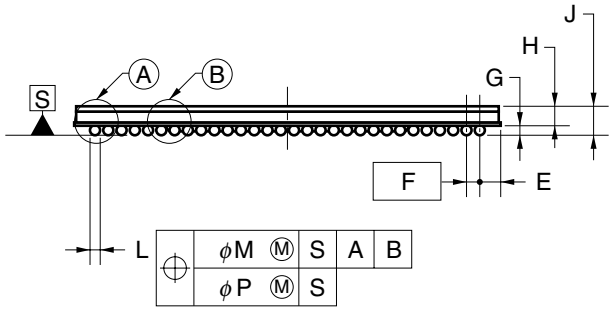


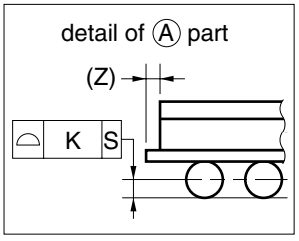
	Parameter	Symbol	Conditions	Min.	Max.	Unit
	JMS setup time	t_{SJMS}		5		ns
★	JMS hold time	t_{HJMS}		10		ns
	JDI setup time	t_{SJDI}		5		ns
★	JDI hold rime	t_{HJDI}		12		ns
★	JDO output delay	t_{DJDO}	Load 50 pF		30	ns
	JRSTB_B low pulse width	t_{WLJRT}		$5 \times t_{CYJCK}$		ns

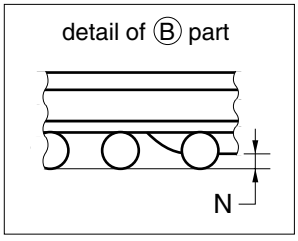
3. PACKAGE DRAWING

500-PIN TAPE BGA (HEAT SPREADER TYPE) (40x40)









ITEM	MILLIMETERS
A	40.00±0.20
A_1	23.00 MAX.
A_2	23.00 MAX.
B	39.60±0.15
C	39.60±0.15
D	40.00±0.20
E	1.585
F	1.27 (T.P.)
G	0.60±0.10
H	$0.80^{+0.20}_{-0.10}$
J	$1.40^{+0.30}_{-0.20}$
K	0.15
L	φ0.75±0.15
M	0.30
N	0.25 MIN.
P	0.10
Q	3.0
R	2.0
S	2.0
T	3.0
W	22.73
X	22.73
Y	C 0.40
Z	0.20

S500N7-127-H6-1

4. RECOMMENDED SOLDERING CONDITIONS

The μPD98502 should be soldered and mounted under the following recommended conditions. For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

μPD98502N7-H6: 500-pin tape BGA (Heat spreader type) (40 × 40)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less, Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less, Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours)	VP15-107-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

Phase-out/Discontinued

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Ethernet is a trademark of Xerox Corp.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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M8E 00.4