To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD98414

2.4 Gbps ATM SONET FRAMER

The μPD98414 (NEASCOT-P70™) is one of ATM LSIs and provides the functions of the TC sublayer of the SONET/SDH-base physical layer of the ATM protocol specified by the ATM Forum.

Its main functions include a transmission function for mapping an ATM cell passed from a high-end ATM layer device to the payload of a 2.4 Gbps SONET STS-48c/SDH STM-16c frame and transmitting the cell to a MUX device in the circuit, and a reception function for separating the overhead and ATM cell from the data string received from a DEMUX device and transmitting the ATM cell to the ATM layer device.

This LSI is ideal for systems that constitute the ATM network of a LAN or WAN, such as a transmission system, ATM switch, and high-speed backbone switch.

Detailed descriptions of its functions, etc., are given in the following user's manual. Be sure to read it for design purposes.

μPD98414 User's Manual: S14166E

FEATURES

- Supplies the functions of the TC (Transmission Convergence) sublayer recommended by the ATM Forum and ITU-T.
- Supports the concatenation frame of 2.4 Gbps SONET STS-48c/SDH STM-16c.
- ATM layer interface
  - 32-bit, 104-MHz LVTTL FIFO interface
  - 15-cell transmit/receive FIFO
  - Supports 52-byte/56-byte cell formats.
  - Prefixes one-word TAG area to receive cell.
- Circuit side interface
  - 16-bit PECL level I/O
- Either of two modes can be selected for CPU interface
  - 16-bit data bus
  - Intel-compatible mode [RD, WR, RDY-type]/Motorola-compatible mode [DS, R/W, ACK-type]
- Supports two types of overhead interfaces (that can access all overhead areas).
  - Incorporates overhead byte insert/drop registers.
  - Incorporates dedicated overhead byte insert/extract interfaces.

Document No. S14242EJ2V0DS00 (2nd edition)
Date Published July 2001 NS CP(K)
Printed in Japan

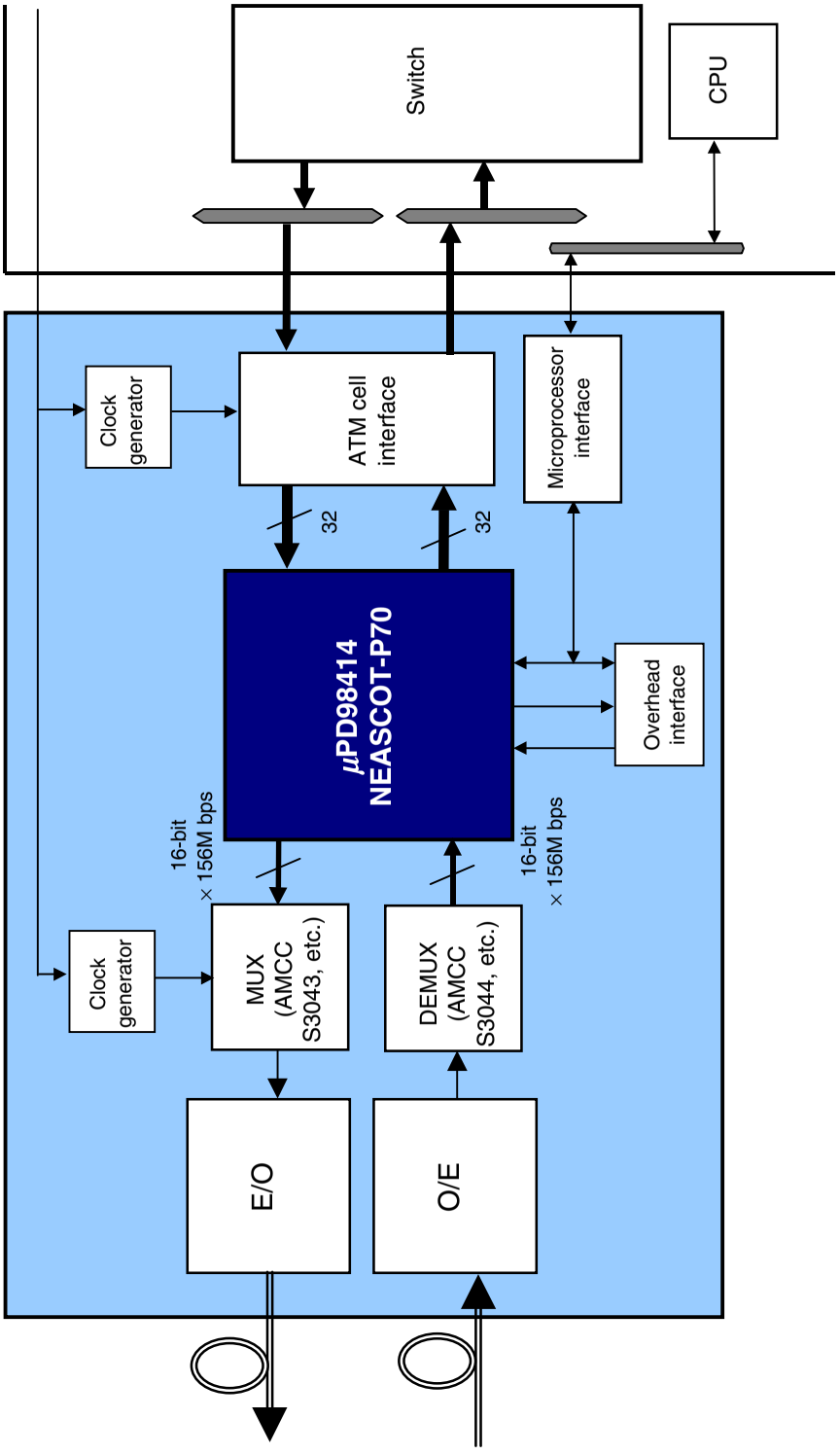
The mark ★ shows major revised points.

- Many OAM functions
  - Fault: Detection of LOS, OOF, LOF, LOP, OCD, and LCD
  - Alarm: Detection and transmission of APS, Line AIS, Line RDI, Path AIS, and Path RDI
  - Receive APS signal and Signal Label (C2 byte) monitoring functions
  - Bit error rate monitoring function
- Transmit/receive message buffer for J0/J1 trace messages (16 bytes or 64 bytes long)
- Supports loopback function.
  Remote: Two modes (ATM layer loopback and circuit side loopback)
- Supports an error generation pseudo frame transmission function for testing.
- Three general-purpose input and five general-purpose output ports
- Supports JTAG boundary scan test (IEEE1149.1).
- 0.35-μm CMOS process
- +3.3 V single power source

ORDERING INFORMATION

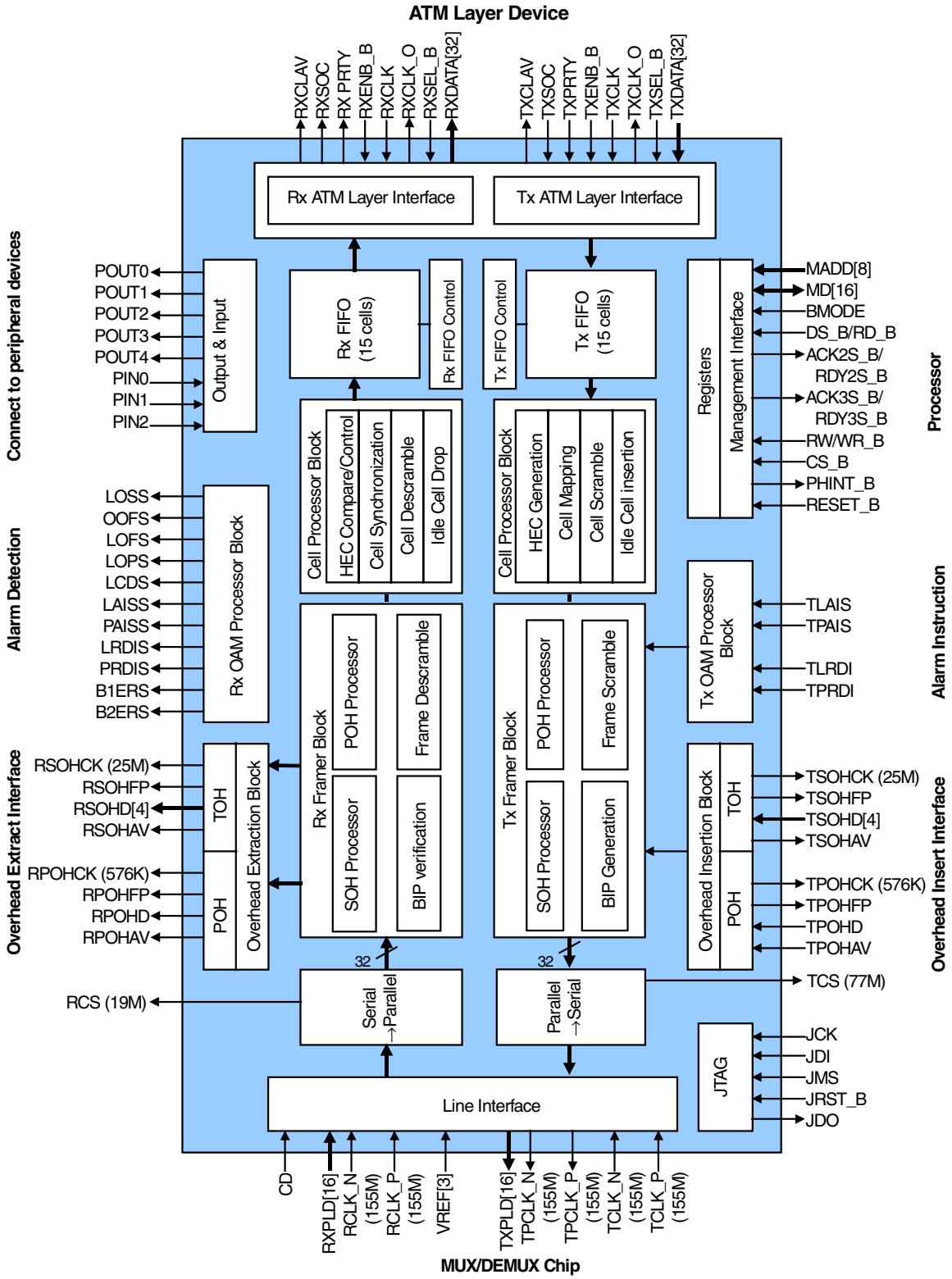
Part Number	Package
μPD98414F2-RN1	352-pin plastic BGA (cavity down advanced type) (35 × 35)

SYSTEM CONFIGURATION

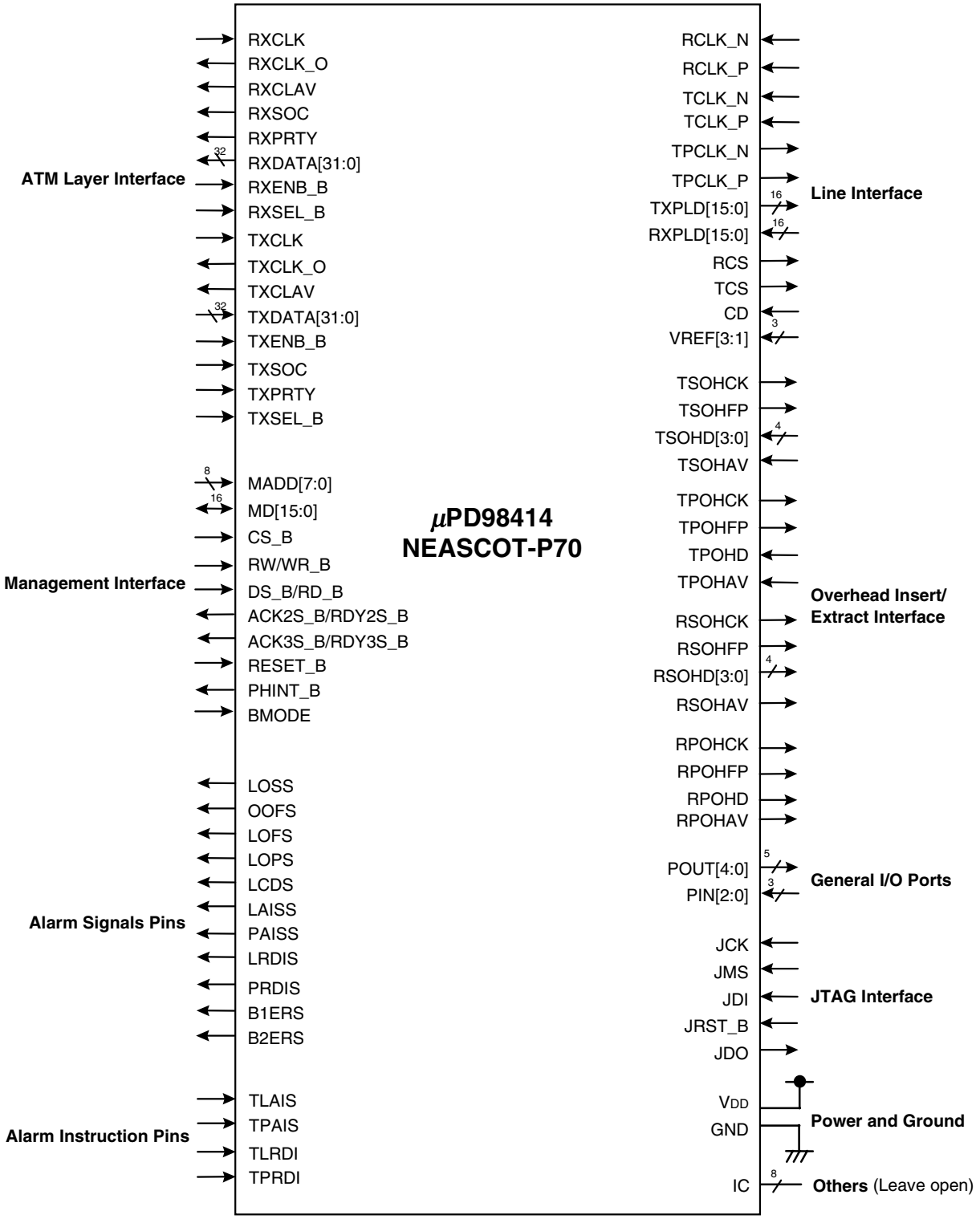


Phase-out/Discontinued

BLOCK DIAGRAM

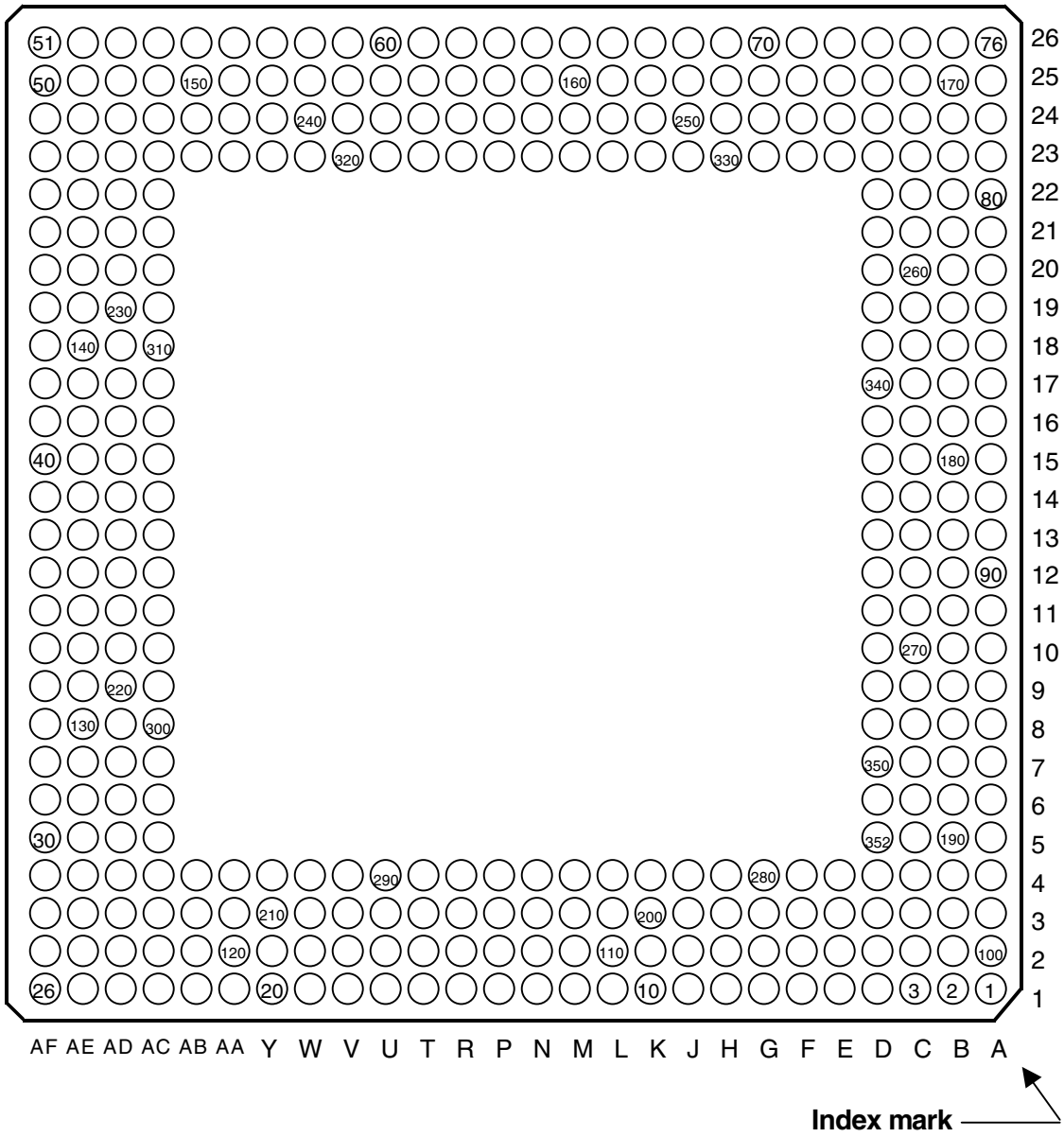


PIN CONFIGURATION



PIN CONFIGURATION (BOTTOM VIEW)

- **352-pin plastic BGA (cavity down advanced type) (35 × 35)**
  μPD98414F2-RN1



PIN ARRANGEMENT TABLE

(1/4)

Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name
1	A01	GND	36	AF11	RXDATA15	71	F26	TXCLAV
2	B01	TCS	37	AF12	RXDATA17	72	E26	GND
3	C01	IC	38	AF13	GND	73	D26	POUT0
4	D01	IC	39	AF14	RXDATA19	74	C26	PHINT_B
5	E01	RXPLD15	40	AF15	GND	75	B26	GND
6	F01	RXPLD13	41	AF16	RXDATA24	76	A26	GND
7	G01	GND	42	AF17	GND	77	A25	RW/WR_B
8	H01	RXPLD10	43	AF18	RXDATA28	78	A24	MADD6
9	J01	RXPLD8	44	AF19	RXDATA30	79	A23	MADD4
10	K01	V_{DD}	45	AF20	RXPRTY	80	A22	MADD1
11	L01	GND	46	AF21	RXCLAV	81	A21	MD13
12	M01	RXPLD4	47	AF22	GND	82	A20	MD10
13	N01	V_{DD}	48	AF23	POUT1	83	A19	MD7
14	P01	GND	49	AF24	PRDIS	84	A18	MD3
15	R01	GND	50	AF25	V_{DD}	85	A17	MD0
16	T01	V_{DD}	51	AF26	GND	86	A16	GND
17	U01	RCLK_P	52	AE26	LAISS	87	A15	TXPLD13
18	V01	RPOHFP	53	AD26	OOFS	88	A14	GND
19	W01	RSOHD2	54	AC26	GND	89	A13	GND
20	Y01	RSOHAV	55	AB26	TXDATA1	90	A12	V_{DD}
21	AA01	TPOHAV	56	AA26	V_{DD}	91	A11	V_{DD}
22	AB01	TSOHD2	57	Y26	GND	92	A10	GND
23	AC01	TSOHD0	58	W26	V_{DD}	93	A09	V_{DD}
24	AD01	POUT4	59	V26	TXDATA10	94	A08	TXPLD3
25	AE01	GND	60	U26	TXDATA12	95	A07	V_{DD}
26	AF01	GND	61	T26	TXDATA15	96	A06	GND
27	AF02	PIN1	62	R26	TXDATA17	97	A05	TPCLK_P
28	AF03	TLRDI	63	P26	GND	98	A04	IC
29	AF04	POUT2	64	N26	TXDATA19	99	A03	JDI
30	AF05	RXDATA1	65	M26	GND	100	A02	V_{DD}
31	AF06	V_{DD}	66	L26	TXDATA24	101	B02	V_{DD}
32	AF07	GND	67	K26	GND	102	C02	RCS
33	AF08	V_{DD}	68	J26	TXDATA28	103	D02	IC
34	AF09	RXDATA10	69	H26	TXDATA30	104	E02	V_{DD}
35	AF10	RXDATA12	70	G26	TXPRTY	105	F02	GND

(2/4)

Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name
106	G02	RXPLD12	141	AE19	RXDATA31	176	B19	MD9
107	H02	RXPLD11	142	AE20	RXENB_B	177	B18	MD5
108	J02	RXPLD9	143	AE21	V_{DD}	178	B17	MD1
109	K02	VREF2	144	AE22	RXCLK_O	179	B16	GND
110	L02	GND	145	AE23	B2ERS	180	B15	V_{DD}
111	M02	V_{DD}	146	AE24	PAISS	181	B14	TXPLD12
112	N02	RXPLD3	147	AE25	V_{DD}	182	B13	TXPLD11
113	P02	RXPLD2	148	AD25	LOSS	183	B12	TXPLD9
114	R02	RXPLD0	149	AC25	LCDS	184	B11	TXPLD7
115	T02	RCLK_N	150	AB25	V_{DD}	185	B10	GND
116	U02	RPOHD	151	AA25	TXDATA3	186	B09	V_{DD}
117	V02	RSOHD3	152	Y25	TXDATA5	187	B08	GND
118	W02	RSOHD1	153	W25	TXDATA6	188	B07	TXPLD1
119	Y02	RSOHFP	154	V25	TXDATA9	189	B06	TCLK_N
120	AA02	TPOHFP	155	U25	V_{DD}	190	B05	TPCLK_N
121	AB02	TSOHD1	156	T25	GND	191	B04	JCK
122	AC02	TSOHFP	157	R25	TXDATA16	192	B03	JRST_B
123	AD02	PIN2	158	P25	TXDATA18	193	C03	V_{DD}
124	AE02	V_{DD}	159	N25	V_{DD}	194	D03	IC
125	AE03	PIN0	160	M25	TXDATA22	195	E03	VREF3
126	AE04	TPAIS	161	L25	TXDATA25	196	F03	GND
127	AE05	V_{DD}	162	K25	TXDATA27	197	G03	V_{DD}
128	AE06	RXDATA3	163	J25	GND	198	H03	V_{DD}
129	AE07	RXDATA5	164	H25	TXDATA31	199	J03	V_{DD}
130	AE08	RXDATA6	165	G25	TXENB_B	200	K03	GND
131	AE09	RXDATA9	166	F25	V_{DD}	201	L03	RXPLD7
132	AE10	V_{DD}	167	E25	TXCLK_O	202	M03	RXPLD5
133	AE11	GND	168	D25	RESET_B	203	N03	V_{DD}
134	AE12	RXDATA16	169	C25	DS_B/RD_B	204	P03	RXPLD1
135	AE13	RXDATA18	170	B25	V_{DD}	205	R03	GND
136	AE14	V_{DD}	171	B24	ACK3S_B/RDY3S_B	206	T03	GND
137	AE15	RXDATA22	172	B23	MADD5	207	U03	RPOHAV
138	AE16	RXDATA25	173	B22	MADD2	208	V03	V_{DD}
139	AE17	RXDATA27	174	B21	MD14	209	W03	RSOHD0
140	AE18	GND	175	B20	MD11	210	Y03	TPOHD

(3/4)

Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name
211	AA03	TSOHD3	246	N24	TXDATA21	281	H04	GND
212	AB03	TSOHAV	247	M24	TXDATA23	282	J04	GND
213	AC03	POUT3	248	L24	TXDATA26	283	K04	V_{DD}
214	AD03	V_{DD}	249	K24	V_{DD}	284	L04	GND
215	AD04	CD	250	J24	V_{DD}	285	M04	RXPLD6
216	AD05	RXDATA0	251	H24	V_{DD}	286	N04	GND
217	AD06	GND	252	G24	TXSEL_B	287	P04	V_{DD}
218	AD07	RXDATA4	253	F24	TXCLK	288	R04	VREF1
219	AD08	V_{DD}	254	E24	IC	289	T04	V_{DD}
220	AD09	RXDATA8	255	D24	CS_B	290	U04	RPOHCK
221	AD10	RXDATA11	256	C24	V_{DD}	291	V04	GND
222	AD11	RXDATA13	257	C23	ACK2S_B/RDY2S_B	292	W04	RSOHCK
223	AD12	V_{DD}	258	C22	MADD3	293	Y04	TPOHCK
224	AD13	V_{DD}	259	C21	MADD0	294	AA04	GND
225	AD14	RXDATA21	260	C20	MD12	295	AB04	TSOHCK
226	AD15	RXDATA23	261	C19	V_{DD}	296	AC04	GND
227	AD16	RXDATA26	262	C18	MD6	297	AC05	TPRDI
228	AD17	V_{DD}	263	C17	MD2	298	AC06	V_{DD}
229	AD18	V_{DD}	264	C16	V_{DD}	299	AC07	RXDATA2
230	AD19	V_{DD}	265	C15	TXPLD14	300	AC08	GND
231	AD20	RXSEL_B	266	C14	V_{DD}	301	AC09	RXDATA7
232	AD21	RXCLK	267	C13	TXPLD10	302	AC10	GND
233	AD22	TLAIS	268	C12	GND	303	AC11	GND
234	AD23	LRDIS	269	C11	TXPLD6	304	AC12	RXDATA14
235	AD24	V_{DD}	270	C10	TXPLD5	305	AC13	GND
236	AC24	LOPS	271	C09	V_{DD}	306	AC14	RXDATA20
237	AB24	TXDATA0	272	C08	TXPLD2	307	AC15	V_{DD}
238	AA24	GND	273	C07	TXPLD0	308	AC16	V_{DD}
239	Y24	TXDATA4	274	C06	V_{DD}	309	AC17	RXDATA29
240	W24	V_{DD}	275	C05	IC	310	AC18	GND
241	V24	TXDATA8	276	C04	JMS	311	AC19	GND
242	U24	TXDATA11	277	D04	GND	312	AC20	RXSOC
243	T24	TXDATA13	278	E04	IC	313	AC21	GND
244	R24	V_{DD}	279	F04	V_{DD}	314	AC22	B1ERS
245	P24	V_{DD}	280	G04	RXPLD14	315	AC23	GND

(4/4)

Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name	Serial No.	Address No.	Pin Name
316	AB23	LOFS	331	G23	TXSOC	346	D11	V_{DD}
317	AA23	V_{DD}	332	F23	GND	347	D10	TXPLD4
318	Y23	TXDATA2	333	E23	BMODE	348	D09	GND
319	W23	GND	334	D23	GND	349	D08	GND
320	V23	TXDATA7	335	D22	MADD7	350	D07	TCLK_P
321	U23	GND	336	D21	V_{DD}	351	D06	GND
322	T23	GND	337	D20	MD15	352	D05	JDO
323	R23	TXDATA14	338	D19	GND			
324	P23	GND	339	D18	MD8			
325	N23	TXDATA20	340	D17	MD4			
326	M23	V_{DD}	341	D16	GND			
327	L23	V_{DD}	342	D15	TXPLD15			
328	K23	TXDATA29	343	D14	GND			
329	J23	GND	344	D13	V_{DD}			
330	H23	GND	345	D12	TXPLD8			

PIN NAME

ACK2S_B	Acknowledge 2 State	RSOHFP	Rx SOH Insert Frame Pulse
ACK3S_B	Acknowledge 3 State	RW	Management Data Read/Write
B1ERS	B1 Error Rate Degrade	RXCLAV	Rx Cell Available
B2ERS	B2 Error Rate Degrade	RXCLK	UTOPIA Rx Clock In
BMODE	Bus Mode	RXCLK_O	UTOPIA Rx Clock Out
CD	Carrier Detect	RXDATA0-	UTOPIA Rx Data
CS_B	Chip Select	RXDATA31	
DS_B	Data Strobe	RXENB_B	Rx Cell Enable
GND	Ground	RXPLD0-RXPLD15	Rx Line Data
IC	Internal Circuits Connection	RXPRTY	Rx Parity
JCK	JTAG Test Clock	RXSEL_B	Rx Cell Select
JDI	JTAG Test Data In	RXSOC	Rx Start Of Cell
JDO	JTAG Test Data Out	TCLK_N	Tx Clock In – (155 MHz)
JMS	JTAG Test Mode Select	TCLK_P	Tx Clock In + (155 MHz)
JRST_B	JTAG Test Reset	TCS	Tx Line Clock Signal Out (77 MHz)
LAISS	Line AIS State	TLAIS	Tx Line AIS Frame Send
LCDS	LCD State	TLRDI	Tx Line RDI Frame Send
LOFS	LOF State	TPAIS	Tx Path AIS Frame Send
LOPS	LOP State	TPCLK_N	Tx Clock Out – (155 MHz)
LOSS	LOS State	TPCLK_P	Tx Clock Out + (155 MHz)
LRDIS	Line RDI State	TPOHAV	Tx POH Insert Available
MADD0-MADD7	Management Address	TPOHCK	Tx POH Insert Clock
MD0-MD15	Management Data	TPOHD	Tx POH Insert Data
OOFS	OOF State	TPOHFP	Tx POH Insert Frame Pulse
PAISS	Path AIS State	TPRDI	Tx Path RDI Frame Send
PHINT_B	Interrupt	TSOHAV	Tx TOH Insert Available
PIN0-PIN2	General In	TSOHCK	Tx TOH Insert Clock
POUT0-POUT4	General Out	TSOHD0-TSOHD3	Tx TOH Insert Data
PRDIS	Path RDI State	TSOHFP	Tx TOH Insert Frame Pulse
RCLK_N	Rx Line Clock – (155 MHz)	TXCLAV	Tx Cell Available
RCLK_P	Rx Line Clock + (155 MHz)	TXCLK	UTOPIA Tx Clock In
RCS	Rx Line Clock Signal Out (19 MHz)	TXCLK_O	UTOPIA Tx Clock Out
RD_B	Read	TXDATA0-	UTOPIA Tx Data
RDY2S_B	Ready 2-State	TXDATA31	
RDY3S_B	Ready 3-State	TXENB_B	Tx Cell Enable
RESET_B	Reset	TXPLD0-TXPLD15	Tx Line Data
RPOHAV	Rx POH Insert Available	TXPRTY	Tx Parity
RPOHCK	Rx POH Insert Clock	TXSEL_B	Tx Cell Select
RPOHD	Rx POH Insert Data	TXSOC	Tx Start Of Cell
RPOHFP	Rx POH Insert Frame Pulse	V_{DD}	V_{DD}
RSOHAV	Rx SOH Insert Available	VREF1-VREF3	Voltage Reference For PECL In
RSOHCK	Rx SOH Insert Clock	WR_B	Write
RSOHD0-RSOHD3	Rx SOH Insert Data		

CONTENTS

1. PIN FUNCTION

1.1 Line Interface

The line interface connects MUX and DEMUX devices in the circuit.

Pin Name	Serial No.	Address No.	I/O, Level	Function
RCLK_N	115	T02	I PECL	Receive clock input (155.52 MHz). These pins input a 155.52-MHz clock, synchronized with the receive data.
RCLK_P	17	U01		
TCLK_N	189	B06	I PECL	Transmit clock input (155.52 MHz). These pins input a transmit clock. The μPD98411 updates transmit data TXPLD15 through TXPLD0 at the rising edge of this clock.
TCLK_P	350	D07		
TPCLK_N	190	B05	O PECL	Transmit clock output (155.52 MHz). The clocks input to TCLK_N and TCLK_P are internally inverted and output from these pins.
TPCLK_P	97	A05		
RXPLD15-RXPLD0	5, 280, 6, 106, 107, 8, 108, 9, 201, 285, 202, 12, 112, 113, 204, 114	E01, G04, F01, G02, H02, H01, J02, J01, L03, M04, M03, M01, N02, P02, P03, R02	I PECL	Receive 16-bit parallel data input.
TXPLD15-TXPLD0	342, 265, 87, 181, 182, 267, 183, 345, 184, 269, 270, 347, 94, 272, 188, 273	D15, C15, A15, B14, B13, C13, B12, D12, B11, C11, C10, D10, A08, C08, B07, C07	O PECL	Transmit 16-bit parallel data output.
TCS	2	B01	O LVTTL	Transmit system clock output (77.76 MHz). The transmit clocks input to TCLK_N and TCLK_P are divided by two in the μPD98414 and output from this pin.
RCS	102	C02	O LVTTL	Receive system clock output (19.44 MHz). The receive clocks input to RCLK_N and RCLK_P are divided by eight in the μPD98414 and output from this pin.
CD	215	AD04	I LVTTL (5V tolerant)	Receive framer function reset. While the input level of this pin is low, the receive framer block (from the circuit up to the receive FIFO) is reset. The transition of this signal from high to low can be used as a condition for LOS detection. The optical input failure alarm signal output by a receive optical link module can be input to this pin.
VREF3-VREF1	195, 109, 288	E03, K02, R04	I VREF	These pins input reference potentials (intermediate potentials) for single-end PECL input signals (RXPLD[15:0]).

1.2 ATM Layer Interface

The ATM layer interface transfers cells to and from a high-end ATM layer device.

(1/3)

Pin Name	Serial No.	Address No.	I/O, Level	Function
RXCLK	232	AD21	I LVTTL	Receive FIFO clock input. This pin inputs the clock, from 8 to 104 MHz, used to transfer receive data.
RXCLK_O	144	AE22	O LVTTL	Receive FIFO clock return output. This pin returns and outputs the clock input to RXCLK.
RXSOC	312	AC20	O LVTTL	Receive cell start position signal output. This pin goes high during the clock cycle in which the first byte of the receive cell is output to RXDATA, to post notification to the ATM layer device.
RXCLAV	46	AF21	O LVTTL	Receive FIFO cell data transfer enable signal output. The μPD98414 drives RXCLAV high if one or more cells of receive data to be transferred exists in the receive FIFO, to post notification to the ATM layer device. RXCLAV is held high if one or more cells of valid data exists in the receive FIFO at the seventh clock cycle or later after the start of output of the cell; otherwise, RXCLAV goes low.
RXENB_B	142	AE20	I LVTTL	Receive enable signal input (byte unit control). The ATM layer device enables or disables the receive cell data output by the μPD98414 in byte units. The μPD98414 samples RXENB_B at the rising edge of RXCLK. When it detects the low level of RXENB_B, it updates the output of RSOC and RXDATA starting from the next clock cycle, and then transfers the receive cell data. If RXENB_B is high, the μPD98414 stops the output of RSOC and RXDATA, starting from the next clock cycle. **Caution This signal cannot be used with RXSEL_B at the same time. Fix this signal to the low level when it is not used.**
RXSEL_B	231	AD20	I LVTTL	Receive enable signal input (cell unit control). The ATM layer device enables the μPD98414 to output receive cell data in cell units. The μPD98414 samples RXSEL_B at the rising edge, one clock cycle before RXSOC goes high, and starts outputting receive cell data from the next clock cycle if RXSEL_B is low. Once the μPD98414 has detected that RXSEL_B has gone low, it does not sample RXSEL_B until the next sampling timing (one clock before RXSOC goes high). When the μPD98414 detects that RXSEL_B has gone high at the sampling timing, it continues sampling RXSEL_B at every clock, and starts outputting cells from the clock cycle next to that in which the low level of RXSEL_B was detected. **Caution This signal cannot be used with RXENB_B at the same time. Fix this signal to the low level when it is not used**.

(2/3)

Pin Name	Serial No.	Address No.	I/O, Level	Function
RXPRTY	45	AF20	O LVTTL	Parity bit output. This pin generates an odd parity bit for the output data on RXDATA and outputs it from RXPRTY. The parity bit is always output. The parity bit to be generated can be changed to even parity depending on the setting of the RRPM bit of the MDR5 register.
RXDATA31- RXDATA0	141, 44, 309, 43, 139, 227, 138, 41, 226, 137, 225, 306, 39, 135, 37, 134, 36, 304, 222, 35, 221, 34, 131, 220, 301, 130, 129, 218, 128, 299, 30, 216	AE19, AF19, AC17, AF18, AE17, AD16, AE16, AF16, AD15, AE15, AD14, AC14, AF14, AE13, AF12, AE12, AF11, AC12, AD11, AF10, AD10, AF09, AE09, AD09, AC09, AE08, AE07, AD07, AE06, AC07, AF05, AD05	O LVTTL	Receive cell data output bus. These pins form a 32-bit data bus through which receive cell data is output to the ATM layer device. The data on this bus is updated at the rising edge of RXCLK.
TXCLK	253	F24	I LVTTL	Transmit FIFO clock input. This pin inputs the clock, from 8 to 104 MHz, used to transfer transmit data.
TXCLK_O	167	E25	O LVTTL	Transmit FIFO clock return output. This pin returns and outputs the clock input to TXCLK.
TXSOC	331	G23	I LVTTL	Transmit cell start position signal input. This pin inputs a signal that indicates the start position of a transmit cell. The μPD98414 recognizes the clock cycle in which TXSOC is high as the first word of a cell.
TXCLAV	71	F26	O LVTTL	Transmit FIFO cell data reception enable signal output. This signal posts notification of the vacancy of the transmit FIFO to the ATM layer device. If the number of cells stored in the transmit FIFO has reached the threshold value set by the TCAV[1:0] bits of the MDR5 register, the μPD98414 drives TXCLAV low. The threshold value can be selected from 9, 11, 13, or 15 cells. The default value is 15 cells, at which point the transmit FIFO is full. The μPD98414 keeps receiving cells, even if TXCLAV is driven low, until the transmit FIFO is full (i.e., 15 cells). The 16th and subsequent cells are dropped and the μPD98414 reports an overflow of the transmit FIFO.

(3/3)

Pin Name	Serial No.	Address No.	I/O, Level	Function
TXENB_B	165	G25	I LVTTL	Transmit enable signal input (byte unit control). This signal indicates, in byte units, that the ATM layer device has output valid transmit cell data to TXDATA. The μPD98414 samples TXENB_B at the rising edge of TXCLK. If TXENB_B is low, it loads the data on TXSOC and TXDATA to the transmit FIFO at the edge of TXCLK. If TXENB_B is high, the data on TXSOC and TXDATA is not loaded to the transmit FIFO. **Caution This signal cannot be used with RXSEL_B at the same time. Fix this signal to the low level when it is not used.**
TXSEL_B	252	G24	I LVTTL	Transmit enable signal input (cell unit control). This signal informs the μPD98414, in cell units, that the ATM layer device is outputting valid transmit cell data to TXDATA. The μPD98414 samples TXSEL_B at the rising edge of the TXCLK clock immediately before a high level is input to TXSOC when it receives a transmit cell from the ATM layer device. If TXSEL_B is low, the μPD98414 loads the cell input in the next clock cycle to the transmit FIFO. Once the μPD98414 has detected the low level of TXSEL_B and started loading the cell, it does not sample TXSEL_B until the next sampling timing (i.e., the clock immediately before the next TXSOC input). If TXSEL_B is high at the clock immediately before the high level is input to TXSOC, the μPD98414 loads the next cell to the transmit FIFO. **Caution This signal cannot be used with RXSEL_B at the same time. Fix this signal to the low level when it is not used.**
TXPRTY	70	G26	I LVTTL (Internal pull-up)	Parity bit input. This pin inputs the odd parity bit of the data input to TXDATA. The μPD98414 calculates a parity based on the input data and parity bit. If it detects an error, it sets the UPED bit of the UEDR register to report the error. The μPD98414 calculates a parity only within the range of 53 bytes of the a transmit cell (H1 to P48). An even parity can be also used depending on the setting of the TRPM bit of the MDR5 register.
TXDATA31- TXDATA0	164, 69, 328, 68, 162, 248, 161, 66, 247, 160, 246, 325, 64, 158, 62, 157, 61, 323, 243, 60, 242, 59, 154, 241, 320, 153, 152, 239, 151, 318, 55, 237	H25, H26, K23, J26, K25, L24, L25, L26, M24, M25, N24, N23, N26, P25, R26, R25, T26, R23, T24, U26, U24, V26, V25, V24, V23, W25, Y25, Y24, AA25, Y23, AB26, AB24	I LVTTL	Transmit cell data input bus. These pins form a 32-bit data bus through which transmit cell data is input. The μPD98414 inputs the data on this bus at the rising edge of TXCLK.

1.3 Management Interface

The management interface is used to access the registers of the μPD98414.

(1/2)

Pin Name	Serial No.	Address No.	I/O, Level	Function
RESET_B	168	D25	I LVTTL (5V tolerant)	System reset input. This signal initializes the μPD98414. Input a low-pulse signal having a width of at least 100 ns.
PHINT_B	74	C26	O LVTTL (5V tolerant)	Interrupt signal output. This signal informs the host of occurrence of an interrupt cause.
BMODE	333	E23	I LVTTL (5V tolerant)	Bus mode select input. The mode of the management interface is determined from the input level of this signal after a reset. BMODE = Low: <DS, R/W, ACK> -type is selected. High: <RD, WR, RDY> -type is selected.
MADD7- MADD0	335, 78, 172, 79, 258, 173, 80, 259	D22, A24, B23, A23, C22, B22, A22, C21	I LVTTL (5V tolerant)	Address input. These pins form the 8-bit bus used to input the addresses of the internal registers.
MD15-MD0	337, 174, 81, 260, 175, 82, 176, 339, 83, 262, 177, 340, 84, 263, 178, 85	D20, B21, A21, C20, B20, A20, B19, D18, A19, C18, B18, D17, A18, C17, B17, A17	I/O LVTTL (5V tolerant)	16-bit data bus. This 16-bit data bus is used to exchange data with the internal registers.
RW (WR_B)	77	A25	I LVTTL (5V tolerant)	Read/write signal input or write signal input. The function of this signal differs depending on the mode set by BMODE. When BMODE = low, it functions as a read/write control signal (RW). RW = High: Ready cycle Low: Write cycle When BMODE = high, it functions as a write signal (WR_B) that specifies a write access.
ACK2S_B (RDY2S_B)	257	C23	O LVTTL (5V tolerant)	Acknowledge signal output or ready signal two-state output. This pin indicates that data is ready when it is accessed for read. It outputs an acknowledge ready signal, which indicates that data can be received, in two states during the write cycle.
ACK3S_B (RDY3S_B)	171	B24	O 3-state LVTTL (5V tolerant)	Acknowledge signal output or ready signal tristate output. This pin indicates that data is ready when it is accessed for read. It outputs an acknowledge ready signal, which indicates that data can be received, in tristate during the write cycle.
CS_B	255	D24	I LVTTL (5V tolerant)	Chip select signal input. When this signal is low, access to the internal registers of the μPD98414 is enabled.

(2/2)

Pin Name	Serial No.	Address No.	I/O, Level	Function
DS_B (RD_B)	169	C25	I LVTTL (5V tolerant)	Data strobe signal input or read signal input. The function of this pin differs depending on the management interface mode selected by the input to the BMODE pin. BMODE = low: Functions as a data strobe signal (DS_B) that indicates that data is output to MD. BMODE = high: Functions as a read signal (RD_B) that specifies a read access.

1.4 Overhead Interface

The overhead interface is used to transfer the contents of the section overhead (SOH) and path overhead (POH) that are exchanged between the peripheral device and μPD98414.

(1/2)

Pin Name	Serial No.	Address No.	I/O, Level	Function
TSOHCK	295	AB04	O LVTTL	Transmit TOH interface clock output (25.92 MHz). This pin outputs a 25.92-MHz clock obtained by internally dividing transmit clock TCLK (155.52 MHz) by six. TSOHFP and TSOHD are output in sync with this divided clock.
TSOHFP	122	AC02	O LVTTL	Transmit TOH frame pulse output. TSOHFP is driven high one clock cycle before the input of transmit TOH data is started.
TSOHD3- TSOHD0	211, 22, 121, 23	AA03, AB01, AB02, AC01	I LVTTL (5V tolerant/ Internal pull-down)	Transmit TOH data input 4-bit bus. This is a 4-bit data bus that inputs transmit TOH data. It inputs the TOH data on TSOHD as 1 byte in two clock cycles, starting from the clock cycle next to that in which TSOHFP is output.
TSOHAV	212	AB03	I LVTTL (5V tolerant/ Internal pull-down)	Transmit TOH data validity indication signal input. This signal informs the μPD98414 that valid TOH data has been output to TSOHD. The μPD98414 samples TSOHAV at the rising edge of TSOHCK during the first of the two clock cycles in which SOH data is input. If TSOHAV is high, the μPD98414 inputs the data on TSOHD in that cycle and the next; when TSOHAV is low, the μPD98414 does not input the data.
TPOHCK	293	Y04	O LVTTL	Transmit POH interface clock output (576 kHz). This pin outputs the 576-kHz clock resulting from internally dividing transmit clock TCLK (155.52 MHz) by 270. TPOHFP and TPOHD are output in sync with this divided clock.
TPOHFP	120	AA02	O LVTTL	Transmit POH frame pulse output. This signal is driven high one cycle before the clock cycle in which the input of the transmit POH data is started.
TPOHD	210	Y03	I LVTTL (5V tolerant/ Internal pull-down)	Transmit POH data input. This pin inputs serial transmit POH data. It inputs the transmit POH data on TPOHD as one byte in eight clock cycles, starting from the clock cycle next to that in which TPOHFP is output.

(2/2)

Pin Name	Serial No.	Address No.	I/O, Level	Function
TPOHAV	21	AA01	I LVTTL (5V tolerant/ Internal pull-down)	Transmit POH data validity indication signal input. This signal informs the μPD98414 that valid POH data has been output to TPOHD. The μPD98414 samples TPOHAV at the rising edge of TPOHCK in the first of the eight clock cycles in which POH data is input. If TPOHAV is high, the μPD98414 inputs the TPOHD data for a duration of eight clock cycles, starting from the cycle in which TPOHAV goes high; if TPOHAV is low, the μPD98414 does not input the TPOHD data.
RSOHCK	292	W04	O LVTTL	Receive TOH interface clock output (25.92 MHz) This pin outputs the 25.92-MHz clock obtained by internally dividing receive clock RCLK (155.52 MHz) by six. RSOHFP and RSOHAV are output in sync with this divided clock.
RSOHFP	119	Y02	O LVTTL	Receive TOH frame pulse output. This signal goes high one cycle before the clock cycle in which output of the receive SOH data is started.
RSOHD3- RSOHD0	117, 19, 118, 209	V02, W01, W02, W03	O LVTTL	Receive TOH data output 4-bit bus. This 4-bit data bus outputs receive TOH data. It starts output of the receive SOH data onto RSOHD starting from the clock cycle next to that in which RSOHFP is output.
RSOHAV	20	Y01	O LVTTL	Receive TOH data validity indication signal output. This signal indicates that valid receive TOH data is output to RSOHD. In the clock cycle in which valid data is output to RSOHD, RSOHAV goes high. In the clock cycle in which valid data is not output, RSOHAV goes low.
RPOHCK	290	U04	O LVTTL	Receive POH interface clock output (576 kHz). This pin outputs a 576-kHz clock obtained by internally dividing receive clock RCLK (155.52 MHz) by 270. RPOHFP and RPOHAV are output in sync with this divided clock.
RPOHFP	18	V01	O LVTTL	Receive POH frame pulse output. This signal goes high one cycle before the clock cycle in which output of receive POH data is started.
RPOHD	116	U02	O LVTTL	Receive POH data output. This pin outputs serial receive POH data. It outputs the receive POH data to RPOHD as one byte in eight clock cycles, starting from the clock cycle next to that in which RPOHFP is output.
RPOHAV	207	U03	O LVTTL	Receive POH data validity indication signal output. This signal indicates that valid receive POH data has been output to RPOHD. In a clock cycle in which valid data is output to RPOHD, RPOHAV goes high; in a cycle in which valid data is not output, it goes low.

1.5 General-Purpose I/O Port

Pin Name	Serial No.	Address No.	I/O, Level	Function
PIN2	123	AD02	I LVTTL (Internal pull-down)	General-purpose input port. These are general-purpose input pins that input the state signals of external peripheral devices. The signal levels of these pins are reflected on the bits of the internal GPSR register. Changes in the statuses of these bits can be used as interrupt causes. **Caution Of PIN2 to PIN0, only PIN2 is not a 5-V tolerant pin.**
PIN1, PIN0	27, 125	AF02, AE03	I LVTTL (5V tolerant/ Internal pull-down)	
POUT4- POUT0	24, 213, 29, 48, 73	AD01, AC03, AF04, AF23, D26	O LVTTL	General-purpose output port. The setting of the bits of the internal POUTR register are output to these pins as signal levels. These pins can be used to control external peripheral devices.

1.6 Alarm Signal Input/Output

Pin Name	Serial No.	Address No.	I/O, Level	Function
B1ERS, B2ERS, LAISS, LCDS, LOFS, LOPS, LOSS, LRDIS, OOFS, PAISS, PRDIS	314, 145, 52, 149, 316, 236, 148, 234, 53, 146, 49	AC22, AE23, AE26, AC25, AB23, AC24, AD25, AD23, AD26, AE24, AF24	O LVTTL	Alarm signal output. If the μPD98414 detects an event such as a fault or alarm at the reception side, it sets the corresponding bit of the internal ESTR register. One of these alarm signals goes high to post notification of the occurrence of the event to an external device. If the event is cleared and the bit of the ESTR register is reset, the signal goes low.
TLAIS, TLRDI, TPAIS, TPRDI	233, 28, 126, 297	AD22, AF03, AE04, AC05	I LVTTL (5V tolerant/ Internal pull-down)	Alarm transmit command input. While any of these signals goes high, the corresponding alarm frame (Line AIS, Line RDI, Path AIS, or Path RDI) is transmitted. The transmission of an alarm frame can also be specified by setting the CMR1 register.

1.7 JTAG Boundary Scan

Pin Name	Serial No.	Address No.	I/O, Level	Function
JCK	191	B04	I LVTTL (5V tolerant)	Boundary scan clock input. Ground this pin when not used.
JDI	99	A03	I LVTTL (5V tolerant)	Boundary scan data input. Ground this pin when not used.
JDO	352	D05	O LVTTL 3-state (5V tolerant)	Boundary scan data output. Open this pin when not used.
JMS	276	C04	I LVTTL (5V tolerant)	Boundary scan mode select signal input. Ground this pin when not used.
JRST_B	192	B03	I LVTTL (5V tolerant)	Boundary scan reset signal input. Ground this pin when not used.

★ **Remark** About the treatment of JTAG boundary scan pins for normal operation

A pulse input to the RESET_B pin does not reset the JTAG logic.

If the JTAG logic has not been reset, the μPD98414 may not operate normally. Either of the following two methods can be used to reset the JTAG logic. If the JRST_B pin is not connected to a ground, be sure to reset the JTAG logic, using either method, after the power is switched on.

- Resetting the JTAG logic without using the JRST_B pin

  Use the JMS and JCK pins to reset the JTAG logic and keep it reset (with the JRST_B pin pulled up).

  Fix the JMS pin at 1 (pulled up), and input five or more clock cycles to the JCK pin.

- Using the JRST_B pin to reset the JTAG logic

  If a low pulse is input to the JRST_B pin, and the JMS and JRST_B pins are pulled up and kept at a high level, the JTAG logic is kept reset, so it does not affect normal operations. As for the JDI and JCK pins, keep the input level pulled down or up.

1.8 Power and Grounding Pins

Pin Name	Serial No.	Address No.	I/O	Function
V_{DD}	10, 13, 16, 31, 33, 50, 56, 58, 90, 91, 93, 95, 100, 101, 104, 111, 124, 127, 132, 136, 143, 147, 150, 155, 159, 166, 170, 180, 186, 193, 197, 198, 199, 203, 208, 214, 219, 223, 224, 228, 229, 230, 235, 240, 244, 245, 249, 250, 251, 256, 261, 264, 266, 271, 274, 279, 283, 287, 289, 298, 307, 308, 317, 326, 327, 336, 344, 346	K01, N01, T01, AF06, AF08, AF25, AA26, W26, A12, A11, A09, A07, A02, B02, E02, M02, AE02, AE05, AE10, AE14, AE21, AE25, AB25, U25, N25, F25, B25, B15, B09, C03, G03, H03, J03, N03, V03, AD03, AD08, AD12, AD13, AD17, AD18, AD19, AD24, W24, R24, P24, K24, J24, H24, C24, C19, C16, C14, C09, C06, F04, K04, P04, T04, AC06, AC15, AC16, AA23, M23, L23, D21, D13, D11	–	Power supply pins (+3.3 ±5%)
GND	1, 7, 11, 14, 15, 25, 26, 32, 38, 40, 42, 47, 51, 54, 57, 63, 65, 67, 72, 75, 76, 86, 88, 89, 92, 96, 105, 110, 133, 140, 156, 163, 179, 185, 187, 196, 200, 205, 206, 217, 238, 268, 277, 281, 282, 284, 286, 291, 294, 296, 300, 302, 303, 305, 310, 311, 313, 315, 319, 321, 322, 324, 329, 330, 332, 334, 338, 341, 343, 348, 349, 351	A01, G01, L01, P01, R01, AE01, AF01, AF07, AF13, AF15, AF17, AF22, AF26, AC26, Y26, P26, M26, K26, E26, B26, A26, A16, A14, A13, A10, A06, F02, L02, AE11, AE18, T25, J25, B16, B10, B08, F03, K03, R03, T03, AD06, AA24, C12, D04, H04, J04, L04, N04, V04, AA04, AC04, AC08, AC10, AC11, AC13, AC18, AC19, AC21, AC23, W23, U23, T23, P23, J23, H23, F23, D23, D19, D16, D14, D09, D08, D06	–	Ground pins

1.9 Others

Pin Name	Serial No.	Address No.	I/O, Level	Function
IC	3, 4, 98, 103, 194, 254, 275, 278	C01, D01, A04, D02, D03, E24, C05, E04	–	Internal circuit connection test pins. These pins must be kept open.

1.10 Handling Unused Pins

Depending on the mode, some pins are not used. These pins must be handled as listed below.

Pin Name	Handling
IC	Leave open.
RCLK_N, TCLK_N	Ground.
RCLK_P, TCLK_P	Pulled up to 3.3 V.
RXPLD[15:0], TXPLD[15:0]	Pulled up to 3.3 V.
CD	Pulled up to 3.3 or 5 V.
RXCLK, RXENB_B, RXSEL_B, TXCLK, TXENB_B, TXSOC, TXSEL_B	Ground.
TXPRTY	Leave open.
CS_B	Pulled up to 3.3 or 5 V.
MADD[7:0] , DS_B, RW	Ground.
TSOHD[3:0], TSOHAV, TPOHD, TPOHAV,	Ground.
PIN[2:0]	Leave open.
TLAIS, TPAIS, TLRDI, TPRDI	Ground.
JCK, JMS, JDI, JRST_B	Ground.
Output pins	Leave open.

1.11 Initial States of Each Pin

Pin Name	During a Reset	Immediately After Reset	Receive framer function reset by CD pin = L
TPCLK_N/TPCLK_P	Not reset. Depends on TCLK_N/P input.		
TXPLD15-TXPLD0	L	L	
TCS	Not reset. Depends on TCLK_N/P input.		
RCS	L	L	
RXCLK_O	Not reset. Depends on RXCLK input.		
RXSOC	L	L	
RXCLAV	L	L	
RXPRTY	Outputs parity bit of RXDATA[31:0].		
RXDATA31-RXDATA0	L	L	
TXCLK_O	Not reset. Depends on TXCLK input.		
TXCLAV	L	L	
PHINT_B	H	H	
MD15-MD0	Input mode (undefined)		
ACK2S_B/RDY2S_B	H	H	
ACK3S_B/RDY3S_B	Hi-Z	Hi-Z	
TSOHCK	L	L	
TSOHFP	L	L	
TPOHCK	L	L	
TPOHFP	L	L	
RSOHCK	L	L	L
RSOHFP	L	L	L
RSOHD3-RSOHD0	L	L	L
RSOHAV	L	L	L
RPOHCK	L	L	L
RPOHFP	L	L	L
RPOHD	L	L	L
RPOHAV	L	L	L
POUT4-POUT0	L	L	
★ B1ERS, B2ERS, LAISS, LCDS, LOFS, LOPS, LOSS, LRDIS, OOFS, PAISS, PRDIS	L	Other than LOPS, OOFS : L LOPS, OOFS : H	LOSS, OOFS, LOFS: **Note** LOPS, LCDS: H B1ERS, B2ERS, LAISS, LRDIS, PAISS, PRDIS: L
JDO	Undefined	Undefined	

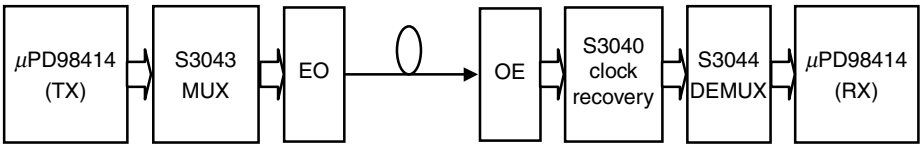
★ **Note** The detection circuits of LOS, OOF, and LOF are not reset when CD pin is set to L. The states of LOSS, OOFS, and LOFS pins depend on the input states of the line.

2. CONNECTION EXAMPLE OF MUX/DEMUX DEVICE

- **Recommended MUX/DEMUX device**

  Connecting the following MUX and DEMUX devices to the μPD98414 is recommended:

AMCC SONET/SDH OC-48	**16:1 TRANSMITTER**	**S3043**
	1:16 RECEIVER	**S3044**
	Clock Recovery	**S3040**



★ (The S3040 is unnecessary if the optical link module (OE) has a clock recovery function.)

- **Circuit connection example**

  Examples of connecting AMCC's S3043 and S3044 are shown below.

Figure 2-1. Example of Connecting μPD98414 and S3043 (Transmission Circuit)

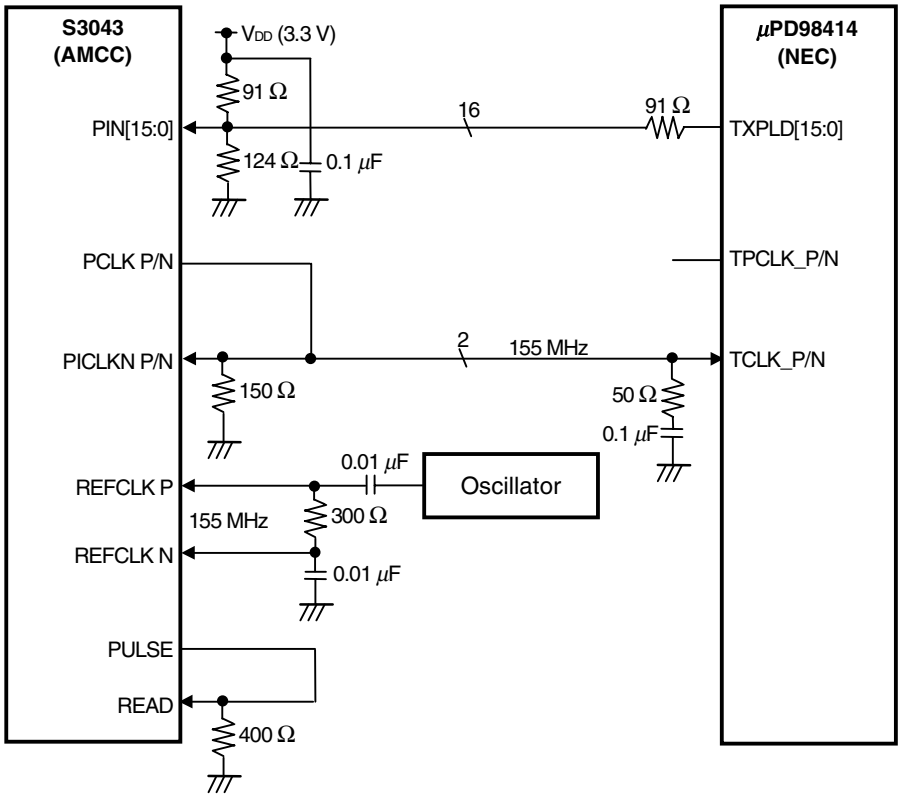
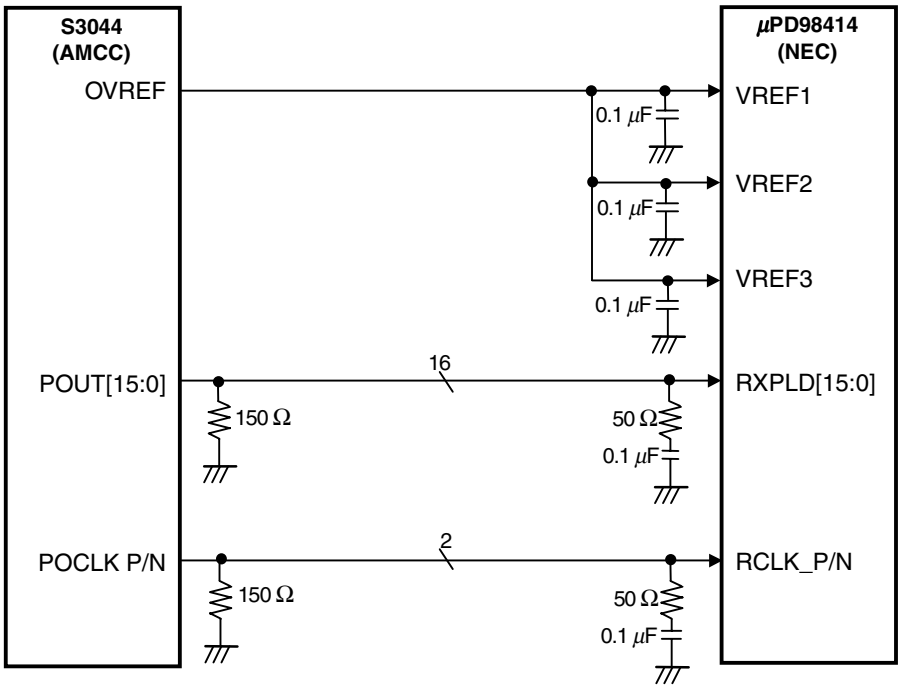


Figure 2-2. Example of Connecting μPD98414 and S3044 (Reception Circuit)



3. ELECTRIC CHARACTERISTICS

When seeing "Absolute Maximum Ratings," "Recommended Operating Conditions," or "DC Characteristics," see also "Pin Classifications" described below.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}		−0.5 to +4.6	V
Input/output voltage	V_{I1}/V_{O1}	LVTTL level	−0.5 to +4.6	V
	V_{I2}/V_{O2}	LVTTL level, 5-V tolerant pin	−0.5 to +6.6	V
	V_{I3}/V_{O3}	PECL-level pin	−0.5 to +4.6	V
Output current	I_{O1}	I_{OL} = 6 mA	20	mA
	I_{O2}	I_{OL} = 9 mA	30	mA
	I_{O3}	I_{OL} = 12 mA	40	mA
	I_{O4}	I_{OL} = 18 mA	60	mA
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

RECOMMENDED OPERATING CONDITIONS

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	Power supply voltage	V_{DD}		3.135	3.3	3.465	V
	Operating ambient temperature	T_A		−40		+85	°C
	High-level input voltage	V_{IH1}	LVTTL-level pin	2.4		V_{DD}	V
		V_{IH2}	LVTTL level, 5-V tolerant pin	2.0		5.0	V
★		V_{IH3}	PECL-level pin (single-ended)	V_{IREF} + 0.15		V_{DD}	V
★		V_{IH4}	PECL-level pin (differential)	V_{DD}−1.2		V_{DD}−0.55	V
	Low-level input voltage	V_{IL1}	LVTTL-level pin	0		0.8	V
		V_{IL2}	LVTTL level, 5-V tolerant pin	0		0.8	V
★		V_{IL3}	PECL-level pin (single-ended)	0		V_{IREF}−0.15	V
★		V_{IL4}	PECL-level pin (differential)	V_{DD}−2.0		V_{DD}−1.4	V
	VREF1-VREF3 pin input voltage	V_{IREF}		V_{DD}/2−0.5		V_{DD}/2+0.5	V
★	PECL differential input voltage	V_{IDFF}	PECL-level pin (differential)	300			mV

Caution Make sure that the product is air-cooled at a velocity of at least 1 m/s during operation.

★ DC CHARACTERISTICS (T_A = –40°C to +85°C, V_{DD} = 3.3 ±5%)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Off-state output current	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
	Input leakage current	I_{LI}	$V_I = V_{DD}$ or GND			±10	μA
	Low-level output current	I_{OL1}	LVTTL-level pin	6			mA
		I_{OL2}	V_{OL} = 0.4 V	12			mA
		I_{OL3}		18			mA
		I_{OL4}	LVTTL level, 5-V tolerant pin	6			mA
		I_{OL5}	V_{OL} = 0.4 V	9			mA
	High-level output current	I_{OH1}	LVTTL-level pin	–6			mA
		I_{OH2}	V_{OH} = 2.4 V	–12			mA
		I_{OH3}		–18			mA
		I_{OH4}	LVTTL level, 5-V tolerant pin	–2			mA
		I_{OH5}	V_{OH} = 2.4 V	–2			mA
	Low-level output voltage	V_{OL1}	LVTTL-level pin, I_{OL} = 0 mA			0.1	V
		V_{OL2}	LVTTL level, 5-V tolerant pin, I_{OL} = 0 mA			0.1	V
★		V_{OL3}	PECL-level pin, I_{OL} = 0 mA When terminated as shown in Figure 2-1.	0.37 × V_{DD}		0.45 × V_{DD}	V
	High-level output voltage	V_{OH1}	LVTTL-level pin, I_{OH} = 0 mA	V_{DD}–0.1			V
		V_{OH2}	LVTTL level, 5-V tolerant pin, I_{OH} = 0 mA	V_{DD}–0.2			V
★		V_{OH3}	PECL-level pin, I_{OH} = 0 mA When terminated as shown in Figure 2-1.	0.66 × V_{DD}		0.75 × V_{DD}	V
★	Supply current	I_{DD}	Normal operation		1.05	1.3	A

CAPACITANCE

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output capacitance	C_O	Frequency = 1 MHz		7	10	pF
Input capacitance	C_I	Frequency = 1 MHz		7	10	pF
I/O capacitance	C_{IO}	Frequency = 1 MHz		7	10	pF

PIN CLASSIFICATIONS

- Input pins

Category			Applicable Pins	Number of Pins
LVTTL-level pin	V_{I1} V_{IH1} V_{IL1}	With pull-up	TXPRTY	1
		With pull-down	PIN2	1
		–	RXCLK, RXENB_B, RXDEL_B, TXCLK, TXDATA[31:0], TXENB_B, TXSEL_B, TXSOC	39
LVTTL level 5-V tolerant pin	V_{I2} V_{IH2} V_{IL2}	With pull-down	PIN0, PIN1, TLAIS, TLRDI, TPAIS, TPOHAV, TPOHD, TPRDI, TSOHAV, TSOHD[3:0]	13
		3-state	MD15-MD0	16
		–	BMODE, CD, CS_B, DS_B/RD_B, MADD[7:0], RESET_B, RW/WR_B, JCK, JDI, JMS, JRST_B	18
★ PECL-level pin (single-ended)	V_{I3} V_{IH3} V_{IL3}	–	RXPLD[15:0]	16
★ PECL-level pin (differential)	V_{I3} V_{IH4} V_{IL4} V_{IDFF}	–	RCLK_P, RCLK_N, TCLK_P, TCLK_N	4

Caution Of general-purpose input pins PIN2 to PIN0, only pin PIN2 is not 5-V tolerant.

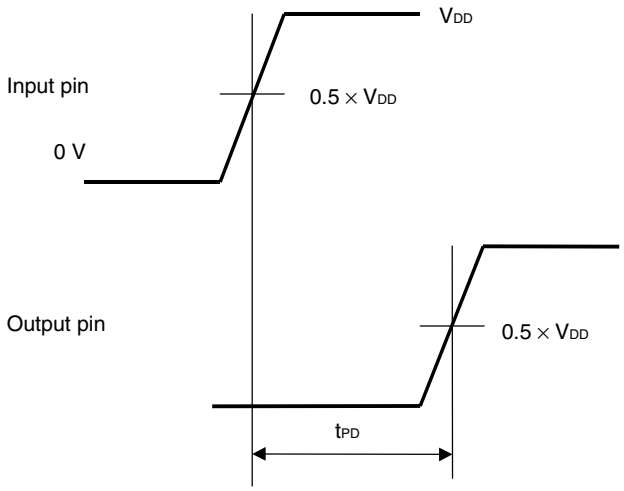
- Output pins

Category				Applicable Pins	Number of Pins
LVTTL-level pin	V_{O1} V_{OL1}/V_{OH1}	I_{OL1}/I_{OH1}	I_{O1}	B1ERS, B2ERS, LAISS, LCDS, LOFS, LOPS, LOSS, LRDIS, OOFS, PAISS, POUT[4:0], PRDIS, RPOHAV, RPOHCK, RPOHD, RPOHFP, RSOHAV, RSOHCK, RSOHD[3:0], RSOHFP, TPOHCK, TPOHFP, TSOHCK, TSOHFP	31
		I_{OL2}/I_{OH2}	I_{O3}	RCS, RXCLAV, RXDATA[31:0], RXPRTY, RXSOC, TCS, TXCLAV	38
		I_{OL3}/I_{OH3}	I_{O4}	RXCLK_O, TXCLK_O	2
LVTTL level 5-V tolerant pin	V_{O2} V_{OL2}/V_{OH2}	I_{OL4}/I_{OH4}	I_{O1}	JDO	1
		I_{OL5}/I_{OH5}	I_{O2}	ACK3S_B/RDY3S_B, ACK2S_B/RDY3S_B, PHINT_B, MD[15:0] (3-state)	19
★ PECL-level pin (single-ended)	V_{O3} V_{OL3}/V_{OH3}	–	I_{O2}	TXPLD[15:0]	16
★ PECL-level pin (differential)	V_{O3} V_{OL3}/V_{OH3}	–	I_{O2}	TPCLK_P, TPCLK_N	2

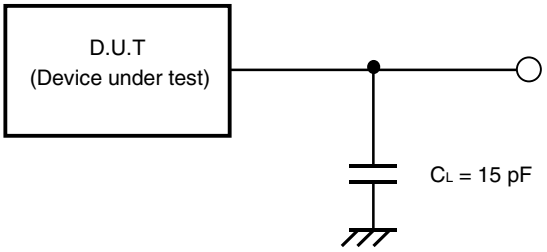
★ AC CHARACTERISTICS (T_A = –40°C to +85°C, V_{DD} = 3.3 ±5%)

AC Test Conditions

- **Delay time definition**



- **Load definition**



(1) RESET_B input

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RESET_B pulse width	t_{WRST}		100			ns

(2) Management interface

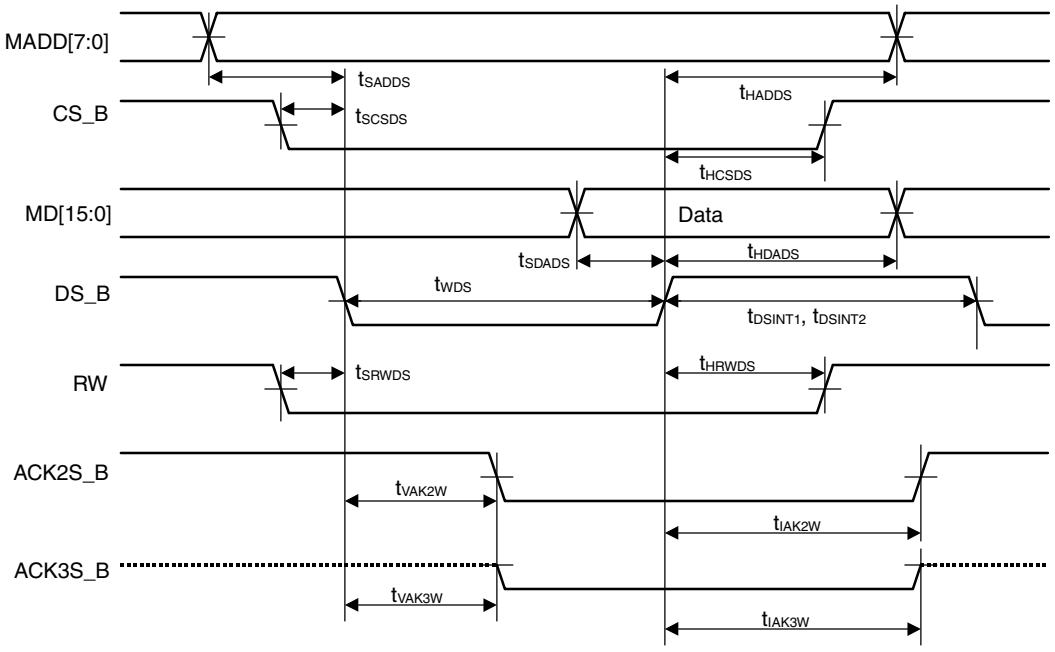
(a) Write timing (BMODE = 0)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Address setup time (referred to DS_B↓)	t_{SADDS}		10			ns
	CS_B setup time (referred to DS_B↓)	t_{SCSDS}		5			ns
	RW setup time (referred to DS_B↓)	t_{SRWDS}		5			ns
	Data setup time (referred to DS_B↑)	t_{SDADS}		15			ns
	Address hold time (referred to DS_B↑)	t_{HADDS}		4			ns
★	CS_B hold time (referred to DS_B↑)	t_{HCSDS}		1			ns
★	RW hold time (referred to DS_B↑)	t_{HRWDS}		1			ns
	Data hold time (referred to DS_B↑)	t_{HDADS}		4			ns
★	Delay from DS_B↓ to ACK2S_B output	t_{VAK2W}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from DS_B↓ to ACK3S_B output	t_{VAK3W}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from DS_B↑ to ACK2S_B float	t_{IAK2W}	**Note**	0		10	ns
★	Delay from DS_B↑ to ACK3S_B float	t_{VAK3W}		0		10	ns
	DS_B pulse width	t_{WDS}		50			ns
★	Minimum interval (1) from DS_B↑ to DS_B↓	t_{DSINT1}		40			ns
	Minimum interval (2) from DS_B↑ to DS_B↓	t_{DSINT2}		150			ns

Note t_{DSINT2} is a minimum interval when the following registers are continuously accessed. A shorter interval for continuous access will cause the ACK2S_B (ACK3S_B) output delay to exceed the maximum value of t_{VAK2W} (t_{VAK3W}).

t_{DSINT1} is a value when a register other than the following registers is accessed, or when one of the following registers is first accessed.

Registers: RJ0ARR, RJ0APR, RJ0BRR, RJ0BPR, RJ1ARR, RJ1APR, RJ1BRR, RJ1BPR,
TJ0ARR, TJ0APR, TJ0BRR, TJ0BPR, TJ1ARR, TJ1APR, TJ1BRR, TJ1BPR



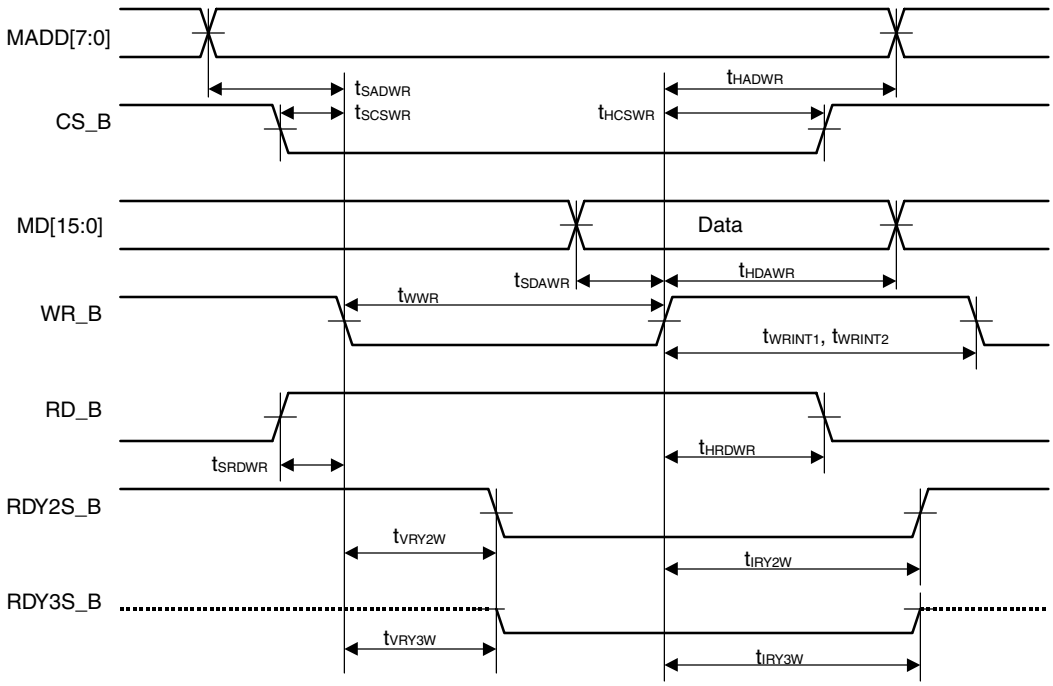
(b) Write timing (BMODE = 1)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Address setup time (referred to WR_B↓)	t_{SADWR}		10			ns
	CS_B setup time (referred to WR_B↓)	t_{SCSWR}		5			ns
	RD_B setup time (referred to WR_B↓)	t_{SRDWR}		5			ns
	Data setup time (referred to WR_B↑)	t_{SDAWR}		15			ns
	Address hold time (referred to WR_B↑)	t_{HADWR}		4			ns
★	CS_B hold time (referred to WR_B↑)	t_{HCSWR}		1			ns
★	RD_B hold time (referred to WR_B↑)	t_{HRDWR}		40			ns
	Data hold time (referred to WR_B↑)	t_{HDAWR}		4			ns
★	Delay from WR_B↓ to RDY2S_B output	t_{VRY2W}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from WR_B↓ to RDY3S_B output	t_{VRY3W}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from WR_B↑ to RDY2S_B float	t_{IRY2W}	**Note**	0		10	ns
★	Delay from WR_B↑ to RDY3S_B float	t_{IRY3W}		0		10	ns
	WR_B pulse width	t_{WWR}		50			ns
★	Minimum interval (1) from WR_B↑ to WR_B↓	t_{WRINT1}		40			ns
	Minimum interval (2) from WR_B↑ to WR_B↓	t_{WRINT2}		150			ns

Note t_{WRINT2} is a minimum interval when the following registers are continuously accessed. A shorter interval for continuous access will cause the RDY2S_B (RDY3S_B) output delay to exceed the maximum value of t_{VRY2W} (t_{VRY3W}).

t_{WRINT1} is a value when a register other than the following registers is accessed, or when one of the following registers is first accessed.

Registers: RJ0ARR, RJ0APR, RJ0BRR, RJ0BPR, RJ1ARR, RJ1APR, RJ1BRR, RJ1BPR,
TJ0ARR, TJ0APR, TJ0BRR, TJ0BPR, TJ1ARR, TJ1APR, TJ1BRR, TJ1BPR



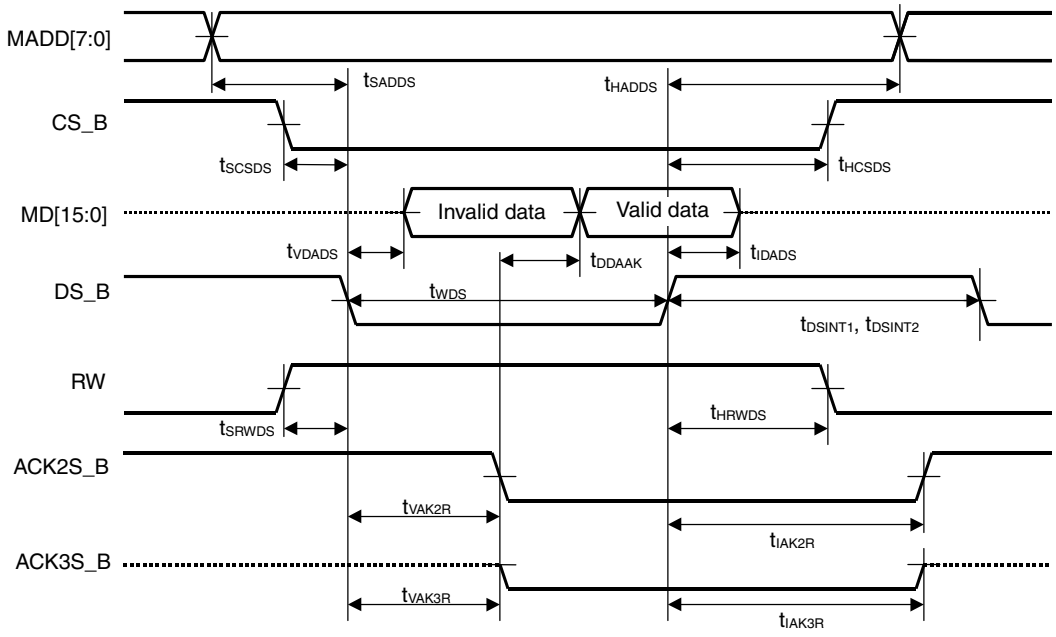
(c) Read timing (BMODE = 0)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Address setup time (referred to DS_B↓)	t_{SADDS}		10			ns
	CS_B setup time (referred to DS_B↓)	t_{SCSDS}		5			ns
	RW setup time (referred to DS_B↓)	t_{SRWDS}		5			ns
	Address hold time (referred to DS_B↑)	t_{HADDS}		4			ns
★	CS_B hold time (referred to DS_B↑)	t_{HCSDS}		1			ns
★	RW hold time (referred to DS_B↑)	t_{HRWDS}		1			ns
★	Delay from DS_B↓ to ACK2S_B output	t_{VAK2R}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from DS_B↓ to ACK3S_B output	t_{VAK3R}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from DS_B↓ to data output	t_{VDADS}	**Note**	0		22	ns
★	Delay from DS_B↑ to ACK2S_B float	t_{IAK2R}		0		10	ns
★	Delay from DS_B↑ to ACK3S_B float	t_{IAK3R}		0		10	ns
	Delay from DS_B↑ to data float	t_{IDADS}		3		22	ns
★	Delay from ACK2S_B[ACK3S_B]↓ to data output	t_{DDAAK}				20	ns
	DS_B pulse width	t_{WDS}		50			ns
★	Minimum interval (1) from DS_B↑ to DS_B ↓	t_{DSINT1}		40			ns
	Minimum interval (2) from DS_B↑ to DS_B ↓	t_{DSINT2}		150			ns

Note t_{DSINT2} is a minimum interval when the following registers are continuously accessed. A shorter interval for continuous access will cause the ACK2S_B (ACK3S_B) output delay to exceed the maximum value of t_{VAK2R} (t_{VAK3R}).

t_{DSINT1} is a value when a register other than the following registers is accessed, or when one of the following registers is first accessed.

Registers: RJ0ARR, RJ0APR, RJ0BRR, RJ0BPR, RJ1ARR, RJ1APR, RJ1BRR, RJ1BPR, TJ0ARR, TJ0APR, TJ0BRR, TJ0BPR, TJ1ARR, TJ1APR, TJ1BRR, TJ1BPR



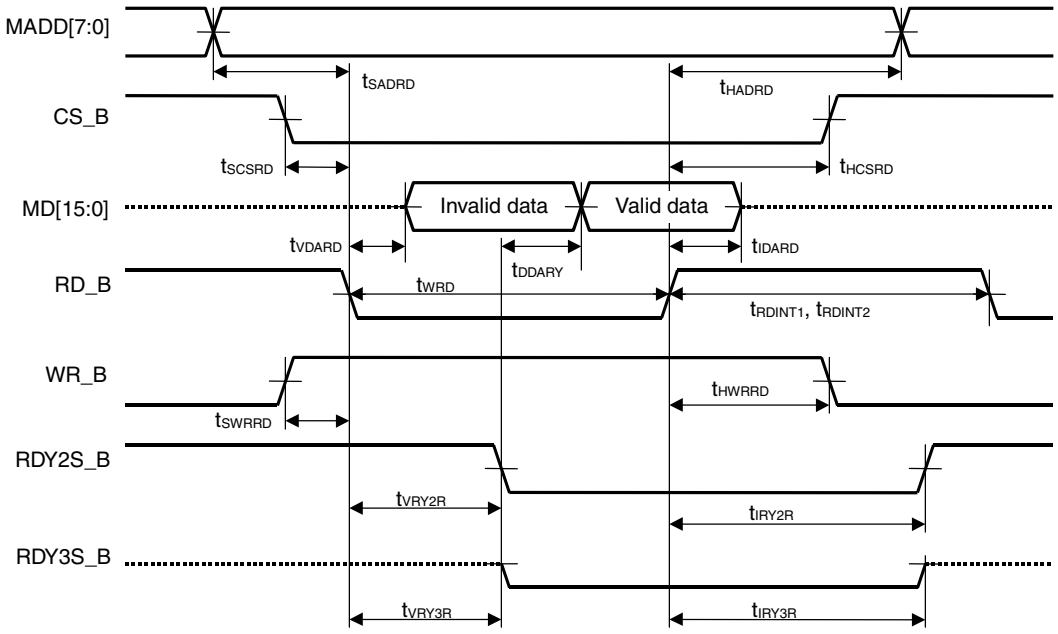
(d) Read timing (BMODE = 1)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Address setup time (referred to RD_B↓)	t_{SADRD}		10			ns
	CS_B setup time (referred to RD_B↓)	t_{SCSRD}		5			ns
	WR_B setup time (referred to RD_B↓)	t_{SWRRD}		5			ns
	Address hold time (referred to RD_B↑)	t_{HADRD}		4			ns
★	CS_B hold time (referred to RD_B↑)	t_{HCSRD}		1			ns
★	WR_B hold time (referred to RD_B↑)	t_{HWRRD}		40			ns
★	Delay from RD_B↓ to RDY2S_B output	t_{VRY2R}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from RD_B↓ to RDY3S_B output	t_{VRY3R}	Load capacitance = 15 pF, **Note**	0		10	ns
★	Delay from RD_B↓ to data output	t_{VDARD}	**Note**	0		22	ns
★	Delay from RD_B↑ to RDY2S_B float	t_{IRY2R}		0		10	ns
★	Delay from RD_B↑ to RDY3S_B float	t_{IRY3R}		0		10	ns
	Delay from RD_B↑ to data float	t_{IDARD}		3		22	ns
★	Delay from RDY2S_B[RDY3S_B]↓ to data output	t_{DDARY}				20	ns
	RD_B pulse width	t_{WRD}		50			ns
★	Minimum interval (1) from RD_B↑ to RD_B↓	t_{RDINT1}		40			ns
	Minimum interval (2) from RD_B↑ to RD_B↓	t_{RDINT2}		150			ns

Note t_{RDINT2} is a minimum interval when the following registers are continuously accessed. A shorter interval for continuous access will cause the RDY2S_B (RDY3S_B) output delay to exceed the maximum value of t_{VRY2R} (t_{VRY3R}).

t_{RDINT1} is a value when a register other than the following registers is accessed, or when one of the following registers is first accessed.

Registers: RJ0ARR, RJ0APR, RJ0BRR, RJ0BPR, RJ1ARR, RJ1APR, RJ1BRR, RJ1BPR, TJ0ARR, TJ0APR, TJ0BRR, TJ0BPR, TJ1ARR, TJ1APR, TJ1BRR, TJ1BPR



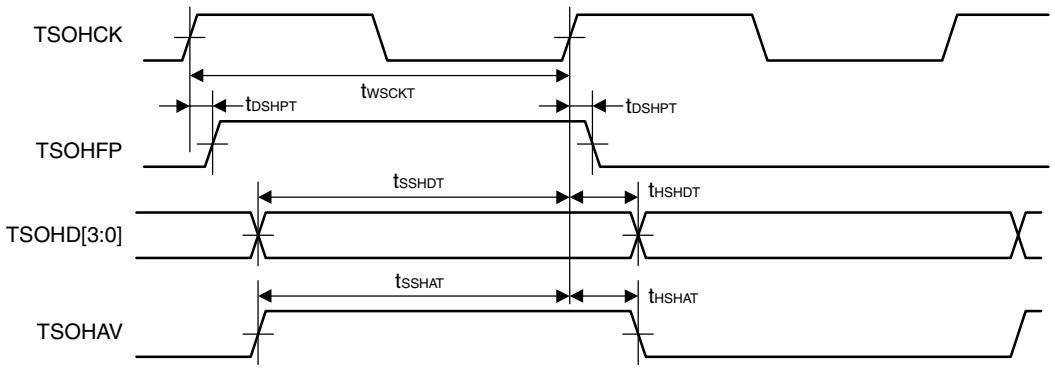
(3) Overhead interface

(a) Insert

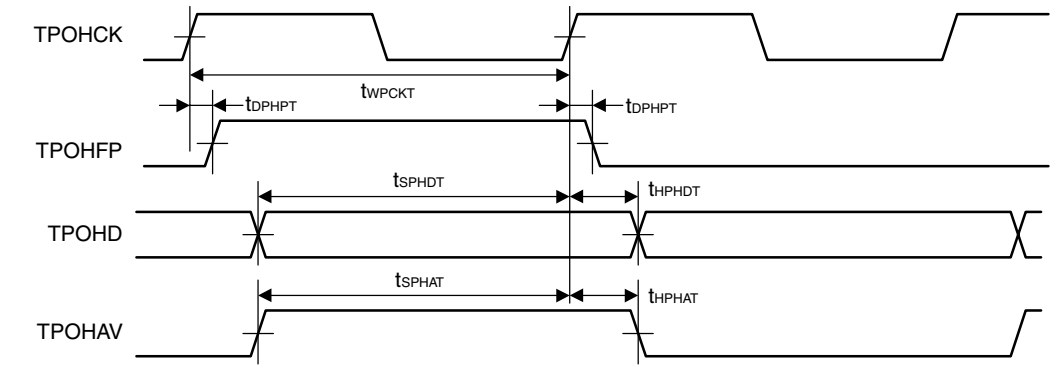
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	TSOHCK frequency	f_{WSCKT}	**Note**		25.92		MHz
	TSOHCK cycle time	t_{WSCKT}	**Note**		38.6		ns
★	Delay from TSOHCK↑ to TSOHFP output	t_{DSHPT}	Load capacitance: 15 pF	−6		+6	ns
	TSOHD setup time (referred to TSOHCK↑)	t_{SSHDT}		20			ns
	TSOHD hold time (referred to TSOHCK↑)	t_{HSHDT}		2			ns
	TSOHAV setup time (referred to TSOHCK↑)	t_{SSHAT}		20			ns
	TSOHAV hold time (referred to TSOHCK↑)	t_{HSHAT}		2			ns
	TPOHCK frequency	f_{WPCKT}	**Note**		576		kHz
	TPOHCK cycle time	t_{WPCKT}	**Note**		1.74		μs
★	Delay from TPOHCK↑ to TPOHFP output	t_{DPHPT}	Load capacitance: 15 pF	−6		+6	ns
	TPOHD setup time (referred to TPOHCK↑)	t_{SPHDT}		10			ns
	TPOHD hold time (referred to TPOHCK↑)	t_{HPHDT}		5			ns
	TPOHAV setup time (referred to TPOHCK↑)	t_{SPHAT}		10			ns
	TPOHAV hold time (referred to TPOHCK↑)	t_{HPHAT}		5			ns

★ **Note** TSOHCK and TPOHCK are divided clocks of TCLK_P/N.

TOH insert



POH insert

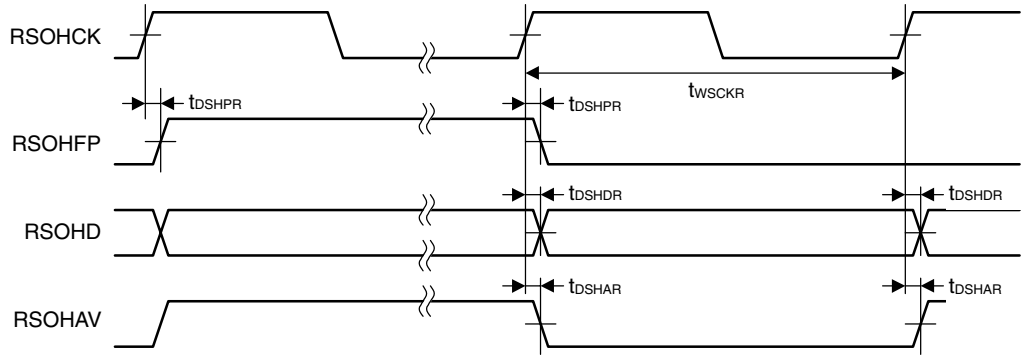


(b) Extract

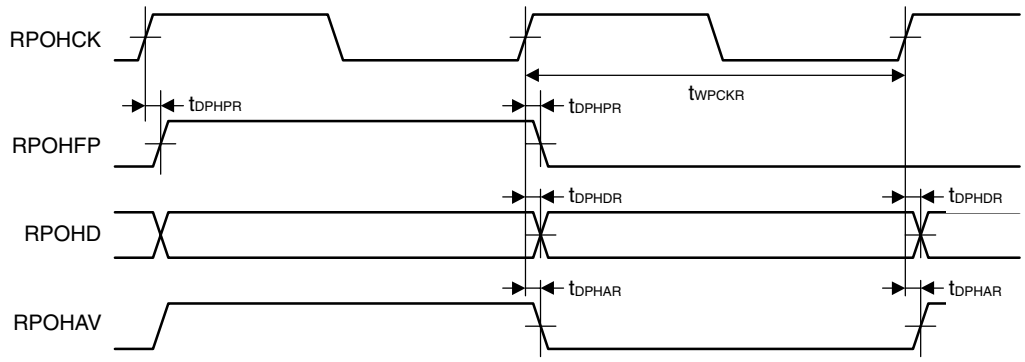
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	RSOHCK frequency	f_{WSCKR}	**Note**		25.92		MHz
	RSOHCK cycle time	t_{WSCKR}	**Note**		38.6		ns
★	Delay from RSOHCK↑ to RSOHFP output	t_{DSHPR}	Load capacitance: 15 pF	–3		+3	ns
★	Delay from RSOHCK↑ to RSOHDT output	t_{DSHDR}	Load capacitance: 15 pF	–3		+3	ns
★	Delay from RSOHCK↑ to RSOHAV output	t_{DSHAR}	Load capacitance: 15 pF	–3		+3	ns
	RPOHCK frequency	f_{WPCKR}	**Note**		576		kHz
	RPOHCK cycle time	t_{WPCKR}	**Note**		1.74		μs
★	Delay from RPOHCK↑ to RPOHFP output	t_{DPHPR}	Load capacitance: 15 pF	–3		+3	ns
★	Delay from RPOHCK↑ to RPOHDT output	t_{DPHDR}	Load capacitance: 15 pF	–3		+3	ns
★	Delay from RPOHCK↑ to RPOHAV output	t_{DPHAR}	Load capacitance: 15 pF	–3		+3	ns

★ **Note** RSOHCK and RPOHCK are divided clocks of RCLK_P/N.

TOH extract



POH extract

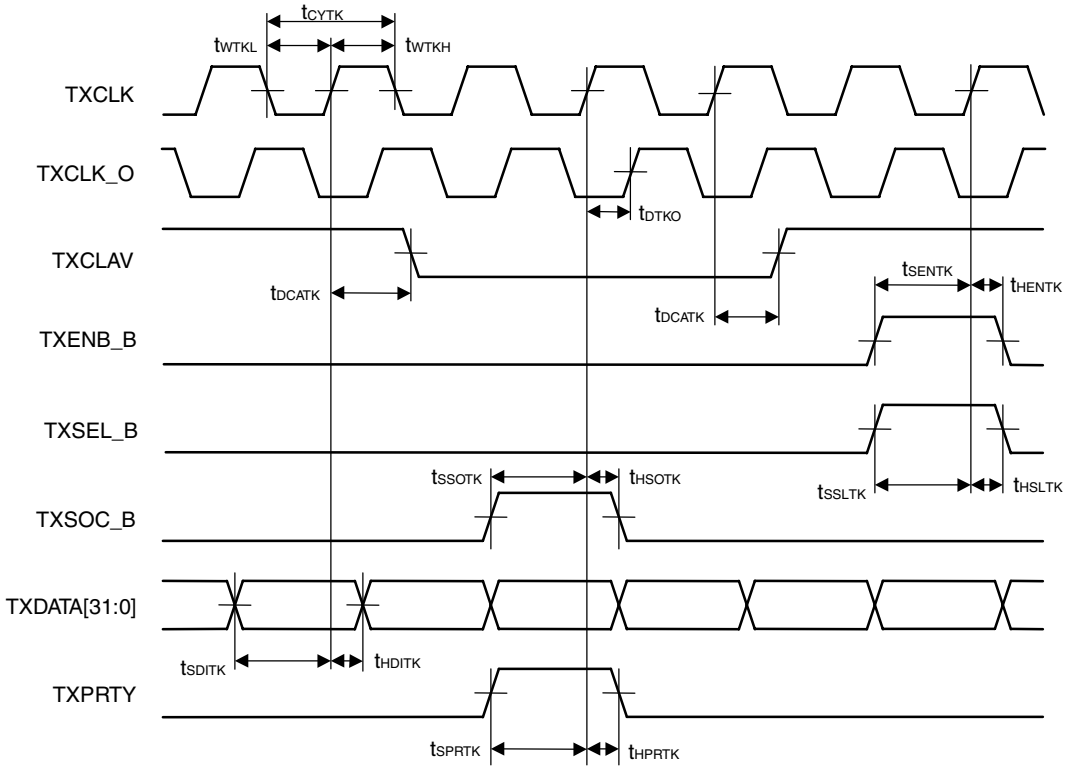


(4) ATM layer interface

(a) Transmit ATM layer interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TXCLK frequency	f_{CYTK}		8		104	MHz
TXCLK cycle time	t_{CYTK}		9.6		125	ns
★ TXCLK high level width	t_{WTKH}		3.9			ns
★ TXCLK low level width	t_{WTKL}		3.9			ns
★ Delay from TXCLK↑ to TXCLK_O output	t_{DTKO}	Load capacitance: 15 pF,**Note**	0.5		6	ns
★ Delay from TXCLK↑ to TXCLAV output	t_{DCATK}	Load capacitance: 15 pF	0.5		6	ns
★ TXDATA[31:0] setup time (referred to TXCLK↑)	t_{SDITK}		2.8			ns
★ TXDATA[31:0] hold time (referred to TXCLK↑)	t_{HDITK}		0.5			ns
★ TXSOC setup time (referred to TXCLK↑)	t_{SSOTK}		2.8			ns
★ TXSOC hold time (referred to TXCLK↑)	t_{HSOTK}		0.5			ns
★ TXPRTY setup time (referred to TXCLK↑)	t_{SPRTK}		2.8			ns
★ TXPRTY hold time (referred to TXCLK↑)	t_{HPRTK}		0.5			ns
★ TXENB_B setup time (referred to TXCLK↑)	t_{SENTK}		2.8			ns
★ TXENB_B hold time (referred to TXCLK↑)	t_{HENTK}		0.5			ns
★ TXSEL_B setup time (referred to TXCLK↑)	t_{SSLTK}		2.8			ns
★ TXSEL_B hold time (referred to TXCLK↑)	t_{HSLTK}		0.5			ns

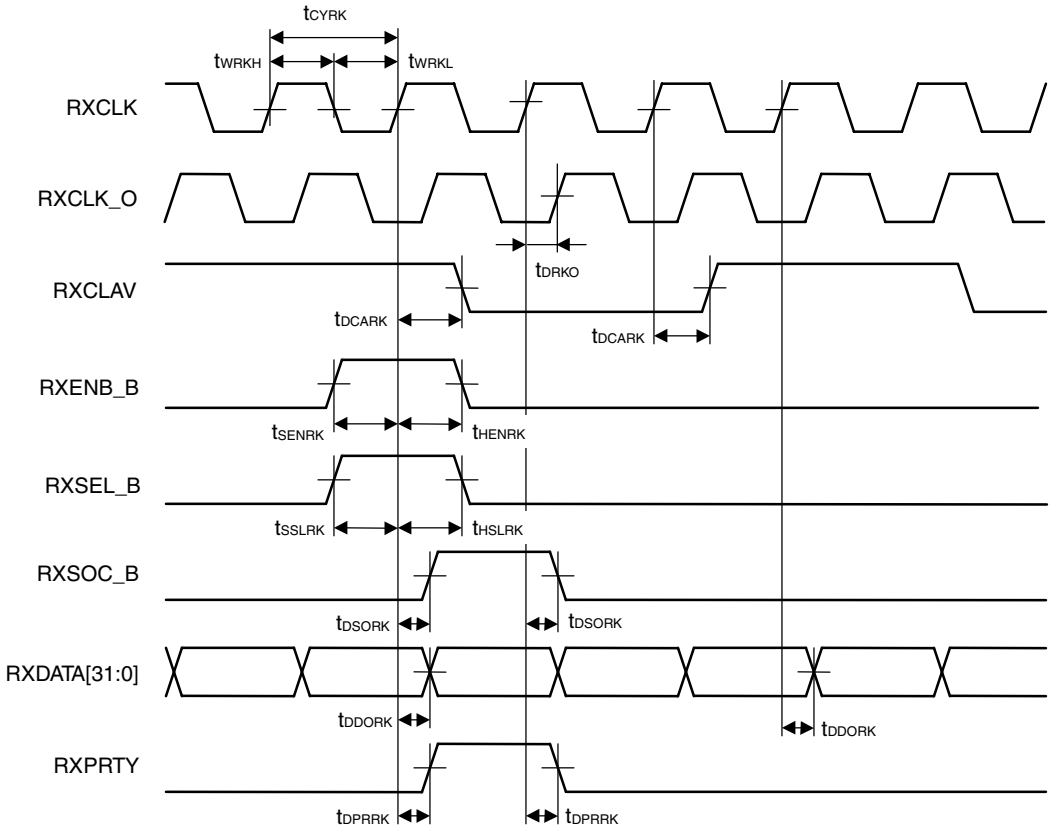
★ **Note** TXCLK_O is logic inversion output of TXCLK.



(b) Recieve ATM layer interface

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	RXCLK frequency	f_{CYRK}		8		104	MHz
	RXCLK cycle time	t_{CYRK}		9.6		125	ns
★	RXCLK high level width	t_{WRKH}		3.9			ns
★	RXCLK low level width	t_{WRKL}		3.9			ns
★	Delay from RXCLK↑ to RXCLK_O output	t_{DRKO}	Load capacitance: 15 pF,**Note**	0.5		6	ns
★	Delay from RXCLK↑ to RXCLAV output	t_{DCARK}	Load capacitance: 15 pF	0.5		6	ns
★	Delay from RXCLK↑ to RXDATA[31:0] output	t_{DDORK}	Load capacitance: 15 pF	0.5		6	ns
★	Delay from RXCLK↑ to RXSOC output	t_{DSORK}	Load capacitance: 15 pF	0.5		6	ns
★	Delay from RXCLK↑ to RXPRTY output	t_{DPRRK}	Load capacitance: 15 pF	0.5		6	ns
★	RXENB_B setup time (referred to RXCLK↑)	t_{SENRK}		2.8			ns
★	RXENB_B hold time (referred to RXCLK↑)	t_{HENRK}		0.5			ns
★	RXSEL_B setup time (referred to RXCLK↑)	t_{SSLRK}		2.8			ns
★	RXSEL_B hold time (referred to TXCLK↑)	t_{HSLRK}		0.5			ns

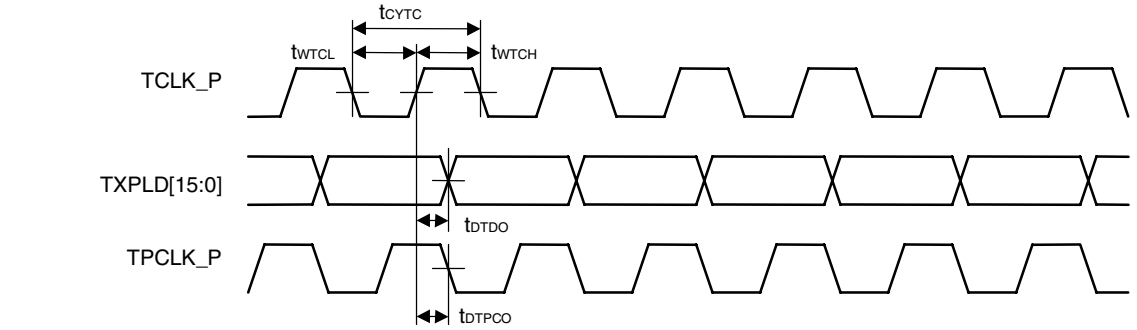
★ **Note** RXCLK_O is logic inversion output of RXCLK.



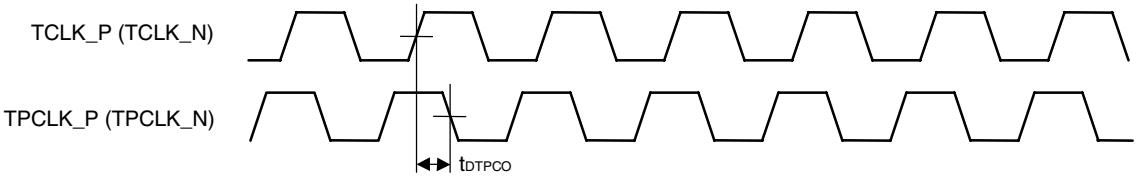
(5) Line interface

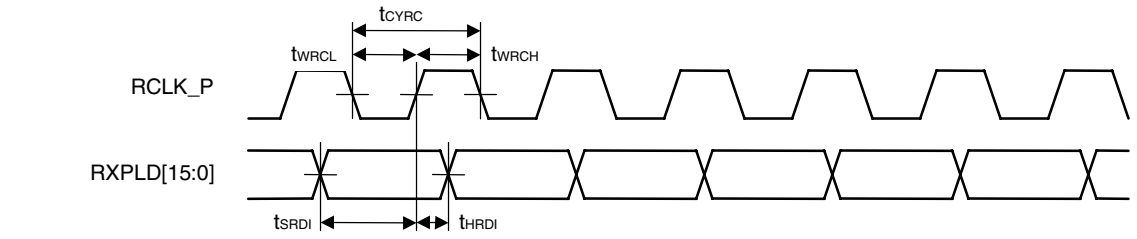
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	TCLK_P[TCLK_N] frequency	f_{CYTC}			155.52		MHz
	TCLK_P[TCLK_N] cycle time	t_{CYTC}			6.43		ns
★	TCLK_P[TCLK_N] high level width	t_{WTCH}		2.6			ns
★	TCLK_P[TCLK_N] low level width	t_{WTCL}		2.6			ns
★	RCLK_P[RCLK_N] frequency	f_{CYRC}			155.52		MHz
	RCLK_P[RCLK_N] cycle time	t_{CYRC}			6.43		ns
★	RCLK_P[RCLK_N] high level width	t_{WRCH}		2.6			ns
★	RCLK_P[RCLK_N] low level width	t_{WRCL}		2.6			ns
★	Delay from TCLK_P↑ to TXPLD[15:0]	t_{DTDO}		0.5		4.0	ns
★	Delay from TCLK_P[TCLK_N]↑ to TPCLK_P[TPCLK_N]↓	t_{DTPCO}	**Note**	0.5		4.5	ns
★	RXPLD[15:0] setup time (referred to RXCLK↑)	t_{SRDI}		1.8			ns
	RXPLD[15:0] hold time (referred to RXCLK↑)	t_{HRDI}		0.5			ns

★ **Note** TPCLK_P, TPCLK_N are logic inversion outputs of TCLK_P, TCLK_N.



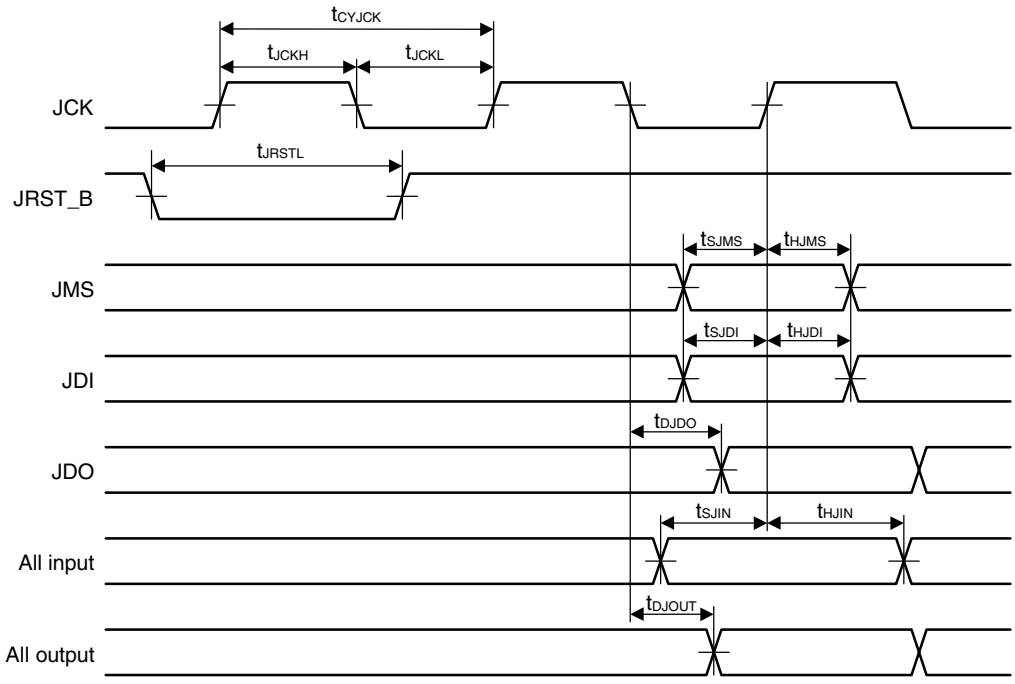
★





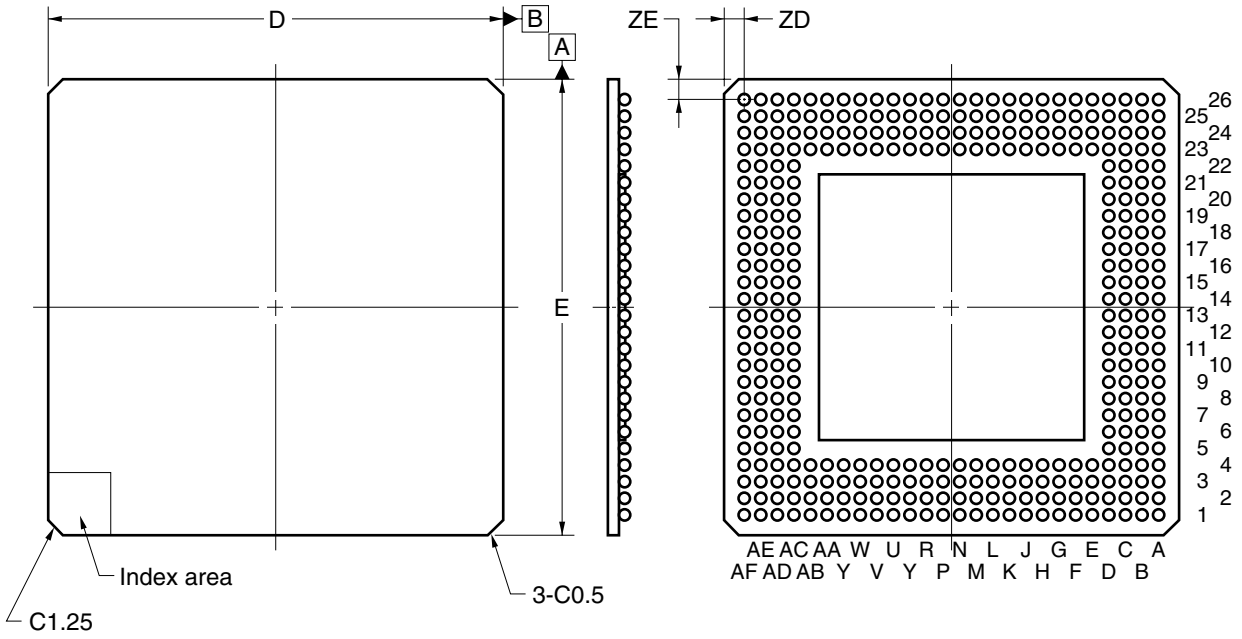
★ (6) JTAG boundary scan

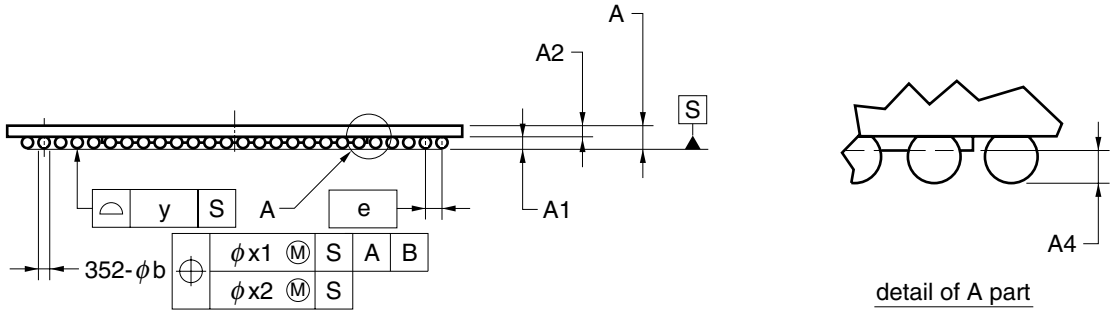
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
JCK cycle time	t_{CYJCK}		250			ns
JCK high level width	t_{JCKH}		100			ns
JCK low level width	t_{JCKL}		100			ns
JMS setup time	t_{SJMS}		30			ns
JMS hold time	t_{HJMS}		30			ns
JDI setup time	t_{SJDI}		30			ns
JDI hold time	t_{HJDI}		30			ns
Capture_DR data input setup time	t_{SJIN}		30			ns
Capture_DR data input hold time	t_{HJIN}		30			ns
Delay from JCK↓ to Up Date_DR output	t_{DJOUT}		0		50	ns
Delay from JCK↓ to JDO	t_{DJDO}		0		50	ns
JRST_B low level width	t_{JRSTL}		t_{CYJCK}			ns



4. PACKAGE DRAWING

352-PIN PLASTIC BGA (CAVITY DOWN ADVANCED TYPE) (35x35)





ITEM	MILLIMETERS
D	35.00±0.20
E	35.00±0.20
e	1.27
A	1.50±0.30
A1	0.60±0.10
A2	0.90
A4	0.25 MIN.
b	0.75±0.15
x1	0.30
x2	0.15
y	0.20
ZD	1.625
ZE	1.625

P352F2-127-RN1-1

5. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD98414.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Surface-Mount Type

- **μPD98414F2-RN1: 352-pin plastic BGA (cavity down advanced type) (35 × 35)**

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 220°C Reflow time: 30 seconds or less (210°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 2 days[Note] (20 hours of pre-baking is required at 125°C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR20-202-2

Note Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

NEASCOT-P70 is a trademark of NEC Corporation.

- **The information in this document is current as of July, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
  (Note)
  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4