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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD8894

5340 PIXELS × 3 + (10680 + 10680) PIXELS × 3
COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8894 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD8894 has 3 rows of 5340 pixels, and each row has a single-sided readout type of charge transfer register ,and has 3 rows of (10680 + 10680) staggered pixels, and each row has dual-sided readout type of charge transfer register.

And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 2400 dpi / A4 color image scanners.

FEATURES

- Valid photocell : 5340 pixels × 3 + (10680 + 10680) pixels × 3
- Photocell's pitch : 8 μm (600 dpi sensor) and 4 μm (2400 dpi sensor)
- Line spacing : (600 dpi sensor) 32 μm (4 lines) Red line - Green line, Green line - Blue line
  (2400 dpi sensor) 64 μm (16 lines) Red line - Green line, Green line - Blue line
  8 μm (2 lines) Odd line - Even line (for each color)
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 96 dot/mm A4 (210 × 297 mm) size (shorter side)
  2400 dpi US letter (8.5" × 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : (2400 dpi sensor) 10 MHz MAX ($f_{\phi 1,2}$ = 5 MHz)
  (600 dpi sensor) 10 MHz MAX ($f_{\phi 1,2}$ = 10 MHz)
- Power supply : +12 V
- On-chip circuit : Reset feed-through level clamp circuits
  Voltage amplifiers

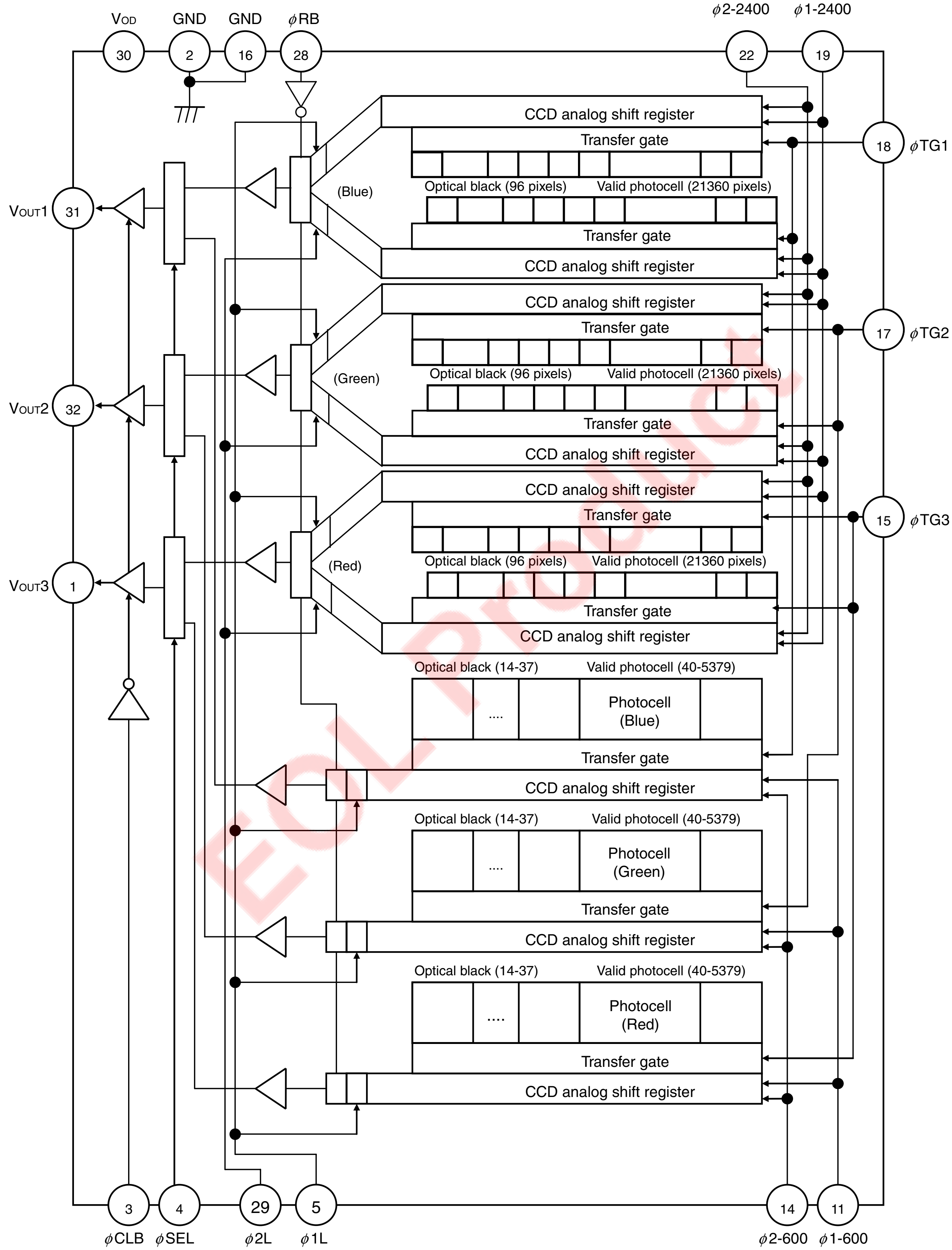
ORDERING INFORMATION

Part Number	Package
μPD8894CY-A	CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

Remark The μPD8894CY-A is a lead-free product.

Document No. S17946EJ1V0DS00 (1st edition)
Date Published March 2006 NS CP (N)
Printed in Japan

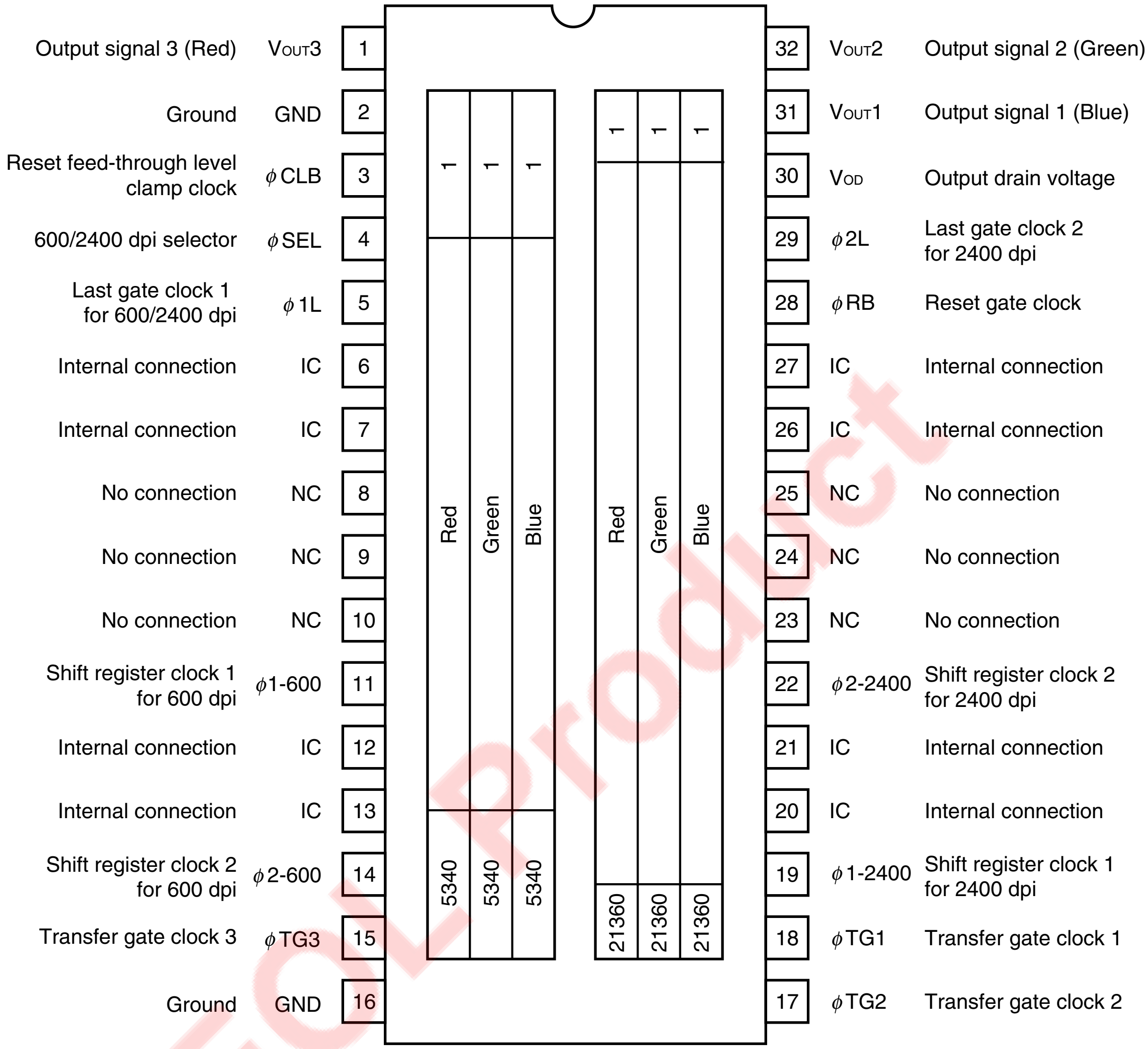
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

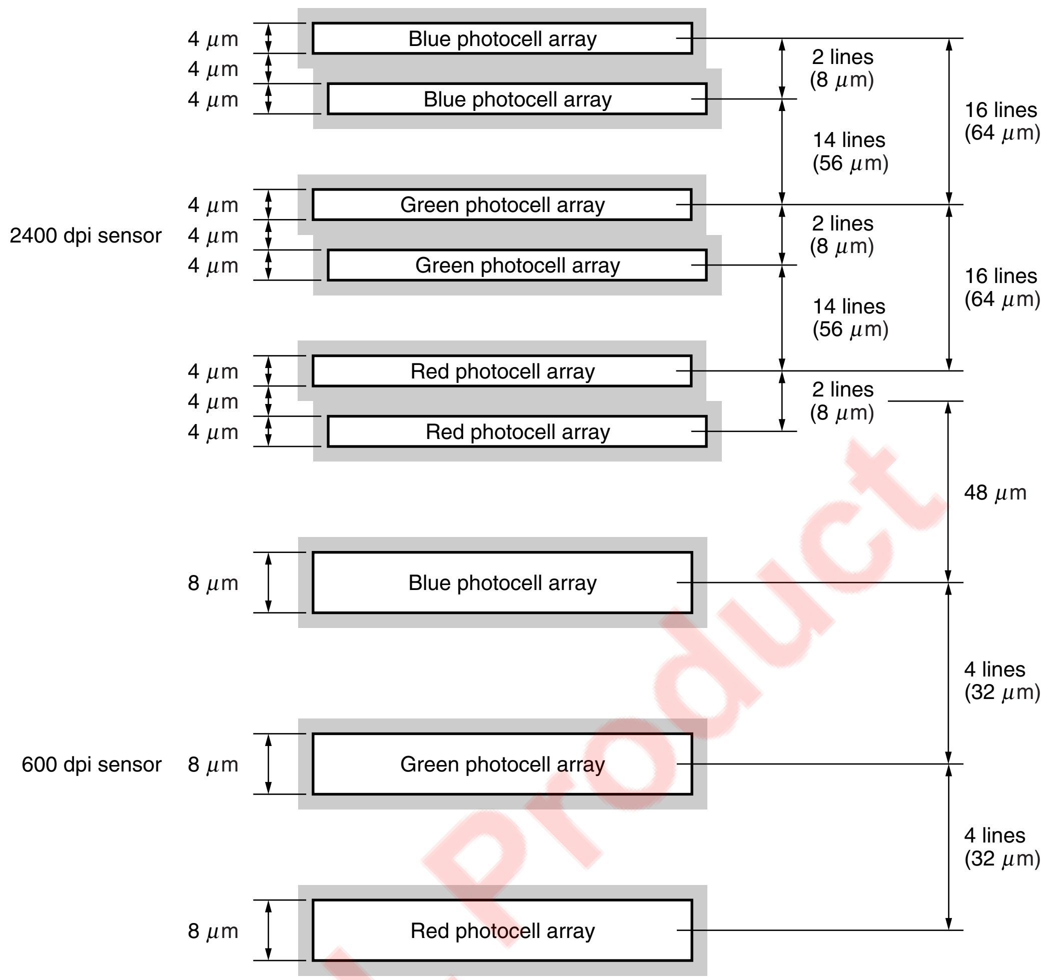
μPD8894CY-A



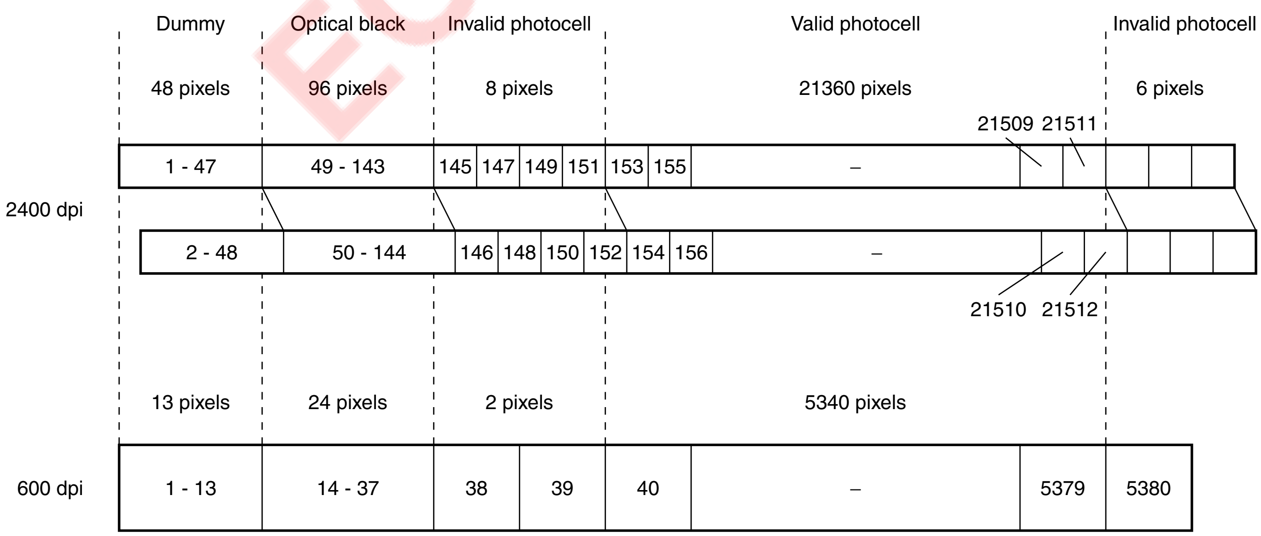
Cautions 1. Leave pins 6, 7, 12, 13, 20, 21, 26, 27 (IC) unconnected.

2. Connect the no connection pins (NC) to GND.

PHOTOCELL ARRAY STRUCTURE DIAGRAM-1 (Line spacing)



PHOTOCELL ARRAY STRUCTURE DIAGRAM-2 (Dummy, Optical Black, for Each Color)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi 1\text{-}600, 1\text{-}2400, 1L}$, $V_{\phi 2\text{-}600, 2\text{-}2400, 2L}$	–0.3 to +8.0	V
Reset gate clock voltage	$V_{\phi RB}$	–0.3 to +8.0	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	–0.3 to +8.0	V
600/2400 dpi select signal voltage	$V_{\phi SEL}$	–0.3 to +8.0	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	–0.3 to +8.0	V
Operating ambient temperature Note	T_A	0 to +60	˚C
Storage temperature	T_{stg}	–40 to +70	˚C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage		V_{OD}	11.4	12.0	12.6	V
Shift register clock high level		$V_{\phi 1\text{-}600H, 1\text{-}2400H, 1LH}$, $V_{\phi 2\text{-}600H, 2\text{-}2400H, 2LH}$	4.75	5.0	5.25	V
Shift register clock low level		$V_{\phi 1\text{-}600L, 1\text{-}2400L, 1LL}$, $V_{\phi 2\text{-}600L, 2\text{-}2400L, 2LL}$	0	0	0.25	V
Reset gate clock high level		$V_{\phi RBH}$	4.75	5.0	5.25	V
Reset gate clock low level		$V_{\phi RBL}$	0	0	0.25	V
Reset feed-through level clamp clock high level		$V_{\phi CLBH}$	4.75	5.0	5.25	V
Reset feed-through level clamp clock low level		$V_{\phi CLBL}$	0	0	0.25	V
600/2400 dpi select signal high level		$V_{\phi SELH}$	4.75	5.0	5.25	V
600/2400 dpi select signal low level		$V_{\phi SELL}$	0	0	0.25	V
Transfer gate clock high level		$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.75	5.0	5.25	V
Transfer gate clock low level		$V_{\phi TG1L}$ to $V_{\phi TG3L}$	0	0	0.25	V
CCD Transfer speed	2400 dpi	$f_{\phi 1}$, $f_{\phi 2}$	–	1.0	5	MHz
	600 dpi				10	MHz
Data rate		$f_{\phi RB}$	–	2.0	10.0	MHz

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, data rate ($f_{\phi RB}$) = 2 MHz, storage time = 11.0 ms, input signal clock = 5 V_{p-p}
light source: 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm)+ HA-50 (heat absorbing filter, t = 3 mm))

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		V_{sat}	2400 dpi	2.5	2.8	–	V
			600 dpi	2.5	2.8	–	V
Saturation exposure	Red	SER	2400 dpi	–	0.664	–	lx•s
			600 dpi	–	0.196	–	lx•s
	Green	SEG	2400 dpi	–	0.700	–	lx•s
			600 dpi	–	0.207	–	lx•s
	Blue	SEB	2400 dpi	–	1.089	–	lx•s
			600 dpi	–	0.323	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6	20	%
Photo response non-uniformity at low illumination		LPRNU2	V_{OUT} = 0.05 V, data rate = 5 MHz, 2400 dpi Note 3, 600 dpi Note 4	–	3	10	mV
Average dark signal		ADS	Light shielding, 2400 dpi	–	0.6	4.0	mV
			Light shielding, 600 dpi	–	1.2	8.0	mV
Dark signal non-uniformity		DSNU	Light shielding, 2400 dpi	–	4.0	8.0	mV
			Light shielding, 600 dpi	–	8.0	16.0	mV
Power consumption		P_W		–	360	430	mW
Output impedance		Z_O		–	0.4	1.0	kΩ
Response	Red	R_R	2400 dpi	2.96	4.22	5.49	V/lx•s
			600 dpi	10.00	14.28	18.57	V/lx•s
	Green	R_G	2400 dpi	2.80	4.00	5.20	V/lx•s
			600 dpi	9.46	13.52	17.57	V/lx•s
	Blue	R_B	2400 dpi	1.80	2.57	3.34	V/lx•s
			600 dpi	6.08	8.68	11.28	V/lx•s
Response ratio (600/2400 dpi)		R6/24		2.6	3.4	4.2	times
Offset level Note 1		V_{OS}		4.0	5.5	7.0	V
Output fall delay time Note 2		t_d	V_{OUT} = 1.0 V	–	20	–	ns
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, data rate = 10 MHz	92	98	–	%
Register imbalance		RI	V_{OUT} = 1.0 V, 2400 dpi	–	1.0	6.0	%
Smear		Sm	V_{OUT} = 1.0 V, 600 dpi	–	–	0.30	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	460	–	nm
Reset feed-through noise		RFTN	Light shielding, 600 dpi, 2400 dpi	–2000	–500	+1000	mV
Random noise (CDS)		σCDS	Light shielding, 600 dpi, 2400 dpi	–	1.2	–	mV

Notes 1. Refer to **TIMING CHART 2**.

2. When the fall time of ϕ1-600, 2400 (t1) is the TYP. value (refer to **TIMING CHART 2**).

3. When the t17 is 500 μs (refer to **ϕTG1 to ϕTG3, ϕ1, ϕ2 TIMING CHART**).

4. When the t17 is 1 μs (refer to **ϕTG1 to ϕTG3, ϕ1, ϕ2 TIMING CHART**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1\text{-}600}$	φ1-600	11	–	600	–	pF
	$C_{\phi 1\text{-}2400}$	φ1-2400	19	–	1400	–	pF
Shift register clock pin capacitance 2	$C_{\phi 2\text{-}600}$	φ2-600	14	–	600	–	pF
	$C_{\phi 2\text{-}2400}$	φ2-2400	22	–	1400	–	pF
Reset gate clock pin capacitance	$C_{\phi RB}$	φRB	28	–	20	–	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	φCLB	3	–	20	–	pF
600/2400 dpi select signal pin capacitance	$C_{\phi SEL}$	φSEL	4	–	20	–	pF
Last shift register clock pin capacitance 1	$C_{\phi 1L}$	φ1L	5	–	20	–	pF
Last shift register clock pin capacitance 2	$C_{\phi 2L}$	φ2L	29	–	20	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	φTG1	18	–	20	–	pF
		φTG2	17	–	20	–	pF
		φTG3	15	–	20	–	pF

APPLICATION NOTE

The μPD8894 has function of two readout modes, High Resolution Mode and Low Resolution Mode. These two modes can be selected by φSEL switch.

Mode	Description	φSEL	600 dpi Data	2400 dpi Data	φ1, 2-600	φ1, 2-2400	φ1L	φ2L
1	High Resolution	Low	Flush	Use	5 V (High)	Clocked	Clocked	Clocked
2	Low Resolution	High	Use	Flush	Clocked	5 V (High)	Clocked	5 V (High)

Remark Flush means that data is continuously sunk via reset gate.

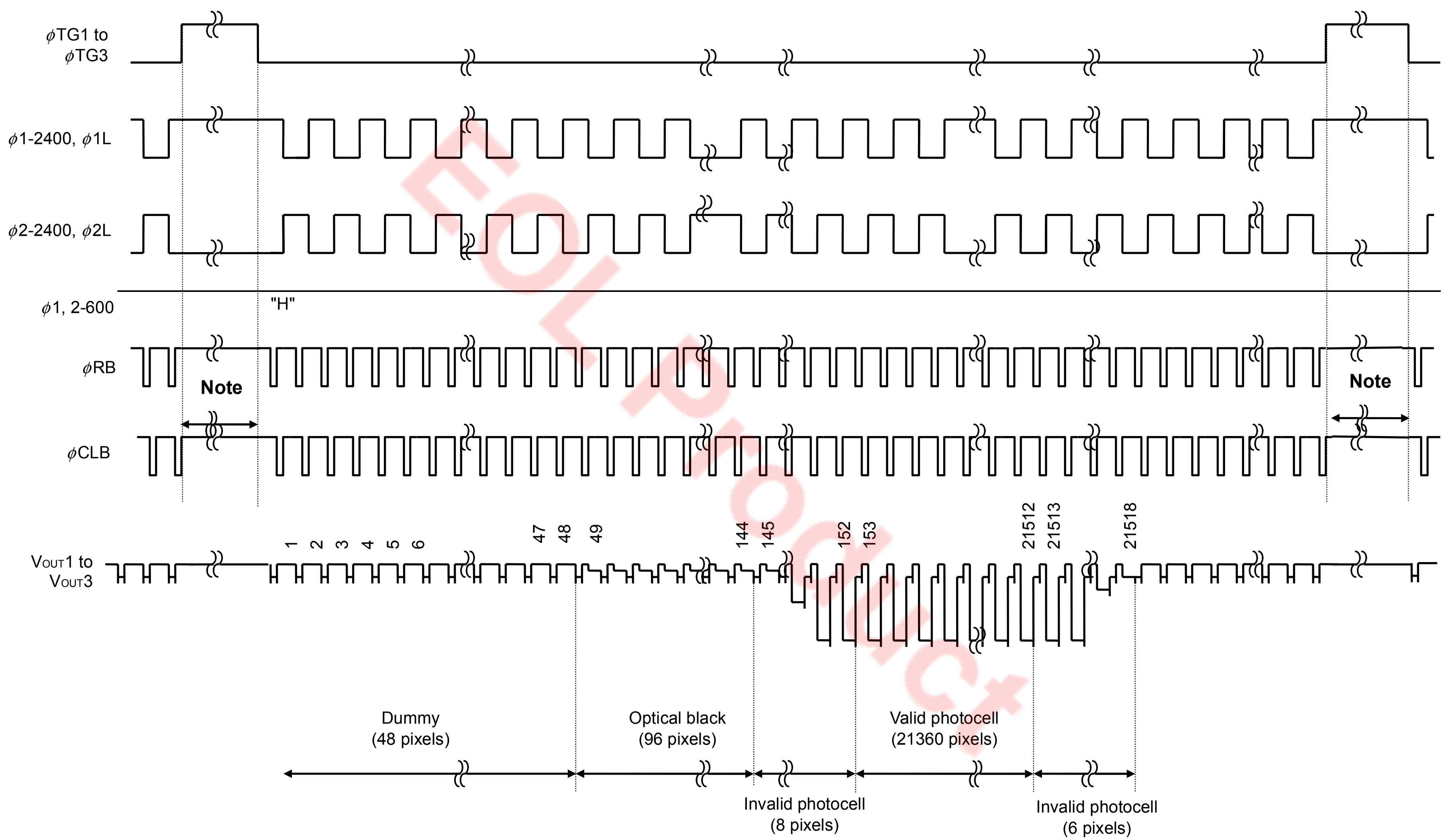
(1) High Resolution Mode

In this mode, both signals in even lines and odd lines can be read out. This mode enables 2400 dpi (max) resolution with A4 size (210 × 297 mm, shorter side).

(2) Low Resolution Mode

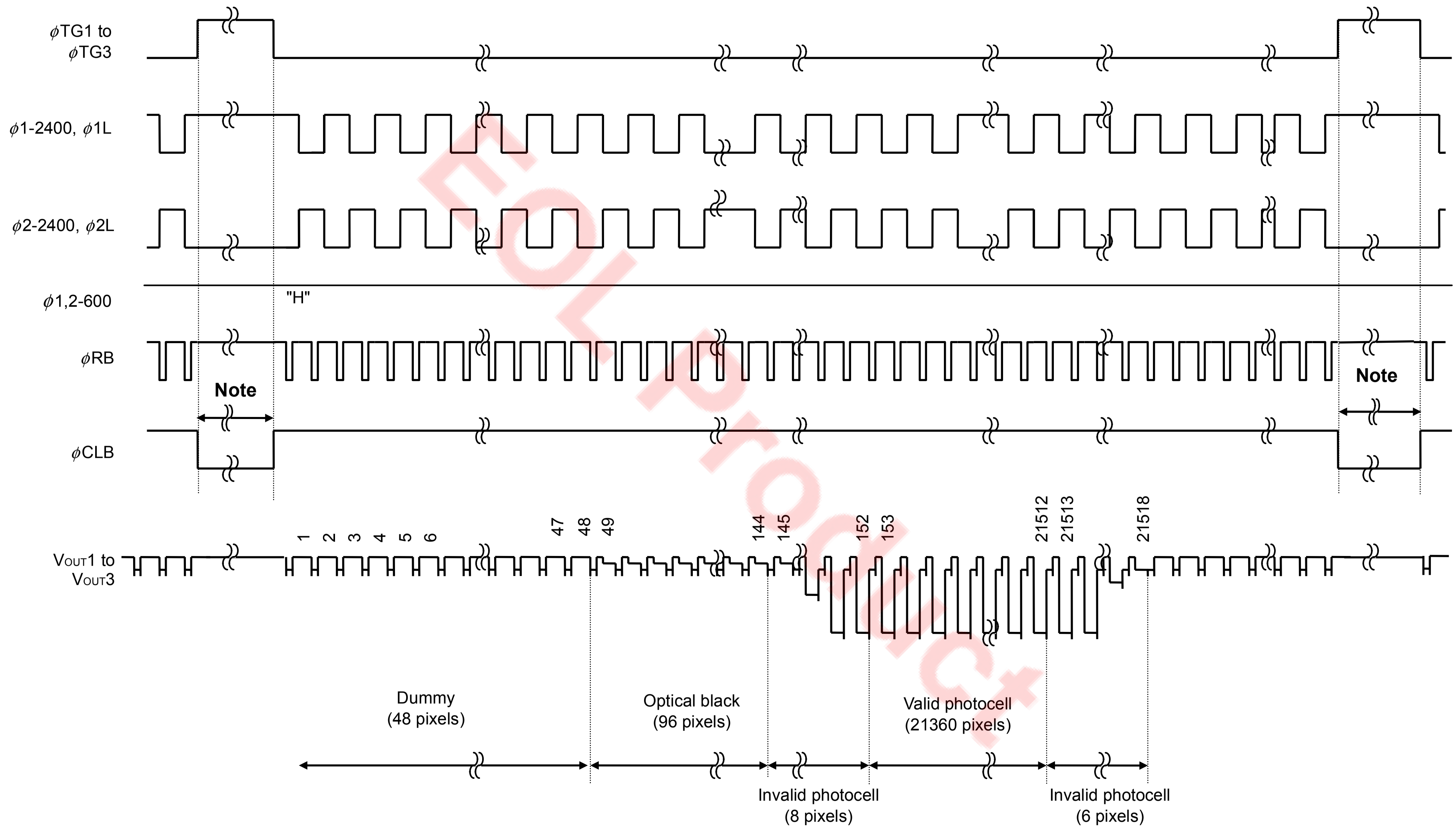
This mode enables 600 dpi (max) resolution with A4 size (210 × 297 mm, shorter side). Then it can achieve low resolution with A4 size such as 300,150 dpi.

TIMING CHART 1-1-1 (for each color, 2400 dpi, φSEL = low, bit clamp mode)



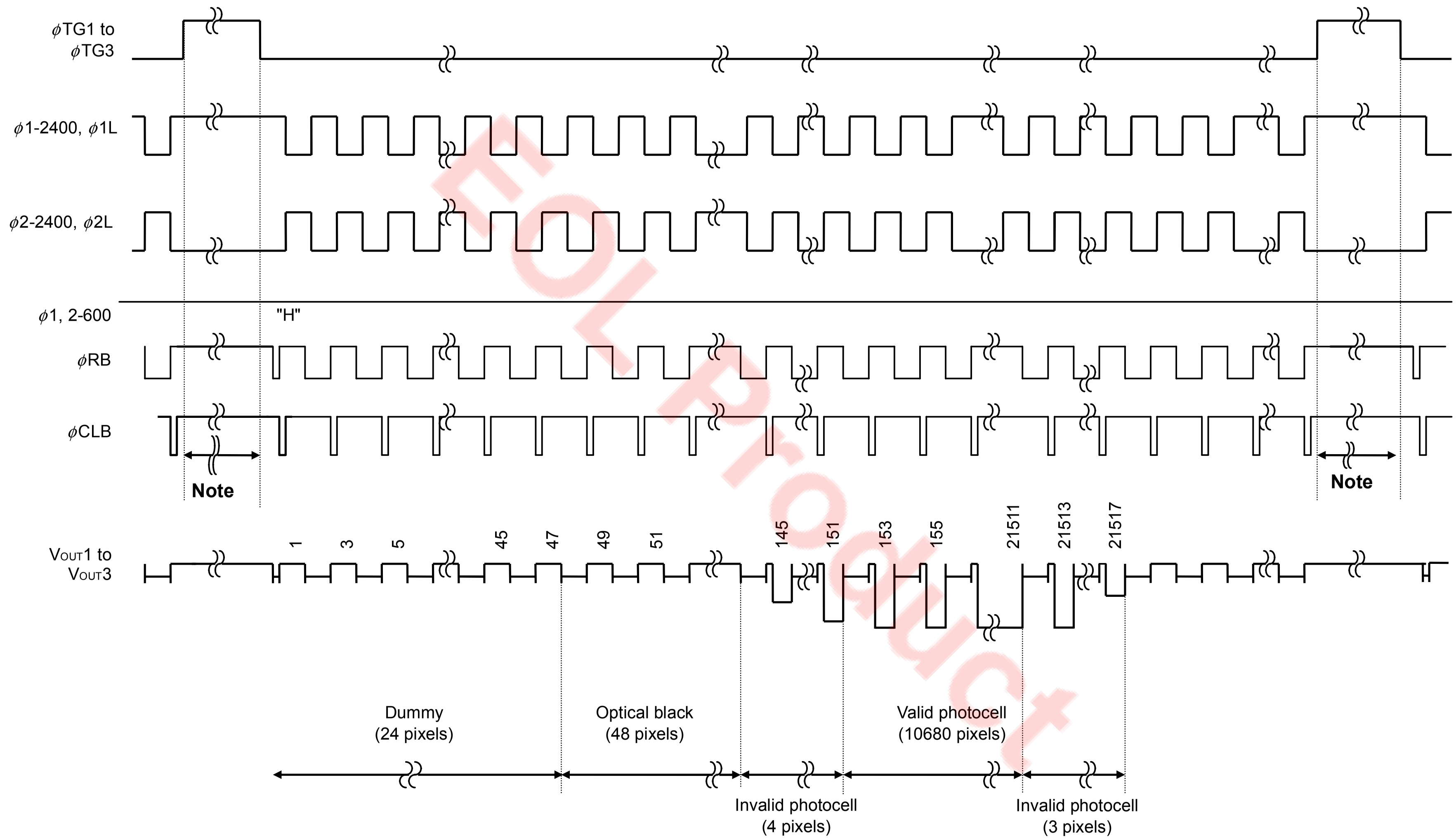
Note Input the φRB and φCLB pulse stop during this period.

TIMING CHART 1-1-2 (for each color, 2400 dpi, φSEL = low, line clamp mode)



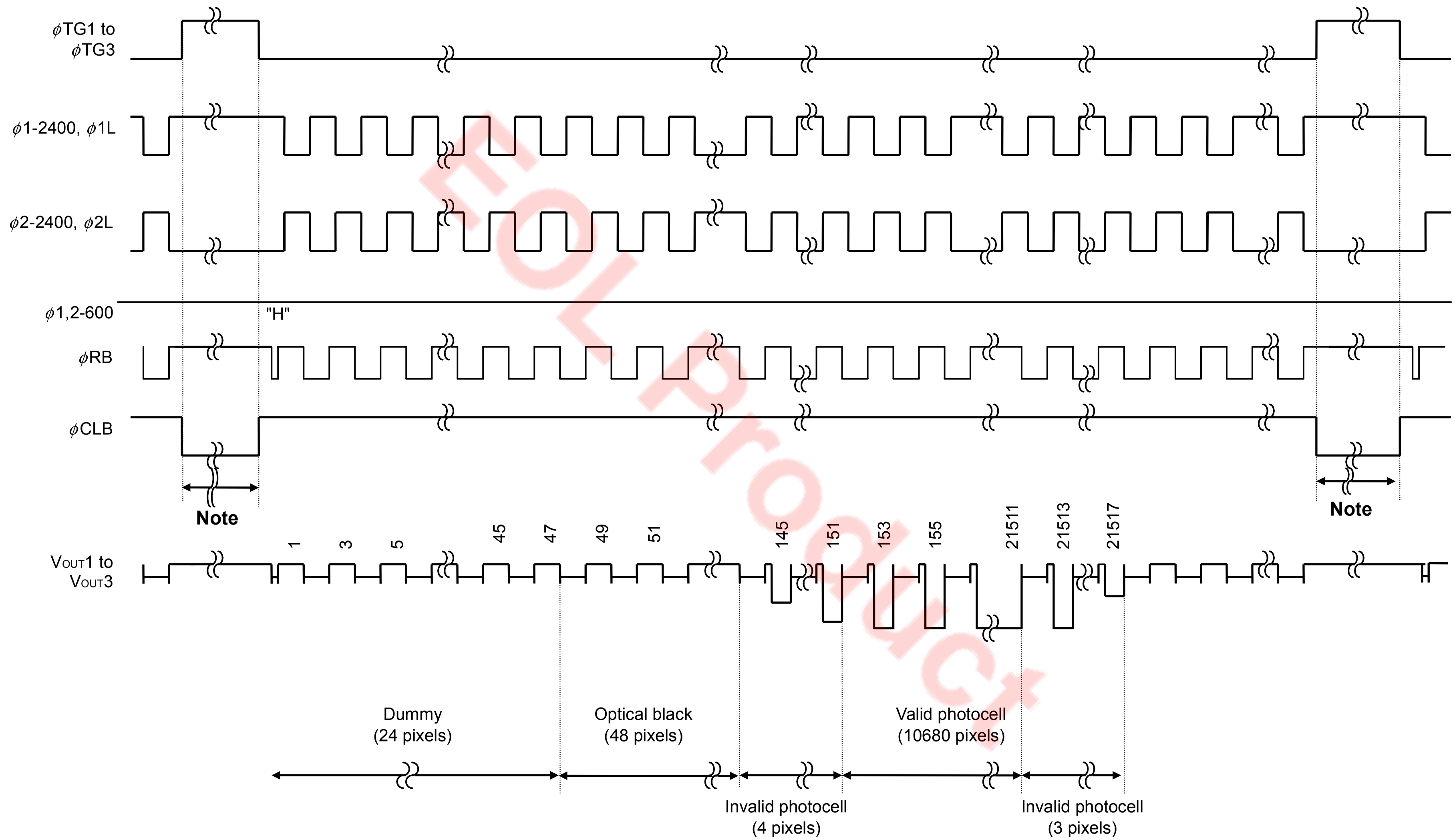
Note Input the φRB and φCLB pulse stop during this period.

TIMING CHART 1-2-1 (for each color, 1200 dpi, ϕSEL = low, bit clamp mode)



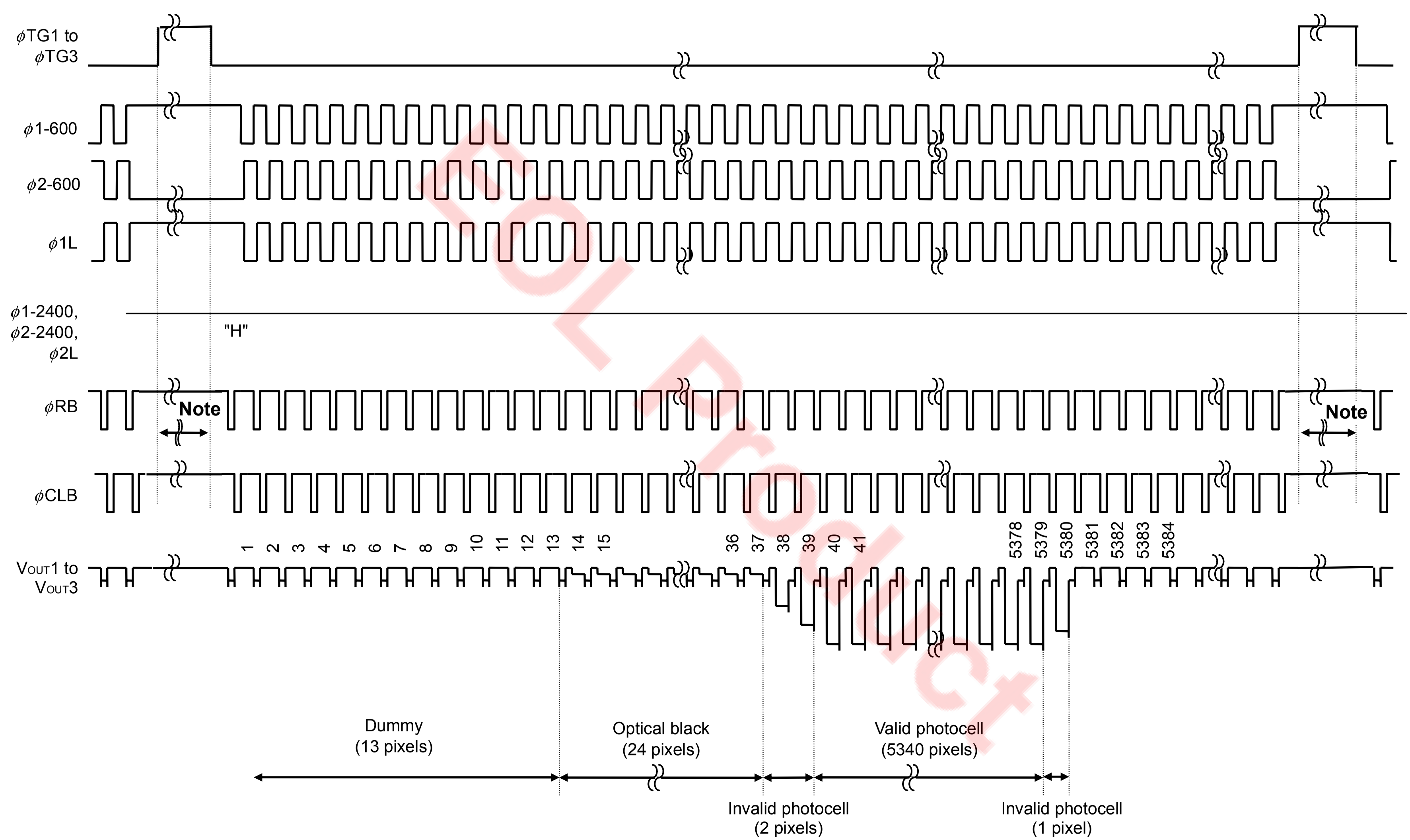
Note Input the ϕRB and ϕCLB pulse stop during this period.

TIMING CHART 1-2-2 (for each color, 1200 dpi, ϕSEL = low, line clamp mode)



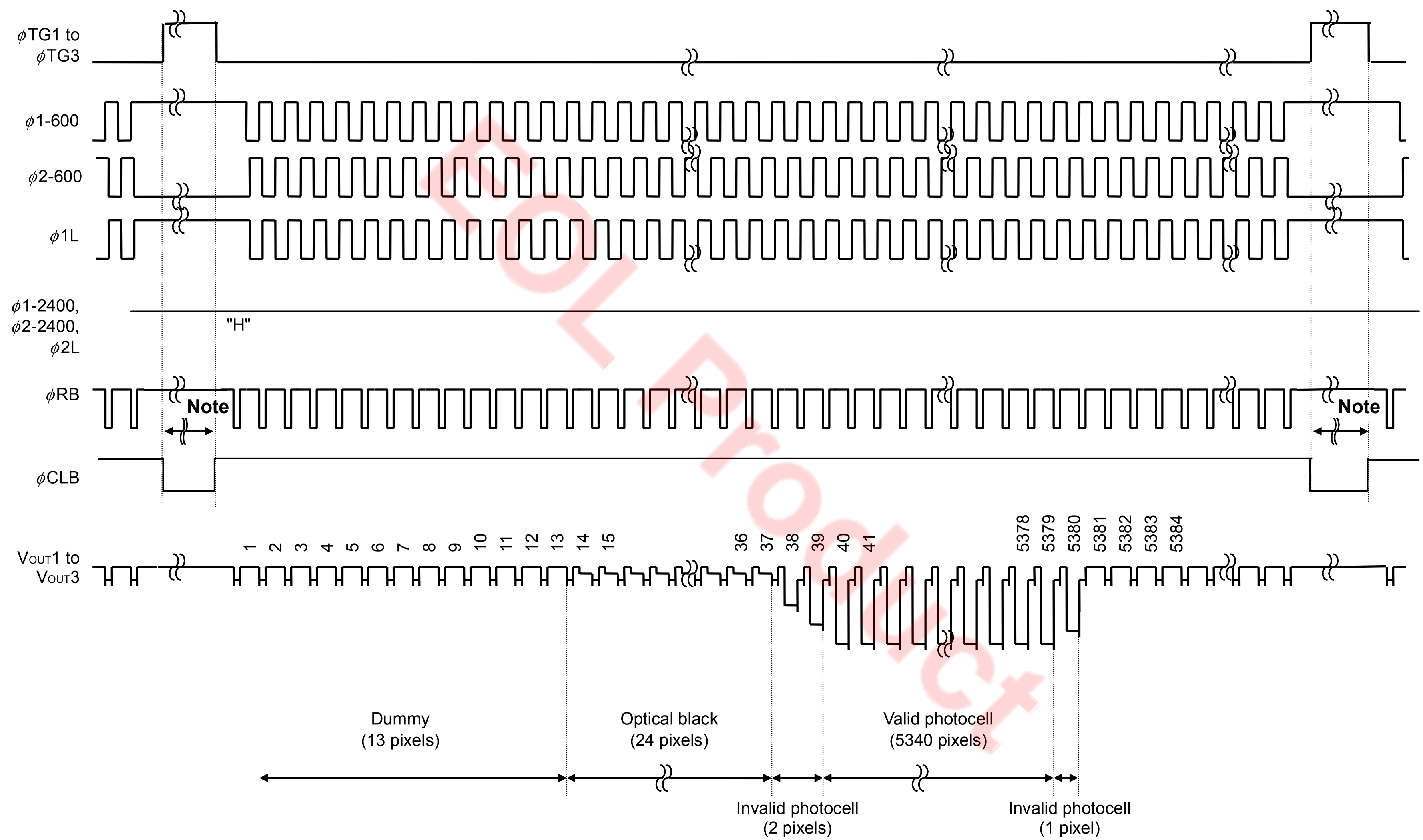
Note Input the ϕRB and ϕCLB pulse stop during this period.

TIMING CHART 1-3-1 (for each color, 600 dpi, φSEL = high, bit clamp mode)



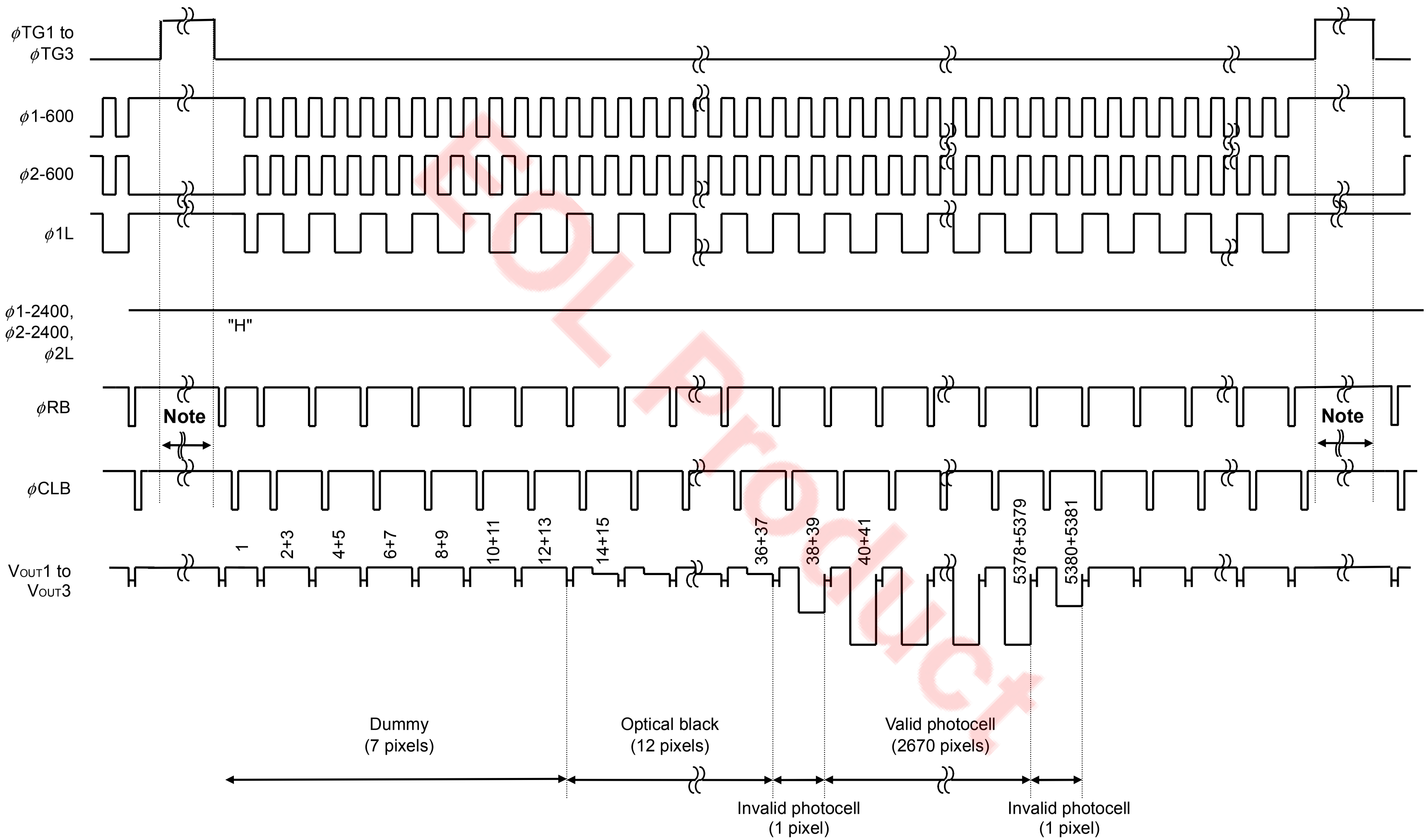
Note Input the φRB and φCLB pulse stop during this period.

TIMING CHART 1-3-2 (for each color, 600 dpi, φSEL = high, line clamp mode)



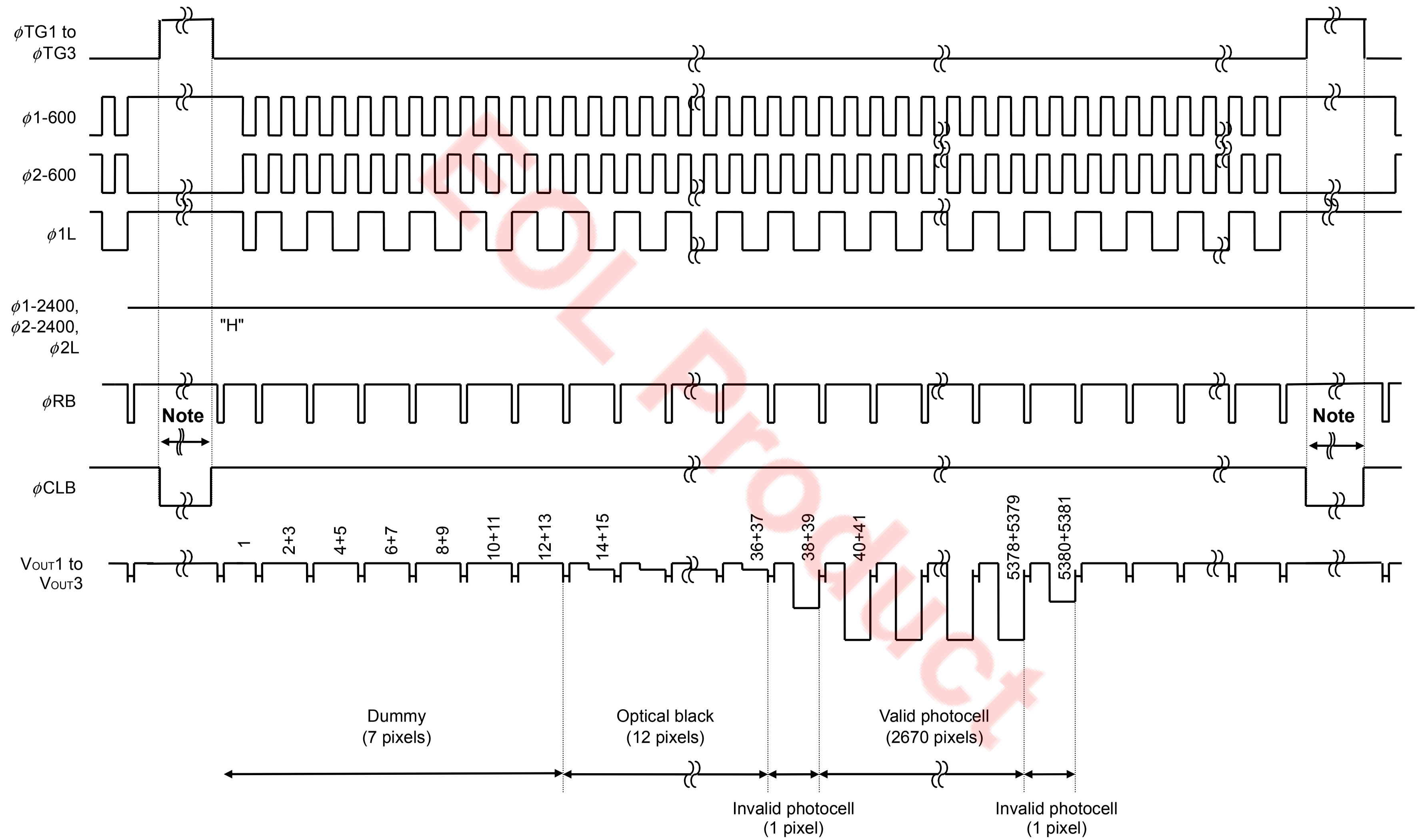
Note Input the φRB and φCLB pulse stop during this period.

TIMING CHART 1-4-1 (for each color, 300 dpi, φSEL = high, bit clamp mode)



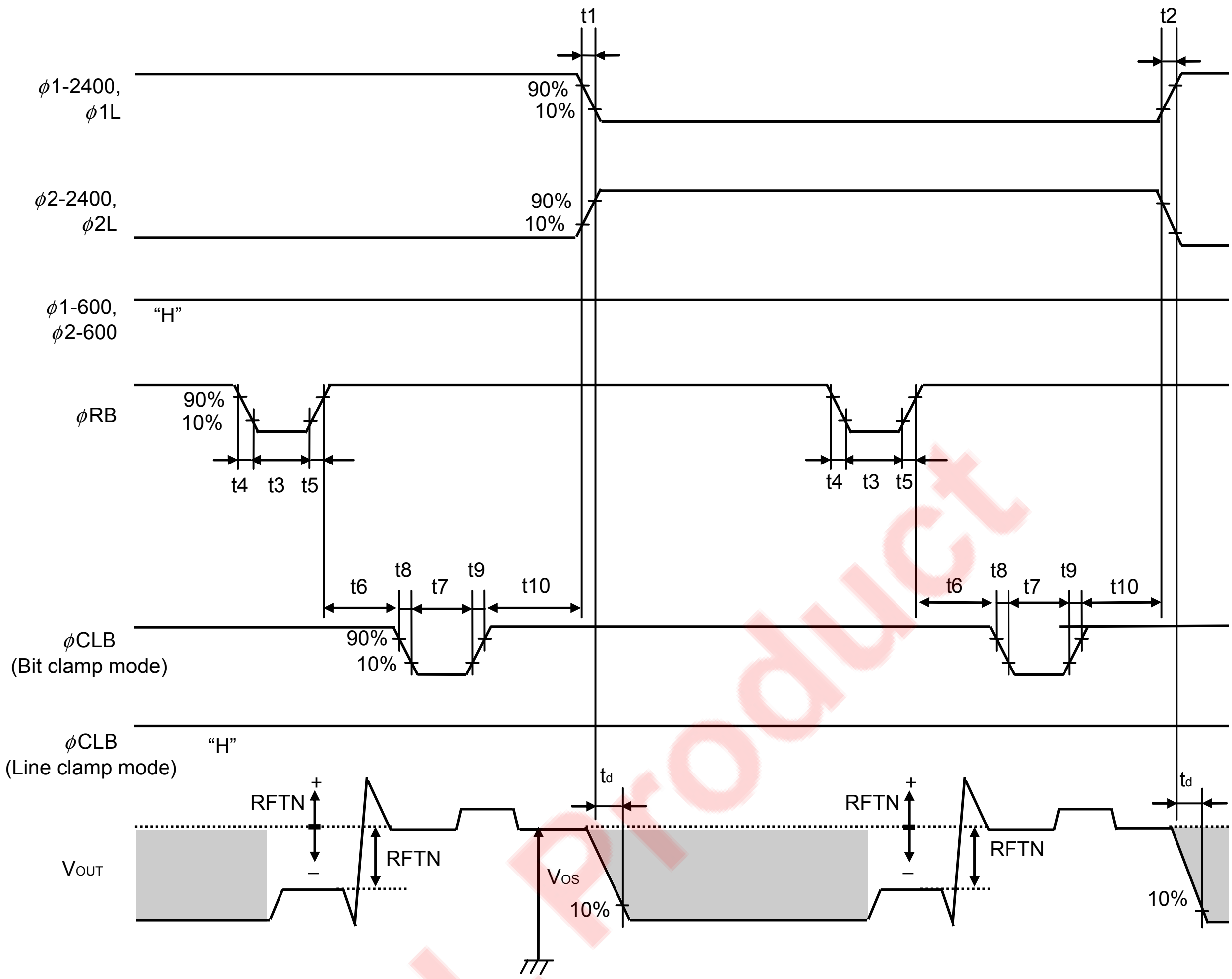
Note Input the φRB and φCLB pulse stop during this period.

TIMING CHART 1-4-2 (for each color, 300 dpi, φSEL = high, line clamp mode)



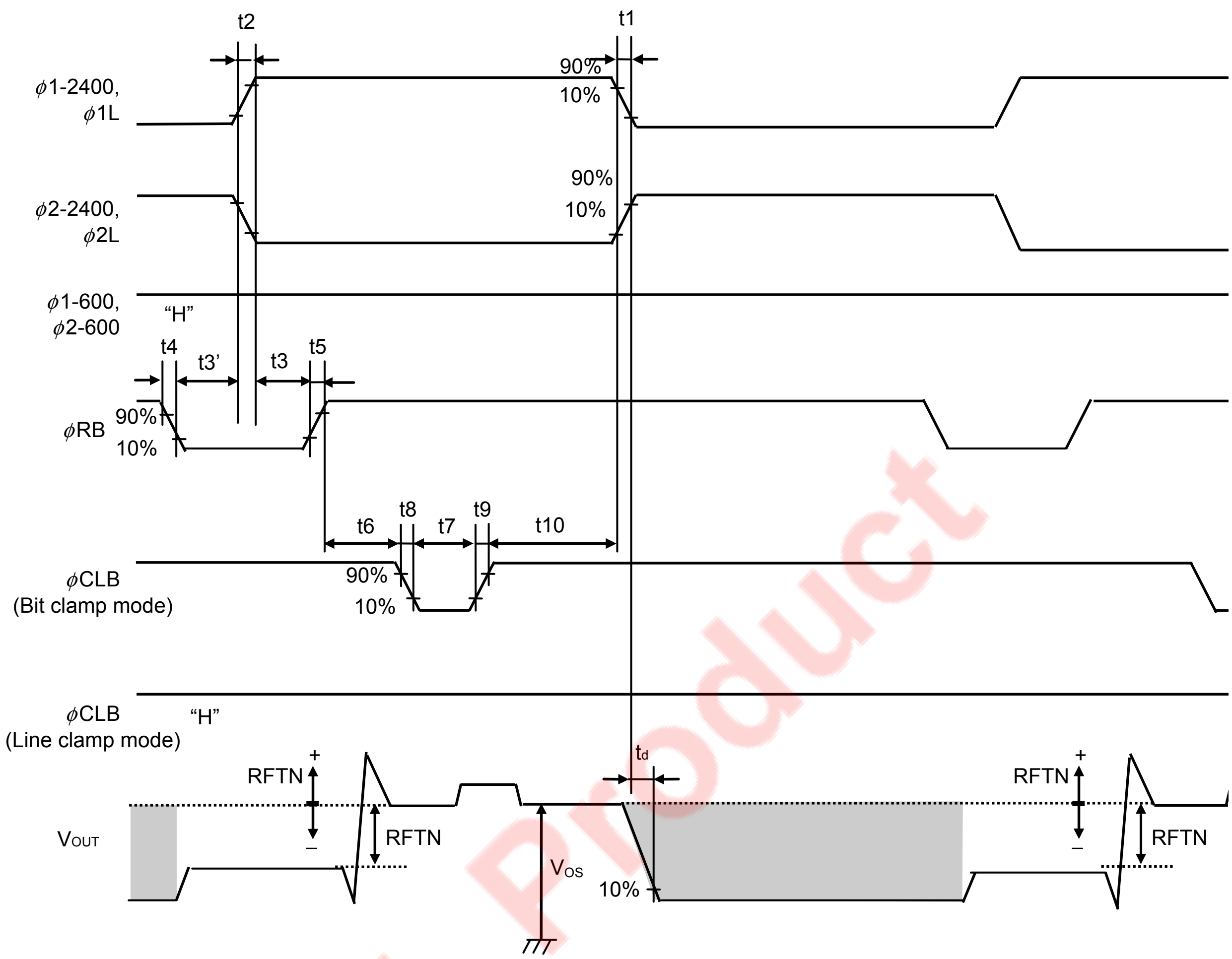
Note Input the φRB and φCLB pulse stop during this period.

TIMING CHART 2-1 (2400 dpi, for each color)



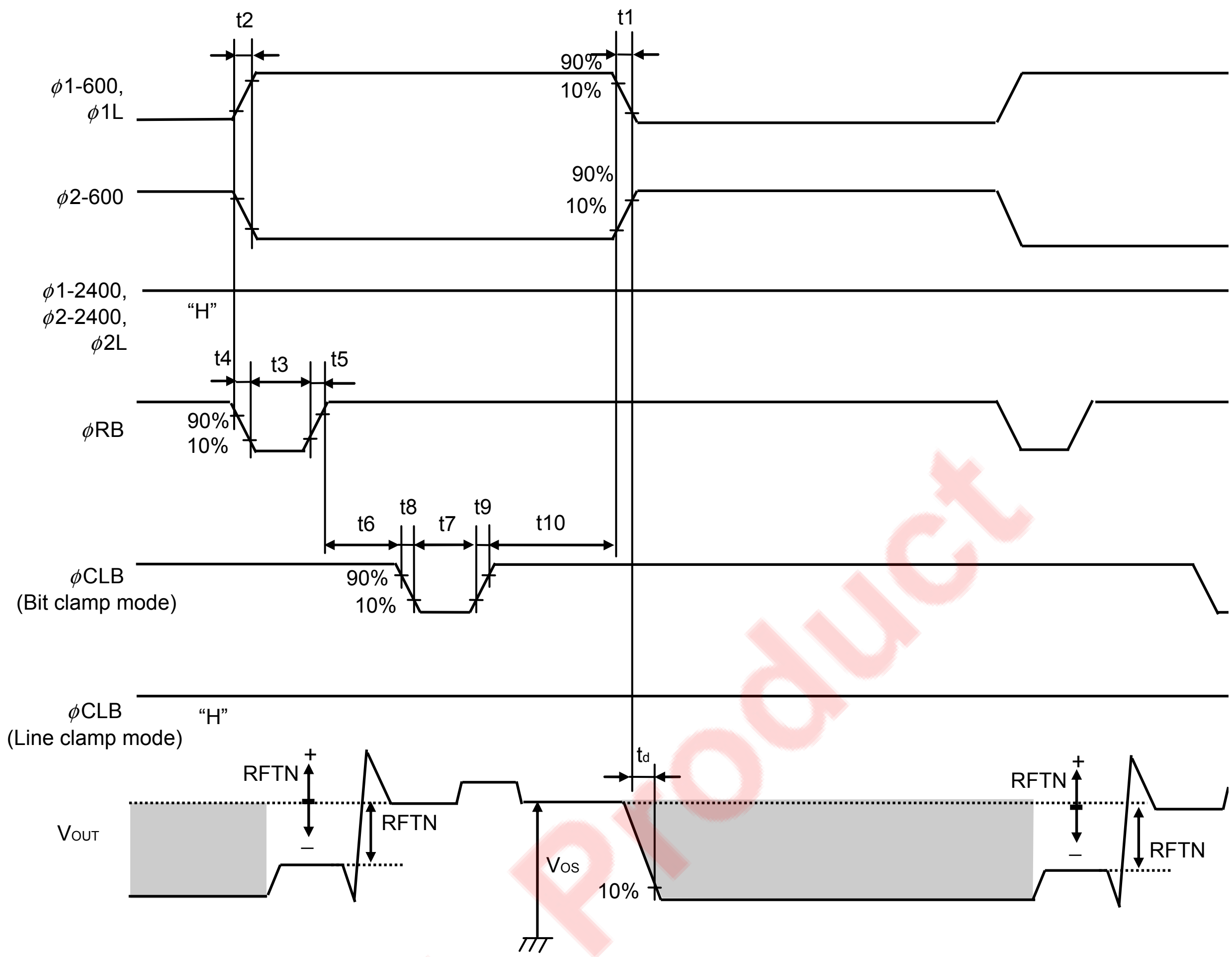
Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	–	ns
t3	20	50	–	ns
t4, t5	0	20	–	ns
t6	15	25	–	ns
t7	10	50	–	ns
t8, t9	0	20	–	ns
t10	5	45	–	ns

TIMING CHART 2-2 (1200 dpi, for each color)



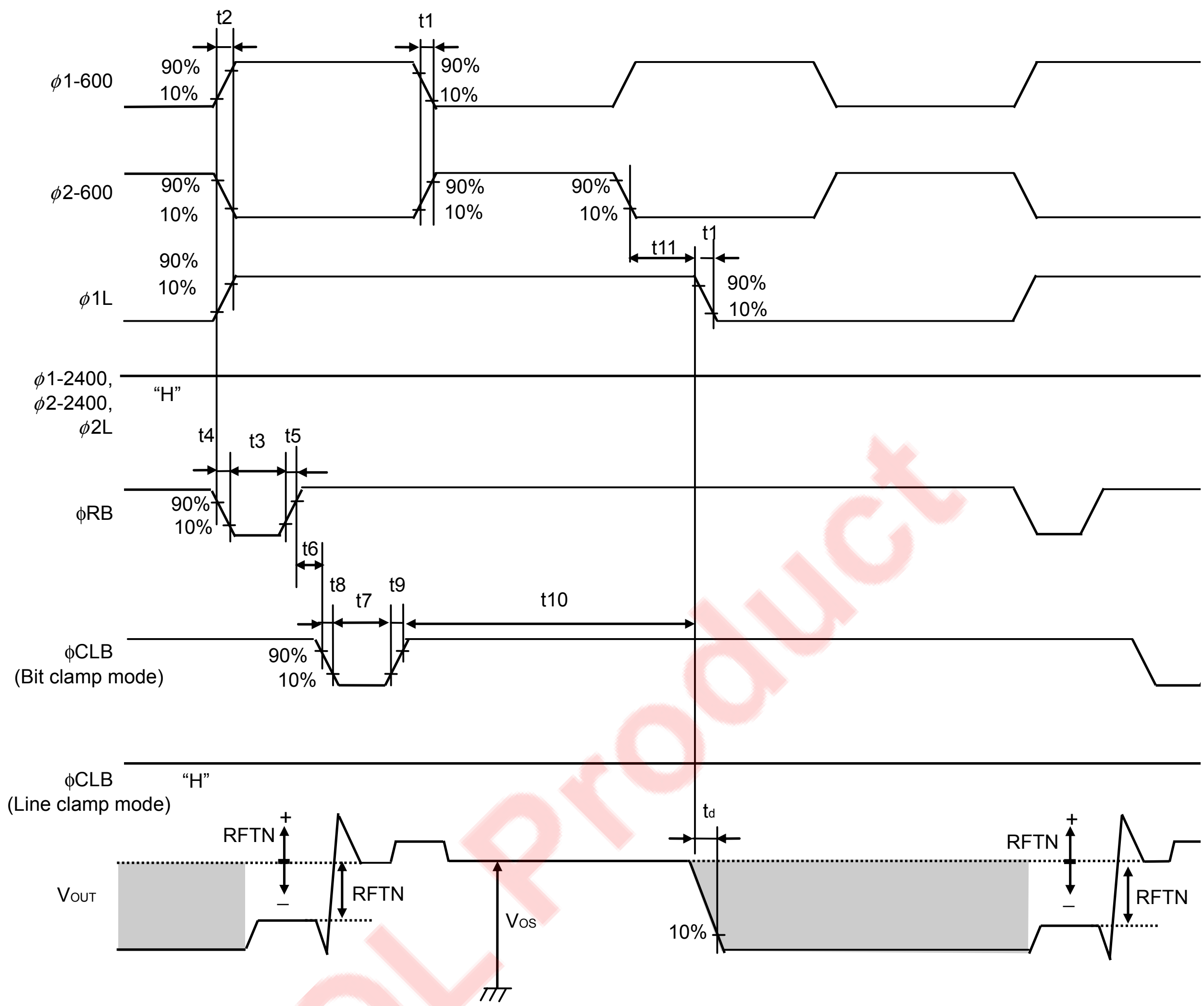
Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	–	ns
t3	20	50	–	ns
t3'	0	20	–	ns
t4, t5	0	20	–	ns
t6	15	25	–	ns
t7	10	50	–	ns
t8, t9	0	20	–	ns
t10	5	45	–	ns

TIMING CHART 2-3 (600 dpi, for each color)



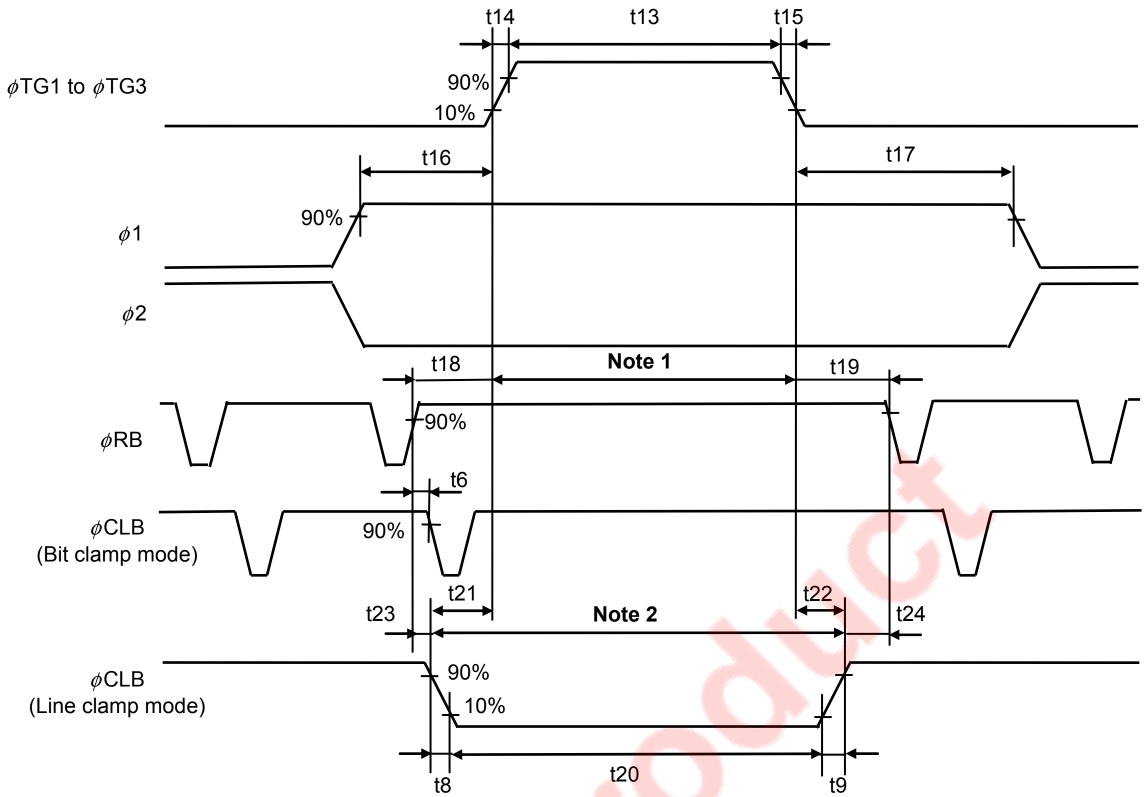
Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	–	ns
t3	20	50	–	ns
t4, t5	0	20	–	ns
t6	15	25	–	ns
t7	10	50	–	ns
t8, t9	0	20	–	ns
t10	5	45	–	ns

TIMING CHART 2-4 (300dpi, for each color)



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	–	ns
t3	20	50	–	ns
t4,t5	0	20	–	ns
t6	15	25	–	ns
t7	10	50	–	ns
t8,t9	0	20	–	ns
t10	5	45	–	ns
t11	50	80	–	ns

φTG1 to φTG3, φ1, φ2 TIMING CHART

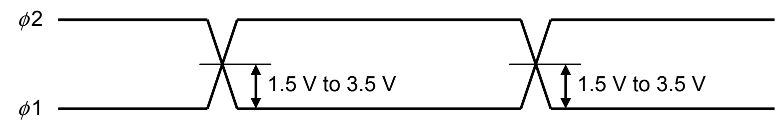


Symbol		MIN.	TYP.	MAX.	Unit
t6		15	25	–	ns
t8, t9		0	20	–	ns
t13		5000	10000	50000	ns
t14, t15		0	50	–	ns
t16		900	1000	–	ns
t17	2400 dpi	200000	500000	–	ns
	600 dpi	900	1000	–	ns
t18, t19		200	400	–	ns
t20		t13	t13	50000	ns
t21, t22		0	50	–	ns
t23		t6	t6	–	ns
t24		0	350	–	ns

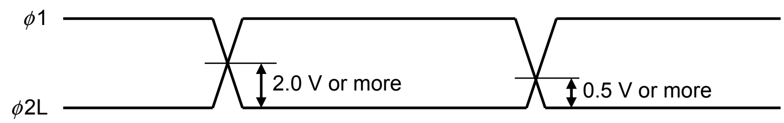
Notes 1. Set the φCLB and φRB to high level during this period.
2. Set the φRB to high level during this period.

Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB.

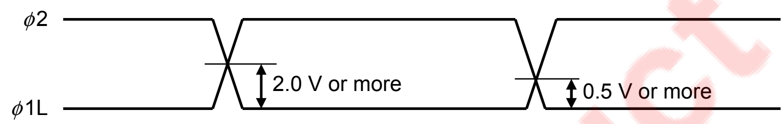
ϕ1, ϕ2 cross points



ϕ1, ϕ2L cross points



ϕ2, ϕ1L cross points



Remark Adjust cross points (ϕ1, ϕ2), (ϕ1, ϕ2L) and (ϕ2, ϕ1L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : V_{sat}

Output signal voltage at which the response linearity is lost.

2. Saturation exposure : SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : PRNU

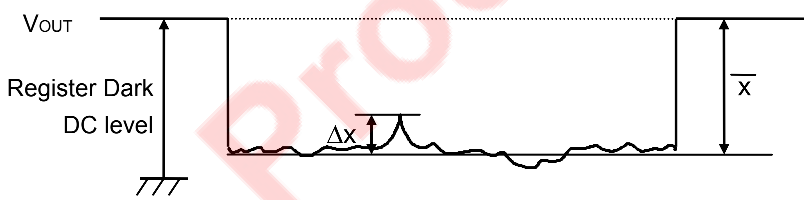
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $| x_j - \overline{x} |$

$$\overline{x} = \frac{\sum_{j=1}^{\text{Valid pixels}} x_j}{\text{Valid pixels}}$$

x_j : Output voltage of valid pixel number j



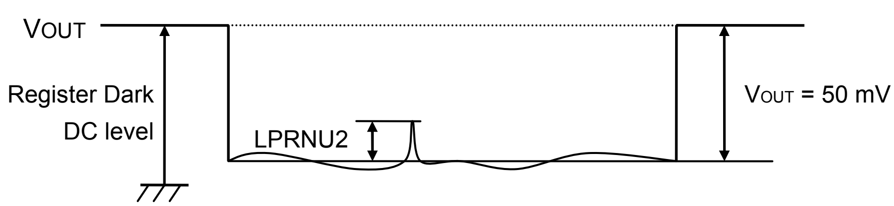
4. Photo response non-uniformity 2 at low illumination : LPRNU2

The difference in output voltage of the adjoining valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

LPRNU2 (mV) : maximum of $| x_j - x_{j+2} |_{\ j = 1 \text{ to Valid pixels}}$ (2400 dpi)

: maximum of $| x_j - x_{j+1} |_{\ j = 1 \text{ to Valid pixels}}$ (600 dpi)

x_j : Output voltage of valid pixel number j



5. Average dark signal : ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{ADS (mV)} = \frac{\sum_{j=1}^{\text{Valid pixels}} d_j}{\text{Valid pixels}}$$

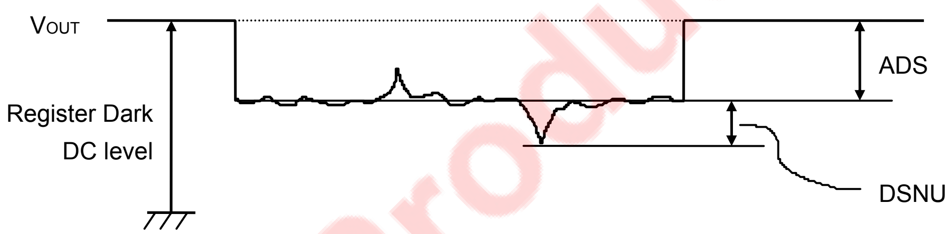
d_j : Dark signal of valid pixel number j

6. Dark signal non-uniformity : DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV)} : \text{maximum of } |\, d_j - \text{ADS} \,|_{\, j = 1 \text{ to Valid pixels}}$$

d_j : Dark signal of valid pixel number j



7. Output impedance : Zo

Impedance of the output pins viewed from outside.

8. Response : R

Output voltage divided by exposure (lx•s).
Note that the response varies with a light source (spectral characteristic).

9. Register imbalance : RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$\text{RI (\%)} = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}}(V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels
V_j : Output voltage of each pixel

10. Smear : Sm

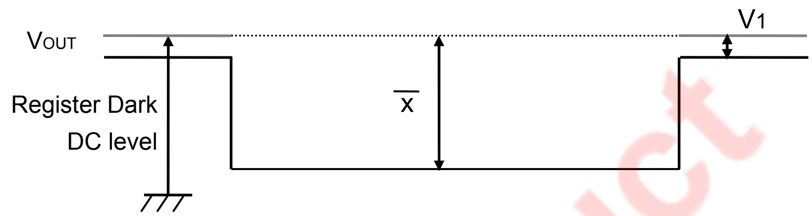
The rate of output voltage of CCD shift register signal, against the average output voltage of all the valid pixels.

$$Sm\ (\%) = \frac{V_1}{\overline{x}} \times 100$$

V_1: Output voltage of CCD shift register signal

$$\overline{x} = \frac{\sum_{j=1}^{\text{Valid pixels}} x_j}{\text{Valid pixels}}$$

x_j : Output voltage of valid pixel number j



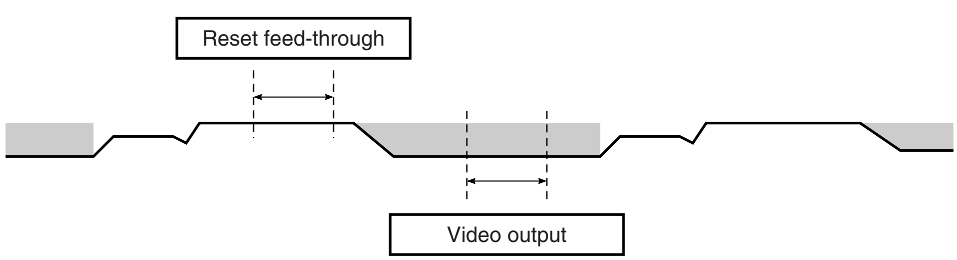
11. Random noise(CDS) : σCDS

Random noise σCDS is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding). σCDS is calculated by the following procedure.

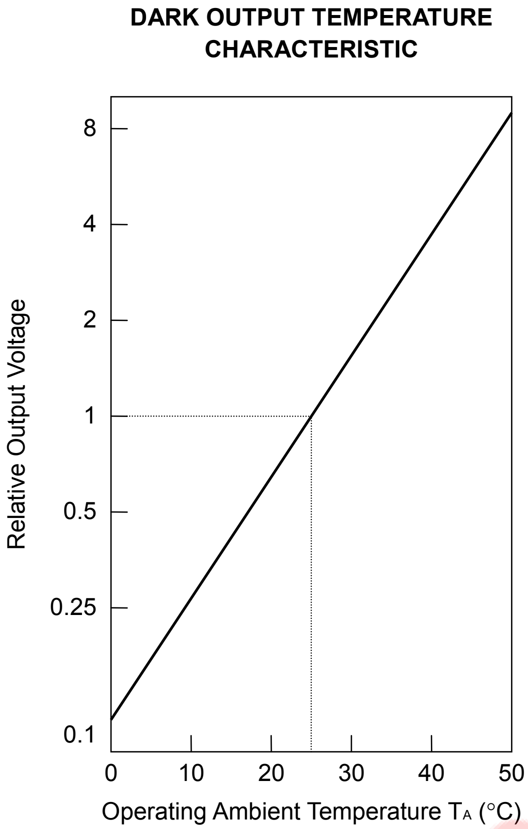
1. One valid photocell in one reading is fixed as measurement point.
2. The output level is measured during the reset feed-through period which is averaged over 100 ns to get “VDi”.
3. The output level is measured during the video output time averaged over 100 ns to get “VOi”.
4. The correlated double sampling output is defined by the following formula.
   VCDSi = VDi – VOi
5. Repeat the above procedure (1 to 4) for 100 times (= 100 lines).
6. Calculate the standard deviation σCDS using the following formula equation.

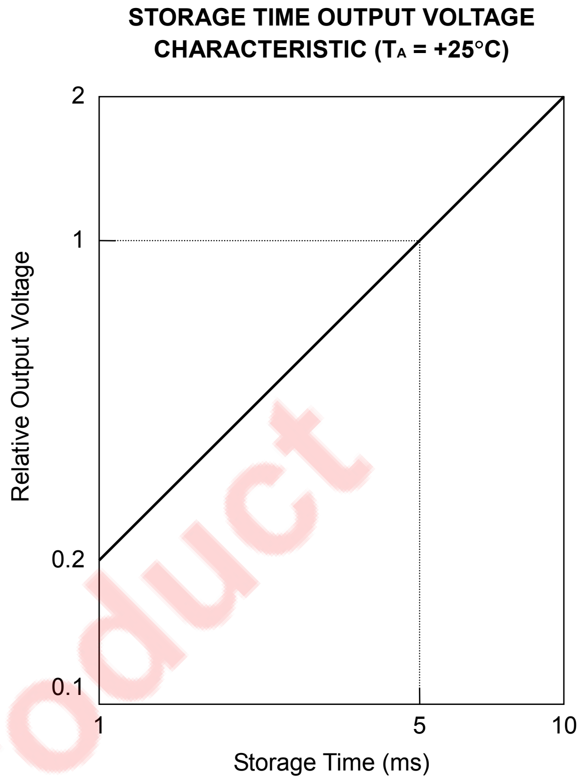
The following figure shows output waveform (valid photocell under dark condition).

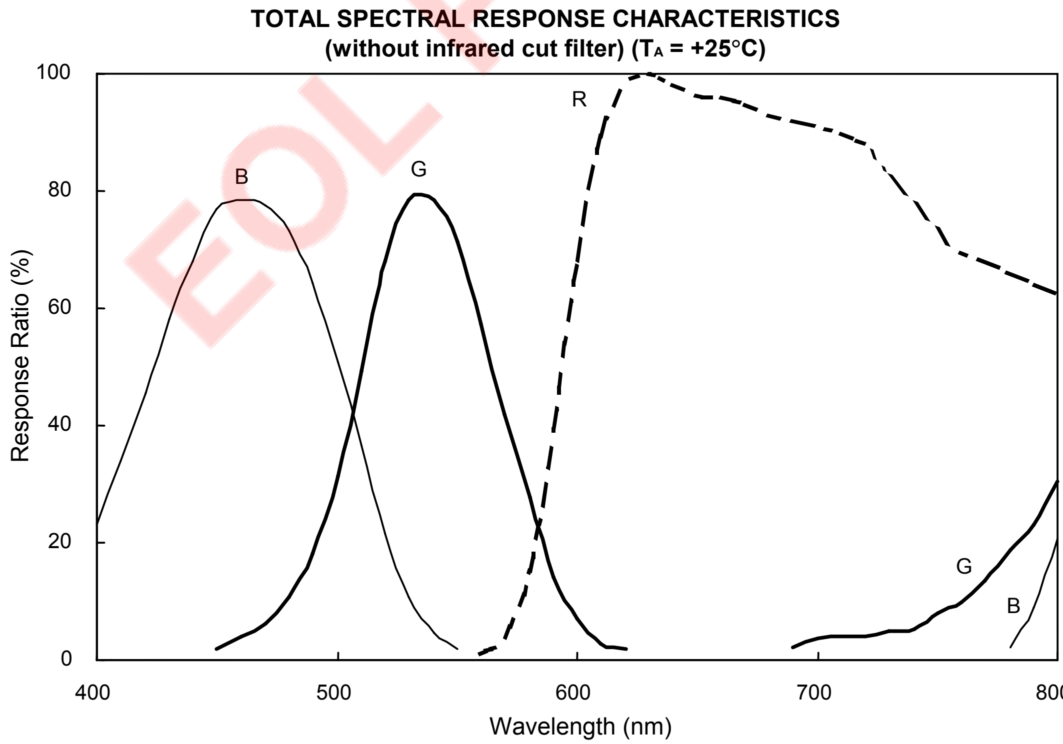
$$\sigma CDS\ (mV) = \sqrt{\frac{\sum_{i=1}^{100} (VCDS_i - \overline{V})^2}{100}} \qquad \overline{V} = \frac{1}{100} \sum_{i=1}^{100} VCDS_i$$



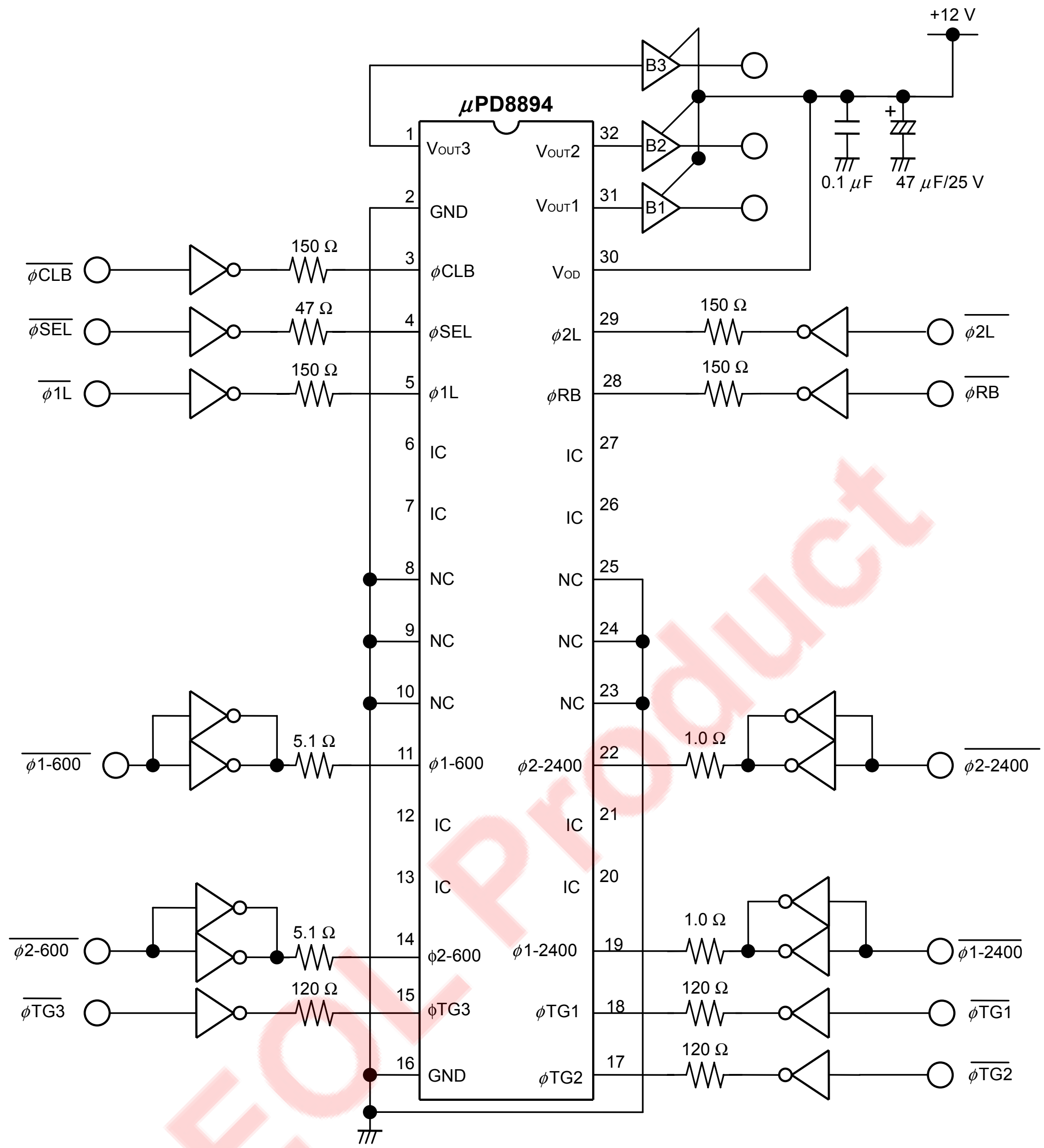
STANDARD CHARACTERISTIC CURVES (Reference Value)







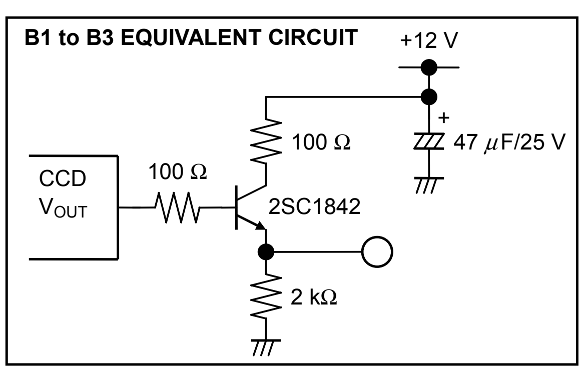
APPLICATION CIRCUIT EXAMPLE



Cautions 1. Leave pins 6, 7, 12, 13, 20, 21, 26, 27 (IC) unconnected.

2. Connect the no connection pins (NC) to GND.

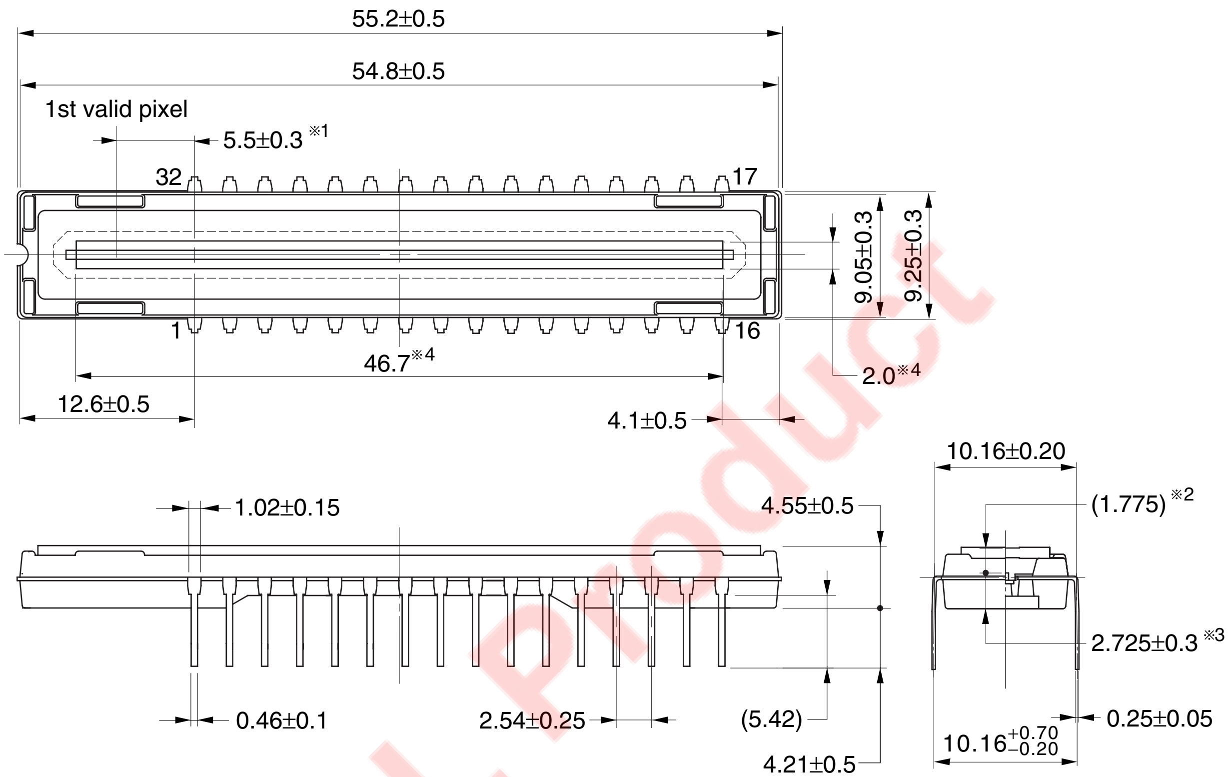
Remark The inverters shown in the above application circuit example are the 74AC04.



PACKAGE DRAWING

μPD8894CY-A
CCD LINEAR IMAGE SENSOR 32-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	52.2×6.4×0.8 (0.7※5)	1.5

※1 1st valid pixel ←→ The center of the pin1
※2 The surface of the CCD chip ←→ The top of the cap
※3 The bottom of the package ←→ The surface of the CCD chip
※4 Mirror finishied surface
※5 Thickness of mirror finished surface

32C-1CCD-PKG13

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8894CY-A: CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per pin).

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don't either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.

Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.