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Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

μPD78P356

16 BIT SINGLE-CHIP MICROCOMPUTER

The μPD78P356 is produced by replacing the internal mask ROM of the μPD78356 with a one-time PROM or EPROM. One-time PROM products, in which data can be written once are effective for manufacture of small quantities of multiple products and early stage start-up of application. EPROM products, to which programs can be re-written after previously written programs have been erased, are suited for system evaluation.

The following user's manuals completely describe the functions of the μPD78P356. Be sure to read them before designing an application system.

μPD78356 User's Manual, Hardware : IEU-1361
μPD78356 User's Manual, Instruction : IEU-1395

FEATURES

- Compatible with the μPD78356
  - Can be replaced with the μPD78356 containing mask ROM on a full-production basis.
- Internal PROM: 48K bytes
  - Data can be written once (one-time PROM product without an erasure window)
  - Written data can be erased by exposure to ultraviolet light and re-written electrically (EPROM product with an erasure window)
- Contained ECC circuit
  - The circuit ensures that highly reliable data is stored in the internal PROM.
- PROM programming: Same as for the μPD27C1001A
- QTOP™ microcomputer

Remark The QTOP microcomputer is a single-chip microcomputer with a built-in one-time PROM that is totally supported by NEC. The support includes writing application programs, marking, screening, and verification.

ORDERING INFORMATION

Part number	Package	Internal ROM
μPD78P356GC-7EA	100-pin plastic QFP (14 × 14 mm)	One-time PROM
μPD78P356GD-5BB	120-pin plastic QFP (28 × 28 mm)	One-time PROM
μPD78P356KP-S**Note**	120-pin ceramic WQFN	EPROM

Note Under development

In this manual, the description of the PROM is for both a one-time PROM and EPROM.

The information in this document is subject to change without notice.

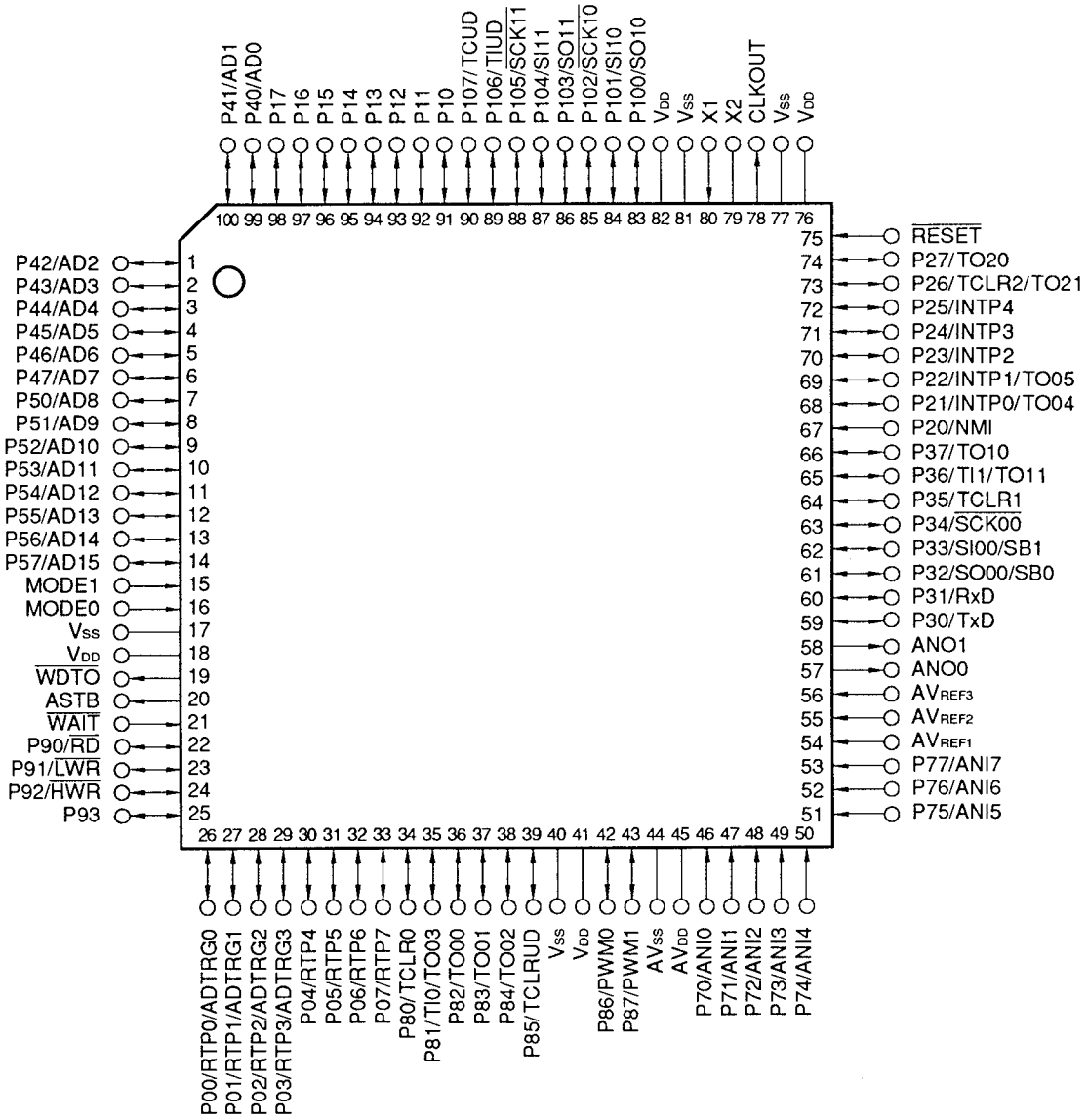
Document No. U10325EJ1V0DS00 (1st edition)
(Previous No. IP-3146)
Date Published October 1995 P
Printed in Japan

Major changes in this revision are indicated by stars (★) in the margins.

PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode (MODE0 = L, MODE1 = L)

- **100-pin plastic QFP (14 × 14 mm)**
  μPD78P356GC-7EA

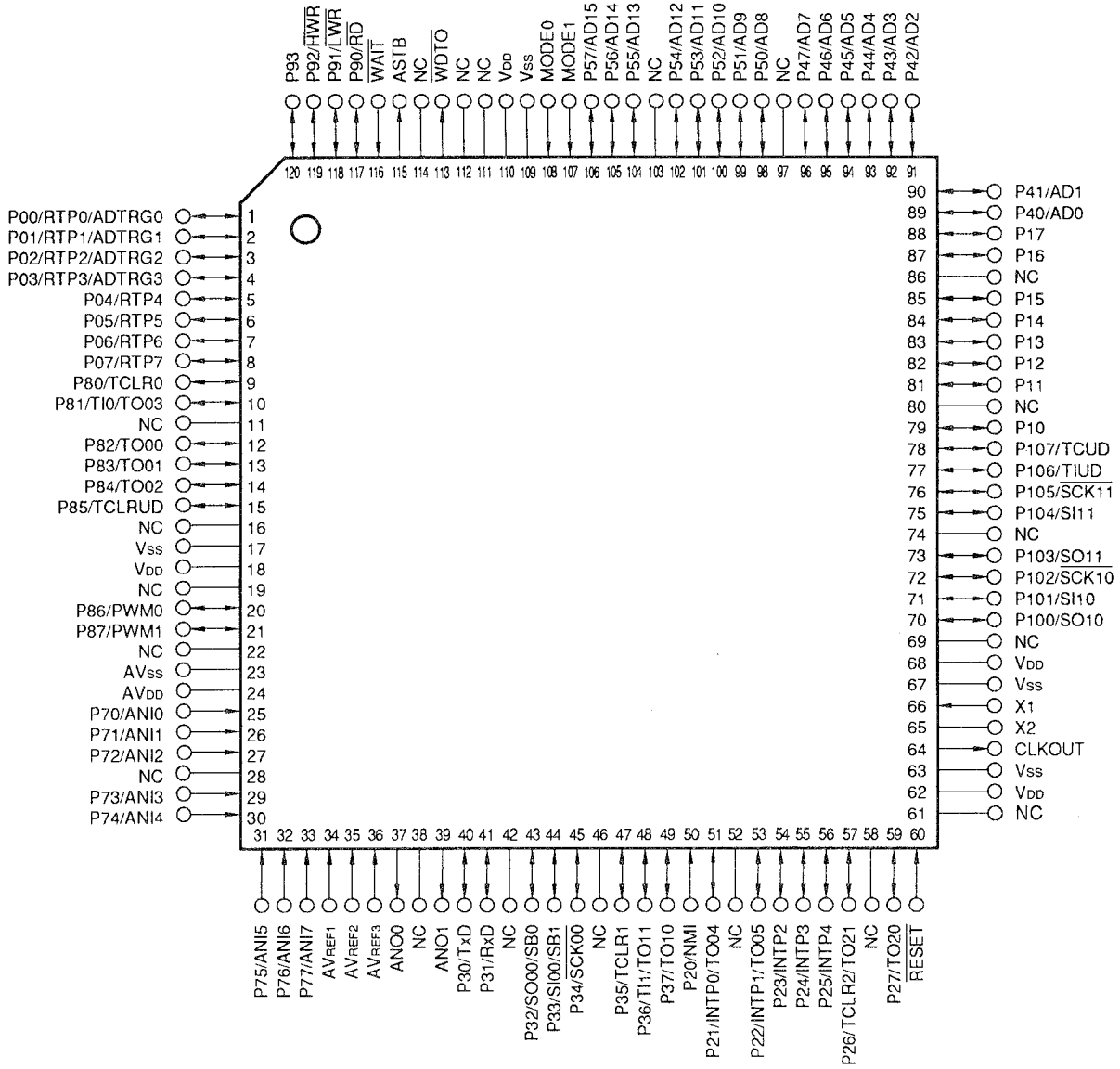


Caution Connect the MODE0 and MODE1 pins directly to the Vss pins.

Remark Pin compatible with the μPD78356GC

- **120-pin plastic QFP (28 × 28 mm)**
  μPD78P356GD-5BB

- **120-pin ceramic WQFN**
  μPD78P356KP-S



Caution **Connect the MODE0 and MODE1 pins directly to the Vss pins.**

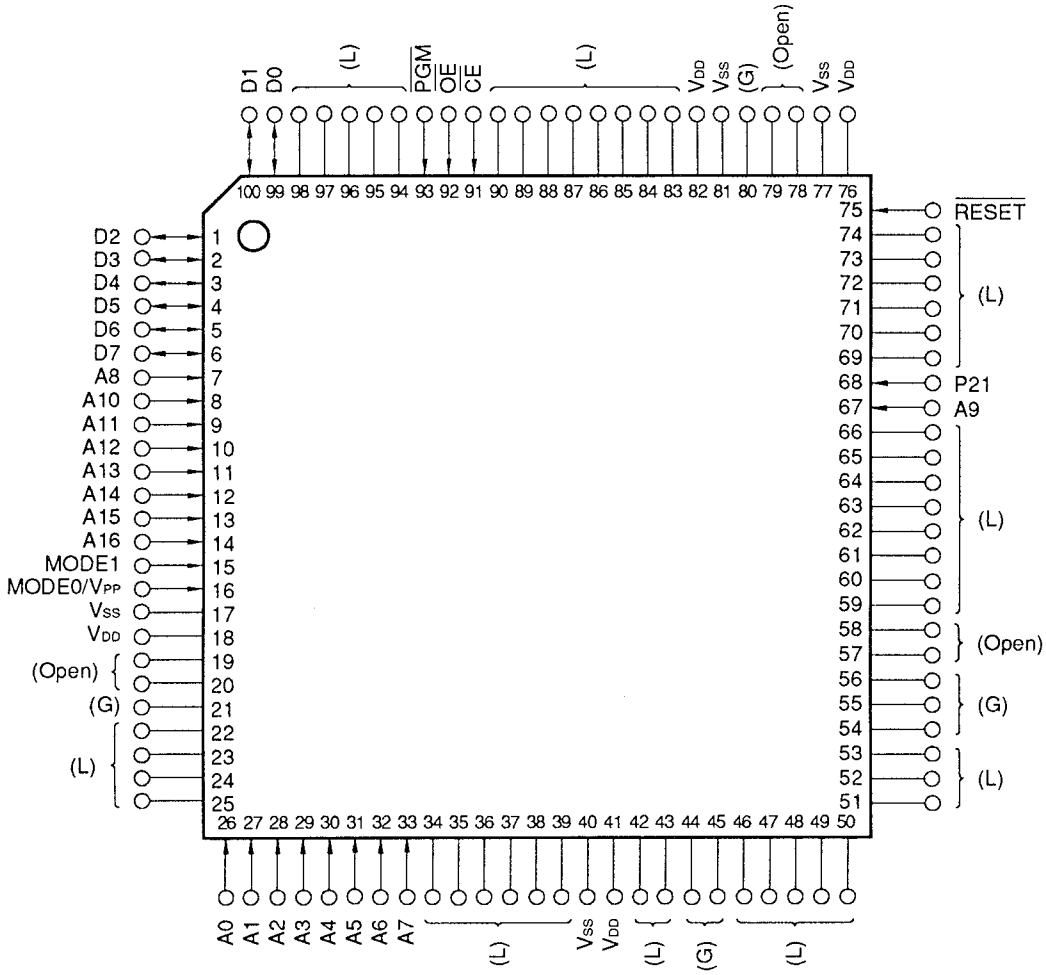
Remark Pin compatible with the μPD78356GD

P00-P07	:	Port 0
P10-P17	:	Port 1
P20-P27	:	Port 2
P30-P37	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P70-P77	:	Port 7
P80-P87	:	Port 8
P90-P93	:	Port 9
P100-P107	:	Port 10
RTP0-RTP7	:	Real-time port
NMI	:	Nonmaskable interrupt
INTP0-INTP4	:	Interrupt from peripherals
TO00-TO05	:	Timer output
TO10, TO11	:	Timer output
TO20, TO21	:	Timer output
TCLR0-TCLR2	:	Timer clear input
TCLRUD	:	Timer clear input
TI0, TI1	:	Timer input
TIUD	:	Count pulse input
TCUD	:	Control pulse input
ANI0-ANI7	:	Analog input
ADTRG0-ADTRG3	:	A/D trigger input
ANO0, ANO1	:	Analog output
TxD	:	Transmit data
RxD	:	Receive data

SI00, SI10	:	Serial input
SI11	:	Serial input
SO00, SO10	:	Serial output
SO11	:	Serial output
SB0, SB1	:	Serial bus
$\overline{SCK00}$, $\overline{SCK10}$	:	Serial clock
$\overline{SCK11}$	:	Serial clock
PWM0, PWM1	:	Pulse width modulation output
$\overline{WDTO}$	:	Watchdog timer output
MODE0, MODE1	:	Mode
AD0-AD15	:	Address/data bus
ASTB	:	Address strobe
$\overline{RD}$	:	Read strobe
$\overline{LWR}$	:	Low-address write strobe
$\overline{HWR}$	:	High-address write strobe
$\overline{WAIT}$	:	Wait
CLKOUT	:	Clock output
$\overline{RESET}$	:	Reset
X1,X2	:	Crystal
AV_{DD}	:	Analog V_{DD}
AV_{SS}	:	Analog Vss
AV_{REF1}-AV_{REF3}	:	Analog reference voltage
V_{DD}	:	Power supply
Vss	:	Ground
NC	:	No connection

(2) PROM programming mode (MODE0/V_{PP} = +5 V, MODE1 = G, P21 = G, $\overline{RESET}$ = G)

- **100-pin plastic QFP (14 × 14 mm)**
  μPD78P356GC-7EA



Caution Symbols in parentheses denote how the pins not used in the PROM programming mode should be treated.

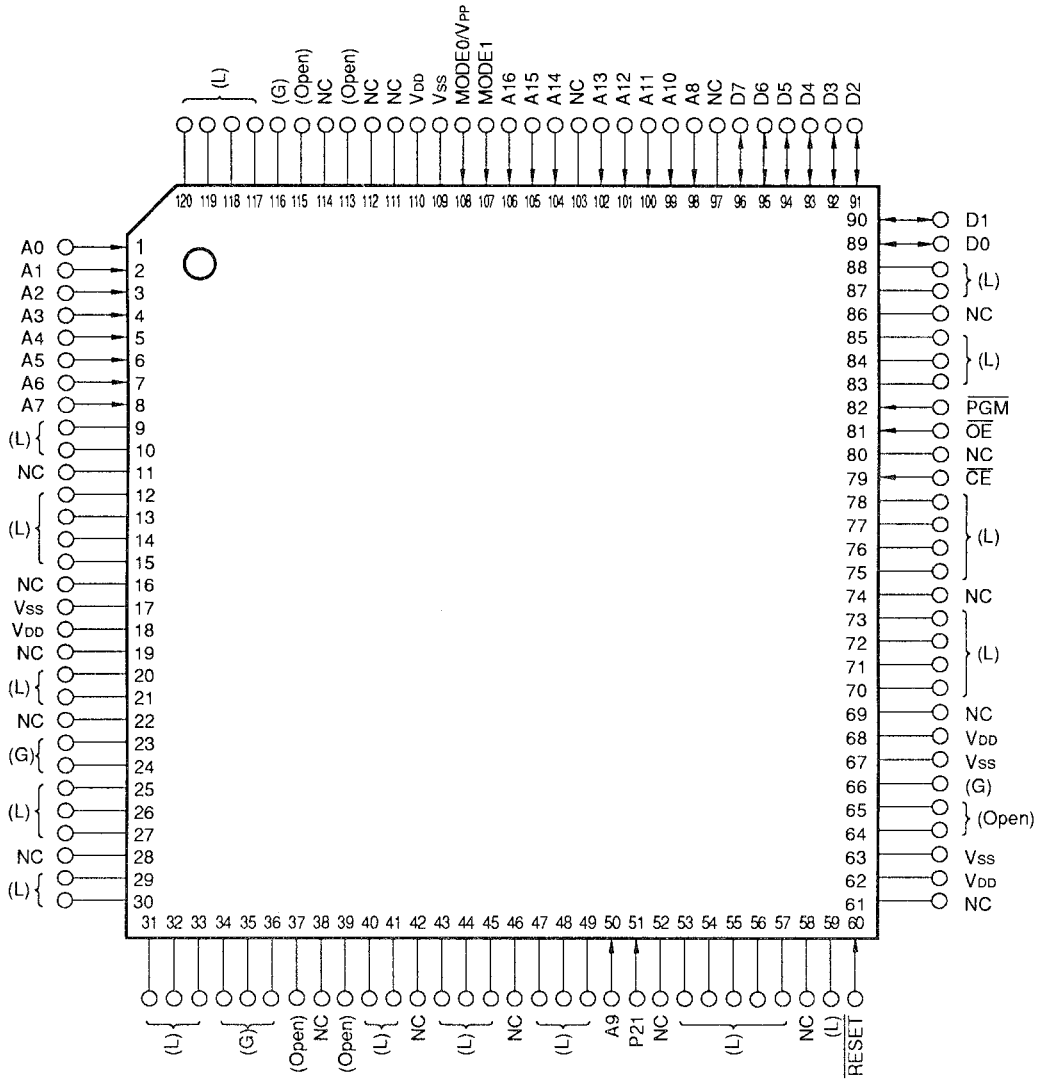
L : Connect these pins to the V_{SS} pins through separate resistors.

G : Connect these pins to the V_{SS} pins.

Open: Do not connect these pins to anything.

- **120-pin plastic QFP (28 × 28 mm)**
  μPD78P356GD-5BB

- **120-pin ceramic WQFN**
  μPD78P356KP-S



Caution Symbols in parentheses denote how the pins not used in the PROM programming mode should be treated.

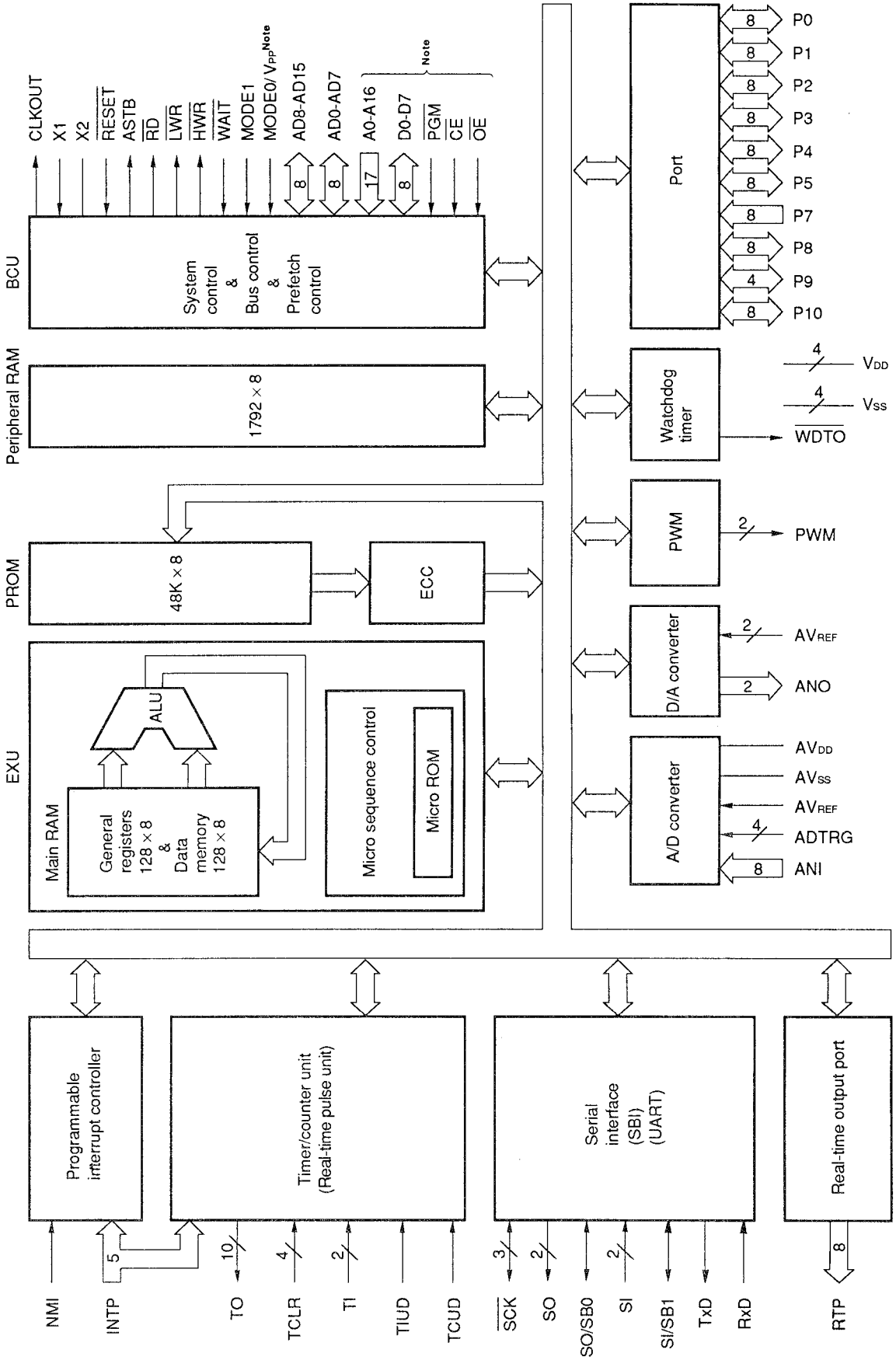
L : Connect these pins to the Vss pins through separate resistors.

G : Connect these pins to the Vss pins.

Open: Do not connect these pins to anything.

A0-A16	: Address bus	MODE0, MODE1	:	Programming mode set
D0-D7	: Data bus	P21	:	
$\overline{CE}$	: Chip enable	$\overline{RESET}$	:	
$\overline{OE}$	: Output enable	V_{DD}	:	Power supply
$\overline{PGM}$	: Programming mode	Vss	:	Ground
		V_{PP}	:	Programming power supply

BLOCK DIAGRAM



Note Pins used in the PROM programming mode

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1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE (MODE0 = L, MODE1 = L)

(1) Port pins (1/2)

Pin	I/O	Function	Dual-function pin
P00	I/O	Port 0. 8-bit I/O port. Can be specified as input or output bit by bit.	RTP0/ADTRG0
P01			RTP1/ADTRG1
P02			RTP2/ADTRG2
P03			RTP3/ADTRG3
P04-P07			RTP4-RTP7
P10-P17	I/O	Port 1. 8-bit I/O port. Can be specified as input or output bit by bit.	–
P20	I	Port 2. 8-bit I/O port. Can be specified as input or output bit by bit. (P20/NMI is excluded.)	NMI
P21	I/O		INTP0/TO04
P22			INTP1/TO05
P23			INTP2
P24			INTP3
P25			INTP4
P26			TCLR2/TO21
P27			TO20
P30	I/O	Port 3. 8-bit I/O port. Can be specified as input or output bit by bit.	TxD
P31			RxD
P32			SO00/SB0
P33			SI00/SB1
P34			$\overline{SCK00}$
P35			TCLR1
P36			TI1/TO11
P37			TO10
P40-P47	I/O	Port 4. 8-bit I/O port. Can be specified as input or output in units of 8 bits.	AD0-AD7
P50-P57	I/O	Port 5. 8-bit I/O port. Can be specified as input or output bit by bit.	AD8-AD15
P70-P77	I	Port 7. Port used only for 8-bit input.	ANI0-ANI7

(1) Port pins (2/2)

Pin	I/O	Function	Dual-function pin
P80	I/O	Port 8. 8-bit I/O port. Can be specified as input or output bit by bit.	TCLR0
P81			TI0/TO03
P82			TO00
P83			TO01
P84			TO02
P85			TCLRUD
P86			PWM0
P87			PWM1
P90	I/O	Port 9. 4-bit I/O port. Can be specified as input or output bit by bit.	$\overline{RD}$
P91			$\overline{LWR}$
P92			$\overline{HWR}$
P93			–
P100	I/O	Port 10. 8-bit I/O port. Can be specified as input or output bit by bit.	SO10
P101			SI10
P102			$\overline{SCK10}$
P103			SO11
P104			SI11
P105			$\overline{SCK11}$
P106			TIUD
P107			TCUD

(2) Non-port pins (1/2)

Pin	I/O	Function	Dual-function pin
RTP0	O	Outputs a pulse in real time as triggered by a trigger signal sent from the real-time pulse unit.	P00/ADTRG0
RTP1			P01/ADTRG1
RTP2			P02/ADTRG2
RTP3			P03/ADTRG3
RTP4-RTP7			P04-P07
NMI	I	Nonmaskable interrupt request input	P20
INTP0		External interrupt request input	P21/TO04
INTP1			P22/TO05
INTP2			P23
INTP3			P24
INTP4			P25
TI0	I	External count clock input to timer 0	P81/TO03
TI1		External count clock input to timer 1	P36/TO11
TIUD		External count clock input to the up/down counter	P106
TCUD		Input for the control signal to determine whether the up/down counter counts up or down.	P107
TCLR0		Clear signal input to the real-time pulse unit	P80
TCLR1			P35
TCLR2			P26/TO21
TCLRUD			P85
TO00	O	Timer output from the real-time pulse unit (RPU)	P82
TO01			P83
TO02			P84
TO03			P81/TI0
TO04			P21/INTP0
TO05			P22/INTP1
TO10			P37
TO11			P36/TI1
TO20			P27
TO21			P26/TCLR2
ANI0-ANI7	I	Analog input to the A/D converter	P70-P77
ADTRG0		External trigger signal input to the A/D converter	P00/RTP0
ADTRG1			P01/RTP1
ADTRG2			P02/RTP2
ADTRG3			P03/RTP3
ANO0	O	Analog output from the D/A converter	–
ANO1			–
TxD	O	Serial data output from the asynchronous serial interface	P30
RxD	I	Serial data input to the asynchronous serial interface	P31

(2) Non-port pins (2/2)

Pin	I/O	Function	Dual-function pin
$\overline{SCK00}$	I/O	Serial clock I/O for the clock synchronous serial interface	P34
$\overline{SCK10}$			P102
$\overline{SCK11}$			P105
SI00	I	Serial data input to the clock synchronous serial interface in the 3-wire mode	P33/SB1
SI10			P101
SI11			P104
SO00	O	Serial data output from the clock synchronous serial interface in the 3-wire mode	P32/SB0
SO10			P100
SO11			P103
SB0	I/O	Serial data I/O for the clock synchronous serial interface in the SBI mode	P32/SO00
SB1			P33/SI00
PWM0	O	PWM signal output	P86
PWM1			P87
$\overline{WDTO}$	O	Output for the signal which indicates the watchdog timer overflowed. (A nonmaskable interrupt is generated.)	–
AD0-AD7	I/O	Lower-order bits of the multiplexed address/data bus used when external memory is expanded	P40-P47
AD8-AD15		Higher-order bits of the multiplexed address/data bus used when external memory is expanded	P50-P57
ASTB	O	Output for the timing signal used in externally latching address information output from the AD0 to AD15 pins, in order to access the external memory	–
$\overline{RD}$		Read strobe signal output to the external memory	P90
$\overline{LWR}$		Write strobe signal output to the 8 low-order bits in the external memory	P91
$\overline{HWR}$		Write strobe signal output to the 8 high-order bits in the external memory	P92
$\overline{WAIT}$	I	Input for the control signal which causes wait in the bus cycle	–
MODE0	I	Input for the control signal which sets the operation mode. Normally, both MODE0 and MODE1 are directly connected to the Vss pin.	–
MODE1			
CLKOUT	O	System clock output	–
$\overline{RESET}$	I	System reset input	–
X1	I	Crystal input pin for the system clock. A clock signal provided externally is input to the X1 pin. The X2 pin is left open.	–
X2	–		
AV_{REF1}	I	A/D converter reference voltage input	–
AV_{REF2}		D/A converter reference voltage input	–
AV_{REF3}			–
AV_{DD}	–	Analog power supply for the A/D converter	–
AV_{SS}	–	Ground for the A/D converter	–
V_{DD}	–	Positive power supply	–
V_{SS}	–	Ground	–
NC	–	Not internally connected. Connect the NC pin to the Vss pin (can also be left open).	–

1.2 PROM PROGRAMMING MODE (MODE0/V_{PP} = H, MODE1 = L, P21 = L, $\overline{\text{RESET}}$ = L)

Pin	I/O	Function
MODE0/V_{PP}	I	PROM programming mode set/programming supply voltage
MODE1	I	PROM programming mode set
P21		
$\overline{\text{RESET}}$		
A0-A16	I	Address bus
D0-D7	I/O	Data bus
$\overline{\text{PGM}}$	I	Program input
$\overline{\text{CE}}$	I	Enable PROM
$\overline{\text{OE}}$	I	Read strobe to PROM
V_{DD}	–	Positive power supply
V_{SS}		GND

Caution Connect the MODE0/V_{PP}, MODE1, P21, and $\overline{\text{RESET}}$ pins directly to the V_{DD} or V_{SS} pin.

1.3 INPUT/OUTPUT CIRCUIT TYPE FOR EACH PIN AND HANDLING OF UNUSED PINS

Table 1-1 lists the input and output circuit type for each pin and how to handle it when it is not used. Fig. 1-1 shows the circuits.

Table 1-1 Input/Output Circuit Type for Each Pin and Recommended Connection Methods for Unused Pins (1/2)

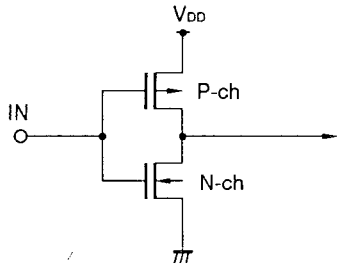
Pin	I/O circuit type	Recommended connection method
P00/RTP0/ADTRG0-P03/RTP3/ADTRG3	8-A	Input state : Each pin is connected to the V_{DD} or V_{SS} pin via a separate resistor. Output state : Open
P04/RTP4-P07/RTP7	5-A	
P10-P17		
P20/NMI	2	Connected to the V_{SS} pin.
P21/INTP0/TO04	8-A	Input state : Each pin is connected to the V_{DD} or V_{SS} pin via a separate resistor. Output state : Open
P22/INTP1/TO05		
P23/INTP2		
P24/INTP3		
P25/INTP4		
P26/TCLR2/TO21		
P27/TO20		
P30/TxD	5-A	
P31/RxD		
P32/SO00/SB0	10-A	
P33/SI00/SB1		
P34/$\overline{SCK00}$	8-A	
P35/TCLR1		
P36/TI1/TO11		
P37/TO10	5-A	
P40/AD0-P47/AD7		
P50/AD8-P57/AD15		
P70/ANI0-P77/ANI7	9	Connected to the V_{SS} pin.
P80/TCLR0	8-A	Input state : Each pin is connected to the V_{DD} or V_{SS} pin via a separate resistor. Output state : Open
P81/TI0/TO03		
P82/TO00	5-A	
P83/TO01		
P84/TO02		
P85/TCLRUD	8-A	
P86/PWM0	5-A	
P87/PWM1		
P90/$\overline{RD}$		
P91/$\overline{LWR}$		
P92/$\overline{HWR}$		
P93		

Table 1-1 Input/Output Circuit of Type for Each Pin and Recommended Connection Methods for Unused Pins (2/2)

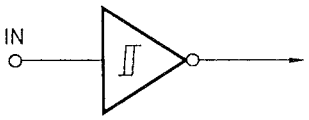
Pin	I/O circuit type	Recommended connection method
P100/SO10	5-A	Input state : Each pin is connected to the V_{DD} or V_{SS} pin via a separate resistor. Output state : Open
P101/SI10	8-A	
P102/$\overline{SCK10}$		
P103/SO11	5-A	
P104/SI11	8-A	
P105/$\overline{SCK11}$		
P106/TIUD		
P107/TCUD		
ANO0, ANO1	12	Open
CLKOUT	3	
ASTB	4	
$\overline{WDTO}$	19	Connected to the V_{SS} pin.
$\overline{WAIT}$	1	Connected to the V_{DD} pin.
MODE0, MODE1	1	–
$\overline{RESET}$	2	
AV_{REF1}-AV_{REF3}, AV_{SS}	–	Connected to the V_{SS} pin.
AV_{DD}		Connected to the V_{DD} pin.
NC		Connected to the V_{SS} pin (or open).

Fig. 1-1 Input/Output Circuits of Each Pin

Type 1

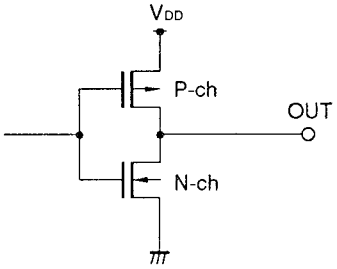


Type 2

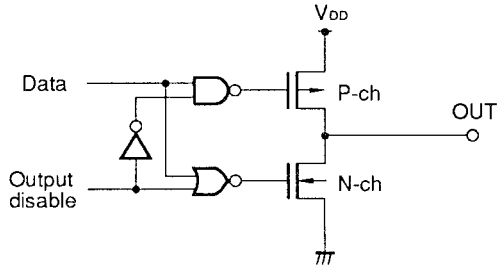


Schmitt trigger input with hysteresis characteristics

Type 3

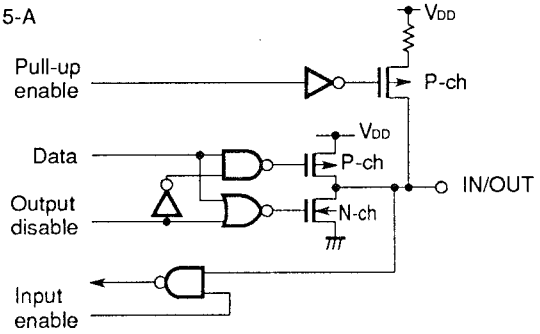


Type 4

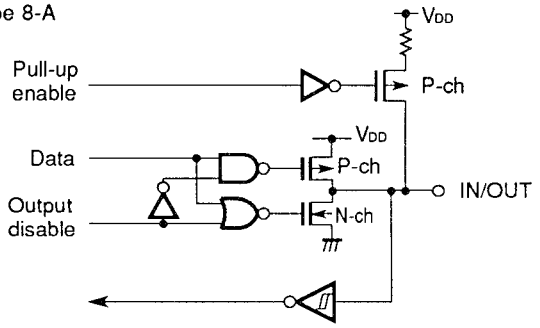


Push-pull output which can output high impedance
(Both the positive and negative channels are off.)

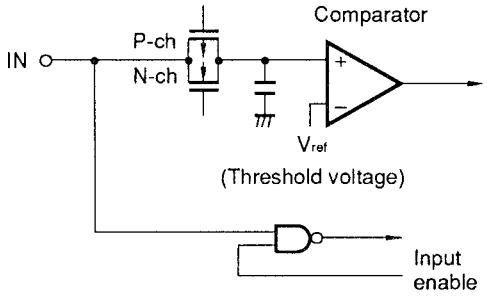
Type 5-A



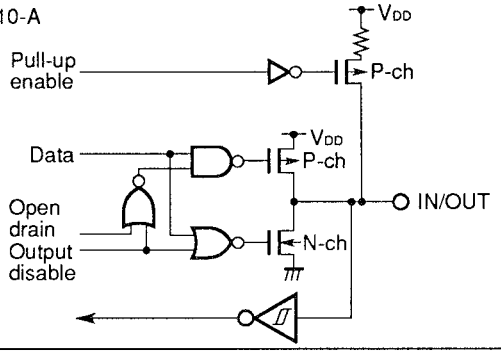
Type 8-A



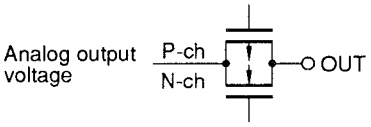
Type 9



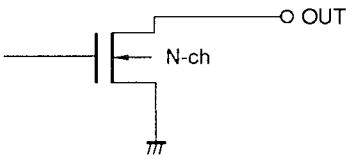
Type 10-A



Type 12



Type 19



2. DIFFERENCES BETWEEN THE μPD78P356 AND μPD78356

The μPD78P356 is produced by replacing the internal mask ROM of the μPD78356 with a 48K-byte PROM. Both have the same functions except some differences in ROM specifications, such as write and verify modes. Table 2-1 shows the differences.

In this manual, the functions specific to the μPD78P356 are explained. For details of the other functions, refer to the μPD78356 document.

Table 2-1 Differences between the μPD78P356 and μPD78356

Item \ Part number	μPD78P356		μPD78356
Internal program memory (Electrical write)	One-time PROM (Data can be written once)	EPROM (Data can be written multiple times)	Mask ROM
ECC circuit	Provided		Not provided
PROM programming terminal	Provided		Not provided
Setting of MODE0 and MODE1	• Normal operation mode MODE0, 1 = LL • Programming mode MODE0, 1 = HL • ROM-less mode (with an external 16-bit bus) MODE0, 1 = HH		• Normal operation mode MODE0, 1 = LL • ROM-less mode (with an external 8-bit bus) MODE0, 1 = HL (with an external 16-bit bus) MODE0, 1 = HH
Package	• 100-pin plastic QFP • 120-pin plastic QFP	• 120-pin ceramic WQFN	• 100-pin plastic QFP • 120-pin plastic QFP
Electrical characteristics	They differ in supply current and other factors.		
Others	Since they differ in circuit scale and mask layout, they differ in noise immunity and noise radiation.		

Cautions 1. The PROM and mask ROM products differ in noise immunity and noise radiation. Use not ES products but CS products (mask ROM products) to evaluate them thoroughly when considering the change from the PROM products to the mask ROM products during processes from preproduction to volume production.

2. Connect the MODE0 and MODE1 pins directly to the V_{DD} or V_{SS} pin.

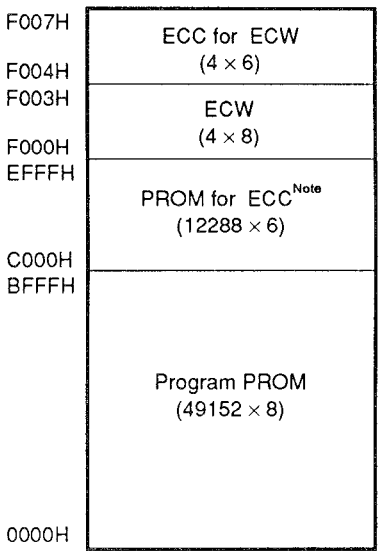
3. PROM PROGRAMMING

The μPD78P356 is provided with an electrically writable PROM of 48K × 8 bits for programming and a PROM of 12K × 6 bits for error correcting codes (ECCs).

The ECCs correct errors of the codes written in the programming PROM, improving the reliability of data stored in the PROM.

Fig. 3-1 shows the memory map in the programming mode.

Fig. 3-1 Memory Map in the Programming Mode



Note The six low-order bits are effective in the ECC PROM.

Before programming the PROM, input appropriate signals to the MODE0/V_{PP}, MODE1, P21, and $\overline{\text{RESET}}$ pins to change the mode to the PROM programming mode.

Program the PROM in the same way as for the μPD27C1001A.

To use the ECCs, reset the lowest-order bit (F000.0) in the lowest-order byte of ECW (ECC control word) to enable the ECC circuit operation. The ECW is a 4-byte register for controlling the ECC circuit operation.

The ECCs and ECW are automatically generated by ECCGEN (ECC generator) supplied with the RA78K3 assembler package. (The ECCs are generated in the six low-order bits of the PROM. The two high-order bits are fixed to 1.)

Table 3-1 Pin Functions in Programming Mode

Function	Normal operation mode	Programming mode
Address input	P00-P07, P50, P20, P51-P57	A0-A16
Data input	P40-P47	D0-D7
Program pulse	P12	$\overline{\text{PGM}}$
Chip enable	P10	$\overline{\text{CE}}$
Output enable	P11	$\overline{\text{OE}}$
Program voltage	MODE0/V_{PP}	
Mode voltage	MODE1, P21, $\overline{\text{RESET}}$	

3.1 OPERATION MODE

To enter the program write/verify mode, set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, $\overline{RESET}$ = L. In addition, any of the operation modes listed in Table 3-2 can be selected by setting the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins in this mode.

Set the μPD78P356 to the read mode in order to read the contents of PROM.

Handle unused pins according to the caution in PIN CONFIGURATION (2).

Table 3-2 Operation Modes for PROM Programming

Mode	MODE1	P21	$\overline{RESET}$	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	MODE0/V_{PP}	V_{DD}	D0-D7
Page data latch	L	L	L	H	L	H	+12.5 V	+6.5 V	Data input
Page program				H	H	L			High impedance
Byte program				L	H	L			Data input
Program verify				L	L	H			Data output
Program inhibit				×	L	L			High impedance
				×	H	H			
Read				L	L	H	+5 V	+5 V	Data output
Output disable				L	H	×			High impedance
Standby				H	×	×			High impedance

Remark L : Directly connected to the Vss pin
H : Directly connected to the V_{DD} pin
× : L or H

3.2 PROCEDURE FOR WRITING ON PROM (PAGE PROGRAM MODE)

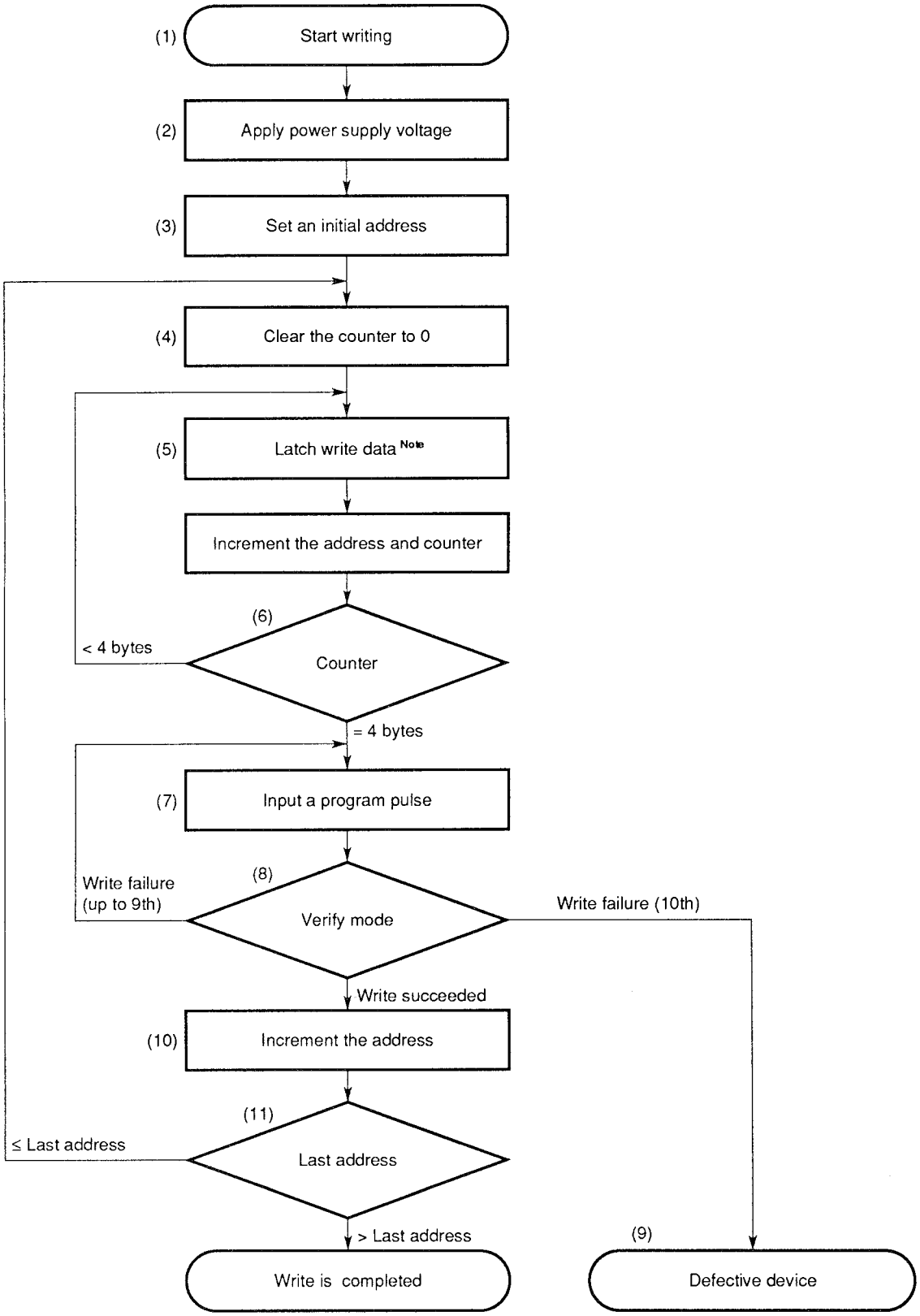
The following is a procedure for writing on PROM. (See **Fig. 3-2**.)

In the page program mode, data is written in units of pages (four bytes). When write data completes midway of a page, latch FFH after the data so that the data fits into pages.

(1) Always set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, and $\overline{RESET}$ = L. Connect unused pins according to PIN CONFIGURATION (2).
(2) Apply +6.5 V to the V_{DD} pin and +12.5 V to the MODE0/V_{PP} pin.
(3) Input an initial address to the A0 to A16 pins.
(4) Clear the page counter.
(5) Data latch mode. Input write data to the D0 to D7 pins and input an active-low pulse to the $\overline{OE}$ pin. Increment the address and the page counter.
(6) Repeat step (5) for a page (four bytes).
(7) Input a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin.
(8) Verify mode. Checks if data has been written in PROM.
Apply a low level to the $\overline{CE}$ pin, input an active-low pulse to the $\overline{OE}$ pin, and then read the write data from the D0 to D7 pins. Repeat this for a page (four bytes). When verification completes, apply a high level to the $\overline{CE}$ pin.
  - If data has been written, go to step (10).
  - If not, repeat steps (7) and (8). If no data is written yet after the steps have been repeated 10 times, go to step (9).
(9) Assume the device to be defective and stop write operation.
(10) Increment the address.
(11) Repeat steps (4) to (10) until the address exceeds the last address.

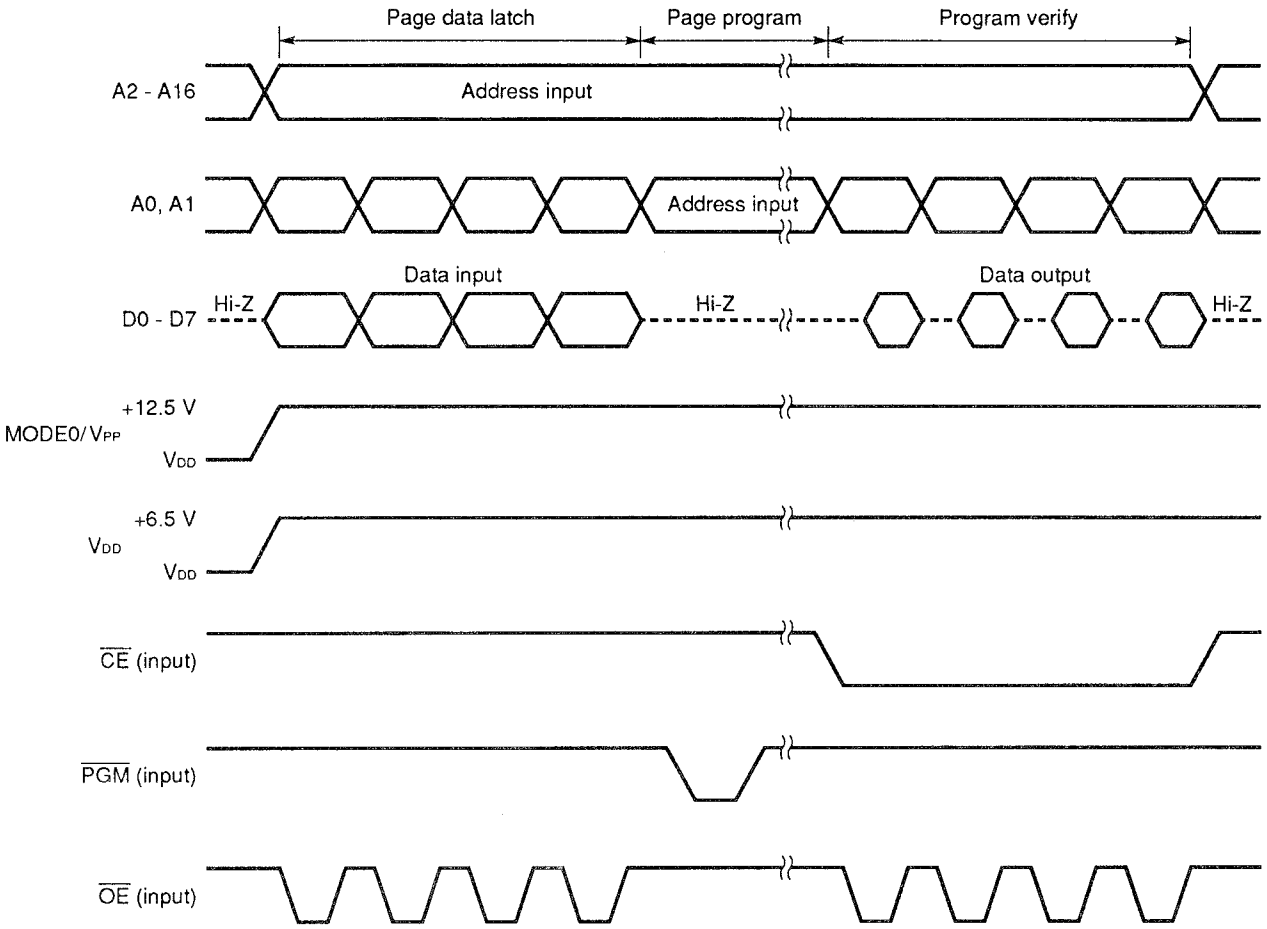
Fig. 3-3 is a timing chart of these steps (2) to (9).

Fig. 3-2 Flowchart of Procedure for Writing (Page Program Mode)



Note If write data does not fill a page, latch FFH for the rest of the page.

Fig. 3-3 PROM Write/Verify Timing Chart (Page Program Mode)



3.3 PROCEDURE FOR WRITING ON PROM (BYTE PROGRAM MODE)

The following is a procedure for writing on PROM. (See **Fig. 3-4**.)

(1) Always set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, and $\overline{RESET}$ = L. Connect unused pins according to PIN CONFIGURATION (2).
(2) Apply +6.5 V to the V_{DD} pin and +12.5 V to the MODE0/V_{PP} pin, and input a low-level signal to the $\overline{CE}$ pin.
(3) Input an initial address to the A0 to A16 pins.
(4) Input write data to the D0 to D7 pins.
(5) Input a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin.
(6) Verify mode. Checks if data has been written in PROM.
Input an active-low pulse to the $\overline{OE}$ pin and read the write data from the D0 to D7 pins.
- If data has been written, go to step (8).
- If not, repeat steps (4) to (6). If no data is written yet after the steps have been repeated 10 times, go to step (7).

(7) Assume the device to be defective and stop write operation.
(8) Increment the address.
(9) Repeat steps (4) to (8) until the address exceeds the last address.

Fig. 3-5 is a timing chart of these steps (2) to (7).

Fig. 3-4 Flowchart of Procedure for Writing (Byte Program Mode)

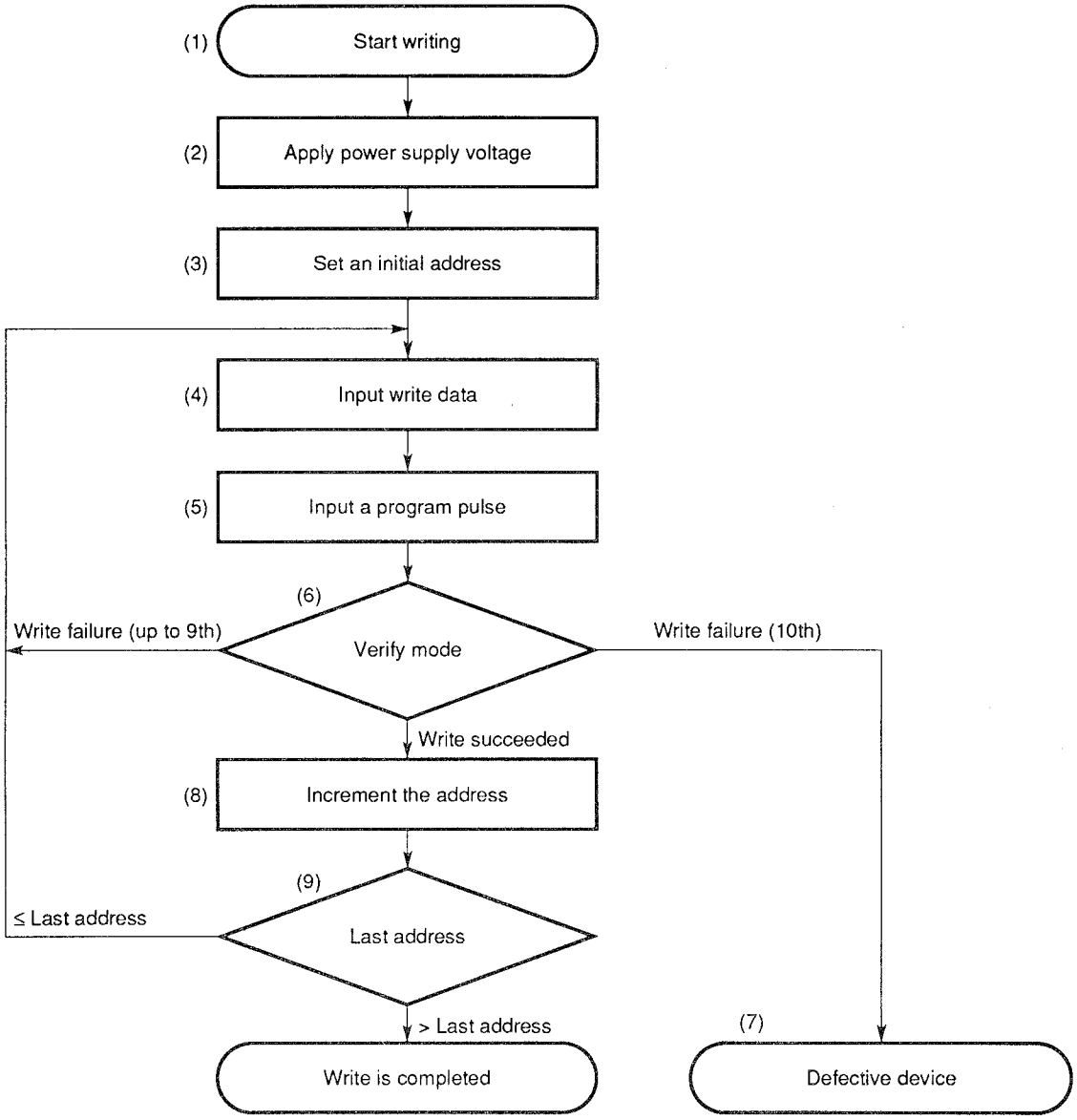
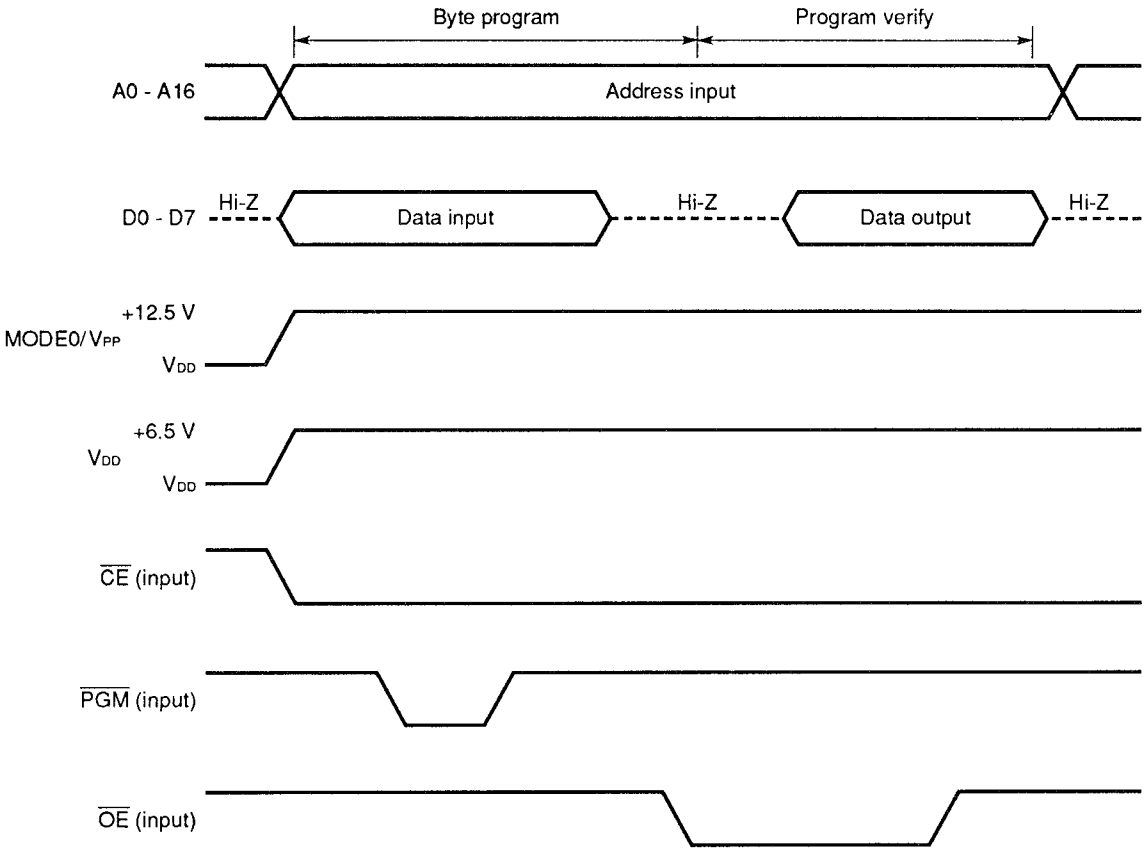


Fig. 3-5 PROM Write/Verify Timing Chart (Byte Program Mode)



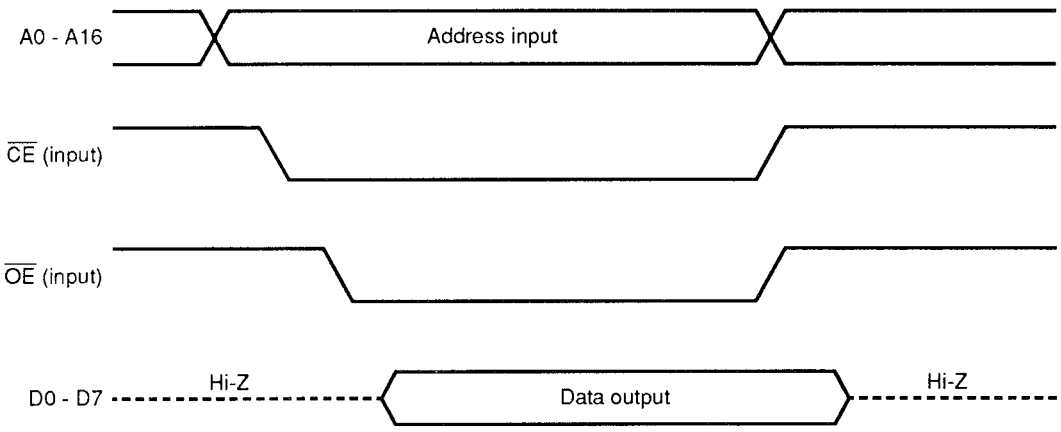
3.4 PROCEDURE FOR READING FROM PROM

The following is a procedure for reading out the contents of PROM to the external data bus (D0 to D7).

(1) Always set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, and $\overline{RESET}$ = L. Connect unused pins according to PIN CONFIGURATION (2).
(2) Apply +5 V to the V_{DD} and MODE0/V_{PP} pins.
(3) Input the address of data to be read into the A0 to A16 pins.
(4) Read mode ($\overline{CE}$ = L, $\overline{OE}$ = L)
(5) Output the data on the D0 to D7 pins.

Fig. 3-6 is a timing chart of these steps (2) to (5).

Fig. 3-6 PROM Read Timing Chart



4. ERASURE CHARACTERISTICS (μPD78P356KP-S ONLY)

Data written in the μPD78P356KP-S program memory can be erased (FFH); therefore users can write other data in the memory.

To erase the written data, expose the erasure window to light with a wavelength shorter than approx. 400 nm. Normally, ultraviolet light with a wavelength of 254 nm is employed. The amount of light required to completely erase the data is as follows:

- Intensity of ultraviolet light × erasing time: 15 W•s/cm² min.
- Erasing time: 15 to 20 minutes (When using a 12,000 μW/cm² ultraviolet lamp. It may, however, take more time due to lamp deterioration, dirt on the erasure window, or the like.)

The ultraviolet lamp should be placed within 2.5 cm from the erasure window during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

5. PROTECTIVE FILM COVERING THE ERASURE WINDOW (μPD78P356KP-S ONLY)

After the erasure window of the μPD78P356KP-S has been exposed to sunlight or a fluorescent lamp for a long time, data in EPROM may be erased and the internal circuits may malfunction. To prevent these failures, the erasure window should be covered with a protective film when it is not used for erasure.

EPROM package products with a window are supplied with a NEC-guaranteed protective film when they are delivered.

6. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products (μPD78P356GC-7EA, μPD78P356GD-5BB) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125 °C for 24 hours.

NEC offers a charged service called QTOP microcomputer service. This service includes writing to one-time PROM, marking, screening, and verification. For the μPD78P356, this service is yet to be supported. Ask your sales representative for details.

7. ELECTRICAL CHARACTERISTICS ★

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			−0.5 to +7.0	V
	AV_{DD}			−0.5 to V_{DD} + 0.5	V
	V_{PP}			−0.5 to +13.5	V
	AV_{SS}			−0.5 to +0.5	V
Input voltage	V_I	Note 1		−0.5 to V_{DD} + 0.5	V
Output voltage	V_O			−0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	Each pin		4.0	mA
		Total of all output pins		140	mA
High-level output current	I_{OH}	Each pin		−1.0	mA
		Total of all output pins		−30	mA
Analog input voltage	V_{IAN}	Note 2	$AV_{DD} > V_{DD}$	−0.5 to V_{DD} + 0.5	V
			$V_{DD} \geq AV_{DD}$	−0.5 to AV_{DD} + 0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	−0.5 to V_{DD} + 0.5	V
			$V_{DD} \geq AV_{DD}$	−0.5 to AV_{DD} + 0.5	
Operating temperature	T_A			−10 to +70	°C
Storage temperature	T_{stg}			−65 to +150	°C

Notes 1. Pins other than those listed below
2. P70/ANI0 - P77/ANI7

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

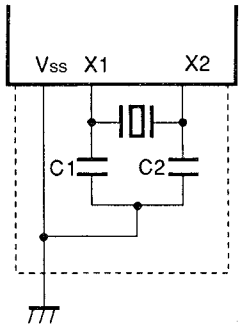
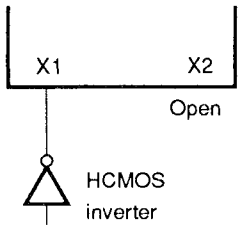
RECOMMENDED OPERATING CONDITIONS

Oscillator frequency	T_A	V_{DD}
8 MHz ≤ fxx ≤ 32 MHz	−10 to +70 °C	+5.0 V ±10 %

CAPACITANCE (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f = 1 MHz 0 V on pins other than measured pins			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

OSCILLATOR CHARACTERISTICS (T_A = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Ceramic resonator or crystal		Oscillator frequency (f_{XX})	8	32	MHz
External clock		X1 input frequency (f_X)	8	32	MHz
		X1 input rising and falling times (t_{XR}, t_{XF})	0	10	ns
		X1 input high-level and low-level widths (t_{WXH}, t_{WXL})	10	115	ns

Caution When using the system clock generator, run wires in the portion surrounded by dotted lines according to the following rules to avoid effects such as stray capacitance:

- **Minimize the wiring.**
- **Never cause the wires to cross other signal lines or run near a line carrying a large varying current.**
- **Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS}. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

DC CHARACTERISTICS (T_A = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Note 1		2.2			V
	V_{IH2}	Note 2		0.8V_{DD}			
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = −400 μA		V_{DD} − 1.0			V
Input leakage current	I_{LI}	Note 3	0 V ≤ V_I ≤ V_{DD}			±10	μA
		MODE0/V_{PP} pin	V_I = V_{DD}			+10	μA
			V_I = 0 V			−200	μA
Analog pin input leakage current	I_{LIAN}	Note 4	0 V ≤ V_I ≤ AV_{REF}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode			86	125	mA
	I_{DD2}	HALT mode			40	60	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	20	μA
			V_{DDDR} = 5.0 V ±10 %		10	50	μA
Software pull-up resistance	R_L	V_I = 0 V		20	40	90	kΩ

Notes 1. For pins other than those described in Note 2

2. $\overline{\text{RESET}}$, X1, X2, P00/RTP0/ADTRG0, P01/RTP1/ADTRG1, P02/RTP2/ADTRG2, P03/RTP3/ADTRG3, P20/NMI, P21/INTP0/TO04, P22/INTP1/TO05, P23/INTP2, P24/INTP3, P25/INTP4, P26/TCLR2/TO21, P27/TO20, P32/SO00/SB0, P33/SI00/SB1, P34/$\overline{\text{SCK00}}$, P35/TCLR1, P36/TI1/TO11, P80/TCLR0, P81/TI0/TO03, P85/TCLRUD, P101/SI10, P102/$\overline{\text{SCK10}}$, P104/SI11, P105/$\overline{\text{SCK11}}$, P106/TIUD, and P107/TCUD

3. For input and input/output pins (excluding MODE0/V_{PP}, X1, X2, and P70/ANI0 to P77/ANI7 being used for analog input.)

4. For P70/ANI0 to P77/ANI7 (only when being used for analog input, during nonsampling operation)

AC CHARACTERISTICS (T_A = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V, C_L = 100 pF, f_{XX} = 32 MHz)

Read/Write Operation (When the General Memory Is Connected)

Parameter	Symbol	Conditions	Min.	Max.	Unit
System clock cycle time	t_{CYK}		62.5	250	ns
Address setup time (to ASTB ↓)	t_{SAST}		7		ns
Address hold time (to ASTB ↓)	t_{HSTA}		11		ns
Delay from $\overline{RD}$ ↓ to address float	t_{FRA}			0	ns
Delay from address to data input	t_{DAID}			100	ns
Delay from $\overline{RD}$ ↓ to data input	t_{DRID}			49	ns
Delay from ASTB ↓ to $\overline{RD}$ ↓	t_{DSTR}		15		ns
Data hold time (to $\overline{RD}$ ↑)	t_{HRID}		0		ns
Delay from $\overline{RD}$ ↑ to address active	t_{DRA}		17		ns
$\overline{RD}$ low-level width	t_{WRL}		63		ns
ASTB high-level width	t_{WSTH}		14		ns
Delay from $\overline{LWR}$, $\overline{HWR}$ ↓ to data output	t_{DWOD}			21	ns
Delay from ASTB ↓ to $\overline{LWR}$, $\overline{HWR}$ ↓	t_{DSTW}		15		ns
Delay from $\overline{LWR}$, $\overline{HWR}$ ↑ to ASTB ↑	t_{DWST}		78		ns
Data setup time (to $\overline{LWR}$, $\overline{HWR}$ ↑)	t_{SODW}		57		ns
Data hold time (to $\overline{LWR}$, $\overline{HWR}$ ↑)	t_{HWOD}		8		ns
$\overline{LWR}$, $\overline{HWR}$ low-level width	t_{WWL}		63		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT}			47	ns
$\overline{WAIT}$ hold time (to address)	t_{HAWT}		93		ns
$\overline{WAIT}$ setup time (to ASTB ↓)	t_{SASRY}			15	ns
$\overline{WAIT}$ hold time (to ASTB ↓)	t_{HASRY}		62		ns
$\overline{WAIT}$ setup time (to $\overline{RD}$ ↓)	t_{SRRY}			−25	ns
$\overline{WAIT}$ setup time (to $\overline{LWR}$, $\overline{HWR}$ ↓)	t_{SWRY}			−25	ns
$\overline{WAIT}$ hold time (to $\overline{RD}$ ↓)	t_{HRRY}		22		ns
$\overline{WAIT}$ hold time (to $\overline{LWR}$, $\overline{HWR}$ ↓)	t_{HWRY}		22		ns
Delay from address to $\overline{RD}$ ↓	t_{DAR}			77	ns
Delay from address to $\overline{LWR}$, $\overline{HWR}$ ↓	t_{DAW}			77	ns
Delay from $\overline{WAIT}$ ↑ to data input	t_{DWTID}			52	ns
Delay from $\overline{WAIT}$ ↑ to $\overline{RD}$ ↑	t_{DWTR}		62		ns
Delay from $\overline{WAIT}$ ↑ to $\overline{LWR}$, $\overline{HWR}$ ↑	t_{DWTW}		62		ns

t_{CYK}-Dependent Bus Timing Definition

Symbol	Formula	Min./Max.	Unit
t_{SAST}	(0.5 + a)T – 24	Min.	ns
t_{HSTA}	0.5T – 20	Min.	ns
t_{WSTH}	(0.5 + a)T – 17	Min.	ns
t_{DSTR}	0.5T – 16	Min.	ns
t_{WRL}	(1.5 + n)T – 30	Min.	ns
t_{DAID}	(2.5 + a + n)T – 56	Max.	ns
t_{DRID}	(1.5 + n)T – 44	Max.	ns
t_{DRA}	0.5T – 14	Min.	ns
t_{DSTW}	0.5T – 16	Min.	ns
t_{DWST}	1.5T – 15	Min.	ns
t_{WWL}	(1.5 + n)T – 30	Min.	ns
t_{DWOD}	0.5T – 10	Max.	ns
t_{SODW}	(1 + n)T – 5	Min.	ns
t_{SAWT}	(a + n)T – 15	Max.	ns
t_{HAWT}	(0.5 + a + n)T	Min.	ns
t_{SASRY}	(n – 0.5)T – 16	Max.	ns
t_{HASRY}	nT	Min.	ns
t_{SRRY}	(n – 1)T – 25	Max.	ns
t_{SWRY}	(n – 1)T – 25	Max.	ns
t_{HRRY}	(n – 0.5)T – 9	Min.	ns
t_{HWRY}	(n – 0.5)T – 9	Min.	ns
t_{DAR}	(a + 1)T + 15	Max.	ns
t_{DAW}	(a + 1)T + 15	Max.	ns
t_{DWTID}	T – 10	Max.	ns
t_{DWTR}	T	Min.	ns
t_{DWTW}	T	Min.	ns

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)

2. When an address wait is inserted, the value of a is 1. Otherwise, it is 0.

3. The number n represents the number of wait cycles specified by the external wait pin ($\overline{WAIT}$) or PWC register.

4. Only the bus timing items listed above are dependent on t_{CYK}.

Serial Operation (T_A = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{SCK}$ output	Internal, divided by 8	500		ns
		$\overline{SCK}$ input	External clock	500		ns
Serial clock low-level width	t_{WSKL}	$\overline{SCK}$ output	Internal, divided by 8	210		ns
		$\overline{SCK}$ input	External clock	210		ns
Serial clock high-level width	t_{WSKH}	$\overline{SCK}$ output	Internal, divided by 8	210		ns
		$\overline{SCK}$ input	External clock	210		ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SRXSK}			80		ns
SI hold time (to $\overline{SCK}$ ↑)	t_{HSKRX}			80		ns
$\overline{SCK}$ ↓ → SO delay time	t_{DSKTX}	R = 1 kΩ, C = 100 pF			110	ns

t_{CYK}-Dependent Serial Operations

Symbol	Conditions		Formula	Min./Max.	Unit
t_{CYSK}	$\overline{SCK}$ output	Internal, divided by 8	8T	Min.	ns
	$\overline{SCK}$ input	External clock	8T	Min.	ns
t_{WSKL}	$\overline{SCK}$ output	Internal, divided by 8	4T − 40	Min.	ns
	$\overline{SCK}$ input	External clock	4T − 40	Min.	ns
t_{WSKH}	$\overline{SCK}$ output	Internal, divided by 8	4T − 40	Min.	ns
	$\overline{SCK}$ input	External clock	4T − 40	Min.	ns

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)

2. The items listed above are dependent on t_{CYK}.

Up/Down Counter Operations (T_A = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Max.	Unit
TIUD high/low level width	t_{WTIUH}, t_{WTIUL}	Other than mode 4	NIUD = 0	250		ns
			NIUD = 1	1		μs
		Mode 4	NIUD = 0	500		ns
			NIUD = 1	1		μs
TCUD high/low level width	t_{WTCUH}, t_{WTCUL}	Other than mode 4	NCUD = 0	250		ns
			NCUD = 1	1		μs
		Mode 4	NCUD = 0	500		ns
			NCUD = 1	1		μs
TCLRUD high/low level width	t_{WCLUH}, t_{WCLUL}		NRUD = 0	250		ns
			NRUD = 1	1		μs
TCUD setup time (to TIUD ↑)	t_{STCU}	Mode 3		0		ns
TCUD hold time (to TIUD ↑)	t_{HTCU}	Mode 3		125		ns
TIUD setup time (to TCUD)	t_{S4TIU}	Mode 4		250		ns
TIUD hold time (to TCUD)	t_{H4TIU}	Mode 4		250		ns
Cycle time for TIUD and TCUD	t_{CYC4}	Mode 4		1		μs

Remark NIUD, NCUD, NRUD: Bits 5, 6, and 7 of the noise protection control register (NPC)

t_{CYK}-Dependent Up/Down Counter Operations

Symbol	Conditions		Formula	Min./Max.	Unit
t_{WTIUH}, t_{WTIUL}	Other than mode 4	NIUD = 0	4T	Min.	ns
		NIUD = 1	16T		
	Mode 4	NIUD = 0	8T		
		NIUD = 1	16T		
t_{WTCUH}, t_{WTCUL}	Other than mode 4	NCUD = 0	4T	Min.	ns
		NCUD = 1	16T		
	Mode 4	NCUD = 0	8T		
		NCUD = 1	16T		
t_{WTCLUH}, t_{WTCLUL}		NRUD = 0	4T	Min.	ns
		NRUD = 1	16T		
t_{HTCU}	Mode 3		2T	Min.	ns
t_{S4TIU}	Mode 4		4T	Min.	ns
t_{H4TIU}	Mode 4		4T	Min.	ns

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)

2. The items listed above are dependent on t_{CYK}.

3. NIUD, NCUD, NRUD: Bits 5, 6, and 7 of the noise protection control register (NPC)

Other Operations (T_A = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Max.	Unit
NMI high/low level width	t_{WNIH}, t_{WNIL}	No analog noise	2		μs
INTP0 high/low level width	t_{WI0H}, t_{WI0L}		250		ns
INTP1 high/low level width	t_{WI1H}, t_{WI1L}		250		ns
INTP2 high/low level width	t_{WI2H}, t_{WI2L}		250		ns
INTP3 high/low level width	t_{WI3H}, t_{WI3L}		250		ns
INTP4 high/low level width	t_{WI4H}, t_{WI4L}		250		ns
TI0 high/low level width	t_{WTI0H}, t_{WTI0L}	NI0 = 0	250		ns
		NI0 = 1	1		μs
TI1 high/low level width	t_{WTI1H}, t_{WTI1L}	NI1 = 0	250		ns
		NI1 = 1	1		μs
TCLR0 high/low level width	t_{WCL0H}, t_{WCL0L}	NR0 = 0	250		ns
		NR0 = 1	1		μs
TCLR1 high/low level width	t_{WCL1H}, t_{WCL1L}	NR1 = 0	250		ns
		NR1 = 1	1		μs
TCLR2 high/low level width	t_{WCL2H}, t_{WCL2L}	NR2 = 0	250		ns
		NR2 = 1	1		μs
$\overline{\text{RESET}}$ high/low level width	t_{WRSH}, t_{WRSL}	No analog noise	1.5		μs

Remark NI0, NI1 : Bits 0 and 2 of the noise protection control register (NPC)
NR0, NR1, NR2: Bits 1, 3, and 4 of the noise protection control register (NPC)

Other t_{CYK}-Dependent Operations

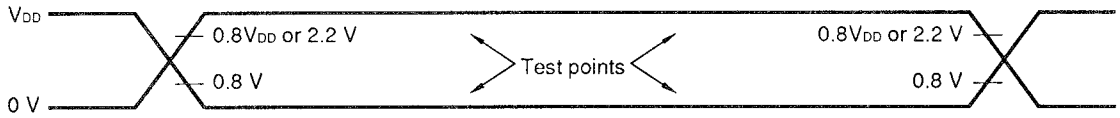
Symbol	Conditions	Formula	Min./Max.	Unit
t_{WI0H}, t_{WI0L}		4T	Min.	ns
t_{WI1H}, t_{WI1L}		4T	Min.	ns
t_{WI2H}, t_{WI2L}		4T	Min.	ns
t_{WI3H}, t_{WI3L}		4T	Min.	ns
t_{WI4H}, t_{WI4L}		4T	Min.	ns
t_{WTI0H}, t_{WTI0L}	NI0 = 0	4T	Min.	ns
	NI0 = 1	16T		
t_{WTI1H}, t_{WTI1L}	NI1 = 0	4T	Min.	ns
	NI1 = 1	16T		
t_{WCL0H}, t_{WCL0L}	NR0 = 0	4T	Min.	ns
	NR0 = 1	16T		
t_{WCL1H}, t_{WCL1L}	NR1 = 0	4T	Min.	ns
	NR1 = 1	16T		
t_{WCL2H}, t_{WCL2L}	NR2 = 0	4T	Min.	ns
	NR2 = 1	16T		

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)

2. The bus timing items listed above are dependent on t_{CYK}.

3. NI0, NI1 : Bits 0 and 2 of the noise protection control register (NPC)
NR0, NR1, NR2 : Bits 1, 3, and 4 of the noise protection control register (NPC)

AC Timing Test Points



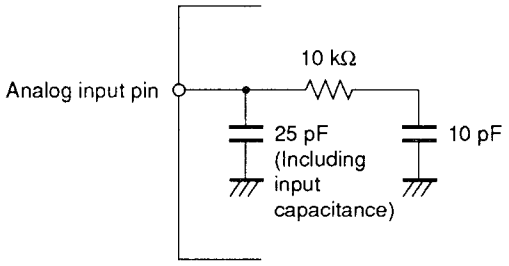
A/D CONVERTER CHARACTERISTICS (T_A = −10 to +70 °C, AV_{DD} = V_{DD} = +5 V ±10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			10			bit
Total error[Note 1]		4.5 V ≤ AV_{REF1} ≤ AV_{DD}			±0.4	%FSR
		3.4 V ≤ AV_{REF1} ≤ AV_{DD}			±0.7	%FSR
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	A/D trigger mode	2			μs
		Timer trigger mode, external trigger mode	2 + 5T			μs
Sampling time	t_{SAMP}	t_{CYK} = 62.5 ns	7.5			t_{CYK}
Zero-scale calibration[Note 1]		4.5 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±4.5	LSB
Full scale calibration[Note 1]		4.5 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±3.0	LSB
		3.4 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±4.5	LSB
Nonlinearity calibration[Note 1]		4.5 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±4.5	LSB
Analog input voltage[Note 2]	V_{IAN}		−0.3		AV_{REF1} + 0.3	V
Analog input impedance	R_{AN}	Nonsampling		10		MΩ
		Sampling		Note 3		
Reference voltage	AV_{REF1}		3.4		AV_{DD}	V
AV_{REF1} current	AI_{REF1}			3.0	8.0	mA
AV_{DD} supply current	AI_{DD}	Operation mode		3.3	13.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode: AV_{DDDR} = 2.5 V		2	10	μA
		STOP mode: AV_{DDDR} = 5 V ±10 %		10	50	μA

Notes 1. Quantization error is excluded.

2. When −0.3 V ≤ V_{IAN} ≤ 0 V, the conversion result is 000H.
When 0 V < V_{IAN} < AV_{REF1}, the voltage is converted with a 10-bit resolution.
When AV_{REF1} ≤ V_{IAN} ≤ AV_{REF1} + 0.3 V, the conversion result is 3FFH.

3. During sampling, the analog input impedance is equal to that of the following equivalent circuit.
(The figure below shows typical values. These values may not be correct for your application.)

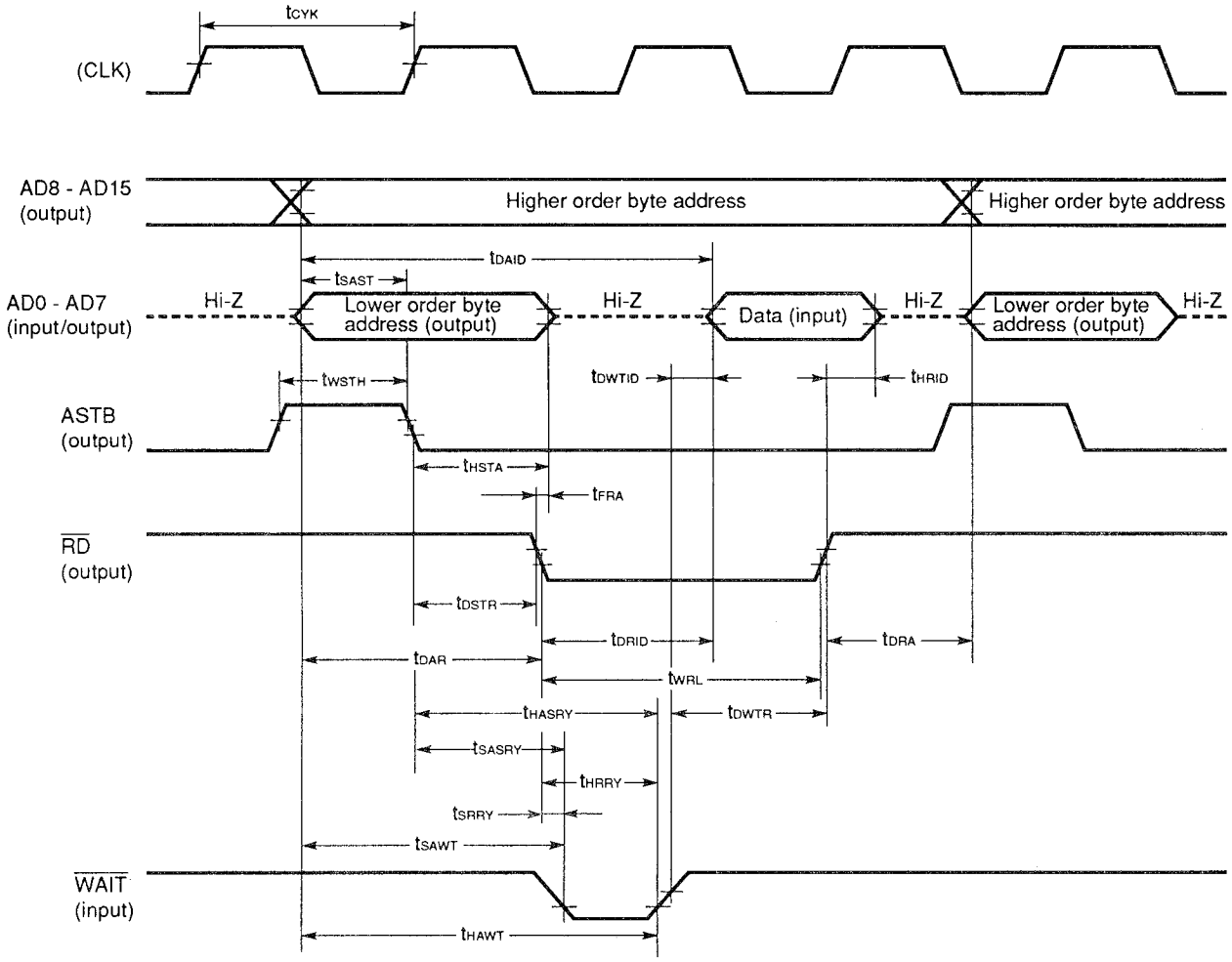


Remark T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)

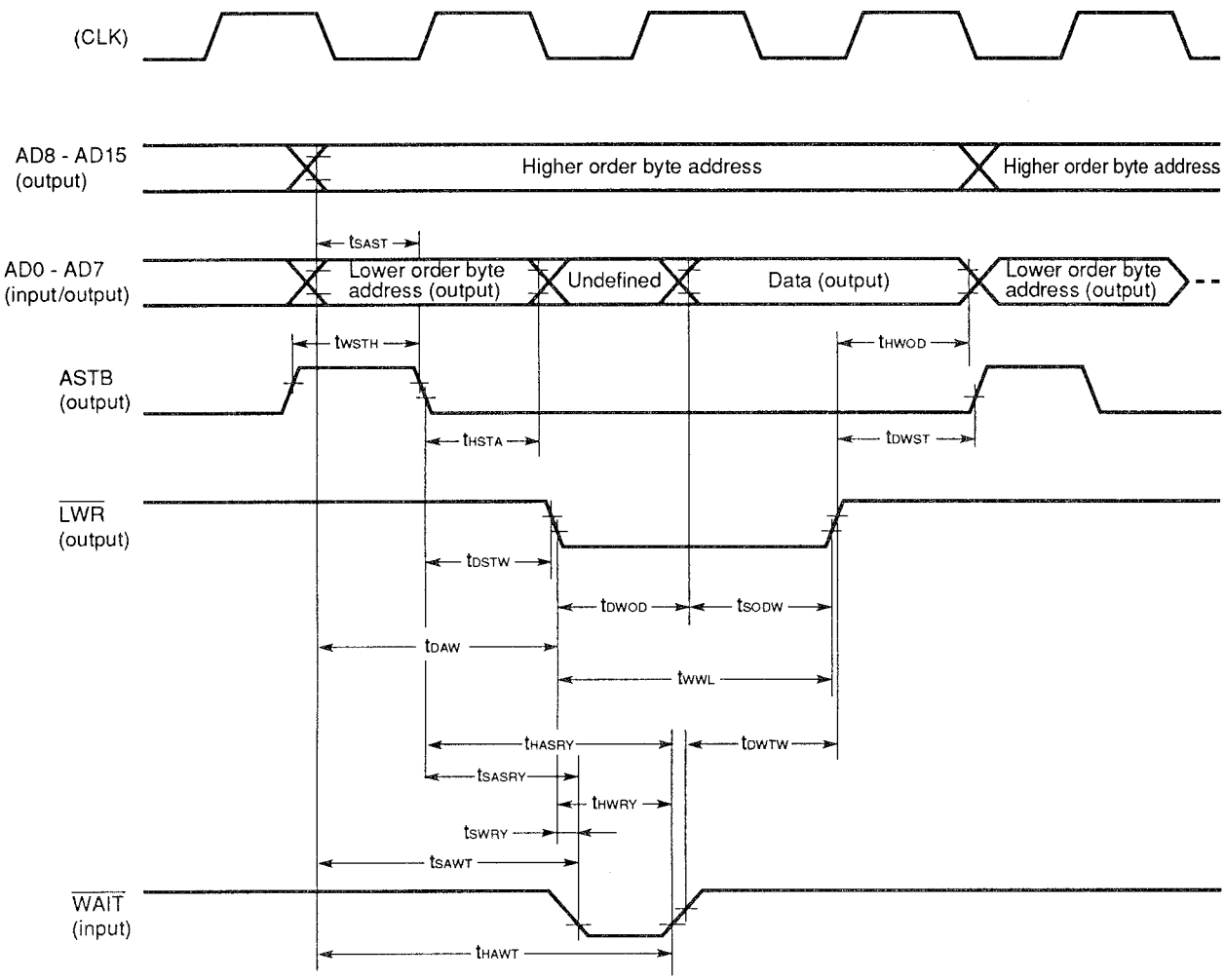
D/A CONVERTER CHARACTERISTICS (T_A = −10 to +70 °C, AV_{REF2} = V_{DD} = +5 V ±10 %, AV_{REF3} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution					8	bit
Total error		AV_{REF2} = V_{DD} = +5 V, AV_{REF3} = V_{SS} = 0 V			±0.4	%
Setting time		Load: 2 MΩ, 30 pF			2	μs
Output resistance	R_O	DACS0, DACS1 = 7FH		10		kΩ
Analog reference voltage	AV_{REF2}		0.75V_{DD}		V_{DD}	V
Analog reference voltage	AV_{REF3}		V_{SS}		0.2V_{DD}	V
Reference power supply input current	AI_{REF2}		0		5	mA
Reference power supply input current	AI_{REF3}		−5		0	mA

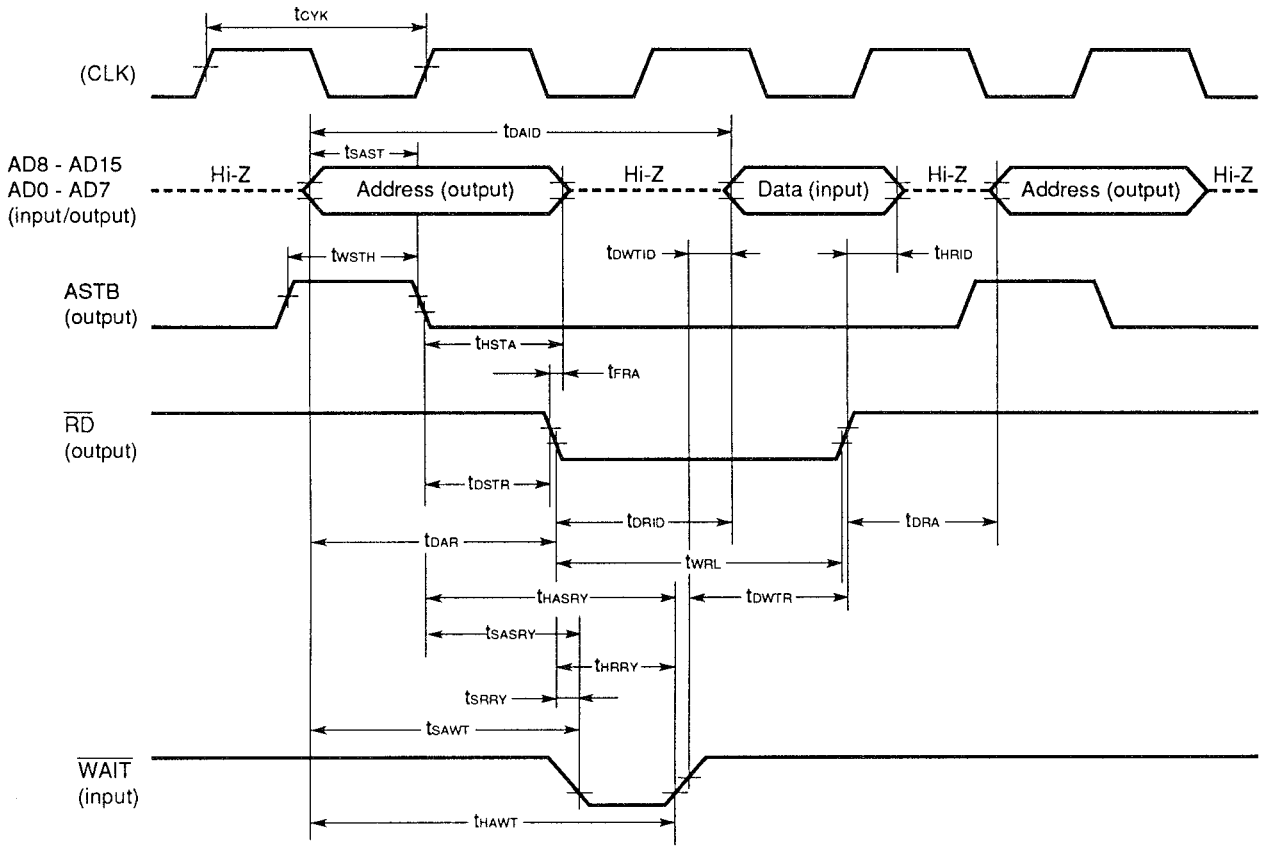
Read Operation (for 8-bit)



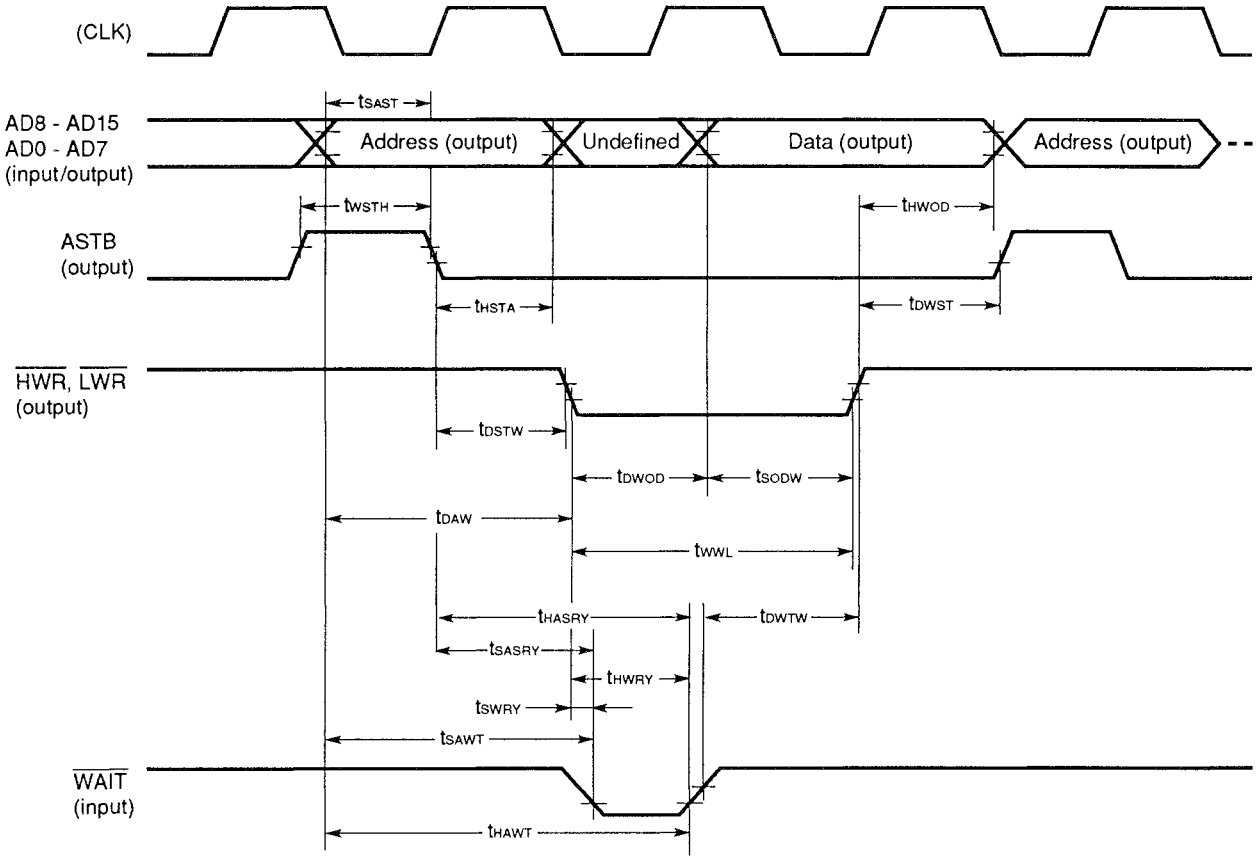
Write Operation (for 8-bit)



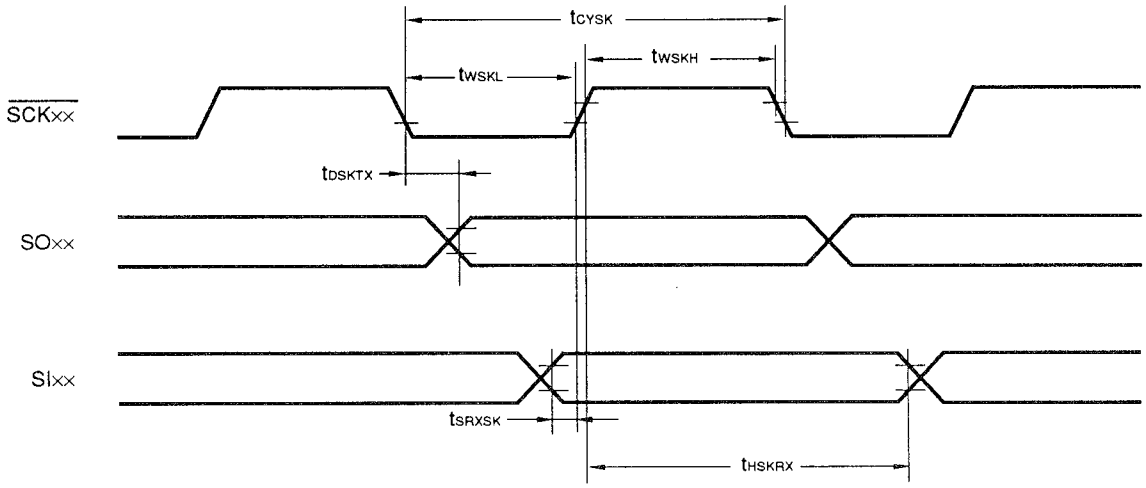
Read Operation (for 16-bit)



Write Operation (for 16-bit)

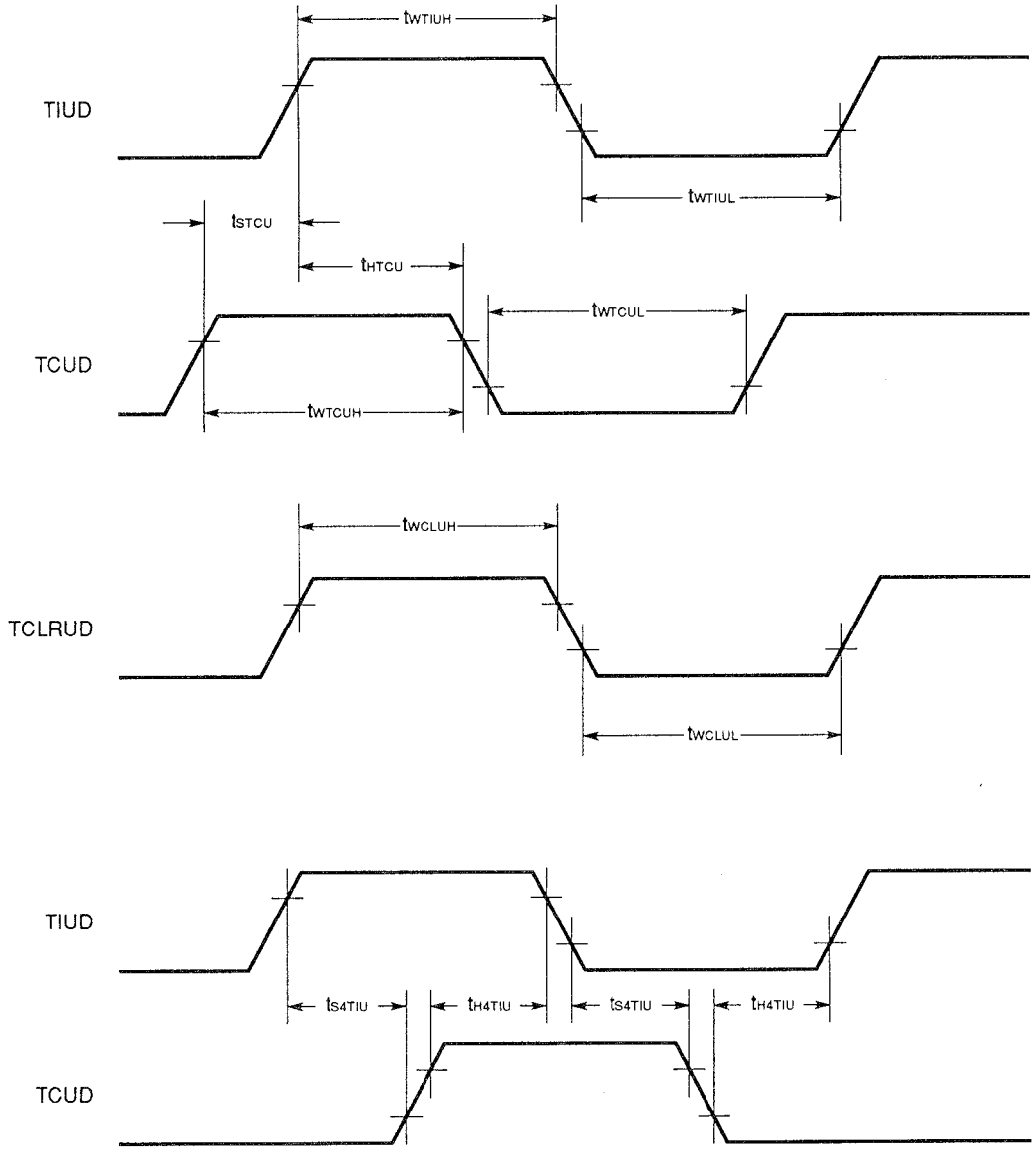


Serial Operation

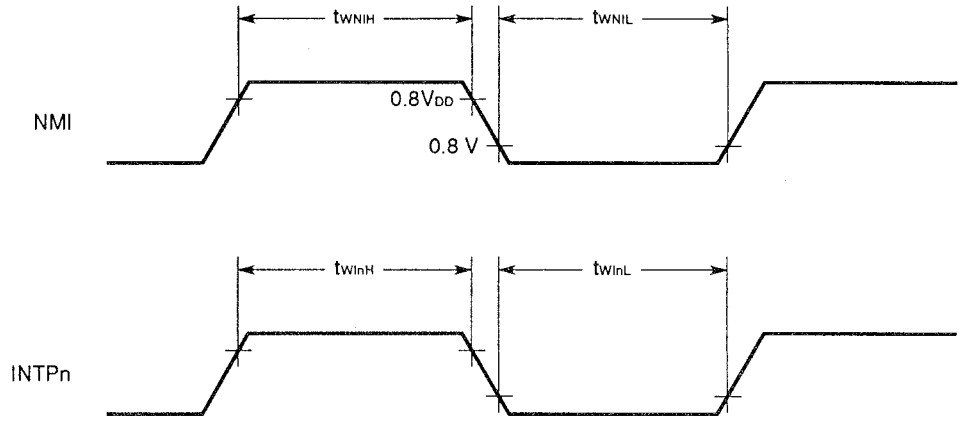


Remark xx: 00, 10, or 11

Up/Down Counter Input Timing

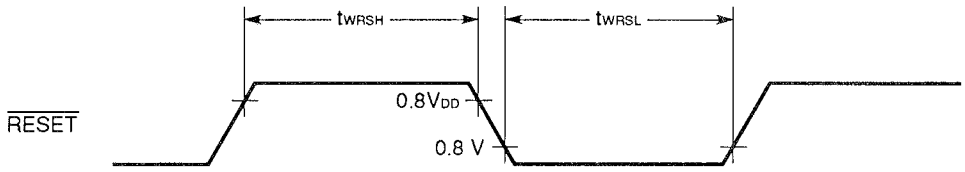


Interrupt Input Timing

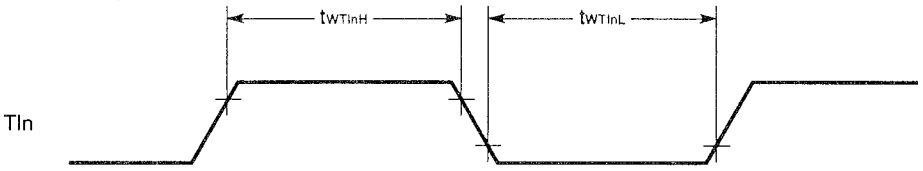


Remark n = 0 to 4

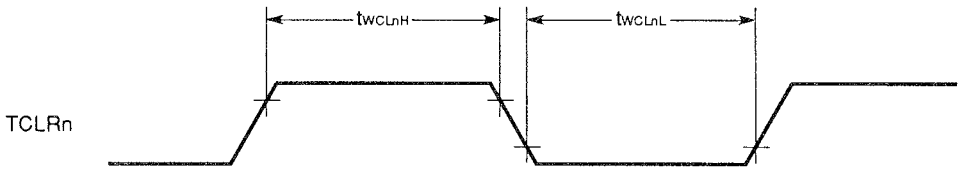
Reset Input Timing



Timer Pin Input Timing



Remark n = 0 or 1



Remark n = 0 to 2

DC PROGRAMMING CHARACTERISTICS (T_A = 25 ±5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note 1]	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.2		V_{DDP} + 0.3	V
Low-level input voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	0 ≤ V_I ≤ V_{DDP}[Note 2]			±10	μA
High-level output voltage	V_{OH}	V_{OH}	I_{OH} = –400 μA	2.4			V
Low-level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Input current	I_{A9}	–	A9 (P20/NMI) pin			±10	μA
Output leakage current	I_{LO}	–	0 ≤ V_O ≤ V_{DDP}, $\overline{OE}$ = V_{IH}			±10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory write mode	6.25	6.5	6.75	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} supply current	I_{DD}	I_{DD}	Program memory write mode			30	mA
			Program memory read mode			100	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode			50	mA
			Program memory read mode		1.0	100	μA

Notes 1. Symbols for the corresponding μPD27C1001A

2. The V_{DDP} represents the V_{DD} pin as viewed in the programming mode.

AC PROGRAMMING CHARACTERISTICS (T_A = 25 ±5 °C, V_{SS} = 0 V)

PROM Write Mode (Page Program Mode)

Parameter	Symbol[Note 1]	Conditions	Min.	Typ.	Max.	Unit
Address set up time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
	t_{AHL}		2			μs
	t_{AHV}		0			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		250	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS}[Note 2]		2			μs
Initial program pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}				1.0	μs
$\overline{OE}$ pulse width in the data latch	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}		2			μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the μPD27C1001A.

2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Write Mode (Byte Program Mode)

Parameter	Symbol[Note 1]	Conditions	Min.	Typ.	Max.	Unit
Address set up time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		250	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS}[Note 2]		2			μs
Initial program pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}				1.0	μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the μPD27C1001A.

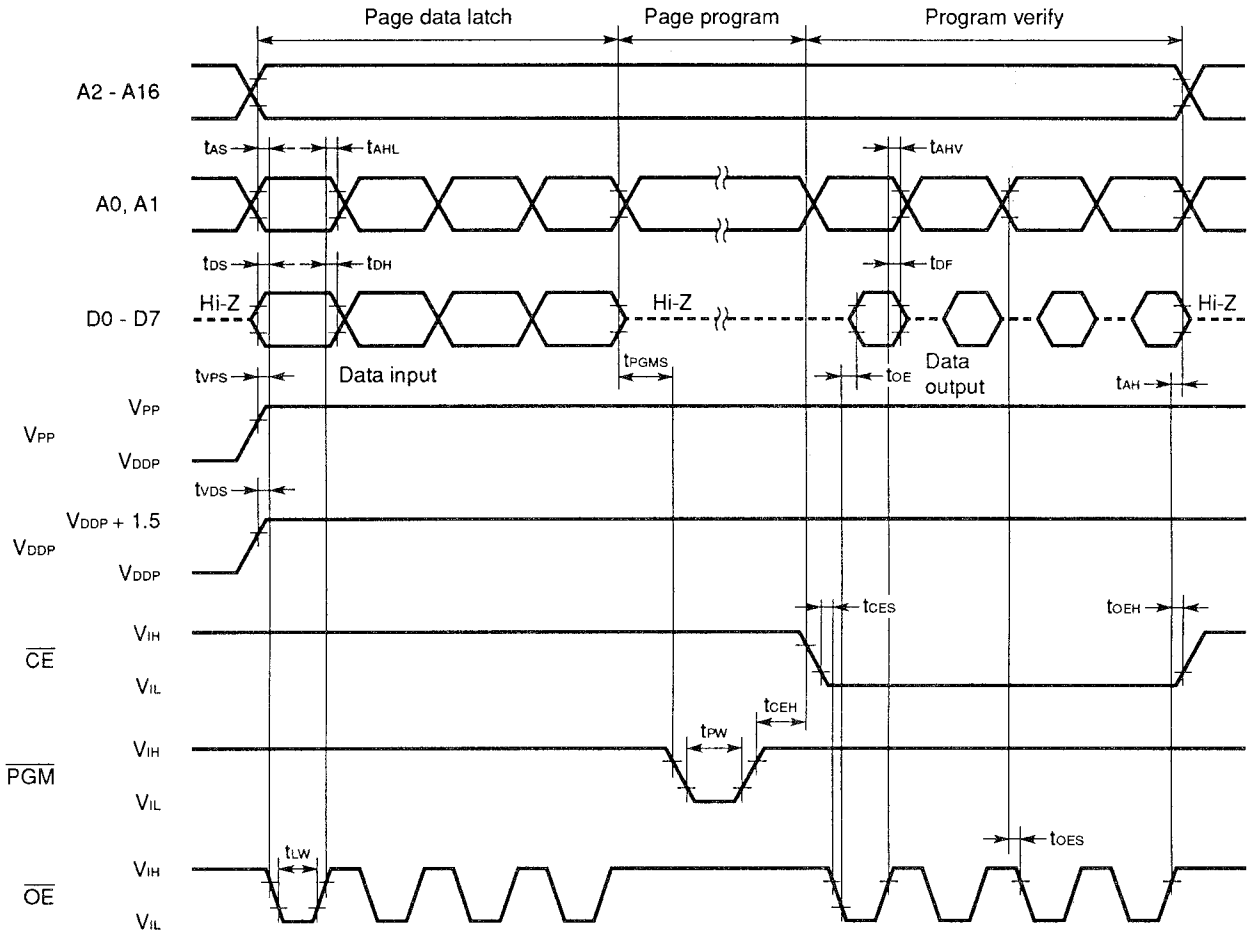
2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Read Mode

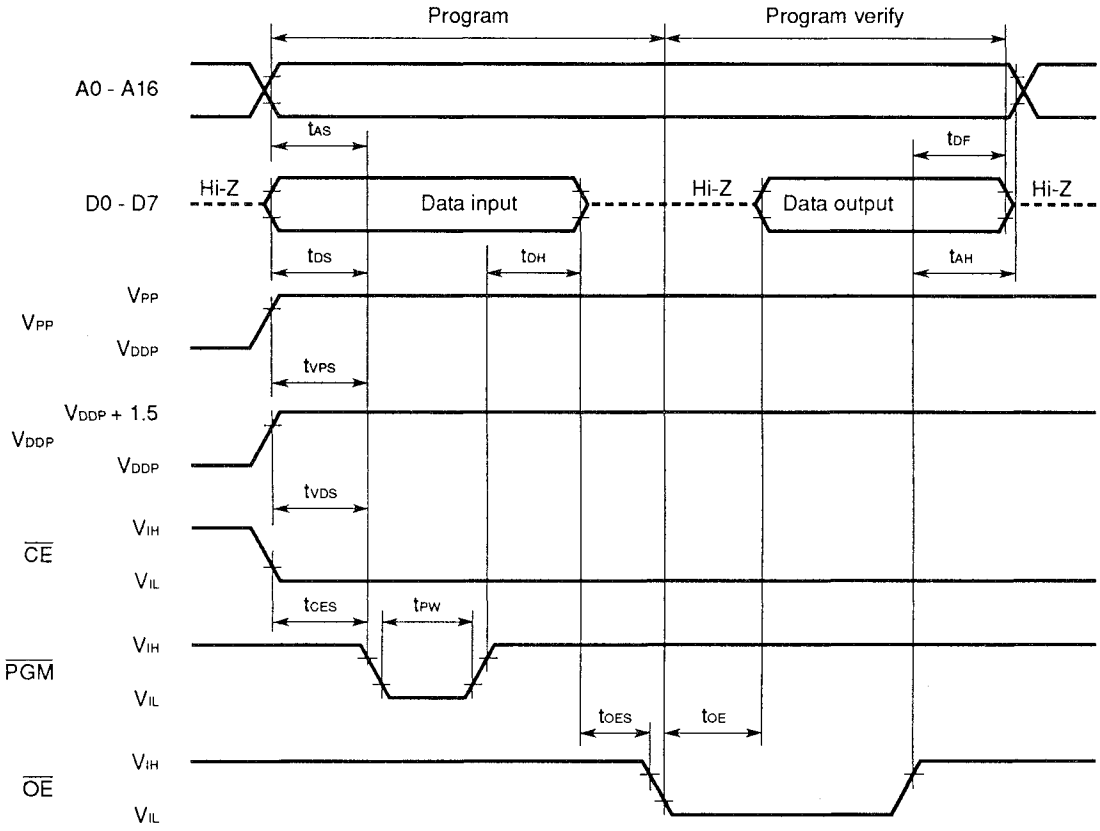
Parameter	Symbol[Note]	Conditions	Min.	Typ.	Max.	Unit
Data output time from address	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			1.0	μs
$\overline{CE} \downarrow \rightarrow$ data output time	t_{CE}	$\overline{OE} = V_{IL}$			1.0	μs
$\overline{OE} \downarrow \rightarrow$ data output time	t_{OE}	$\overline{CE} = V_{IL}$			1.0	μs
Data hold time to $\overline{OE} \uparrow$	t_{DF}	$\overline{CE} = V_{IL}$	0		250	ns
Data hold time to address	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note These symbols correspond to those of the μPD27C1001A.

PROM Write Mode Timing (Page Program Mode)



PROM Write Mode Timing (Byte Program Mode)

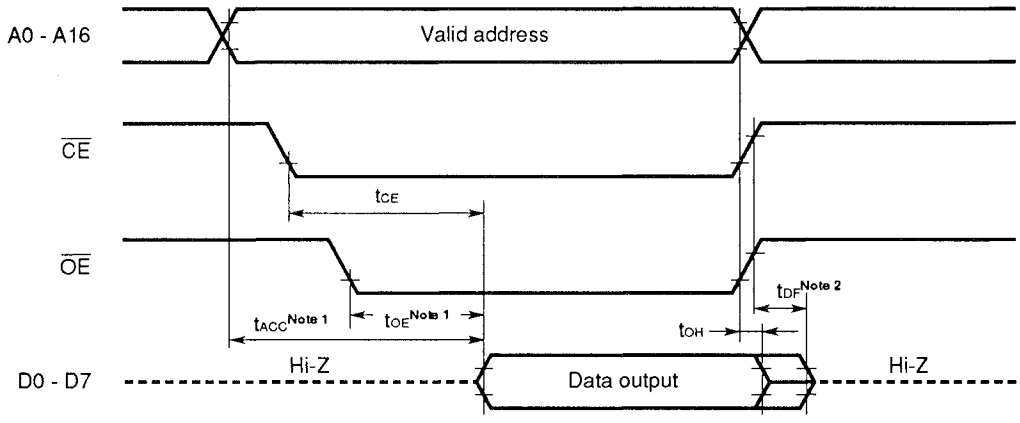


Cautions 1. V_{DDP} must be applied before V_{PP}, and must be cut after V_{PP}.

2. V_{PP} including overshoot must not exceed +13.5 V.

3. Plugging in or out the board with the V_{PP} pin supplied with 12.5 V may adversely affect its reliability.

PROM Read Mode Timing

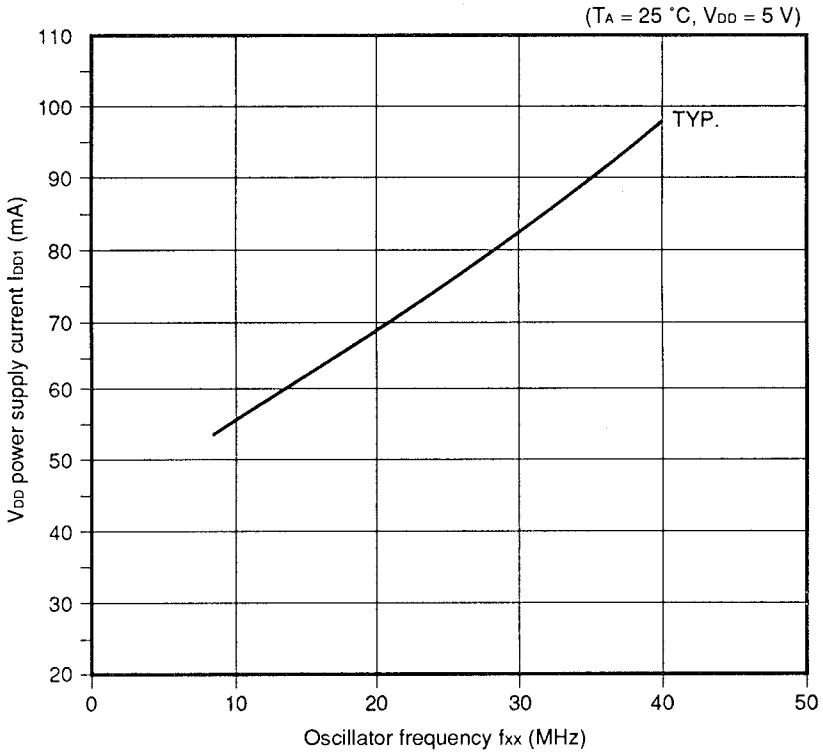


Notes 1. For reading within t_{ACC}, the delay of the $\overline{OE}$ input from falling edge of $\overline{CE}$ must be within $t_{ACC} - t_{OE}$.

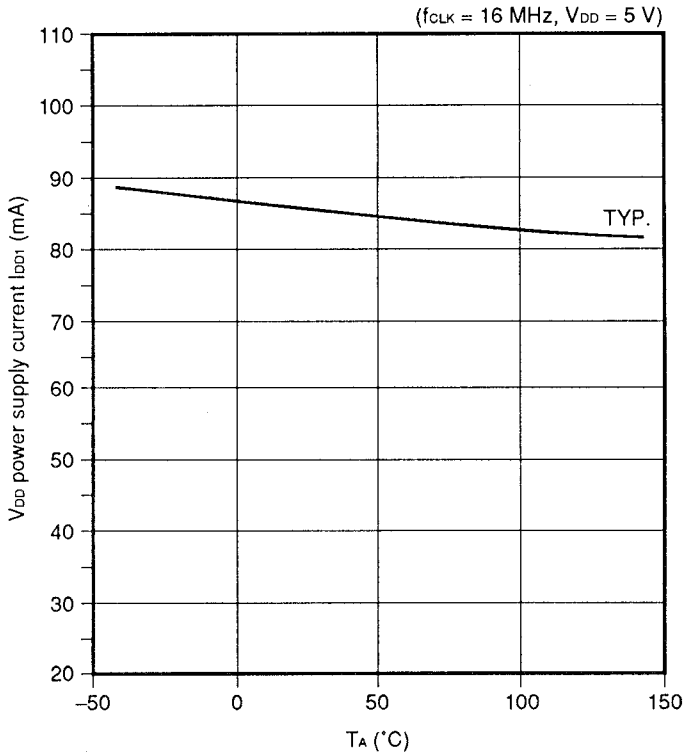
2. t_{DF} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

8. CHARACTERISTIC CURVES (FOR REFERENCE) ★

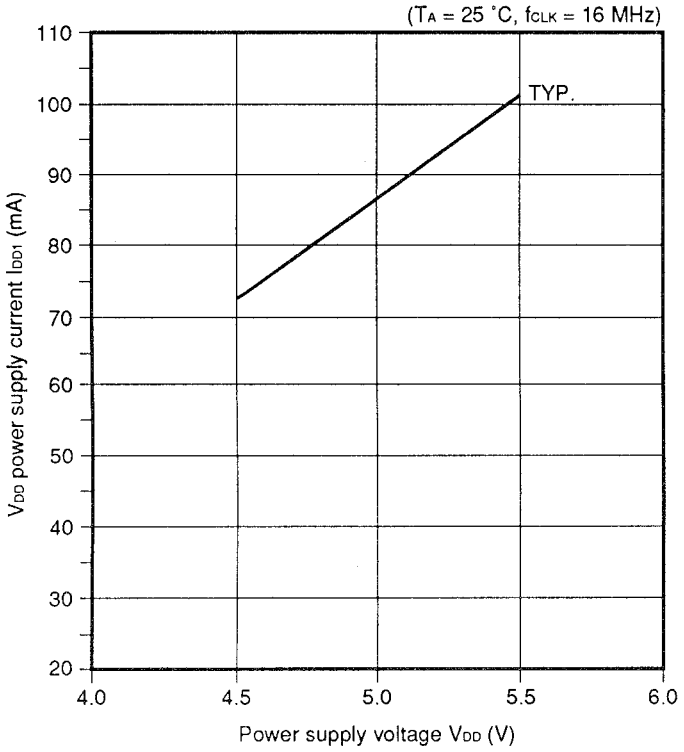
I_{DD1} vs f_{XX}



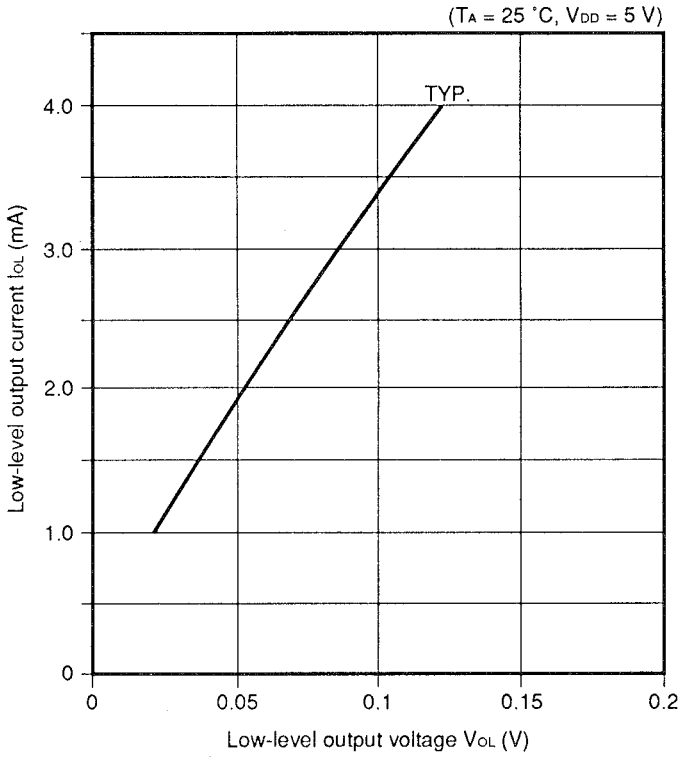
I_{DD1} vs T_A



I_{DD1} vs V_{DD}

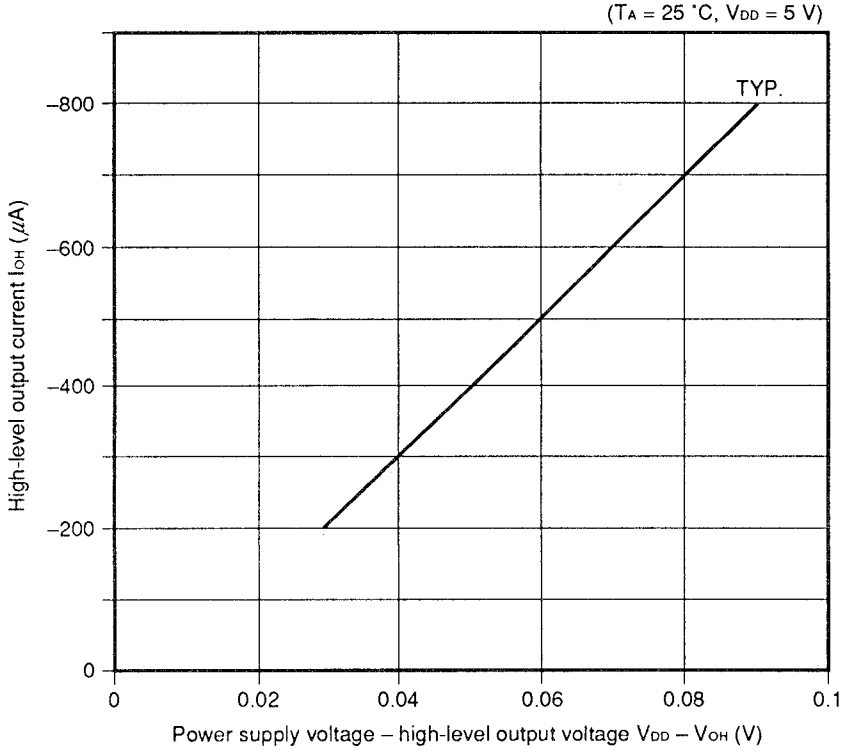


I_{OL} vs V_{OL}



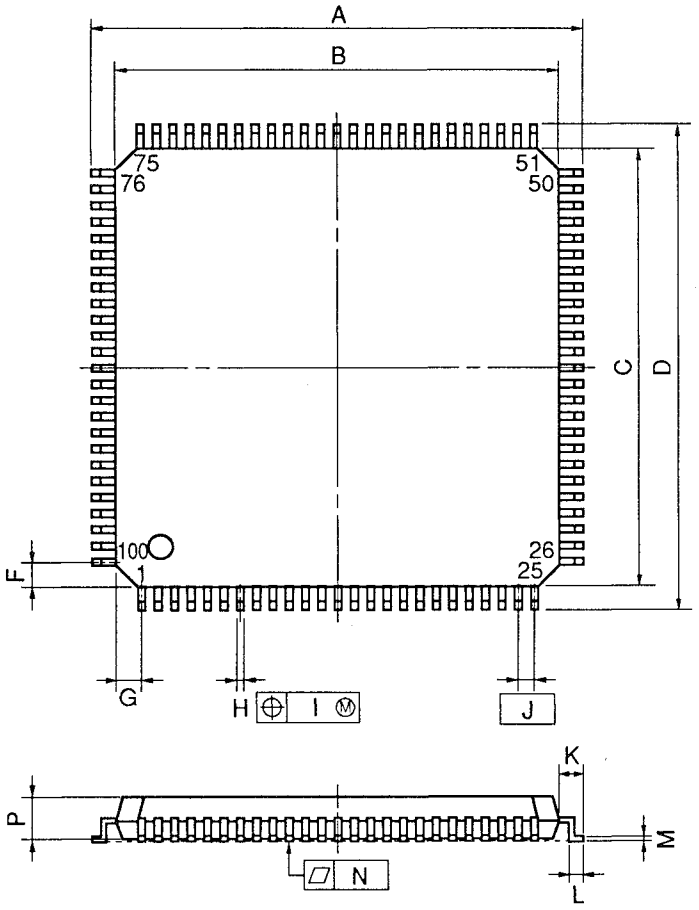
I_{OH} vs (V_{DD} – V_{OH})

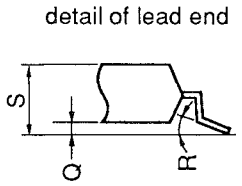
(T_A = 25 °C, V_{DD} = 5 V)



9. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)





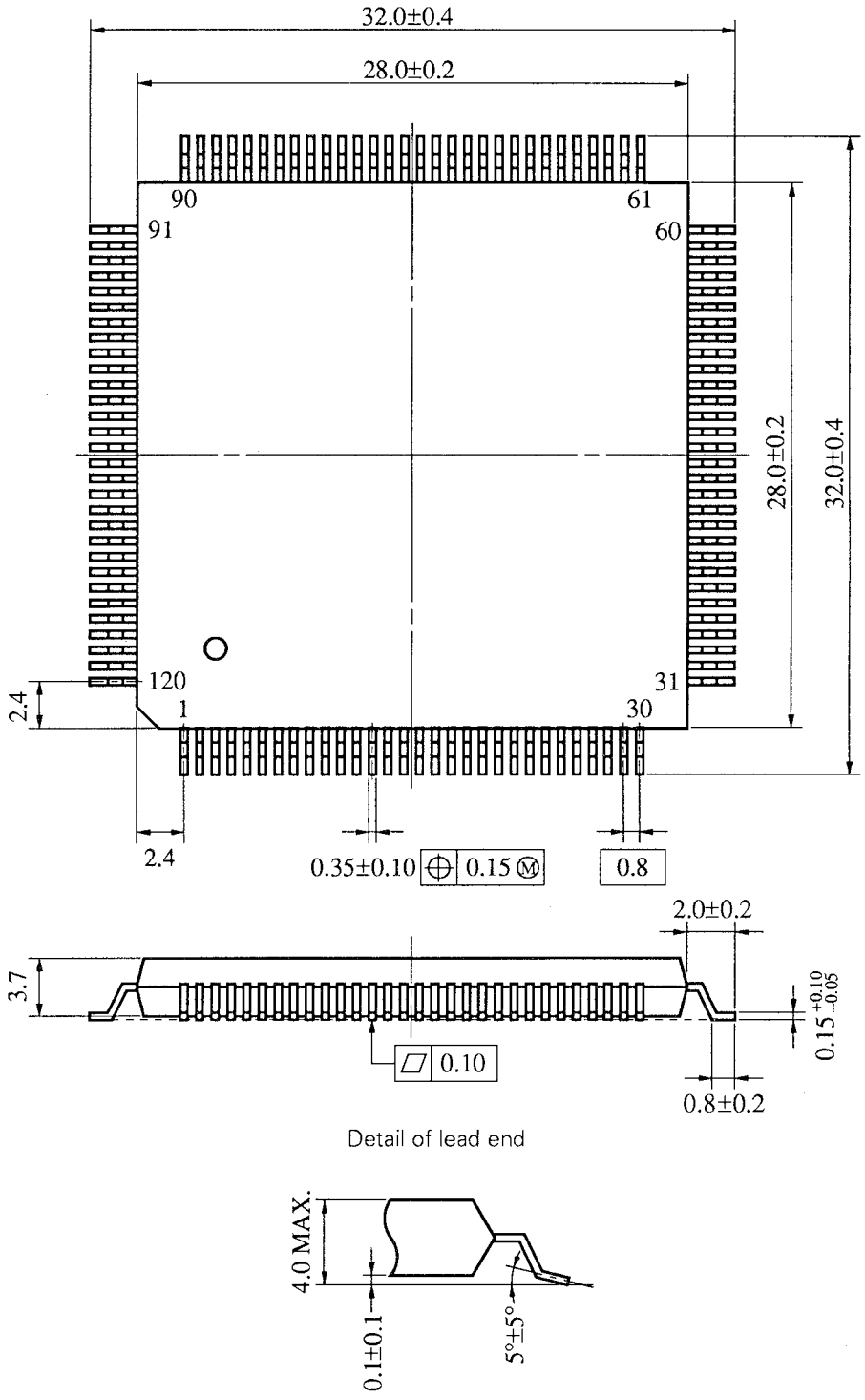
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

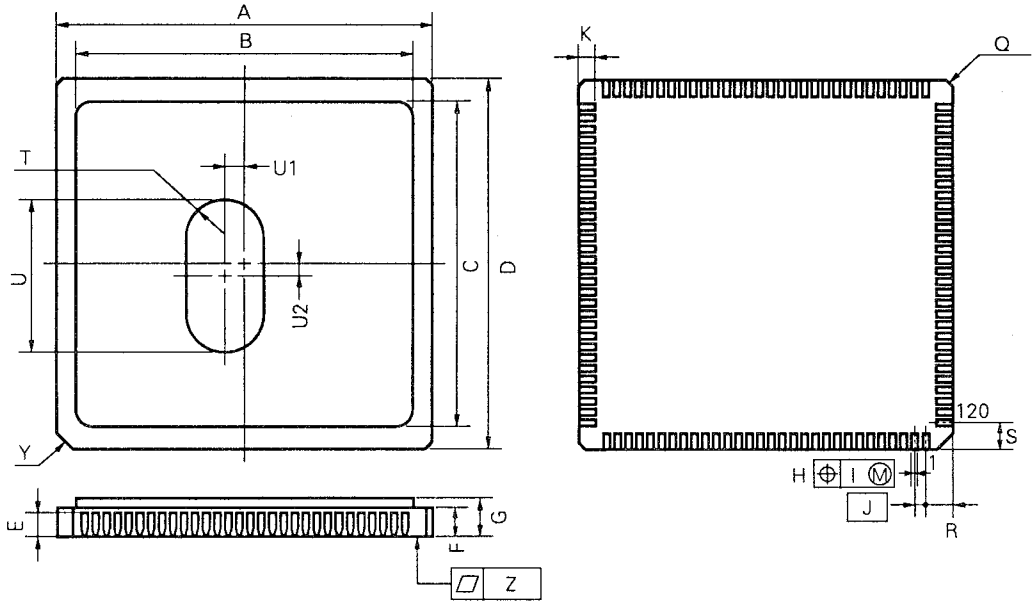
P100GC-50-7EA-2

120-pin plastic QFP (28 x 28) (units: mm)



P120GD-80-5BB-3

120 PIN CERAMIC WQFN



X120KW-80A-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	27.3±0.27	1.075±0.011
B	24.5	0.965
C	24.5	0.965
D	27.3±0.27	1.075±0.011
E	1.94	0.076
F	2.14	0.084
G	3.57 MAX.	0.141 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8	0.031
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C0.3	C0.012
R	2.05	0.081
S	2.05	0.081
T	R3.0	R0.118
U	12.0	0.472
U1	1.5	0.059
U2	1.0	0.039
Y	C1.0	C0.039
Z	0.10	0.004

10. RECOMMENDED SOLDERING CONDITIONS ★

The conditions listed below shall be met when soldering the μPD78P356.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 10-1 Soldering Conditions for Surface-Mount Devices (1)

μPD78P356GC-7EA: 100-pin plastic QFP (14 × 14 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit[Note]: 7 days (10 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-107-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit[Note]: 7 days (10 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-107-2
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow process: 1 Preheating temperature: 120 °C max. (measured on the package surface) Exposure limit[Note]: 7 days (10 hours of pre-baking is required at 125 °C afterward.)	WS60-107-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

Table 10-2 Soldering Conditions for Surface-Mount Devices (2)

μPD78P356GD-5BB: 120-pin plastic QFP (28 × 28 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit[Note]: 7 days (36 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-367-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit[Note]: 7 days (36 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-367-2
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow process: 1 Preheating temperature: 120 °C max. (measured on the package surface) Exposure limit[Note]: 7 days (36 hours of pre-baking is required at 125 °C afterward.)	WS60-367-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

APPENDIX A TOOLS ★

A.1 DEVELOPMENT TOOLS

The following tools are provided for developing a system that uses the μPD78P356:

Language processor

<table>
<tr><td rowspan="9">78K/III series relocatable assembler (RA78K/III)</td><td colspan="4">This relocatable program can be used for all 78K/III series emulators. With its macro functions, it allows the user to improve program development efficiency. A structured-programming assembler is also provided, which enables explicit description of program control structures. This assembler could improve productivity in program production and maintenance.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td colspan="2">MS-DOS™</td><td>3.5-inch 2HD</td><td>μS5A13RA78K3</td></tr>
<tr><td></td><td colspan="2"></td><td>5.25-inch 2HD</td><td>μS5A10RA78K3</td></tr>
<tr><td>IBM PC/AT™ or compatibles</td><td colspan="2">PC DOS™</td><td>3.5-inch 2HC</td><td>μS7B13RA78K3</td></tr>
<tr><td></td><td colspan="2"></td><td>5.25-inch 2HC</td><td>μS7B10RA78K3</td></tr>
<tr><td>HP9000 series 700™</td><td colspan="2">HP-UX™</td><td>DAT</td><td>μS3P16RA78K3</td></tr>
<tr><td>SPARCstation™</td><td colspan="2">SunOS™</td><td rowspan="2">Cartridge tape (QIC-24)</td><td>μS3K15RA78K3</td></tr>
<tr><td>NEWS™</td><td colspan="2">NEWS-OS™</td><td>μS3R15RA78K3</td></tr>
<tr><td rowspan="9">78K/III series C compiler (CC78K/III)</td><td colspan="4">This C compiler can be used for all 78K/III series emulators. The compiler converts programs written in C language into object codes executable on the microcomputer. When the compiler is used, the 78K/III series relocatable assembler package (RA78K/III) is needed.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td colspan="2">MS-DOS</td><td>3.5-inch 2HD</td><td>μS5A13CC78K3</td></tr>
<tr><td></td><td colspan="2"></td><td>5.25-inch 2HD</td><td>μS5A10CC78K3</td></tr>
<tr><td>IBM PC/AT or compatibles</td><td colspan="2">PC DOS</td><td>3.5-inch 2HC</td><td>μS7B13CC78K3</td></tr>
<tr><td></td><td colspan="2"></td><td>5.25-inch 2HC</td><td>μS7B10CC78K3</td></tr>
<tr><td>HP9000 series 700</td><td colspan="2">HP-UX</td><td>DAT</td><td>μS3P16CC78K3</td></tr>
<tr><td>SPARCstation</td><td colspan="2">SunOS</td><td rowspan="2">Cartridge tape (QIC-24)</td><td>μS3K15CC78K3</td></tr>
<tr><td>NEWS</td><td colspan="2">NEWS-OS</td><td>μS3R15CC78K3</td></tr>
</table>

Remark It is guaranteed that the relocatable assembler and C compiler run only under the OSs on the corresponding host machines described above.

Connections between development tools and target devices

Development tool / Target device	In-circuit emulator	Emulation probe and EPROM product	Conversion adapter	Conversion socket or conversion adapter
GC package (100-pin QFP)	IE-78350-R and IE-78355-R-EM1	EP-78355GC-R	—	EV-9500GC-100
		EP-78355GD-R	EV-9501GC-100	
	—	μPD78P356KP (120-pin WQFN)		
GD package (120-pin QFP)	IE-78350-R and IE-78355-R-EM1	EP-78355GD-R	—	EV-9200GD-120
	—	μPD78P356KP (120-pin WQFN)		

PROM programming tools

Hardware	PG-1500	The PG-1500 PROM programmer is used together with an accessory board and optional program adapter. It allows the user to program a single chip microcomputer containing PROM independently or from a host machine. The PG-1500 can be used to program typical 256K-bit to 4M-bit PROMs.			
	PA-78P356GC PA-78P356GD PA-78P356KP	Programmer adapter for writing programs to the μPD78P356A. Used with a PROM programmer such as the PG-1500. PA-78P356GC : For μPD78P356GC PA-78P356GD : For μPD78P356GD PA-78P356KP : For μPD78P356KP			
Software	PG-1500 controller	This program enables the host machine to control the PG-1500 through the serial and parallel interfaces.			
		Host machine	OS	Distribution media	Part number
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13PG1500
				5.25-inch 2HD	μS5A10PG1500
		IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13PG1500
				5.25-inch 2HC	μS7B10PG1500

Remark It is guaranteed that the PG-1500 controller runs only under the OSs on the corresponding host machines described above.

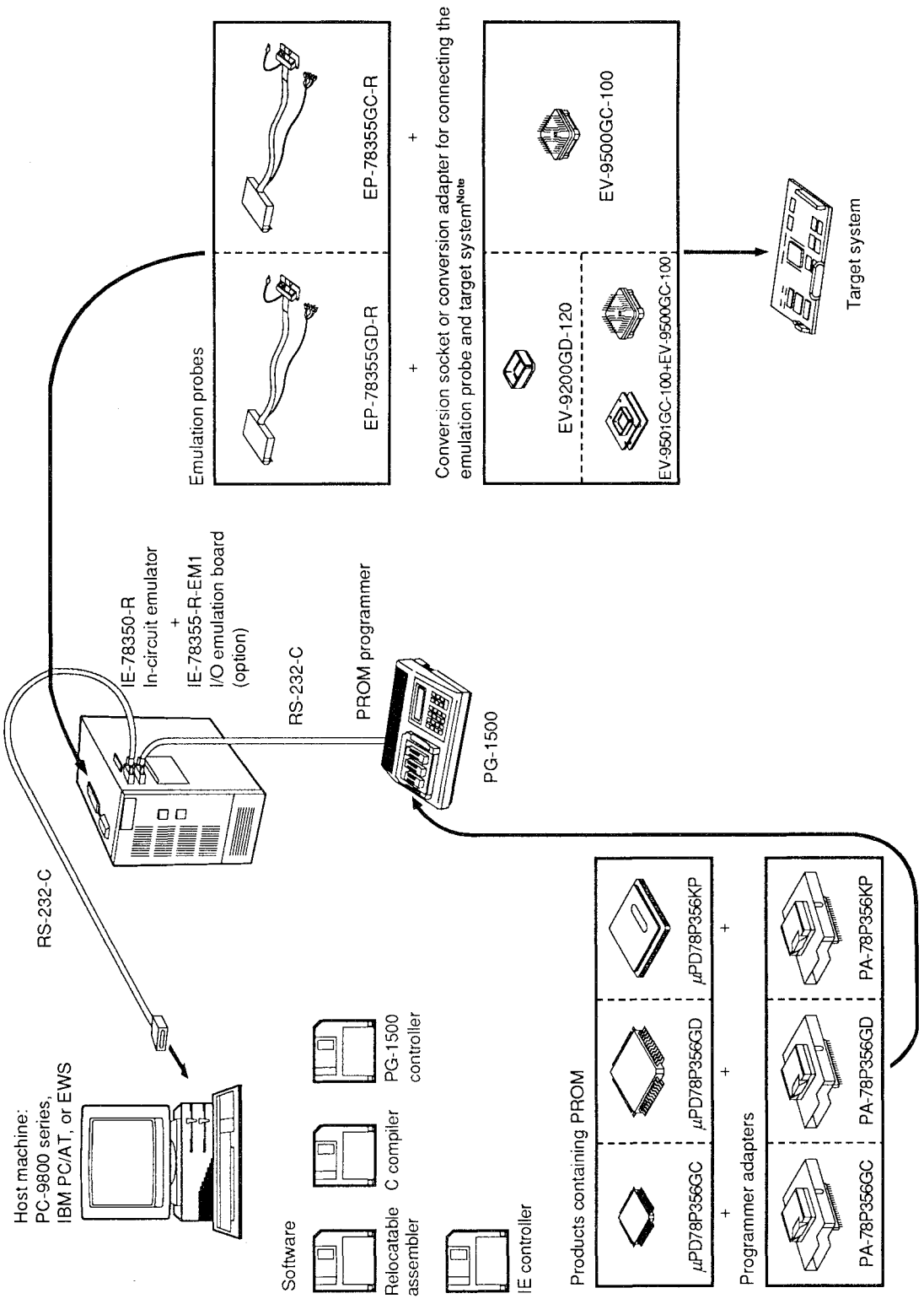
Debugging tools (when the IE controller is used)

Hardware	IE-78350-R	In-circuit emulator for developing and debugging an application system. For debugging, connect the emulator to the host machine.
	IE-78355-R-EM1	I/O emulation board for emulating peripheral hardware such as the I/O ports of the target device.
	EP-78355GC-R EV-9500GC-100	Emulation probe for connecting the IE-78350-R to the target system, used for the 100-pin QFP of the μPD78P356. The EV-9500GC-100 conversion adapter is supplied with the emulation probe, to connect the target system.
	EP-78355GD-R EV-9200GD-120 EV-9501GC-100 + EV-9500GC-100	Emulation probe for connecting the IE-78350-R to the target system, used for the 120-pin QFP of the μPD78P356. The EV-9200GD-120 conversion socket is supplied with the emulation probe, to connect the target system. By connecting this emulation probe to the optional 100-pin QFP conversion adapter, EV-9501GC-100, the 100-pin QFP of the μPD78356 can be developed. To connect the target system, however, also use the optional EV-9500GC-100 conversion adapter.
Software	IE-78350-R control program (IE controller)	This control program allows the user to control the IE-78350-R from the host machine. Its automatic command execution function ensures more efficient debugging.

Host machine			Part number
	OS	Distribution media	
PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78355
		5.25-inch 2HD	μS5A10IE78355
IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13IE78355
		5.25-inch 2HC	μS7B10IE78355

Remark It is guaranteed that the IE controller runs only under the OSs on the corresponding host machines described above.

Development tool configuration (when the IE controller is used)



Note The conversion socket or conversion adapter is supplied with the emulation probe.

Remarks 1. The PG-1500 can be directly connected to the host machine via the RS-232-C interface.

2. In this figure, a 3.5-inch floppy disk is shown as an example distribution medium for the software.

Phase-out/Discontinued

Debugging tools (when the integrated debugger is used) (1/2)

Hardware	IE-784000-R	In-circuit emulator for developing and debugging an application system. For debugging, connect the emulator to the host machine.
	IE-78350-R-EM-A[Note]	Emulation board for emulating peripheral hardware such as the I/O ports of the target device.
	IE-78355-R-EM1	I/O emulation board for emulating peripheral hardware such as the I/O ports of the target device.
	EP-78355GC-R EV-9500GC-100	Emulation probe for connecting the IE-784000-R to the target system, used for the 100-pin QFP of the μPD78P356. One EV-9500GC-100 conversion adapter is provided for connection to the target system.
	EP-78355GD-R EV-9200GD-120 EV-9501GC-100 + EV-9500GC-100	Emulation probe for connecting the IE-784000-R to the target system, used for the 120-pin QFP of the μPD78P356. The EV-9200GD-120 conversion socket is supplied with the emulation probe, to connect the target system. By connecting this emulation probe to the optional 100-pin QFP conversion adapter, EV-9501GC-100, the 100-pin QFP of the μPD78356 can be developed. To connect the target system, however, also use the optional EV-9500GC-100 conversion adapter.
	IE-70000-98-IF-B	Interface adapter and cable when the PC-9800 series computer (other than a notebook) is used as the host machine.
	IE-70000-98N-IF	Interface adapter and cable when a PC-9800 series notebook is used as the host machine.
	IE-70000-PC-IF-B	Interface adapter and cable when the IBM PC/AT is used as the host machine.
	IE-78000-R-SV3[Note]	Interface board when the EWS is used as the host machine.

Note Under development

Debugging tools (when the integrated debugger is used) (2/2)

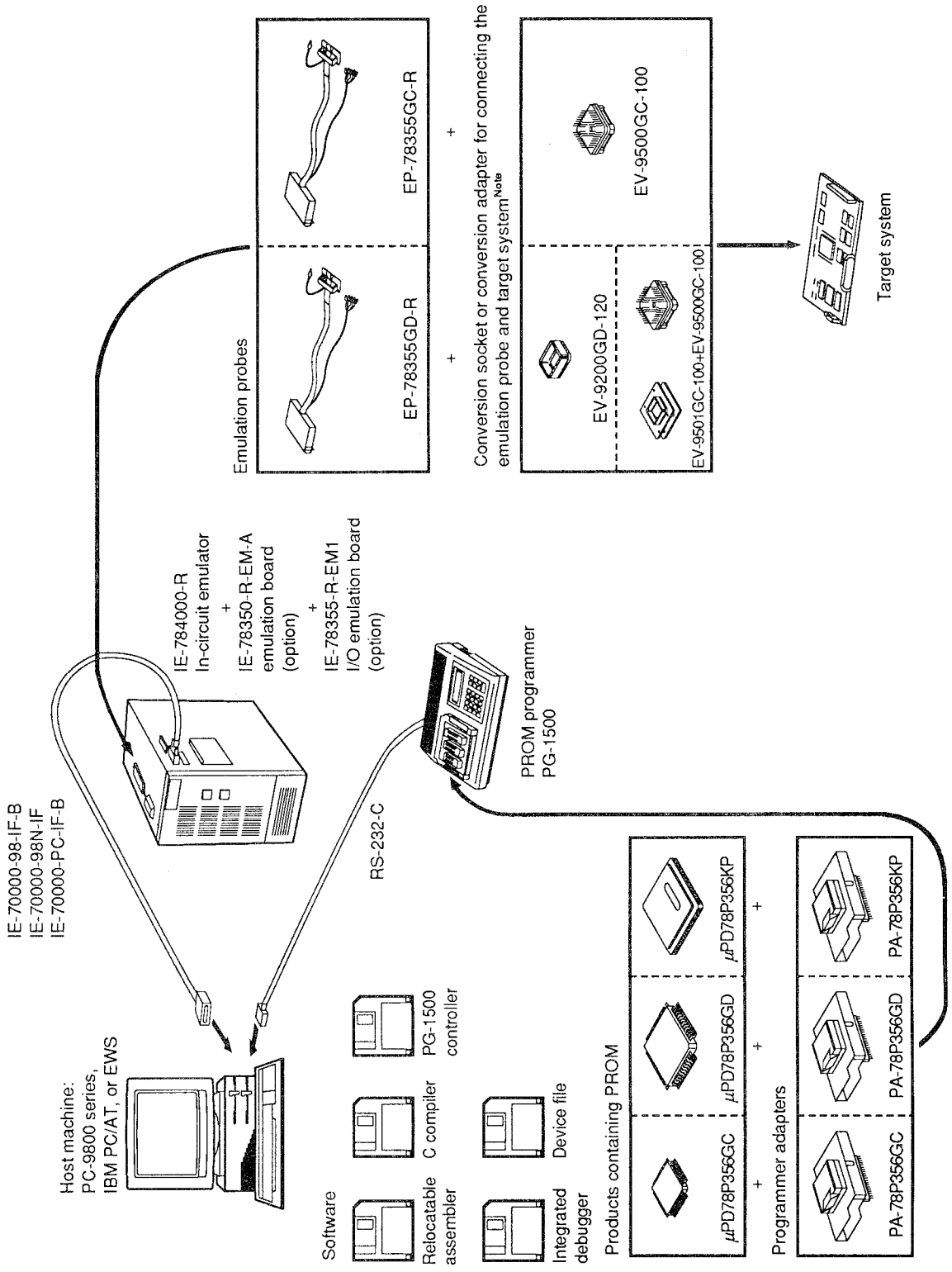
<table>
<tr><td rowspan="11">Software</td><td rowspan="6">Integrated debugger (ID78K/III)Note</td><td colspan="4">Program for controlling the in-circuit emulator for the 78K/III series. The integrated debugger (ID78K/III) is used together with the device file (DF78355).
Debugging can be performed for the source program written in C, structured assembly language, or assembly language. The ID78K/III can display various information simultaneously on the host machine screen divided into multiple areas. This ensures efficient debugging.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td rowspan="2">MS-DOS + Windows™</td><td>3.5-inch 2HD</td><td>μSAA13ID78K3</td></tr>
<tr><td></td><td>5.25-inch 2HD</td><td>μSAA10ID78K3</td></tr>
<tr><td>IBM PC/AT or compatibles (Japanese Windows)</td><td rowspan="3">PC DOS + Windows</td><td>3.5-inch 2HC</td><td>μSAB13ID78K3</td></tr>
<tr><td></td><td>5.25-inch 2HC</td><td>μSAB10ID78K3</td></tr>
<tr><td rowspan="2">IBM PC/AT or compatibles (Windows)</td><td>3.5-inch 2HC</td><td>μSBB13ID78K3</td></tr>
<tr><td></td><td>5.25-inch 2HC</td><td>μSBB10ID78K3</td></tr>
<tr><td rowspan="5">Device file (DF78355)Note</td><td colspan="4">File which contains the device-specific information. The device file (DF78355) is used together with the assembler (RA78K/III), C compiler (CC78K/III), or integrated debugger (ID78K/III).</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td>MS-DOS</td><td>3.5-inch 2HD</td><td>μS5A13DF78355</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HD</td><td>μS5A10DF78355</td></tr>
<tr><td>IBM PC/AT or compatibles</td><td>PC DOS</td><td>3.5-inch 2HC</td><td>μS7B13DF78355</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HC</td><td>μS7B10DF78355</td></tr>
</table>

Note Under development

Remark It is guaranteed that the integrated debugger and device file run only under the OSs on the corresponding host machines described above.

Phase-out/Discontinued

Development tool configuration (when the integrated debugger is used)



Note The conversion socket or conversion adapter is supplied with the emulation probe.

Remarks 1. In this figure, a 3.5-inch floppy disk is shown as an example distribution medium of software.

2. In this figure, a desk-top personal computer is shown as an example host machine.

A.2 EMBEDDED SOFTWARE

To improve the efficiency of program development and simplify the maintenance of systems incorporating this microcomputer, the following embedded software is provided.

Real-time OS

<table>
<tr><td rowspan="5">Real-time OS
(RX78K/III)Note</td><td colspan="3">This operating system was designed to provide a multitasking environment for control applications that require real-time processing. System performance is improved by using the idling CPU for other processing.
RX78K/III provides system calls that conform to μITRON specifications.
The RX78K/III package provides the RX78K/III nucleus and a tool (Configurator) that is used for creating multiple information tables.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td>MS-DOS</td><td>3.5-inch 2HD</td><td>Undecided</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HD</td><td>Undecided</td></tr>
<tr><td></td><td>IBM PC/AT or compatibles</td><td>PC DOS</td><td>3.5-inch 2HC</td><td>Undecided</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HC</td><td>Undecided</td></tr>
</table>

Note Under development

Caution Before purchasing this software, complete the purchase application sheet and sign the software license agreement.

Remark To use the RX78K/III real-time operating system, the optional RA78K/III assembler package is required.

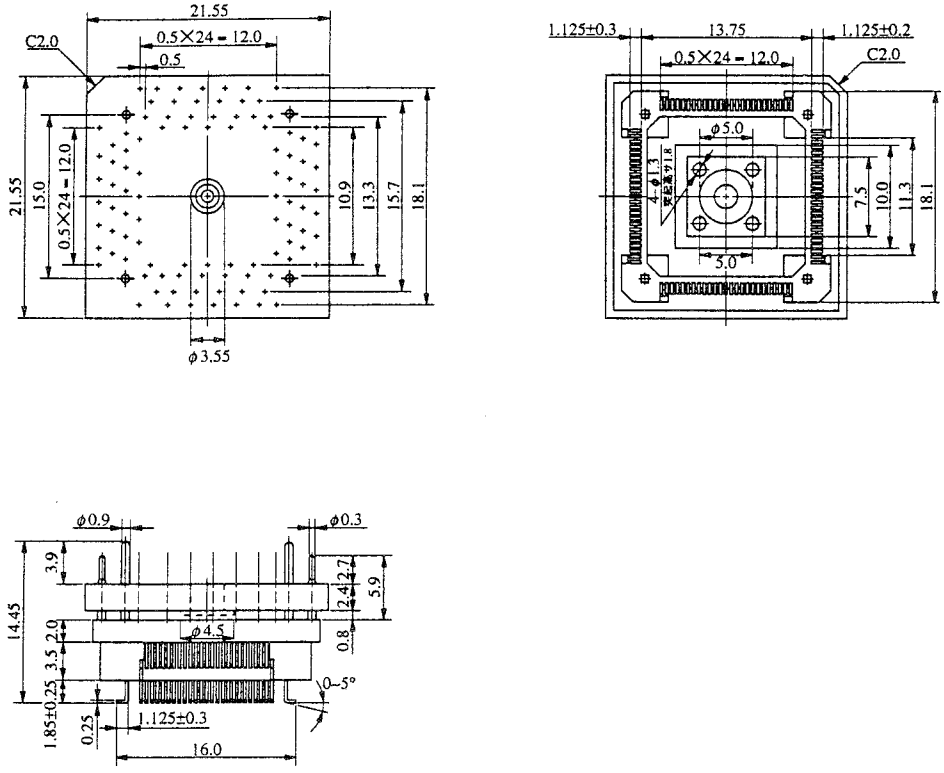
Fuzzy inference development support system

Tool for creating fuzzy knowledge data (FE9000, FE9200)	This program supports the input/editing and simulation of fuzzy knowledge data (fuzzy rules and membership functions).			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FE9000
			5.25-inch 2HD	μS5A10FE9000
	IBM PC/AT or compatibles	PC DOS + Windows	3.5-inch 2HC	μS7B13FE9200
			5.25-inch 2HC	μS7B10FE9200
Translator (FT78K3)[Note]	This program converts fuzzy knowledge data, obtained using the tool for creating fuzzy knowledge data, into an assembler source program for RA78K/III.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FT78K3
			5.25-inch 2HD	μS5A10FT78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FT78K3
			5.25-inch 2HC	μS7B10FT78K3
Fuzzy inference module (FI78K/III)[Note]	This program performs fuzzy inference by linking the fuzzy knowledge data converted by Translator.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FI78K3
			5.25-inch 2HD	μS5A10FI78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FI78K3
			5.25-inch 2HC	μS7B10FI78K3
Fuzzy inference debugger (FD78K/III)	This software supports the evaluation and adjustment of fuzzy knowledge data at the hardware level, by using an in-circuit emulator.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FD78K3
			5.25-inch 2HD	μS5A10FD78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FD78K3
			5.25-inch 2HC	μS7B10FD78K3

Note Under development

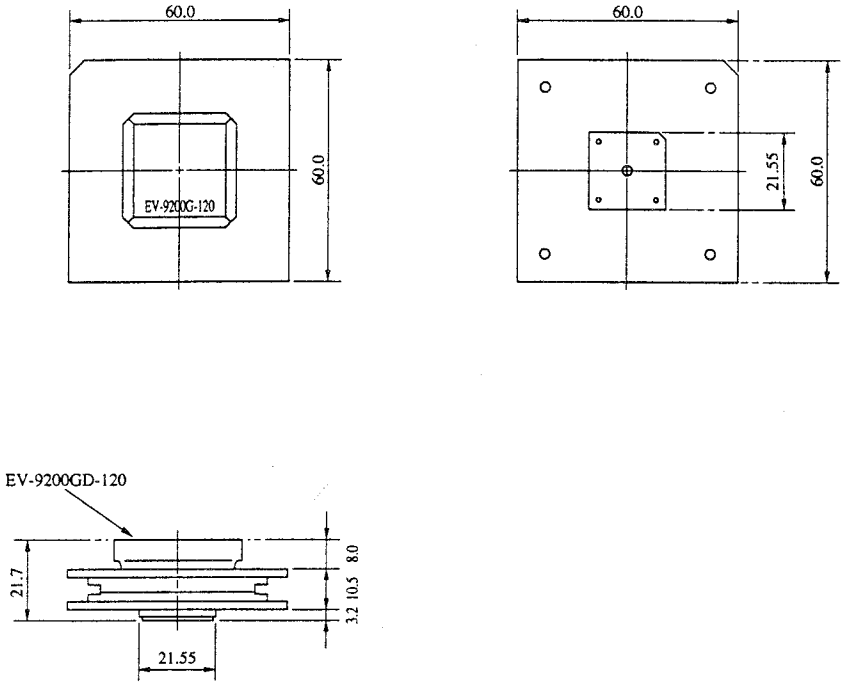
★ APPENDIX B DRAWINGS OF THE CONVERSION ADAPTER

Fig. B-1 Drawings of the Conversion Adapter (EV-9500GC-100) (Reference)



EV-9500GC-100-G0

Fig. B-2 Drawings of the Conversion Adapter (EV-9501GC-100) (Reference)



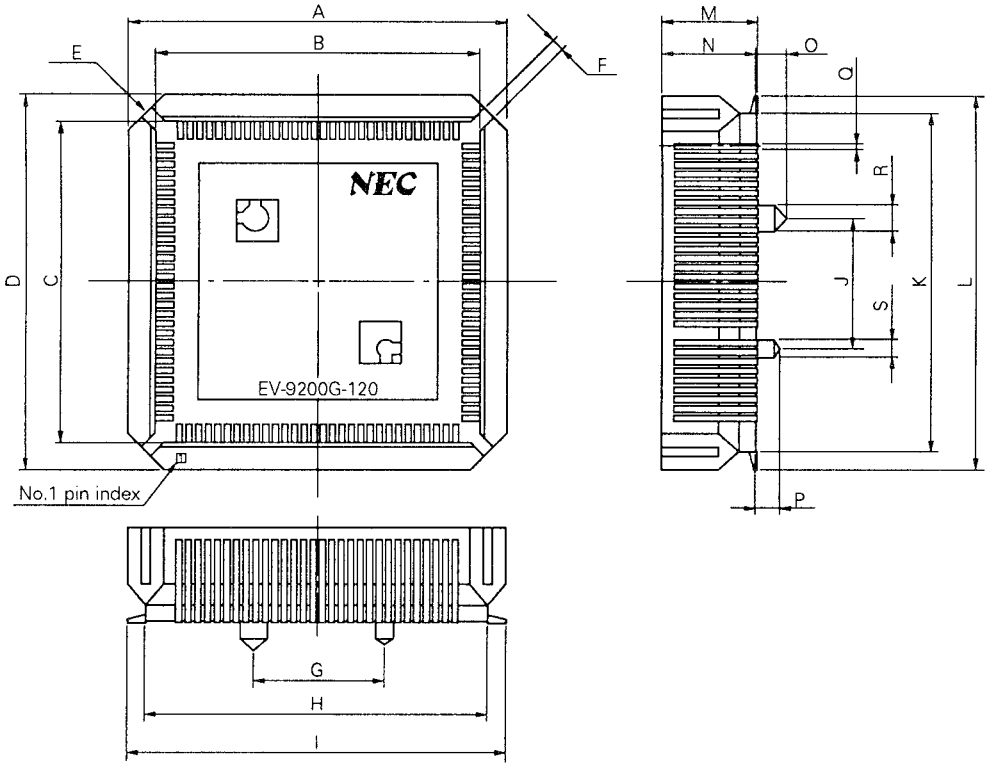
EV-9501GC-100-G0

APPENDIX C DRAWINGS OF THE CONVERSION SOCKET AND RECOMMENDED PATTERN ON BOARDS

Caution Although the part number is EV-9200GD-120, number EV-9200G-120 is marked on the part.

Fig. C-1 Drawings of the Conversion Socket (EV-9200GD-120) (Reference)

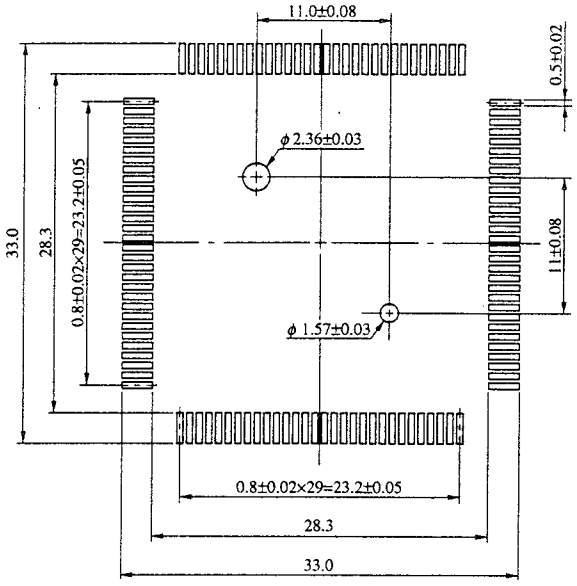
Based on EV-9200G-120
(1) Package drawing (in mm)



EV-9200G-120-G0

ITEM	MILLIMETERS	INCHES
A	32.3	1.272
B	27.6	1.087
C	27.6	1.087
D	32.3	1.272
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	11.0	0.433
H	29.3	1.154
I	32.0	1.26
J	11.0	0.433
K	29.3	1.154
L	32.0	1.26
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	0.35±0.1	$0.014^{+0.004}_{-0.005}$
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Fig. C-2 Recommended Pattern on Boards for the Conversion Socket (EV-9200GD-120) (Reference)



EV-9200G-120-P1

[MEMO]

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

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License not needed	: μPD78P356KP-S
The customer must judge the need for license	: μPD78P356GC-7EA and μPD78P356GD-5BB

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