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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

Phase-out/Discontinued

MOS Integrated Circuit

μPD78P322

16/8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78P322 is a version provided by replacing the μPD75322's internal mask ROM with one-time PROM or EPROM.

Because the one-time PROM version is programmable only once by users, it is ideally suited for small-scale production of many different products, and rapid development and time-to-market of application sets.

The EPROM version is reprogrammable, and suited for the evaluation of systems.

> The μPD78P322K, which is the EPROM version, does not maintain planned reliability when used in mass-produced products. Please use only experimentally or for evaluating functions during trial manufacture.

Functions are described in detail in the following user's manual. Be sure to read it for designing.
μPD78322 User's Manual: IEU-1248

FEATURES

- μPD78322 compatible
  - For mass-production, the μPD78P322 can be replaced with the μPD78322 which incorporates mask ROM
- Internal PROM: 16,384 × 8 bits
  - Programmable once only (one-time PROM version without window)
  - Erasable with ultraviolet rays and electrically programmable (EPROM version with window)
- PROM programming characteristics: μPD27C256A compatible
- The μPD78P328 is a QTOP™ microcontroller

Remark QTOP microcontroller is a general term for microcontrollers which incorporate one-time PROM, and are totally supported by NEC's programming service (from programming to marking, screening, and verification).

ORDERING INFORMATION

Part Number	Package	Internal ROM	Quality Grade
μPD78P322GF-3B9	80-pin plastic QFP (14 × 20 mm)	One-time PROM	Standard
μPD78P322GJ-5BJ	74-pin plastic QFP (20 × 20 mm)	One-time PROM	Standard
μPD78P322L	68-pin plastic QFJ (950 × 950 mils)	One-time PROM	Standard
μPD78P322K	80-pin ceramic WQFN	EPROM	Not applicable
μPD78P322KC	68-pin ceramic WQFN	EPROM	Standard
μPD78P322KD	74-pin ceramic WQFN	EPROM	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Functions common to the one-time PROM and EPROM versions are referred to as PROM functions throughout this document.

The information in this document is subject to change without notice.

Document No. U10435EJ5V0DS00 (5th edition)
(Previous No. IC-2485)
Date Published December 1995 P
Printed in Japan

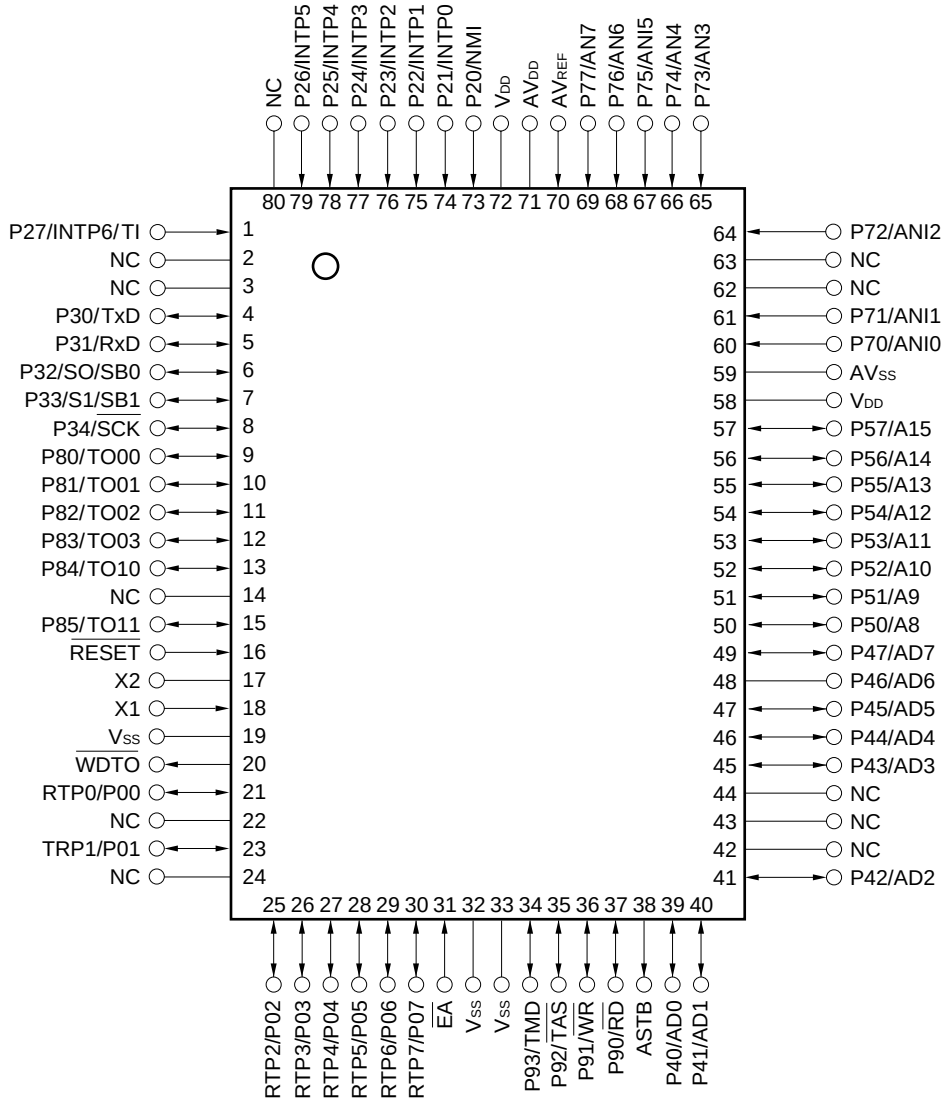
The mark ✱ shows revised points.

Phase-out/Discontinued

PIN CONFIGURATIONS (Top View)

(1) Normal operating mode

- **80-pin plastic QFP (14 × 20 mm)**
  μPD78P322GF-3B9
- **80-pin ceramic WQFN**
  μPD78P322K



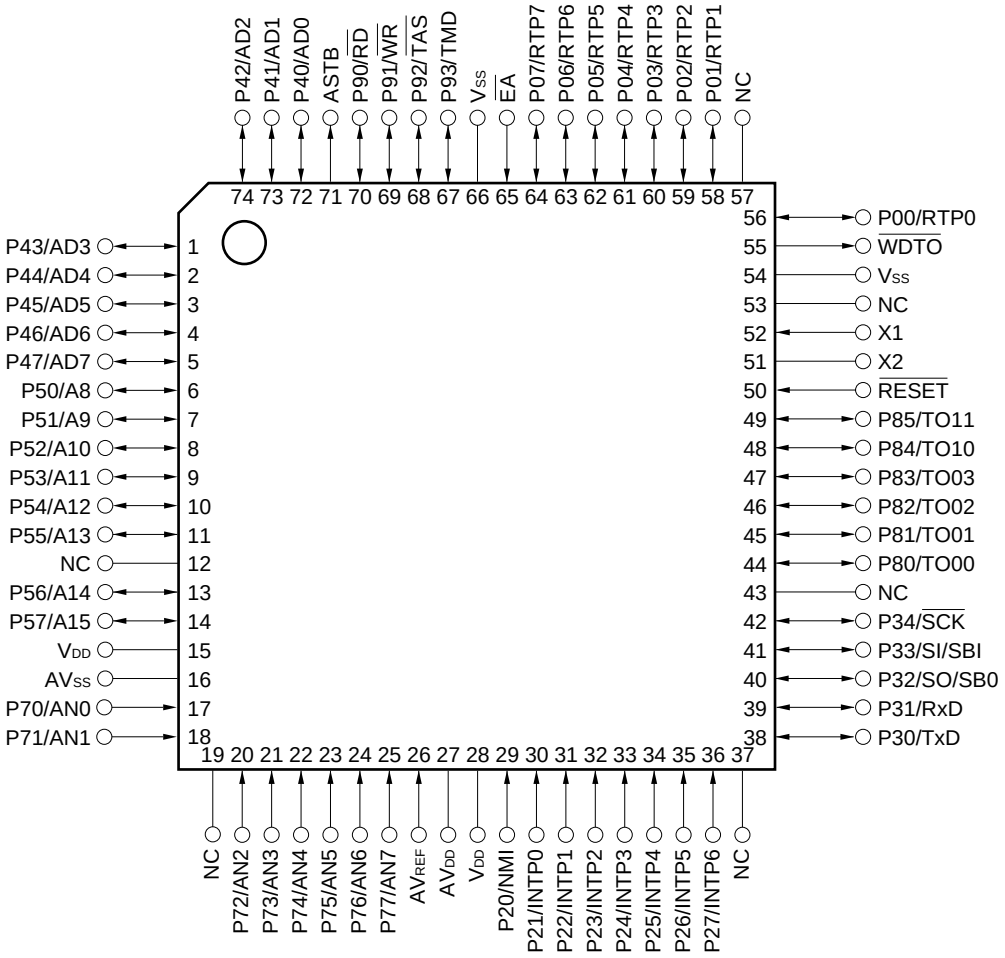
Caution Connect NC pins to V_{SS} as a measure against noise (can leave open).

Remark These pins are compatible with the μPD78322GF pins.

The μPD78P322K does not maintain planned reliability when used in mass-produced products. Please use only experimentally or for evaluating functions during trial manufacture.

Phase-out/Discontinued

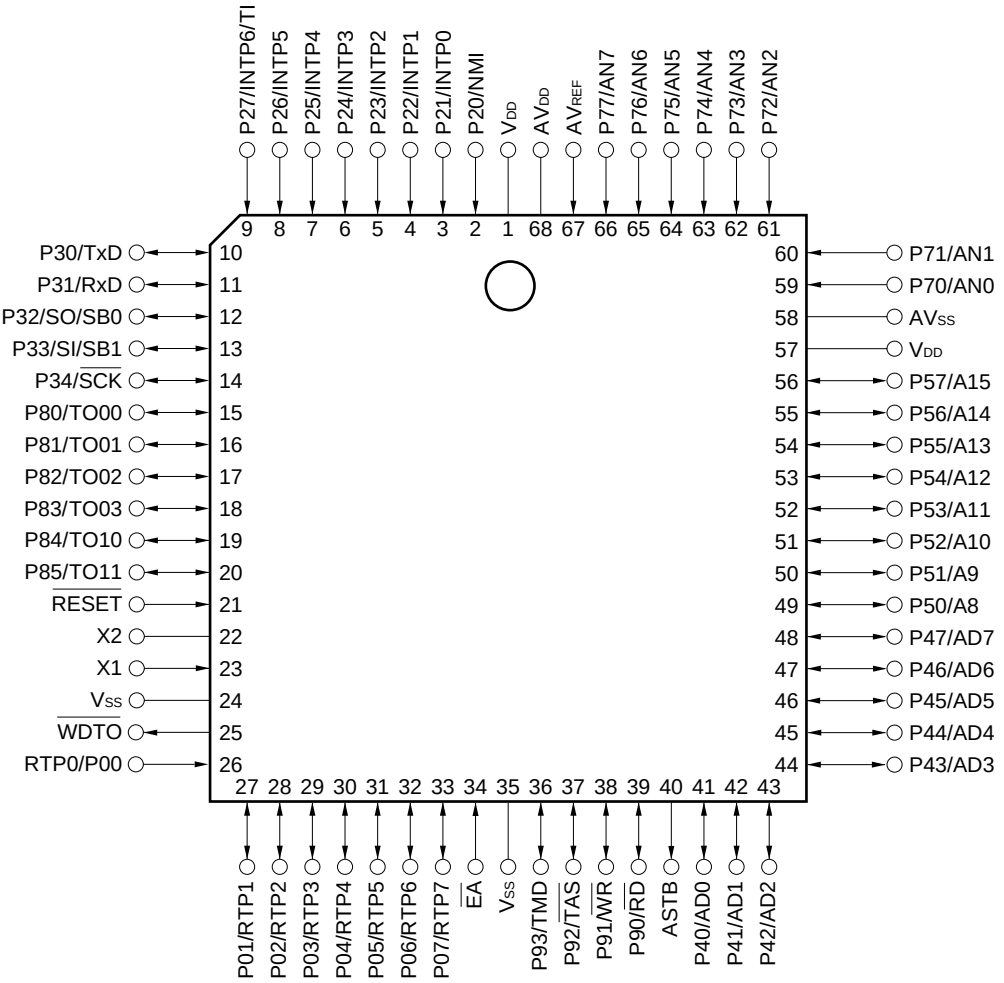
- **74-pin plastic QFP (20 × 20 mm)**
  μPD78P322GJ-5BJ
- **74-pin ceramic WQFN**
  μPD78P322KD



Caution Connect NC pins to V_{SS} for measures against noise (can leave open).

Remark These pins are compatible with the μPD78322GJ pins.

- **68-pin plastic QFJ (950 × 950 mils)**
  μPD78P322L
- **68-pin ceramic WQFN**
  μPD78P322KC



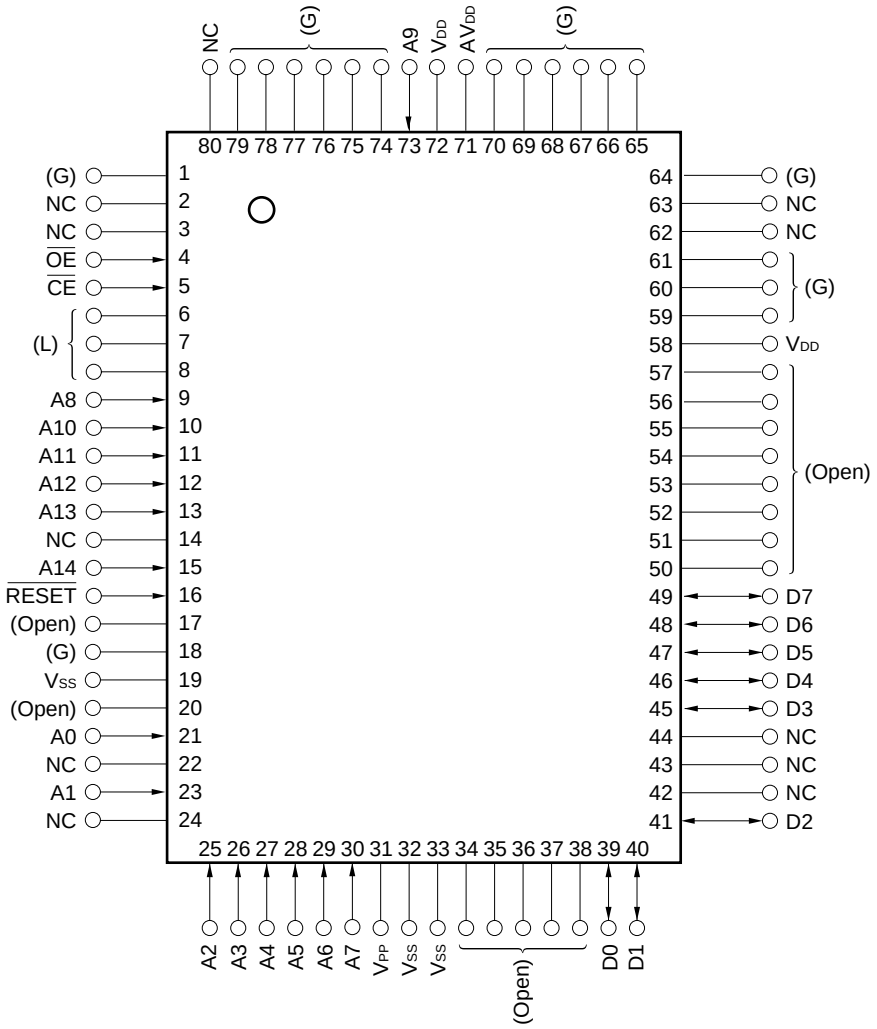
Remark These pins are compatible with the μPD78322L pins.

P00-P07	:	Port 0
P20-P27	:	Port 2
P30-P34	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P70-P77	:	Port 7
P80-P85	:	Port 8
P90-P93	:	Port 9
NMI	:	Nonmaskable Interrupt
INTP0-INTP6	:	Interrupt From Peripherals
RTP0-RTP7	:	Real-Time Port
TI	:	Timer Input
TxD	:	Transmit Data
RxD	:	Receive Data
SB0/SO	:	Serial Bus/Serial Output
SB1/SI	:	Serial Bus/Serial Input
$\overline{SCK}$	:	Serial Clock
TO00-TO03	:	} Timer Output
TO10, TO11	:	

$\overline{RESET}$	:	Reset
X1, X2	:	Crystal
$\overline{WDTO}$	:	Watchdog Timer Output
$\overline{EA}$	:	External Access
TMD	:	Turbo Mode
$\overline{TAS}$	:	Turbo Access Strobe
$\overline{WR}$	:	Write Strobe
$\overline{RD}$	:	Read Strobe
ASTB	:	Address Strobe
AD0-AD7	:	Address/Data Bus
A8-A15	:	Address Bus
AN0-AN7	:	Analog Input
AV_{REF}	:	Analog Reference Voltage
AV_{SS}	:	Analog V_{SS}
AV_{DD}	:	Analog V_{DD}
V_{DD}	:	Power Supply
V_{SS}	:	Ground
NC	:	No Connection

(2) PROM programming mode ($\overline{RESET}$ = H, AV_{DD} = L)

- **80-pin plastic QFP (14 × 20 mm)**
  μPD78P322GF-3B9
- **80-pin ceramic WQFN**
  μPD78P322K



Cautions 1. The recommended connection of the unused pins in the PROM programming mode are indicated in parentheses.

L : Connect each pin to V_{SS} via a resistor.

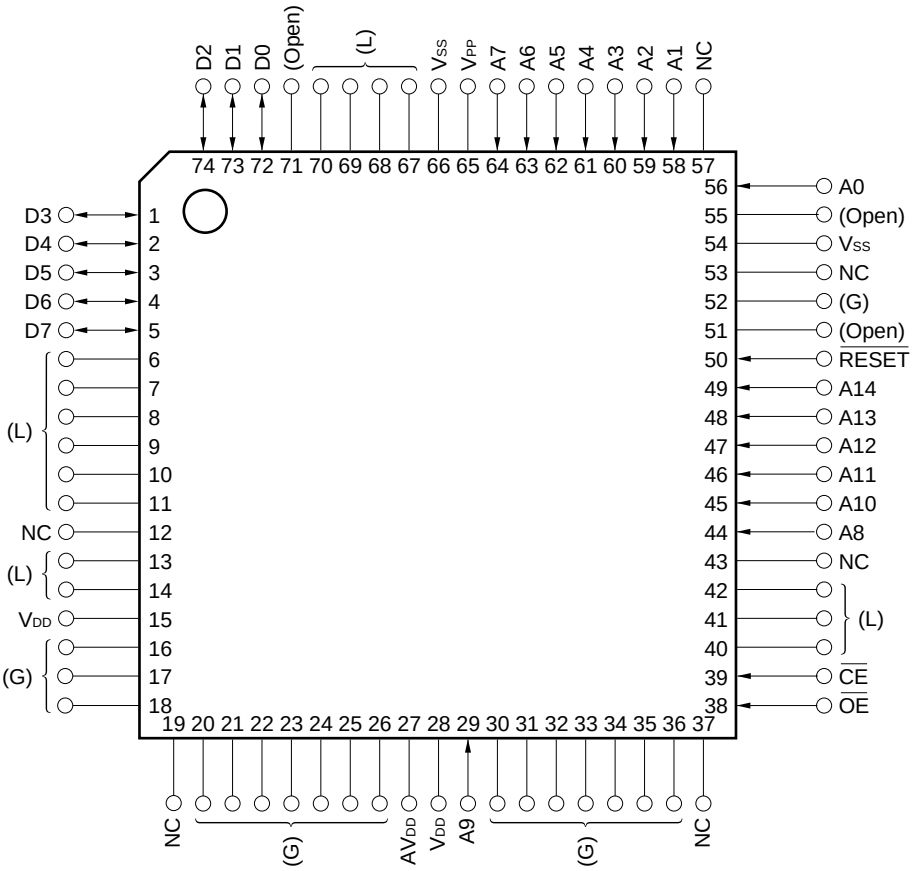
G : Connect the pin to V_{SS}.

Open : Leave the pin unconnected.

2. Connect NC pins to V_{SS} for measures against noise (can leave open).

The μPD78P322K does not maintain planned reliability when used in mass-produced products. Please use only experimentally or for evaluating functions during trial manufacture.

- **74-pin plastic QFP (20 × 20 mm)**
  μPD78P322GJ-5BJ
- **74-pin ceramic WQFN**
  μPD78P322KD



Cautions 1. The recommended connection of the unused pins in the PROM programming mode are indicated in parentheses.

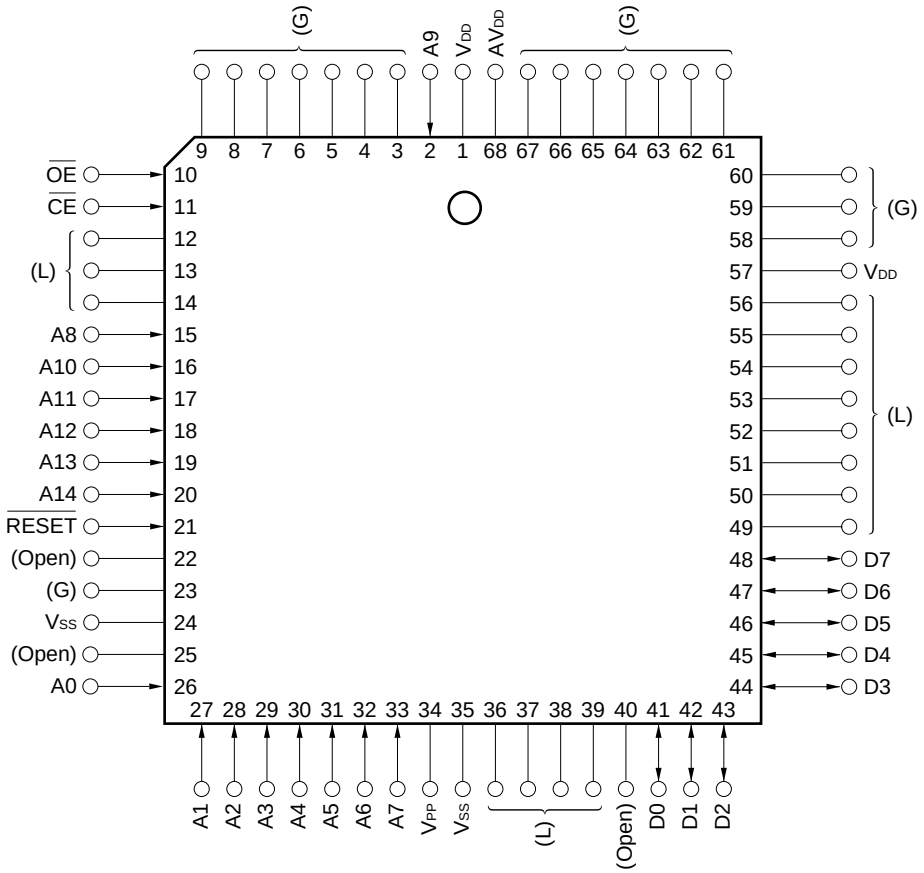
L : Connect each pin to VSS via a resistor.

G : Connect the pin to VSS.

Open : Leave the pin unconnected.

2. Connect NC pins to VSS as measure against noise.

- **68-pin plastic QFJ (950 × 950 mil)**
  μPD78P322L
- **68-pin ceramic WQFN**
  μPD78P322KC



Caution The recommended connection of the unused pins in the PROM programming mode are indicated in parentheses.

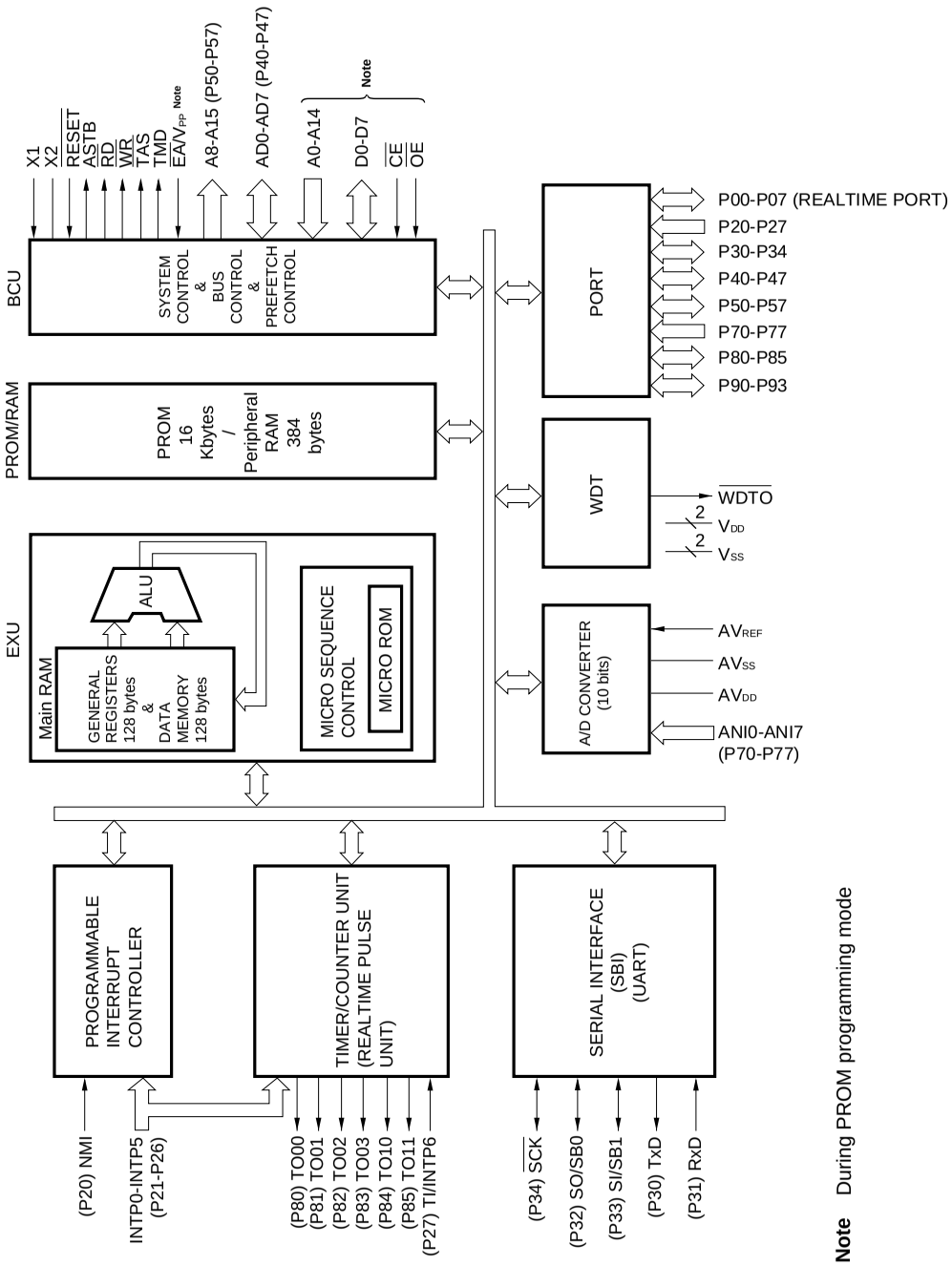
L : Connect each pin to VSS via a resistor.

G : Connect the pin to VSS.

Open : Leave the pin unconnected.

A0-A14	: Address Bus	$\overline{\text{RESET}}$	: }	Programming Mode set
D0-D7	: Data Bus	AVDD	: }	
$\overline{\text{CE}}$	: Chip Enable	VPP	: Programming Power Supply	
$\overline{\text{OE}}$	: Output Enable	NC	: No Connection	

BLOCK DIAGRAM



Note During PROM programming mode

Phase-out/Discontinued

CONTENTS

1. PIN FUNCTIONS

1.1 Normal Operating Mode

(1) Port Pins

Pin Name	Input/Output	Function	Alternate Function
P00-P07	Input/Output (Output)	PORT0 8-bit input/output port Input or output mode can be specified bit-wise. The port can also operate as a real-time output port.	RTP0-RTP7
P20	Input	PORT 2 8-bit input-only port	NMI
P21			INTP0
P22			INTP1
P23			INTP2
P24			INTP3
P25			INTP4
P26			INTP5
P27			INTP6/TI
P30	Input/Output	PORT 3 5-bit input/output port Input or output mode can be specified bit-wise.	TxD
P31			RxD
P32			SO/SB0
P33			SI/SB1
P34			$\overline{\text{SCK}}$
P40-P47	Input/Output	PORT 4 8-bit input/output port Input or output mode can be specified in 8-bit units.	AD0-AD7
P50-P57	Input/Output	PORT 5 8-bit input/output port Input or output mode can be specified bit-wise.	A8-A15
P70-P77	Input	PORT 7 8-bit input-only port	AN0-AN7
P80	Input/Output	PORT 8 6-bit input/output port Input or output mode can be specified bit-wise.	TO00
P81			TO01
P82			TO02
P83			TO03
P84			TO10
P85			TO11
P90	Input/Output	PORT 9 4-bit input/output port Input or output mode can be specified bit-wise.	$\overline{\text{RD}}$
P91			$\overline{\text{WR}}$
P92			$\overline{\text{TAS}}$
P93			$\overline{\text{TMD}}$

(2) Non-Port Pins (1/2)

Pin Name	Input/Output	Function	Alternate Function
RTP0-RTP7	Output	Real-time output port which outputs a pulse in synchronization with the trigger signal from the real-time pulse unit (RPU).	P00-P07
INTP0	Input	Edge-detected external interrupt request input. The valid edge can be specified in the mode register.	P21
INTP1			P22
INTP2			P23
INTP3			P24
INTP4			P25
INTP5			P26
INTP6			P27/TI
NMI	Input	Edge-detected nonmaskable interrupt request input. The rising or falling edge can be selected for the valid edge by setting the mode register.	P20
TI	Input	External count clock input pin to timer 1 (TM1).	P27/INTP6
RxD	Input	Serial data input pin to asynchronous serial interface (UART).	P31
TxD	Output	Serial data output pin from asynchronous serial interface (UART).	P30
SI	Input	Serial data input pin to clocked serial interface in 3-wire mode.	P33/SB1
SO	Output	Serial data output pin from clocked serial interface in 3-wire mode.	P32/SB0
SB0	Input/Output	Serial data input/output pins to/from clocked serial interface in SBI mode.	P32/SO
SB1			P33/SI
$\overline{SCK}$	Input/Output	Serial clock input/output pin to/from clocked serial interface.	P34
AD0-AD7	Input/Output	Multiplexed address/data bus used when external memory is added.	P40-P47
A8-A15	Output	Address bus used when external memory is added.	P50-P57
$\overline{RD}$	Output	Strobe signal output for external memory read operation.	P90
$\overline{WR}$		Strobe signal output for external memory write operation.	P91
* $\overline{TAS}$	Output	Control signal output pins to access turbo access manager (μPD71P301). Note	P92
TMD			P93
TO00	Output	Pulse output from real-time pulse unit.	P80
TO01			P81
TO02			P82
TO03			P83
TO10			P84
TO11			P85
ASTB	Output	Timing signal output pin to externally latch low-order address information output from AD0-AD7 for external memory access.	—
$\overline{WDTO}$	Output	Signal output which indicates that watchdog timer generated non-maskable interrupt.	—
$\overline{EA}$	Input	For μPD78P322, normally connect the $\overline{EA}$ pin to V_{DD}. When the $\overline{EA}$ pin is connected to V_{SS}, the μPD78P322 enters the ROMless mode and external memory is accessed. The EA pin level cannot be changed during operation.	—

Note Turbo access manager (μPD71P301) is available for maintenance purposes only.

(2) Non-Port Pins (2/2)

Pin Name	Input/Output	Function	Alternate Function
AN0-AN7	Input	Analog input to A/D converter.	P70-P77
AV_{REF}	Input	A/D converter reference voltage input.	—
AV_{DD}	—	A/D converter analog power supply.	—
AV_{SS}	—	A/D converter GND.	—
$\overline{RESET}$	Input	System reset input.	—
X1	Input	Crystal resonator connection pin for system clock generation. To supply external clock, input to the X1 and input inverted signal to the X2 pin (X2 pin can be unconnected.)	—
X2			
V_{DD}	—	Positive power supply pin.	—
V_{SS}	—	GND pin.	—
NC	—	No internal connection. Connect to V_{SS} (can leave open).	—

1.2 PROM Programming Mode ($\overline{RESET}$ = H, AV_{DD} = L)

Pin Name	Input/Output	Function
AV_{DD}	Input	PROM programming mode setting.
$\overline{RESET}$		
A0-A14	Input	Address bus.
D0-D7	Input/Output	Data bus.
$\overline{CE}$	Input	PROM enable to PROM.
$\overline{OE}$	Input	Read strobe to PROM.
V_{PP}	—	Write power supply.
V_{DD}		Positive power supply.
V_{SS}		GND.
NC		No internal connection. Connect to V_{SS} (can leave open).

1.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

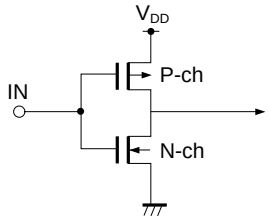
Table 1-1 and Figure 1-1 show the pin input/output circuit schematically.

Table 1-1. Pin Input/Output Circuits and Recommended Connection of Unused Pins

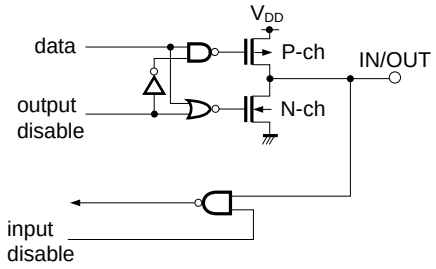
Pin	Input/Output circuit type	Recommended connection of unused pins
P00/RTP0-P07/RTP7	5	Input state: Independently connect to V_{DD} or V_{SS} via a resistor. Output state: Leave Open.
P20/NMI P21/INTP0-P26/INTP5 P27/INTP6/TI	2	Connect to V_{SS}.
P30/TxD P31/RxD	5	Input state: Independently connect to V_{DD} or V_{SS} via a resistor. Output state: Leave Open.
P32/SO/SB0 P33/SI/SB1 P34/$\overline{SCK}$	8	
P40/AD0-P47/AD7 P50/A8-P57/A15	5	
P70/AN0-P77/AN7	9	Connect to V_{SS}.
P80/TO00-P83/TO03 P84/TO10, P85/TO11	5	Input state: Independently connect to V_{DD} or V_{SS} via a resistor. Output state: Leave Open.
P90/$\overline{RD}$ P91/$\overline{WR}$ P92/$\overline{TAS}$ P93/TMD	5	
$\overline{WDTO}$	3	Leave Open.
ASTB	4	
$\overline{EA}$	1	—
$\overline{RESET}$	2	—
AV_{DD}	—	Connect to V_{DD}.
AV_{REF} AV_{SS}	—	Connect to V_{SS}.
V_{PP}	—	Connect to V_{DD}.
NC	—	Connect to V_{SS} (can leave open).

Figure 1-1. Pin Input/Output Circuits

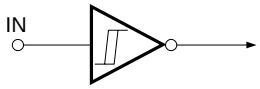
TYPE 1



TYPE 5

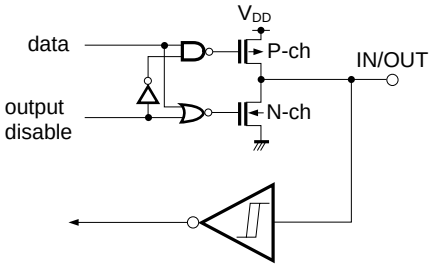


TYPE 2

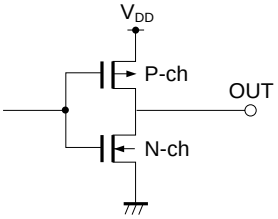


Schmitt-triggerred input with hysteresis characteristics

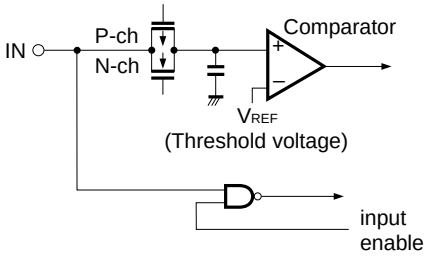
TYPE 8



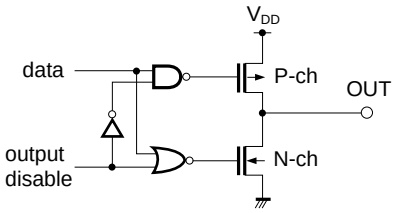
TYPE 3



TYPE 9



TYPE 4



Push-pull output that can be placed in high impedance (both P-ch and N-ch off).

Phase-out/Discontinued

2. DIFFERENCES BETWEEN μPD78P322 and μPD78322

The μPD78P322 is a version provided by replacing the μPD78322's on-chip mask ROM with one-time PROM or EPROM. Thus, the μPD78P322 and μPD78322 are the same in function except for the ROM specifications such as write or verify. Table 2-1 lists the differences between these two products.

This Data Sheet describes the PROM specification function. Refer to the μPD78322 documents for details of other functions.

Table 2-1. Differences between μPD78P322 and μPD78322

Item \ Part Number	**μPD78P322**		μPD78322
Internal program memory (electrical program)	One-time PROM (programmable only once)	EPROM (reprogrammable)	Mask ROM (nonprogrammable)
PROM programming pin	Contained		Not contained
Package	• 68-pin plastic QFJ • 74-pin plastic QFP • 80-pin plastic QFP	• 68-pin ceramic WQFN • 74-pin ceramic WQFN • 80-pin ceramic WQFN	• 68-pin plastic QFJ • 74-pin plastic QFP • 80-pin plastic QFP
* Electrical specifications	Current dissipations are different.		
* Others	Noise immunity and noise radiation differ because circuit complexity and mask layout are different.		

* **Caution The noise immunity and noise radiation differ between the PROM and mask ROM versions. To replace the PROM version with the mask ROM version when shifting from experimental production to mass production, evaluate your system by using the CS version (not ES version) of the mask ROM version.**

3. PROM PROGRAMMING

The PROM incorporated in the μPD78P322 is a 16,384 × 8-bit electrically writable PROM. For programming, set the PROM programming mode by using the $\overline{\text{RESET}}$ and AV_{DD} pins.

The programming characteristics are compatible with the μPD27C256A programming characteristics.

Table 3-1. Pin Function in Programming Mode

Function	Normal Operating Mode	Programming Mode
Address input	P00-P07, P80, P20, P81-P85	A0-A14
Data input	P40-P47	D0-D7
Chip enable/program pulse	P31	$\overline{\text{CE}}$
Output enable	P30	$\overline{\text{OE}}$
Program voltage	V_{PP}	
Mode control	$\overline{\text{RESET}}$, AV_{DD}	

3.1 Operation Mode

To set the program write/verify mode, set $\overline{\text{RESET}}$ = H and AV_{DD} = L. For the mode, the operation mode can be selected by setting the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins, as listed in Table 3-2.

To read the PROM contents, set the read mode.

Connect the unused pins exactly as indicated in Pin Configuration.

Table 3-2. PROM Programming Operation Mode

Mode	$\overline{\text{RESET}}$	AV_{DD}	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{DD}	D0-D7
Program write	H	L	L	H	+12.5 V	+6 V	Data input
Program verify			H	L			Data output
Program inhibit			H	H			High impedance
Read			L	L	+5 V	+5 V	Data output
Output disable			L	H			High impedance
Standby			H	L/H			High impedance

Caution When V_{PP} is set to +12.5 V and V_{DD} is set to +6V, setting both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ to L is prohibited.

3.2 PROM Write Procedure

The write procedure into PROM is as follows:

(1) Fix $\overline{\text{RESET}}$ = H and AV_{DD} = L. Connect other unused pins exactly as indicated in section "Pin Configuration."
(2) Supply +6 V to the V_{DD} and +12.5 V to the V_{PP} pin.
(3) Supply an initial address.
(4) Supply write data.
(5) Supply 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Execute the verify mode. Check whether or not the write data is written normally.
  • When it is written normally: Proceed to step (8).
  • When it is not written normally: Repeat steps (4) to (6).
  If the data is not written normally after 25 repetitions of the steps, proceed to step (7).
(7) Assume the device to be defective. Stop write operation.
(8) Supply write data and X (number of steps (4) to (6) repetitions) x 3 ms program pulses (additional write).
(9) Increment the address.
(10) Repeat steps (4) to (9) to the last address.

Figure 3-1 shows the PROM Write/Verify Timing Steps (2) to (8) above.

Figure 3-1. PROM Write/Verify Timing

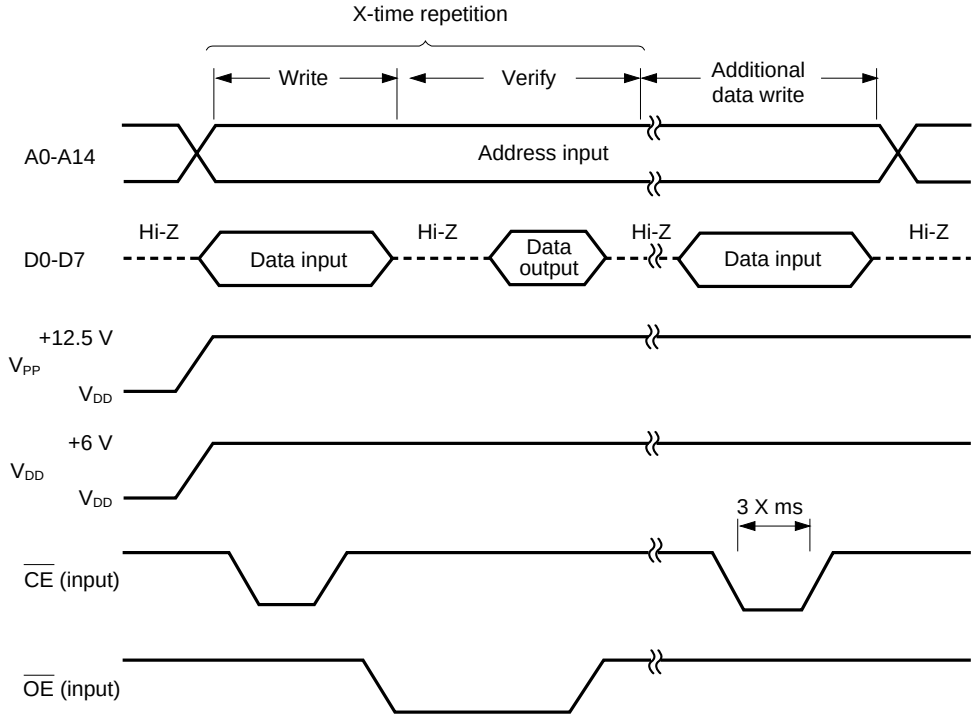
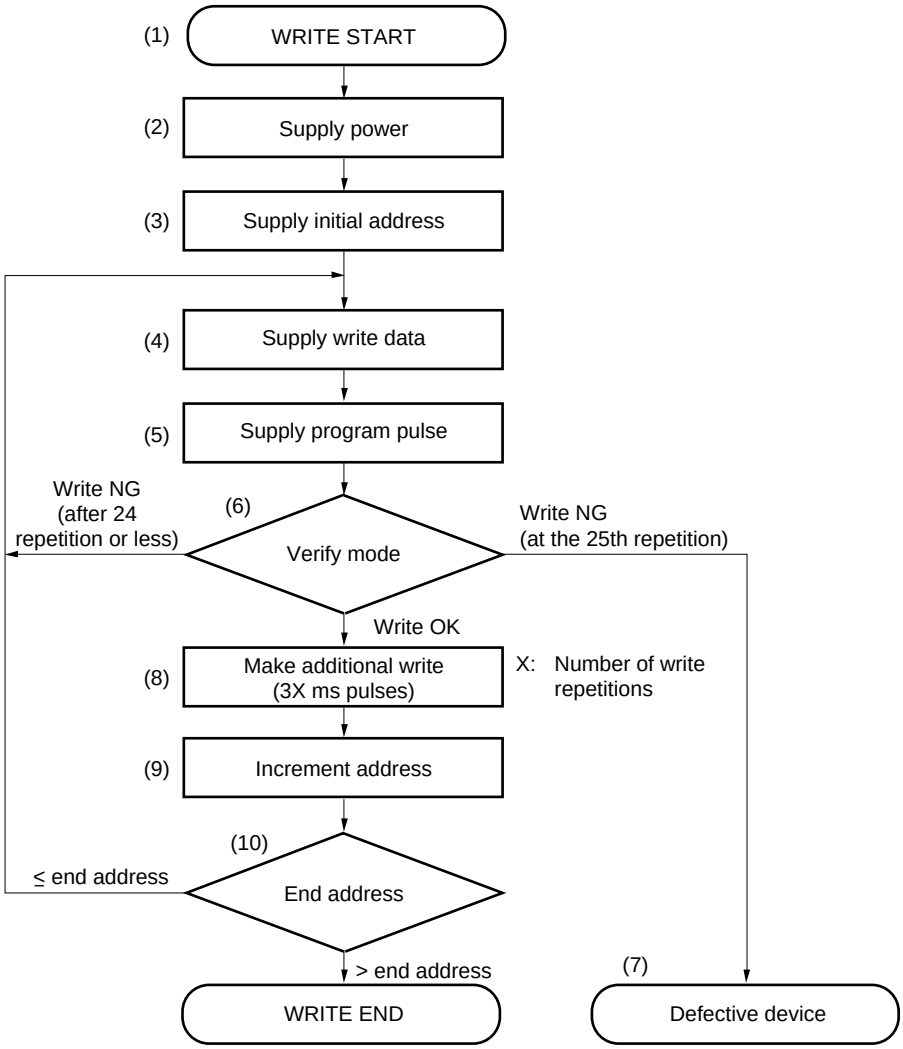


Figure 3-2. Write Procedure Flowchart



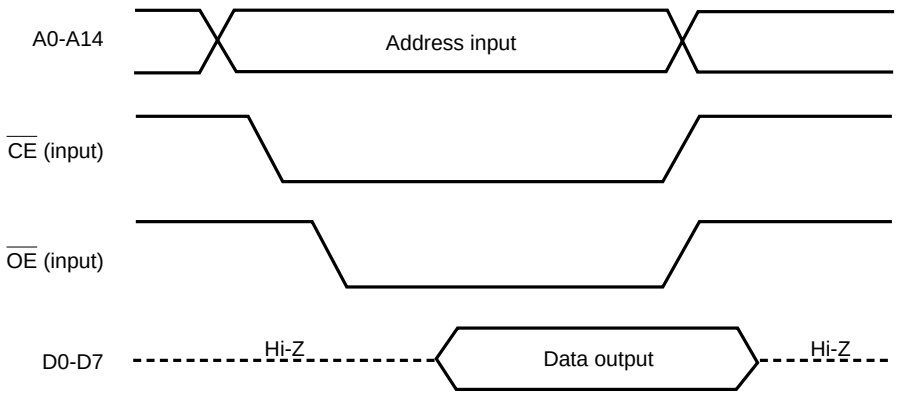
3.3 PROM Read Procedure

The read procedure of the PROM contents into the external data bus (D0-D7) is as follows.

(1) Fix $\overline{\text{RESET}}$ = H and AV_{DD} = L. Connect other unused pins exactly as indicated in Pin Configuration.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0-A14 pins.
(4) Execute the read mode.
(5) The data is output to the D0-D7 pins.

Figure 3-3 shows the PROM read timing steps (2) to (5) above.

Figure 3-3. PROM Read Timing



4. ERASURE CHARACTERISTICS (FOR μPD78P322K/KC/KD ONLY)

The data written into the μPD78P322K/KC/KD program memory can be erased (FFH) and new data can be rewritten into the memory.

To erase data, apply light with a wavelength shorter than 400 nm to the window. Normally, apply ultraviolet rays having the 254-nm wavelength. The radiation amount required to completely erase data is as follows:

- Ultraviolet strength x erasure time: 15 W•s/cm^2 or more
- Erasure time: 15 to 20 minutes when a 12,000 μW/cm^2 ultraviolet lamp is used. However, the time may be prolonged due to ultraviolet lamp performance deterioration, dirty window, etc.

For erasure, place an ultraviolet lamp at a position within 2.5 cm from the window. If a filter is attached to the ultraviolet lamp, remove the filter before applying ultraviolet rays.

5. OPAQUE FILM ON ERASURE WINDOW (FOR μPD78P322K/KC/KD ONLY)

If the μPD78P322K/KC/KD window is exposed to sunlight or fluorescent lamp light for hours, EPROM data may be erased and the internal circuit may operate erroneously. To prevent such accidents from occurring, put a protective seal on the window.

A protective seal whose quality is guaranteed by NEC is attached to every EPROM version with window at shipment.

6. ONE-TIME PROM VERSION SCREENING

The one-time PROM versions (μPD78P322GF-3B9, 78P322GJ-5BJ, 78P322L) cannot be completely tested by NEC for shipment because of their structure. For screening, it is recommended to verify PROM after storing the necessary data under the following conditions:

Storage temperature	Storage time
125°C	24 hours

NEC provides chargeable services ranging from one-time PROM writing to marking, screening and verification for QTOP microcontroller products. For details, contact an NEC sales representative.

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Power supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} +0.5	V
	V_{PP}			–0.5 to +13.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_{I1}	**Note 1**		–0.5 to V_{DD} +0.5	V
	V_{I2}	P20/NIM (A9) PIN		–0.5 to +13.5	V
Output voltage	V_O			–0.5 to V_{DD} +0.5	V
Output current, low	I_{OL}	All output pins		4.0	mA
		Total for all pins		90	mA
Output current, high	I_{OH}	All output pins		–1.0	mA
		Total for all pins		–20	mA
Analog input voltage	V_{IAN}	**Note 2**	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.3	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.3	
Operating ambient temperature	T_A			–10 to +70	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes 1. Pins except for P20/NMI (A9), P70/AN0-P77/AN7

2. P70/AN0-P77/AN7

* **Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

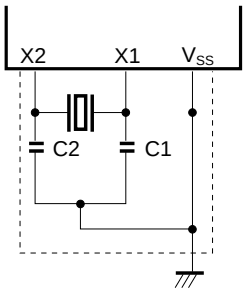
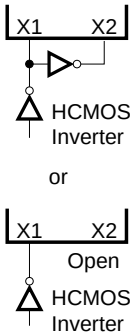
Recommended Operating Conditions

Oscillation frequency	T_A	V_{DD}
8 MHz ≤ f_{XX} ≤ 16 MHz	–10 to +70 ˚C	+5.0 V ±5%

Capacitance (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O	Unmeasured pins returned to 0 V			20	pF
I/O capacitance	C_{IO}				20	pF

Oscillator Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V±5%, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic or crystal resonator		Oscillation frequency (f_{XX})	8	16	MHz
External clock		X1 input frequency (f_X)	8	16	MHz
		X1 input rise, fall time (f_{XR}, t_{XF})	0	20	ns
		X1 input high, low level width (t_{WXH}, t_{WXL})	25	80	ns

Caution When using the system clock oscillator, wire the portion enclosed in broken lines in the figure as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{SS}. Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillator.**

Recommended Oscillator Constants

Ceramic resonator

Manufacturer Name	Part Number	Frequency [MHz]	Recommended Constants	
			C1 [pF]	C2 [pF]
MURATA	CSA8.00MT	8.0	30	30
	CSA12.0MT	12.0		
	CSA14.74MXZ040	14.74	15	15
	CSA16.00MX040	16.0		
	CST8.00MTW	8.0	Internal	Internal
	CST12.0MTW	12.0		
	CST14.74MXW0C3	14.74		
	CST16.00MXW0C3	16.0		

Crystal resonator

Manufacturer Name	Part Number	Frequency [MHz]	Recommended Constants	
			C1 [pF]	C2 [pF]
KINSEKI	HC49/U-S	8 to 16	10	10
	HC49/U			

DC Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V ±5%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL}			0		0.8	V
Input voltage, high	V_{IH1}	**Note 1**		2.2			V
	V_{IH2}	**Note 2**		$0.8V_{DD}$			
Output voltage, low	V_{OL}	I_{OL} = 2.0 mA				0.45	V
Output voltage, high	V_{OH}	I_{OH} = –400 μA		V_{DD}–1.0			V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} power supply current	I_{DD1}	Operation mode			40	65	mA
	I_{DD2}	HALT mode			20	35	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	10	μA
			V_{DDDR} = 5.0 V ±5%		10	50	μA

Notes 1. Pins other than mentioned in **Note 2**.

2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/TI, P32/SO/SB0, P33/SI/SB1, or P34/$\overline{\text{SCK}}$ pins.

* **AC Characteristics** (T_A = –10 to +70 °C, V_{DD} = +5 V ±5%, V_{SS} = 0 V)

Discontinuous read/write operation (when general-purpose memory is connected)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		125	250	ns
Address setup time (to ASTB ↓)	t_{SAST}		32		ns
Address hold time (from ASTB ↓)	t_{HSTA}		32		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR}		85		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			0	ns
Address → data input time	t_{DAID}			222	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			112	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR}		42		ns
Data hold time (from $\overline{RD}$ ↑)	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA}		50		ns
$\overline{RD}$ low level width	t_{WRL}		157		ns
ASTB high level width	t_{WSTH}		37		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW}		85		ns
ASTB ↓ → data output time	t_{DSTOD}			102	ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			40	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW}		42		ns
Data setup time (to $\overline{WR}$ ↑)	t_{SODW}		147		ns
Data hold time (from $\overline{WR}$ ↑)	t_{HWOD}		32		ns
$\overline{WR}$ ↑ → ASTB ↑ delay time	t_{DWST}		42		ns
$\overline{WR}$ low level width	t_{WWL}		157		ns

t_{CYK}-Dependent Bus Timing Definition

Parameter	Calculation expression	MIN./MAX.	Unit
t_{SAST}	0.5T – 30	MIN.	ns
t_{HSTA}	0.5T – 30	MIN.	ns
t_{DAR}	T – 40	MIN.	ns
t_{DAID}	(2.5 + n) T – 90	MAX.	ns
t_{DRID}	(1.5 + n) T – 75	MAX.	ns
t_{DSTR}	0.5T – 20	MIN.	ns
t_{DRA}	0.5T – 12	MIN.	ns
t_{WRL}	(1.5 + n) T – 30	MIN.	ns
t_{WSTH}	0.5T – 25	MIN.	ns
t_{DAW}	T – 40	MIN.	ns
t_{DSTOD}	0.5T + 40	MAX.	ns
t_{DSTW}	0.5T – 20	MIN.	ns
t_{SODW}	1.5T – 40	MIN.	ns
t_{HWOD}	0.5T – 30	MIN.	ns
t_{DWST}	0.5T – 20	MIN.	ns
t_{WWL}	(1.5 + n) T – 30	MIN.	ns

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency).

2. n is the number of wait cycles defined by user software.

3. Only parameters listed in the table are dependent on t_{CYK}.

Serial Operation (T_A = –10 to +70 °C, V_{DD} = +5 V ±5%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	SCK Output	Internal divide by 8	1		μs
		SCK Input	External clock	1		μs
Serial clock high-level width	t_{WSKL}	SCK Output	Internal divide by 8	420		ns
		SCK Input	External clock	420		ns
Serial clock high-level width	t_{WSKH}	SCK Output	Internal divide by 8	420		ns
		SCK Input	External clock	420		ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SRXSK}			80		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKRX}			80		ns
$\overline{SCK}$ ↓ → SO delay time	t_{DSKTX}	R = 1 kΩ, C = 100 pF			210	ns

Other operations (T_A = –10 to +70°C, V_{DD} = +5 V±5%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI high, low-level width	t_{WNIH}, t_{WNIL}		5		μs
INTP0 high, low-level width	t_{WI0H}, t_{WI0L}		8T		t_{CYK}
INTP1 high, low-level width	t_{WI1H}, t_{WI1L}		8T		t_{CYK}
INTP2 high, low-level width	t_{WI2H}, t_{WI2L}		8T		t_{CYK}
INTP3 high, low-level width	t_{WI3H}, t_{WI3L}		8T		t_{CYK}
INTP4 high, low-level width	t_{WI4H}, t_{WI4L}		8T		t_{CYK}
INTP5 high, low-level width	t_{WI5H}, t_{WI5L}		8T		t_{CYK}
INTP6 high, low-level width	t_{WI6H}, t_{WI6L}		8T		t_{CYK}
$\overline{RESET}$ high, low-level width	t_{WRSH}, t_{WRSL}		5		μs
TI high, low-level width	t_{WTIH}, t_{WTIL}	TM1 In the event counter mode	8T		t_{CYK}

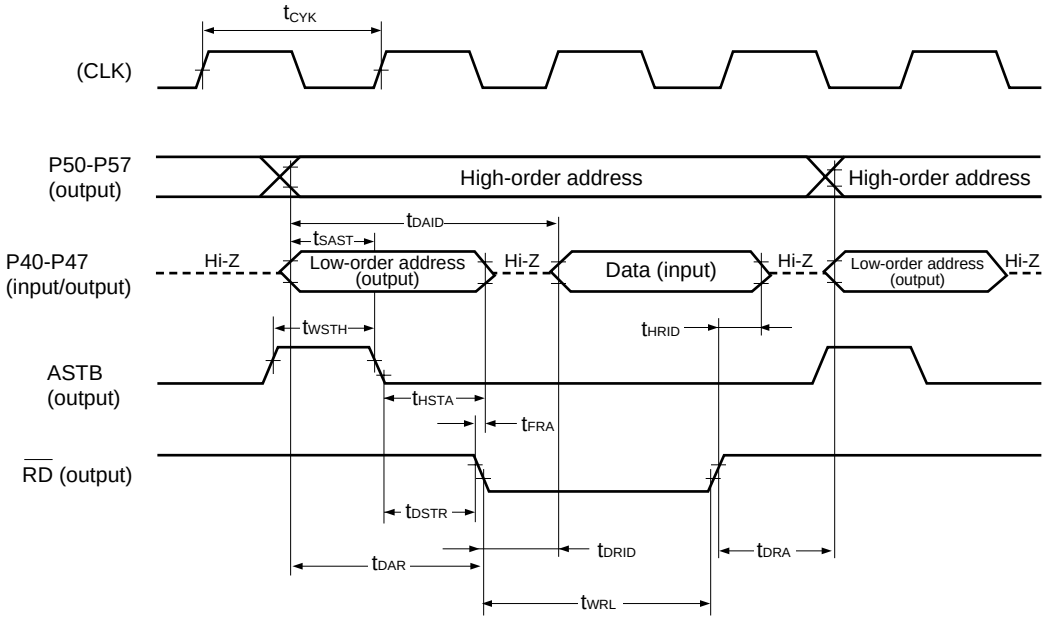
A/D Converter (T_A = –10 to +70°C, V_{DD} = +5 V±5%, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.4	%FSR
		3.4 V ≤ AV_{REF} ≤ AV_{DD}				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}			144			t_{CYK}
Sampling time	t_{SAMP}			24			t_{CYK}
Zero scale error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±4.5	LSB
Fullscale error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±4.5	LSB
Nonlinear error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±4.5	LSB
Analog input voltage Note2	V_{IAN}			–0.3		AV_{DD}	V
Basic voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}				2.0	6.0	mA
A/D converter data	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2.0	10	μA
retention current			AV_{DDDR} = 5 V±5%		10	50	μA

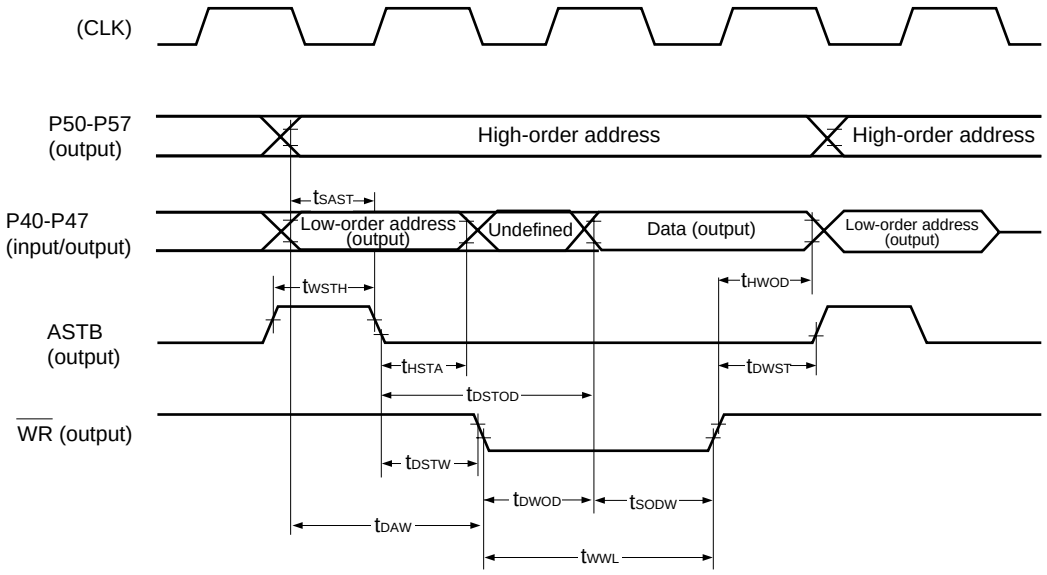
Notes 1. Quantization error is excluded.

2. When –0.3 V ≤ V_{IAN} ≤ 0 V, conversion result is 000H.
When 0 V < V_{IAN} < AV_{REF}, conversion is executed with 10-bit resolution.
When AV_{REF} ≤ V_{IAN} ≤ AV_{DD}, conversion result is 3FFH.

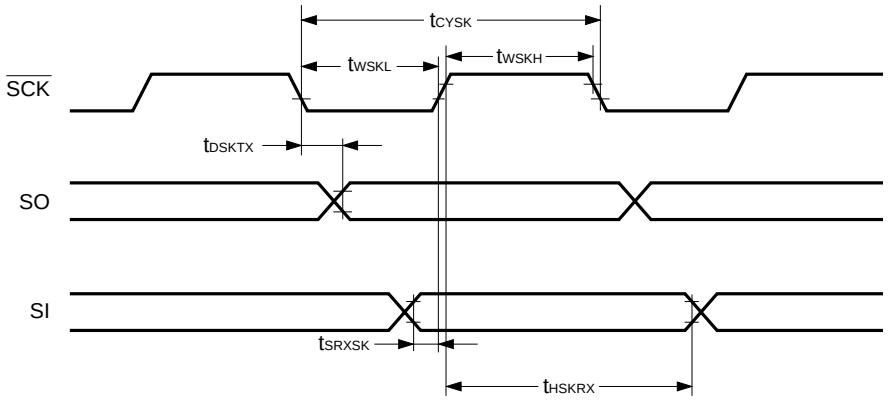
Discontinuous Read Operation



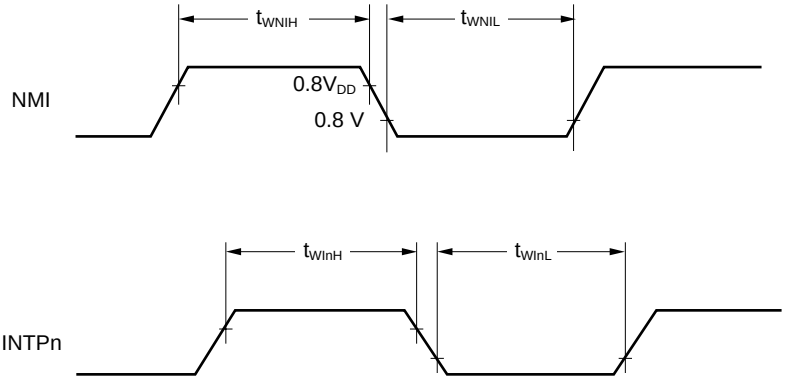
Discontinuous Write Operation



Serial Operation

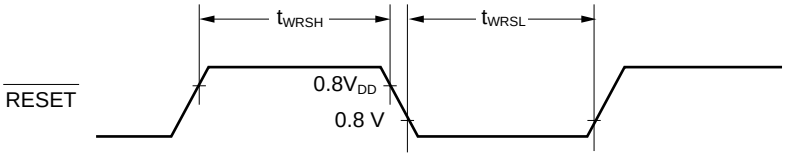


Interrupt Input Timing

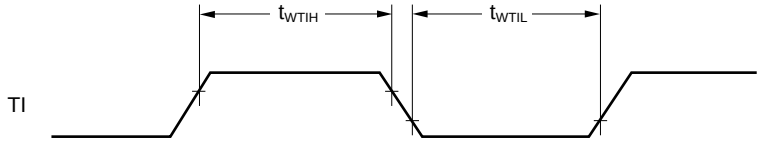


Remark n = 0-6

Reset Input Timing



TI Pin Input Timing



DC Programming Characteristics (T_A = 25 ± 5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol Note1	Test conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		2.2		V_{DDP} +0.3	V
Input voltage, low	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$ Note 2			±10	μA
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –400 μA	2.4			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Input current	I_{A9}	—	A9 (P20/NMI) pin			±10	μA
Output leakage current	I_{LO}	—	$0 \le V_O \le V_{DDP}$, $\overline{OE} = V_{IN}$			10	μA
PROG pin high voltage input current	I_{IP}	—				±10	μA
V_{DDP} power supply voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} power supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	$V_{PP} = V_{DDP}$			V
V_{DDP} power supply current	I_{DD}	I_{DD}	Program memory write mode		10	30	mA
			Program memory read mode $\overline{CE} = V_{IL}$, $V_I = V_{IH}$		10	30	mA
V_{PP} power supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		10	30	mA
			Program memory read mode		1	100	μA

Notes 1. Corresponding μPD27C256A symbols.

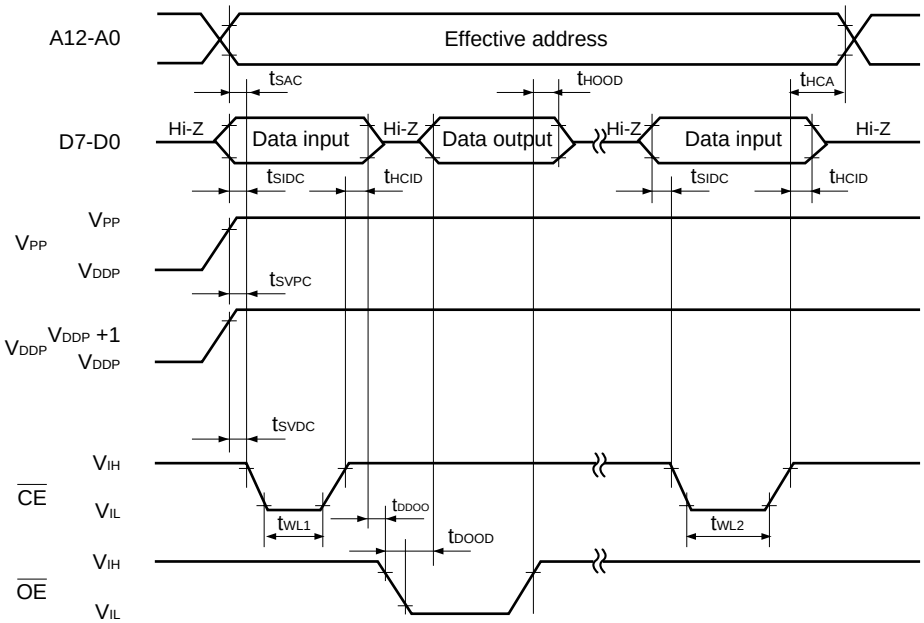
2. V_{DDP} is V_{DD} pin during the programming mode.

AC Programming Characteristics (T_A = 25 ± 5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol Note	Test conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{CE}$ ↓)	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time (to $\overline{CE}$ ↓)	t_{SIDC}	t_{DS}		2			μs
Address hold time (from $\overline{CE}$ ↑)	t_{HCA}	t_{AH}		2			μs
Input data hold time (from $\overline{CE}$ ↑)	t_{HCID}	t_{DH}		2			μs
Output data hold time (from $\overline{OE}$ ↑)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (to $\overline{CE}$ ↓)	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} setup time (to $\overline{CE}$ ↓)	t_{SVDC}	t_{VDS}		2			μs
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
Address → data output time	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{OE}$ ↓ → data output time	t_{DOOD}	t_{OE}				1	μs
Data hold time (from $\overline{OE}$ ↑)	t_{HCOD}	t_{DF}		0		130	ns
Data hold time (from address)	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C256A symbols.

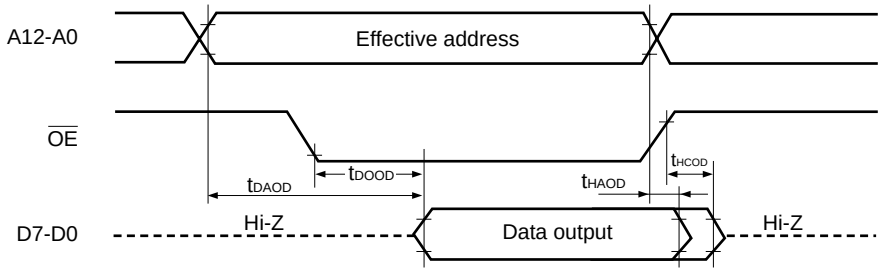
PROM Write Mode Timing



Cautions 1. Apply V_{DDP} before V_{PP} and remove it after V_{PP}.

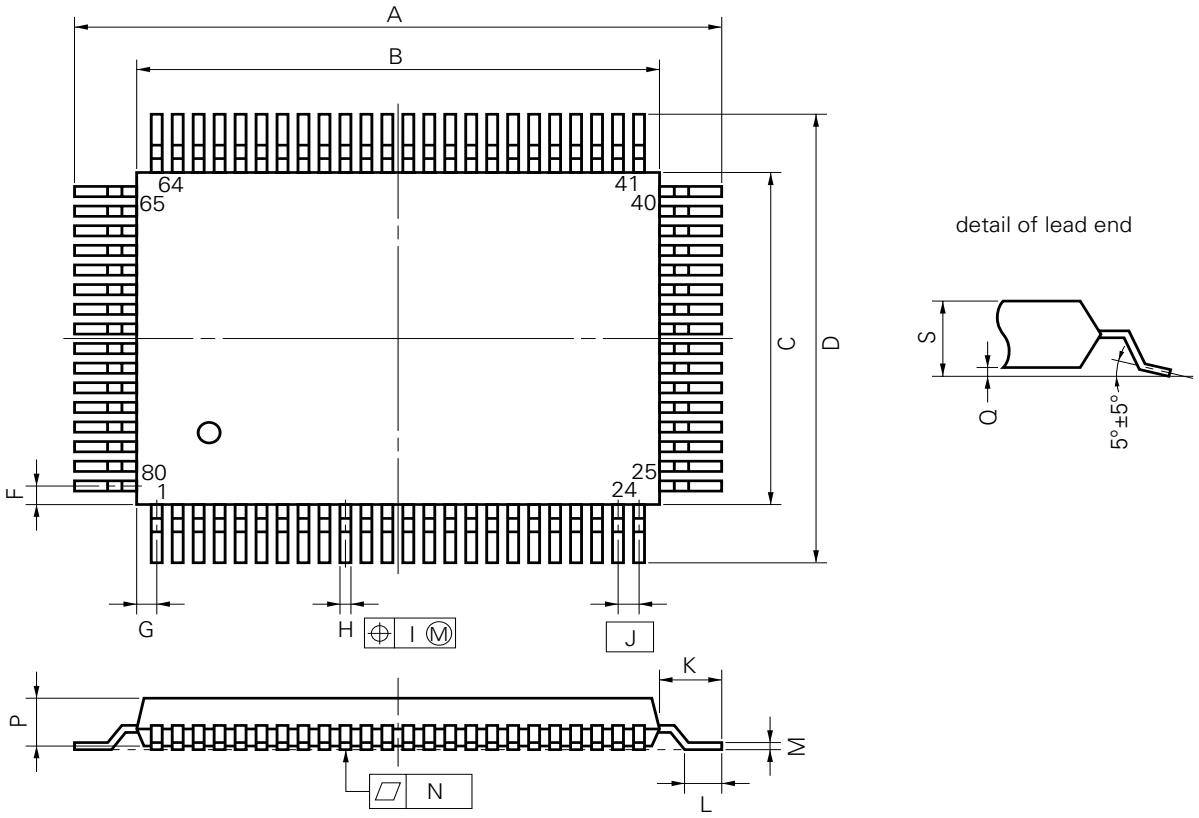
2. V_{PP} must not exceed +13 V, including the overshoot.

PROM Read Mode Timing



8. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)



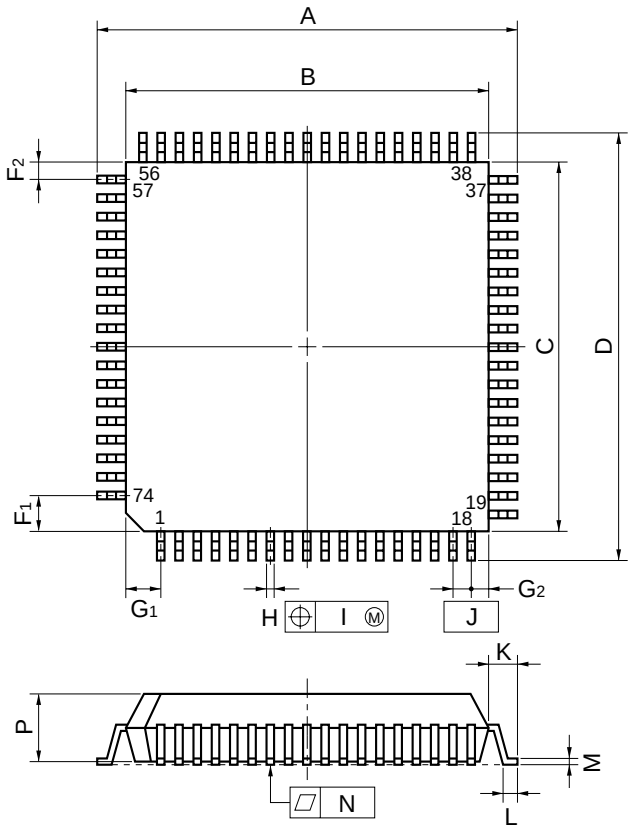
P80GF-80-3B9-2

NOTE

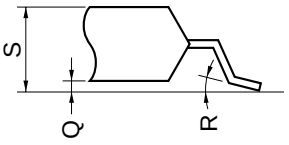
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

74 PIN PLASTIC QFP (□20)



detail of lead end



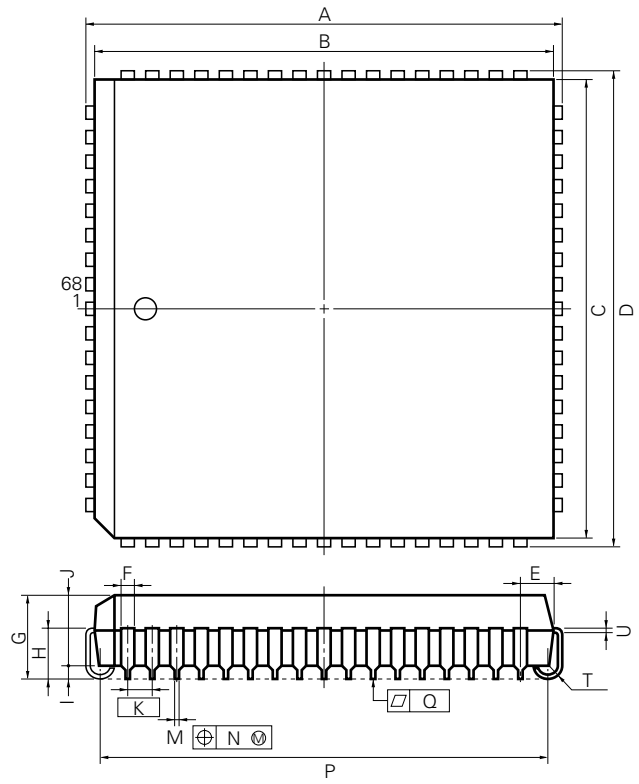
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	$0.913^{+0.017}_{-0.016}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	23.2±0.4	$0.913^{+0.017}_{-0.016}$
F_1	2.0	0.079
F_2	1.0	0.039
G_1	2.0	0.079
G_2	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	4.0 MAX.	0.158 MAX.

S74GJ-100-5BJ-3

68 PIN PLASTIC QFJ (□950 mil)



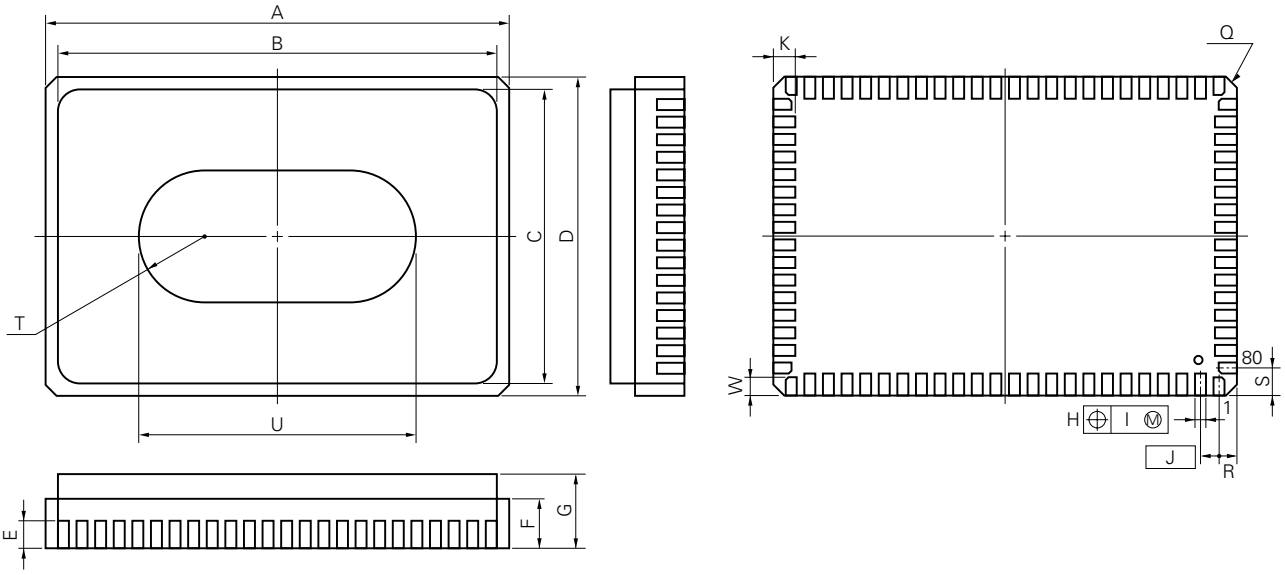
P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

80 PIN CERAMIC WQFN



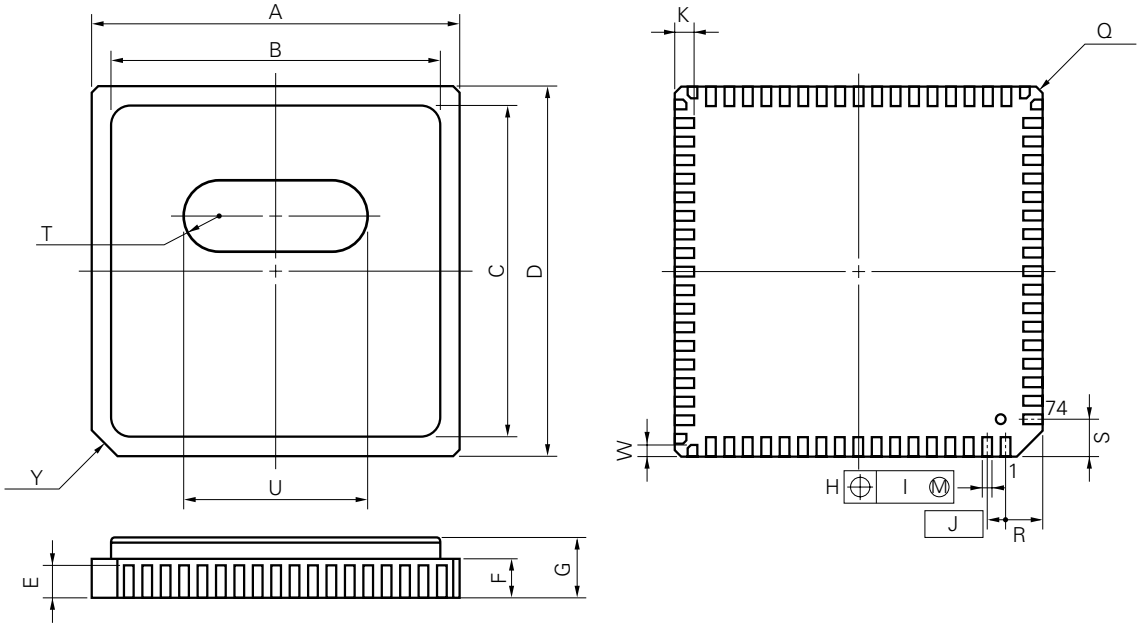
X80KW-80A-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	14.2±0.4	0.559±0.016
E	1.64	0.065
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.5	C 0.020
R	0.8	0.031
S	1.1	0.043
T	R 3.0	R 0.118
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$

74 PIN CERAMIC WQFN



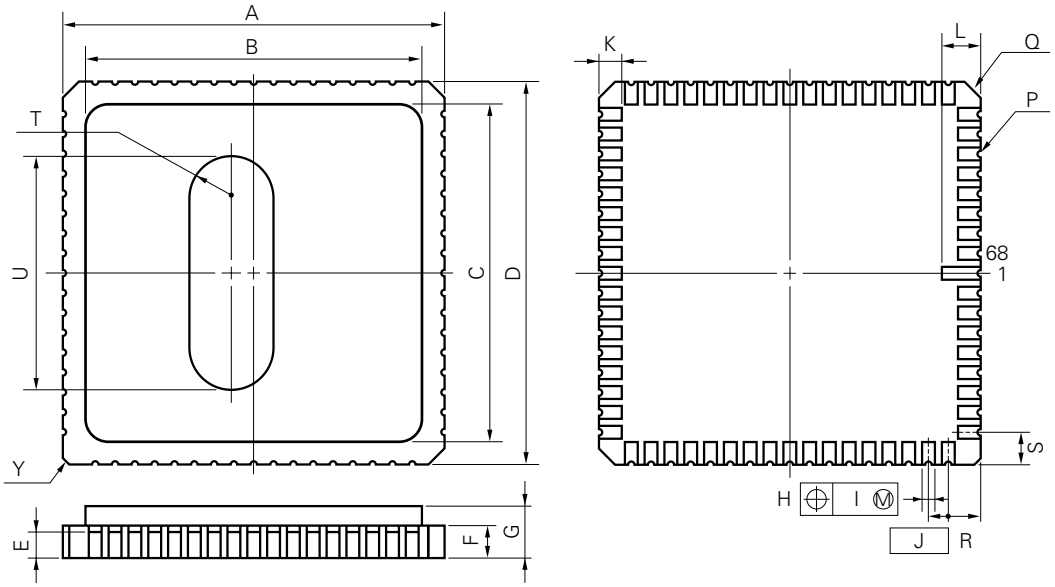
X74KW-100A-1

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	18.0	0.709
C	18.0	0.709
D	20.0±0.4	$0.787^{+0.017}_{-0.016}$
E	1.94	0.076
F	2.14	0.084
G	4.0 MAX.	0.158 MAX.
H	0.51±0.10	0.020±0.004
I	0.10	0.004
J	1.0 (T.P.)	0.039 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	2.0	0.079
S	2.0	0.079
T	R 2.0	R 0.079
U	10.0	0.394
W	0.7±0.2	$0.028^{+0.008}_{-0.009}$
Y	C 1.5	C 0.059

68 PIN CERAMIC WQFN



X68KW-50A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	24.13±0.4	0.950±0.016
B	21.5	0.846
C	21.5	0.846
D	24.13±0.4	0.950±0.016
E	1.65	0.065
F	2.03	0.080
G	3.50 MAX.	0.138 MAX.
H	0.64±0.10	$0.025^{+0.005}_{-0.004}$
I	0.12	0.005
J	1.27 (T.P.)	0.05 (T.P.)
K	1.27±0.2	0.05±0.008
L	2.16±0.2	0.085±0.008
P	R 0.2	R 0.008
Q	C 1.02	C 0.04
R	1.905	0.075
S	1.905	0.075
T	R 3.0	R 0.118
U	12.0	0.472
Y	C 0.5	C 0.020

Phase-out/Discontinued

9. RECOMMENDED SOLDERING CONDITIONS

It is recommended that this device be soldered under the following conditions.

For details on the recommended soldering conditions, refer to information document **"Semiconductor Devices Mounting Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 9-1. Soldering Conditions for Surface Mount Devices (1/2)

* **μPD78P322GF-3B9: 80-pin plastic QFP (14 × 20 mm)**

Soldering Method	Soldering Conditions	Recommended Soldering Code
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Maximum number of days: 7 days[Note] (thereafter, 20 hours of prebaking is required at 125°C) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-207-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 2 max., Maximum number of days: 7 days[Note] (thereafter, 20 hours of prebaking is required at 125°C) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-207-2
Wave soldering	Soldering bath temperature: 260°C max., Time: 10 seconds max., Number of times: 1, Preheating temperature: 120°C max. (package surface temperature), Maximum number of days: 7 days[Note] (thereafter, 20 hours of prebaking is required at 125°C).	WS60-207-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin)	—

μPD78P322GJ-5BJ: 74-pin plastic QFP (20 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Soldering Code
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (210°C min.), Number of times: 1, Maximum number of days: 7 days[Note] (thereafter, 10 hours of prebaking is required at 125°C)	IR30-107-1
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 1, Maximum number of days: 7 days[Note] (thereafter, 20 hours of prebaking is required at 125°C)	VP15-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin)	—

Note Number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

Caution Do not use different soldering methods together (except for partial heating method).

Table 9-1. Soldering Conditions for Surface Mount Devices (2/2) *

μPD78P322L: 68-pin plastic QFJ (950 × 950 mils)

Soldering Method	Soldering Conditions	Recommended Soldering Code
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Maximum number of days: 7 days[Note] (thereafter, 36 hours of prebaking is required at 125°C) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-367-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 2 max., Maximum number of days: 7 days[Note] (thereafter, 36 hours of prebaking is required at 125°C) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-367-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin)	—

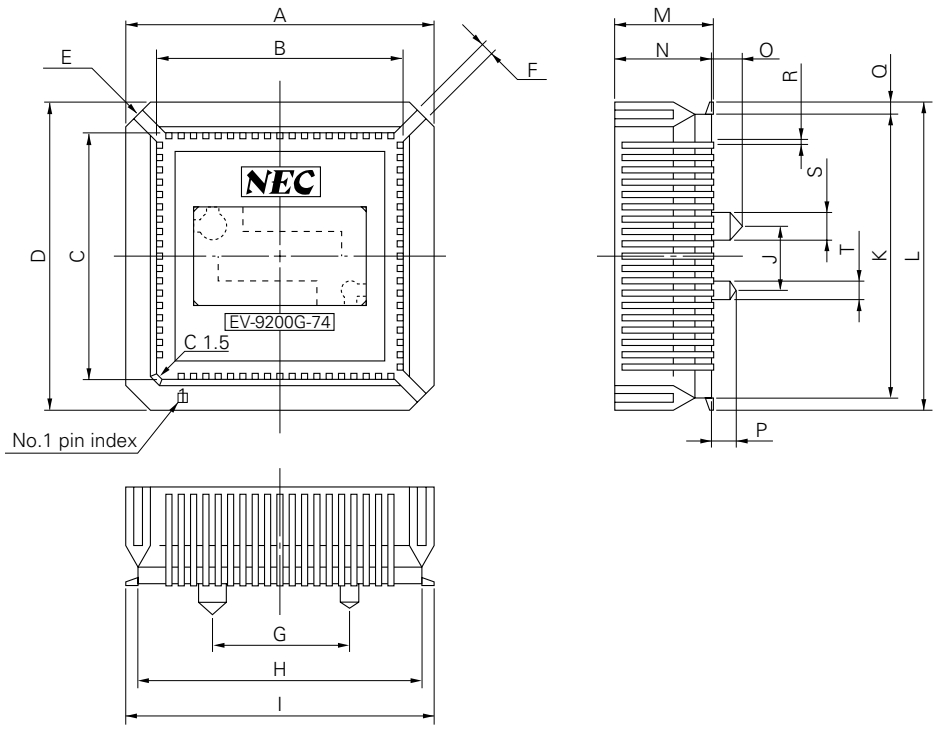
Note Number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

Caution Do not use different soldering methods together (except for partial heating method).

APPENDIX A. DRAWINGS OF CONVERSION SOCKETS AND RECOMMENDED FOOTPRINTS

(1) EV-9200G-74

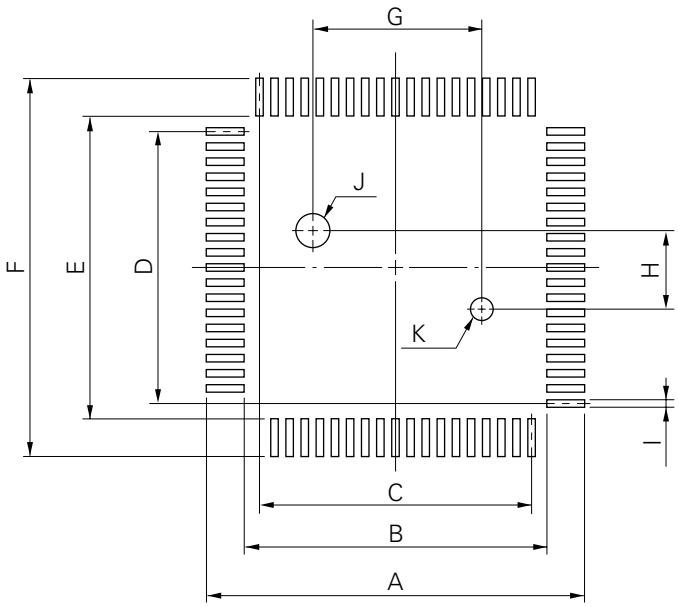
Figure A-1. Drawing of Conversion Socket (EV-9200G-74)
(For reference only)



EV-9200G-74-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.35	0.801
C	20.35	0.801
D	25.0	0.984
E	4-C 2.8	4-C 0.11
F	1.0	0.039
G	11.0	0.433
H	22.0	0.866
I	24.7	0.972
J	5.0	0.197
K	22.0	0.866
L	24.7	0.972
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	$0.014^{+0.004}_{-0.005}$
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Figure A-2. Recommended Footprint of Conversion Socket (EV-9200G-74) (For reference only)



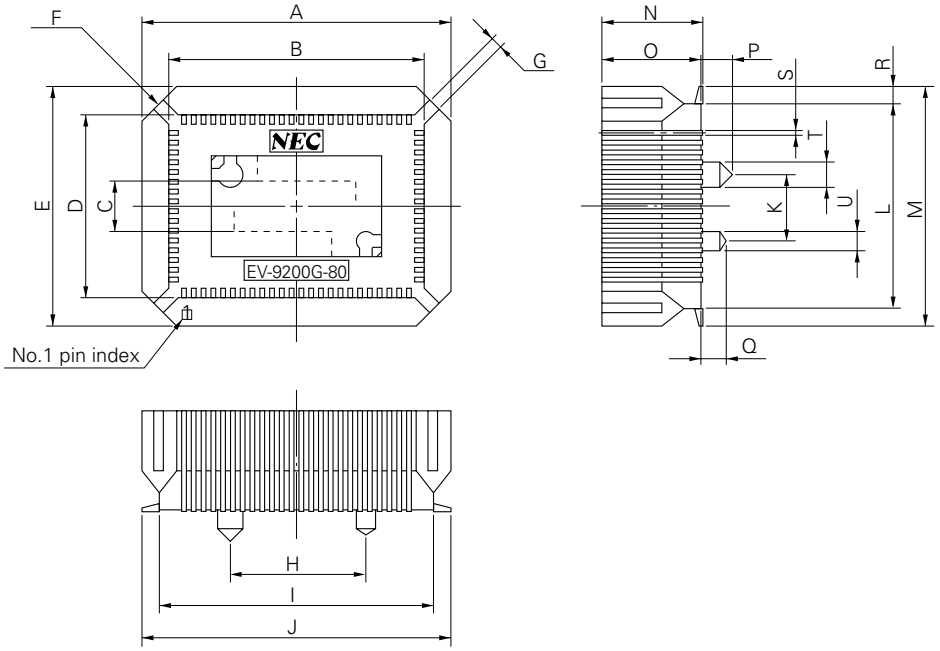
EV-9200G-74-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	1.0±0.02 × 18=18.0±0.05	$0.039^{+0.002}_{-0.001}\times 0.709=0.709^{+0.002}_{-0.003}$
D	1.0±0.02 × 18=18.0±0.05	$0.039^{+0.002}_{-0.001}\times 0.709=0.709^{+0.002}_{-0.003}$
E	21.0	0.827
F	25.7	1.012
G	11.00±0.08	$0.433^{+0.004}_{-0.003}$
H	5.00±0.08	$0.197^{+0.003}_{-0.004}$
I	0.6±0.02	$0.024^{+0.001}_{-0.002}$
J	ϕ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	ϕ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

(2) EV-9200G-80

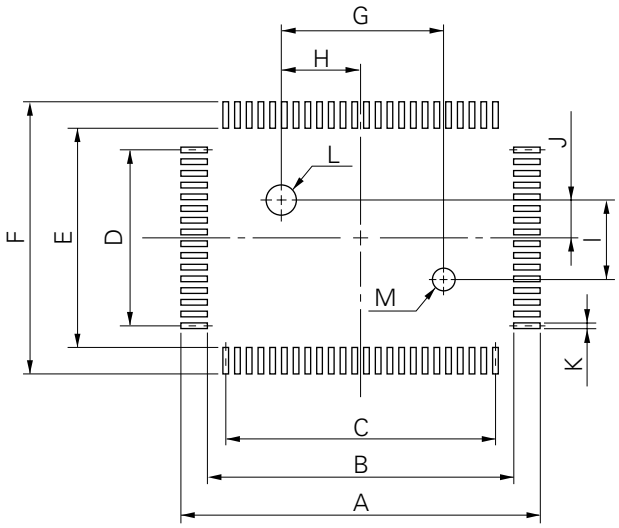
Figure A-3. Drawing of Conversion Socket (EV-9200G-80)
(For reference only)



EV-9200G-80-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.30	0.799
C	4.0	0.157
D	14.45	0.569
E	19.0	0.748
F	4-C 2.8	4-C 0.11
G	0.8	0.031
H	11.0	0.433
I	22.0	0.866
J	24.7	0.972
K	5.0	0.197
L	16.2	0.638
M	18.9	0.744
O	8.0	0.315
N	7.8	0.307
P	2.5	0.098
Q	2.0	0.079
R	1.35	0.053
S	0.35±0.1	$0.014^{+0.004}_{-0.005}$
T	φ2.3	φ0.091
U	φ1.5	φ0.059

Figure A-4. Recommended Footprint of Conversion Socket (EV-9200G-80) (For reference only)



EV-9200G-80-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	$0.8\pm0.02\times23=18.4\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.906=0.724^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
E	15.2	0.598
F	19.9	0.783
G	11.00 ± 0.08	$0.433^{+0.004}_{-0.003}$
H	5.50 ± 0.03	$0.217^{+0.001}_{-0.002}$
I	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
J	2.50 ± 0.03	$0.098^{+0.002}_{-0.001}$
K	0.5 ± 0.02	$0.02^{+0.001}_{-0.002}$
L	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
M	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

* APPENDIX B. TOOLS

B.1 Development Tools

The following development tools are readily available to support development of systems using the μPD78P322:

Language Processor

78K/III Series relocatable assembler (RA78K/III)	Relocatable assembler common to the 78K/III series. Since it contains the macro function, the development efficiency can be improved. A structured assembler which enables you to explicity describe program control structure is also attached and program productivity and maintenance can be improved.			
	Host machine			Ordering code
		OS	Supply medium	(product name)
	PC-9800 series	MS-DOS™	3.5-inch 2HD	μS5A13RA78K3
			5-inch 2HD	μS5A10RA78K3
	IBM PC/AT™ and compatible machine	PC DOS™	3.5-inch 2HC	μS7B13RA78K3
			5-inch 2HC	μS7B10RA78K3
	HP9000 series 700™	HP-UX™	DAT	μS3P16RA78K3
	SPARCstation™	SunOS™	Cartridge tape (QIC-24)	μS3K15RA78K3
	NEWS™	NEWS-OS™		μS3R15RA78K3
78K/III Series C compiler (CC78K/III)	C compiler common to the 78K/III series. This is a program to convert a program written in C language into an object code executable with a microcontroller. When using the compiler, 78K/III series relocatable assembler (RA78K/III) is necessary.			
	Host machine			Ordering code
		OS	Supply medium	(product name)
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13CC78K3
			5-inch 2HD	μS5A10CC78K3
	IBM PC/AT™ and compatible machine	PC DOS	3.5-inch 2HC	μS7B13CC78K3
			5-inch 2HC	μS7B10CC78K3
	HP9000 series 700	HP-UX	DAT	μS3P16CC78K3
	SPARCstation	SunOS	Cartridge tape (QIC-24)	μS3K15CC78K3
	NEWS	NEWS-OS		μS3R15CC78K3

Remark The operation of the relocatable assembler and C compiler is guaranteed only on the host machine under the operating systems listed above.

PROM Write Tools

Hard-ware	PG-1500	PG-1500 is a PROM programmer which enables you to program single chip micro-controllers containing PROM by stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500. It also enables you to program typical PROM devices of 256K bits to 4M bits.			
	UNISITE 2900	PROM programmer manufactured by Data I. O. Japan.			
	PA-78P322GF PA-78P322GJ PA-78P322K PA-78P322KC PA-78P322KD PA-78P322L	PROM programmer adapters to write programs onto the μPD78P322 on a general purpose PROM programmer such as PG-1500. PA-78P322GF ... μPD78P322GF PA-78P322GJ ... μPD78P322GJ PA-78P322K ... μPD78P322K PA-78P322KC ... μPD78P322KC PA-78P322KD ... μPD78P322KD PA-78P322L ... μPD78P322L			
Soft-ware	PG-1500 controller	Connects PG-1500 and a host machine by a serial or parallel interface and controlls PG-1500 on the host machine.			
		Host machine			Ordering code
			OS	Supply medium	(product name)
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13PG1500
				5-inch 2HD	μS5A10PG1500
		IBM PC/AT and compatible machine	PC DOS	3.5-inch 2HD	μS7B13PG1500
				5-inch 2HC	μS7B10PG1500

Remark The operation of the PG-1500 controller is guaranteed only on the host machine under the operating systems listed above.

Debugging Tools

Hard-ware	IE-78327-R IE-78320-R Note	IE-78327-R and IE-78320-R are in-circuit emulators that can be used for application system development and debugging. Connect a host machine for debugging. IE-78327-R can be used in common for the μPD78322 subseries and the μPD78328 subseries. IE-78320-R can be used for the μPD78322 subseries.			
	EP-78320GF-R EP-78320GJ-R EP-78320L-R	Emulation probe to connect IE-78327-R or IE-78320-R to the target system. EP-78320GF-R ..... 80-pin plastic QFP EP-78320GJ-R..... 74-pin plastic QFP EP-78320L-R ..... 68-pin plastic QFJ			
Soft-ware	IE-78327-R control program (IE controller)	Program to control IE-78327-R on a host machine. Automatic execution of commands, etc., is enabled for more efficient debugging.			
		Host machine			Ordering code
			OS	Supply medium	(product name)
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78327
				5-inch 2HD	μS5A10IE78327
		IBM PC/AT and compatible machine	PC DOS	3.5-inch 2HC	μS7B13IE78327
				5-inch 2HC	μS7B10IE78327
	IE-78320-R control program Note (IE controller)	Program to control IE-78320-R on a host machine. Automatic execution of commands, etc., is enabled for more efficient debugging.			
		Host machine			Ordering code
			OS	Supply medium	(product name)
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78320
				5-inch 2HD	μS5A10IE78320
		IBM PC/AT and compatible machine	PC DOS	5-inch 2HC	μS7B10IE78320

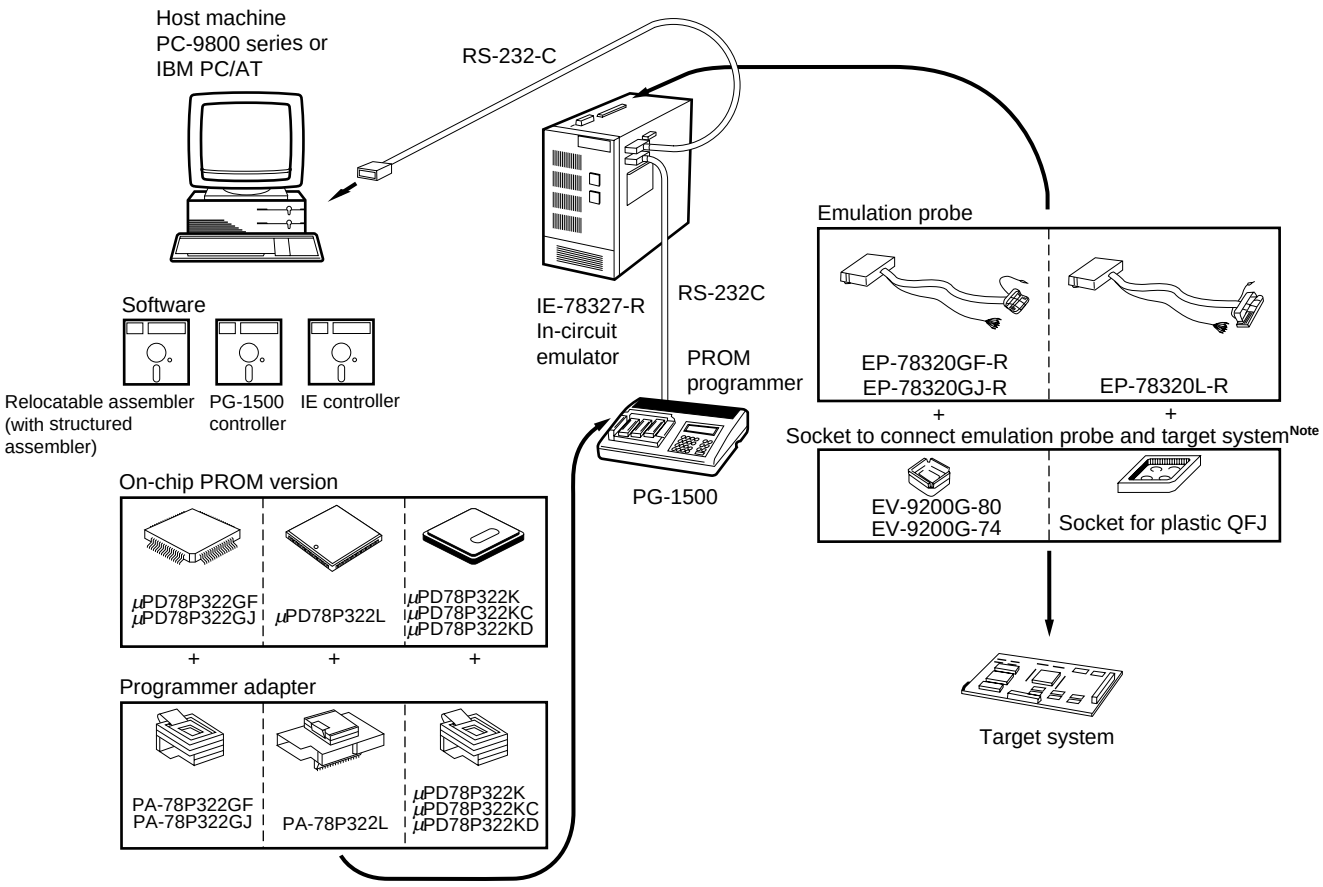
Remarks 1. The operation of the IE controller is guaranteed only on the host machine under the operating systems listed above.

2. μPD78322 subseries: μPD78320, 78322, 78P322, 78323, 78324, 78P324, 78320(A), 78320(A1), 78320(A2), 78322(A), 78322(A1), 78322(A2), 78323(A), 78323(A1), 78323(A2), 78324(A), 78324(A1), 78324(A2), 78P324(A), 78P324(A1), 78P324(A2)

μPD78328 subseries: μPD78327, 78328, 78P328, 78327(A), 78328(A)

Note Conventional IE-78320-R is a maintenance product. When purchasing a new incircuit emulator, use an alternative product IE-78327-R.

Phase-out/Discontinued



Note The socket is attached to the emulation probe.

Remarks The host machine and PG-1500 can be connected directly by RS-232-C.

B.2 Evaluation Tools

The following evaluation tools are provided to evaluate the μPD78P322 function:

Ordering Code (product name)	Host Machine	Function
EB-78320-98	PC-9800 series	The μPD78P322 function can be easily evaluated by connecting the evaluation tool to a host machine. The EB-78320-98/PC command system basically is compliant with the IE-78327-R or IE-78320-R command system. Thus, easy transition to application system development process by IE-78327-R or IE-78320-R can be made. The evaluation tools enable turbo access manager (μPD71P301)Note to be mounted on the printed circuit board.
EB-78320-PC	IBM PC/AT and compatible machine	

Note Turbo access manager (μPD71P301) is available for maintenance purpose only.

Cautions 1. EB-78320-98/PC is not the μPD78P322 application system development tool.

2. EB-78320-98/PC does not contain the emulation function at internal PROM execution of the μPD78P322.

B.3 Embedded Software

The following embedded software products are readily available to support more efficient program development and maintenance:

Real-time OS

Real-time OS (RX78K/III)	The purpose of RX78K/III is to realize a multi-task environment in a control area which requires real-time processing. RX78K/III allocates idle times of CPU to other processing to improve overall performance of the system. RX78K/III provides a system call based on the μITRON specification. RX78K/III assembler package provides the RX78K/III nucleus and a tool (configurator) to prepare multiple information tables.			
	Host machine			Ordering code (product name)
		OS	Supply medium	
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13RX78320
			5-inch 2HD	μS5A10RX78320
	IBM PC/AT and compatible machine	PC DOS	3.5-inch 2HC	μS7B13RX78320
			5-inch 2HC	μS7B10RX78320

Caution When purchasing the RX78K/III, fill in the purchase application form in advance, and sign the User's Agreement.

Remark When using the RX78K/III Real-time OS, the RA78K/III assembler package (option) is necessary.

Fuzzy Inference Development Support System

Fuzzy Knowledge Data Preparation Tool (FE9000, FE9200)	Program supporting input of fuzzy knowledge data (fuzzy rule and membership function), input/editing (edit), and evaluation (simulation).				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FE9000
				5-inch 2HD	μS5A10FE9000
	IBM PC/AT and compatible machine	PC DOS	Windows™	3.5-inch 2HC	μS7B13FE9200
				5-inch 2HC	μS7B10FE9200
Translator (FT78K3)Note	Program converting fuzzy knowledge data obtained by using fuzzy knowledge data preparation tool to the assembler source program for the RA78K/III.				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FT78K3
				5-inch 2HD	μS5A10FT78K3
	IBM PC/AT and compatible machine	PC DOS		3.5-inch 2HC	μS7B13FT78K3
				5-inch 2HC	μS7B10FT78K3
Fuzzy Inference Module (FI78K/III)Note	Program executing fuzzy inference. Fuzzy inference is executed by linking fuzzy knowledge data converted by translator.				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FI78K3
				5-inch 2HD	μS5A10FI78K3
	IBM PC/AT and compatible machine	PC DOS		3.5-inch 2HC	μS7B13FI78K3
				5-inch 2HC	μS7B10FI78K3
Fuzzy Inference Debugger (FD78K/III)	Support software evaluating and adjusting fuzzy knowledge data at hardware level by using in-circuit emulator.				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FD78K3
				5-inch 2HD	μS5A10FD78K3
	IBM PC/AT and compatible machine	PC DOS		3.5-inch 2HC	μS7B13FD78K3
				5-inch 2HC	μS7B10FD78K3

Note Under development

[MEMO]

Phase-out/Discontinued

NOTES FOR CMOS DEVICES

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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License not needed: μPD78P322K, 78P322KC, 78P322KD
The customer must judge the need for license: μPD78P322GF-3B9, 78P322GJ-5BJ, 78P322L