

To our customers,

---

## Old Company Name in Catalogs and Other Documents

---

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

## Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
  - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
  - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
  - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

## 8-BIT SINGLE-CHIP MICROCOMPUTER

### DESCRIPTION

The μPD78P214 is an 8-bit single-chip microcomputer with the on-chip mask ROM of the μPD78214 replaced with an EPROM or one-time PROM. Since the μPD78P214 is a user-programmable microcomputer, it is suitable for system development evaluation and small production.

Use this manual together with μPD78214 manuals.

Furthermore, for details of the internal functions, be sure to see the separate "78K/II Series User's Manual Instruction Volume" and "μPD78214 Series User's Manual Hardware Volume"

In this document, "PROM" is used in parts common to one-time PROM products and EPROM products.

### FEATURES

- μPD78214 compatible
- On-chip EPROM
  - μPD78P214DW : Reprogrammable (suitable for system development)
  - μPD78P214CW/GC/GJ/GQ/L : One-time programmable (suitable for small production)
- QTOP™ microcomputer compatibility

**Remarks** "QTOP microcomputer" is the generic name for NEC single-chip microcomputers with on-chip one-time PROM which are totally supported from program writing through printing, screening and verification.

### ORDERING INFORMATION

| Ordering Code   | Package  | On-chip ROM   |
|-----------------|--|---------------|
| μPD78P214CW     | 64-pin plastic shrink DIP (750 mil)                          | one-time PROM |
| μPD78P214GC-AB8 | 64-pin plastic QFP (□ 14 mm)                                 | one-time PROM |
| μPD78P214GJ-5BJ | 74-pin plastic QFP (□ 20 mm)                                 | one-time PROM |
| μPD78P214GQ-36  | 64-pin plastic QUIP  | one-time PROM |
| μPD78P214L      | 64-pin plastic QFJ (□ 950 mil)                               | one-time PROM |
| μPD78P214DW     | 64-pin ceramic shrink DIP (CERDIP)<br>(with window) (750mil) | EPROM         |

### QUALITY GRADE

Standard

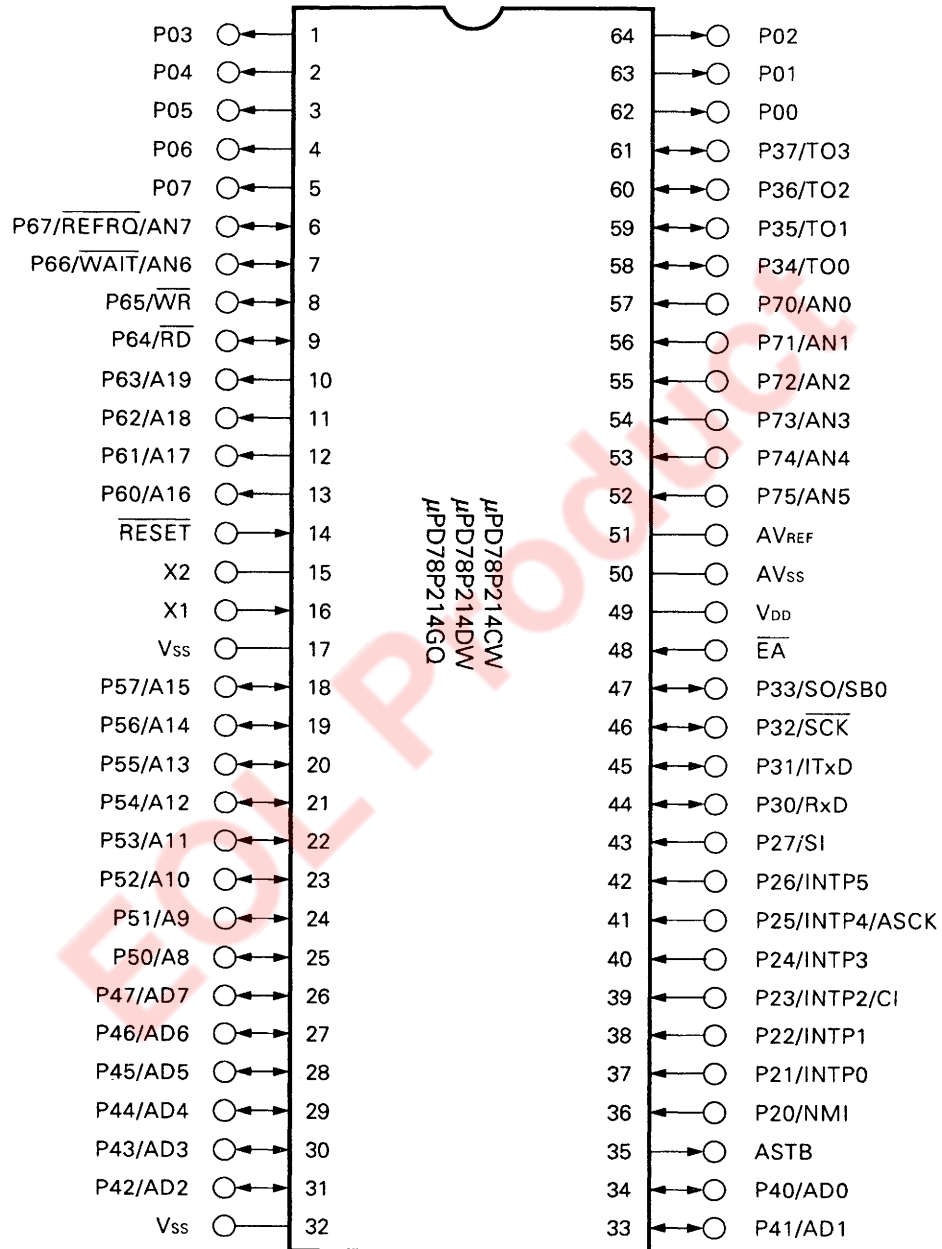
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change with- out notice.

**PIN CONFIGURATION (TOP VIEW)**

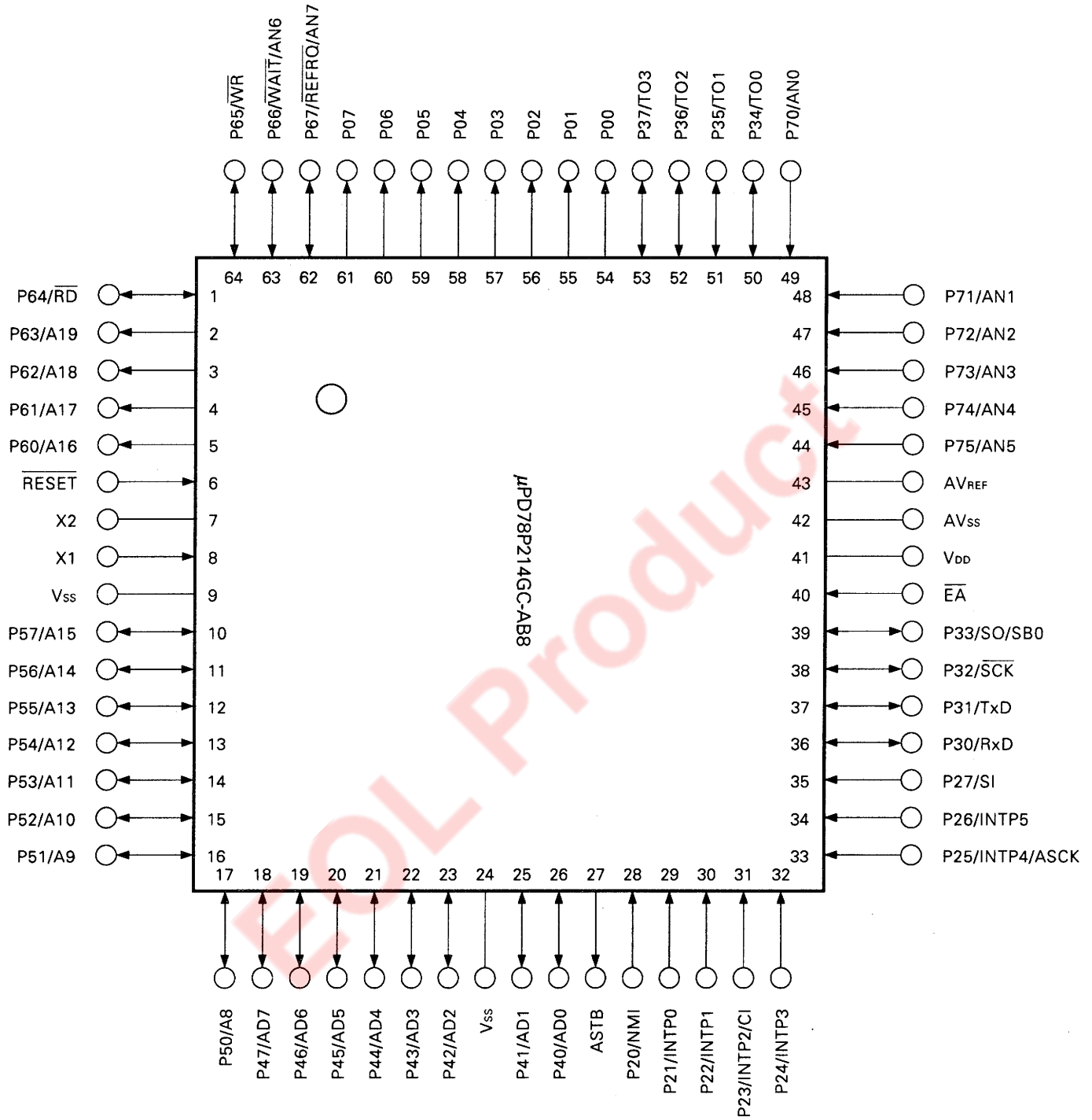
**(1) Normal Operating Mode**

**(a) 64-pin plastic shrink DIP, 64-pin plastic QUIP,  
and 64-pin ceramic shrink DIP (CERDIP) (with window)**

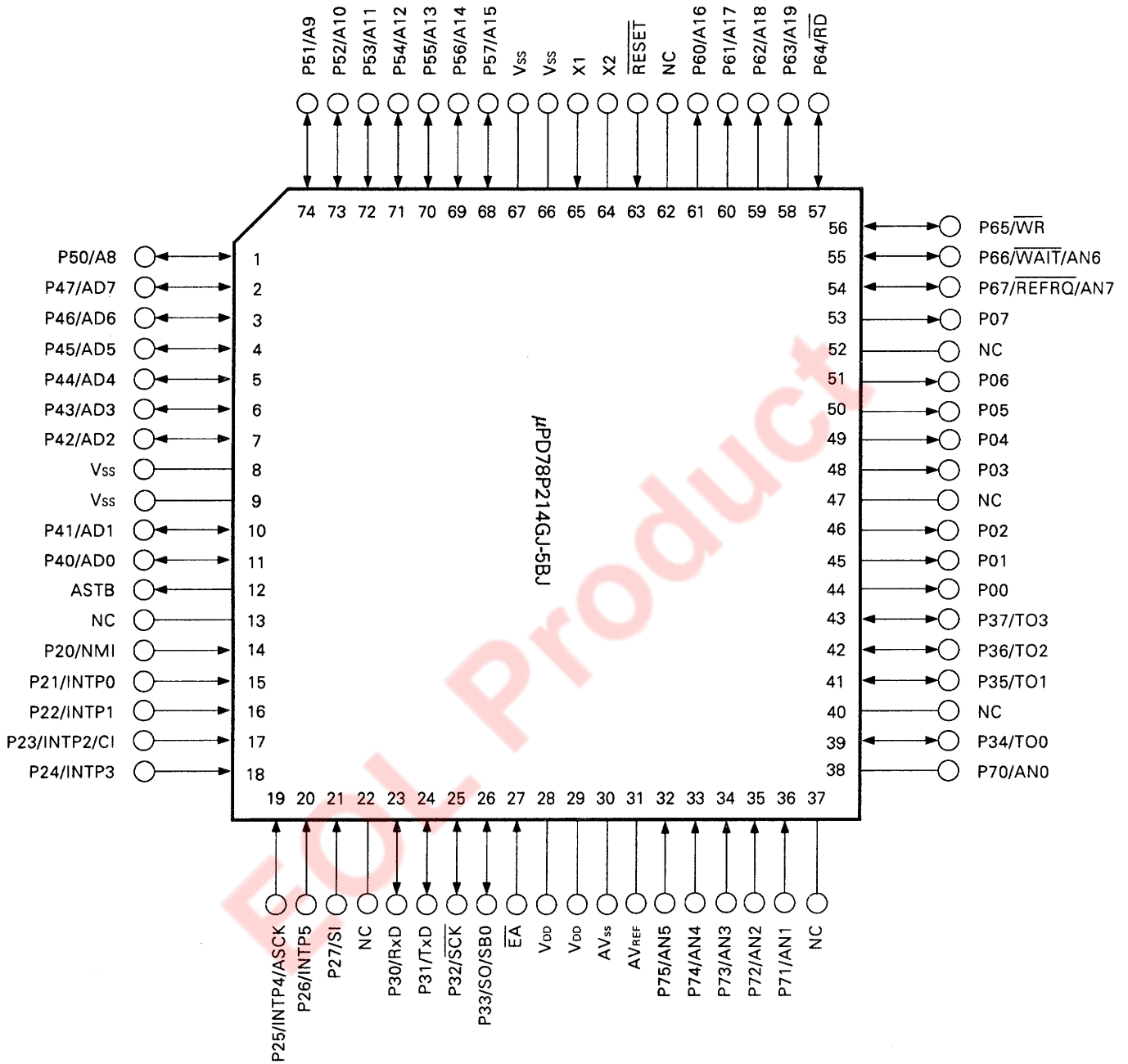


**Remarks** Pin compatible with μPD78210CW/GQ.

(b) 64-pin plastic QFP

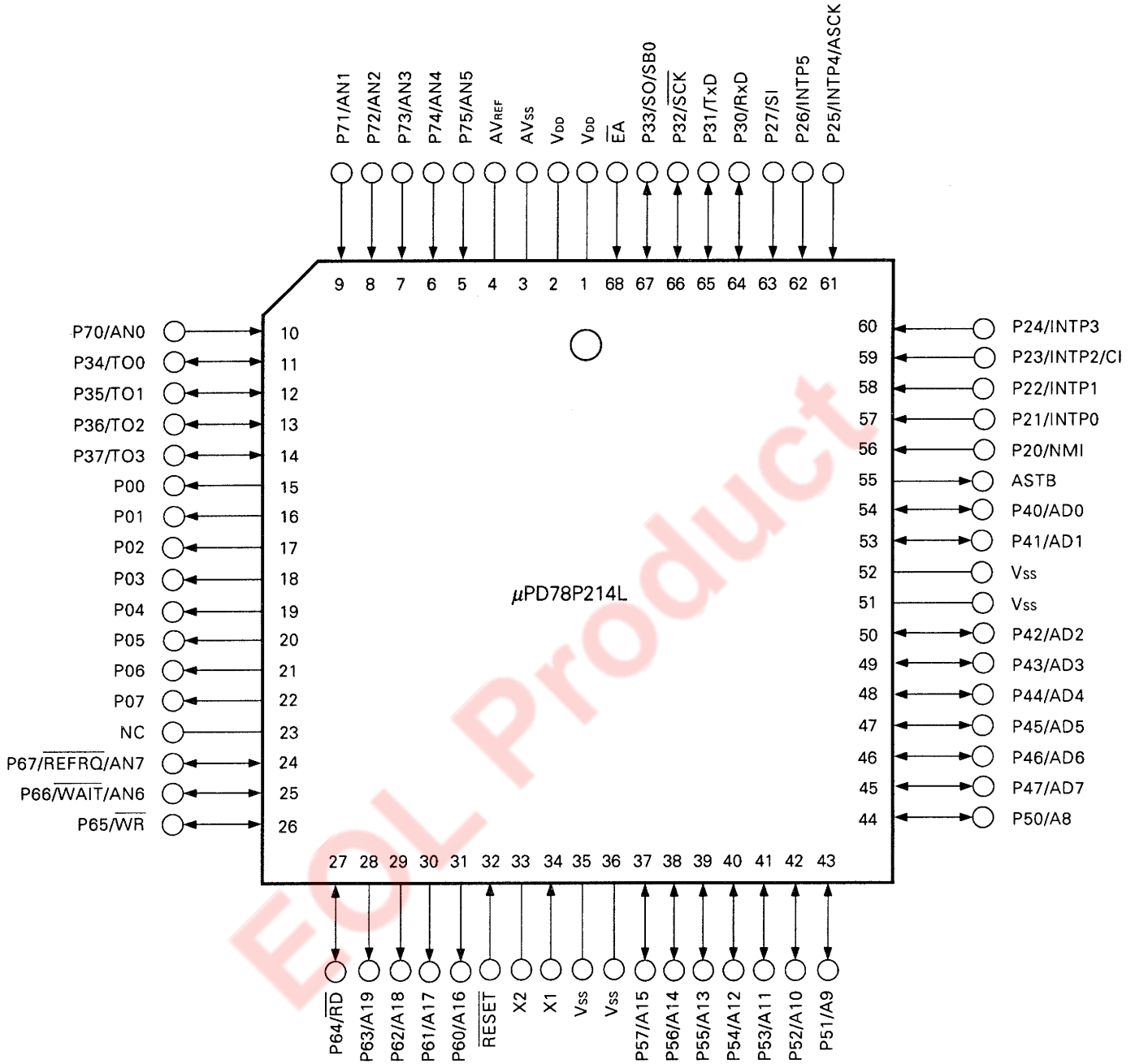


(c) 74-pin plastic QFP



- Remarks**
1. Pin compatible with μPD78210GJ.
  2. NC : not connected internally.

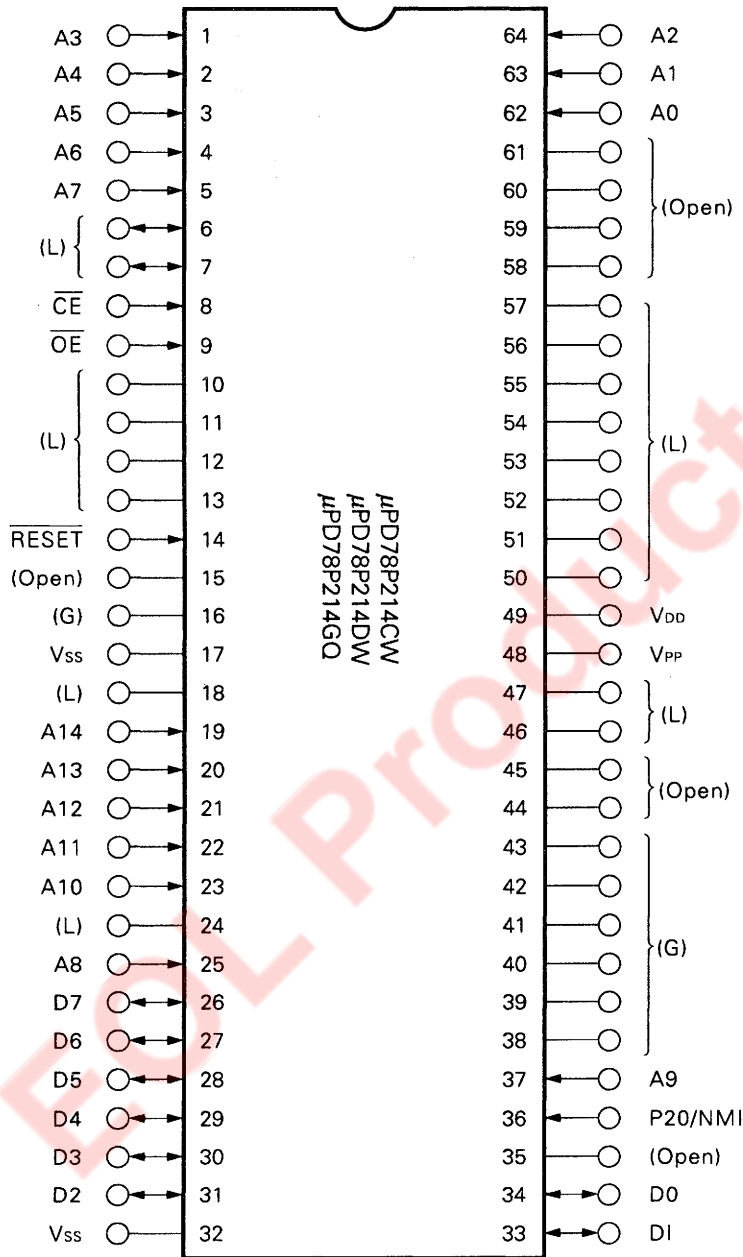
(d) 68-pin plastic QFJ



- Remarks**
1. Pin compatible with μPD78210L.
  2. NC : not connected internally.

(2) PROM Programming Mode (P20/NMI = 12.5 V,  $\overline{\text{RESET}} = \text{L}$ )

(a) 64-pin plastic shrink DIP, 64-pin plastic QUIP, and 64-pin ceramic shrink DIP (CERDIP) (with window)



**Note** Processing for pins which are not used in the PROM programming mode is indicated in parentheses.

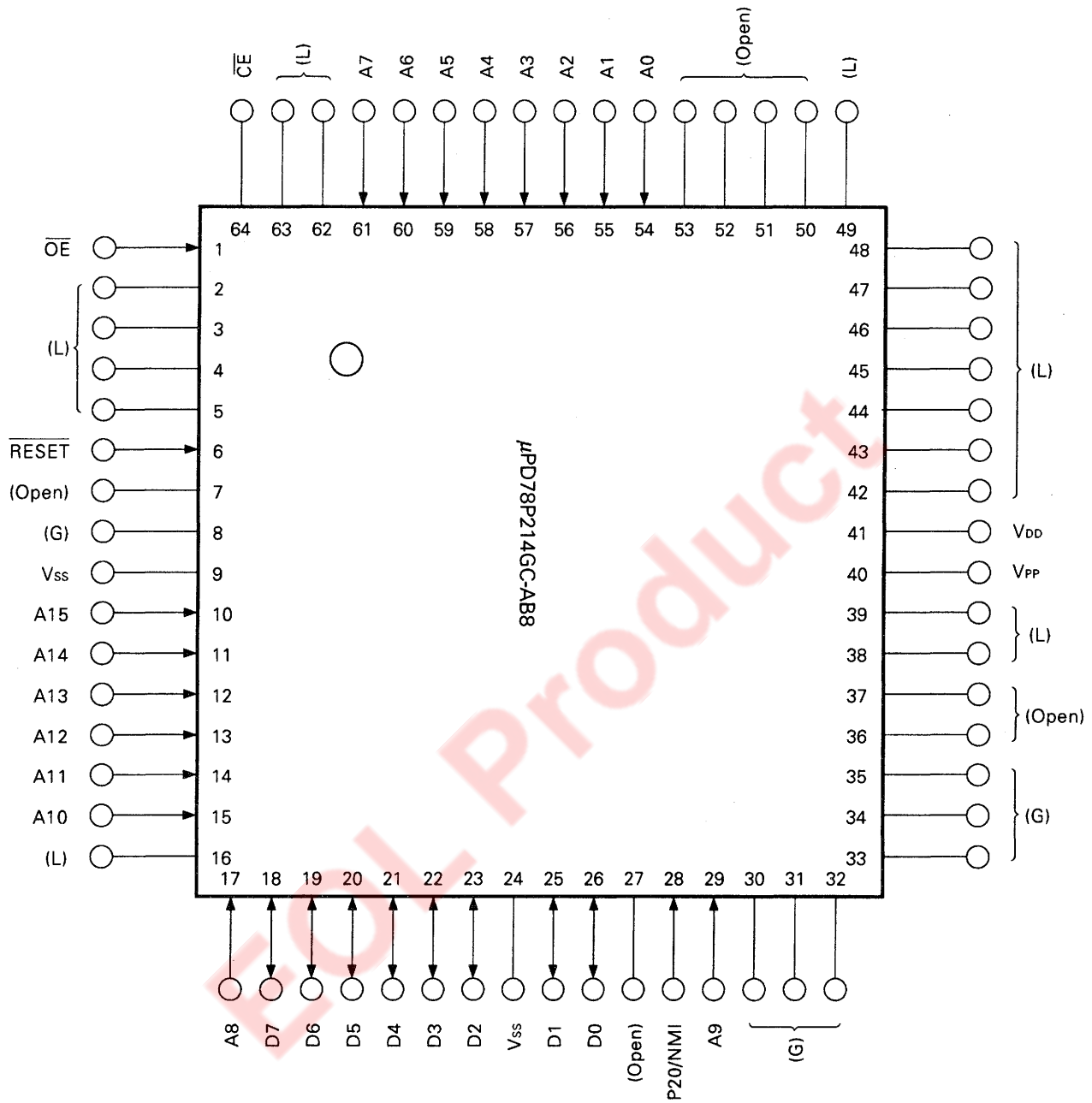
**L** : Connect these pins independently to VSS via a resistor.

**G** : Connect these pins to VSS.

**Open** : No connection required.

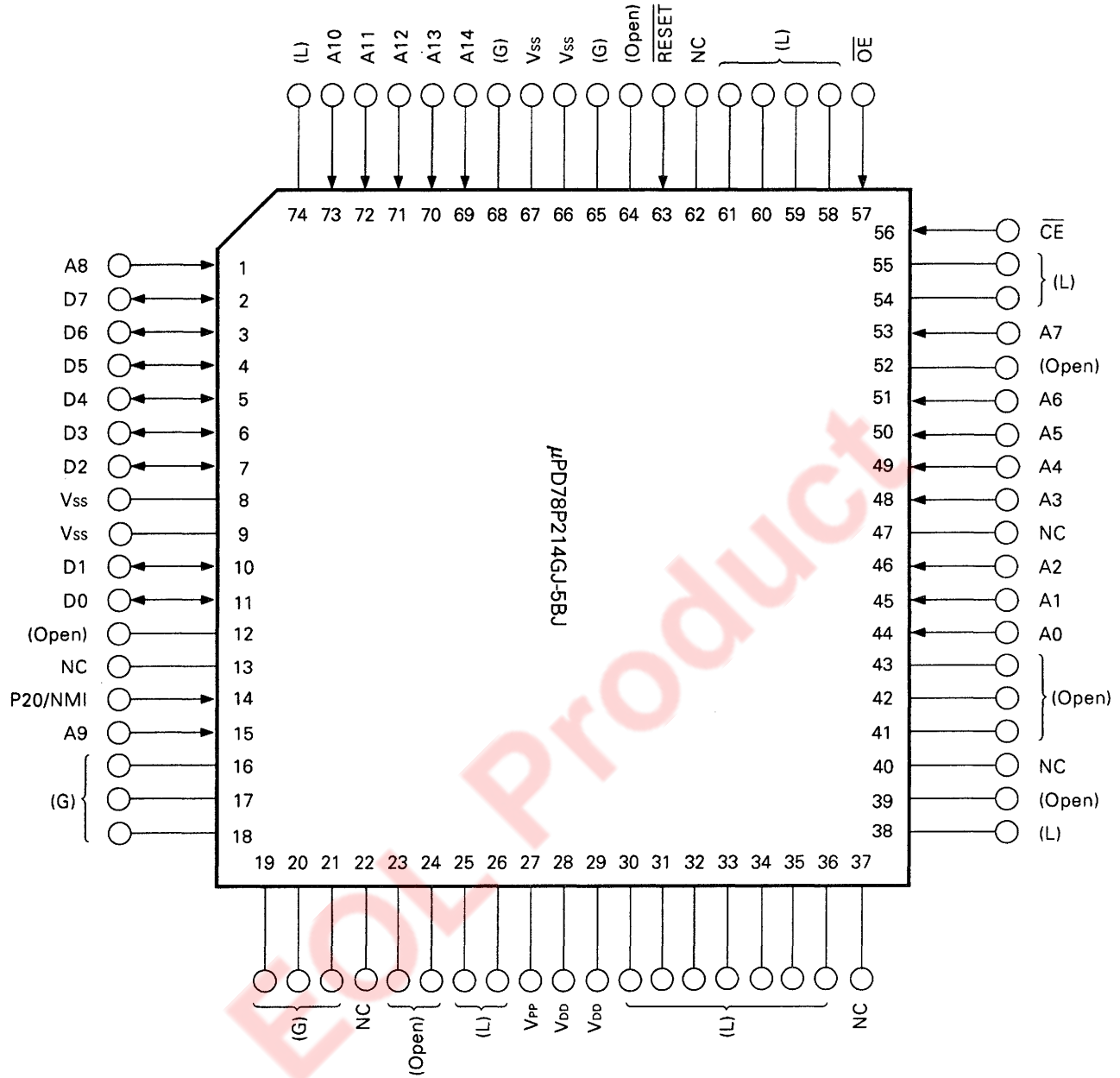


(b) 64-pin plastic QFP



**Note** Processing for pins which are not used in the PROM programming mode is indicated in parentheses.  
**L** : Connect these pins independently to V<sub>ss</sub> via a resistor.  
**G** : Connect these pins to V<sub>ss</sub>.  
**Open** : No connection required.

(c) 74-pin plastic QFP



**Note** Processing for pins which are not used in the PROM programming mode is indicated in parentheses.

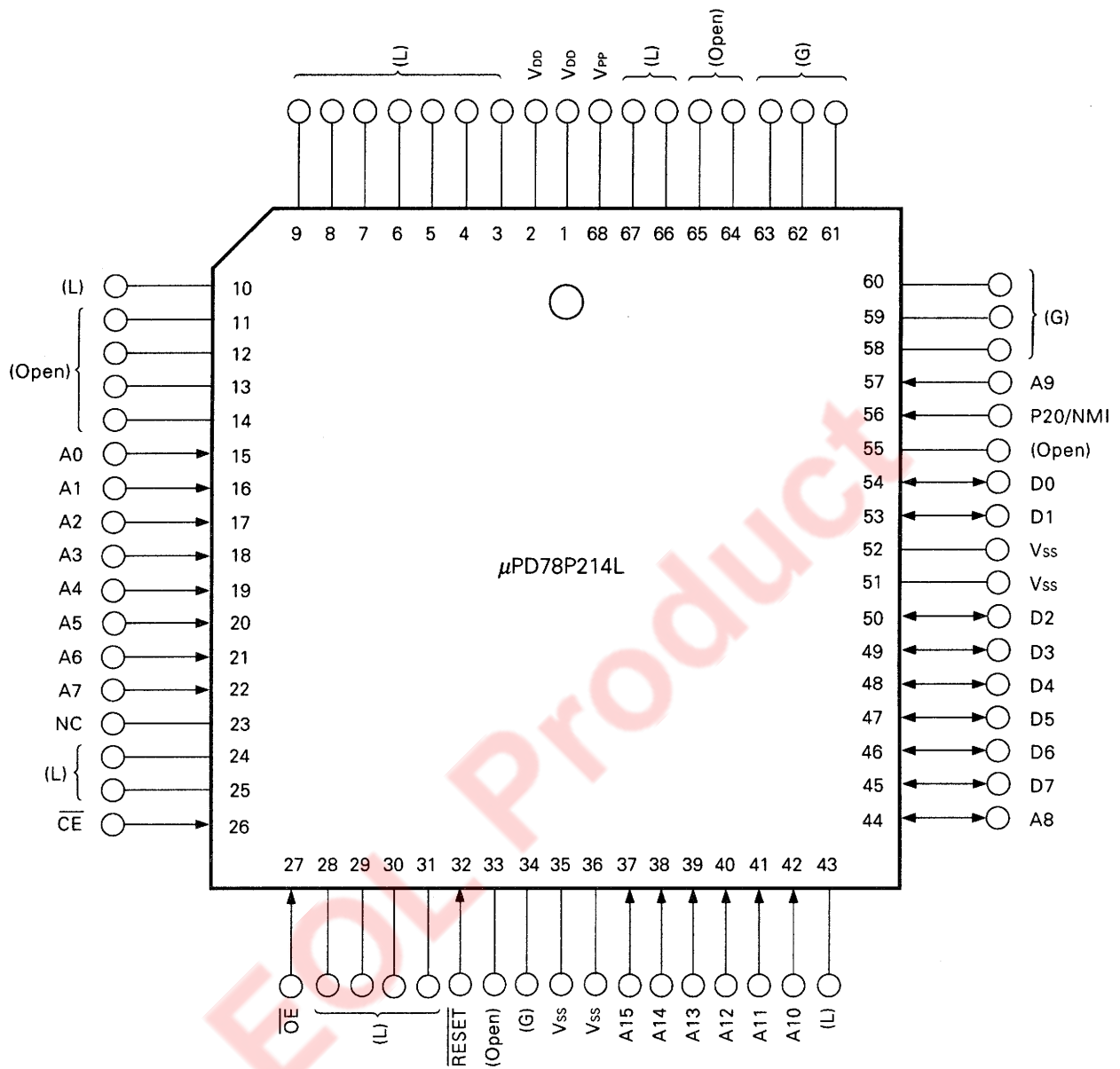
**L** : Connect these pins independently to V<sub>ss</sub> via a resistor.

**G** : Connect these pins to V<sub>ss</sub>.

**Open** : No connection required.

**Remarks** NC : not connected internally.

(d) 68-pin plastic QFJ



**Note** Processing for pins which are not used in the PROM programming mode is indicated in parentheses.

**L** : Connect these pins independently to V<sub>ss</sub> via a resistor.

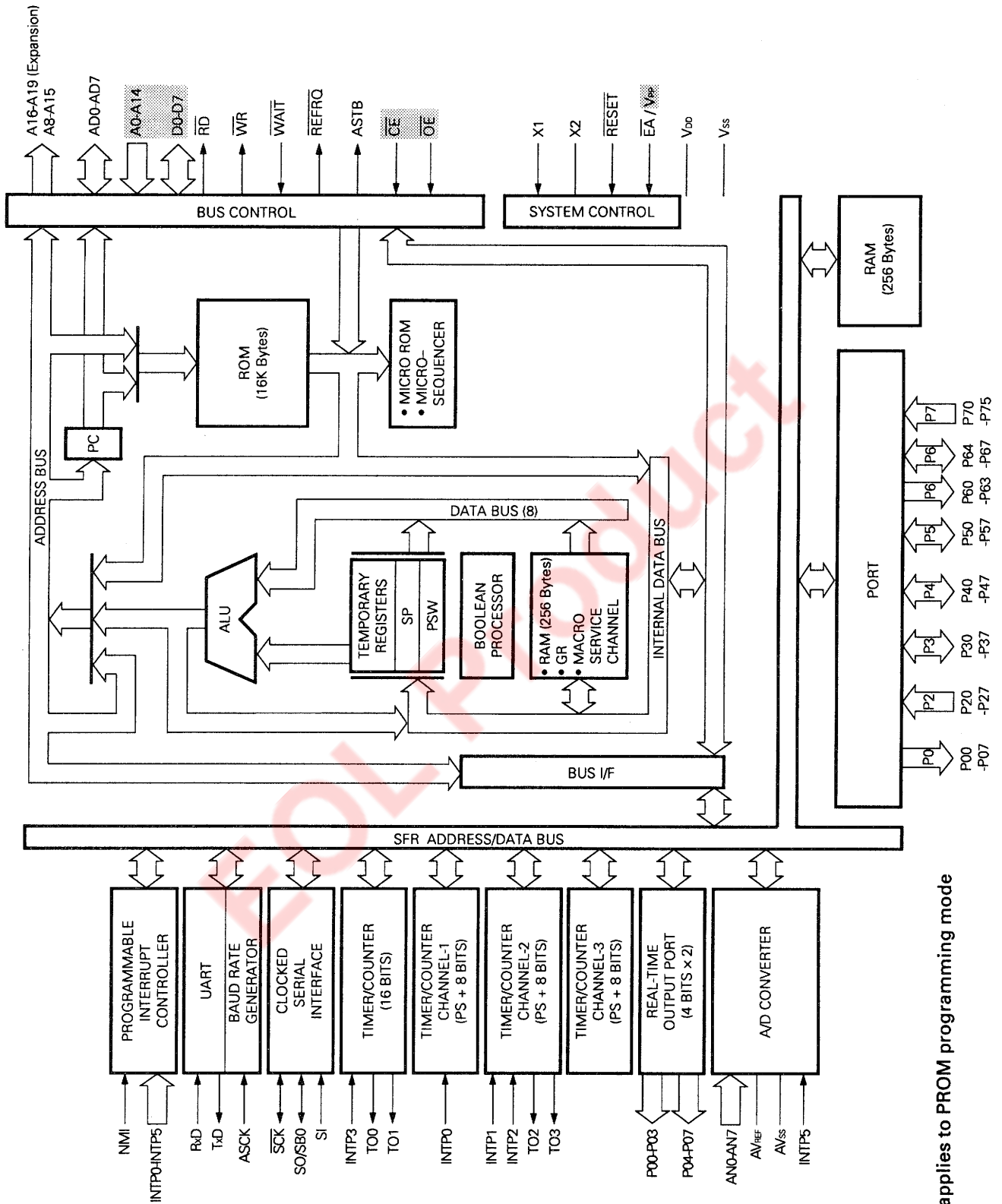
**G** : Connect these pins to V<sub>ss</sub>.

**Open** : No connection required.

**Remarks** NC : not connected internally.

|                         |   |                            |                           |   |                          |
|-------------------------|---|----------------------------|---------------------------|---|--------------------------|
| P00 to P07              | : | Port 0                     | $\overline{\text{RD}}$    | : | Read Strobe              |
| P20 to P27              | : | Port 2                     | $\overline{\text{WR}}$    | : | Write Strobe             |
| P30 to P37              | : | Port 3                     | $\overline{\text{WAIT}}$  | : | Wait                     |
| P40 to P47              | : | Port 4                     | $\overline{\text{ASTB}}$  | : | Address Strobe           |
| P50 to P57              | : | Port 5                     | $\overline{\text{REFRQ}}$ | : | Refresh Request          |
| P60 to P67              | : | Port 6                     | $\overline{\text{RESET}}$ | : | Reset                    |
| P70 to P75              | : | Port 7                     | X1, X2                    | : | Crystal                  |
| TO0 to TO3              | : | Timer Output               | $\overline{\text{EA}}$    | : | External Access          |
| Cl                      | : | Clock Input                | AN0 to AN7                | : | Analog Input             |
| RxD                     | : | Receive Data               | AV <sub>REF</sub>         | : | Reference Voltage        |
| TxD                     | : | Transmit Data              | AV <sub>SS</sub>          | : | Analog Ground            |
| $\overline{\text{SCK}}$ | : | Serial Clock               | V <sub>DD</sub>           | : | Power Supply             |
| ASCK                    | : | Asynchronous Serial Clock  | V <sub>SS</sub>           | : | Ground                   |
| SB0                     | : | Serial Bus                 | NC                        | : | Non-Connection           |
| SI                      | : | Serial Input               | $\overline{\text{CE}}$    | : | Chip Enable              |
| SO                      | : | Serial Output              | $\overline{\text{OE}}$    | : | Output Enable            |
| NMI                     | : | Non-Maskable Interrupt     | V <sub>PP</sub>           | : | Programming Power Supply |
| INTP0 to INTP5          | : | Interrupt From Peripherals |                           |   |                          |
| AD0 to AD7              | : | Address/Data Bus           |                           |   |                          |
| A8 to A19               | : | Address Bus                |                           |   |                          |

INTERNAL BLOCK DIAGRAM



Shading applies to PROM programming mode

**CONTENTS**

**1. PIN FUNCTIONS ..... 13**

**1.1 NORMAL OPERATING MODE ..... 13**

**1.2 PROM PROGRAMMING MODE ..... 15**

**2. DIFFERENCES BETWEEN μPD78P214 AND μPD78214 ..... 16**

**3. PROGRAMMING ..... 17**

**3.1 OPERATING MODE ..... 17**

**3.2 PROM WRITE PROCEDURE ..... 18**

**3.3 PROM READ PROCEDURE ..... 20**

**4. ERASE CHARACTERISTICS (μPD78P214DW ONLY) ..... 21**

**5. ERASE WINDOW SEALING (μPD78P214DW ONLY) ..... 21**

**6. SCREENING OF ONE-TIME PROM PRODUCTS ..... 21**

**7. ELECTRICAL SPECIFICATIONS ..... 22**

**8. PACKAGE INFORMATION ..... 42**

**9. RECOMMENDED SOLDERING CONDITIONS ..... 47**

**APPENDIX. DEVELOPMENT TOOLS ..... 49**

EOL Product

1. PIN FUNCTIONS

1.1 NORMAL OPERATING MODE

(1) Ports

| Pin Name   | Input/Output | Dual Function Pin      | Function  |
|------------|--------------|------------------------|---|
| P00 to P07 | Output       | —                      | Port 0 (P0):<br>Use enabled as a real-time output port (4 bits × 2).<br>Transistor direct drive capability.   |
| P20        | Input        | NMI                    | Port 2 (P2):<br>P20 is abled for use as a general-purpose port (non-maskable interrupt).<br>However, input level can be checked in the interrupt routine.<br>P22 to P27 are specifiable for on-chip resistor connection in 6-bit batch by software. |
| P21        |              | INTP0                  |   |
| P22        |              | INTP1                  |   |
| P23        |              | INTP2/CI               |   |
| P24        |              | INTP3                  |   |
| P25        |              | INTP/ASCK              |   |
| P26        |              | INTP5                  |   |
| P27        |              | SI                     |   |
| P30        | Input/output | RxD                    | Port 3 (P3):<br>Input/output specifiable as a bit-wise.<br>Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software.  |
| P31        |              | TxD                    |   |
| P32        |              | $\overline{SCK}$       |   |
| P33        |              | SO/SB0                 |   |
| P34 to P37 |              | TO0 to TO3             |   |
| P40 to P47 | Input/output | AD0 to AD7             | Port 4 (P4):<br>Input/output specifiable for eight bits at one time.<br>Specifiable for on-chip pull-up resistor connection in 8-bit batch by software.   |
| P50 to P57 | Input/output | A8 to A15              | Port 5 (P5):<br>Input/output specifiable as a bit-wise.<br>Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software.<br>LED direct drive capability.  |
| P60 to P63 | Output       | A16 to A19             | Port 6 (P6):<br>Input/output specifiable as a bit-wise for P64 to P67.<br>The connection of the on-chip pull-up resistor can be specified as a batch for input mode pins P64 to P67 in a software.  |
| P64        | Input/output | $\overline{RD}$        |   |
| P65        |              | $\overline{WR}$        |   |
| P66        |              | $\overline{WAIT}/AN6$  |   |
| P67        |              | $\overline{REFRQ}/AN7$ |   |
| P70 to P75 | Input        | AN0 to AN5             | Port 7 (P7)   |

(2) Other than ports

| Pin Name                  | Input/Output | Function  | Dual Function Pin   |
|---------------------------|--------------|---|---|
| T00 to T03                | Output       | Timer output  | P34 to P37  |
| CI                        | Input        | Count clock input to 8-bit timer/counter 2  | P23/INTP2   |
| RxD                       | Input        | Serial data input (UART)  | P30   |
| TxD                       | Output       | Serial data output (UART)   | P31   |
| ASCK                      | Input        | Baud rate clock input (UART)  | P25/INTP4   |
| SB0                       | Input/output | Serial data input/output (SBI)  | P33/SO  |
| SI                        | Input        | Serial data input (3-wire serial I/O)   | P27   |
| SO                        | Output       | Serial data output (3-wire serial I/O)  | P33/SB0   |
| $\overline{\text{SLK}}$   | Input/output | Serial clock input/output (SBI, 3-wire serial I/O)  | P32   |
| NMI                       | Input        | External interrupt request  | P20   |
| INTP0                     |              |   | P21   |
| INTP1                     |              |   | P22   |
| INTP2                     |              |   | P23/CI  |
| INTP3                     |              |   | P24   |
| INTP4                     |              |   | P25/ASCK  |
| INTP5                     |              |   | P26   |
| AD0 to AD7                | Input/output | Time-multiplexing address/data bus (external memory connection)                           | P40 to P47  |
| A8 to A15                 | Output       | Higher address bus (external memory connection)   | P50 to P57  |
| A16 to A19                | Output       | Expanded higher address (external memory connection)                                      | P60 to P63  |
| $\overline{\text{RD}}$    | Output       | Read strobe for external memory   | P64   |
| $\overline{\text{WR}}$    | Output       | Write strobe for external memory  | P65   |
| $\overline{\text{WAIT}}$  | Input        | Wait insert   | P66/AN6   |
| ASTB                      | Output       | Latch timing output of time-multiplexing addresses (A0 to A7) (in external memory access) | —   |
| $\overline{\text{REFRQ}}$ | Output       | Refresh pulse output to external pseudo static memory                                     | P67/AN7   |
| $\overline{\text{RESET}}$ | Input        | Chip reset  | —   |
| X1                        | Input        | Crystal connection for system clock oscillation (clock to X1 enabled)                     | —   |
| X2                        | —            |   |   |
| $\overline{\text{EA}}$    | Input        | ROM-less operation specification (external access in the same space as internal ROM)      | —   |
| AN0 to AN5                | Input        | Analog voltage input for A/D converter  | P70 to P75  |
| AN6, AN7                  |              |   | P66/ $\overline{\text{WAIT}}$ ,<br>P67/ $\overline{\text{REFRQ}}$ |
| AV <sub>REF</sub>         | —            | Reference voltage application for A/D converter   | —   |
| AV <sub>SS</sub>          |              | GND for A/D converter   |   |
| V <sub>DD</sub>           |              | Positive power supply   |   |
| V <sub>SS</sub>           |              | GND   |   |
| NC                        |              | —   |   |



1.2 PROM PROGRAMMING MODE (P20/NMI = +12.5 V,  $\overline{\text{RESET}}$  = L)

| Pin Name                  | Input/Output | Function                  |
|---------------------------|--------------|---------------------------|
| P20/NMI                   | Input        | PROM programming mode set |
| $\overline{\text{RESET}}$ |              |                           |
| A0 to A14                 |              |                           |
| D0 to D7                  | Input/output | Data bus                  |
| $\overline{\text{CE}}$    | Input        | PROM enable input         |
| $\overline{\text{OE}}$    |              | Read strobe for PROM      |
| V <sub>PP</sub>           | —            | Write power supply        |
| V <sub>DD</sub>           |              | Positive power supply     |
| V <sub>SS</sub>           |              | GND                       |
| NC                        |              | —                         |

EOL Product

**2. DIFFERENCES BETWEEN μPD78P214 AND μPD78214**

Since the μPD78P214 is a product with the μPD78214 on-chip mask ROM replaced with a rewritable EPROM, functions other than those related to EPROM, such as write/verify, are the same as those of the μPD78214. Table 2-1 shows the differences between μPD78P214 and μPD78214.

For details regarding the CPU functions and on-chip hardware, refer to the μPD78214 Series User's Manual and relevant manuals.

**Table 2-1 Differences between μPD78P214 and μPD78214**

| Item                   | μPD78P214  | μPD78214 |
|------------------------|--|----------|
| On-chip program memory | EPROM  | Mask ROM |
| EPROM programming pin  | Yes  | No       |
| Package                | <ul style="list-style-type: none"> <li>• 64-pin plastic shrink DIP</li> <li>• 64-pin plastic QUIP</li> <li>• 64-pin plastic QFJ</li> <li>• 64-pin plastic QFP</li> <li>• 74-pin plastic QFP</li> </ul> |          |
|                        | • 64-pin ceramic shrink DIP (with window)*   | —        |

\* Reprogrammable.

### 3. PROGRAMMING

The on-chip program memory of the μPD78P214 is a 16384 × 8-bit electrically programmable PROM. For PROM programming, the PROM programming mode is set using the NMI and  $\overline{\text{RESET}}$  pins.

The programming characteristics are compatible with the μPD27C256A\*. However, no write is performed to addresses 4000H to 7FFFH. In a data read or verify operation, FFH is read from addresses 4000H to 7FFFH. ★

\* Not applicable to a mode with a program pulse of 100μs.

**Note** In PROM programming, the address range of 000H to 3FFFH should be programmed. For a programmer with which address specification is impossible, be sure to write FFH to address 4000H. If data guaranteed for the μPD78P214.

The use of address 4000H is reserved by NEC for the future function expansion.

#### 3.1 OPERATING MODE

When +6 V and +12.5 V are applied to V<sub>DD</sub> pin and V<sub>PP</sub> pin, respectively, the μPD78P214 is set to the program-write/ verify mode. This mode can be reset to the operating mode described in Table 3-1 by setting  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  pins.

In the read mode, the μPD78P214 can read the PROM contents.

Table 3-1 PROM Programming Operating Mode

| Mode \ Pin      | NMI     | $\overline{\text{RESET}}$ | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | V <sub>PP</sub> | V <sub>DD</sub> | D0 to D7       |
|-----------------|---------|---------------------------|------------------------|------------------------|-----------------|-----------------|----------------|
| Program write   | +12.5 V | L                         | L                      | H                      | +12.5 V         | +6 V            | Data input     |
| Program verify  |         |                           | H                      | L                      |                 |                 | Data output    |
| Program inhibit |         |                           | H                      | H                      |                 |                 | High impedance |
| Read            |         |                           | L                      | L                      | +5 V            | +5 V            | Data output    |
| Output disable  |         |                           | L                      | H                      |                 |                 | High impedance |
| Standby         |         |                           | H                      | L/H                    |                 |                 | High impedance |

**Note** When V<sub>PP</sub> is set to +12.5 V and V<sub>DD</sub> is set to +6 V, it is inhibited to set both  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  to L.

**3.2 PROM WRITE PROCEDURE**

PROM write can be executed at high speeds using the following procedure:

- (1) Fix the  $\overline{\text{RESET}}$  pin to the low level. Apply +12.5 V to the NMI pin. Treat all other unused pins as shown in the pin configuration.
- (2) Apply +6 V to the  $V_{DD}$  pin and +12.5 V to the  $V_{PP}$  pin.
- (3) Supply the initial address.
- (4) Supply write data.
- (5) Supply a 1 ms program pulse (active low) to the  $\overline{\text{CE}}$  pin.
- (6) Set the verify mode. If data has been written, procedure to step (8). If data has not been written, repeat steps (4) to (6). If data cannot yet be written after repeating the three steps 25 times, proceed to step (7).
- (7) Stop carrying out the write operation assuming that the device is defective.
- (8) Supply write data and then supply (number of repetitions of steps (4) to (6): X) × 3 ms program pulses (additional write).
- (9) Increment the address.
- (10) Repeat steps (4) to (9) up to the final address.

The timings in steps (2) to (8) are shown in Fig. 3-1.

**Fig. 3-1 PROM Write/Verify Timings**

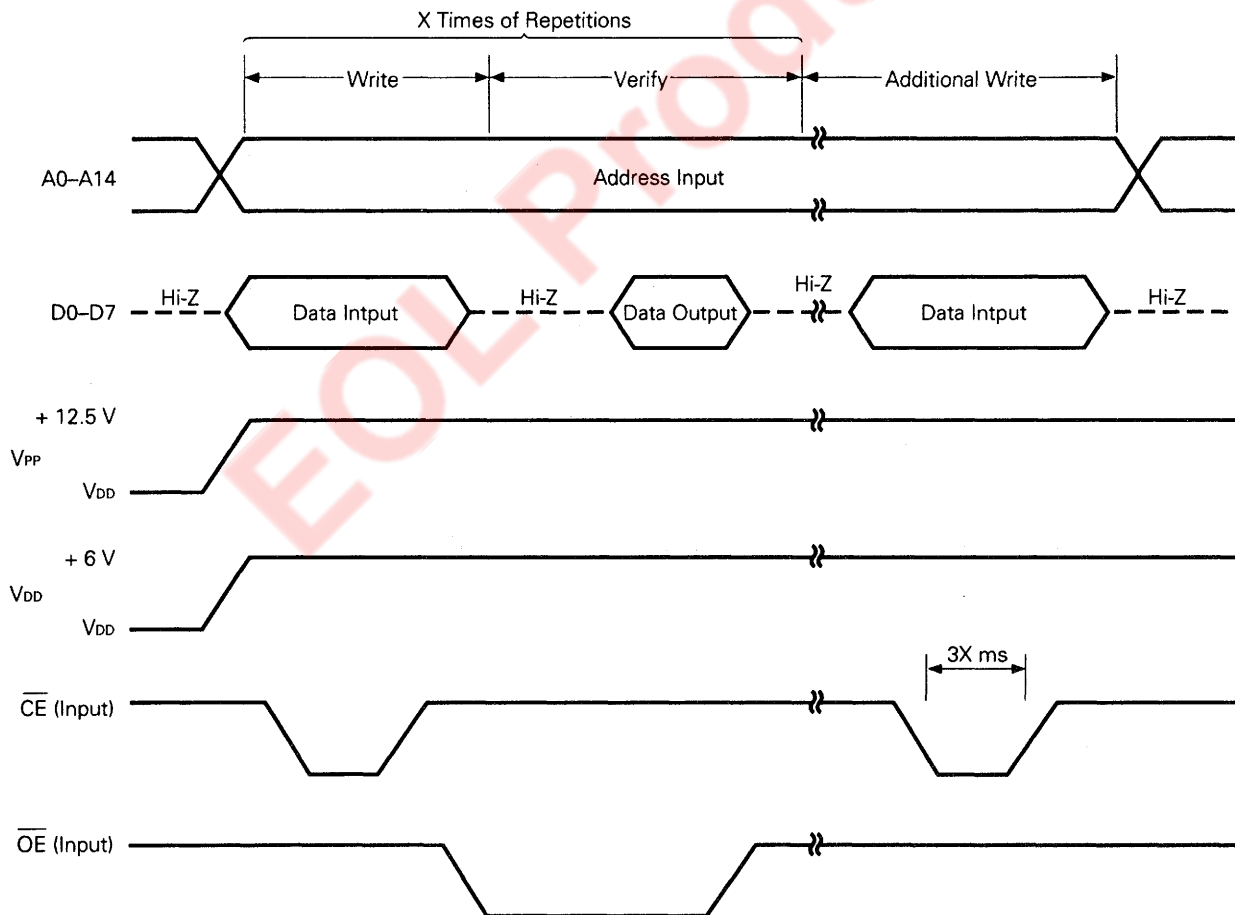
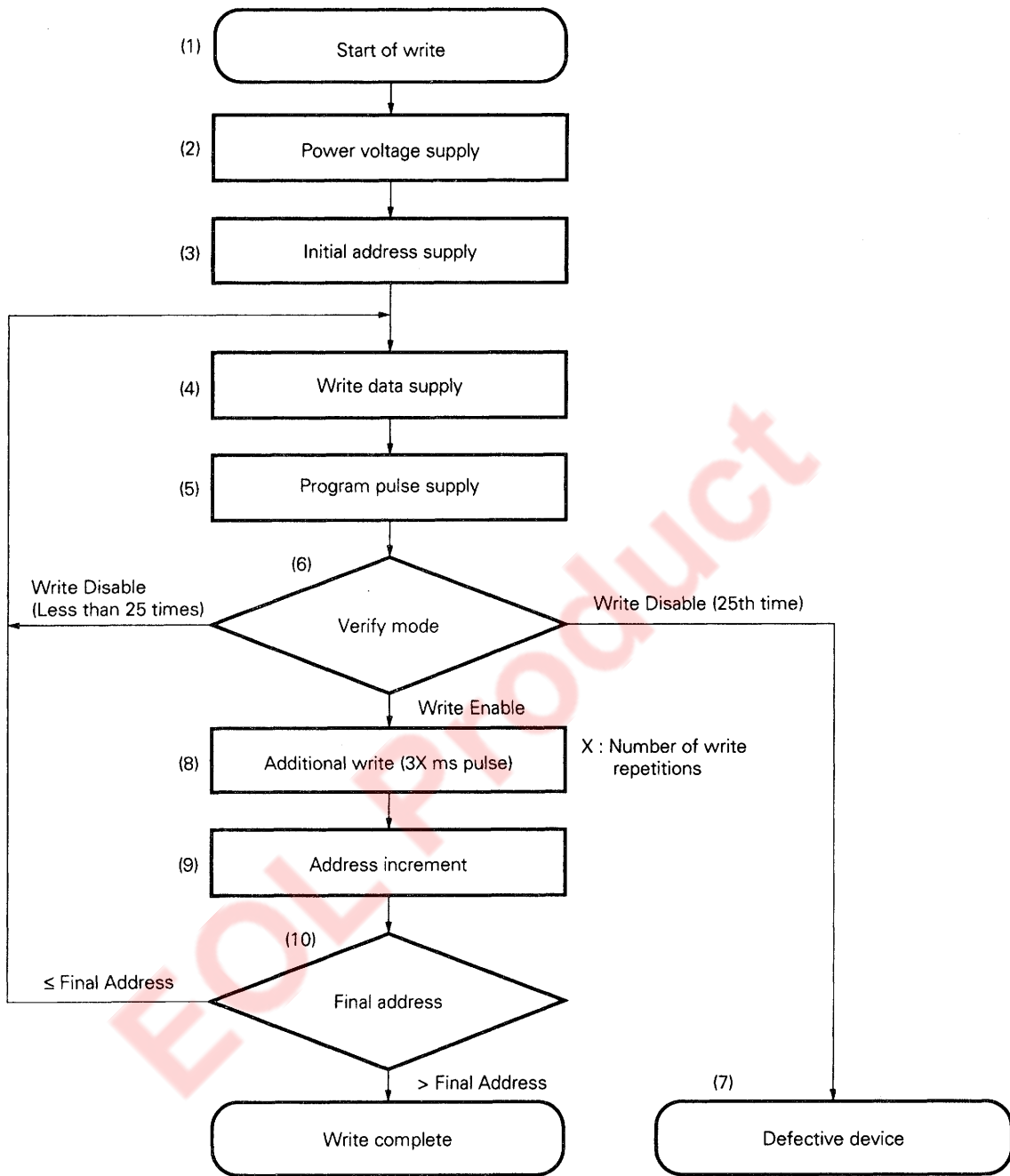


Fig. 3-2 Write Operation Flowchart



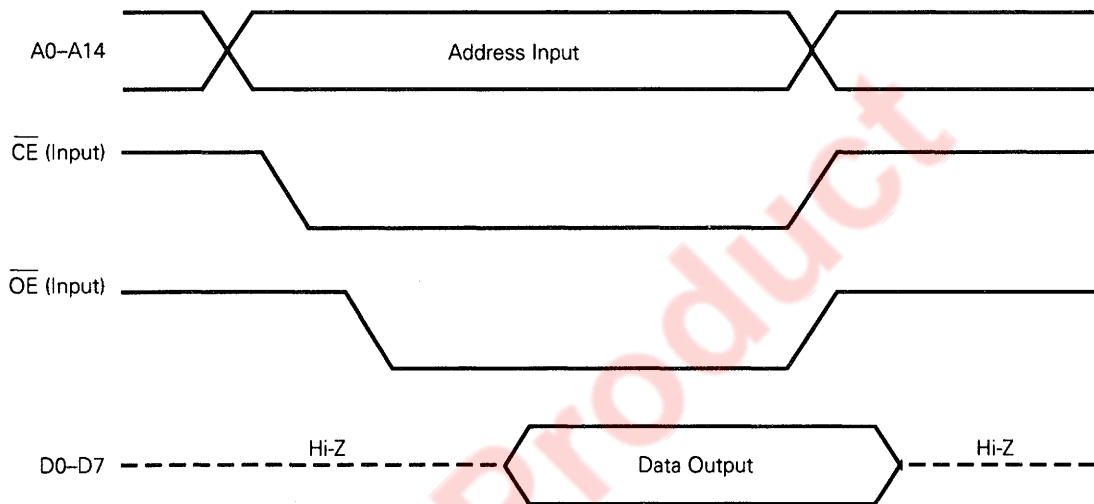
**3.3 PROM READ PROCEDURE**

PROM contents can be read into the external data bus (D0 to D7) using the following procedure:

- (1) Fix the  $\overline{\text{RESET}}$  pin to the low level. Apply +12.5 V to the NMI pin. Treat all other unused pins as shown in the pin configuration.
- (2) Apply +5 V to the  $V_{\text{DD}}$  and  $V_{\text{PP}}$  pins.
- (3) Input the address of the data to be read to the A0 to A14 pins.
- (4) Set the read mode.
- (5) Output data to the D0 to D7 pins.

The timings in steps (2) to (5) are shown in Fig. 3-3.

**Fig. 3-3 PROM Read Timings**



**4. ERASE CHARACTERISTICS (μPD78P214DW ONLY)**

The μPD78P214DW can erase the programmed data content (FFH) by applying light having wavelengths of less than about 400 nm.

To erase the μPD78P214DW program memory contents, normally apply ultraviolet rays having a wavelength of 254 nm. The total radiation required to erase the μPD78P214DW contents completely is a minimum of 15 W·s/cm<sup>2</sup> (ultraviolet strength × erase time). The erase time is approximately 15 to 20 minutes (when a 12000 μW/cm<sup>2</sup> ultraviolet lamp is used). The erase time may possible become longer due to deterioration in the performance of the ultraviolet lamp or fouling of the package window. For the erase operation, place the μPD78P214DW within 2.5 cm from the ultraviolet lamp. Use the ultraviolet lamp with the filter removed.

**5. ERASE WINDOW SEALING (μPD78P214DW ONLY)**

Except when erasing EPROM contents, apply a protective seal to the erase window. This is important to prevent the EPROM contents from being inadvertently erased due to light other than the erase lamp or the internal circuits other than the EPROM from malfunctioning due to light.

**6. SCREENING OF ONE-TIME PROM PRODUCTS**

By reason of their structure, one-time PROM products (μPD78P214CW, μPD78P214GC-AB8, μPD78P214GJ-5BJ, μPD78P214GQ-36, and μPD78P214L) cannot be fully tested by NEC prior to shipment. After the necessary data has been written, it is recommended that screening be performed for PROM verification after high-temperature storage under the following conditions.

| Storage Temperature | Storage Period |
|---------------------|----------------|
| 125 °C              | 24 hrs.        |

Under the generic name "QTOP microcomputer", NEC offers a charged service covering one-time PROM writing, printing, screening and verification. Please consult our sales representative for details.

7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = +25 °C)

| PARAMETER             | SYMBOL            | TEST CONDITIONS       | RATING                         | UNIT |
|-----------------------|-------------------|-----------------------|--------------------------------|------|
| Supply voltage        | V <sub>DD</sub>   |                       | -0.5 to +7.0                   | V    |
|                       | AV <sub>REF</sub> |                       | -0.5 to V <sub>DD</sub> +0.5   | V    |
|                       | AV <sub>SS</sub>  |                       | -0.5 to +0.5                   | V    |
| Input voltage         | V <sub>I1</sub>   |                       | -0.5 to V <sub>DD</sub> +0.5   | V    |
|                       | V <sub>I2</sub>   | *1                    | -0.5 to AV <sub>REF</sub> +0.5 | V    |
|                       | V <sub>I3</sub>   | *2                    | -0.5 to +13.5                  | V    |
| Output voltage        | V <sub>O</sub>    |                       | -0.5 to V <sub>DD</sub> +0.5   | V    |
| Output current low    | I <sub>OL</sub>   | 1 pin                 | 15                             | mA   |
|                       |                   | All output pins total | 100                            | mA   |
| Output current high   | I <sub>OH</sub>   | 1 pin                 | -10                            | mA   |
|                       |                   | All output pins total | -50                            | mA   |
| Operating temperature | T <sub>opt</sub>  |                       | -40 to +85                     | °C   |
| Storage temperature   | T <sub>stg</sub>  |                       | -65 to +150                    | °C   |

- \* 1. 70/AN0 to P75/AN5, P66/WAIT/AN6, and P67/REFRQ/AN7 pins except for those used as A/D converter input pins and those selected by ANI0 to ANI2 bits of the ADM register when the A/D converter is not in operation. However, it is required that the V<sub>I1</sub> absolute maximum rating is satisfied.
- 2. P20/NMI, EA/V<sub>PP</sub> and P21/INTP0/A9 pins in the PROM programming mode

OPERATING CONDITIONS

| CLOCK FREQUENCY                  | OPERATING TEMPERATURE (T <sub>opt</sub> ) | SUPPLY VOLTAGE (V <sub>DD</sub> ) |
|----------------------------------|---|-----------------------------------|
| 4 MHz ≤ f <sub>xx</sub> ≤ 12 MHz | -40 to +85 °C                             | +5.0 V ±10 %                      |

CAPACITANCE (Ta = +25 °C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

| PARAMETER          | SYMBOL          | TEST CONDITIONS                                  | MIN. | TYP. | MAX. | UNIT |
|--------------------|-----------------|--|------|------|------|------|
| Input capacitance  | C <sub>i</sub>  | f = 1 MHz<br>unmeasured pins<br>returned to 0 V. |      |      | 20   | pF   |
| Output capacitance | C <sub>o</sub>  |  |      |      | 20   | pF   |
| I/O capacitance    | C <sub>io</sub> |  |      |      | 20   | pF   |



OSCILLATOR CHARACTERISTICS (Ta = -40 to +85 °C, VDD = +5 V ±10 %, VSS = 0 V)

| RESONATOR                              | RECOMMENDED CIRCUIT | PARAMETER  | MIN. | MAX. | Unit |
|--|---------------------|--|------|------|------|
| Ceramic resonator or crystal resonator |                     | Oscillator frequency (f <sub>xx</sub> )                              | 4    | 12   | MHz  |
| External clock                         |                     | X1 input frequency (f <sub>x</sub> )                                 | 4    | 12   | MHz  |
|  |                     | X1 input rising/falling time (t <sub>xR</sub> , t <sub>xF</sub> )    | 0    | 30   | ns   |
|  |                     | X1 input high/low level width (t <sub>wXH</sub> , t <sub>wXL</sub> ) | 30   | 130  | ns   |

**Note** When using the clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V<sub>ss</sub>. Do not ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

**RECOMMENDED OSCILLATION CIRCUIT CONSTANTS**

**CERAMIC RESONATOR**

| MANUFACTURER          | FREQUENCY [MHz] | PRODUCT NAME | RECOMMENDED CONSTANTS  |         |
|-----------------------|-----------------|--------------|------------------------|---------|
|                       |                 |              | C1 [pF]                | C2 [pF] |
| Murata Mfg. Co., Ltd. | 12              | CSA12.0MT    | 30                     | 30      |
|                       |                 | CST12.0MT    | Capacitor on-chip type |         |
|                       | 4               | CSA4.00MG040 | 100                    | 100     |
|                       |                 | CST4.00MG040 | Capacitor on-chip type |         |
| Kyocera Corporation   | 12              | KBR12.0M     | 33                     | 33      |

**CRYSTAL RESONATOR**

| MANUFACTURER  | FREQUENCY [MHz] | PRODUCT NAME | RECOMMENDED CONSTANTS |         |
|---------------|-----------------|--------------|-----------------------|---------|
|               |                 |              | C1 [pF]               | C2 [pF] |
| Kinseki, Ltd. | 12              | HC-49/U      | 18                    | 18      |

EOL Product

DC CHARACTERISTICS (Ta = -40 to +85 °C, VDD = +5 V  $\pm$ 10 %, VSS = 0 V)

| PARAMETER                      | SYMBOL            | TEST CONDITIONS   | MIN.                               | TYP. | MAX.              | UNIT       |         |
|--------------------------------|-------------------|---|------------------------------------|------|-------------------|------------|---------|
| Input voltage low              | V <sub>IL</sub>   |   | 0                                  |      | 0.8               | V          |         |
| Input voltage high             | V <sub>IH1</sub>  | Pins except for *1 and *2                                     | 2.2                                |      | V <sub>DD</sub>   | V          |         |
|                                | V <sub>IH2</sub>  | Pin of *1   | 2.2                                |      | AV <sub>REF</sub> | V          |         |
|                                | V <sub>IH3</sub>  | Pin of *2   | 0.8V <sub>DD</sub>                 |      | V <sub>DD</sub>   | V          |         |
| Output voltage low             | V <sub>OL1</sub>  | I <sub>OL</sub> = 2.0 mA                                      |                                    |      | 0.45              | V          |         |
|                                | V <sub>OL2</sub>  | I <sub>OL</sub> = 8.0 mA *3                                   |                                    |      | 1.0               | V          |         |
| Output voltage high            | V <sub>OH1</sub>  | I <sub>OH</sub> = -1.0 mA                                     | V <sub>DD</sub> -1.0               |      |                   | V          |         |
|                                | V <sub>OH2</sub>  | I <sub>OH</sub> = -100 $\mu$ A                                | V <sub>DD</sub> -0.5               |      |                   | V          |         |
|                                | V <sub>OH3</sub>  | I <sub>OH</sub> = -5.0 mA *4                                  | 2.0                                |      |                   | V          |         |
| X1 input current low           | I <sub>IL</sub>   | 0 V $\leq$ V <sub>i</sub> $\leq$ V <sub>IL</sub>              |                                    |      | -100              | $\mu$ A    |         |
| X1 input current high          | I <sub>IH</sub>   | V <sub>IH3</sub> $\leq$ V <sub>i</sub> $\leq$ V <sub>DD</sub> |                                    |      | 100               | $\mu$ A    |         |
| Input leakage current          | I <sub>LI</sub>   | 0 V $\leq$ V <sub>i</sub> $\leq$ V <sub>DD</sub>              |                                    |      | $\pm$ 10          | $\mu$ A    |         |
| Output leakage current         | I <sub>LO</sub>   | 0 V $\leq$ V <sub>o</sub> $\leq$ V <sub>DD</sub>              |                                    |      | $\pm$ 10          | $\mu$ A    |         |
| AV <sub>REF</sub> current      | AI <sub>REF</sub> | Operating mode f <sub>xx</sub> = 12 MHz                       |                                    | 1.5  | 5.0               | mA         |         |
| V <sub>DD</sub> supply current | I <sub>DD1</sub>  | Operating mode f <sub>xx</sub> = 12 MHz                       |                                    | 20   | 40                | mA         |         |
|                                | I <sub>DD2</sub>  | HALT mode f <sub>xx</sub> = 12 MHz                            |                                    | 7    | 20                | mA         |         |
| Data retention voltage         | V <sub>DDDR</sub> | STOP mode   | 2.5                                |      | 5.5               | V          |         |
| Data retention current         | I <sub>DDDR</sub> | STOP mode   | V <sub>DDDR</sub> = 2.5 V          |      | 2                 | 20         | $\mu$ A |
|                                |                   |   | V <sub>DDDR</sub> = 5 V $\pm$ 10 % |      | 5                 | 50         | $\mu$ A |
| Pull-up resistor               | R <sub>L</sub>    | V <sub>i</sub> = 0 V  | 15                                 | 40   | 80                | k $\Omega$ |         |

- \* 1. P70/AN0 to P75/AN5, P66/ $\overline{\text{WAIT}}$ /AN6, and P67/ $\overline{\text{REFRQ}}$ /AN7 pins except for those used as A/D converter input pins and those selected by ANI0 to ANI2 bits of the ADM register when the A/D converter is not in operation.
2. X1, X2,  $\overline{\text{RESET}}$ , P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/ $\overline{\text{SCK}}$ , P33/SO/SB0,  $\overline{\text{EA}}$  pins
3. P40/AD0 to P47/AD7, P50/A8 to P57/A15 pins
4. P00 to P07 pins

AC CHARACTERISTICS (Ta = -40 to +85 °C, VDD = +5 V ±10 %, VSS = 0 V)

READ/WRITE OPERATION (1/2)

| PARAMETER                        | SYMBOL   | TEST CONDITIONS                                 | MIN. | MAX. | UNIT |
|----------------------------------|----------|---|------|------|------|
| X1 input clock cycle time        | tcyx     |   | 82   | 250  | ns   |
| Address set-up time (to ASTB↓)   | tsAST •  |   | 52   |      | ns   |
| Address hold time (from ASTB↓) * | thSTA    |   | 25   |      | ns   |
| Address hold time (from RD↑)     | thRA     |   | 30   |      | ns   |
| Address hold time (from WR↑)     | thWA     |   | 30   |      | ns   |
| RD↓ delay time from address      | tdAR •   |   | 129  |      | ns   |
| Address float time (from RD↓)    | tfAR •   |   | 11   |      | ns   |
| Data input time from address     | tdAID •  | Number of waits = 0                             |      | 228  | ns   |
| Data input time from ASTB↓       | tdSID •  | Number of waits = 0                             |      | 181  | ns   |
| Data input time from RD↓         | tdRID •  | Number of waits = 0                             |      | 100  | ns   |
| RD↓ delay time from ASTB↓        | tdSTR •  |   | 52   |      | ns   |
| Data hold time (from RD↑)        | thRID    |   | 0    |      | ns   |
| Address active time from RD↑     | tdRA •   |   | 124  |      | ns   |
| ASTB↑ delay time from RD↑        | tdRST •  |   | 124  |      | ns   |
| RD low-level width               | twRL •   | Number of waits = 0                             | 124  |      | ns   |
| ASTB high-level width            | twSTH •  |   | 52   |      | ns   |
| WR↓ delay time from address      | tdAW •   |   | 129  |      | ns   |
| Data output time from ASTB↓      | tdSTOD • |   |      | 142  | ns   |
| Data output time from WR↓        | tdWOD    |   |      | 60   | ns   |
| ★ WR↓ delay time from ASTB↓      | tdSTW1 • | With refreshing disabled                        | 52   |      | ns   |
|                                  | tdSTW2 • | With refreshing enabled                         | 129  |      | ns   |
| Data set-up time (to WR↑)        | tsODWR • | Number of waits = 0                             | 146  |      | ns   |
| Data set-up time (to WR↓)        | tsODWF • | With refreshing enabled                         | 22   |      | ns   |
| Data hold time (from WR↑) *      | thWOD    |   | 20   |      | ns   |
| ASTB↑ delay time from WR↑        | tdWST •  |   | 42   |      | ns   |
| ★ WR low-level width             | twWL1 •  | With refreshing disabled<br>Number of waits = 0 | 196  |      | ns   |
|                                  | twWL2 •  | With refreshing enabled<br>Number of waits = 0  | 114  |      | ns   |
| WAIT↓ input time from address    | tdAWT •  |   |      | 146  | ns   |
| WAIT↓ input time from ASTB↓      | tdSTWT • |   |      | 84   | ns   |

\* The hold time includes the time to hold the VOH and VOL under the load conditions of CL = 100 pF and RL = 2 kΩ.

- Remarks**
1. The values in the above table are based on "fxx = 12 MHz and CL = 100 pF".
  2. For a parameter with a dot(•) in the SYMBOL column, refer to "tcyx **DEPENDENT BUS TIMING DEFINITION**" as well.

READ/WRITE OPERATION (2/2)

| PARAMETER  | SYMBOL                | TEST CONDITIONS           | MIN.                      | MAX. | UNIT |
|--|-----------------------|---------------------------|---------------------------|------|------|
| $\overline{\text{WAIT}}$ hold time from $\text{ASTB}\downarrow$                                    | $t_{\text{HSTWT}}^*$  | No. of external waits = 1 | 174                       |      | ns   |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\text{ASTB}\downarrow$                           | $t_{\text{DSTWTH}}^*$ | No. of external waits = 1 |                           | 273  | ns   |
| $\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{RD}}\downarrow$                | $t_{\text{DRWTL}}^*$  |                           |                           | 22   | ns   |
| $\overline{\text{WAIT}}$ hold time from $\overline{\text{RD}}\downarrow$                           | $t_{\text{HRWT}}^*$   | No. of external waits = 1 | 87                        |      | ns   |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\overline{\text{RD}}\downarrow$                  | $t_{\text{DRWTH}}^*$  | No. of external waits = 1 |                           | 186  | ns   |
| Data input time from $\overline{\text{WAIT}}\uparrow$  | $t_{\text{DWTID}}^*$  |                           |                           | 62   | ns   |
| $\overline{\text{WR}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$                    | $t_{\text{DWTW}}^*$   |                           | 154                       |      | ns   |
| $\overline{\text{RD}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$                    | $t_{\text{DWTR}}^*$   |                           | 72                        |      | ns   |
| $\overline{\text{WAIT}}$ input time from $\overline{\text{WR}}\downarrow$<br>(At refresh disabled) | $t_{\text{DWWTL}}^*$  |                           |                           | 22   | ns   |
| $\overline{\text{WAIT}}$ hold time from $\overline{\text{WR}}\downarrow$                           | Refresh disabled      | $t_{\text{HWWT1}}^*$      | No. of external waits = 1 | 87   | ns   |
|  | Refresh enabled       | $t_{\text{HWWT2}}^*$      | No. of external waits = 1 | 5    | ns   |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\overline{\text{WR}}\downarrow$                  | Refresh disabled      | $t_{\text{DWWTH1}}^*$     | No. of external waits = 1 | 186  | ns   |
|  | Refresh enabled       | $t_{\text{DWWTH2}}^*$     | No. of external waits = 1 | 104  | ns   |
| $\overline{\text{REFRQ}}\downarrow$ delay time from $\overline{\text{RD}}\uparrow$                 | $t_{\text{DRRFQ}}^*$  |                           | 154                       |      | ns   |
| $\overline{\text{REFRQ}}\downarrow$ delay time from $\overline{\text{WR}}\uparrow$                 | $t_{\text{DWRFQ}}^*$  |                           | 72                        |      | ns   |
| $\overline{\text{REFRQ}}$ low-level width  | $t_{\text{WRFQL}}^*$  |                           | 120                       |      | ns   |
| $\text{ASTB}\uparrow$ delay time from $\overline{\text{REFRQ}}\uparrow$                            | $t_{\text{DRFQST}}^*$ |                           | 280                       |      | ns   |

- Remarks**
1. The values in the above table are based on "f<sub>xx</sub> = 12 MHz and C<sub>L</sub> = 100 pF".
  2. For a parameter with a dot(\*) in the SYMBOL column, refer to "tcvx **DEPENDENT BUS TIMING DEFINITION** " as well.

SERIAL OPERATION

| PARAMETER  | SYMBOL | TEST CONDITIONS                                   |                        | MIN. | MAX. | UNIT |
|--|--------|---|------------------------|------|------|------|
| Serial clock cycle time  | tcvsk  | Input   | External clock         | 1.0  |      | μs   |
|  |        | Output  | Internal divided by 16 | 1.3  |      | μs   |
|  |        |   | Internal divided by 64 | 5.3  |      | μs   |
| Serial clock low-level width                                   | twskL  | Input   | External clock         | 420  |      | ns   |
|  |        | Output  | Internal divided by 16 | 556  |      | ns   |
|  |        |   | Internal divided by 64 | 2.5  |      | μs   |
| Serial clock high-level width                                  | twskH  | Input   | External clock         | 420  |      | ns   |
|  |        | Output  | Internal divided by 16 | 556  |      | ns   |
|  |        |   | Internal divided by 64 | 2.5  |      | μs   |
| SI, SB0 set-up time (to $\overline{SCK}\uparrow$ )             | tsssk  |   |                        | 150  |      | ns   |
| SI, SB0 hold time (from $\overline{SCK}\uparrow$ )             | thssk  |   |                        | 400  |      | ns   |
| SO/SB0 output delay time<br>(from $\overline{SCK}\downarrow$ ) | tdssk1 | CMOS push-pull output<br>(3-wire serial I/O mode) |                        | 0    | 300  | ns   |
|  | tdssk2 | Open-drain output (SBI mode),<br>RL = 1 kΩ        |                        | 0    | 800  | ns   |
| SB0 high hold time (from $\overline{SCK}\uparrow$ )            | thssk  | SBI mode  |                        | 4    |      | tcvx |
| SB0 low set-up time (to $\overline{SCK}\downarrow$ )           | tsssk  |   |                        | 4    |      | tcvx |
| SB0 low-level width  | twssL  |   |                        | 4    |      | tcvx |
| SB0 high-level width   | twssH  |   |                        | 4    |      | tcvx |

Remarks The values in the above table are based on "fxx = 12 MHz and CL = 100 pF".

**OTHER OPERATIONS**

| PARAMETER                       | SYMBOL | TEST CONDITIONS | MIN. | MAX. | UNIT |
|---------------------------------|--------|-----------------|------|------|------|
| NMI low-level width             | tWNIL  |                 | 10   |      | μs   |
| NMI high-level width            | tWNIH  |                 | 10   |      | μs   |
| INTP0 to INTP5 low-level width  | tWTL   |                 | 24   |      | tcyx |
| INTP0 to INTP5 high-level width | tWTH   |                 | 24   |      | tcyx |
| RESET low-level width           | tWRBL  |                 | 10   |      | μs   |
| RESET high-level width          | tWRBH  |                 | 10   |      | μs   |

**EXTERNAL CLOCK TIMING**

| PARAMETER                 | SYMBOL | TEST CONDITIONS | MIN. | MAX. | UNIT |
|---------------------------|--------|-----------------|------|------|------|
| X1 input low-level width  | twXL   |                 | 30   | 130  | ns   |
| X1 input high-level width | twXH   |                 | 30   | 130  | ns   |
| X1 input rise time        | txR    |                 | 0    | 30   | ns   |
| X1 input fall time        | txF    |                 | 0    | 30   | ns   |
| X1 input clock cycle time | tcyx   |                 | 82   | 250  | ns   |

**A/D CONVERTER CHARACTERISTICS (Ta = -40 to +85 °C, VDD = +5 V ±10 %, VSS = AVSS = 0 V)**

| PARAMETER              | SYMBOL | TEST CONDITIONS  | MIN. | TYP. | MAX.          | UNIT |
|------------------------|--------|--|------|------|---------------|------|
| Resolution             |        |  | 8    |      |               | bit  |
| Overall error*         |        | 4.0 V ≤ AVREF ≤ VDD<br>Ta = -10 to +70 °C                  |      |      | 0.4           | %    |
|                        |        | 3.4 V ≤ AVREF ≤ VDD<br>Ta = -10 to +70 °C                  |      |      | 0.8           | %    |
|                        |        | 4.0 V ≤ AVREF ≤ VDD  |      |      | 0.8           | %    |
| Quantization error     |        |  |      |      | ±1/2          | LSB  |
| Conversion time        | tCONV  | 82 ns ≤ tcyx < 125 ns<br>(The FR bit of ADM is to be "0")  | 360  |      |               | tcyx |
|                        |        | 125 ns ≤ tcyx ≤ 250 ns<br>(The FR bit of ADM is to be "1") | 240  |      |               | tcyx |
| Sampling time          | tSAMP  | 82 ns ≤ tcyx < 125 ns<br>(The FR bit of ADM is to be "0")  | 72   |      |               | tcyx |
|                        |        | 125 ns ≤ tcyx ≤ 250 ns<br>(The FR bit of ADM is to be "1") | 48   |      |               | tcyx |
| Analog input voltage   | VIAN   |  | -0.3 |      | AVREF<br>+0.3 | V    |
| Analog input impedance | RAN    |  |      | 1000 |               | MΩ   |
| Reference voltage      | AVREF  |  | 3.4  |      | VDD           | V    |
| AVREF current          | AIREF  | fxx = 12 MHz   |      | 1.5  | 5.0           | mA   |
|                        |        | STOP mode  |      | 0.2  | 1.5           | mA   |

\* Quantization error is not included. Represented by the ratio to full-scale value.

tcyx DEPENDENT BUS TIMING DEFINITION (1/2)

| PARAMETER                                   | SYMBOL | CALCULATION FORMULA                              | MIN./MAX. | 12 MHZ | UNIT |
|---|--------|--|-----------|--------|------|
| X1 input clock cycle time                   | tcyx   |  | MIN.      | 82     | ns   |
| Address set-up time (to ASTB↓)              | tsAST  | tcyx - 30  | MIN.      | 52     | ns   |
| $\overline{RD}$ ↓ delay time from address   | tdAR   | 2tcyx - 35                                       | MIN.      | 129    | ns   |
| Address float time (from $\overline{RD}$ ↓) | tFAR   | tcyx/2 - 30                                      | MIN.      | 11     | ns   |
| Data input time from address                | tDAID  | (4 + 2n) tcyx - 100                              | MAX.      | 228*   | ns   |
| Data input time from ASTB↓                  | tdSTID | (3 + 2n) tcyx - 65                               | MAX.      | 181*   | ns   |
| Data input time from $\overline{RD}$ ↓      | tdRID  | (2 + 2n) tcyx - 64                               | MAX.      | 100*   | ns   |
| $\overline{RD}$ ↓ delay time from ASTB↓     | tdSTR  | tcyx - 30  | MIN.      | 52     | ns   |
| Address active time from $\overline{RD}$ ↑  | tdRA   | 2tcyx - 40                                       | MIN.      | 124    | ns   |
| ASTB↑ delay time from $\overline{RD}$ ↑     | tdRST  | 2tcyx - 40                                       | MIN.      | 124    | ns   |
| $\overline{RD}$ low-level width             | twRL   | (2 + 2n) tcyx - 40                               | MIN.      | 124*   | ns   |
| ASTB high-level width                       | twSTH  | tcyx - 30  | MIN.      | 52     | ns   |
| $\overline{WR}$ ↓ delay time from address   | tdAW   | 2tcyx - 35                                       | MIN.      | 129    | ns   |
| Data output time from ASTB↓                 | tdSTOD | tcyx + 60  | MAX.      | 142    | ns   |
| ★ $\overline{WR}$ ↓ delay time from ASTB↓   | tdSTW1 | tcyx - 30<br>(With refreshing disabled)          | MIN.      | 52     | ns   |
|   | tdSTW2 | 2tcyx - 35<br>(With refreshing enabled)          | MIN.      | 129    | ns   |
| Data set-up time (to $\overline{WR}$ ↑)     | tsODWR | (3 + 2n) tcyx - 100                              | MIN.      | 146*   | ns   |
| Data set-up time (to $\overline{WR}$ ↓)     | tsODWF | tcyx - 60<br>(With refreshing enabled)           | MIN.      | 22     | ns   |
| ASTB↑ delay time from $\overline{WR}$ ↑     | tdWST  | tcyx - 40  | MIN.      | 42     | ns   |
| ★ $\overline{WR}$ low-level width           | twWL1  | (3 + 2n) tcyx - 50<br>(With refreshing disabled) | MIN.      | 196*   | ns   |
|   | twWL2  | (2 + 2n) tcyx - 50<br>(With refreshing enabled)  | MIN.      | 114*   | ns   |
| $\overline{WAIT}$ ↓ input time from address | tdAWT  | 3tcyx - 100                                      | MAX.      | 146    | ns   |
| $\overline{WAIT}$ ↓ input time from ASTB↓   | tdSTWT | 2tcyx - 80                                       | MAX.      | 84     | ns   |

Remarks "n" indicates the number of waits.

\* When n = 0



t<sub>cyx</sub> DEPENDENT BUS TIMING DEFINITION (2/2)

| PARAMETER  | SYMBOL              | CALCULATION FORMULA    | MIN./MAX. | 12 MHZ | UNIT |
|--|---------------------|------------------------|-----------|--------|------|
| $\overline{\text{WAIT}}$ hold time from $\text{ASTB}\downarrow$                                    | t <sub>HSTWT</sub>  | $2Xt_{cyx} + 10$       | MIN.      | 174*   | ns   |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\text{ASTB}\downarrow$                           | t <sub>DSTWTH</sub> | $2(1 + X)t_{cyx} - 55$ | MAX.      | 273*   | ns   |
| $\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{RD}}\downarrow$                | t <sub>DRWTL</sub>  | $t_{cyx} - 60$         | MAX.      | 22     | ns   |
| $\overline{\text{WAIT}}$ hold time from $\overline{\text{RD}}\downarrow$                           | t <sub>HRWT</sub>   | $(2X - 1)t_{cyx} + 5$  | MIN.      | 87*    | ns   |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\overline{\text{RD}}\downarrow$                  | t <sub>DRWTH</sub>  | $(2X + 1)t_{cyx} - 60$ | MAX.      | 186*   | ns   |
| Data input time from $\overline{\text{WAIT}}\uparrow$  | t <sub>DWTID</sub>  | $t_{cyx} - 20$         | MAX.      | 62     | ns   |
| $\overline{\text{WR}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$                    | t <sub>DWTW</sub>   | $2t_{cyx} - 10$        | MIN.      | 154    | ns   |
| $\overline{\text{RD}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$                    | t <sub>DWTR</sub>   | $t_{cyx} - 10$         | MIN.      | 72     | ns   |
| $\overline{\text{WAIT}}$ input time from $\overline{\text{WR}}\downarrow$<br>(At refresh disabled) | t <sub>DWWTL</sub>  | $t_{cyx} - 60$         | MAX.      | 22     | ns   |
| $\overline{\text{WAIT}}$ hold time<br>from $\overline{\text{WR}}\downarrow$                        | Refresh disabled    | t <sub>HWWT1</sub>     | MIN.      | 87*    | ns   |
|  | Refresh enabled     | t <sub>HWWT2</sub>     | MIN.      | 5*     | ns   |
| $\overline{\text{WAIT}}\uparrow$ delay<br>time from $\overline{\text{WR}}\downarrow$               | Refresh disabled    | t <sub>DWWTH1</sub>    | MAX.      | 186*   | ns   |
|  | Refresh enabled     | t <sub>DWWTH2</sub>    | MAX.      | 104*   | ns   |
| $\overline{\text{REFRQ}}\downarrow$ delay time from $\overline{\text{RD}}\uparrow$                 | t <sub>DRRFQ</sub>  | $2t_{cyx} - 10$        | MIN.      | 154    | ns   |
| $\overline{\text{REFRQ}}\downarrow$ delay time from $\overline{\text{WR}}\uparrow$                 | t <sub>DWRFQ</sub>  | $t_{cyx} - 10$         | MIN.      | 72     | ns   |
| $\overline{\text{REFRQ}}$ low-level width  | t <sub>WRFQL</sub>  | $2t_{cyx} - 44$        | MIN.      | 120    | ns   |
| $\text{ASTB}\uparrow$ delay time from $\overline{\text{REFRQ}}\uparrow$                            | t <sub>DRFQST</sub> | $4t_{cyx} - 48$        | MIN.      | 280    | ns   |

- Remarks 1. X : The number of the external wait. (1, 2, ...)  
2. t<sub>cyx</sub> ≅ 82 ns (f<sub>xx</sub> = 12 MHz)

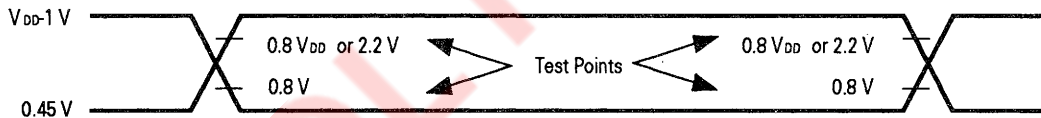
\* When X = 1

DATA RETENTION CHARACTERISTICS (Ta = -40 to +85 °C)

| PARAMETER  | SYMBOL            | TEST CONDITIONS               | MIN.                  | TYP. | MAX.                  | UNIT |
|--|-------------------|-------------------------------|-----------------------|------|-----------------------|------|
| Data retention voltage                             | V <sub>DDDR</sub> | STOP mode                     | 2.5                   |      | 5.5                   | V    |
| Data retention current                             | I <sub>DDDR</sub> | V <sub>DDDR</sub> = 2.5 V     |                       | 2    | 20                    | μA   |
|  |                   | V <sub>DDDR</sub> = 5 V ±10 % |                       | 5    | 50                    | μA   |
| V <sub>DD</sub> rise time                          | t <sub>RVD</sub>  |                               | 200                   |      |                       | μs   |
| V <sub>DD</sub> fall time                          | t <sub>FVD</sub>  |                               | 200                   |      |                       | μs   |
| V <sub>DD</sub> hold time (from STOP mode setting) | t <sub>HVD</sub>  |                               | 0                     |      |                       | ms   |
| STOP release signal input time                     | t <sub>DREL</sub> |                               | 0                     |      |                       | ms   |
| Oscillation stabilization wait time                | t <sub>WAIT</sub> | Crystal resonator             | 30                    |      |                       | ms   |
|  |                   | Ceramic resonator             | 5                     |      |                       | ms   |
| Low-level input voltage                            | V <sub>IL</sub>   | Specified pin*                | 0                     |      | 0.1 V <sub>DDDR</sub> | V    |
| High-level input voltage                           | V <sub>IH</sub>   |                               | 0.9 V <sub>DDDR</sub> |      | V <sub>DDDR</sub>     | V    |

\* RESET, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/SCK, P33/SO/SB0 EA pins

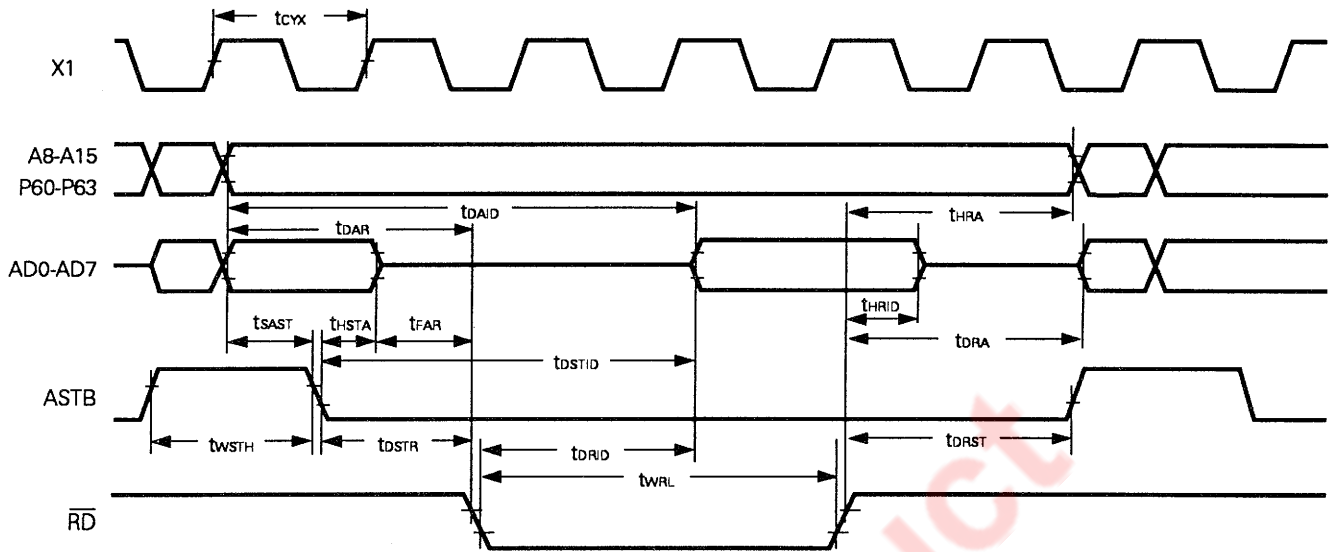
AC Timing Test Point



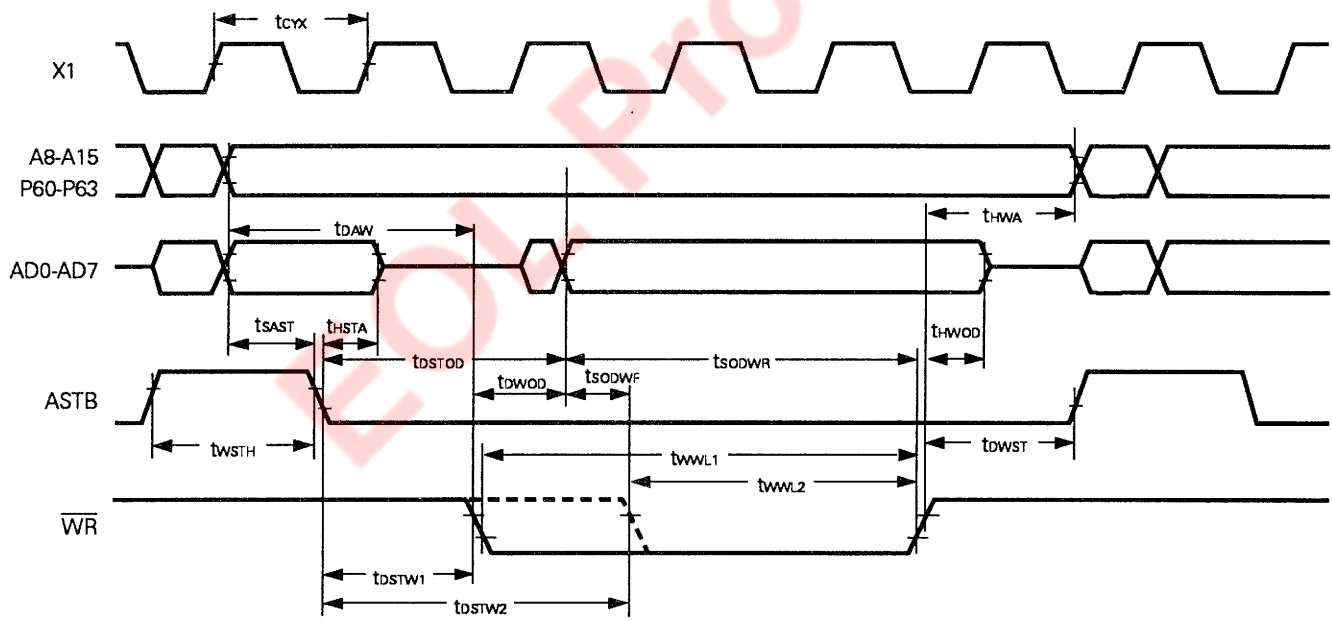
Timing Waveform



Read operation

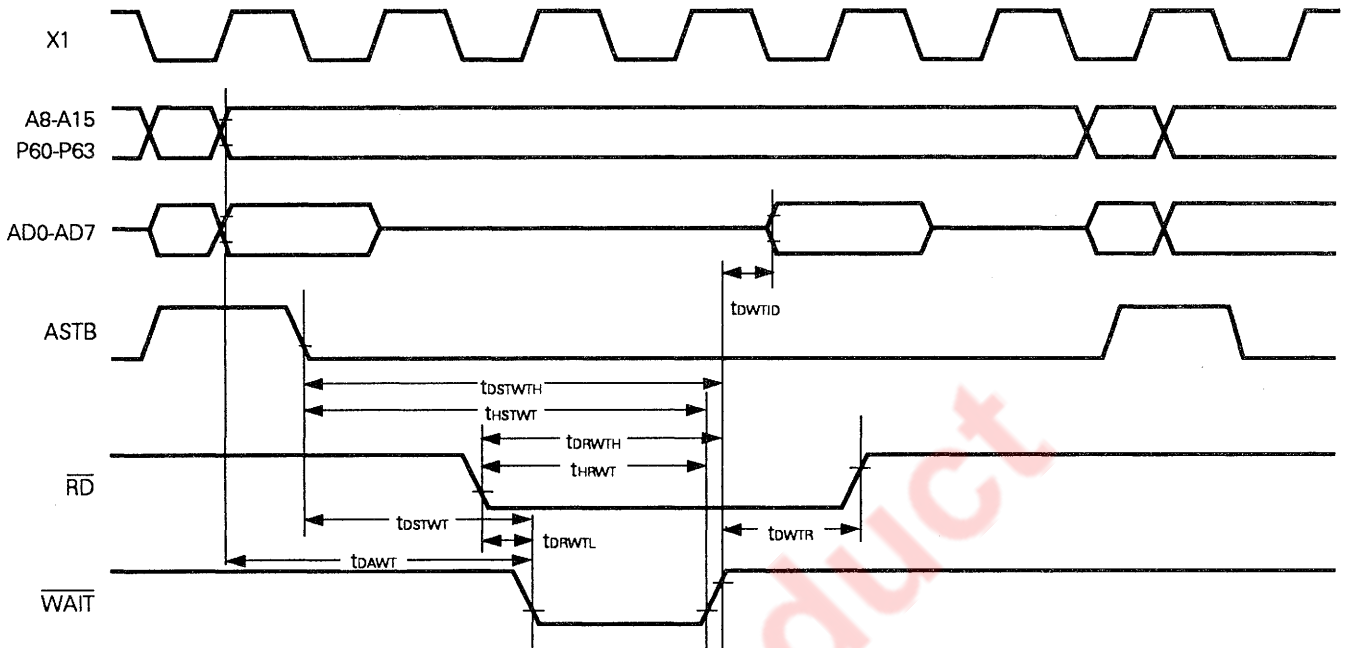


Write operation

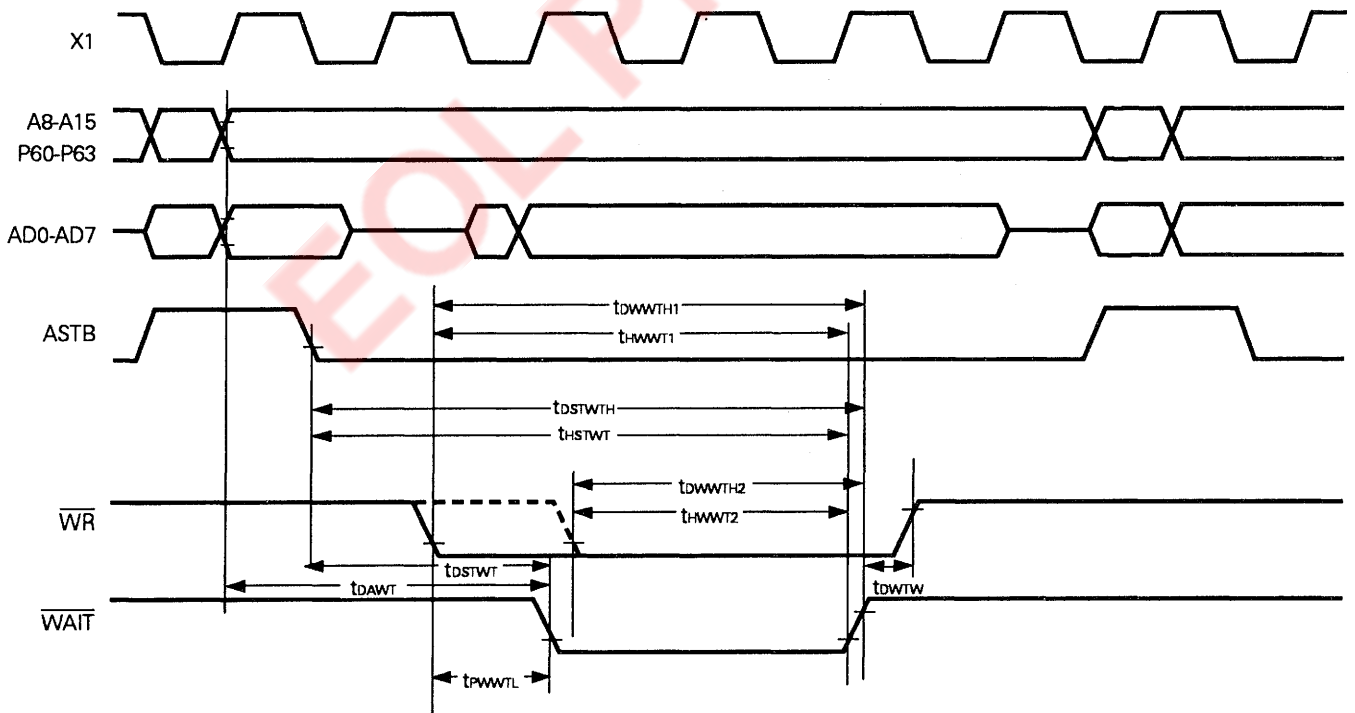


External WAIT Signal Input Timing

Read operation

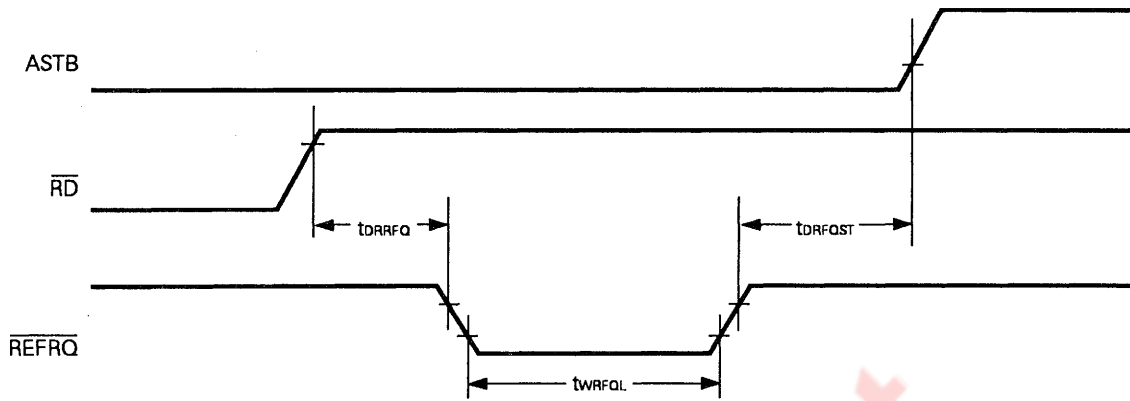


Write operation

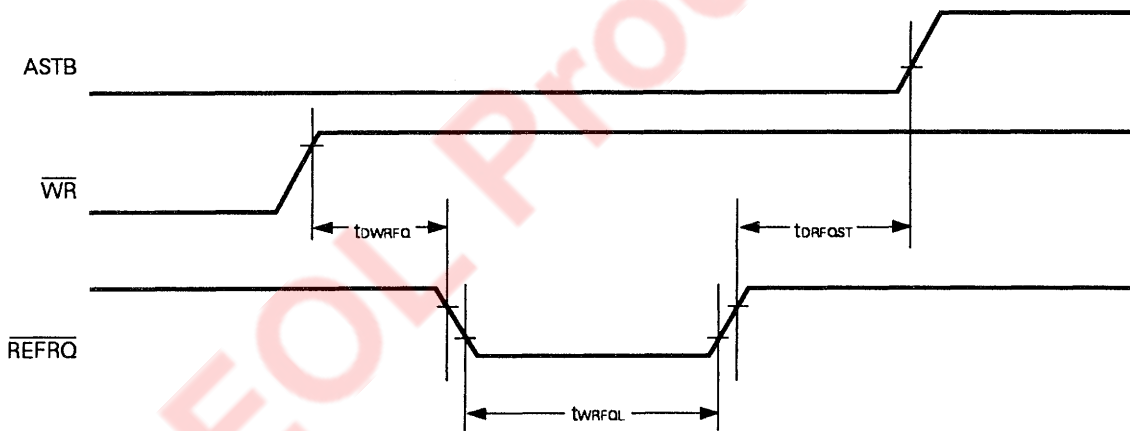


Refresh Timing Waveform

Refresh after read



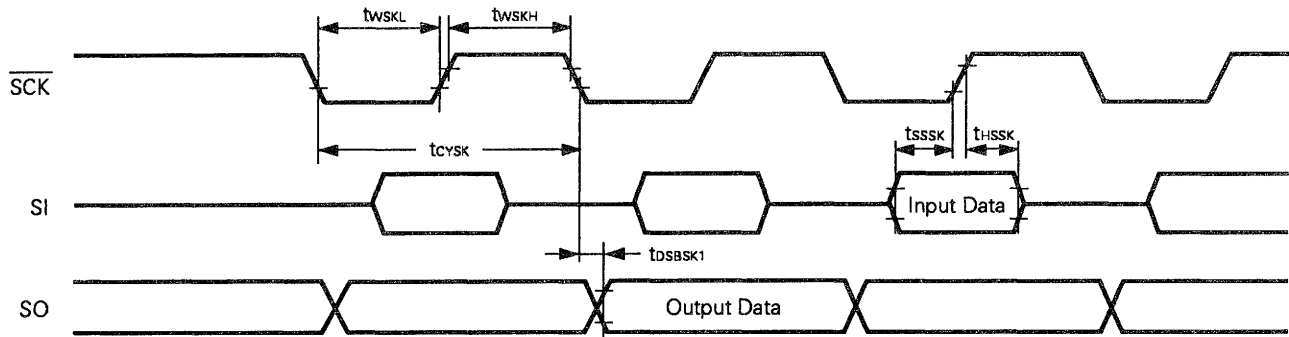
Refresh after write



EOL Product

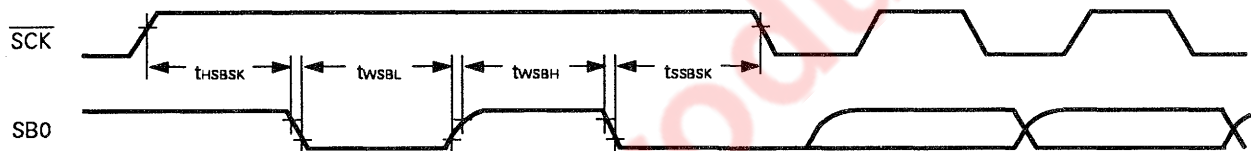
Serial Operation

3-wire serial I/O mode

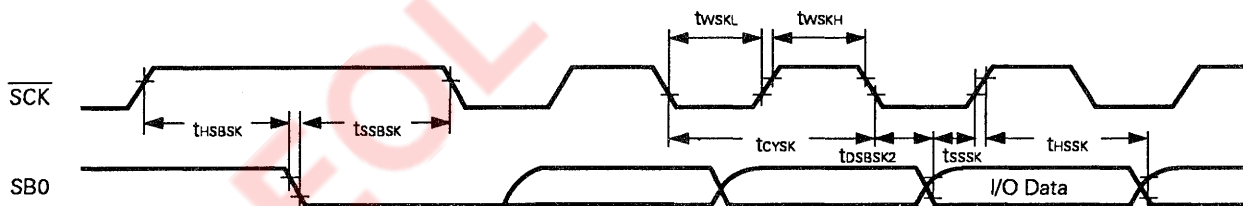


SBI Mode

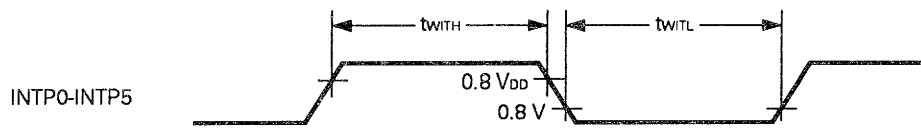
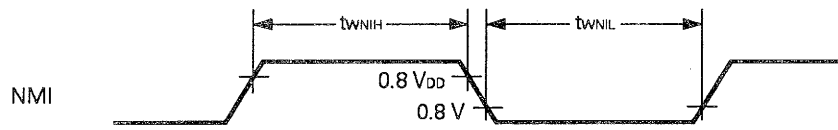
Bus release signal transfer



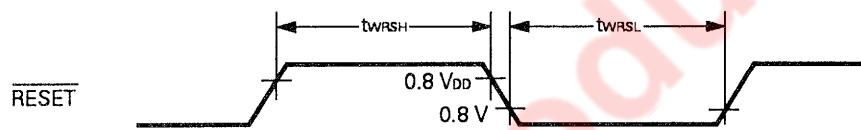
Command signal transfer



**Interrupt Input Timing**

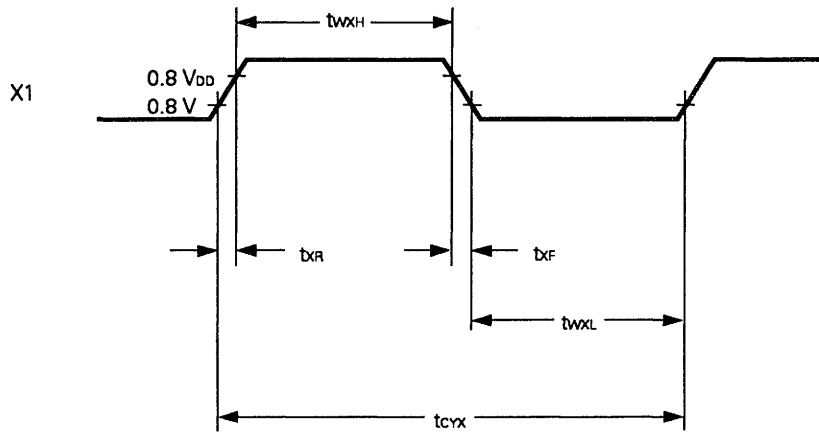


**Reset Input Timing**

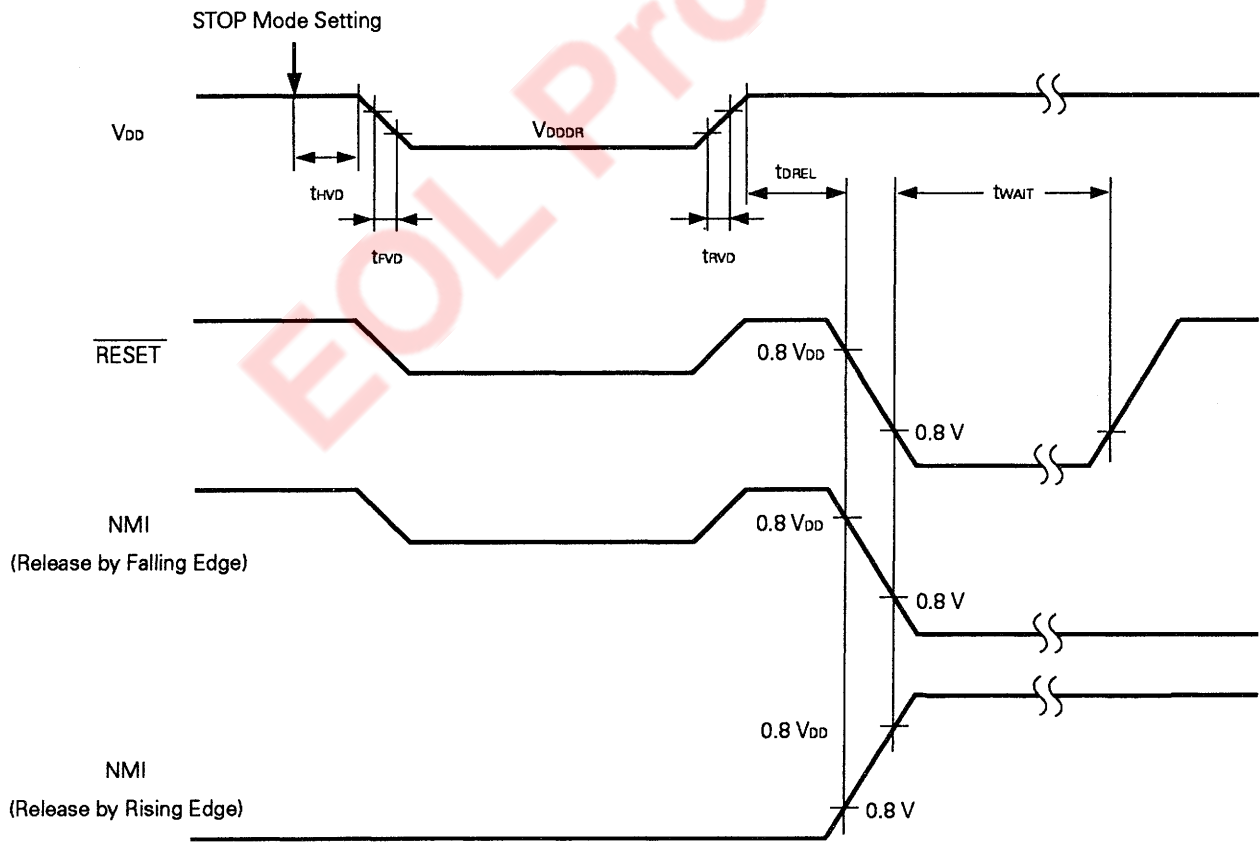


EOL Product

External Clock Timing



Data Retention Characteristics





DC PROGRAMMING CHARACTERISTICS (Ta = 25 ±5 °C, V<sub>IP</sub> \*1= 12.5 ±0.5 V, V<sub>SS</sub> = 0 V)

| PARAMETER                             | SYMBOL           | SYMBOL*2         | TEST CONDITIONS   | MIN.                               | TYP. | MAX.                  | UNIT |
|---------------------------------------|------------------|------------------|---|------------------------------------|------|-----------------------|------|
| Input voltage high                    | V <sub>IH</sub>  | V <sub>IH</sub>  |   | 2.4                                |      | V <sub>DDP</sub> +0.3 | V    |
| Input voltage low                     | V <sub>IL</sub>  | V <sub>IL</sub>  |   | -0.3                               |      | 0.8                   | V    |
| Input leakage current                 | I <sub>LIP</sub> | I <sub>LI</sub>  | 0 ≤ V <sub>I</sub> ≤ V <sub>DDP</sub>   |                                    |      | 10                    | μA   |
| Output voltage high                   | V <sub>OH1</sub> | V <sub>OH1</sub> | I <sub>OH</sub> = -400 μA   | 2.4                                |      |                       | V    |
|                                       | V <sub>OH2</sub> | V <sub>OH2</sub> | I <sub>OH</sub> = -100 μA   | V <sub>DD</sub> -0.7               |      |                       | V    |
| Output voltage low                    | V <sub>OL</sub>  | V <sub>OL</sub>  | I <sub>OH</sub> = 2.1 mA  |                                    |      | 0.45                  | V    |
| Output leakage current                | I <sub>LO</sub>  |                  | 0 ≤ V <sub>O</sub> ≤ V <sub>DDP</sub> , $\overline{OE} = V_{IH}$              |                                    |      | 10                    | μA   |
| NMI pin high-voltage input current    | I <sub>IP</sub>  |                  |   |                                    |      | ±10                   | μA   |
| V <sub>DDP</sub> power supply voltage | V <sub>DDP</sub> | V <sub>CC</sub>  | Program memory write mode   | 5.75                               | 6.0  | 6.25                  | V    |
|                                       |                  |                  | Program memory read mode  | 4.5                                | 5.0  | 5.5                   | V    |
| V <sub>PP</sub> power supply voltage  | V <sub>PP</sub>  | V <sub>PP</sub>  | Program memory write mode   | 12.2                               | 12.5 | 12.8                  | V    |
|                                       |                  |                  | Program memory read mode  | V <sub>PP</sub> = V <sub>DDP</sub> |      |                       | V    |
| V <sub>DDP</sub> power supply current | I <sub>DD</sub>  | I <sub>CC</sub>  | Program memory write mode   |                                    | 5    | 30                    | mA   |
|                                       |                  |                  | Program memory read mode<br>$\overline{CE} = V_{IL}, V_I = V_{IH}$            |                                    | 5    | 30                    | mA   |
| V <sub>PP</sub> power supply current  | I <sub>PP</sub>  | I <sub>PP</sub>  | Program memory write mode<br>$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$ |                                    | 5    | 30                    | mA   |
|                                       |                  |                  | Program memory read mode  |                                    | 1    | 100                   | μA   |

- \* 1. Voltage applied to P20/NMI pin
- 2. Symbol of the corresponding μPD27C256A

**PROGRAM OPERATION**

**AC CHARACTERISTICS (Ta = 25 ±5 °C, V<sub>IP</sub> \*1 = 12.5 ±0.5 V, V<sub>DD</sub> = 6 ±0.25 V, V<sub>PP</sub> = 12.5 ±0.3 V, V<sub>SS</sub> = 0 V)**

| PARAMETER  | SYMBOL | SYMBOL*2 | TEST CONDITIONS | MIN. | TYP. | MAX.  | UNIT |
|--|--------|----------|-----------------|------|------|-------|------|
| Address set-up time (to $\overline{CE}\downarrow$ )                | tsac   | tas      |                 | 2    |      |       | μs   |
| $\overline{OE}$ hold time (from input data disable)                | tddoo  | toes     |                 | 2    |      |       | μs   |
| Input data set-up time (to $\overline{CE}\downarrow$ )             | tsidc  | tbs      |                 | 2    |      |       | μs   |
| Address hold time (from $\overline{CE}\uparrow$ )                  | thca   | tah      |                 | 2    |      |       | μs   |
| Input data hold time (from $\overline{CE}\uparrow$ )               | thcid  | tdh      |                 | 2    |      |       | μs   |
| Output data hold time (from $\overline{OE}\uparrow$ )              | thood  | tdf      |                 | 0    |      | 130   | ns   |
| V <sub>PP</sub> set-up time (to $\overline{CE}\downarrow$ )        | tsvpc  | tvps     |                 | 1    |      |       | ms   |
| V <sub>DDP</sub> set-up time (to $\overline{CE}\downarrow$ )       | tsvdc  | tvcs     |                 | 1    |      |       | ms   |
| Initial program puls width   | twl1   | tpw      |                 | 0.95 | 1.0  | 1.05  | ms   |
| Additional program pulse width                                     | twl2   | topw     |                 | 2.85 |      | 78.75 | ms   |
| NMI high-voltage input set-up time (to $\overline{CE}\downarrow$ ) | tspc   |          |                 | 2    |      |       | μs   |
| Data output time from $\overline{OE}\downarrow$                    | tdood  | toe      |                 |      |      | 150   | ns   |

- \* 1. Voltage applied to P20/NMI pin
- 2. Symbol of the corresponding μPD27C256A

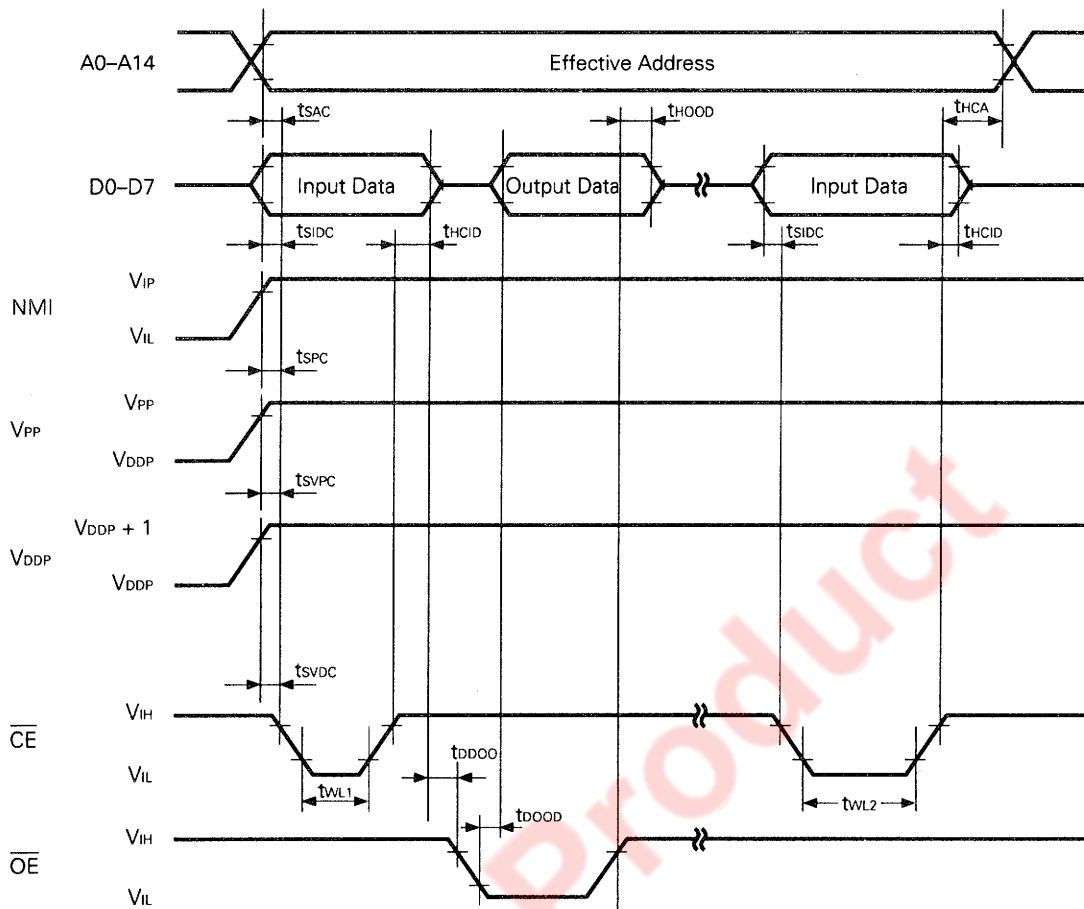
**READ OPERATION**

**AC CHARACTERISTICS (Ta = 25 ±5 °C, V<sub>IP</sub> \*1 = 12.5 V, V<sub>DD</sub> = 5 ±0.5 V, V<sub>PP</sub> = V<sub>DDP</sub>, V<sub>SS</sub> = 0 V)**

| PARAMETER   | SYMBOL | SYMBOL*2 | TEST CONDITIONS                                      | MIN. | TYP. | MAX. | UNIT |
|---|--------|----------|--|------|------|------|------|
| Address data output time  | tDAOD  | tACC     | $\overline{CE} = \overline{OE} = V_{IL}$             |      |      | 200  | ns   |
| Data output time from $\overline{CE}\downarrow$                           | tDCOD  | tCE      | $\overline{OE} = V_{IL}$                             |      |      | 200  | ns   |
| Data output time from $\overline{OE}\downarrow$                           | tDOOD  | toe      | $\overline{CE} = V_{IL}$                             |      |      | 75   | ns   |
| ★ Data hold time (from $\overline{OE}\uparrow, \overline{CE}\uparrow$ )*3 | tHCOD  | tdf      | $\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$ | 0    |      | 60   | ns   |
| Data hold time (from address)   | tHAOD  | toH      | $\overline{CE} = \overline{OE} = V_{IL}$             | 0    |      |      | ns   |

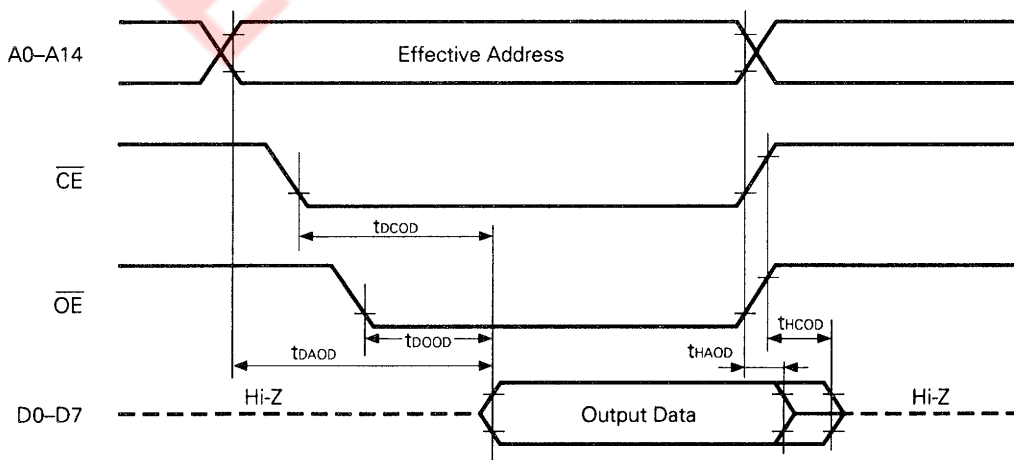
- \* 1. Voltage applied to P20/NMI pin
- 2. Symbol of the corresponding μPD27C256A
- 3. t<sub>HCOD</sub> is the time counted from when either  $\overline{OE}$  or  $\overline{CE}$  becomes V<sub>IH</sub>.

PROM Write Mode Timing



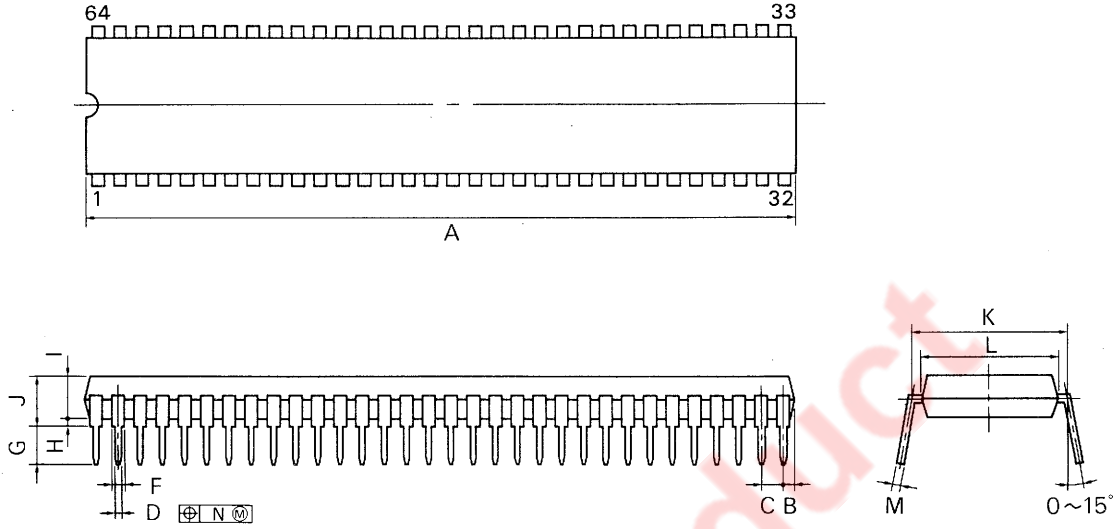
- Note**
1. Apply  $V_{DDP}$  before  $V_{PP}$  and shut it off after  $V_{PP}$ .
  2. Do not allow  $V_{PP}$  to become +13 V or more including an overshoot.

PROM Read Mode Timing



8. PACKAGE INFORMATION

64PIN PLASTIC SHRINK DIP (750 mil)



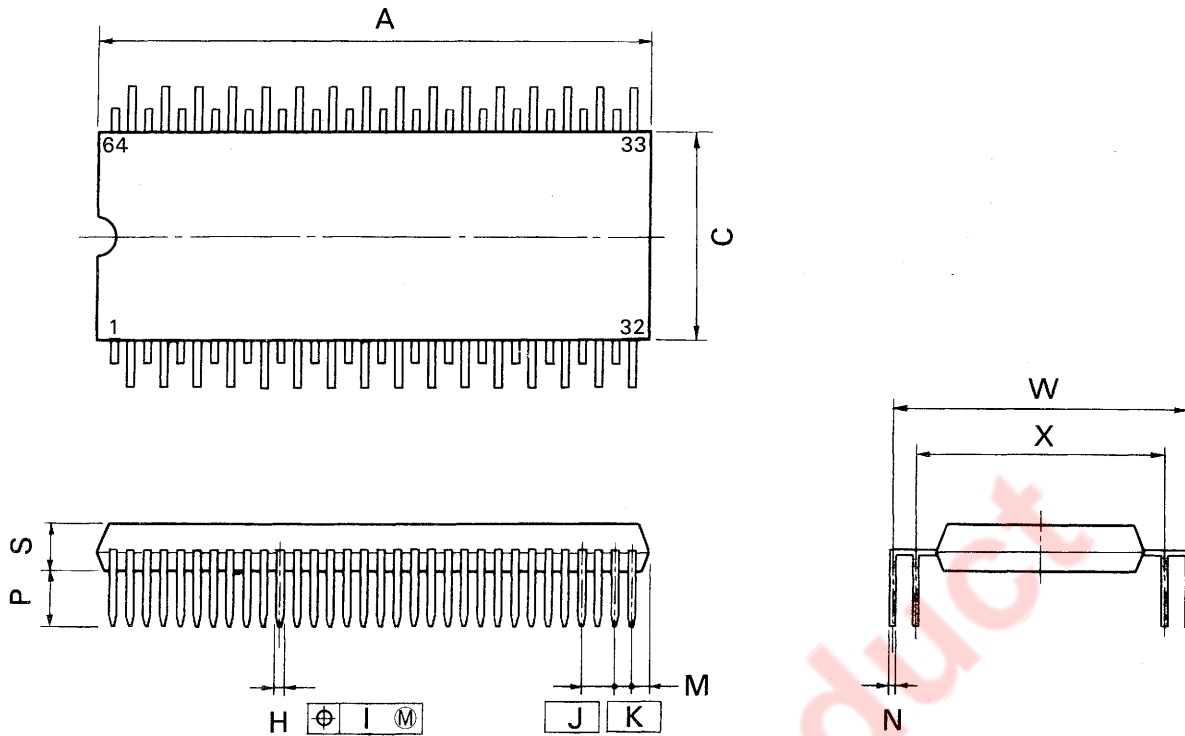
P64C-70-750A,C

NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS                              | INCHES                                      |
|------|--|---|
| A    | 58.68 MAX.                               | 2.311 MAX.                                  |
| B    | 1.78 MAX.                                | 0.070 MAX.                                  |
| C    | 1.778 (T.P.)                             | 0.070 (T.P.)                                |
| D    | 0.50 ±0.10                               | 0.020 <sup>+0.004</sup> / <sub>-0.005</sub> |
| F    | 0.9 MIN.                                 | 0.035 MIN.                                  |
| G    | 3.2 ±0.3                                 | 0.126 ±0.012                                |
| H    | 0.51 MIN.                                | 0.020 MIN.                                  |
| I    | 4.31 MAX.                                | 0.170 MAX.                                  |
| J    | 5.08 MAX.                                | 0.200 MAX.                                  |
| K    | 19.05 (T.P.)                             | 0.750 (T.P.)                                |
| L    | 17.0                                     | 0.669                                       |
| M    | 0.25 <sup>+0.10</sup> / <sub>-0.05</sub> | 0.010 <sup>+0.004</sup> / <sub>-0.003</sub> |
| N    | 0.17                                     | 0.007                                       |

64 PIN PLASTIC QUIP



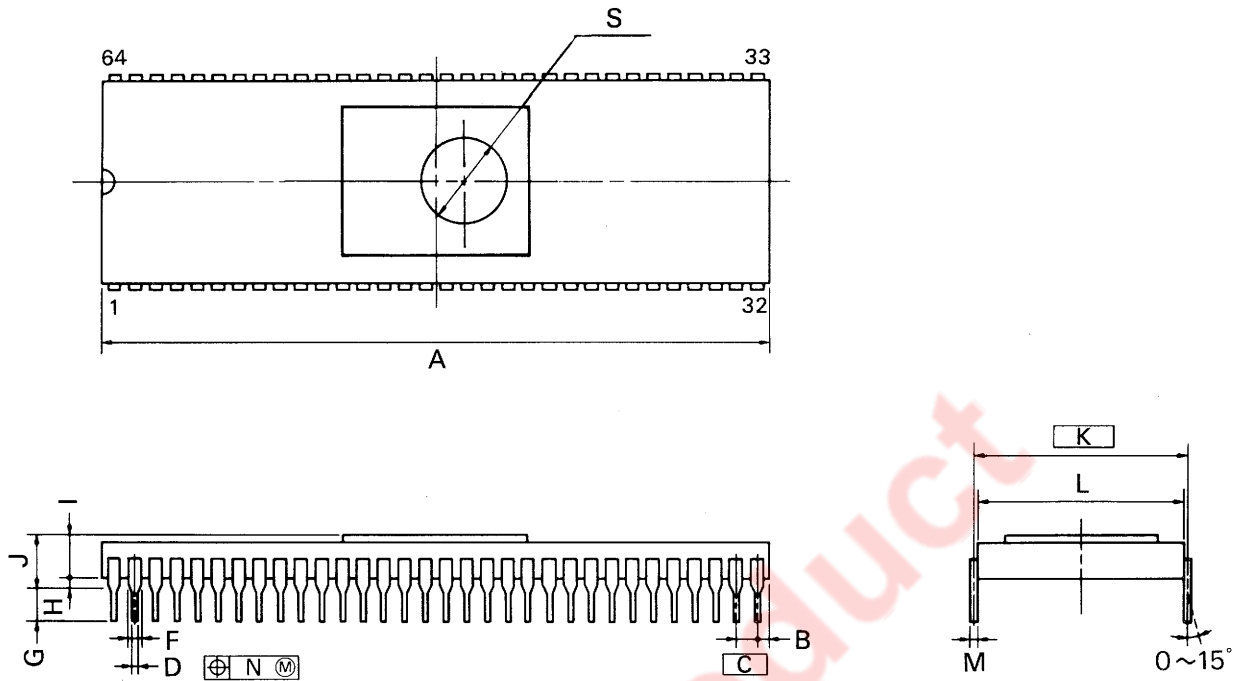
P64GQ-100-36

**NOTE**

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS            | INCHES                  |
|------|------------------------|-------------------------|
| A    | 41.5 <sup>+0.2</sup>   | 1.634 <sup>+0.012</sup> |
| C    | 16.5                   | 0.650                   |
| H    | 0.50 <sup>±0.10</sup>  | 0.020 <sup>+0.004</sup> |
| I    | 0.25                   | 0.010                   |
| J    | 2.54 (T.P.)            | 0.100 (T.P.)            |
| K    | 1.27 (T.P.)            | 0.050 (T.P.)            |
| M    | 1.1 <sup>+0.25</sup>   | 0.043 <sup>+0.011</sup> |
| N    | 0.25 <sup>+0.02</sup>  | 0.010 <sup>+0.004</sup> |
| P    | 4.0 <sup>±0.3</sup>    | 0.157 <sup>+0.012</sup> |
| S    | 3.6 <sup>±0.1</sup>    | 0.142 <sup>+0.004</sup> |
| W    | 24.13 <sup>±1.05</sup> | 0.950 <sup>±0.042</sup> |
| X    | 19.05 <sup>±1.05</sup> | 0.750 <sup>±0.042</sup> |

64PIN CERAMIC SHRINK DIP (CERDIP) (WINDOW) (750 mil)



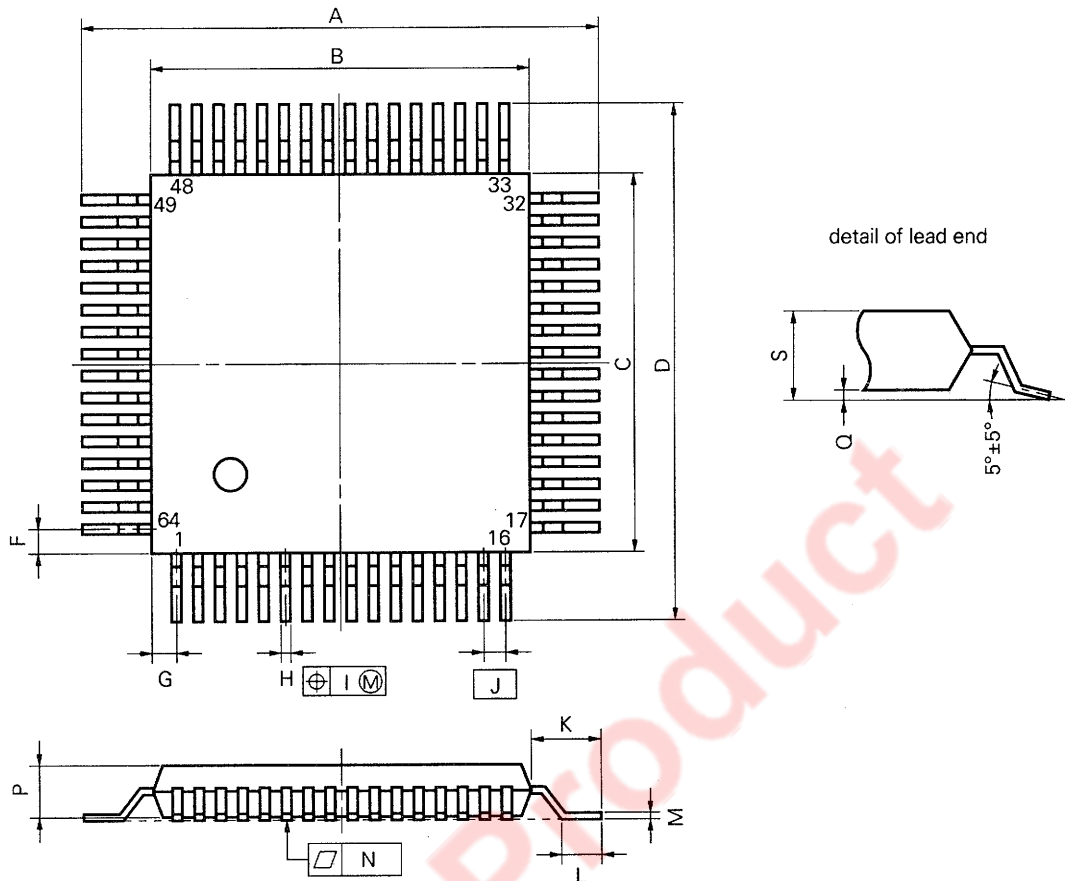
P64DW-70-750A1

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS  | INCHES                                      |
|------|--------------|---|
| A    | 58.68 MAX.   | 2.310 MAX.                                  |
| B    | 1.78 MAX.    | 0.070 MAX.                                  |
| C    | 1.778 (T.P.) | 0.070 (T.P.)                                |
| D    | 0.46 ±0.05   | 0.018 ±0.002                                |
| F    | 0.8 MIN.     | 0.031 MIN.                                  |
| G    | 3.5 ±0.3     | 0.138 ±0.012                                |
| H    | 1.0 MIN.     | 0.039 MIN.                                  |
| I    | 3.0          | 0.118                                       |
| J    | 5.08 MAX.    | 0.200 MAX.                                  |
| K    | 19.05 (T.P.) | 0.750 (T.P.)                                |
| L    | 18.8         | 0.740                                       |
| M    | 0.25 ±0.05   | 0.010 <sup>+0.002</sup> / <sub>-0.003</sub> |
| N    | 0.25         | 0.01  |
| S    | φ7.62        | φ0.300                                      |

64 PIN PLASTIC QFP (□14)



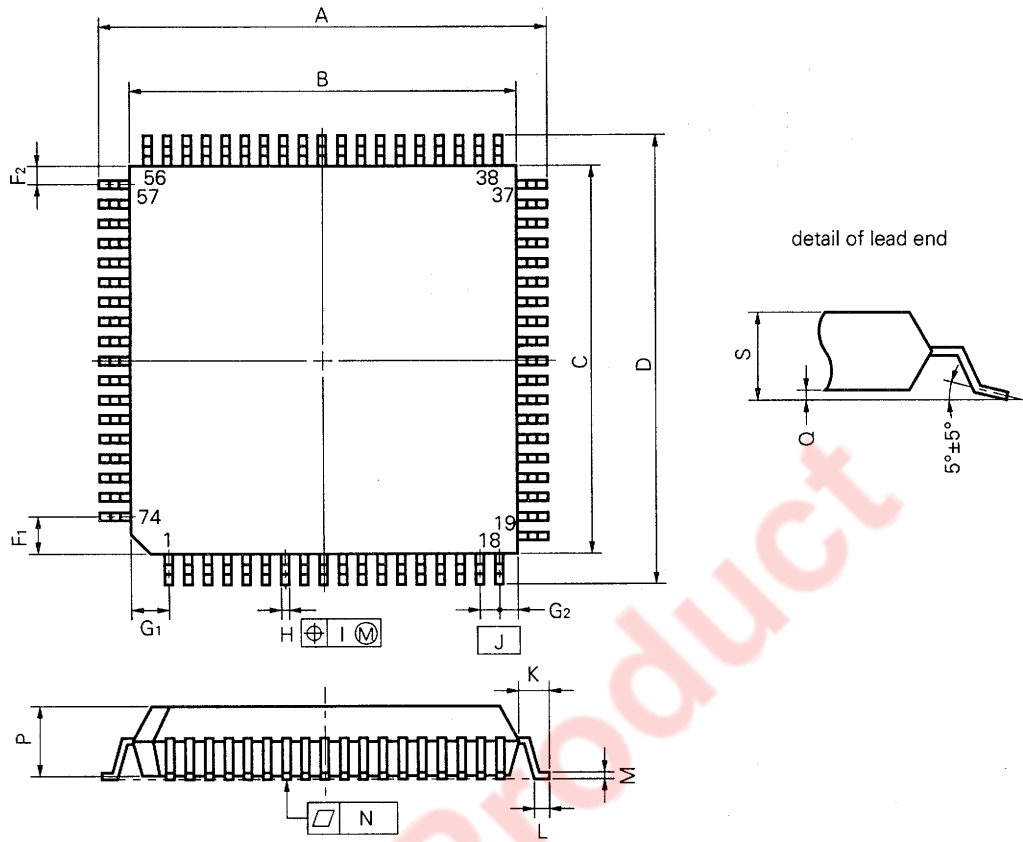
P64GC-80-AB8-3

**NOTE**

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|--|---|
| A    | 17.6±0.4                               | 0.693±0.016                               |
| B    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 17.6±0.4                               | 0.693±0.016                               |
| F    | 1.0                                    | 0.039                                     |
| G    | 1.0                                    | 0.039                                     |
| H    | 0.35±0.10                              | 0.014 <sup>+0.004</sup> <sub>-0.005</sub> |
| I    | 0.15                                   | 0.006                                     |
| J    | 0.8 (T.P.)                             | 0.031 (T.P.)                              |
| K    | 1.8±0.2                                | 0.071±0.008                               |
| L    | 0.8±0.2                                | 0.031 <sup>+0.009</sup> <sub>-0.008</sub> |
| M    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 2.55                                   | 0.100                                     |
| Q    | 0.1±0.1                                | 0.004±0.004                               |
| S    | 2.85 MAX.                              | 0.112 MAX.                                |

74 PIN PLASTIC QFP (□20)



S74GJ-100-5BJ-2

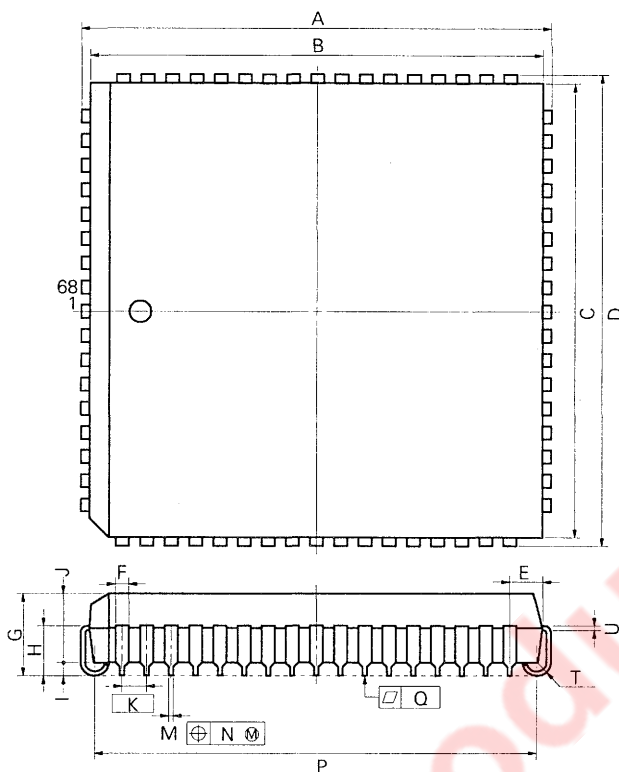
**NOTE**

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

| ITEM           | MILLIMETERS                            | INCHES                                    |
|----------------|--|---|
| A              | 23.2±0.4                               | 0.913 <sup>+0.017</sup> <sub>-0.016</sub> |
| B              | 20.0±0.2                               | 0.787 <sup>+0.009</sup> <sub>-0.008</sub> |
| C              | 20.0±0.2                               | 0.787 <sup>+0.009</sup> <sub>-0.008</sub> |
| D              | 23.2±0.4                               | 0.913 <sup>+0.017</sup> <sub>-0.016</sub> |
| F <sub>1</sub> | 2.0                                    | 0.079                                     |
| F <sub>2</sub> | 1.0                                    | 0.039                                     |
| G <sub>1</sub> | 2.0                                    | 0.079                                     |
| G <sub>2</sub> | 1.0                                    | 0.039                                     |
| H              | 0.40±0.10                              | 0.016 <sup>+0.004</sup> <sub>-0.005</sub> |
| I              | 0.20                                   | 0.008                                     |
| J              | 1.0 (T.P.)                             | 0.039 (T.P.)                              |
| K              | 1.6±0.2                                | 0.063±0.008                               |
| L              | 0.8±0.2                                | 0.031 <sup>+0.009</sup> <sub>-0.008</sub> |
| M              | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N              | 0.12                                   | 0.005                                     |
| P              | 3.7                                    | 0.146                                     |
| Q              | 0.1±0.1                                | 0.004±0.004                               |
| S              | 4.0 MAX.                               | 0.158 MAX.                                |



68 PIN PLASTIC QFJ (□ 950 mil)



P68L-50A1-2

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|--|---|
| A    | 25.2±0.2                               | 0.992±0.008                               |
| B    | 24.20                                  | 0.953                                     |
| C    | 24.20                                  | 0.953                                     |
| D    | 25.2±0.2                               | 0.992±0.008                               |
| E    | 1.94±0.15                              | 0.076 <sup>+0.007</sup> <sub>-0.006</sub> |
| F    | 0.6                                    | 0.024                                     |
| G    | 4.4±0.2                                | 0.173 <sup>+0.009</sup> <sub>-0.008</sub> |
| H    | 2.8±0.2                                | 0.110 <sup>+0.009</sup> <sub>-0.008</sub> |
| I    | 0.9 MIN.                               | 0.035 MIN.                                |
| J    | 3.4                                    | 0.134                                     |
| K    | 1.27 (T.P.)                            | 0.050 (T.P.)                              |
| M    | 0.40±1.0                               | 0.016 <sup>+0.004</sup> <sub>-0.005</sub> |
| N    | 0.12                                   | 0.005                                     |
| P    | 23.12±0.20                             | 0.910 <sup>+0.009</sup> <sub>-0.008</sub> |
| Q    | 0.15                                   | 0.006                                     |
| T    | R 0.8                                  | R 0.031                                   |
| U    | 0.20 <sup>+0.10</sup> <sub>-0.05</sub> | 0.008 <sup>+0.004</sup> <sub>-0.002</sub> |

**9. RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions for the surface mounting type, refer to the information document "Surface Mount Technology Manual" (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our salesman.

**Table 9-1 Surface Mounting Type Soldering Conditions**

**(1) μPD78P214GC-AB8 : 64-pin plastic QFP ( □ 14mm )**

| Soldering Method | Soldering Conditions  | Recommended Condition Symbol |
|------------------|---|------------------------------|
| Infrared reflow  | Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above)<br>Number of times: Once<br>Time limit: 2 days*1 (thereafter 16 hours prebaking required at 125°C)  | IR30-162-1*2                 |
| VPS              | Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above)<br>Number of times: Once<br>Time limit: 2 days*1 (thereafter 16 hours prebaking required at 125 °C) | VP15-162-1*2                 |
| Pin part heating | Pin part temperature: 300 °C max., Duration: 3 sec. max. (per device side)  | —                            |

**(2) μPD78P214GJ-5BJ : 74-pin plastic QFP ( □ 20mm )**

| Soldering Method | Soldering Conditions  | Recommended Condition Symbol |
|------------------|---|------------------------------|
| Infrared reflow  | Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above)<br>Number of times: Once<br>Time limit: 7 days*1 (thereafter 10 hours prebaking required at 125 °C) | IR30-107-1                   |
| VPS              | Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above)<br>Number of times: Once<br>Time limit: 7 days*1 (thereafter 10 hours prebaking required at 125 °C) | VP15-107-1                   |
| Pin part heating | Pin part temperature: 300°C max. Duration: 3 sec. max. (per device side)  | —                            |

**(3) μPD78P214L : 68-pin plastic QFJ ( □ 950mil )**

| Soldering Method | Soldering Conditions  | Recommended Condition Symbol |
|------------------|---|------------------------------|
| VPS              | Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above)<br>Number of times: Once<br>Time limit: 7 days*1 (thereafter 10 hours prebaking required at 125 °C) | VP15-107-1                   |
| Pin part heating | Pin part temperature: 300 °C max. Duration: 3 sec. max. (per device side)   | —                            |

- \* 1. For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65% RH.
- 2. This condition is not applicable to the "K" specification product.

**Note Use of more than one soldering method should be avoided (except in the case of pin part heating).**

**Table 9-2 Insert Type Soldering Conditions**

- μPD78P214CW : 64-pin plastic shrink DIP(750mil)**
- μPD78P214DW : 64-pin ceramic shrink DIP (CERDIP)(with window)(750mil)**
- μPD78P214GQ-36 : 64-pin plastic QUIP**

| Soldering Method                   | Soldering Conditions   |
|------------------------------------|--|
| Wave soldering<br>(lead part only) | Solder bath temperature: 260 °C max., Duration: 10 sec. max. |
| Pin part heating                   | Pin part temperature: 260 °C max., Duration: 10 sec. max.    |

**Note** Ensure that the application of wave soldering is limited to the lead part and no solder touches the main unit directly.

**Notification**

**A version of this product with improved recommended soldering conditions is available. For details (improvements such as infrared reflow peak temperature extension (235°C), number of times : twice, relaxation of time limit), contact NEC sales personnel.**

EOL Product

**APPENDIX. DEVELOPMENT TOOLS**

The following development tools are available for system development using μPD78P214.

For development tools manufactured by a third party, see the "78K/II Series Development Tools Selection Guide (EF-2)".

**Hardware (1/2)**

|   |  |
|---|--|
| IE-78240-R-A  | <p>The IE-78240-R-A is a functionally enhanced version of the IE-78210-R and IE-78240-R, and is an in-circuit emulator for use with the entire μPD78214 series. It can be used when a PC-9800 series or IBM PC/AT™ model is used as the host machine. The separately available screen debugger and device file are required, and in combination with these it is possible to perform debugging at the C language or structured assembly language source program level. More efficient debugging and program testing is possible through simultaneous data access and program fetch trace and C0 coverage functions, etc. If the user already has an IE-78210-R or IE-78240-R, this can be used in the same way as the IE-78240-R-A by purchasing a separately available board (IE-78200-R-BK).</p> |
| IE-78240-R<br>IE-78210-R*   | <p>IE-78210-R and IE-78240-R are in-circuit emulators which can be used in common with the μPD78214 series. Debugging is performed by connecting a host machine or a console. Connecting it to a host machine permits a symbolic debugging, object file transfer to a host machine, and efficient debugging. This tool incorporates RS-232-C serial interface for 2 channels, which enables connection to the PG-1500 PROM programmer. The IE-78240-R also executes the high-speed down loading of an object file and symbol file via Centronics I/F.</p>  |
| IE-78240-R-EM<br>IE-78210-R-EM*<br>IE-78200-R-EM<br>IE-78200-R-BK | <p>This board upgrades an in-circuit emulator for the 75X series and 78K series to the IE-78210-R, IE-78240-R or IE-78240-R-A. For details, refer to "System upgrade" described later.</p>   |
| EP-78210CW*<br>EP-78240CW-R                                       | <p>This is an emulation probe for μPD78P214CW. EP-78240CW-R is the same product as EP-78210CW except its longer cable length.</p>  |
| EP-78210GC*<br>EP-78240GC-R                                       | <p>This is an emulation probe for μPD78P214GC-AB8. It should be used together with EV-9200GC-64. EP-78240GC-R is the same product as EP-78210GC except its longer cable length.</p>  |
| EP-78210GJ*   | <p>This is an emulation probe for μPD78P214GJ-5BJ. It should be used together with either EP-78210L, EP-78240LP-R or EV-9200G-74.</p>  |
| EP-78240GJ-R  | <p>This is an emulation probe for μPD78P214GJ-5BJ. It should be used together with EV-9200G-74. Unlike the EP-78210GJ, this is an integral probe, allowing easy operation.</p>   |
| EP-78210GQ*<br>EP-78240GQ-R                                       | <p>This is an emulation probe for μPD78P214GQ-36. EP-78240GQ-R is the same product as EP-78210GQ except its longer cable length.</p>   |
| EP-78210L*<br>EP-78240LP-R  | <p>This is an emulation probe for μPD78P214L. EP-78240LP-R is the same product as EP-78210L except its longer cable length.</p>  |

\* No longer manufactured.

**Remarks** The cables EP-78210GJ, EP-78210GC, EP-78240GC-R, EP-78240GJ-R are respectively provided with one piece of the socket EV-9200GC-74 or EV-9200GC-64.

## Hardware (2/2)

|              |  |
|--------------|--|
| EV-9200G-74  | This is a socket mounted on the board of user system which is made for $\mu$ PD78P214GJ-5BJ. It should be used together with either EP-78210GJ or EP-78240GJ-R.  |
| EV-9200GC-64 | This is a socket mounted on the board of user system which is made for $\mu$ PD78P214GC-AB8. It should be used together with either EP-78210GC or EP-78240GC-R.  |
| ★ PG-1500    | PROM programmer which enables a single-chip microcomputer with on-chip PROM to be programmed in stand-alone mode or by operations from a host machine by connection of the supplied board and separately available programmer adapter. Typical PROMs from 256K bits to 4M bits can also be programmed. |
| PA-78P214CW  | This is a PROM programmer adapter for $\mu$ PD78P214CW/78P214DW, and should be used in combination with PG-1500, etc.  |
| PA-78P214GC  | This is a PROM programmer adapter for $\mu$ PD78P214GC-AB8 and should be used in combination with PG-1500, etc.  |
| PA-78P214GJ  | This is a PROM programmer adapter for $\mu$ PD78P214GJ-5BJ and should be used in combination with PG-1500, etc.  |
| PA-78P214GQ  | This is a PROM programmer adapter for $\mu$ PD78P214GQ-36 and should be used in combination with PG-1500, etc.   |
| PA-78P214L   | This is a PROM programmer adapter for $\mu$ PD78P214L and should be used in combination with PG-1500, etc.   |

\* No longer manufactured.

**Remarks** EV-9200GC-74 or EV-9200GC-64 is available by the 5- piece set (ordered in units of a set).

Software

① Language Processing Software (1/2)

| 78K/II series<br>relocatable assembler<br>(RA78K/II) | <p>A relocatable assembler package which can be used by the entire 78K/II series. Because it is a relocatable assembler with a macro function, development efficiency can be improved.</p> <p>A structured assembler which can describe explicitly the program control structure is also provided. Thus program productivity and maintainability can be improved.</p>  |                                      |                            |               |
|--|--|--------------------------------------|----------------------------|---------------|
|  | Host Machine   | OS                                   | Supply Medium              | Ordering Code |
|  | PC-9800 series   | MS-DOS™<br>(Ver.3.30 to Ver.5.00A*3) | 8-inch 2D *1               | μS5A1RA78K2   |
|  |  |                                      | 5-inch 2HD                 | μS5A10RA78K2  |
|  |  |                                      | 3.5-inch 2HD               | μS5A13RA78K2  |
|  | IBM PC / AT  | PC DOS™<br>(Ver.3.1)                 | 5-inch 2D *2               | μS7B11RA78K2  |
|  |  |                                      | 5-inch 2HC                 | μS7B10RA78K2  |
|  | HP9000 series 300™   | HP-UX™<br>(rel.7.05B)                | Cartridge tape<br>(QIC-24) | μS3H15RA78K2  |
| SPARKstation™  | Sun OS™<br>(rel.4.1.1)   | μS3K15RA78K2                         |                            |               |
| EWS-4800 series™<br>(RISC)                           | EWS-UX/V™<br>(rel.4.0)   | S3M15RA78K2                          |                            |               |
| 78K/II series<br>C compiler<br>(CC78K/II)            | <p>A C compiler which can be used by the entire 78K/II series. Its language specification is compliant with ANSI, thus programs can be converted into ROM. It is provided with such functions as special function register manipulation, bit manipulation, variables using short direct addressing, interrupt control functions. Use of these function allows efficient programming and higher object efficiency to be achieved.</p> <p>It is also provided with start-up routine sample programs and standard function object libraries.</p> <p>Use of this compiler requires 78K/II series relocatable assembler (RA78K/II).</p> |                                      |                            |               |
|  | Host Machine   | OS                                   | Supply Medium              | Ordering Code |
|  | PC-9800 series   | MS-DOS<br>(Ver.3.30 to Ver.5.00A*3)  | 5-inch 2HD                 | μS5A10CC78K2  |
|  |  |                                      | 3.5-inch 2HD               | μS5A13CC78K2  |
|  | IBM PC / AT  | PC DOS<br>(Ver.3.1)                  | 5-inch 2D *2               | μS7B11CC78K2  |
|  |  |                                      | 5-inch 2HC                 | μS7B10CC78K2  |
|  | HP9000 series 300  | HP-UX<br>(rel.7.05B)                 | Cartridge tape<br>(QIC-24) | μS3H15CC78K2  |
|  | SPARKstation   | Sun OS<br>(rel.4.1.1)                |                            | μS3K15CC78K2  |
| EWS-4800 series<br>(RISC)                            | EWS-UX/V<br>(rel.4.0)  | S3M15CC78K2                          |                            |               |

★  
★  
★

★  
★  
★

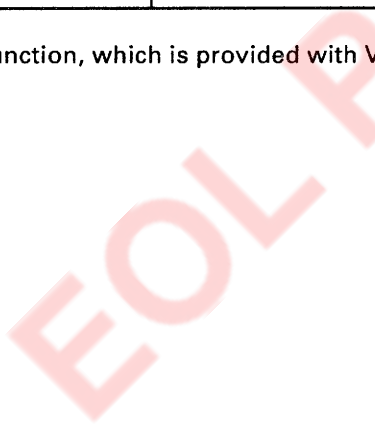
- \* 1. No longer available for purchase with 8-inch 2D. 5-inch 2HD or 3.5-inch 2HD should be selected instead. If it has been purchased with 8-inch 2D, the 5-inch 2HD will be sent in the next version upgrade.
- 2. The 5-inch 2D version is no longer sold. Please note that users who have previously purchased software in 5-inch 2D format will be sent future version upgrades in 5-inch 2HC format.
- 3. The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.

① Language Processing Software (2/2)

| 78K/II series<br>C compiler<br>library source file<br>(CC78K/II-L) | A source program of a library which belongs to the CC78K/II. Required to improve (to adapt more to the user specifications.) the library. |                                    |                            |                |
|--|---|------------------------------------|----------------------------|----------------|
|  | Host Machine  | OS                                 | Supply Medium              | Ordering Code  |
|  | PC-9800 series  | MS-DOS<br>(Ver.3.30 to Ver.5.00A*) | 5-inch 2HD                 | μS5A10CC78K2-L |
|  |   |                                    | 3.5-inch 2HD               | μS5A13CC78K2-L |
|  | IBM PC / AT   | PC DOS<br>(Ver.3.1)                | 5-inch 2HC                 | μS7B10CC78K2-L |
|  | HP9000 series 300   | HP-UX<br>(rel.7.05B)               | Cartridge tape<br>(QIC-24) | μS3H15CC78K2-L |
|  | SPARKstation  | Sun OS<br>(rel.4.1.1)              |                            | μS3K15CC78K2-L |
| EWS-4800 series<br>(RISC)  | EWS-UX/V<br>(rel.4.0)   | μS3M15CC78K2-L                     |                            |                |

- ★
- ★
- ★

\* The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.



② In-Circuit Emulator Software

|  |   |                                     |                   |                   |
|--|---|-------------------------------------|-------------------|-------------------|
| Screen debugger<br>(SD78K/II)                            | <p>Program which controls the 78K/II series in-circuit emulator. Used in conjunction with the device file (DF78210).<br/>Using the IE-78240-R-A or an in-circuit emulator system-upgraded to equivalence with the IE-78240-R-A , can be used with a PC-9800 series or IBM PC/AT host machine.<br/>This software enables highly efficient debugging to be performed through functions for source program level debugging of programs written in C language, structured assembly language or assembly language, and host machine screen splitting for the simultaneous display of various kinds of information.</p> |                                     |                   |                   |
|  | Host Machine  | OS                                  | Supply Medium     | Ordering Code     |
|  | PC-9800 series  | MS-DOS<br>(Ver.3.30 to Ver.5.00A*1) | 5-inch 2HD        | μS5A10SD78K2      |
|  |   |                                     | 3.5-inch 2HD      | μS5A13SD78K2      |
| IBM PC / AT  | PC DOS<br>(Ver.3.1)   | 5-inch 2HC                          | μS7B10SD78K2*2    |                   |
| Device file<br>(DF78210)                                 | <p>Required to perform μPD78214 series debugging in conjunction with the screen debugger (SD78K/II).</p>  |                                     |                   |                   |
|  | Host Machine  | OS                                  | Supply Medium     | Ordering Code     |
|  | PC-9800 series  | MS-DOS<br>(Ver.3.30 to Ver.5.00A*1) | 5-inch 2HD        | μS5A10DF78210     |
|  |   |                                     | 3.5-inch 2HD      | μS5A13DF78210     |
| IBM PC / AT  | PC DOS<br>(Ver.3.1)   | 5-inch 2HC                          | μS7B10DF78210*2   |                   |
| IE-78210-R<br>IE-78210-R-EM control program<br>(IE78210) | <p>A program which controls the IE-78210 from the host machine. Its automatic command execution capability allows more efficient debugging.</p>   |                                     |                   |                   |
|  | Host Machine  | OS                                  | Supply Medium     | Ordering Code     |
|  | PC-9800 series  | MS-DOS<br>(Ver.3.30 to Ver.5.00A*1) | 8-inch 2D *3      | μS5A11E78210-P01  |
|  |   |                                     | 5-inch 2HD        | μS5A10IE78210-P01 |
|  |   |                                     | 3.5-inch 2HD      | μS5A13IE78210     |
| IBM PC / AT  | PC DOS<br>(Ver.3.1)   | 5-inch 2D *4                        | μS7B11IE78210-P02 |                   |
|  |   | 5-inch 2HC                          | μS7B10IE78210     |                   |
| IE-78240-R<br>IE-78240-R-EM control program<br>(IE78240) | <p>A program which controls the IE-78240 from the host machine. Its automatic command execution capability allows more efficient debugging.</p>   |                                     |                   |                   |
|  | Host Machine  | OS                                  | Supply Medium     | Ordering Code     |
|  | PC-9800 series  | MS-DOS<br>(Ver.3.30 to Ver.5.00A*1) | 8-inch 2D *3      | μS5A11E78240      |
|  |   |                                     | 5-inch 2HD        | μS5A10IE78240     |
|  |   |                                     | 3.5-inch 2HD      | μS5A13IE78240     |
| IBM PC / AT  | PC DOS<br>(Ver.3.1)   | 5-inch 2D *4                        | μS7B11IE78240     |                   |
|  |   | 5-inch 2HC                          | μS7B10IE78240     |                   |

★

★

★

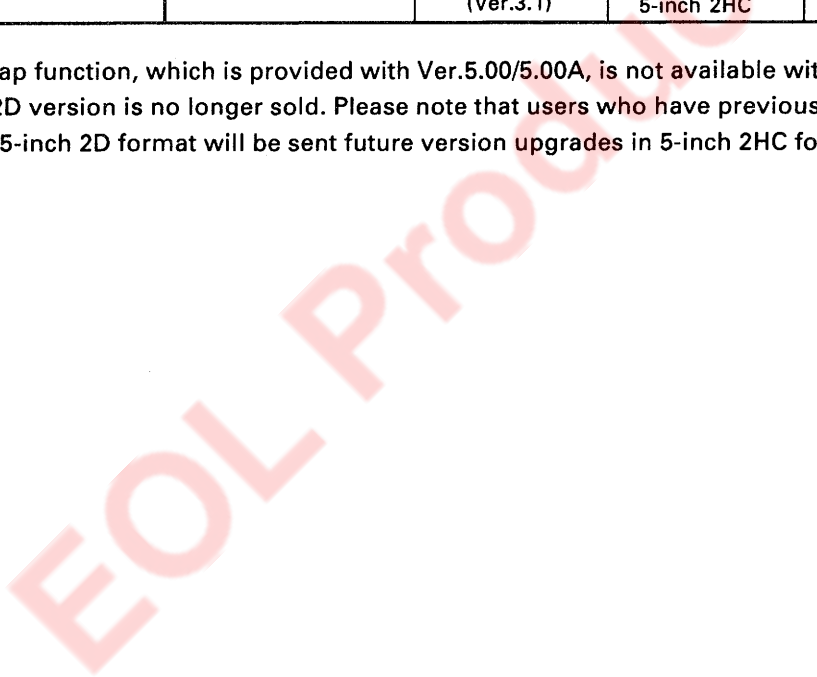


- \* 1. The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.
- 2. Under development.
- 3. No longer available for purchase with 8-inch 2D. 5-inch 2HD or 3.5-inch 2HD should be selected instead. If it has been purchased with 8-inch 2D, the 5-inch 2HD will be sent in the next version upgrade.
- 4. The 5-inch 2D version is no longer sold. Please note that users who have previously purchased software in 5-inch 2D format will be sent future version upgrades in 5-inch 2HC format.

③ PROM Programmer Software

| PG-1500<br>controller | Controls the PG-1500 on the host machine, with the PG-1500 and host machine connected via a serial or parallel interface. |  |               |               |
|-----------------------|---|--|---------------|---------------|
|                       | Host Machine  | OS                                     | Supply Medium | Ordering Code |
|                       | PC-9800<br>series   | MS-DOS<br>(Ver.3.30 to<br>Ver.5.00A*1) | 5-inch 2HD    | μS5A10PG1500  |
|                       |   |  | 3.5-inch 2HD  | μS5A13PG1500  |
|                       | IBM PC / AT   | PC DOS<br>(Ver.3.1)                    | 5-inch 2D *2  | μS7B11PG1500  |
| 5-inch 2HC            |   |  | μS7B10PG1500  |               |

- \* 1. The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.
- 2. The 5-inch 2D version is no longer sold. Please note that users who have previously purchased software in 5-inch 2D format will be sent future version upgrades in 5-inch 2HC format.



**System Upgrade from Another In-Circuit Emulator**

① **System upgrade to IE-78240-R-A**

| Current Emulator   | IE-Group No. | Boards to be Purchased           | Remarks  |
|--|--------------|----------------------------------|--|
| IE-78230-R-A<br>IE-78140-R   | 1            | IE-78240-R-EM                    | —  |
| IE-78240-R   | 2            | IE-78200-R-BK                    | —  |
| IE-78112-R*1<br>IE-78220-R*1<br>IE-78310-R*1<br>IE-78310A-R  | 3            | IE-78200-R-BK<br>IE-78240-R-EM*2 | The high-speed download function cannot be used.<br>If you also have an IE Group 1/2/4 in-circuit emulator, a system upgrading based on the IE Group 1/2/4 in-circuit emulator is recommended.<br>If you also have an IE Group 1 in-circuit emulator, the IE-78200-R-BK is not required (the IE Group 1 in-circuit emulator contains an IE-78200-R-BK and therefore this board can be used). |
| IE-75000-R<br>IE-78000-R<br>IE-78130-R<br>IE-78230-R<br>IE-78320-R*1<br>IE-78327-R<br>IE-78330-R<br>IE-78350-R<br>IE-78600-R | 4            | IE-78200-R-BK<br>IE-78240-R-EM   | If you also have an IE Group 1, in-circuit emulator, the IE-78200-R-BK is not required (the IE Group 1 in-circuit emulator contains an IE78200-R-BK, and therefore this board can be used).  |
| IE-78210-R*1   | 5            | IE-78200-R-BK                    | The high-speed download function cannot be used.   |

- \* 1. No longer manufactured and not available for purchase.
- 2. When performing emulation of the μPD78214 series, if you have already the IE-78210-R-EM\*1, the IE-78240-R-EM is not required.

② System upgrade to IE-78240-R

| Current Emulator   | IE-Group No. | Boards to be Purchased           | Remarks  |
|--|--------------|----------------------------------|--|
| IE-78112-R*1<br>IE-78210-R*1<br>IE-78220-R*1   | 1            | IE-78240-R-EM*2                  | The high-speed download function cannot be used.<br>If you also have an IE of Group 4, use of IE cabinet of Group 4 is recommended.  |
| IE-78130-R<br>IE-78230-R   | 2            | IE-78240-R-EM                    | —  |
| IE-78310-R*1<br>IE-78310A-R  | 3            | IE-78200-R-EM<br>IE-78240-R-EM*2 | The high-speed download function cannot be used.<br>If you have an IE of Group 1, the IE-7800-R-EM is not required (the IE of Group 1 contains an IE-78200-R-EM and therefore this board can be used). |
| IE-75000-R<br>IE-78000-R<br>IE-78320-R*1<br>IE-78327-R<br>IE-78330-R<br>IE-78350-R<br>IE-78600-R | 4            | IE-78200-R-EM<br>IE-78240-R-EM   | If you have an IE of Group 1, the IE-78200-R-EM is not required (the IE of Group 1 contains an IE-78200-R-EM, and therefore this board can be used).   |
| IE-78140-R<br>IE-78230-R-A   | 5            | IE-78200-R-EM<br>IE-78240-R-EM   | A system upgrading to IE-78240-R-A equivalence is recommended.   |

- \* 1. No longer manufactured and not available for purchase.
- 2. When performing emulation of the μPD78214 series, if you have already the IE-78210-R-EM\*1, the IE-78240-R-EM is not required.

★ ③ System upgrade to IE-78210-R\*1

| Current Emulator   | IE-Group No. | Boards to be Purchased           | Remarks  |
|--|--------------|----------------------------------|--|
| IE-78112-R*1<br>IE-78220-R*1   | 1            | IE-78210-R-EM*2                  | —  |
| IE-78310-R*1<br>IE-78310A-R  | 2            | IE-78200-R-EM<br>IE-78210-R-EM*1 | If you have an IE of Group 1, the IE-7800-R-EM is not required (the IE of Group 1 contains an IE-78200-R-EM and therefore this board can be used). |
| IE-75000-R<br>IE-78000-R<br>IE-78130-R<br>IE-78140-R<br>IE-78230-R<br>IE-78230-R-A<br>IE-78320-R*1<br>IE-78327-R<br>IE-78330-R<br>IE-78350-R<br>IE-78600-R | 3            | —                                | A system upgrading to IE-78210-R is not possible.<br>A system upgrading to IE-78240-R is recommended.  |

- \* 1. No longer manufactured and not available for purchase.
- 2. IE-78210-R-EM no longer manufactured and not available for purchase. Therefore, if you do not have the IE-78210-R-EM, a system upgrade to IE-78240-R or IE-78240-R-A is recommended.

Built-In Software

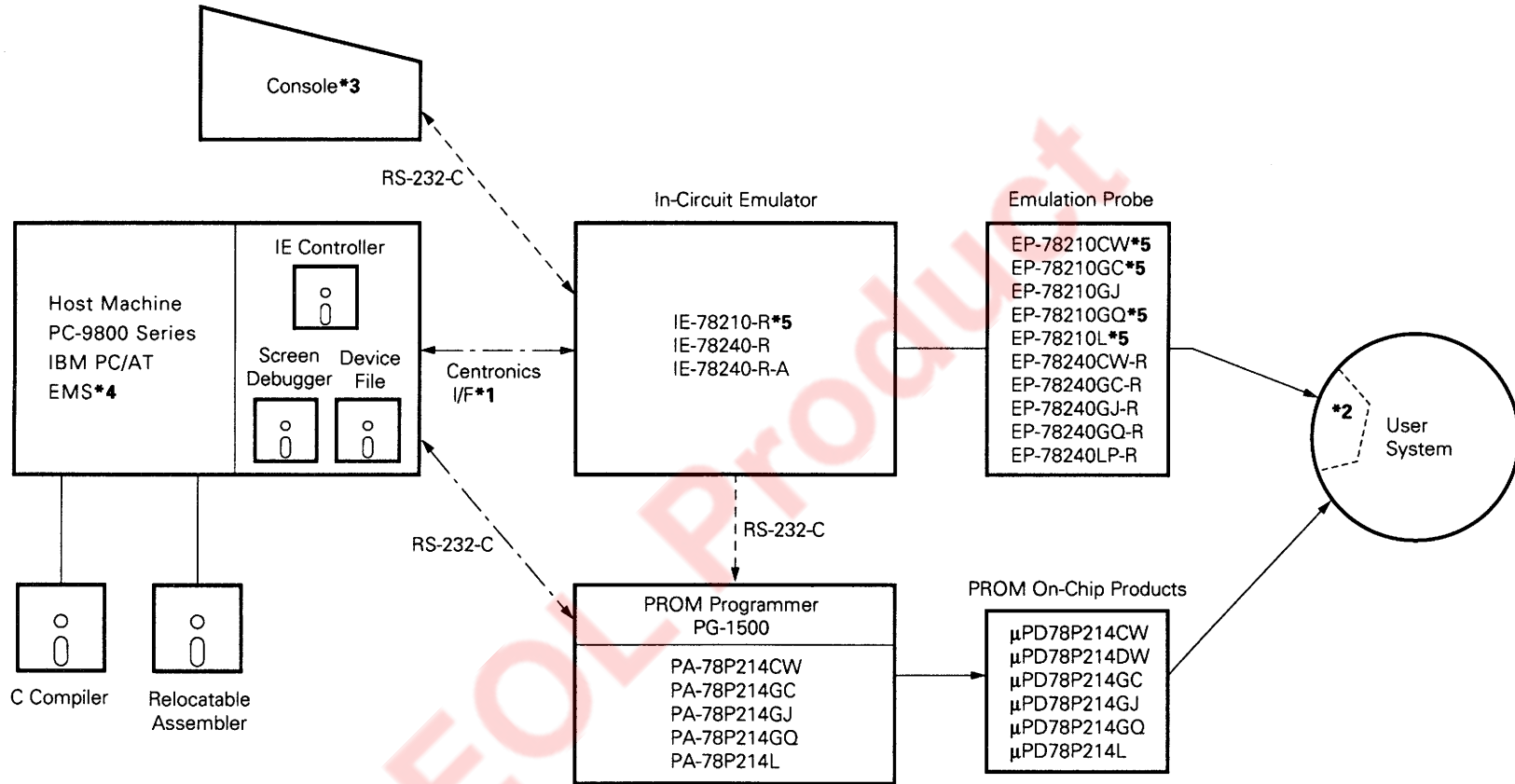


① Fuzzy Inference Development Support System

|   |   |                                |               |               |
|---|---|--------------------------------|---------------|---------------|
| Fuzzy knowledge data creation tool (FE9000) | A program to support fuzzy knowledge data (fuzzy rules and membership function) input/editing and evaluation (simulation).                |                                |               |               |
|   | Host Machine  | OS                             | Supply Medium | Ordering Code |
|   | PC-9800 series  | MS-DOS (Ver.3.10 to Ver.3.30C) | 5-inch 2HD    | μS5A10FE9000  |
|   |   |                                | 3.5-inch 2HD  | μS5A13FE9000  |
| IBM PC / AT                                 | PC DOS (Ver.3.1)  | 5-inch 2HC                     | μS7B10FE9000  |               |
| Translator (FT9080)                         | A program to convert the fuzzy knowledge data obtained by the fuzzy knowledge data creation tool to an RA78K/II assembler source program. |                                |               |               |
|   | Host Machine  | OS                             | Supply Medium | Ordering Code |
|   | PC-9800 series  | MS-DOS (Ver.3.10 to Ver.3.30C) | 5-inch 2HD    | μS5A10FT9080  |
|   |   |                                | 3.5-inch 2HD  | μS5A13FT9080  |
| IBM PC / AT                                 | PC DOS (Ver.3.1)  | 5-inch 2HC                     | μS7B10FT9080  |               |
| Fuzzy inference module (FI78k/II)           | A program to execute fuzzy inference. Executes fuzzy inference by linking with the fuzzy knowledge data converted by the translator.      |                                |               |               |
|   | Host Machine  | OS                             | Supply Medium | Ordering Code |
|   | PC-9800 series  | MS-DOS (Ver.3.10 to Ver.3.30C) | 5-inch 2HD    | μS5A10FI78K2  |
|   |   |                                | 3.5-inch 2HD  | μS5A13FI78K2  |
| IBM PC / AT                                 | PC DOS (Ver.3.1)  | 5-inch 2HC                     | μS7B10FI78K2  |               |
| Fuzzy debugger (FD78K/II)*                  | A support software to evaluate and adjust the fuzzy knowledge data at the hardware level using an in-circuit emulator.                    |                                |               |               |
|   | Host Machine  | OS                             | Supply Medium | Ordering Code |
|   | PC-9800 series  | MS-DOS (Ver.3.10 to Ver.3.30C) | 5-inch 2HD    | μS5A10FD78K2  |
|   |   |                                | 3.5-inch 2HD  | μS5A13FD78K2  |
| IBM PC / AT                                 | PC DOS (Ver.3.1)  | 5-inch 2HC                     | μS7B10FD78K2  |               |

\* Under development

Development Tool Configuration ★



- \* 1. It is used when a file is transferred at high speed (down-loading).      - - - - : When using by connecting with a host machine
- 2. EV-9200GC-64, EV-9200G-74      - - - - : Using the IE as stand-alone by connecting with a console
- 3. Only when the IE-78240-R is used
- 4. The EWS used are HP9000 series 300, SUN4/3900 and EWS-4800/200 series. The EWS cannot be connected to an in-circuit emulator.
- 5. Not available for purchase

[MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

The devices listed in this document are not suitable for use in aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. If customers intend to use NEC devices for above applications or they intend to use "Standard" quality grade NEC devices for applications not intended by NEC, please contact our sales people in advance.

Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

M4 92.6

**QTOP is a trademark of NEC Corporation.**

**EWS-4800 series and EWS-UX/V are trademarks of NEC Corporation.**

**MS-DOS is a trademark of MicroSoft Corporation.**

**PC/AT, PC DOS is a trademark of IBM Corporation.**

**SPARCstation is a trademark of SPARC International, Inc.**

**Sun OS is a trademark of Sun Microsystems Corporation.**

**HP9000 series 300 and HP-UX are trademarks of Hewlett-Packard Company.**