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RENESAS

MOS INTEGRATED CIRCUIT

μPD78P064

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P064 is a product of μPD78064 subseries in 78K/0 series, in which the on-chip mask ROM of the μPD78064 is replaced by one-time PROM or EPROM.

As program write by user is possible, the μPD78P064 is best suited for evaluation, short-run and multiple-device production, and early rise upon system development.

Functions are described in detail in the following User's Manuals, which should be read when carrying out design work.

μPD78064, 78064Y Subseries User's Manual : U10105E
78K/0 Series User's Manual Instruction : U12326E

FEATURES

- Pin compatible with mask ROM products (except the V_{PP} pin)
- Internal PROM: 32K bytes[Note]
  - μPD78P064KL-T : Reprogrammable (ideal for system evaluation)
  - μPD78P064GC, 78P064GF: Programmable once only (ideal for small-scale production)
- Internal high-speed RAM: 1024 bytes[Note]
- LCD display RAM: 40 × 4 bits
- Operable in the same supply voltage as mask ROM products (V_{DD} = 2.0 to 6.0 V)
- Corresponding to QTOP™ microcontrollers

Note Internal PROM and internal high-speed RAM capacities can be changed by memory size switching register (IMS).

Remarks 1. For the differences between PROM products and mask ROM products, refer to **1. DIFFERENCES BETWEEN μPD78P064 AND MASK ROM PRODUCTS**.

2. A QTOP microcontroller is the general name for a single-chip microcontroller with one-time PROM for which program writing, marking, screening, and verifying are completely supported by NEC.

In this document, "PROM" is used in parts common to one-time PROM products and EPROM products.

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(Previous No. IC-3224)
Date Published August 1997 N
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

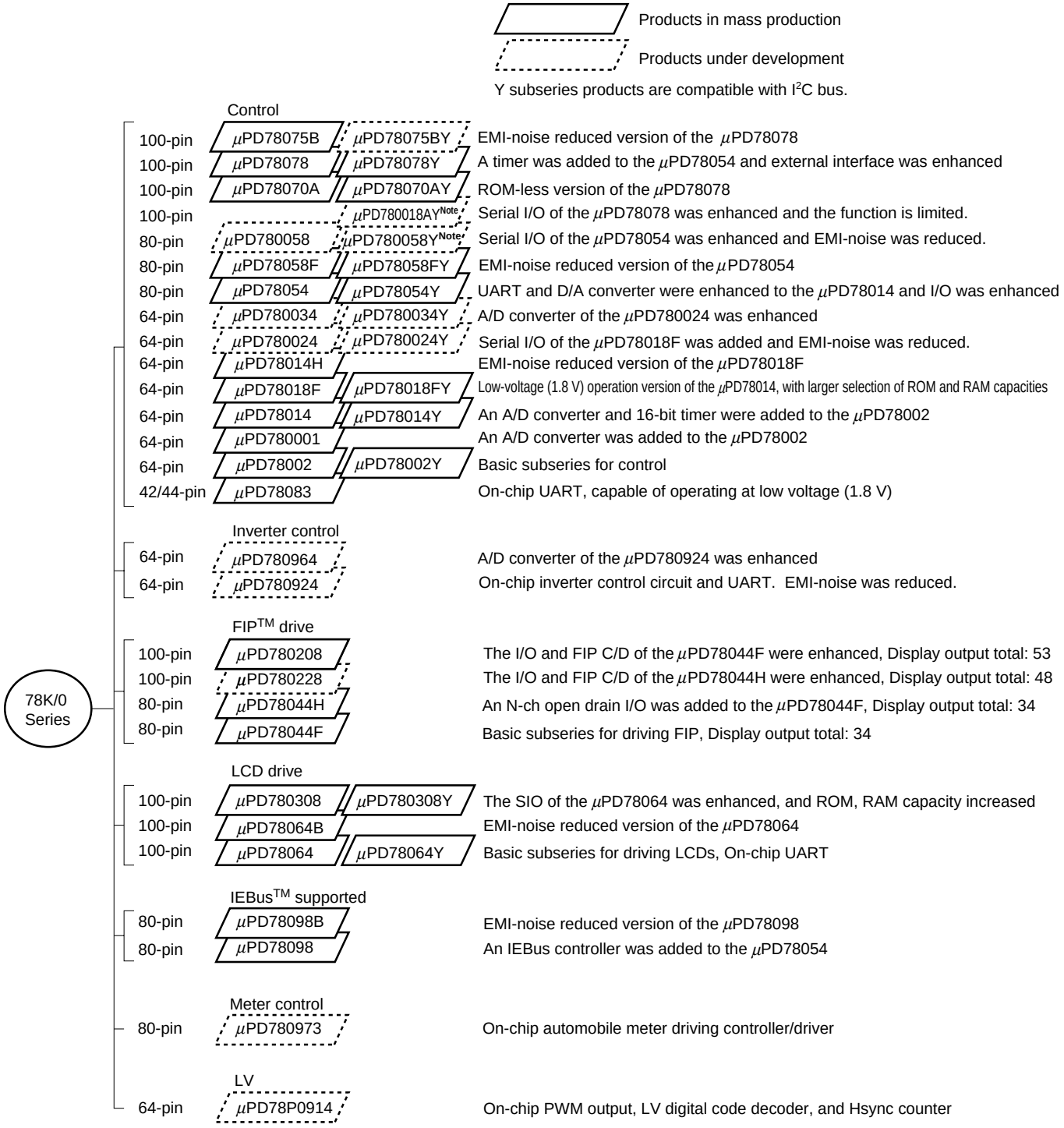
Part Number	Package	On-Chip ROM
μPD78P064GC-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	One-time PROM
★ μPD78P064GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	One-time PROM
μPD78P064GF-3BA	100-pin plastic QFP (14 × 20 mm)	One-time PROM
μPD78P064KL-T[Note]	100-pin ceramic WQFN (14 × 20 mm)	EPROM

Note Under development

Caution The μPD78P064GC has two types of package. (Refer to 10. PACKAGE DRAWINGS). For the package suppliable to your device, consult NEC sales personnels.

★ 78K/0 SERIES DEVELOPMENT

The following shows the products organized according to usage. The names in the parallelograms are subseries names.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32K-40K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	88	1.8 V	○
	μPD78078	48K-60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24K-60K	2ch						2ch	3ch (time division UART: 1ch)	68	1.8 V	
	μPD78058F	48K-60K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16K-60K										2.0 V	
	μPD780034	8K-32K					–	8ch	–	3ch (UART: 1ch, time division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8ch	–					
	μPD78014H									2ch	53	1.8 V	
	μPD78018F	8K-60K											
	μPD78014	8K-32K										2.7 V	
	μPD780001	8K		–	–					1ch	39		–
	μPD78002	8K-16K			1ch		–				53		○
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
Inverter control	μPD780964	8K-32K	3ch	**Note**	–	1ch	–	8ch	–	2ch (UART: 2ch)	47	2.7 V	○
	μPD780924						8ch	–					
FIP drive	μPD780208	32K-60K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48K-60K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32K-48K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16K-40K								2ch			
LCD drive	μPD780308	48K-60K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time division UART: 1ch)	57	2.0 V	–
	μPD78064B	32K								2ch (UART: 1ch)			
	μPD78064	16K-32K											
IEBus supported	μPD78098	40K-60K	2ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	69	2.7 V	○
	μPD78098B	32K-60K											
Meter control	μPD780973	24K-32K	3ch	1ch	1ch	1ch	5ch	–	–	2ch (UART: 1ch)	56	4.5 V	–
LV	μPD78P0914	32K	6ch	–	–	1ch	8ch	–	–	2ch	54	4.5 V	○

Note 10-bit timer: 1 channel

FUNCTION DESCRIPTION

Item		Function
Internal memory		• PROM : 32 K bytes[Note 1] • RAM High-speed RAM : 1024 bytes[Note 1] LCD display RAM : 40 × 4 bits
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (when operating at 5.0 MHz)
	When subsystem clock is selected	122 μs (when operating at 32.768 kHz)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.
I/O ports [Include segment signal output dual-function pin]		Total : 57 • CMOS input : 2 • CMOS input/output : 55
A/D converter		• 8-bit resolution × 8 ch
LCD controller/driver		• Segment signal output : 40 max. • Common signal output : 4 max. • Bias : 1/2, 1/3, Bias switchable
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 ch • 3-wire serial I/O/UART mode selectable : 1 ch
Timer		• 16-bit timer/event counter : 1 ch • 8-bit timer/event counter : 2 ch • Watch timer : 1 ch • Watchdog timer : 1 ch
Timer output		3 pins (14-bit PWM output enable : 1 pin)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (when operating at main system clock 5.0 MHz), 32.768 kHz (when operating at subsystem clock 32.768 kHz)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (when operating at main system clock 5.0 MHz)
Vectored interrupt sources	Maskable	Internal : 12, External : 6
	Non-maskable	Internal : 1
	Software	1
Test input		Internal : 1, External : 1
Supply voltage		V_{DD} = 2.0 to 6.0 V
★ Package		• 100-pin plastic (fine pitch) QFP (14 × 14 mm) • 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN (14 × 20 mm)[Note 2]

Notes 1. Internal PROM/internal high-speed RAM capacity can be changed by memory size switching register (IMS).

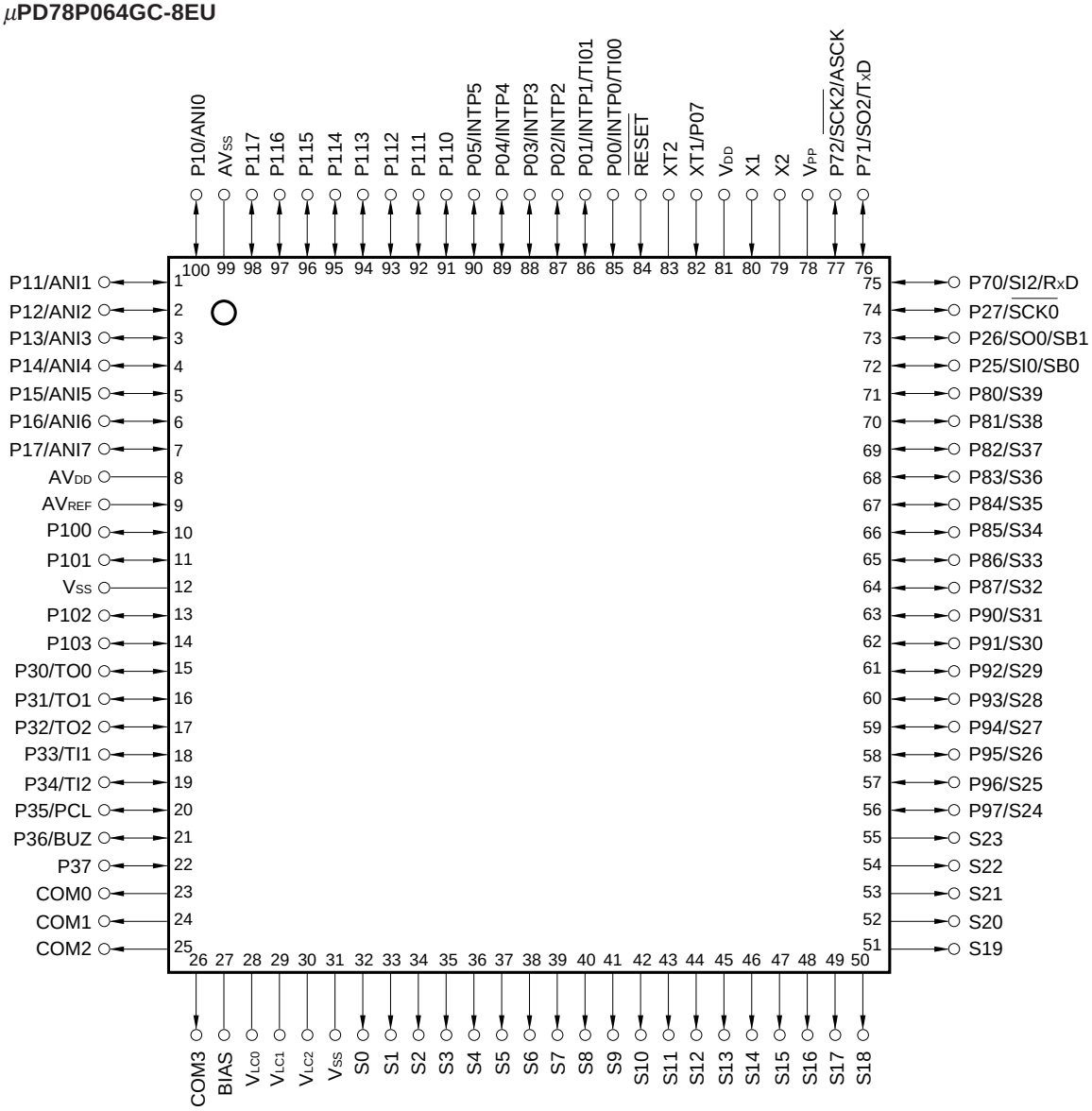
2. Under development

PIN CONFIGURATION (Top View)

(1) Normal operating mode

- **100-pin plastic QFP (fine pitch) (14 × 14 mm)**
  μPD78P064GC-7EA

★ - **100-pin plastic LQFP (fine pitch) (14 × 14 mm)**
  μPD78P064GC-8EU

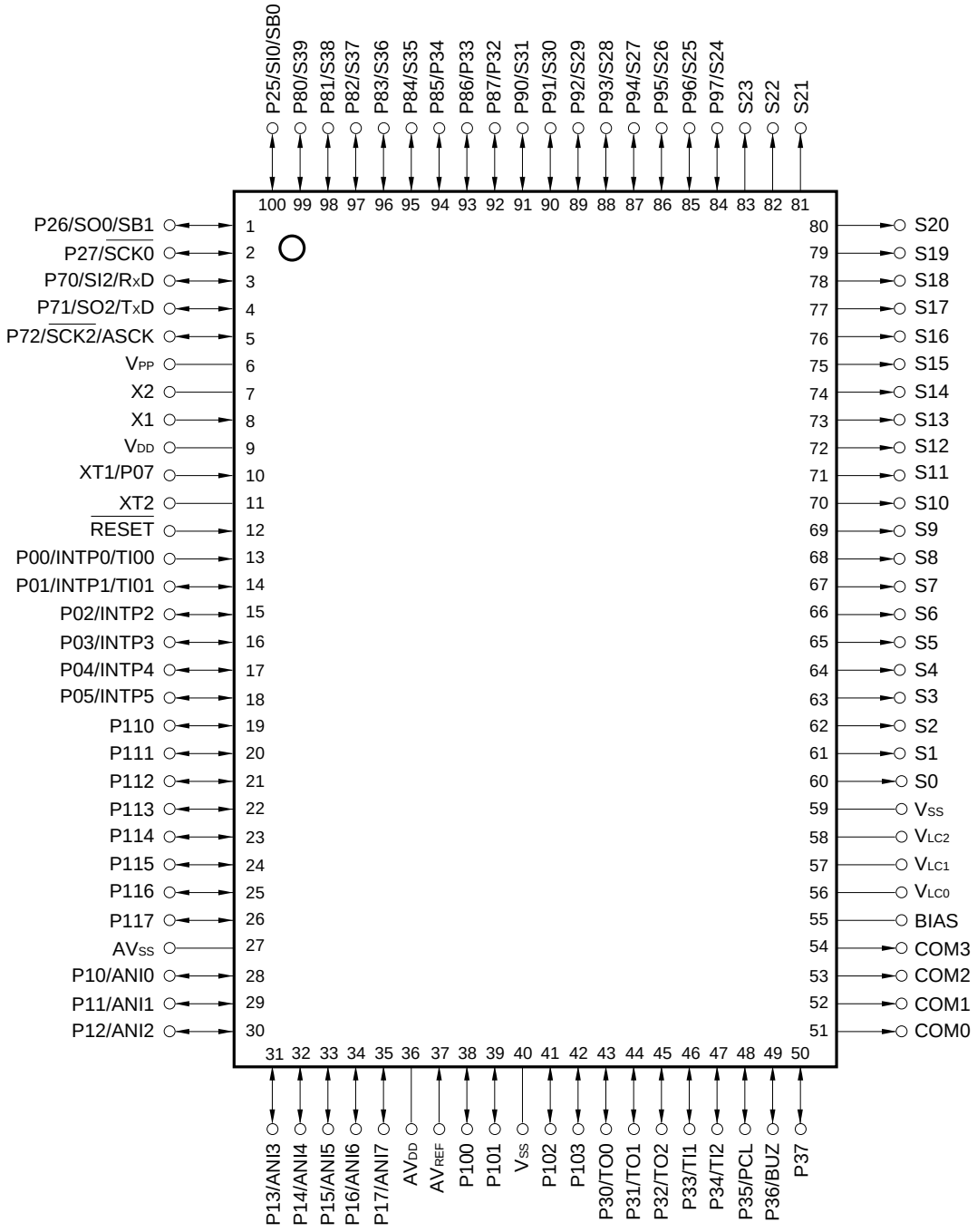


Cautions 1. Connect V_{PP} pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

- **100-pin plastic QFP (14 × 20 mm)**
  μPD78P068GF-3BA
- **100-pin ceramic WQFN (14 × 20 mm)**
  μPD78P064KL-T[Note]



Note Under development

Cautions 1. Connect V_{PP} pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

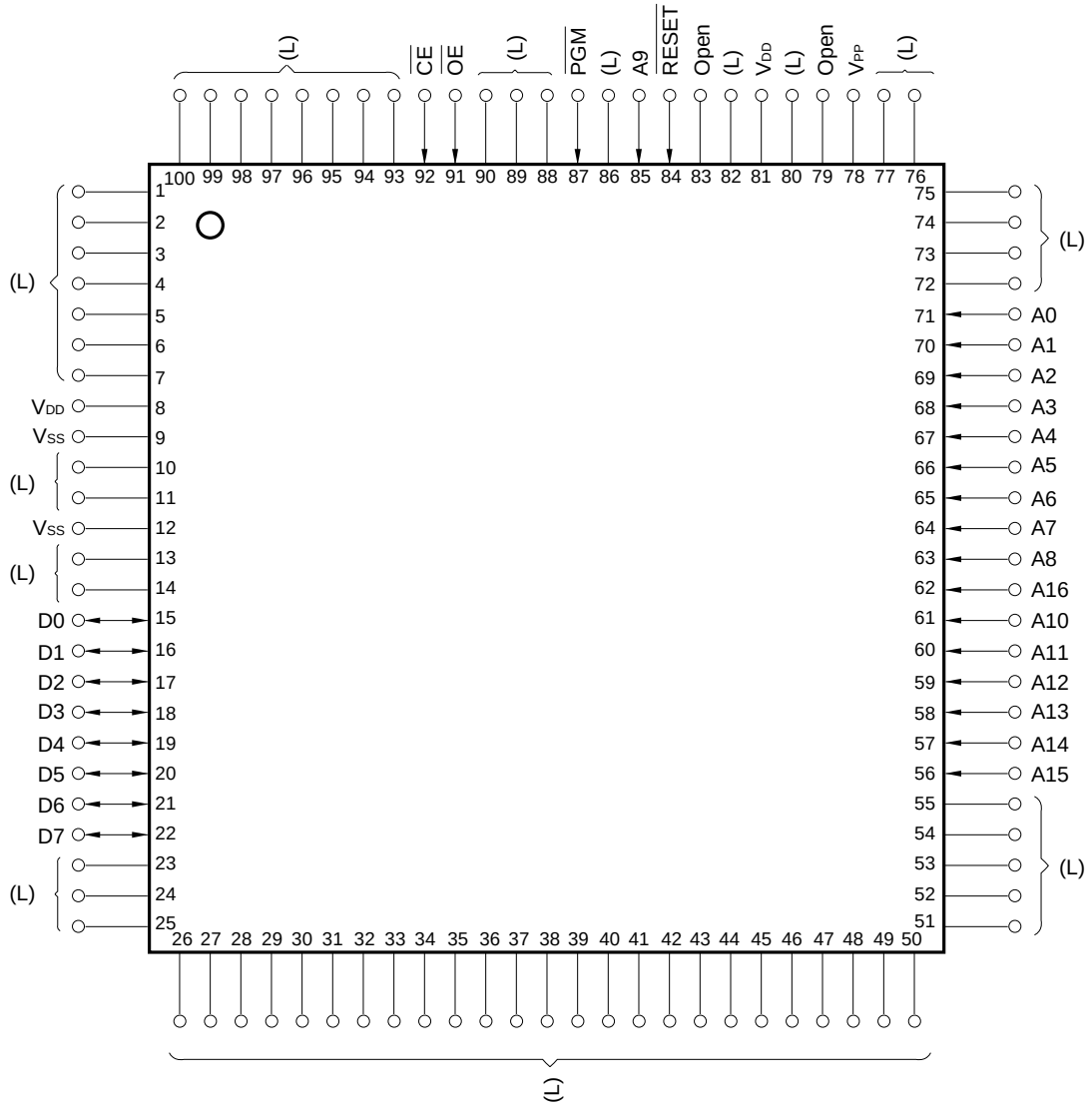
3. Connect AV_{SS} pin to V_{SS}.

ANI0-ANI7	:	Analog Input	PCL	:	Programmable Clock
ASCK	:	Asynchronous Serial Clock	$\overline{\text{RESET}}$	:	Reset
AV_{DD}	:	Analog Power Supply	RxD	:	Receive Data
AV_{REF}	:	Analog Reference Voltage	S0-S39	:	Segment Output
AV_{SS}	:	Analog Ground	SB0, SB1	:	Serial Bus
BIAS	:	LCD Power Supply Bias Control	SI0, SI2	:	Serial Input
BUZ	:	Buzzer Clock	SO0, SO2	:	Serial Output
COM0-COM3	:	Common Output	$\overline{\text{SCK0}}$, $\overline{\text{SCK2}}$	:	Serial Clock
INTP0-INTP5	:	Interrupt from Peripherals	TI00, TI01	:	Timer Input
P00-P05, P07	:	Port 0	TI1,TI2	:	Timer Input
P10-P17	:	Port 1	TO0-TO2	:	Timer Output
P25-P27	:	Port 2	TxD	:	Transmit Data
P30-P37	:	Port 3	V_{DD}	:	Power Supply
P70-P72	:	Port 7	V_{LC0}-V_{LC2}	:	LCD Power Supply
P80-P87	:	Port 8	V_{SS}	:	Ground
P90-P97	:	Port 9	V_{PP}	:	Programming Power Supply
P100-P103	:	Port 10	X1, X2	:	Crystal (Main System Clock)
P110-P117	:	Port 11	XT1, XT2	:	Crystal (Subsystem Clock)

(2) PROM programming mode

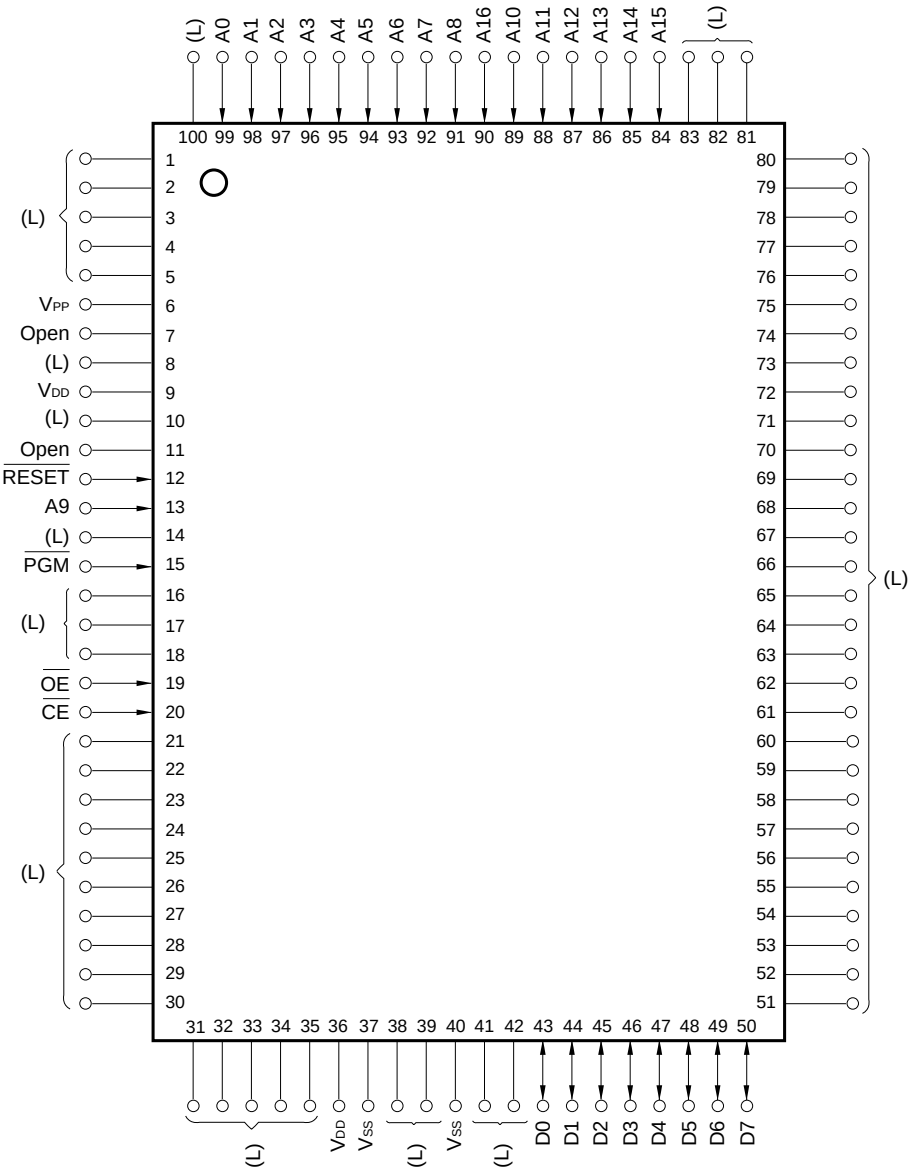
- **100-pin plastic QFP (fine pitch) (14 × 14 mm)**
  μPD78P064GC-7EA
- **100-pin plastic LQFP (fine pitch) (14 × 14 mm)**

★ **μPD78P064GC-8EU**



Cautions 1. (L) : Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS} : Connect to GND.
3. $\overline{RESET}$: Set to low level.
4. Open : No connection

- **100-pin plastic QFP (14 × 20 mm)**
  μPD78P064GF-3BA
- **100-pin ceramic WQFN (14 × 20 mm)**
  μPD78P064KL-T[Note]

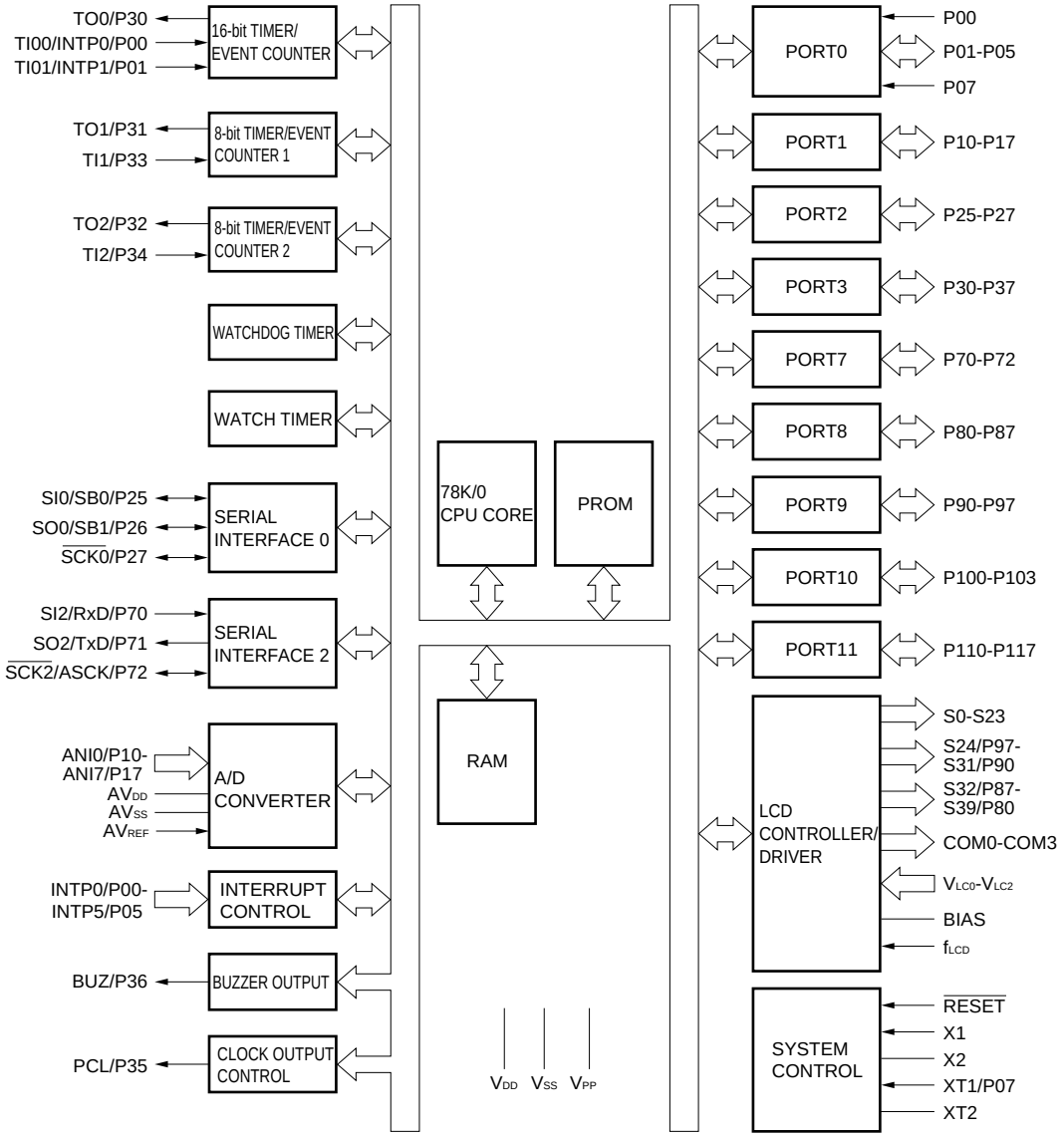


Note Under development

Cautions 1. (L) : Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS} : Connect to GND.
3. $\overline{RESET}$: Set to low level.
4. Open : No connection

A0 to A16	: Address Bus	$\overline{RESET}$	: Reset
$\overline{CE}$	: Chip Enable	V_{DD}	: Power Supply
D0 to D7	: Data Bus	V_{PP}	: Programming Power Supply
$\overline{OE}$	: Output Enable	V_{SS}	: Ground
$\overline{PGM}$	: Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78P064 AND MASK ROM PRODUCTS

The μPD78P064 is a single-chip microcontroller with an on-chip one-time writable PROM or with an on-chip EPROM which has program write, erasure, and rewrite capability.

It is possible to make all the functions exception PROM specification, and mask option of LCD drive power supply dividing resistor, to the same as those of mask ROM products by setting the memory size switching register (IMS).

Difference between the PROM product (μPD78P064) and mask ROM product (μPD78062, 78063, 78064) are shown is Table 1-1.

Table 1-1. Differences between μPD78P064 and Mask ROM Products

Item	μPD78P064	Mask ROM Products
Internal ROM structure	One-time PROM/EPROM	Mask ROM
Changing internal ROM/internal high-speed RAM capacity by memory size switching register (IMS)	Can be changed[Note]	Cannot be changed
IC pin	No	Yes
V_{PP} pin	Yes	No
Mask option of LCD drive power supply dividing resistor	No	Yes
Electrical characteristics	Refer to **Data Sheet** for each product	

Note The internal PROM becomes to 32K bytes and the internal high-speed RAM becomes 1024 bytes by the $\overline{\text{RESET}}$ input.

★ **Caution Noise resistance and noise radiation are different in PROM version and mask ROM versions. If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS of the mask ROM version (not ES).**

2. PIN FUNCTION TABLE

2.1 PINS IN NORMAL OPERATING MODE

(1) PORT PINS (1/2)

Pin Name	Input/Output	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 7-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output is specifiable bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software.[Note 2]		Input	ANI0 to ANI7
P25	Input/output	Port 2 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software.		Input	SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					——
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{\text{SCK2}}$/ASCK

Notes 1. When P07/XT1 pins are used as the input ports, set processor clock control register (PCC) bit 6 (FRC) to 1. (Do not use the on-chip feedback resistor of the subsystem clock oscillation circuit.)

2. When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for A/D converter, set port 1 to input mode. The on-chip pull-up resistor is automatically disabled.

(1) PORT PINS (2/2)

Pin Name	Input/Output	Function	After Reset	Dual-Function Pin
P80 to P87	Input/output	Port 8 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD display control register (LCDC).	Input	S39 to S32
P90 to P97	Input/output	Port 9 8-bit input/output port. Input/output is specifiable bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD display control register. (LCDC).	Input	S31 to S24
P100 to P103	Input/output	Port 10 4-bit input/output port Input/output is specifiable in bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software. It is possible to directly drive LED.	Input	——
P110 to P117	Input/output	Port 11 8-bit input/output port Input/output is specifiable in bit-wise. When used as the input port, an on-chip pull-up resistor can be used by software. Falling edge detection possible.	Input	——

(2) PINS OTHER THAN PORT PINS (1/2)

Pin Name	Input/Output	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt request input with specifiable Valid edges (rising edge, falling edge, and both rising and falling edges).	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial data input of the serial interface	Input	P25/SB0
SI2				P70/RxD
SO0	Output	Serial data output of the serial interface	Input	P26/SBI
SO2				P71/TxD
SB0	Input/output	Serial data input/output of the serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial clock input/output of the serial interface	Input	P27
$\overline{SCK2}$				P72/ASCK
RxD	Input	Serial data input for asynchronouse serial interface	Input	P70/SI2
TxD	Outpu	Serial data output for asynchronous serial interface	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to the 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00).		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1).		P33
TI2		External count clock input to the 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (dual-function as 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
S0 to S23	Output	LCD controller/driver segment signal output	Output	———
S24 to S31			Input	P97-P90
S32 to S39				P87-P80
COM0 to COM3	Output	LCD controller/driver common signal output	Output	———
V_{LC0} to V_{LC2}	——	LCD drive voltage	——	———
BIAS	——	LCD drive power supply	——	———

(2) PINS OTHER THAN PORT PINS (2/2)

Pin Name	Input/Output	Function	After Reset	Dual-Function Pin
ANI0 to ANI7	Input	Analog input of A/D converter	Input	P10 to P17
AV_{REF}	Input	Reference voltage input of A/D converter	—	—
AV_{DD}	—	Analog power supply of A/D converter	—	—
AV_{SS}	—	Ground potential of A/D converter	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Main system clock oscillation crystal connection	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{PP}	—	High-voltage applied during program write/verification Connected directly to V_{SS} in normal operating mode	—	—
V_{SS}	—	Ground potential	—	—

2.2 PINS IN PROM PROGRAMMING MODE

Pin Name	Input/Output	Function
$\overline{RESET}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programing mode.
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

★ 2.3 PIN INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

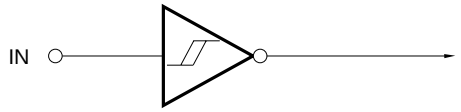
Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, refer to **Figure 2-1**.

Table 2-1. Type of Input/Output Circuit of Each Pin

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection When not Used
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	I/O	Individually connect to V_{SS} via a resistor
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connect to V_{DD}.
P10/ANI0 to P17/ANI7	11	I/O	Individually connect to V_{DD} or V_{SS} via a resistor
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P70/SI2/RxD	8-A		
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P80/S39 to P87/S32	17-A		
P90/S31 to P97/S24			
P100 to P103	5-A		
P110 to P117	8-A		Individually connect to V_{DD} via resistor
S0 to S23	17	Output	Leave open
COM0 to COM3	18		
V_{LC0} to V_{LC2}	——	——	
BIAS			
$\overline{RESET}$	2	Input	——
XT2	16	——	Leave open
AV_{REF}	——		Connect to V_{SS}
AV_{DD}			Connect to V_{DD}.
AV_{SS}			Connect to V_{SS}.
V_{PP}			Connect directly to V_{SS}

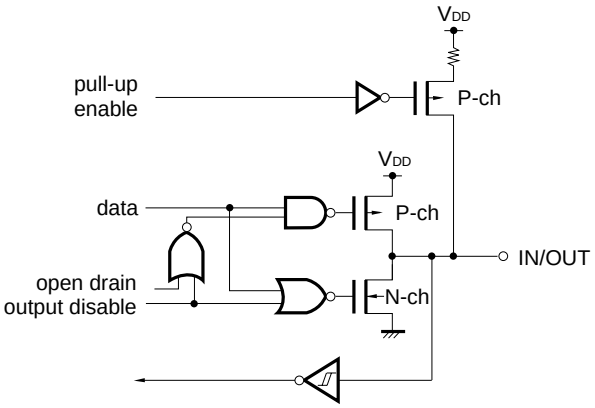
Figure 2-1. List of Pin Input/Output Circuits (1/2)

Type 2

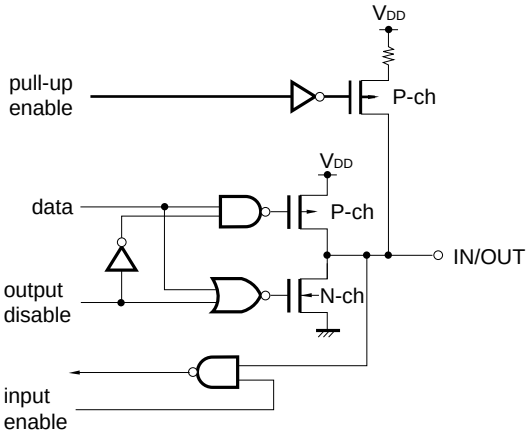


Schmitt-Triggered Input with Hysteresis Characteristic

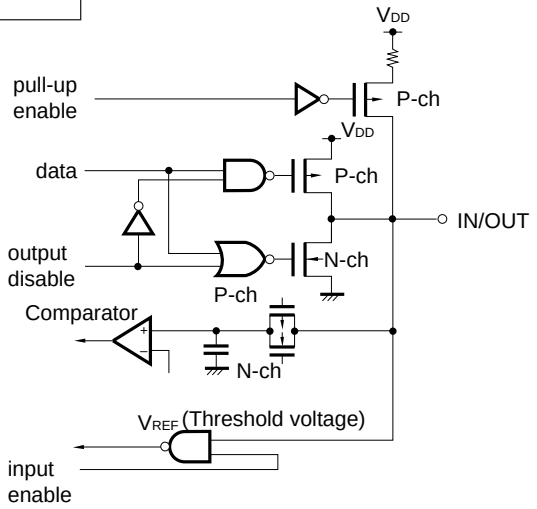
Type 10-A



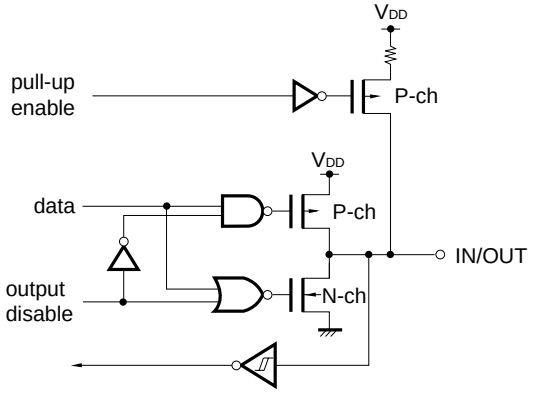
Type 5-A



Type 11



Type 8-A



Type 16

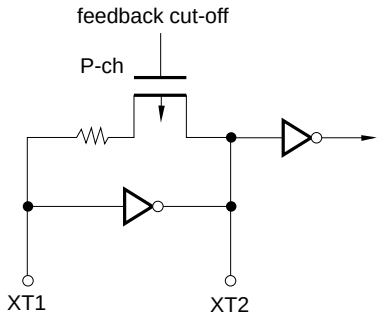
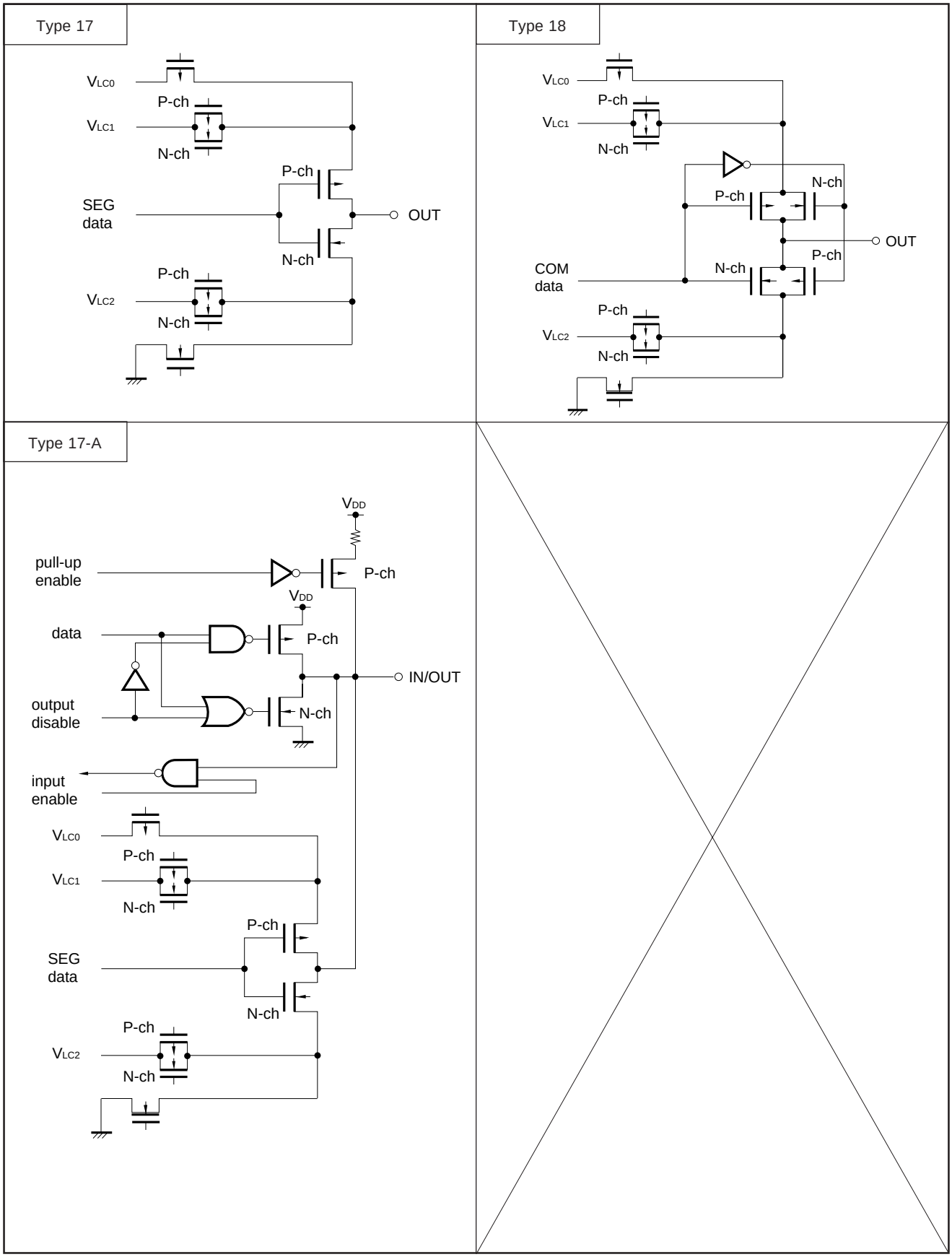


Figure 2-1. List of Pin Input/Output Circuits (2/2)



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of mask ROM product having different internal memories (ROM, RAM).

The IMS is set up by the 8-bit memory manipulating instruction.

C8H will result by the $\overline{\text{RESET}}$ input.

Figure 3-1. Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	0	0	16K bytes
0	1	1	0	24K bytes
1	0	0	0	32K bytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the set values of IMS which makes the memory map the same as that of the various mask ROM products.

Table 3-1. Memory Size Switching Register Setting Values

Target Mask ROM Product	IMS Setting Value
μPD78062	44H
μPD78063	C6H
μPD78064	C8H

4. PROM PROGRAMMING

The μPD78P064 has an on-chip 32K-byte PROM as a program memory. For programming, set the PROM programming mode by the V_{PP} and $\overline{RESET}$ pins. For processing unused pins, refer to **PIN CONFIGURATION (2) PROM programming mode**.

Caution When writing in a program, use locations 0000H-7FFFH. (Specify the last address as 7FFFH). You cannot write in using a PROM programmer that cannot specify the addresses to write.

4.1 OPERATING MODES

When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 4-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

× : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, of $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P064s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set. In this mode, check if a write operation is performed correctly, after the write.

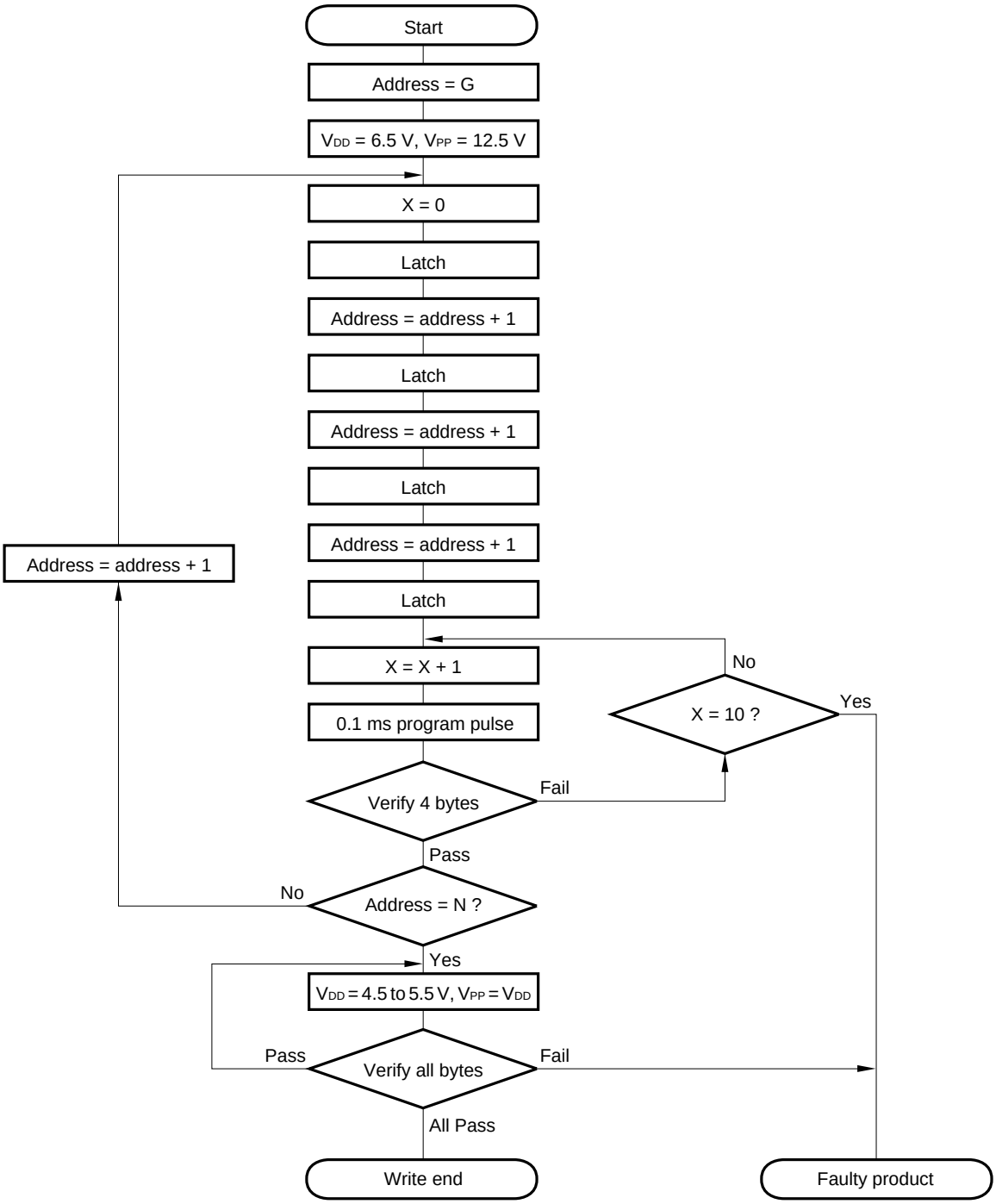
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins of multiple μPD78P064s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

4.2 PROM WRITE PROCEDURE

Figure 4-1. Page Program Mode Flow Chart



G = Start address

N = Program last address

Figure 4-2. Page Program Mode Timing

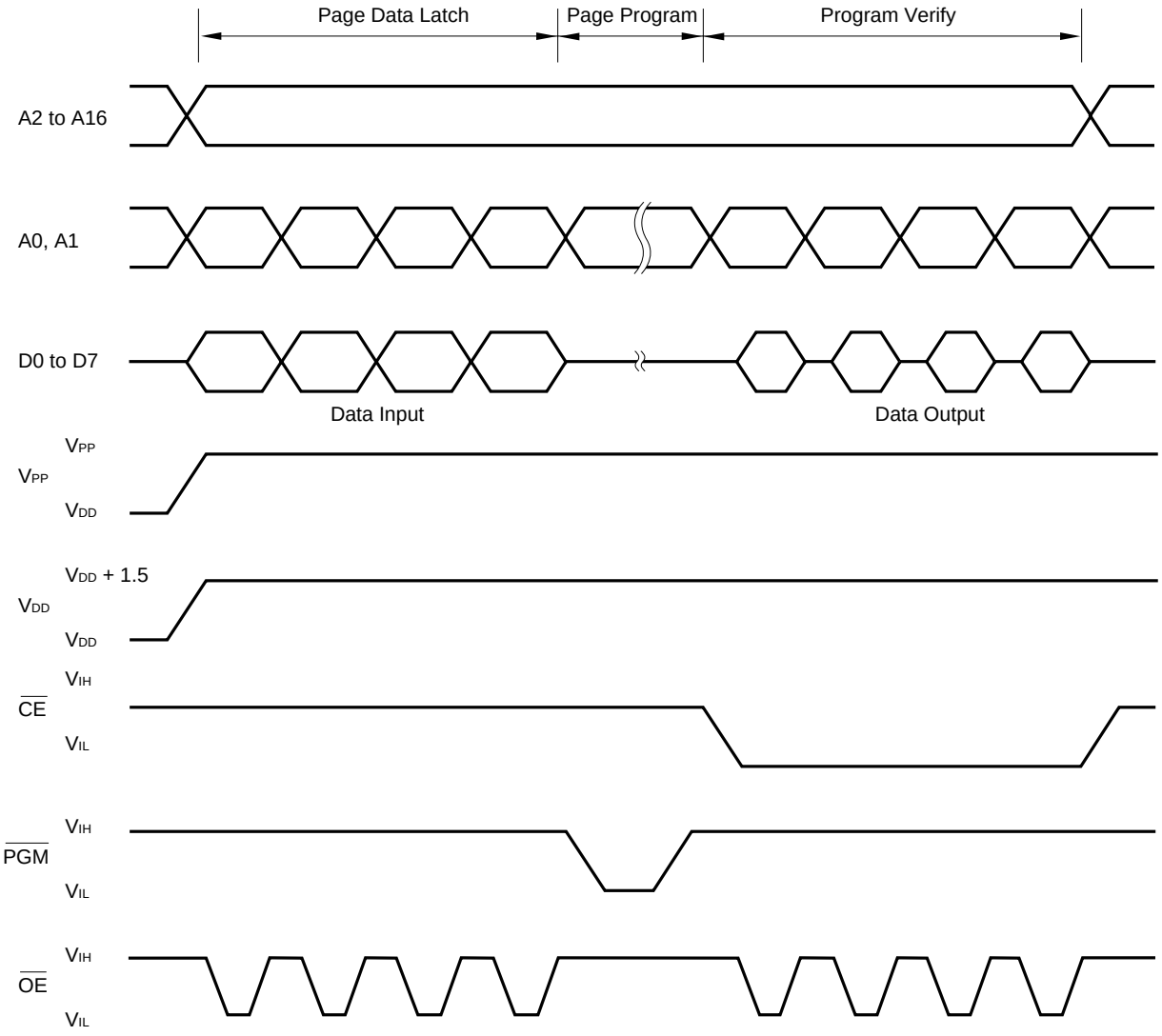
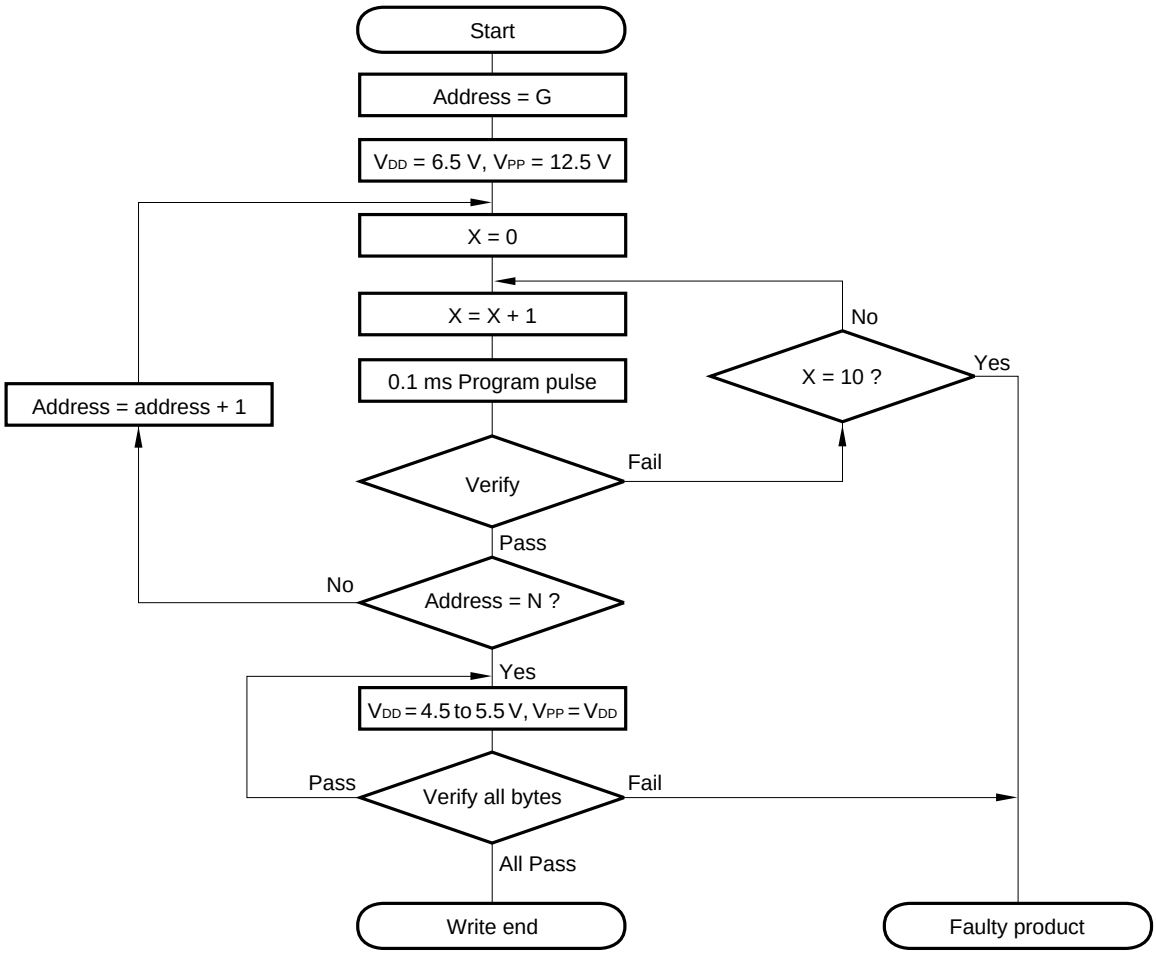


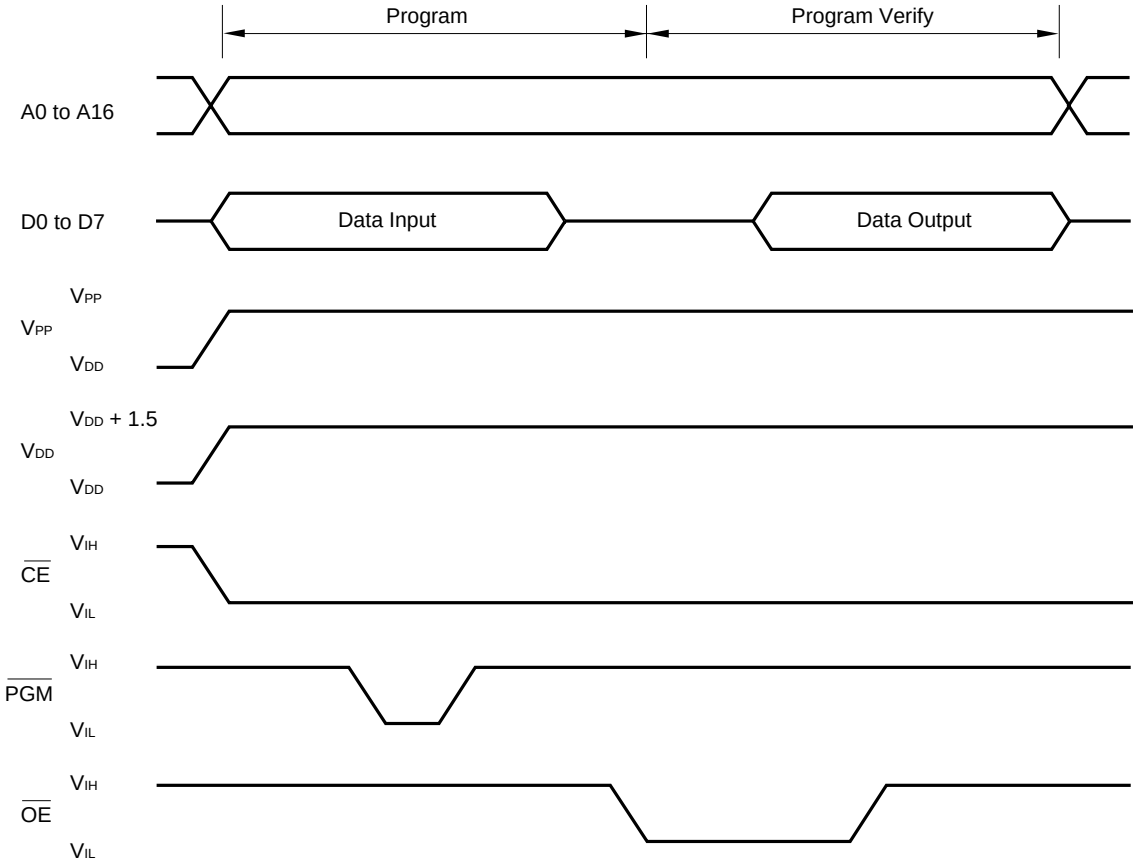
Figure 4-3. Byte Program Mode Flow Chart



G = Start address

N = Program last address

Figure 4-4. Byte Program Mode Timing



Cautions 1. V_{DD} should be applied before V_{PP} and cut after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected of removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

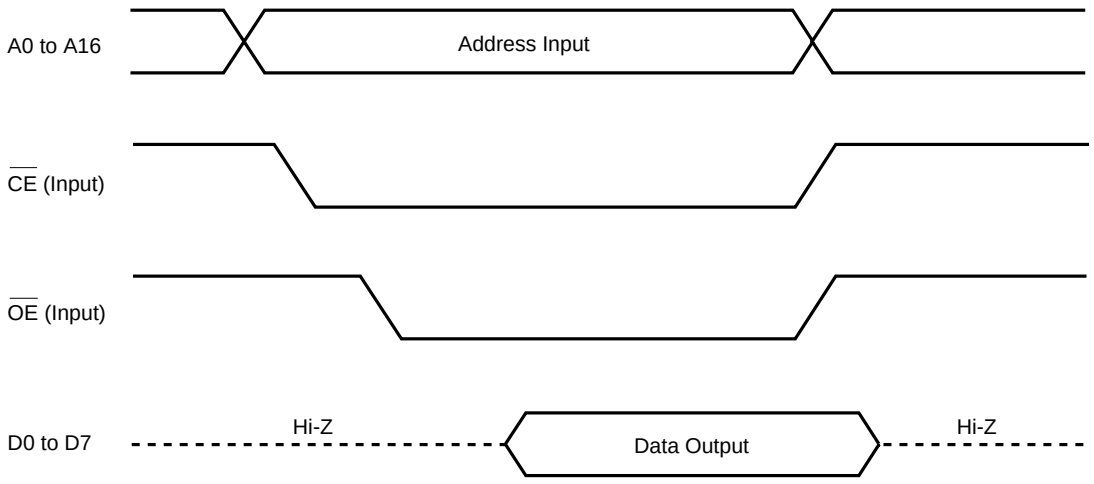
4.3 PROM READ PROCEDURE

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and process all other unused pins as shown in **Pin Configuration (2) PROM programming mode**.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of read data into the A0 to A16 pins.
(4) Read mode
(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 4-5.

Figure 4-5. PROM Read Timings



5. ERASURE METHOD (μPD78064KL-T ONLY)

The μPD78P064KL-T is capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the contents of data, irradiate light having a wavelength of less than about 400 nm to the erasing window. Normally, irradiate ultraviolet rays of 254 nm wavelength. Volume of irradiation required to completely erase the contents of data is as follows:

★ • UV intensity × erasing time : 30 W•s/cm^2 or more

★ • Erasing time : 40 minutes MIN. (When a UV lamp of 12 mW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasing window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

6. ERASURE WINDOW SEAL (μPD78P064KL-T ONLY)

To protect from miserasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, stick a protection seal on the erasure window when EPROM contents erasure is not performed.

7. ONE-TIME PROM PRODUCTS SCREENING

The one-time PROM product (μPD78P064GC-7EA, μPD78P064GC-8EU, μPD78P064GF-3BA) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125 °C	24 hours

At present, a fee is charged by NEC for one-time PROM after-programming writing, marking, screening, and verify service for the QTOP Microcontroller. For details, contact your sales representative.

8. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
	AV_{DD}			–0.3 to V_{DD} +0.3	V
	AV_{REF}			–0.3 to V_{DD} +0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I	P00-P05, P07, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117		–0.3 to V_{DD} +0.3	V
	V_{I2}	A9 (PROM programming mode)		–0.3 to +13.5	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} –0.3 to AV_{REF} +0.3	V
Output current, high	I_{OH}	1 pin		–10	mA
		Total for P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117		–15	mA
Output current, low	I_{OL} Note	1 pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for P01-P05, P10-P17, P100, P101, P110-P117	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P30-P37, P102, P103	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P25-P27, P70-P72, P80-P87, P90-P97	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × $\sqrt{\text{Duty}}$

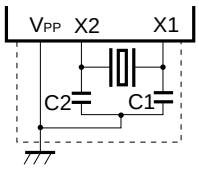
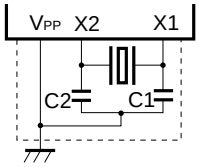
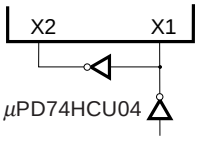
Caution The product quality may be damaged even if a value of only one of the above parameters exceeds the absolute maximum rating or any value exceeds the absolute maximum rating for an instant. That is, the absolute maximum rating is a rating value which may cause a product to be damaged physically. The absolute maximum rating values must therefore be observed in using the product.

Remark Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

CAPACITANCE (T_A= 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended circuit	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X)Note 1	V_{DD} = Oscillator voltage range	1		5	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f_X)Note 1		1		5	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

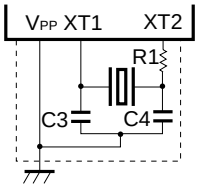
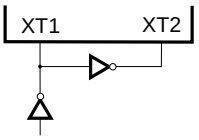
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. If the main system clock oscillation circuit is operated by the subsystem clock when the main system clock is stopped, reswitching to the main system clock should be performed after the stable oscillation time has been obtained by the program.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} has reached the minimum oscillation voltage range.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is designed as a low amplification circuit to provide low consumption current, causing misoperation to noise more frequently than the main system clock oscillation circuit. Special care should therefore be taken to wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATION CIRCUIT CONSTANT

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHZ)	Recommended Circuit Constant		Oscillator Voltage Range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSA5.00MG	5.00	30	30	2.7	6.0	
	CST5.00MGW	5.00	Built-in	Built-in	2.7	6.0	
Matsushita Electronics Components Co., Ltd.	EF0GC5004A4	5.00	Built-in	Built-in	2.7	6.0	Lead type
	EF0EC5004A4	5.00	Built-in	Built-in	2.7	6.0	Round lead type
	EF0EN5004A4	5.00	33	33	2.7	6.0	Lead type
	EF0S5004B5	5.00	Built-in	Built-in	2.7	6.0	Chip type
Kyocera Corp.	KBR-5.0MSA	5.00	33	33	2.7	6.0	Lead type
	PBRC5.00A	5.00	33	33	2.7	6.0	Chip type
	KBR-5.0MKS	5.00	Built-in	Built-in	2.7	6.0	Lead type
	KBR-5.0MWS	5.00	Built-in	Built-in	2.7	6.0	Chip type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103	V_{DD} = 2.7 to 6.0 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2	V_{DD} = 2.7 to 6.0 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
	V_{IH4}	XT1/P07, XT2	4.5 ≤ V_{DD} ≤ 6.0 V	0.8 V_{DD}		V_{DD}	V
			2.7 ≤ V_{DD} < 4.5 V	0.9 V_{DD}		V_{DD}	V
			2.0 ≤ V_{DD} < 2.7 V[Note]	0.9 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103	V_{DD} = 2.7 to 6.0 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	X1, X2	V_{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V_{IL4}	XT1/P07, XT2	4.5 ≤ V_{DD} ≤ 6.0 V	0		0.2 V_{DD}	V
			2.7 ≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			2.0 ≤ V_{DD} < 2.7 V[Note]	0		0.1 V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 6.0 V I_{OH} = –1 mA		V_{DD}–1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD}–0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P100-P103	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P110-P117	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 6.0 V, open-drain, pulled up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When P07/XT1 pin is used as P07, the inverse phase of P07 should be input to XT2 using an inverter.

Remark Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

	Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
	Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117			3	μA
		I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117			–3	μA
		I_{LIH2}		X1, X2, XT1/P07, XT2			–20	μA
	Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
	Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
	Software pull-up resistor	R	V_{IN} = 0 V, P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
				2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ
	Supply current[Note 1]	I_{DD1}	5.00 MHz, Crystal oscillation (f_{XX} = 2.5 MHz)[Note 2] operating mode	V_{DD} = 5.0 V ± 10 %[Note 5]		5.0	15.0	mA
				V_{DD} = 3.0 V ± 10 %[Note 6]		0.7	2.1	mA
				V_{DD} = 2.2 V ± 10 %[Note 6]		0.4	1.2	mA
			5.00 MHz, Crystal oscillation (f_{XX} = 5.0 MHz)[Note 3] operating mode	V_{DD} = 5.0 V ± 10 %[Note 5]		9.0	27.0	mA
				V_{DD} = 3.0 V ± 10 %[Note 6]		1.0	3.0	mA
		I_{DD2}	5.00 MHz, Crystal oscillation (f_{XX} = 2.5 MHz)[Note 2] HALT mode	V_{DD} = 5.0 V ± 10 %		1.4	4.2	mA
				V_{DD} = 3.0 V ± 10 %		500	1500	μA
				V_{DD} = 2.2 V ± 10 %		280	840	μA
			5.00 MHz, Crystal oscillation (f_{XX} = 5.0 MHz)[Note 3] HALT mode	V_{DD} = 5.0 V ± 10 %		1.6	4.8	mA
				V_{DD} = 3.0 V ± 10 %		650	1950	μA
		I_{DD3}	32.768 kHz, Crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ± 10 %		135	270	μA
				V_{DD} = 3.0 V ± 10 %		95	190	μA
				V_{DD} = 2.2 V ± 10 %		70	140	μA
		I_{DD4}	32.768 kHz, Crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ± 10 %		25	55	μA
				V_{DD} = 3.0 V ± 10 %		5	15	μA
				V_{DD} = 2.2 V ± 10 %		2.5	12.5	μA
★		I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is connected	V_{DD} = 5.0 V ± 10 %		1	30	μA
				V_{DD} = 3.0 V ± 10 %		0.5	10	μA
				V_{DD} = 2.2 V ± 10 %		0.3	10	μA
★		I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is disconnected	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
				V_{DD} = 3.0 V ± 10 %		0.05	10	μA
				V_{DD} = 2.2 V ± 10 %		0.05	10	μA

Notes 1. Current flowing V_{DD} pin. Not including on-chip pull-up resistors or LCD dividing resistors.

2. Main system clock $f_{XX} = f_X/2$ operation (when oscillation mode selection register (OSMS) is set to 00H)

3. Main system clock $f_{XX} = f_X$ operation (when OSMS is set to 01H)

4. When the main system clock is stopped.

5. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

6. Low-speed mode operation (when PCC is set to 04H)

Remark Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

DC CHARACTERISTICS (T_A = –10 to +85 °C)

(1) Static Display Mode (V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	2.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD}	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the out voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(2) 1/3 Bias Method (V_{DD} = 2.5 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.5		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	2.5 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD} V_{LCD1} = $V_{LCD} \times \frac{2}{3}$ V_{LCD2} = $V_{LCD} \times \frac{1}{3}$	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the out voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(3) 1/2 Bias Method (V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.7		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	2.7 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD} V_{LCD1} = $V_{LCD} \times \frac{1}{2}$ V_{LCD2} = V_{LCD1}	0		±0.2	V
LCD output voltage deviation[Note](segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the out voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

	Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
	Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock (f_{XX} = 2.5 MHz)Note 1	V_{DD} = 2.7 to 6.0 V	0.8		64	μs
					2.2		64	μs
			Operating on main system clock (f_{XX} = 5.0 MHz)Note 2	4.5 ≤ V_{DD} ≤ 6.0 V	0.4		32	μs
				2.7 ≤ V_{DD} < 4.5 V	0.8		32	μs
			Operating on subsystem clock		40Note 3	122	125	μs
★	TI00 input high/low-level width	t_{TIH00}, t_{TIL00}	4.5 V ≤ V_{DD} ≤ 6.0 V		$2/f_{sam}$+0.1Note 4			μs
			2.7 V ≤ V_{DD} < 4.5 V		$2/f_{sam}$+0.2Note 4			μs
			2.0 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5Note 4			μs
★	TI01 input high/low-level width	t_{TIH01}, t_{TIL01}	V_{DD} = 2.7 to 6.0 V		10			μs
					20			μs
	TI input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		4	MHz
					0		275	kHz
	TI1, TI2 input high/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		100			ns
					1.8			μs
	Interrupt input high/low-level width	t_{INTH}, t_{INTL}	INTP0		$8/f_{sam}$Note 4			μs
			INTP1-INTP5, P110-P117	V_{DD} = 2.7 to 6.0 V	10			μs
					20			μs
	$\overline{RESET}$ low level width	t_{RST}	V_{DD} = 2.7 to 6.0 V			10		μs
					20			μs

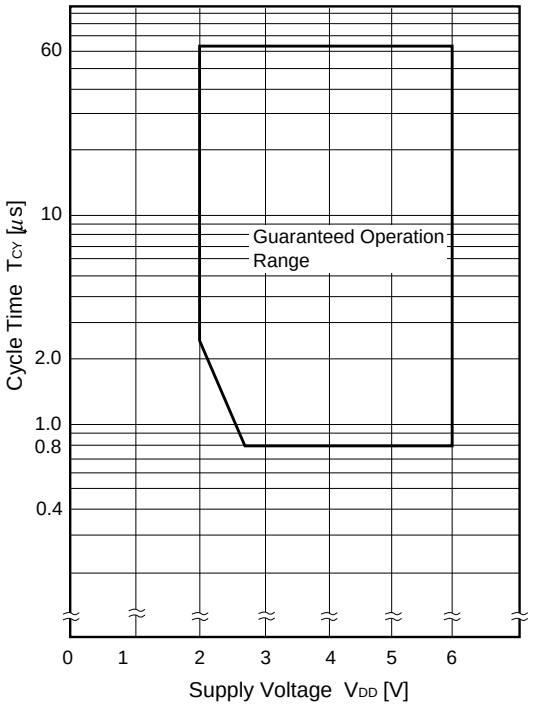
Notes 1. Main system clock f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H)

2. Main system clock f_{XX} = f_X operation (when OSMS is set to 01H)

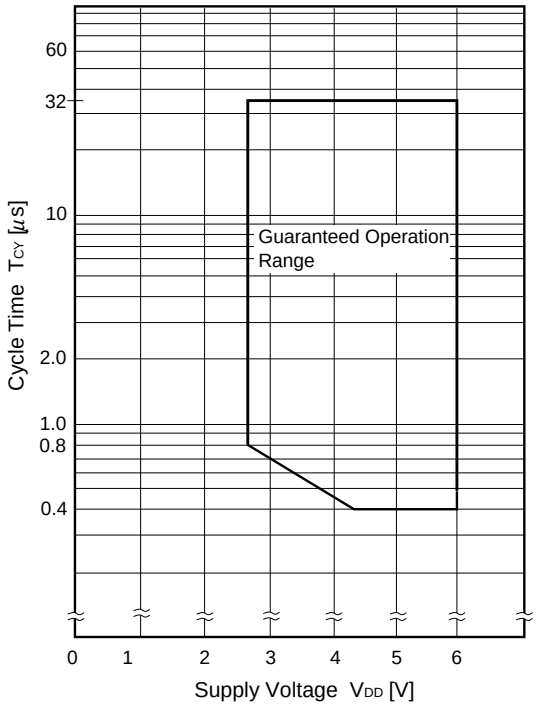
3. This is the value when the external clock is used. The value is 114 μs (min.) when the crystal resonator is used.

4. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $f_{XX}/2^N$, f_{XX}/32, f_{XX}/64 and f_{XX}/128 (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X/2$ operation)



T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X$ operation)



(2) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 6.0 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of $\overline{SCK0}$, SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{SCK0}$...Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH3},	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2–50			ns
	t_{KL3}			t_{KCY3}/2–150			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(iv) SBI mode ($\overline{SCK0}$...External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 6.0 V	t_{KCY5}/2–160			ns
				t_{KCY5}/2–190			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 6.0 V	t_{KCY5}/2–50			ns
				t_{KCY5}/2–100			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 6.0 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}					300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH6}	V_{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{SCK0}$ low-level width	t_{KL6}	V_{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to SCK0↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from SCK0↑)	t_{KSI6}			t_{KCY6}/2			ns
SB0, SB1 output delay time from SCK0↓	t_{KSO6}	R = 1 kΩ,	V_{DD} = 4.5 to 6.0 V	0		300	ns
		C = 100 pF[Note]		0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(b) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high/low-level width	t_{KH7}, t_{KL7}	4.5 V ≤ V_{DD} ≤ 6.0 V	t_{KCY7}/2–50			ns
			t_{KCY7}/2–100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI7}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of $\overline{SCK2}$, SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK8}		100			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI8}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK2}$ rise, fall time	t_{R8}, t_{F8}				1000	ns

Note C is the load capacitance of SO2 output line.

(iii) UART mode (Dedicated baud rate generator output)

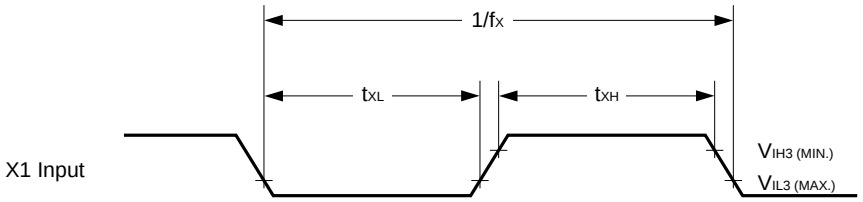
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
					19531	bps

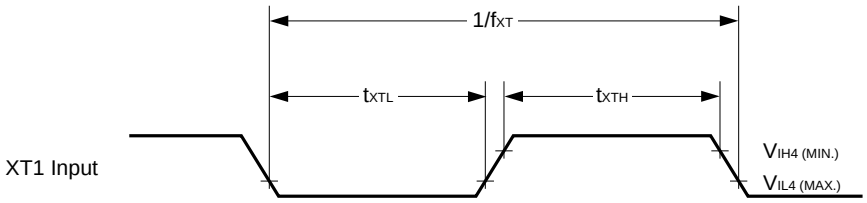
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high/low-level width	t_{KH9}, t_{KL9}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
ASCK rise, fall time	t_{R9}, t_{F9}				1000	ns

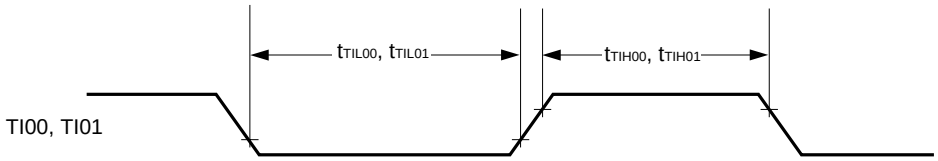
AC Timing Test Point (Excluding X1, XT1 Input)

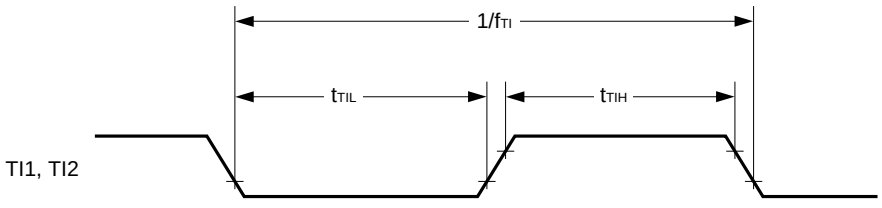
Clock Timing





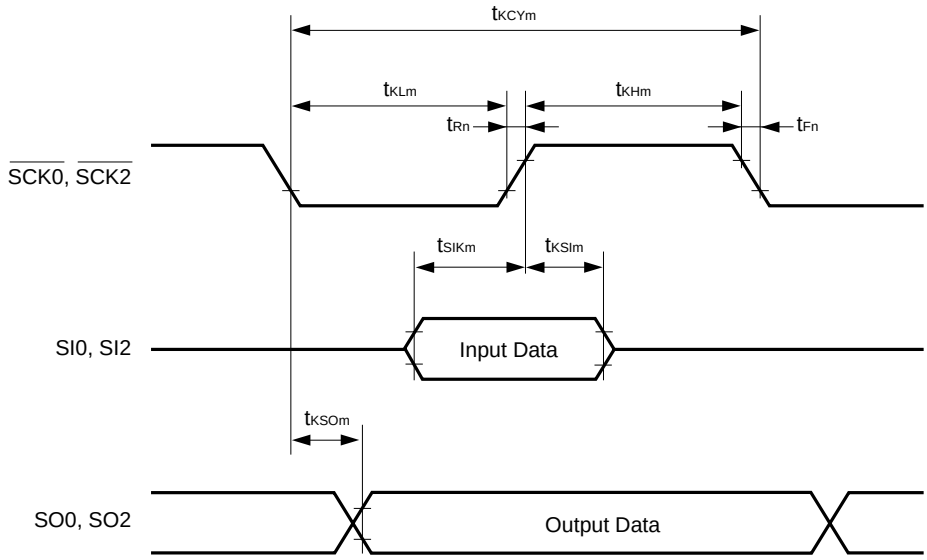
★ TI Timing





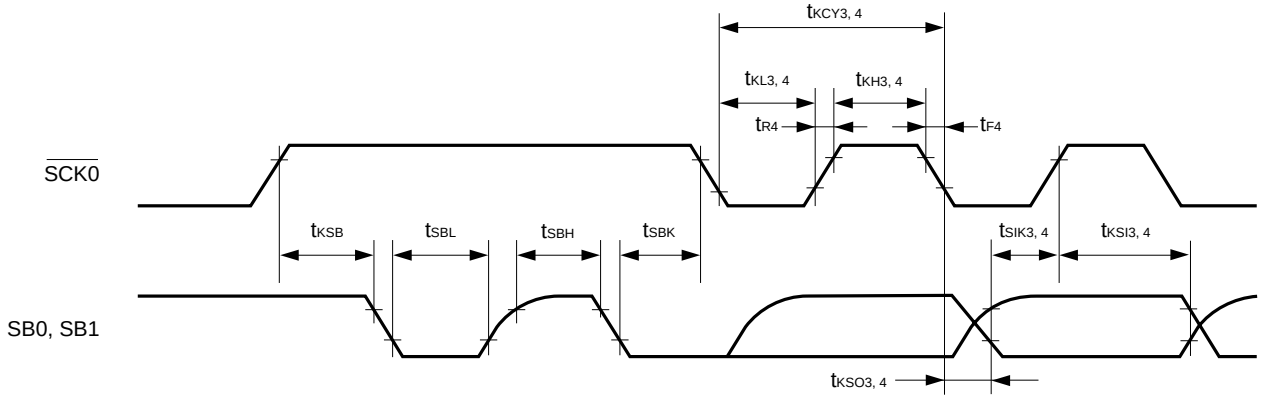
Serial Transfer Timing

3-wire serial I/O mode:

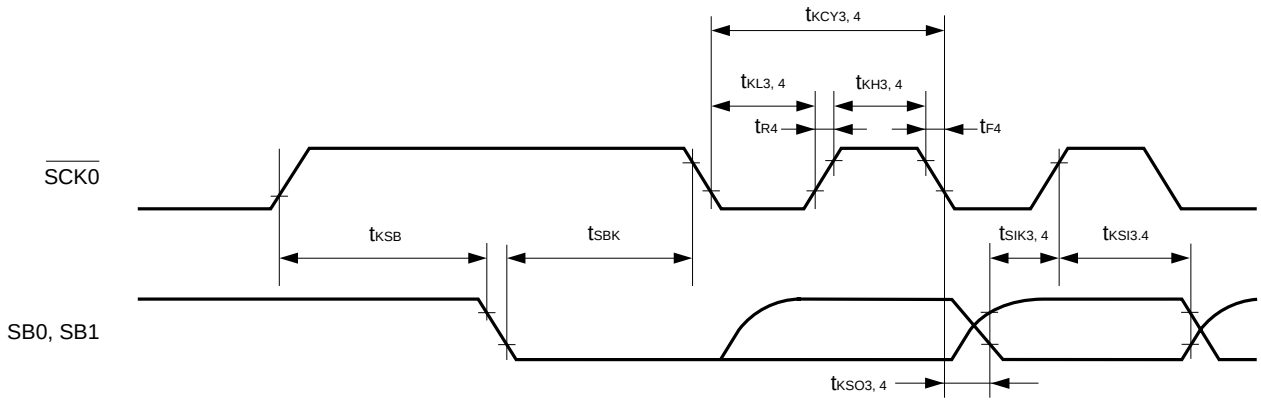


m = 1, 2, 7, 8
n = 2, 8

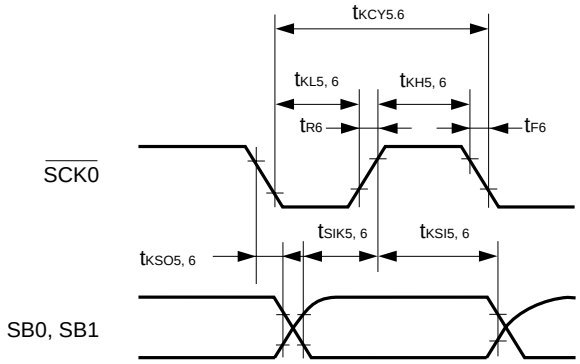
SBI mode (bus release signal transfer):



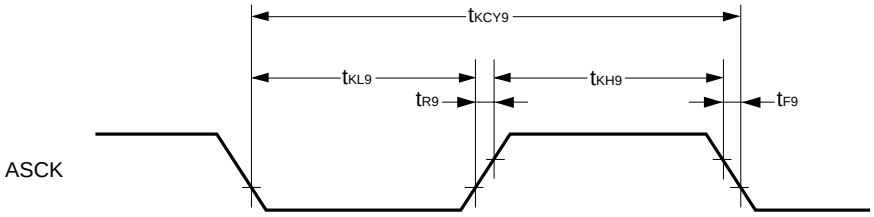
SBI mode (command signal transfer):



2-wire serial I/O mode:



UART mode:



A/D Converter (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 4.5 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		4.5 V ≤ AV_{REF} ≤ AV_{DD}			2.0	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.0		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{AIREF}		4	14		kΩ

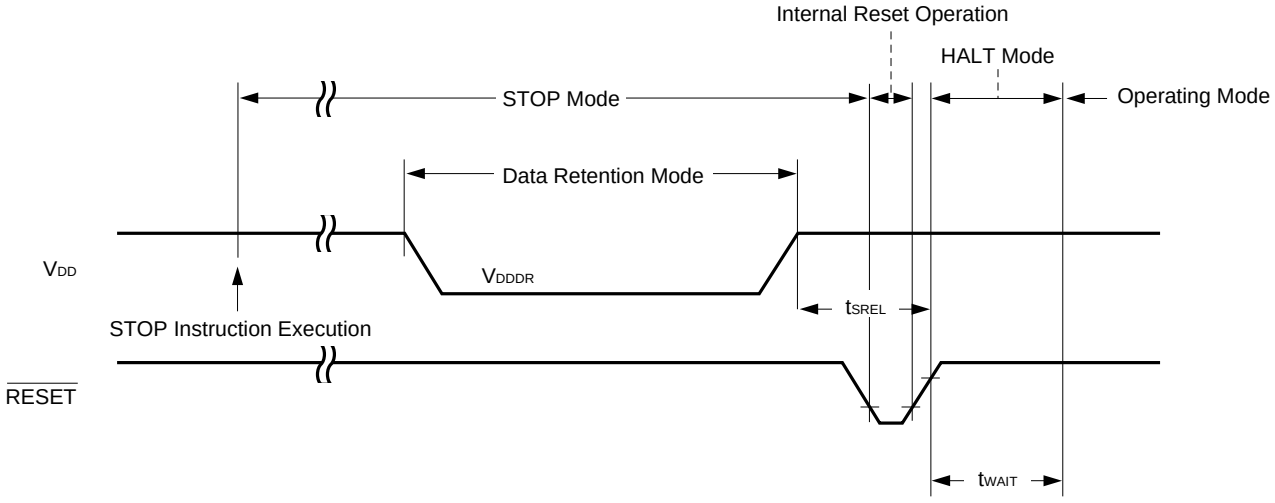
Note Quantization error (±1/2 LSB) is not included. This is expressed in proportion to the full-scale value.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85 °C)

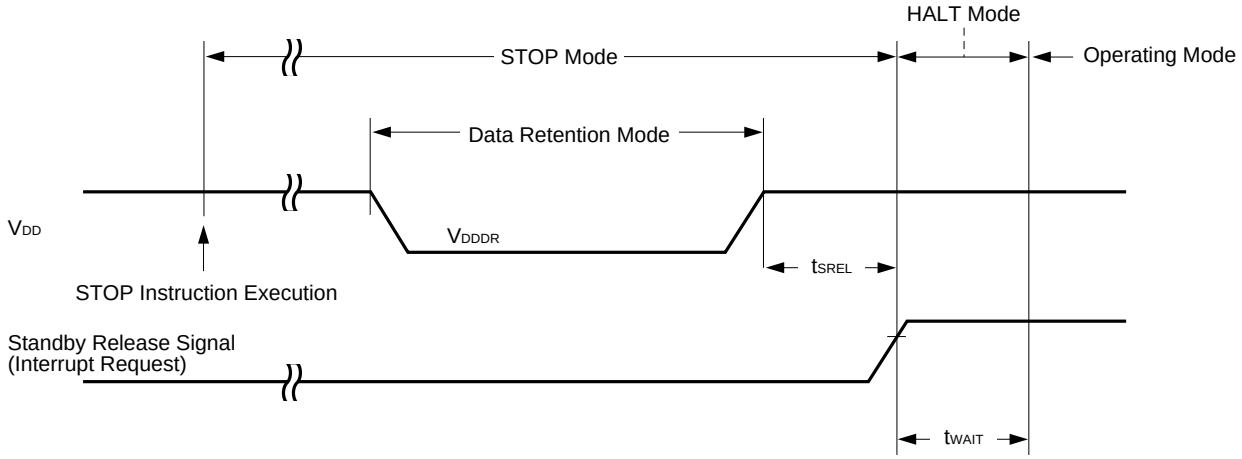
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		6.0	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt		**Note**		ms

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{12}/f_{XX}$ and $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ is possible.

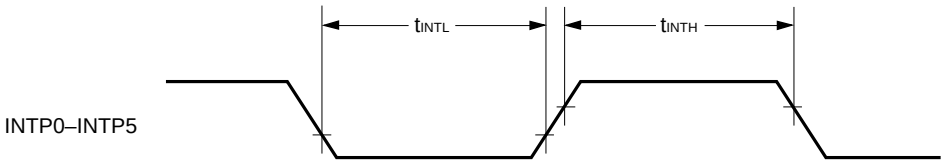
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



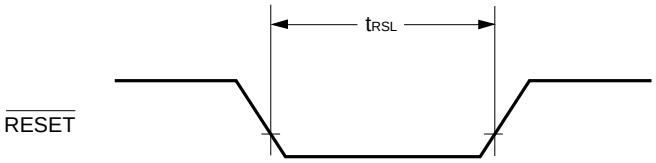
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM Write Mode (T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

Note Symbol corresponding to the μPD27C1001A.

(2) PROM Read Mode (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD} ± 0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} –1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} –0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} –0.6	V_{DD}	V_{DD} +0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Symbol corresponding to the μPD27C1001A.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

Note Corresponding μPD27C1001A symbol

(b) Byte program mode (T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
nput data hold time (from $\overline{PGM}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol

(2) PROM Read Mode (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD} ± 0.6 V)

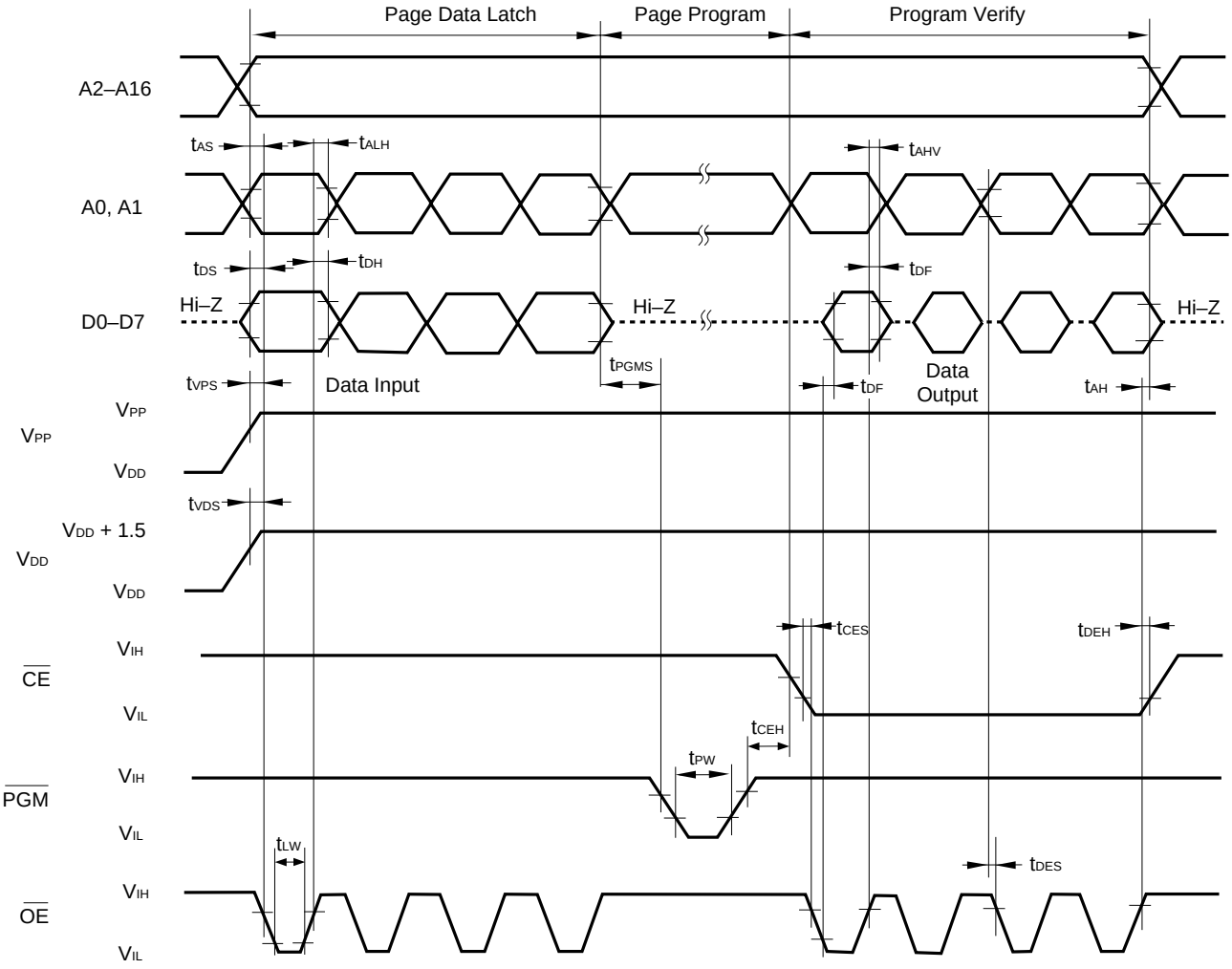
Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output time from address	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{DH}	t_{DH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C1001A symbol

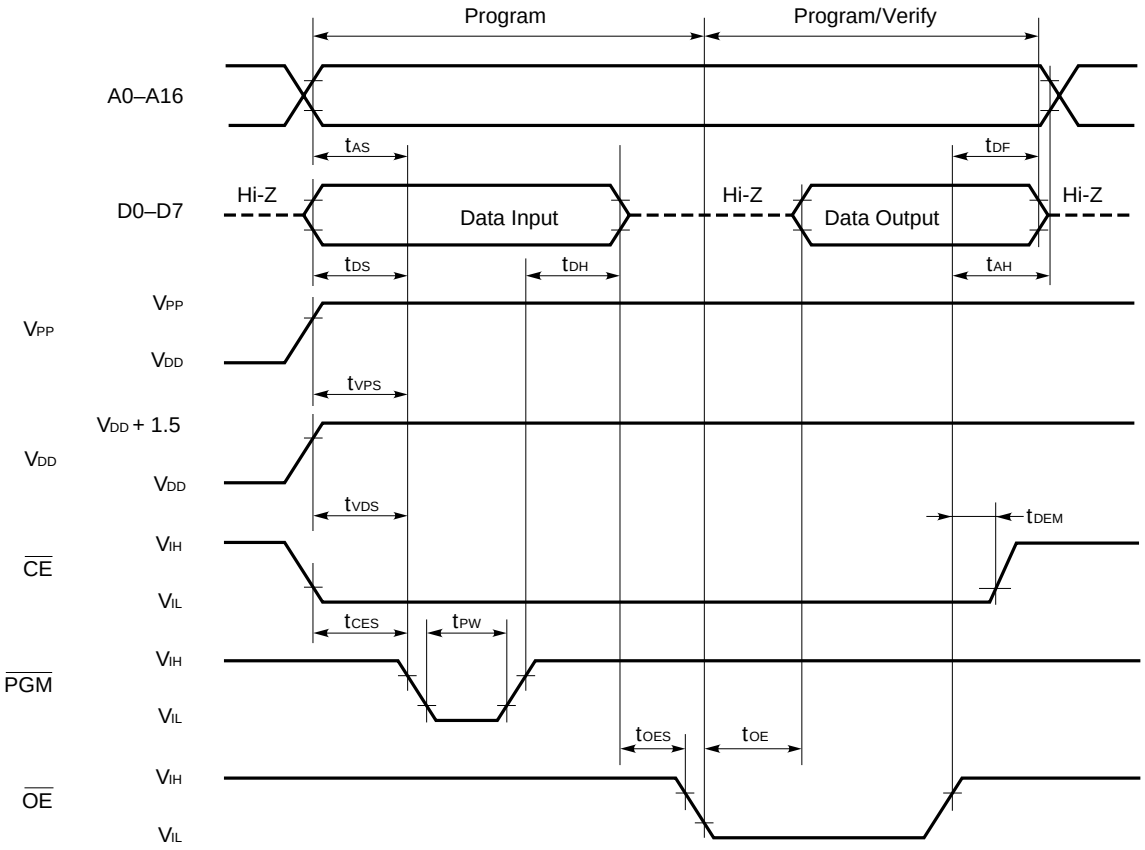
(3) PROM Programming Mode Setting (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (Page program mode)



PROM Write Mode Timing (Byte program mode)

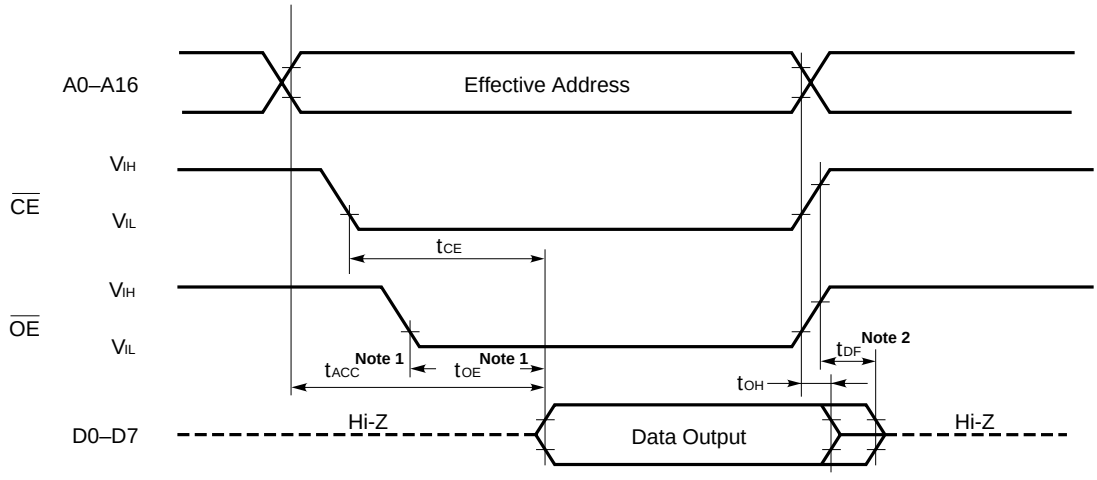


Cautions 1. V_{DD} must be applied before V_{PP} and cut off after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Removing and reinserting may adversely affect in reliability while +12.5 V is applied to V_{PP}.

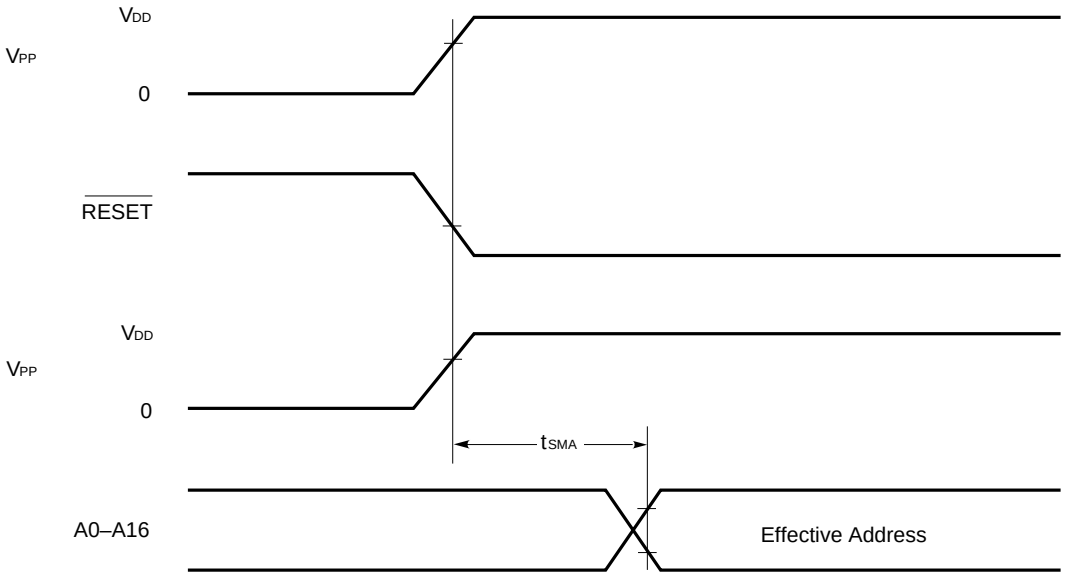
PROM Read Mode Timing



Notes 1. When reading within the t_{ACC} range, the $\overline{OE}$ input delay time from the $\overline{CE}$ fall time must be maximum of $t_{ACC} - t_{OE}$.

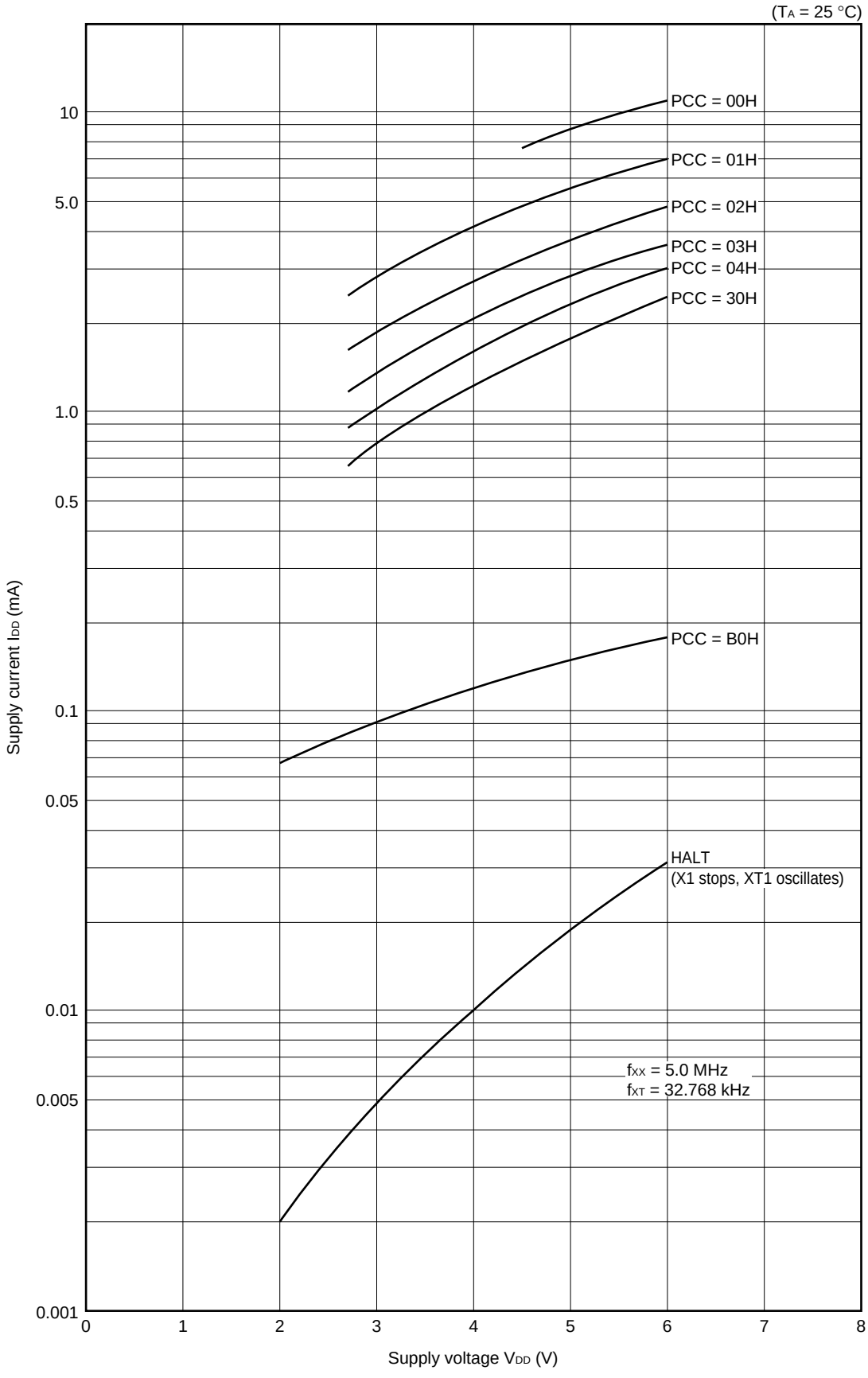
2. t_{DF} is the time from the point at which either $\overline{OE}$ or $\overline{CE}$ (whichever is first) reaches V_{IH}.

PROM Programming Mode Setting Timing

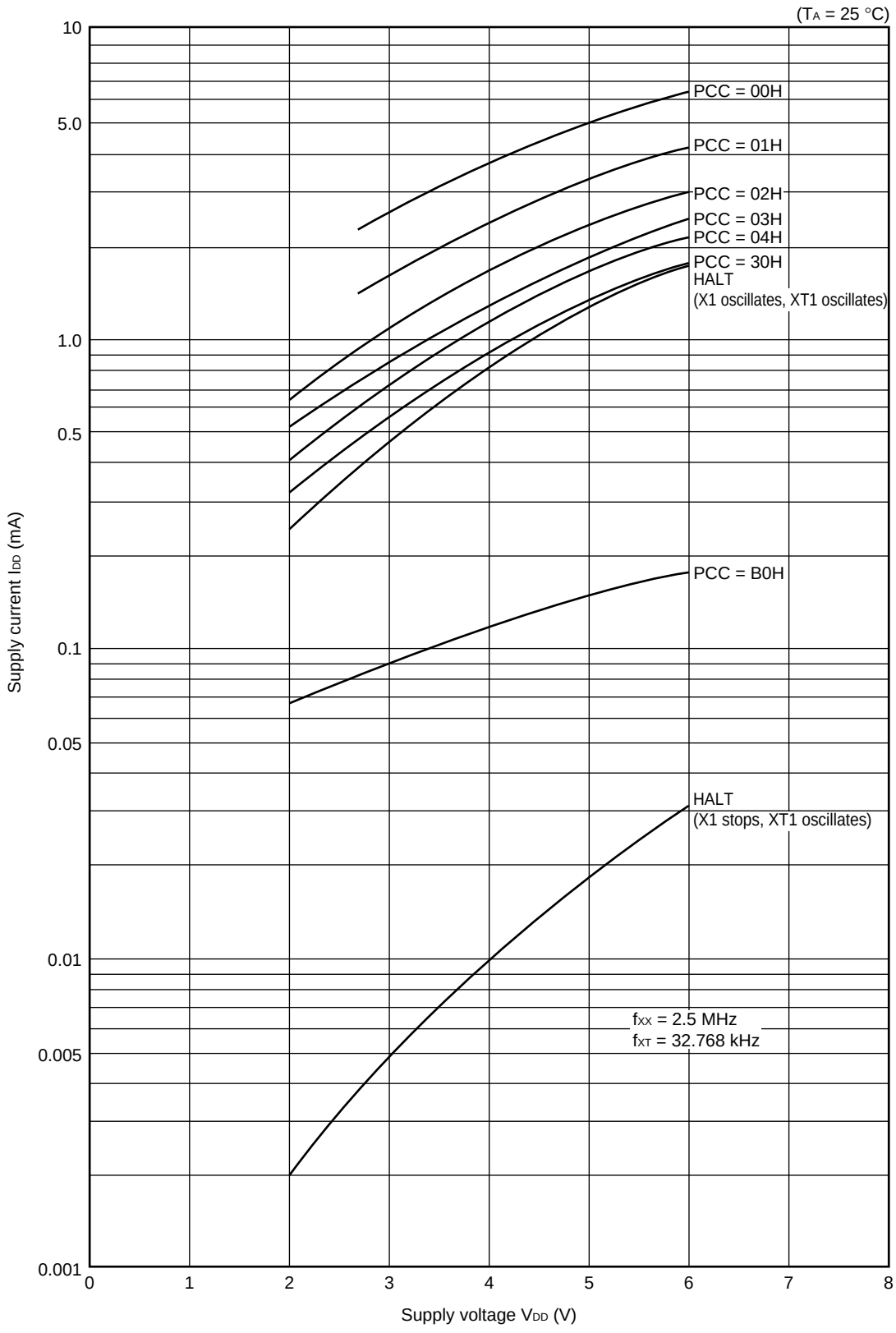


★ 9. CHARACTERISTIC CURVES (REFERENCE VALUES)

I_{DD} vs V_{DD} (f_X = f_{XX} = 5.0 MHz)

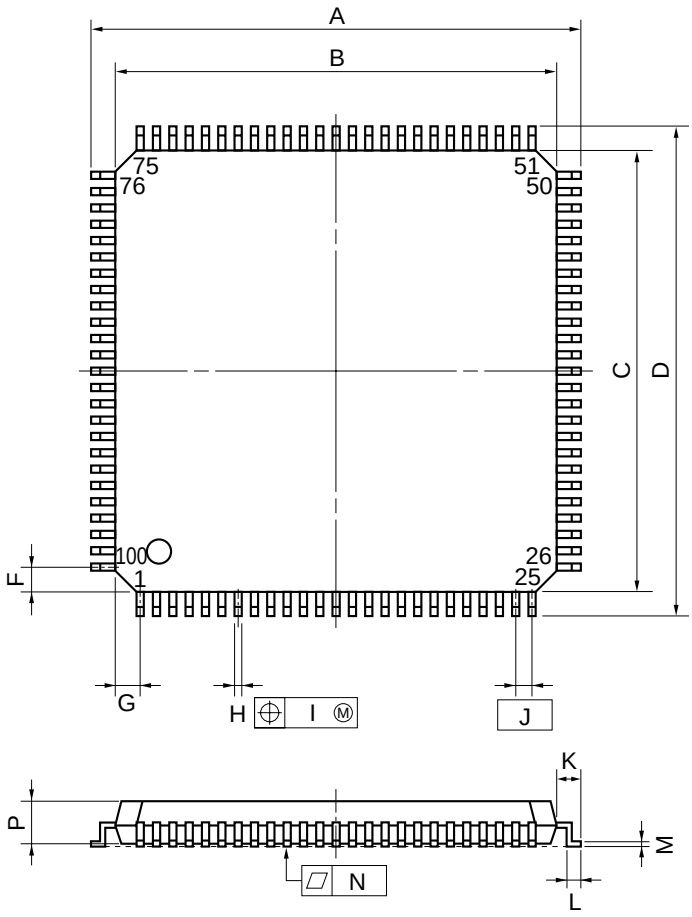


I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)

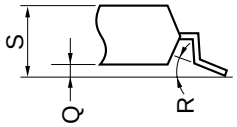


10. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



detail of lead end



NOTE

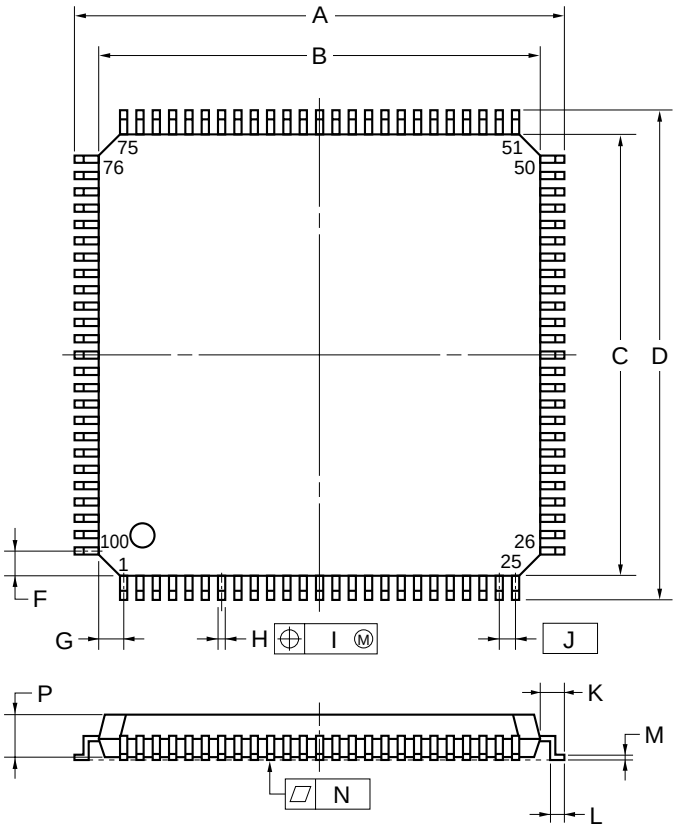
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

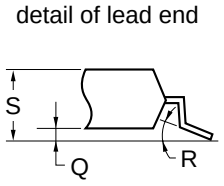
ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

Remark Dimensions and materials of ES products are the same as those of the mass production product.

★ 100 PIN PLASTIC LQFP (FINE PITCH) (14×14)





NOTE

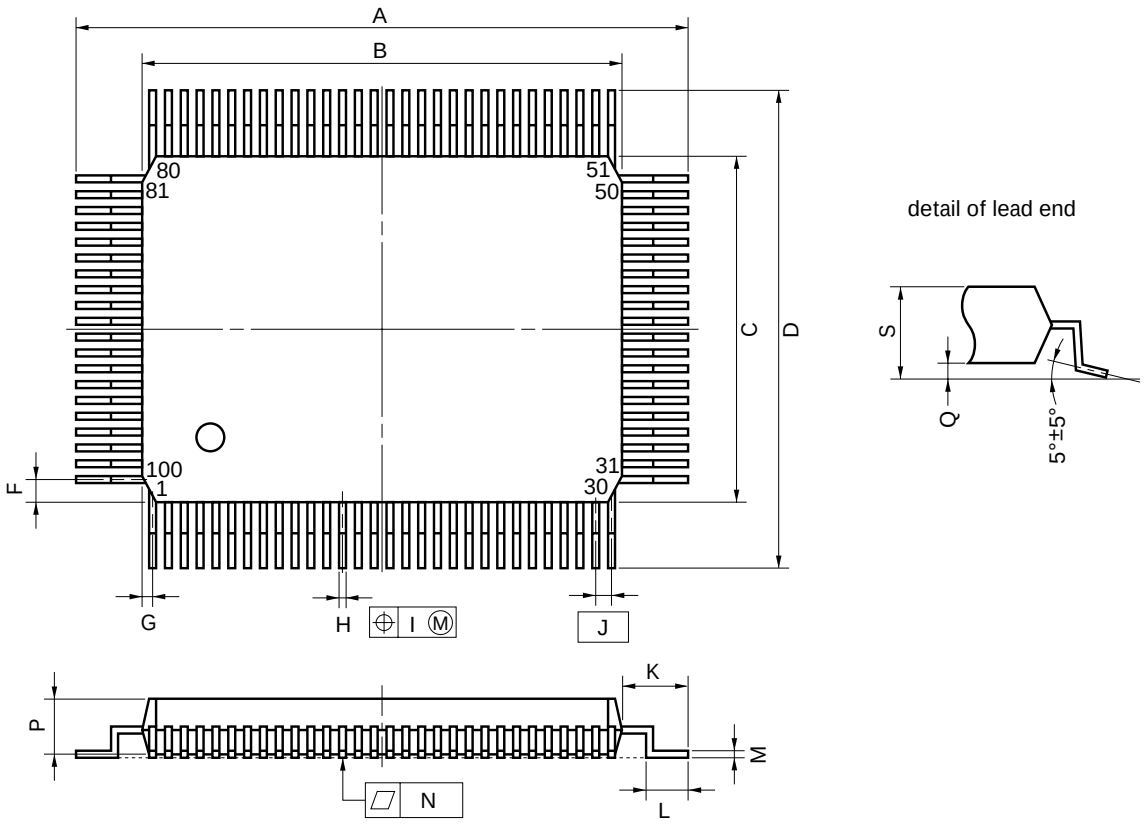
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

Remark Dimensions and materials of ES products are the same as those of the mass production product.

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

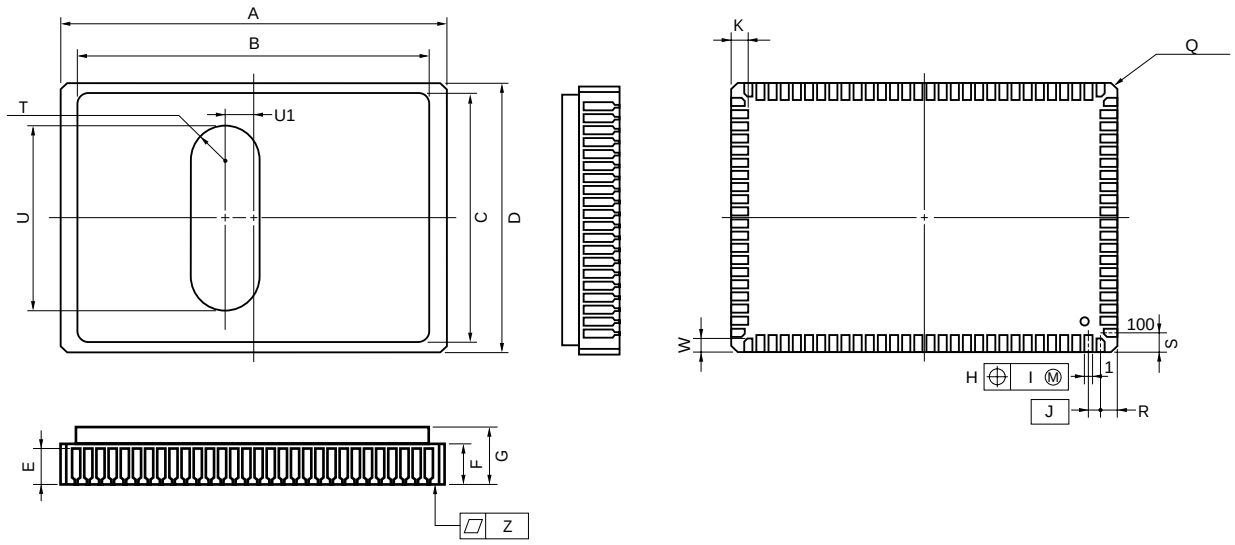
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark Dimensions and materials of ES products are the same as those of the mass production product.

100 PIN CERAMIC WQFN



X100KL-65A

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.6±0.27	0.811±0.011
B	19.0	0.748
C	13.8	0.543
D	14.6±0.27	0.575±0.011
E	1.94	0.076
F	2.14	0.084
G	3.5 MAX.	0.138 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65	0.026
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	0.875	0.034
S	1.125	0.044
T	R 1.925	R 0.076
U	8.45	0.333
U1	1.75	0.069
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$
Z	0.10	0.004

★ 11. RECOMMENDED SOLDERING CONDITIONS

The μPD78P064 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 11-1. Surface Mounting Type Soldering Conditions

(1) μPD78P064GC-7EA: 100-pin plastic QFP (fine pitch) (14 × 14 mm)
μPD78P064GC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Soldering Symbols
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max., Time limit: 7 days[Note] (thereafter 10 hours prebaking required at 125 °C) <Precaution> Products cannot be baked while packed in anything other than in a heat resistant tray (i.e. they cannot be baked in a magazine, taping, or heat-labile tray).	IR35-107-2
VPS	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max., Time limit: 7 days[Note] (thereafter 10 hours prebaking required at 125 °C) <Precaution> Products cannot be baked while packed in anything other than in a heat resistant tray (i.e. they cannot be baked in a magazine, taping, or heat-labile tray).	VP15-107-2
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

(2) μPD78P064GF-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Soldering Symbols
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Duration: 40 sec. (at 200 °C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature: 260 °C max., Duration: 10 sec. max., Number of times: Once, Preheating temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78P064.

Language Processing Software

RA78K/0[Note 1, 2, 3, 4]	78K/0 series common assembler package
CC78K/0[Note 1, 2, 3, 4]	78K/0 series common C compiler package
DF78064[Note 1, 2, 3, 4]	Device file for μPD78064 subseries
CC78K/0-L[Note 1, 2, 3, 4]	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P0308GC (PA-78P064GC[Note 8])	Programmer adapters connected to PG-1500
PA-78P0308GF (PA-78P064GF[Note 8])	
PA-78P0308KL-T (PA-78P064KL-T[Note 8])	
PA-PG-1500 controller[Note 1, 2]	PG-1500 control program

Debugging Tools

IE-78000-R	78K/0 series common in-circuit emulators
IE-78000-R-A	78K/0 series common in-circuit emulators (for integrated debugger)
IE-78000-R-BK	78K/0 series common break board
IE-780308-R-EM	μPD780308 subseries common emulation boards
IE-78000-R-SV3	Interface adapter and cable when an EWS is used as the host machine (for IE-78000-R-A)
IE-70000-98-IF-B	Interface adapter when PC-9800 series (except notebook PC) is used as the host machine (for IE-78000-R-A)
IE-70000-98N-IF	Interface adapter and cable when PC-9800 series notebook PC is used as the host machine (for IE-78000-R-A)
IE-70000-PC-IF-B	Interface adapter when IBM PC/AT™ is used as the host machine (for IE-78000-R-A)
EP-78064GC-R	μPD78064 subseries common emulation probes
EP-78064GF-R	
TGC-100SDW	Adapter to be mounted on a target system board made for 100-pin plastic QFP (GC-7EA, GC-8EU type) A product of Tokyo Eletech Corp. (Tokyo 03-5295-1661). When purchasing this product, consult your NEC distributor.
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
EV-9900	Jig used to remove μPD78P064KL-T from EV-9200GF-100
SM78K0[Note 5, 6, 7]	78K/0 series common system simulators
ID78K0[Note 4, 5, 6, 7]	IE-78000-R-A integrated debuggers
SD78K/0[Note 1, 2]	IE-78000-R screen debuggers
DF78064[Note 1, 2, 4, 5, 6, 7]	Device file for μPD78064 subseries

Real-Time OS

RX78K/0[Note 1, 2, 3, 4]	78K/0 series real-time OS
MX78K/0[Note 1, 2, 3, 4]	78K/0 series OS

Fuzzy Inference Development Support System

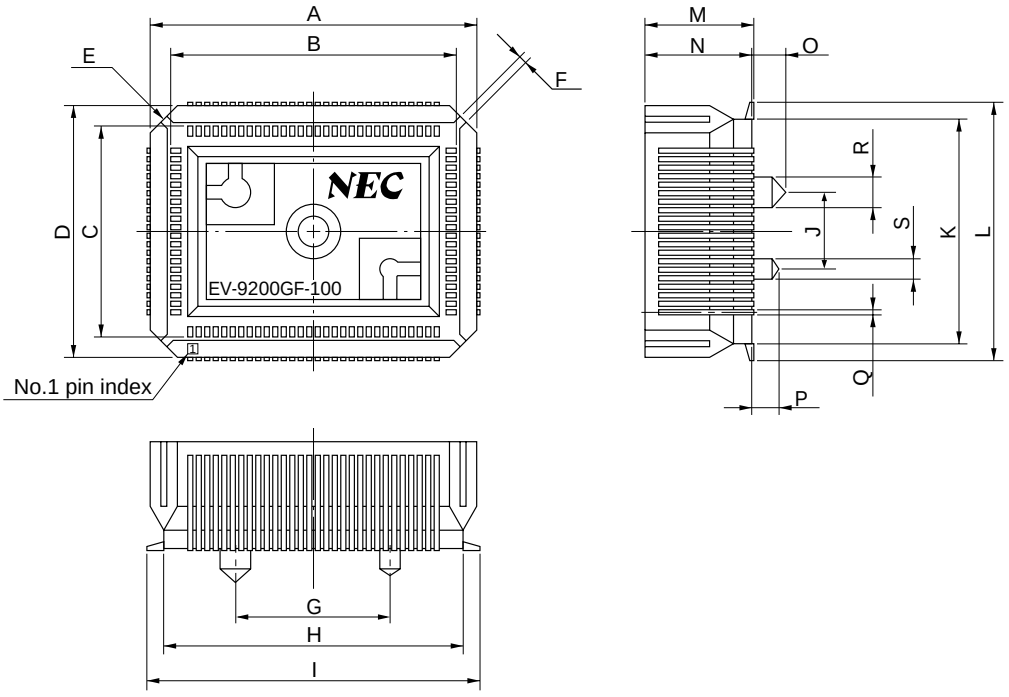
FE9000[Note 1], FE9200[Note 6]	Fuzzy knowledge data creation tool
FT9080[Note 1], FT9085[Note 2]	Translator
FI78K/II[Note 1, 2]	Fuzzy inference module
FD78K/II[Note 1, 2]	Fussy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT and compatible machines (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible machines (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Maintenance Product

Remarks 1. For third party development tools, refer to **78K/0 Series Selection Guide (U11126E)**.
2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with DF78064.

CONVERSION SOCKET (EV-9200GF-100) PACKAGE DRAWINGS AND RECOMMENDED BOARD MOUNTING PATTERN

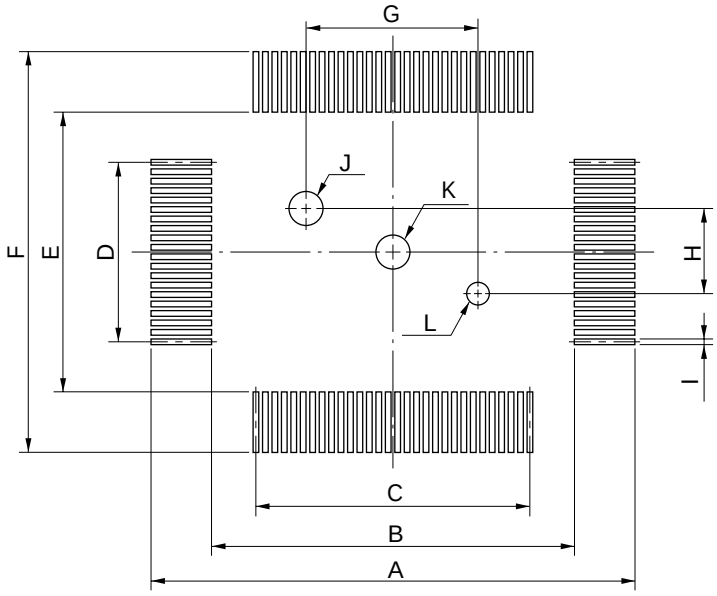
Figure A-1. EV-9200GF-100 Package Drawing



EV-9200GF-100-G0E

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	076
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. EV-9200GF-100 Board Mounting Pattern



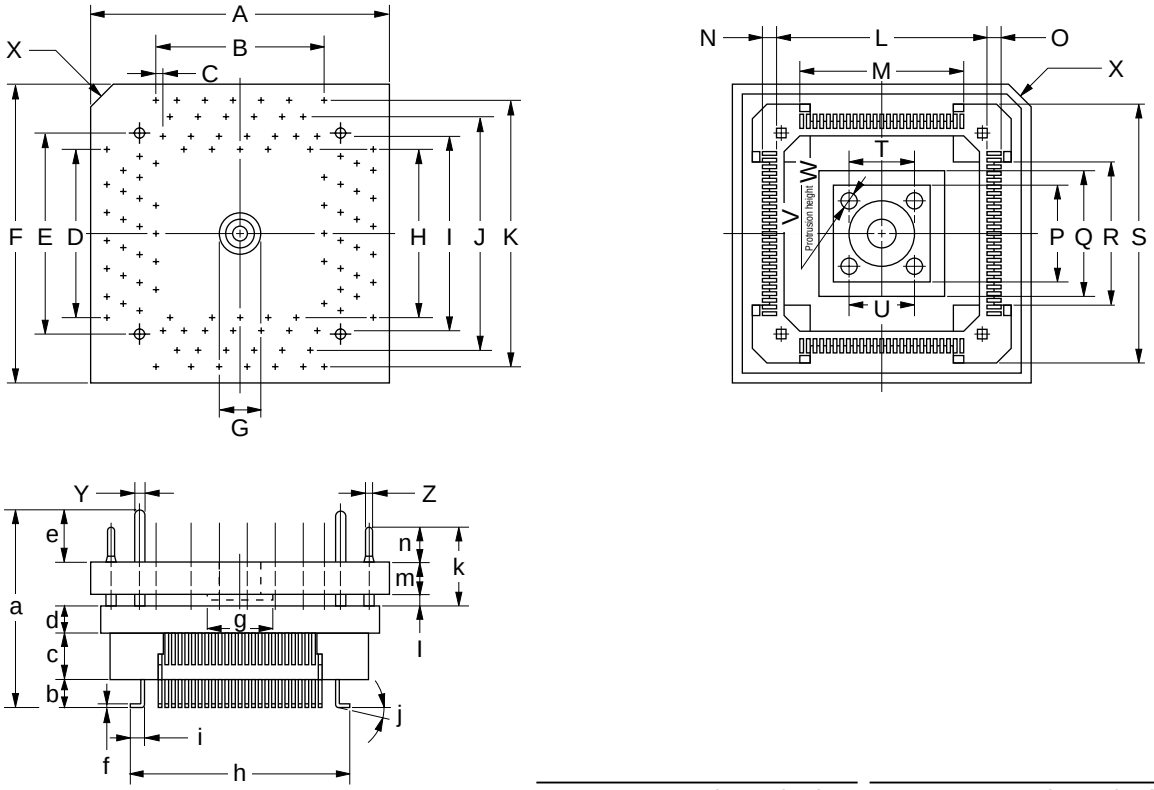
EV-9200GF-100-P1E

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65\pm0.02\times29=18.85\pm0.05$	$0.026^{+0.001}_{-0.002}\times1.142=0.742^{+0.002}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

★ **CONVERSION ADAPTER (TGC-100SDW) PACKAGE DRAWINGS**

Figure A-3. TGC-100SDW Package Drawing



ITEM	MILLIMETERS	INCHES
A	21.55	0.848
B	0.5x24=12	0.020x0.945=0.472
C	0.5	0.020
D	0.5x24=12	0.020x0.945=0.472
E	15.0	0.591
F	21.55	0.848
G	ϕ3.55	ϕ0.140
H	10.9	0.429
I	13.3	0.524
J	15.7	0.618
K	18.1	0.713
L	13.75	0.541
M	0.5x24=12.0	0.020x0.945=0.472
N	1.125±0.3	0.044±0.012
O	1.125±0.2	0.044±0.008
P	7.5	0.295
Q	10.0	0.394
R	11.3	0.445
S	18.1	0.713
T	ϕ5.0	ϕ0.197
U	5.0	0.197
V	4-ϕ1.3	4-ϕ0.051
W	1.8	0.071
X	C 2.0	C 0.079
Y	ϕ0.9	ϕ0.035
Z	ϕ0.3	ϕ0.012

ITEM	MILLIMETERS	INCHES
a	14.45	0.569
b	1.85±0.25	0.073±0.010
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	0.25	0.010
g	ϕ4.5	ϕ0.177
h	16.0	0.630
i	1.125±0.3	0.044±0.012
j	0~5°	0.000~0.197°
k	5.9	0.232
l	0.8	0.031
m	2.4	0.094
n	2.7	0.106

TGC-100SDW-G0E

Remark Manufactured by Tokyo Eletech Corp.

★ APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No.	
		Japanese	English
μPD78064, 78064Y Subseries User's Manual		U10105J	U10105E
μPD78062, 78063, 78064 Data Sheet		U12338J	U12338E
μPD78P064 Data Sheet		U11589J	This document
78K/0 Series User's Manual (Instruction)		U12326J	U12326E
78K/0 Series Instruction Table		U10903J	—
78K/0 Series Instruction Set		U10904J	—
μPD78064 Subseries Special Function Register Table		IEM-6568	—
78K/0 Series Application Note	Fundamental (III)	U10182J	U10182E
	Floating-point arithmetic operation program	IEA-718	IEA-1289

Development Tool Related Documents (User's Manual) (1/2)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly language	U11801J	U11801E
	Structured assembly language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	U11940E
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		U11376J	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-780308-R-EM		U11362J	U11362E
EP-78064		EEU-934	EEU-1469

Development Tool Related Documents (User's Manual) (2/2)

Document Name		Document No.	
		Japanese	English
SM78K0 System Sumilator Windows Based	Reference	EEU-5002	U10181E
SM78K Series System Simulator	External components user open interface specification	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
SD78K/0 Screen Debugger	Introduction	EEU-852	U10539E
PC-9800 Series (MS-DOS) Based	Reference	U10952J	—
SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) Based	Reference	U11279J	U11279E

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

Embedded Software Related Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Fundamental	U11537J	—
	Installation	U11536J	—
78K/0 Series OS MX78K0	Fundamental	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Related Documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Devices Quality Guarantee Guide	C11893J	MEI-1202
Microcomputer-Related Product Guide (Products by Other Manufacturers)	U11416J	—

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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