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MOS INTEGRATED CIRCUIT

μPD78F0974

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F0974 is a product of the μPD780973 Subseries in the 78K/0 Series and equivalent to the μPD780973(A) with a flash memory in place of internal ROM.

This device can be programmed without being removed from the substrate.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μPD780973 Subseries User's Manual : U12406E
78K/0 Series User's Manual -Instruction : U12326E

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory : 32 Kbytes**Note**
- Internal high-speed RAM : 1024 bytes**Note**
- Inclusion of EEPROM™ which can be read/written by software: 256 bytes
- Operable with the same power supply voltage as that of mask ROM version (V_{DD} = 4.5 to 5.5 V)

Note The flash memory and internal high-speed RAM capacities can be changed with the memory size switching register (IMS).

Remark For the difference between the flash memory version and the mask ROM version, refer to **1. DIFFERENCES BETWEEN μPD78F0974 AND MASK ROM VERSION.**

APPLICATION FIELD

Automotive meter (dashboard) control

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0974GF-3B9	80-pin plastic QFP (14 × 20 mm)	Flash memory

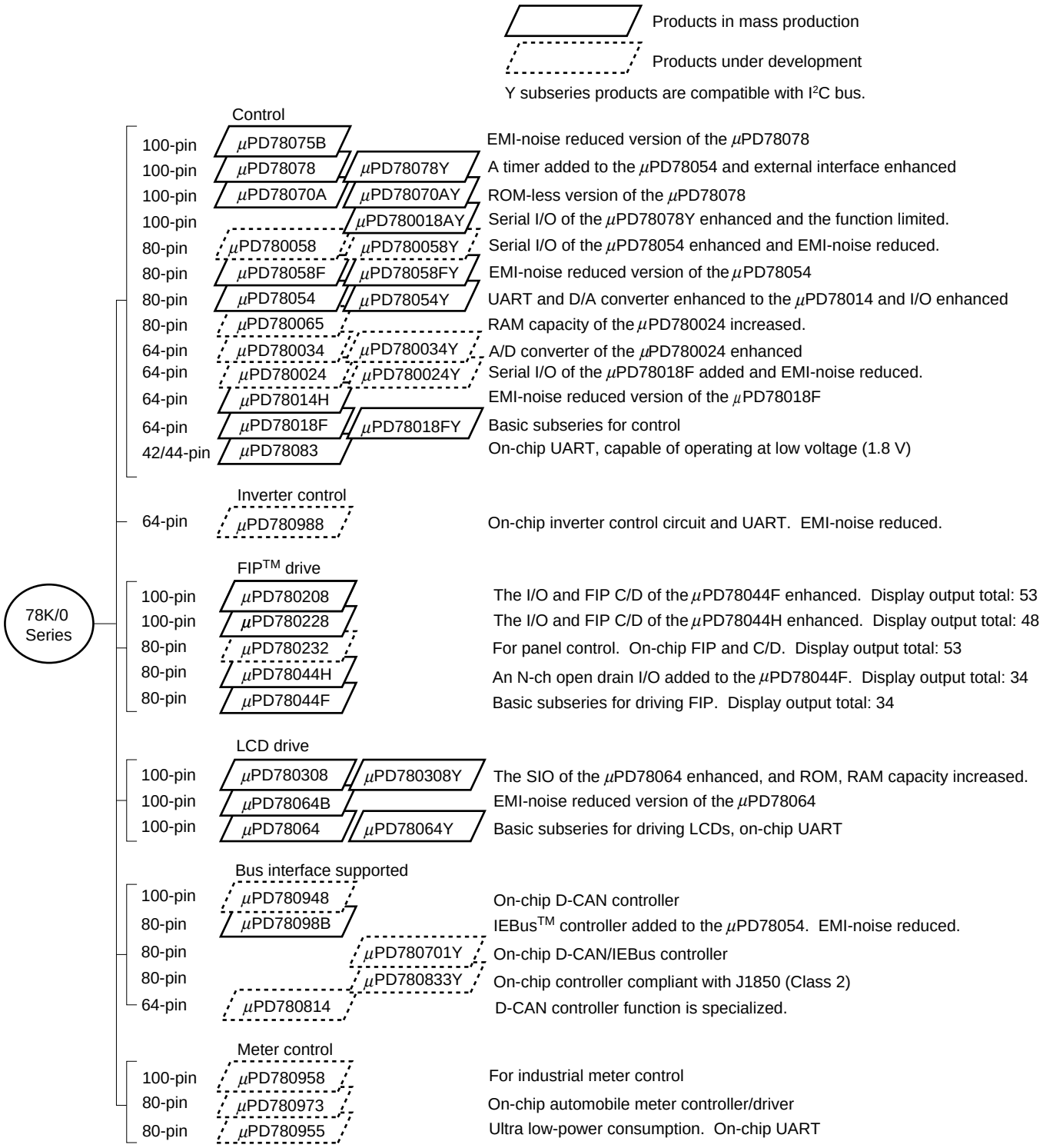
The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Document No. U12646EJ2V1PM00 (2nd edition)
Date Published April 1999 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ 78K/0 SERIES DEVELOPMENT

The following shows the products organized according to usage. The names in the parallelograms are subseries name.



The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32 K-40 K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1 ch)	88	1.8 V	Yes
	μPD78078	48 K-60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K-60 K	2ch							3ch (time-division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K-60 K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16 K-60 K										2.0 V	
	μPD780065	40 K-48 K							–	4ch (UART: 1 ch)	60	2.7 V	
	μPD780034	8 K-32 K					–	8ch		3ch (UART: 1ch,	51	1.8 V	
	μPD780024						8ch	–		time-division 3-wire: 1ch)			
	μPD78014H									2ch	53		
	μPD78018F	8 K-60 K											
	μPD78083	8 K-16 K		–	–					1ch (UART: 1ch)	33		–
Inverter control	μPD780988	32 K-60 K	3ch	**Note**	–	1ch	–	8ch	–	3ch (UART: 2ch)	47	4.0 V	Yes
FIP drive	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48 K-60 K	3ch	–	–					1ch	72	4.5 V	
	μPD780232	16 K-24 K					4ch			2ch	40		
	μPD78044H	32 K-48 K	2ch	1ch	1ch		8ch			1ch	68	2.7 V	
	μPD78044F	16 K-40 K								2ch			
LCD drive	μPD780308	48 K-60 K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time-division UART: 1ch)	57	2.0 V	–
	μPD78064B	32 K								2ch (UART: 1ch)			
	μPD78064	16 K-32 K											
Bus interface compatible	μPD780948	60 K	2ch	2ch	1ch	1ch	8ch	–	–	3ch (UART: 1ch)	79	4.0 V	Yes
	μPD78098B	40 K-60 K		1ch					2ch		69	2.7 V	–
	μPD780814	32 K-60 K		2ch			12ch		–	2ch (UART: 1ch)	46	4.0 V	
Meter control	μPD780958	48 K-60 K	4ch	2ch	–	1ch	–	–	–	2ch (UART: 1ch)	69	2.2 V	–
	μPD780973	24 K-32 K	3ch	1ch	1ch		5ch				56	4.5 V	
	μPD780955	40 K	6ch		–		1ch			2ch (UART: 2ch)	50	2.2 V	

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

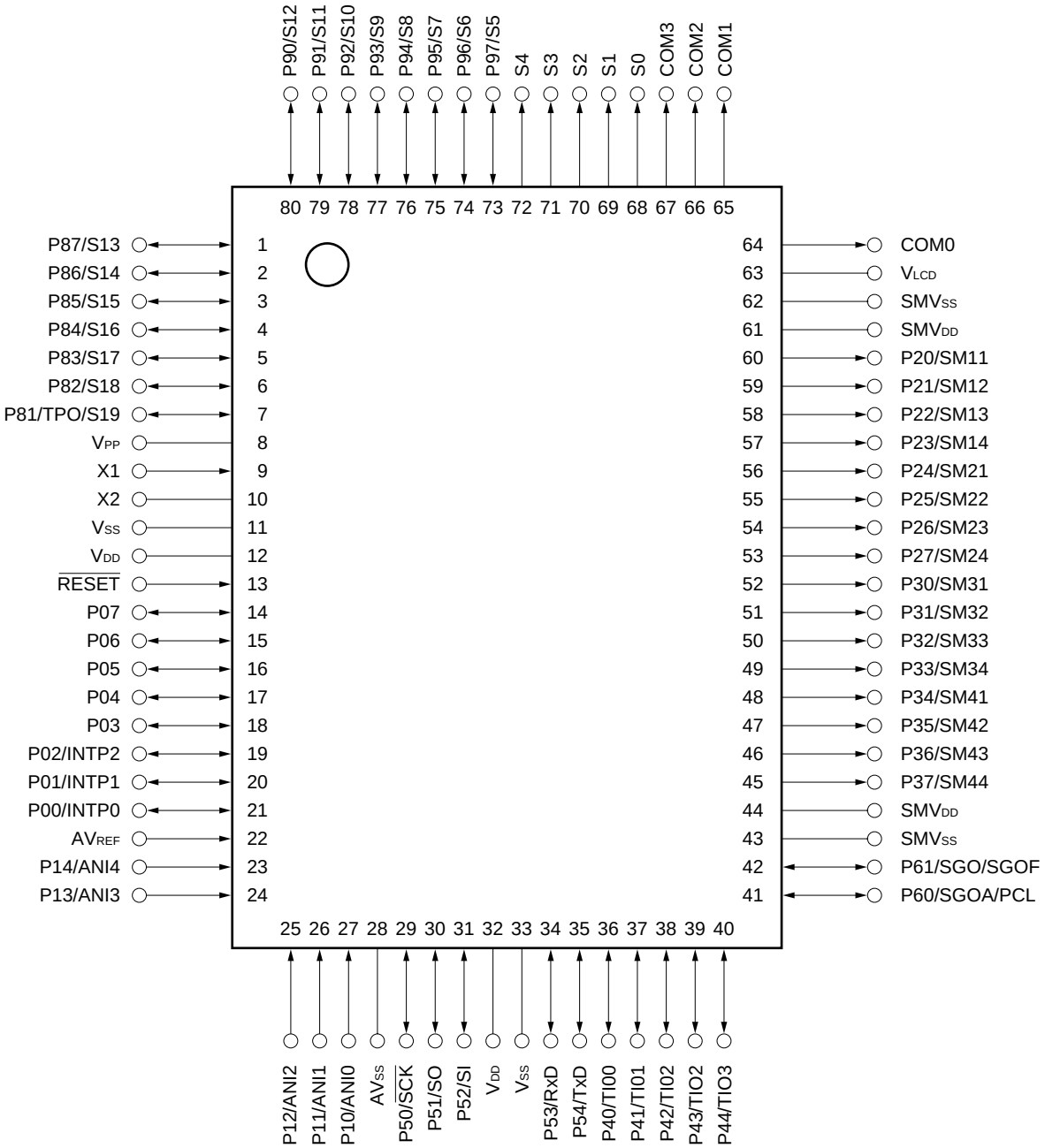
FUNCTION OVERVIEW

Item		Function
Internal Memory	Flash Memory	32 Kbytes[Note]
	High-speed RAM	1024 bytes[Note]
	EEPROM	256 bytes
	LCD display RAM	20 × 4 bits
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip minimum instruction execution time cycle modification function 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38 MHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, boolean operation) • BCD correction, etc.
I/O ports (Including segment signal output pins)		Total : 56 • CMOS input : 5 • CMOS output : 16 • CMOS I/O : 35
A/D converter		• 8-bit resolution × 5 channels • Power fail detector
LCD controller/driver		• Segment signal output : Maximum 20 • Common signal output : Maximum 4 • Bias : 1/3
Serial interface		• 3-wire serial I/O mode : 1 channel • UART mode : 1 channel
Timer		• 16-bit timer : 1 channel • 8-bit timer : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		2 (8-bit PWM output capability: 2)
Meter controller/driver		PWM output (8-bit resolution): 16
Sound generator		1 channel
Clock output		65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.04 MHz, 2.09 MHz, 4.19 MHz, 8.38 MHz (main system clock: at 8.38 MHz operation)
Vectored-interrupt source	Maskable	Internal : 16 External : 3
	Non-maskable	Internal : 1
	Software	1
Supply voltage		V_{DD} (SMV_{DD}) = 4.5 to 5.5 V
Operation ambient temperature		T_A = –40 to +85 °C
Package		80-pin plastic QFP (14 × 20 mm)

Note The capacities of the flash memory and the internal high-speed RAM can be changed with the memory size switching register (IMS).

PIN CONFIGURATION (TOP VIEW)

- **80-Pin Plastic QFP (14 × 20 mm)**
  μPD78F0974GF-3B9



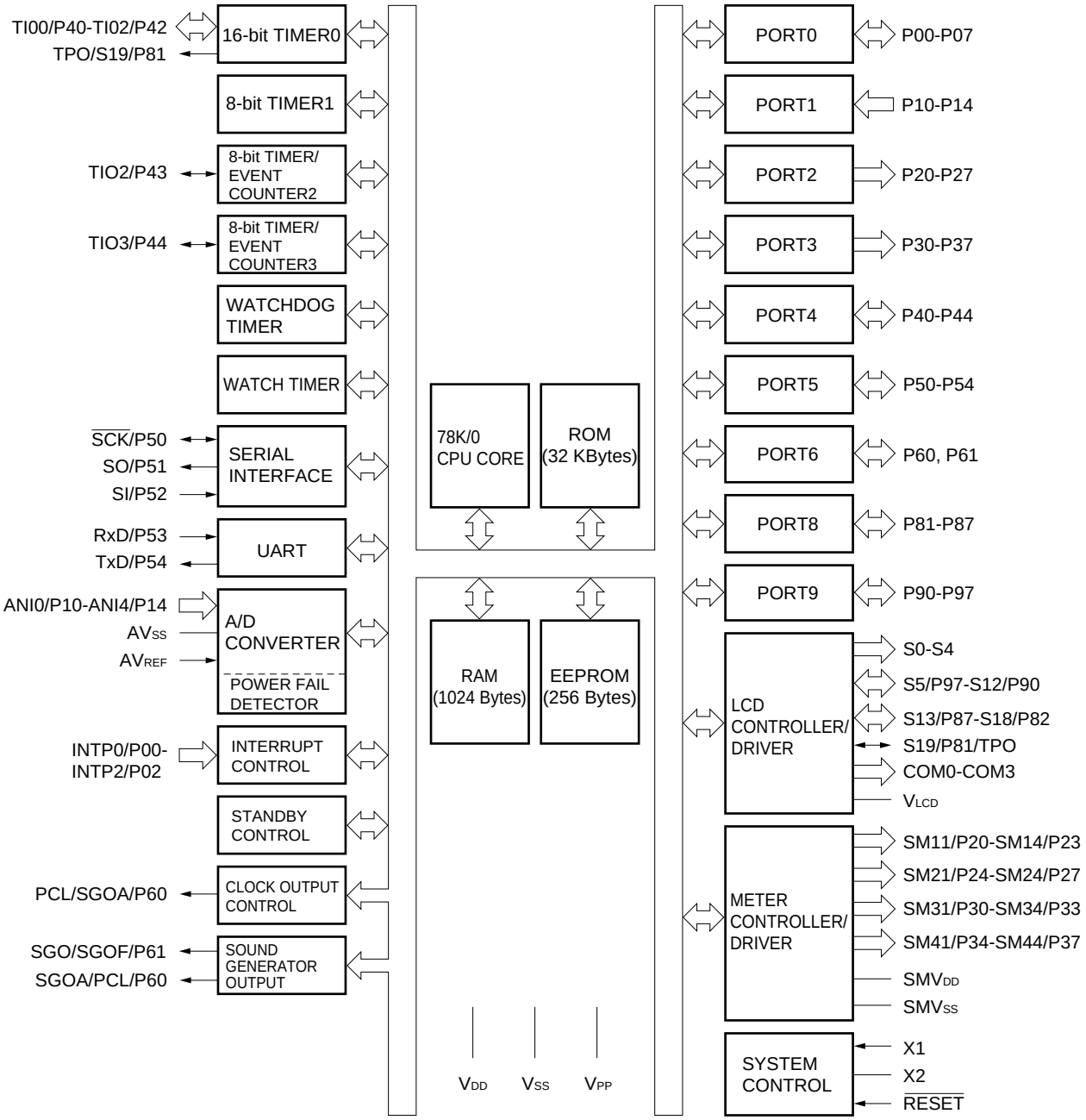
Cautions 1. Connect the V_{PP} pin directly to V_{SS} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS}.

Remark When the μPD78F0974 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to 2 V_{DD}s individually and connecting V_{SS} to different ground lines, is recommended.

ANI0-ANI4 : Analog Input
AV_{REF} : Analog Reference Voltage
AV_{SS} : Analog Ground
COM0-COM3 : Common Output
INTP0-INTP2 : Interrupt from Peripherals
P00-P07 : Port 0
P10-P14 : Port 1
P20-P27 : Port 2
P30-P37 : Port 3
P40-P44 : Port 4
P50-P54 : Port 5
P60, P61 : Port 6
P81-P87 : Port 8
P90-P97 : Port 9
PCL : Programmable Clock Output
$\overline{RESET}$: Reset
RxD : Receive Data
S0-S19 : Segment Output
$\overline{SCK}$: Serial Clock
SGO : Sound Generator Output
SGOA : Sound Generator Amplitude Output
SGOF : Sound Generator Frequency Output
SI : Serial Input
SM11-SM14, SM21-SM24, SM31-SM34, SM41-SM44 : Meter Output
SMV_{DD} : Meter Controller Power Supply
SMV_{SS} : Meter Controller Ground
SO : Serial Output
TI00-TI02 : Timer Input
TIO2, TIO3 : Timer Output/Event Counter Input
TPO : Prescaler Output
TxD : Transmit Data
V_{DD} : Power Supply
V_{LCD} : LCD Power Supply
V_{PP} : Programming Power Supply
V_{SS} : Ground
X1, X2 : Crystal (Main System Clock)

BLOCK DIAGRAM



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1. DIFFERENCES BETWEEN μPD78F0974 AND MASK ROM VERSION

The μPD78F0974 is a product provided with a flash memory which enables on-board reading, erasing, and rewriting of programs with device mounted on target system.

The functions of the μPD78F0974 (except the functions specified for flash memory) can be made the same as those of the mask ROM version by setting the memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory version (μPD78F0974) and the mask ROM version (μPD780973(A)).

Table 1-1. Differences between μPD78F0974 and Mask ROM Version

Item	μPD78F0974	μPD780973(A)
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacity	32 Kbytes	24 Kbytes
Internal high-speed RAM capacity	1024 bytes	768 bytes
Internal ROM and internal high-speed RAM capacity changeable/not changeable with memory size switching register	Changeable[Note]	Not changeable
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided
Electrical specifications	Refer to the data sheet of individual products.	
Quality grade	Standard	Special

Note The default is CFH, but set the value as indicated below.

IMS Set Value	Flash Memory	Internal High-speed RAM	Remarks
06H	24 Kbytes	768 bytes	When making to the same as the memory mapping of μPD780973(A)
C8H	32 Kbytes	1024 bytes	At maximum

2. PIN FUNCTIONS

2.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P02	I/O	Port 0	Input	INTP0 to INTP2
P03 to P07		8-bit input/output port. Input/output can be specified bit-wise. An internal pull-up resistor can be connected by software.		–
P10 to P14	Input	Port 1 5-bit input only port.	Input	ANI0 to ANI4
P20 to P23	Output	Port 2	Hi-Z	SM11 to SM14
P24 to P27		8-bit output only port.		SM21 to SM24
P30 to P33	Output	Port 3	Hi-Z	SM31 to SM34
P34 to P37		8-bit output only port.		SM41 to SM44
P40 to P42	I/O	Port 4 5-bit input/output port.	Input	TI00 to TI02
P43, P44		Input/output can be specified bit-wise.		TIO2, TIO3
P50	I/O	Port 5	Input	$\overline{SCK}$
P51		5-bit input/output port.		SO
P52		Input/output can be specified bit-wise.		SI
P53				RxD
P54				TxD
P60	I/O	Port 6	Input	PCL/SGOA
P61		2-bit input/output port. Input/output can be specified bit-wise.		SGO/SGOF
P81	I/O	Port 8	Input	S19/TPO
P82 to P87		7-bit input/output port. Input/output can be specified bit-wise. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD display control register (LCDC).		S18 to S13
P90 to P97	I/O	Port 9 8-bit input/output port. Input/output can be specified bit-wise. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD display control register (LCDC).	Input	S12 to S5

2.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP2	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00 to P02
SI	Input	Serial interface serial data input	Input	P52
SO	Output	Serial interface serial data output	Input	P51
$\overline{SCK}$	I/O	Serial interface serial clock input/output	Input	P50
RxD	Input	Serial data input for asynchronous serial interface	Input	P53
TxD	Output	Serial data output for asynchronous serial interface	Input	P54
TI00	Input	Capture trigger signal input to capture register (CR00)	Input	P40
TI01		Capture trigger signal input to capture register (CR01)		P41
TI02		Capture trigger signal input to capture register (CR02)		P42
TIO2	I/O	8-bit timer (TM2) input/output (shared with 8-bit PWM output)	Input	P43
TIO3		8-bit timer (TM3) input/output (shared with 8-bit PWM output)		P44
TPO	Output	16-bit timer (TM0) prescaler output	Input	P81/S19
PCL	Output	Clock output (for trimming of main system clock)	Input	SGOA/P60
SGOA	Output	Sound generator signal output	Input	PCL/P60
SGOF				SGO/P61
SGO				SGOF/P61
S0 to S4	Output	LCD controller/driver segment signal output	Output	–
S5 to S12			Input	P97 to P90
S13 to S18				P87 to P82
S19				P81/TPO
COM0 to COM3	Output	LCD controller/driver common signal output	Output	–
V_{LCD}	–	LCD drive voltage	–	–
SM11 to SM14	Output	Meter control signal output	Hi-Z	P20 to P23
SM21 to SM24				P24 to P27
SM31 to SM34				P30 to P33
SM41 to SM44				P34 to P37
ANI0 to ANI4	Input	A/D converter analog input	Input	P10 to P14
AV_{REF}	Input	A/D converter reference voltage input (shared with analog power supply)	–	–
AV_{SS}	–	A/D converter ground potential. Connect to V_{SS}.	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Main system clock oscillation crystal connection	–	–
X2	–		–	–
SMV_{DD}	–	Power supply for meter controller/driver	–	–
SMV_{SS}	–	Ground potential for meter controller/driver	–	–
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
V_{PP}	–	Applying high-voltage for program write/verify. Connected directly to V_{SS} in normal operation mode.	–	–

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output circuit configuration of each type, see Figure 2-1.

Table 2-1. Input/Output Circuit Type of Each Pin

	Pin Name	Input/output Circuit Type	I/O	Recommended Connection When Not Used
	P00/INTP0-P02/INTP2	8-A	Input/output	Independently connect to V_{SS} through resistor.
	P03 to P07			
	P10/ANI0 to P14/ANI4	9	Input	Independently connect to V_{DD} or V_{SS} through resistor.
★	P20/SM11 to P23/SM14	4	Output	Leave open.
	P24/SM21 to P27/SM24			
	P30/SM31 to P33/SM34			
	P34/SM41 to P37/SM44			
	P40/TI00 to P42/TI02	8	Input/output	Independently connect to V_{DD} or V_{SS} through resistor.
	P43/TIO2			
	P44/TIO3			
	P50/$\overline{SCK}$			
	P51/SO	5		
	P52/SI	8		
	P53/RxD			
	P54/TxD	5		
	P60/SGOA/PCL			
	P61/SGO/SGOF			
★	P81/S19/TPO	17-G		
	P82/S18 to P87/S13			
	P90/S12 to P97/S5			
	S0-S4	17	Output	Leave open.
	COM0 to COM3	18		
	V_{LCD}	–	–	
	$\overline{RESET}$	2	Input	Connect to V_{DD}.
	SMV_{DD}	–	–	
	SMV_{SS}			Connect to V_{SS}.
	AV_{REF}			
	AV_{SS}			
	V_{PP}			Directly connect to V_{SS}.

Figure 2-1. Pin Input/Output Circuits (1/2)

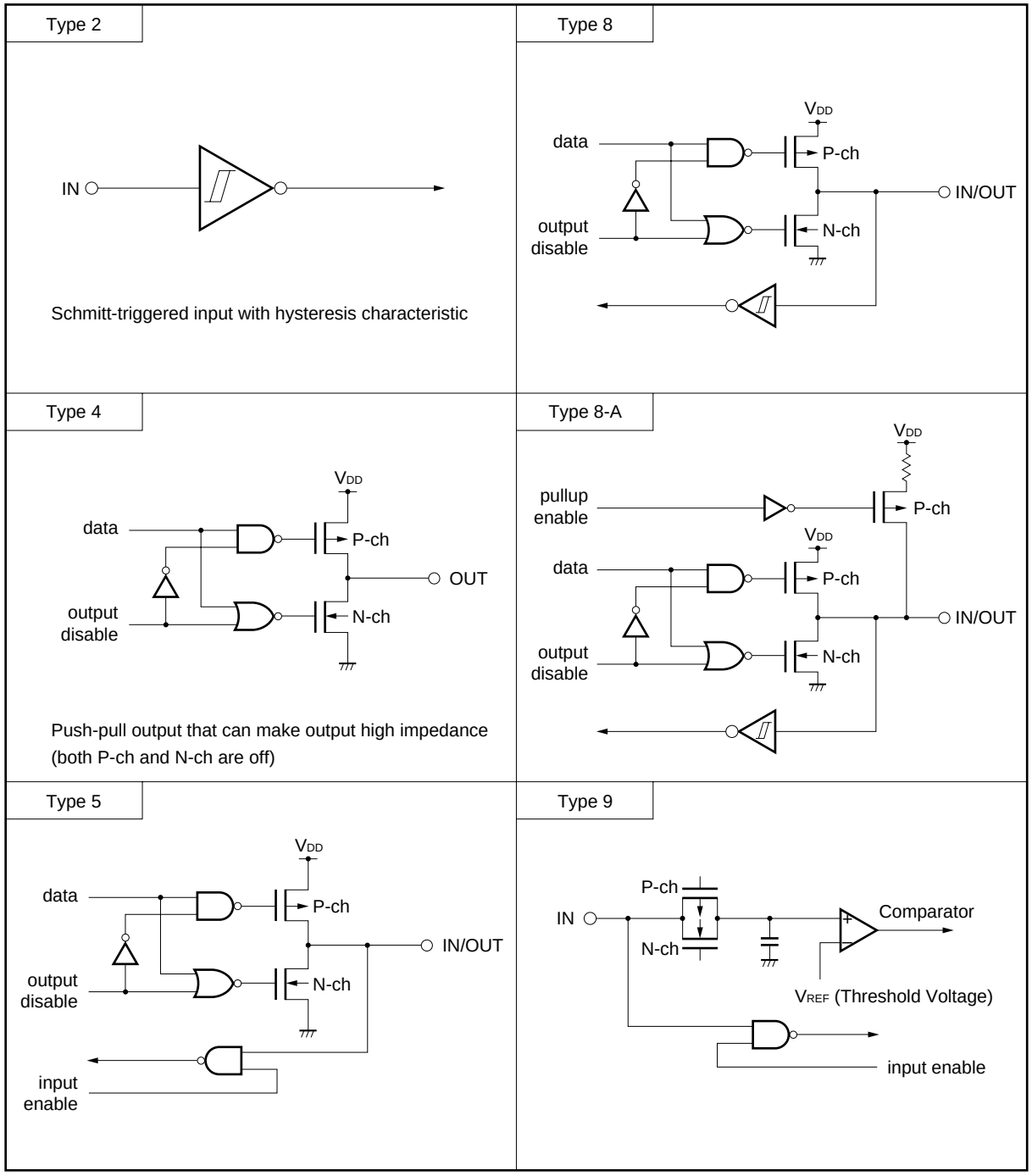
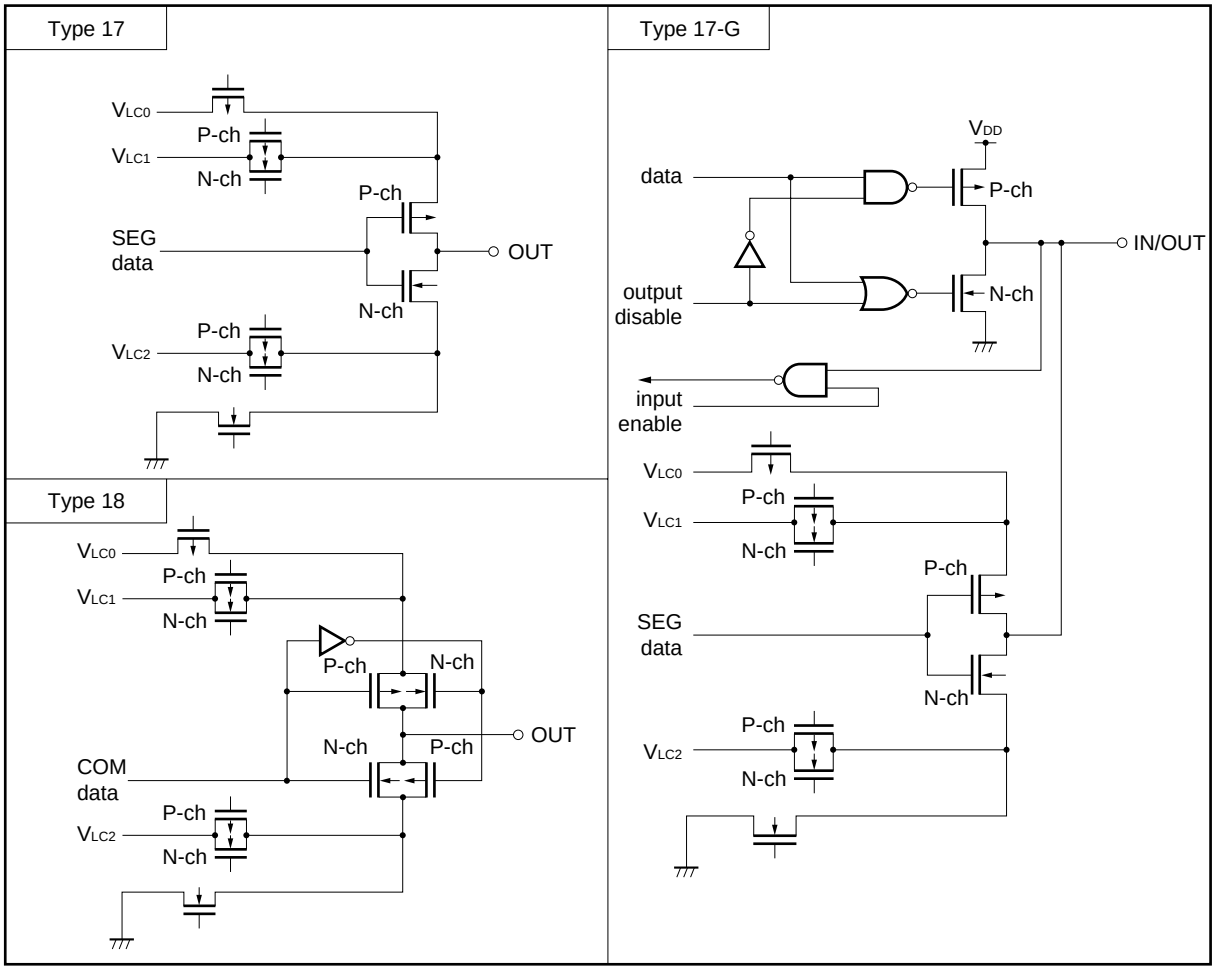


Figure 2-1. Pin Input/Output Circuits (2/2)

★



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This register sets a part of internal memory unused by software. The memory mapping can be made the same as that of mask ROM version with different type of internal memory (ROM, RAM).

The IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IMS to CFH.

Figure 3-1. Format of Memory Size Switching Register

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Selection of Internal High-speed RAM Capacity
0	0	0	768 bytes
1	1	0	1024 bytes
Others			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	1	0	24 Kbytes
1	0	0	0	32 Kbytes
Others				Setting prohibited

Table 3-1 shows the IMS set value to make the memory mapping the same as that of mask ROM version.

Table 3-1. Set Value of Memory Size Switching Register

Target Mask ROM Version	IMS Set Value
μPD780973(A)	06H

4. FLASH MEMORY PROGRAMMING

Writing to a flash memory can be performed without removing the memory from the target system. Writing is performed connecting the dedicated flash programmer (Flashpro III (part number: FL-PR3, PG-FP3)) to the host machine and the target system. Moreover, writing to flash memory can also be performed using a flash memory writing adapter connected to Flashpro III.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.
Inquiry: Naito Densei Machida Mfg. Co., Ltd. (TEL: 044-822-3813)

4.1 Selection of Transmission Method

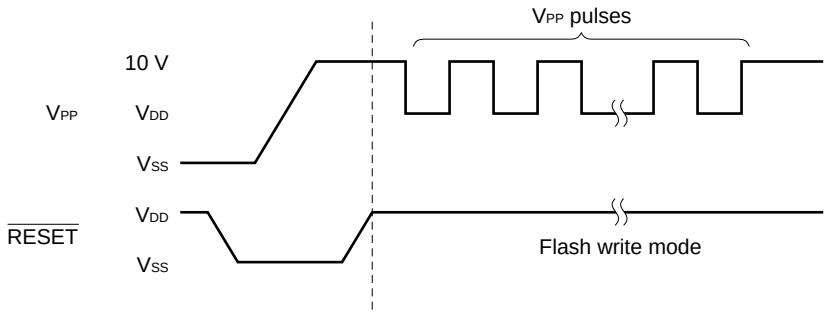
Writing to a flash memory is performed using the Flashpro III with a serial transmission mode. One of the transmission method is selected from those in Table 4-1. The selection of the transmission method is made by using the format shown in Figure 4-1. Each transmission method is selected by the number of V_{PP} pulses shown in Table 4-1.

Table 4-1. List of Transmission Method

Transmission Method	Channels	Pin	V_{PP} Pulses
3-wire serial I/O	1	SI/P52 SO/P51 $\overline{SCK}$/P50	0
UART	1	RxD/P53 TxD/P54	8
Pseudo 3-wire serial I/O	2	P05 (serial clock input) P06 (serial data output) P07 (serial data input)	12
		P95/S7 (serial clock input) P96/S6 (serial data output) P97/S5 (serial data input)	13

Caution Select a communication system always using the number of V_{PP} pulses shown in Table 4-1.

Figure 4-1. Format of Transmission Method Selection



4.2 Function of Flash Memory Programming

Operations such as writing to a flash memory are performed by various command/data transmission and reception operations according to the selected transmission method. Table 4-2 shows major functions of flash memory programming.

Table 4-2. Major Functions of Flash Memory Programming

Functions	Descriptions
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Delete time setting	Sets the memory delete time.
Baud rate setting	Sets the transmission rate in transmission using UART system.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

4.3 Connection of Flashpro III

The connection of the Flashpro III and the μPD78F0974 differs according to the transmission method (3-wire serial I/O, UART pseudo 3-wire serial I/O). The connection for each transmission method is shown in Figures 4-2 and 4-3, respectively.

Figure 4-2. Connection of Flashpro III for 3-wire Serial I/O System

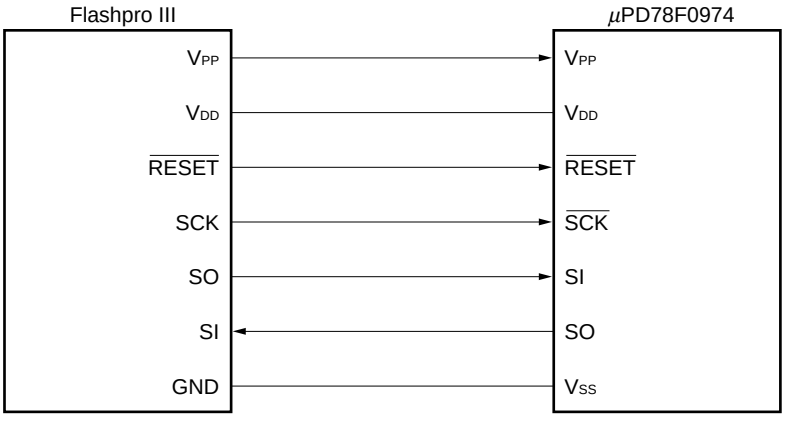


Figure 4-3. Connection of the Flashpro III for UART System

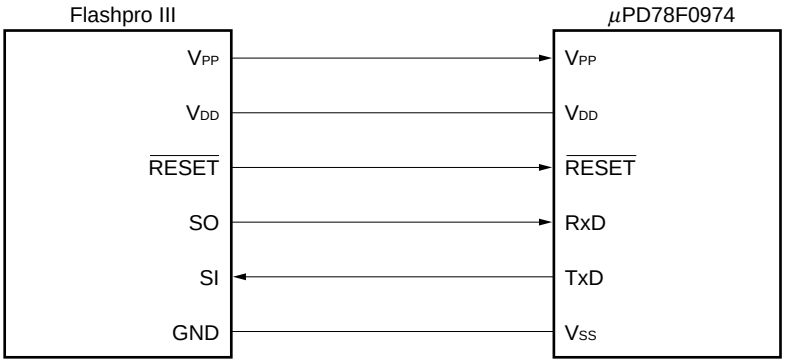
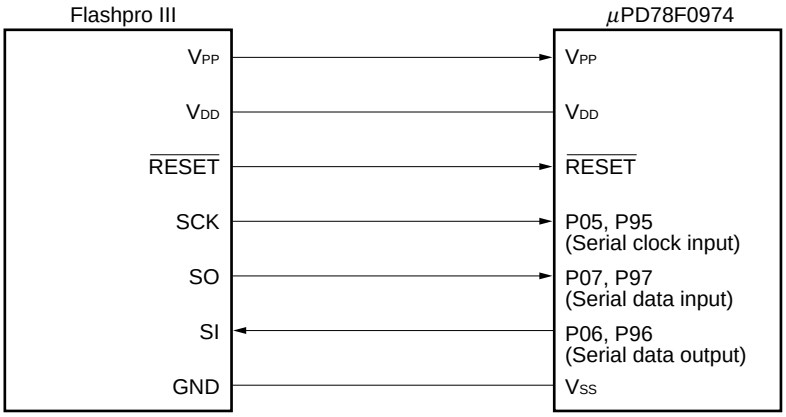


Figure 4-4. Connection of Flashpro III Using Pseudo 3-Wire Serial I/O Method



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +10.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
	SMV_{DD}	$SMV_{DD} = V_{DD}$		–0.3 to +6.5	V
	SMV_{SS}			–0.3 to +0.3	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_{O1}	P00-P07, P40-P44, P50-P54, P60, P61, P81-P87, P90-P97, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{O2}	P20-P27, P30-P37		–0.5 to SMV_{DD} + 0.7	V
Analog input voltage	V_{AN}	P10-P14	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current high	I_{OH}	1 pin (P00-P07, P40-P44, P50-P54, P60, P81-P87, P90-P97)		–10	mA
		P00-P07, P40-P44, P50-P54, P60, P81-P87, P90-P97 total		–15	mA
		P61		–30	mA
		1 pin (P20-P27)		–45	mA
		P20-P27 total		–135	mA
		1 pin (P30-P37)		–45	mA
		P30-P37 total		–135	mA
Output current low	I_{OL} Note	1 pin (P00-P07, P40-P44, P50-P54, P60, P81-P87, P90-P97)	Peak value	20	mA
			r.m.s.	10	mA
		P00-P07, P40-P44, P50-P54, P60, P81-P87, P90-P97 total	Peak value	50	mA
			r.m.s.	20	mA
		P61	r.m.s.	30	mA
		1 pin (P20-P27)		45	mA
		P20-P27 total		135	mA
		1 pin (P30-P37)		45	mA
		P30-P37 total		135	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The root mean square (r.m.s) should be calculated as follows: [r.m.s.] = [peak value] × $\sqrt{\text{duty}}$

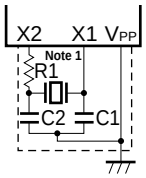
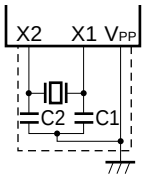
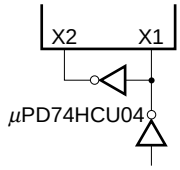
Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, device reliability may be impaired. The absolute maximum ratings are values that may physically damage the product. Be sure to use the product within the ratings.

Remark The characteristics of an alternate-function pin and a port pin are the same unless otherwise specified.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}					15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V.	P00-P07, P40-P44, P50-P54, P60, P81-P87, P90-P97			15	pF
	C_{SM}		P20-P27, P30-P37, P61			30	pF

★ **Main System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)**

Resonator	Recommended Circuit	Parameter	Test Conditions		MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 2	V_{DD} = Oscillation voltage range	OSCM = 00H	4.0		8.38	MHz
				OSCM = 80H	4.0		4.19	MHz
		Oscillation stabilization timeNote 3	After V_{DD} reaches oscillation voltage range MIN.				4	ms
Crystal resonator		Oscillation frequency (f_X)Note 2	V_{DD} = Oscillation voltage range	OSCM = 00H	4.0		8.38	MHz
				OSCM = 80H	4.0		4.19	MHz
		Oscillation stabilization timeNote 3	After V_{DD} reaches oscillation voltage range MIN.				10	ms
External clock		X1 input frequency (f_X)Note 2		OSCM = 00H	4.0		8.38	MHz
				OSCM = 80H	4.0		4.19	MHz
		X1 input high-/low-level width (tXH, tXL)			55		125	ns

Notes 1. Limit resistor R1 may be required depending on the resonator used.

2. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

3. Time required to stabilize oscillation after reset or STOP mode release.

Caution Wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = SMV_{DD} = 4.5 to 5.5 V)

	Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
	Input voltage high	V_{IH1}	P10-P14, P51, P54, P60, P61, P81-P87, P90-P97		0.7 V_{DD}		V_{DD}	V
		V_{IH2}	P00-P07, P40-P44, P50, P52, P53		0.7 V_{DD}		V_{DD}	V
★		V_{IH3}	$\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
		V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	Input voltage low	V_{IL1}	P10-P14, P51, P54, P60, P61, P81-P87, P90-P97		0		0.3 V_{DD}	V
		V_{IL2}	P00-P07, P40-P44, P50, P52, P53		0		0.3 V_{DD}	V
★		V_{IL3}	$\overline{RESET}$		0		0.2 V_{DD}	V
		V_{IL4}	X1, X2		0		0.4	V
	Output voltage high	V_{OH1}	P00-P07, P40-P44, P50-P54, P60, P81-P87, P90-P97	I_{OH} = –1mA	V_{DD} – 1.0		V_{DD}	V
		V_{OH2}	P20-P27, P30-P37	I_{OH} = –27 mA (T_A = 85 °C)	V_{DD} – 0.5		V_{DD} – 0.07	V
				I_{OH} = –30 mA (T_A = 25 °C)	V_{DD} – 0.5		V_{DD} – 0.07	V
				I_{OH} = –40 mA (T_A = –40 °C)	V_{DD} – 0.5		V_{DD} – 0.07	V
		V_{OH3}	P61	I_{OH} = –20 mA	V_{DD} – 0.5			V
	Output voltage low	V_{OL1}	P00-P07, P40-P44, P50-P54, P60, P81-P87, P90-P97	I_{OL} = 1.6 mA			0.4	V
		V_{OL2}	P20-P27, P30-P37	I_{OL} = 27 mA (T_A = 85 °C)	0.07		0.5	V
				I_{OL} = 30 mA (T_A = 25 °C)	0.07		0.5	V
				I_{OL} = 40 mA (T_A = –40 °C)	0.07		0.5	V
		V_{OL3}	P61	I_{OL} = 20 mA			0.5	V
	Input leakage current high	I_{LIH1}	P00-P07, P10-P14, P40-P44, P50-P54, P60, P61, P81-P87, P90-P97	V_{IN} = V_{DD}			3	μA
		I_{LIH2}	X1, X2	V_{IN} = V_{DD}			20	μA
	Input leakage current low	I_{LIL1}	P00-P07, P10-P14, P40-P44, P50-P54, P60, P61, P81-P87, P90-P97	V_{IN} = 0 V			–3	μA
		I_{LIL2}	X1, X2	V_{IN} = 0 V			–20	μA
	Output leakage current high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
	Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
	Software pull-up resistor	R	V_{IN} = 0 V, P00-P07		10	30	100	kΩ

Remark The characteristics of an alternate-function pin and a port pin are the same unless otherwise specified.

★ **DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	8.38-MHz crystal oscillation operation mode[Note 2]		12	36	mA
		4.19-MHz crystal oscillation operation mode[Note 2, 3]		6	18	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode[Note 2]		1.0	2.0	mA
		4.19-MHz crystal oscillation HALT mode[Note 3]		0.7	1.2	mA
	I_{DD3}	STOP mode		1.0	30	μA

Notes 1. This current means the current consumed by the CPU and peripheral functions (internal circuits), oscillator, and V_{DD} pin. However, this does not include the current that flows in the series resistor string of the A/D converter, internal pull-up resistor, LCD dividing resistor, sound generator (SGO, SGOF, P61), meter controller/driver (SM11/P20-SM14/P23, SM21/P24-SM24/P27, SM31/P30-SM34/P33, SM41/P34-SM44/P37), and EEPROM (at read).

2. When operating in high-speed mode (when the processor clock control register (PCC) is set to 00H).

3. When the oscillation mode register (OSCM) is set to 80H.

Remark The characteristics of an alternate-function pin and a port pin are the same unless otherwise specified.

LCD Controller/Driver Characteristics (T_A = –40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

1/3 Bias Method

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 2/3 V_{LCD2} = V_{LCD} × 1/3	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V
LCD split resistor current	I_{LCD}	3.0 V ≤ V_{LCD} ≤ V_{DD}		50		260	μA

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n=0, 1, 2).

The μPD78F0974 does not have a pin to apply a reference voltage (V_{LCD1} and V_{LCD2}). Therefore, the voltage deviation indicates the difference between the segment or common output values generated by the internal dividing resistor and the ideal reference voltage (V_{DD} to 1/3 V_{DD}).

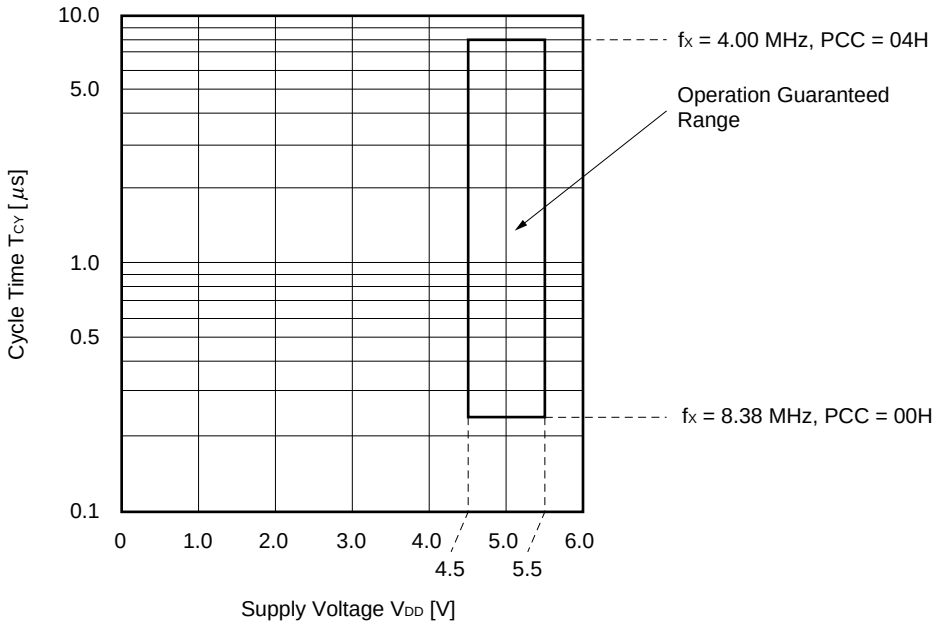
AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

(1) Basic Operation (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle Time (Min. instruction execution time)	T_{CY}	Operation on main system clock	0.238		8	μs
TI input high-/low-level width	t_{TIH0}, t_{TIL0}		3/f_{SAM} Note			μs
TI input frequency	f_{TI}		0		4	MHz
TIO2, TIO3 input high-/low-level width	t_{TIH}, t_{TIL}		100			ns
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

Note In combination with bits 0 (PRM00) and 1 (PRM01) of prescaler mode register (PRM0), selection of f_{SAM} is possible between f_X/8, f_X/16, f_X/32, and f_X/64.

T_{CY} vs. V_{DD} (At main system clock operation)



(2) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5V)

(a) 3-wire serial I/O mode ($\overline{SCK}$ ... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}		950			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2–50			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}		100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}		400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of $\overline{SCK}$ and SO output lines.

(b) 3-wire serial I/O mode ($\overline{SCK}$ ... External clock input)

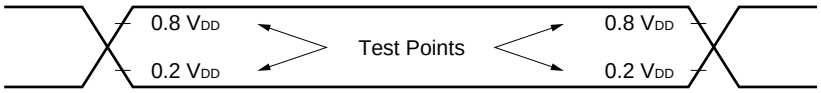
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}		100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}		400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK}$ rise, fall time	t_{R2}, t_{F2}				160	ns

Note C is the load capacitance of SO output line.

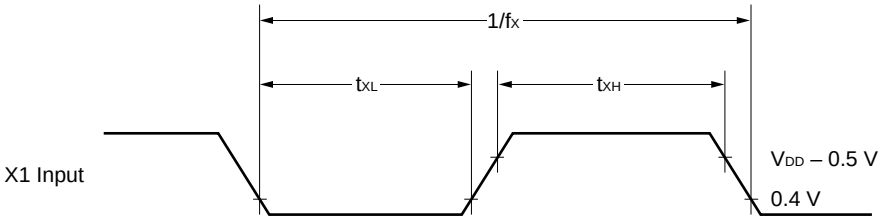
(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					130.9	kbps

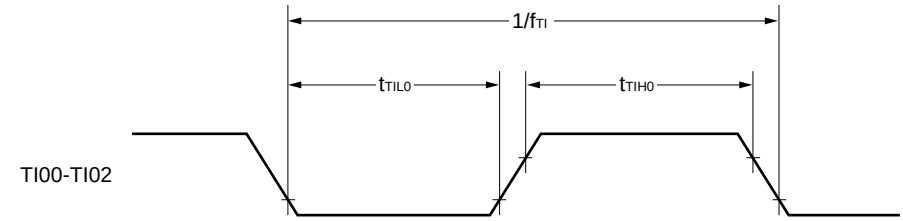
AC Timing Test Point (Excluding X1 Input)

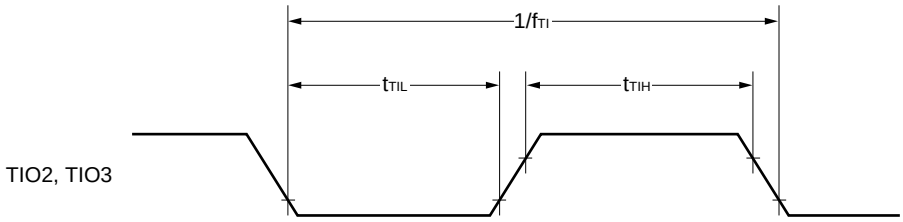


Clock Timing



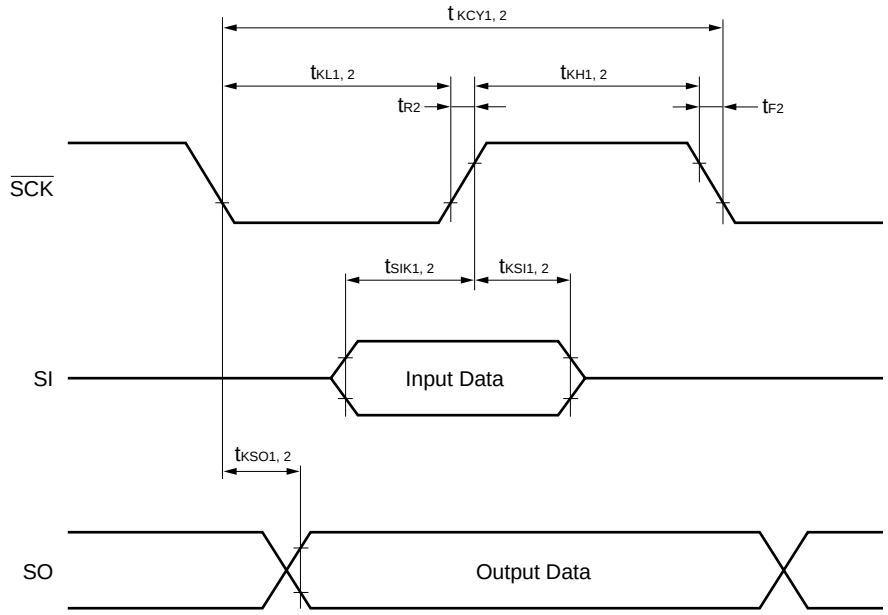
TI Timing





Serial Transfer Timing

3-wire serial I/O mode:



★ **Sound Generator Characteristics (T_A = –40 to +85 °C, V_{DD} = SMV_{DD} = 4.5 to 5.5 V)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Sound generator input frequency	f_{SG1}				4.19	MHz

★ **Meter Controller/Driver Characteristics (T_A = –40 to +85 °C, V_{DD} = SMV_{DD} = 4.5 to 5.5 V)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Meter controller/driver input frequency	f_{MC} Note 1				4.19	MHz
Symmetry performance Note 2	ΔHSPmn	I_{OH} = –30 mA ΔHSPmn = | V_{OH} (SMmn) max – V_{OH} (SMmn) min |			50	mV
	ΔLSPmn	I_{OL} = 30 mA ΔLSPmn = | V_{OL} (SMmn) max – V_{OL} (SMmn) min |			50	mV

Notes 1. Source clock of the free-running counter.

2. Indicates variation of 16 PWM output voltages.

Remark m = 1 to 4, n = 1 to 4

A/D Converter Characteristics (T_A = –40 to +85 °C, AV_{REF} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} =0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error[Note]					±0.6	%
★ Conversion time	t_{CONV}		14.0			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF} + 0.3	V
AV_{REF}–AV_{SS} resistance	R_{AIREF}	When bit 7 (ADCS1) of the A/D converter mode register (ADM1) is set to 0.		21.4		kΩ

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

EEPROM Characteristics (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

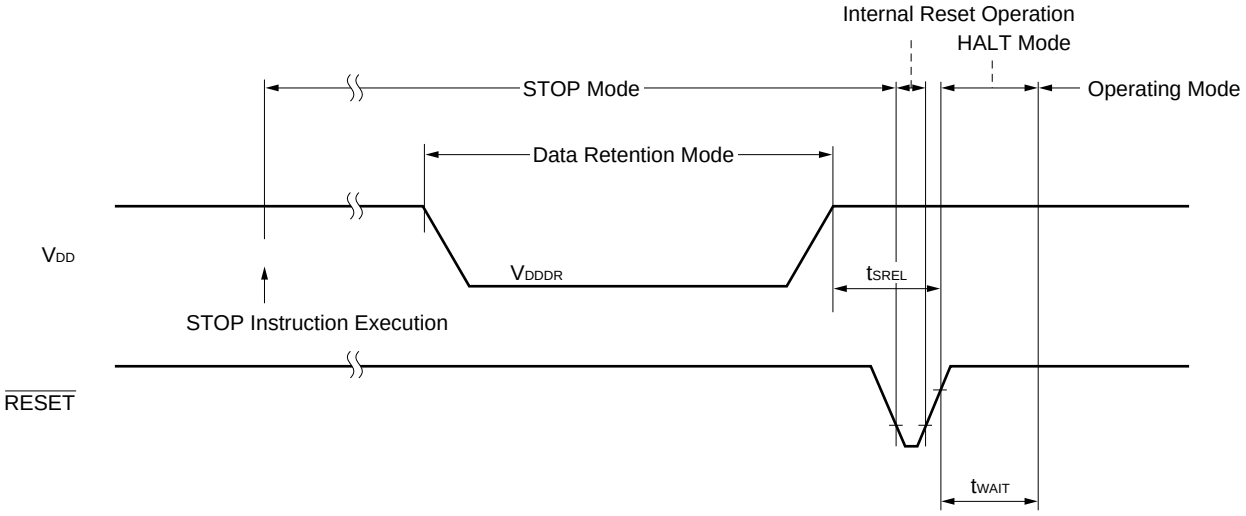
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
EEPROM write time	t_{EEWR}		T.B.D			ms

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

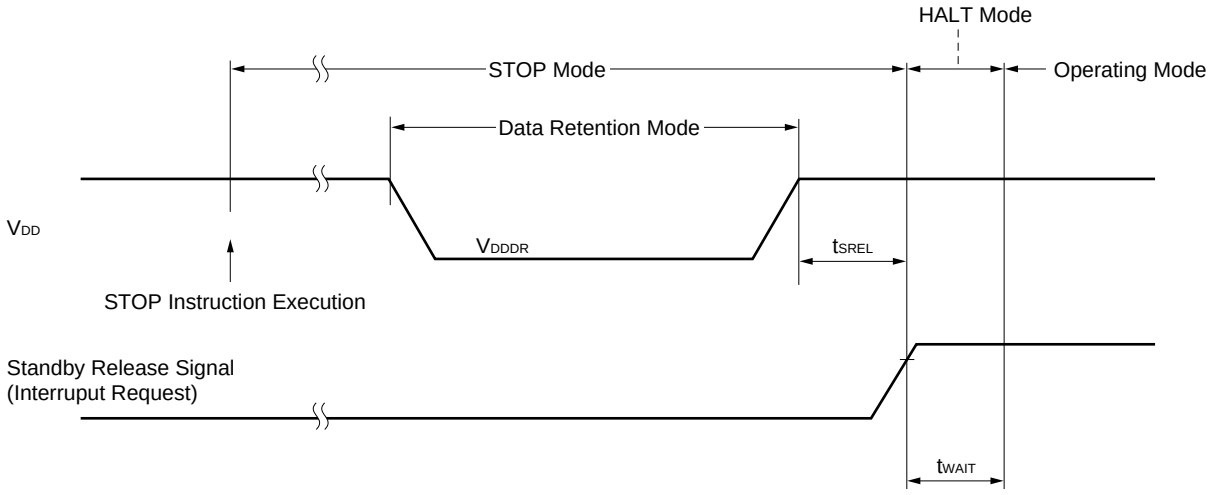
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current disconnected	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible.

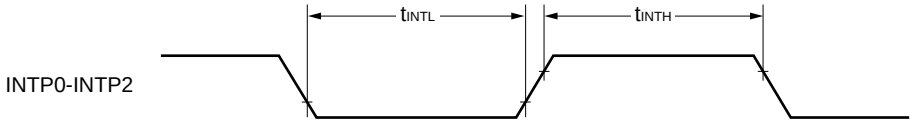
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



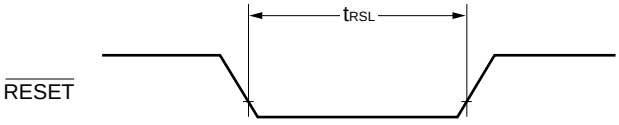
Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Flash Memory Programming Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.5 to 10.5 V)

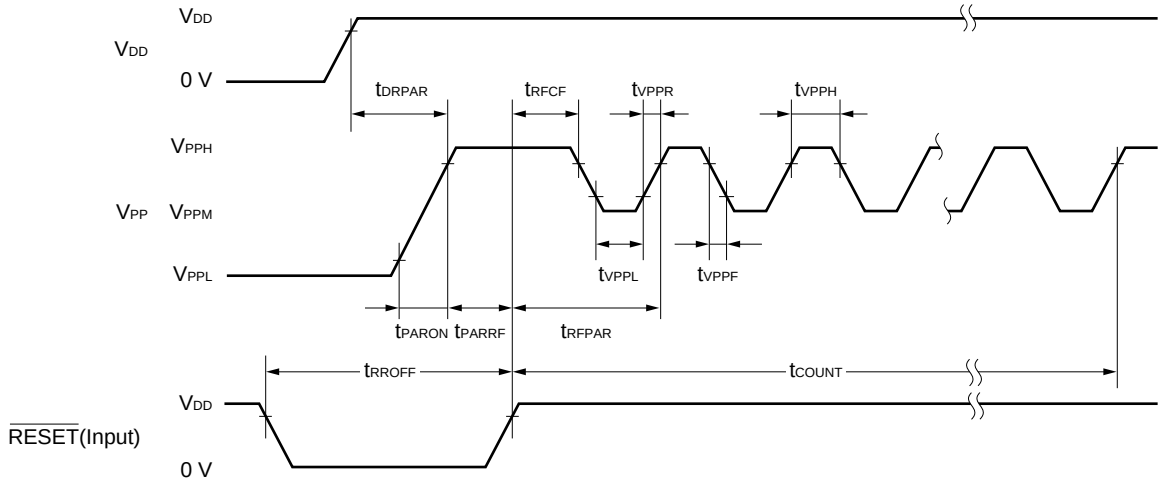
(1) Basic Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	f_X		4		8.38	MHz
Supply voltage	V_{DD}		4.5		5.5	V
	V_{PPL}	When detecting V_{PP} low level	–0.3		0.2 V_{DD}	V
	V_{PPM}	When detecting V_{PP} V_{DD} level	0.8 V_{DD}	V_{DD}	1.2 V_{DD}	V
	V_{PPH}	When detecting V_{PP} high voltage	9.5	10.0	10.5	V
V_{DD} supply current	I_{DD}				50	mA
V_{PP} supply current	I_{PP}				50	mA
Write time (per word)	T_{WRT}			50		μs
Write frequency	C_{WRT}				100	time
Erase time	T_{ERASE}				2	s

(2) Serial Write Operation Characteristics

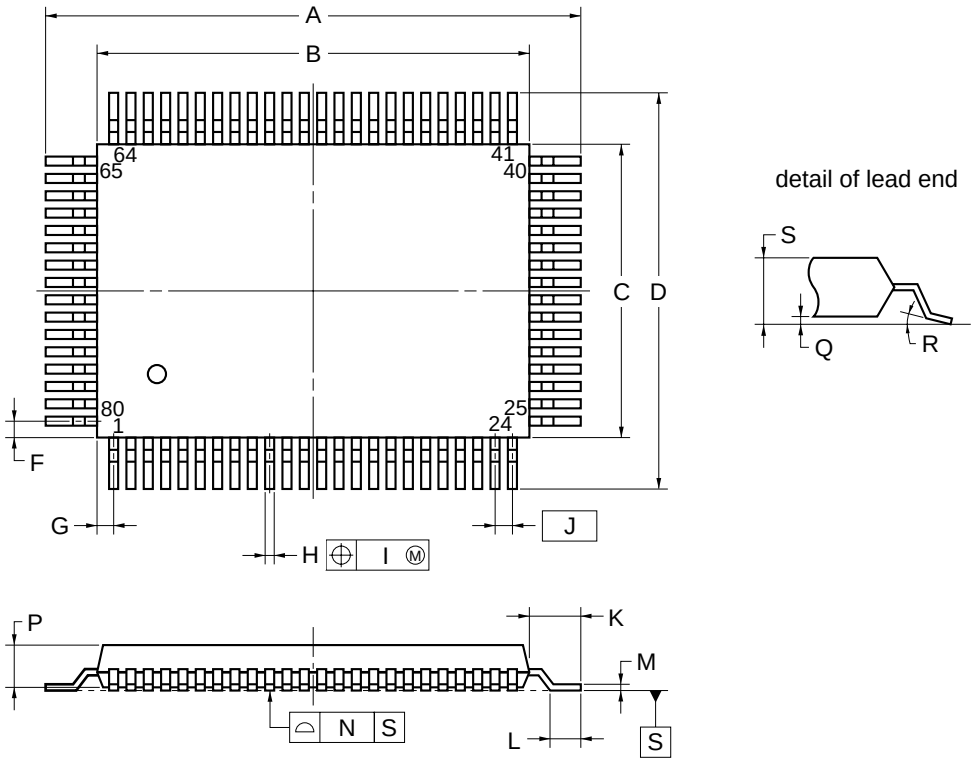
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PARON}	V_{PP} high voltage supply	1.0			μs
$\overline{RESET}$ retention time	t_{RROFF}		1.0			μs
V_{PP}↑ set time from V_{DD}↑	t_{DRPAR}	V_{PP} high voltage supply	1.0			μs
$\overline{RESET}$↑ set time from V_{PP}↑	t_{PARRF}	V_{PP} high voltage supply	1.0			μs
V_{PP}↑ set time from $\overline{RESET}$↑	t_{RFPAR}	V_{PP} high voltage supply	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{VPPH}		1.0			μs
V_{PP} counter low-level width	t_{VPPL}		1.0			μs
V_{PP} counter rise, fall time	t_{VPPR}, t_{VPPF}				1.0	μs

Flash Memory Write Mode Setting Timing



6. PACKAGE DRAWING

80 PIN PLASTIC QFP (14x20)



NOTE

1. Controlling dimension —— millimeter.

2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P80GF-80-3B9-4

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78F0974.
Also refer to **(5) Notes on using development tools**.

(1) Language Processing Software

RA78K/0	78K/0 series common assembler package
CC78K/0	78K/0 series common C compiler package
DF780974	Device file common to μPD780973 subseries
CC78K/0-L	78K/0 series common C compiler library source file

(2) Flash Memory Writing Tools

Flashpro III (Part number: FL-PR3, PG-FP3)	Dedicated flash programmer. FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

(3) Debugging Tools

- **When in-circuit emulator IE-78K0-NS is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-780973-NS-EM1[Note]	Emulation board to emulate μPD780973 subseries
IE-70000-98-IF-C	Interface adapter used when PC-9800 series (except notebook type) is used as host machine (C bus compatible)
IE-70000-CD-IF-A	PC card and interface cable used when notebook type PC is used as host machine (PCMCIA compatible)
IE-70000-PC-IF-C	Interface adapter used when IBM PC/AT™ compatible machine is used as host machine (ISA compatible)
IE-70000-PCI-IF	Interface adapter used when PC with a PCI bus as host machine.
NP-80GF	Emulation probe for 80-pin plastic QFP (GF-3B9 type)
TGF-080RAP (see **Figure A-1**)	Adapter to be mounted on a target system board made for 80-pin plastic QFP (GF-3B9 type)
SM78K0	78K/0 series common system simulator
ID78K0-NS	Integrated debugger for IE-78K0-NS
DF780974	μPD780974 subseries device file

Note Under development

(4) Real-Time OS

RX78K/0	78K/0 series real-time OS
MX78K0	78K/0 series OS

(5) Notes on using development tools

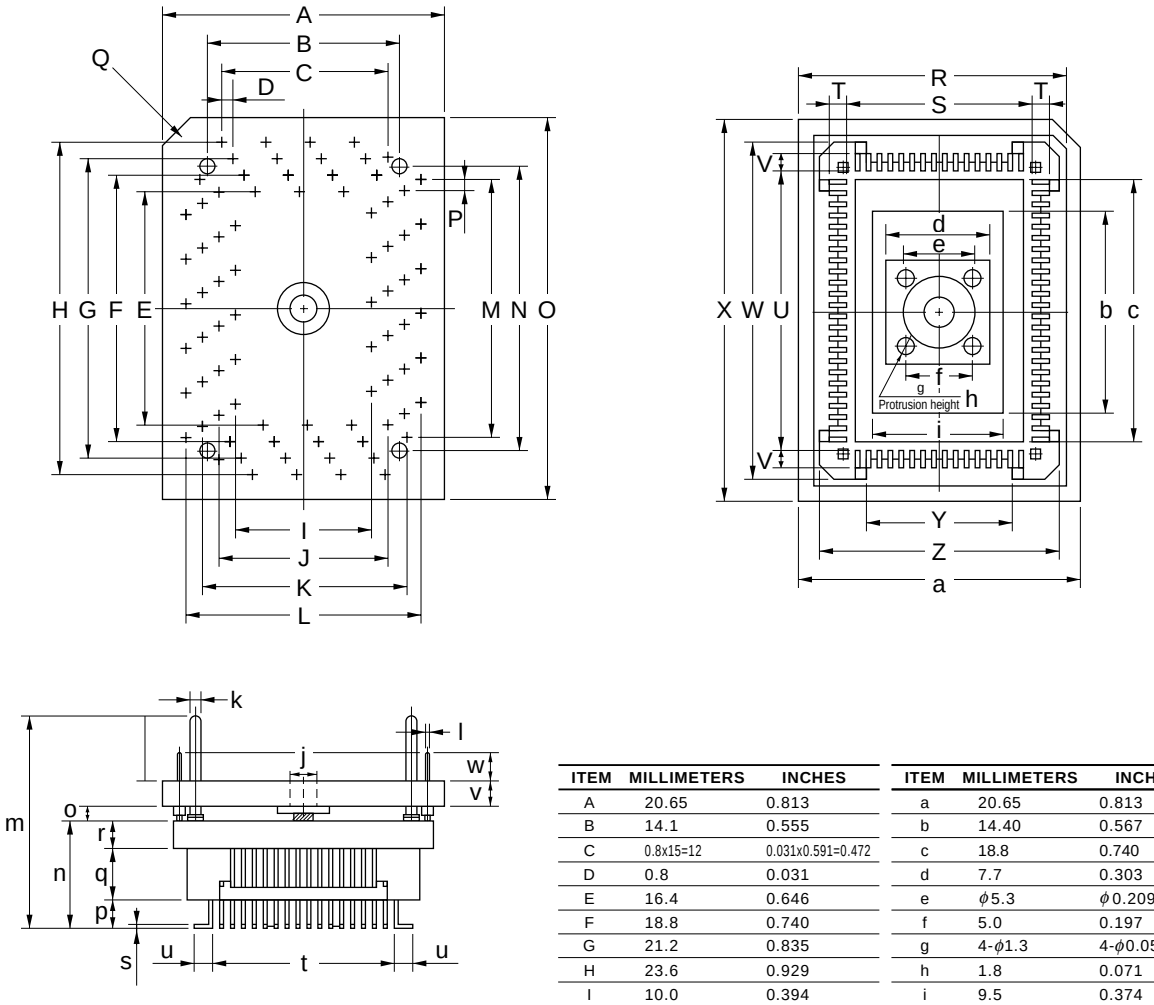
- Use ID78K0-NS and SM78K0 in combination with DF780974.
- Use CC78K/0 and RX78K/0 in combination with RA78K/0 and DF780974.
- TGF-080RAP is a product of Tokyo Eletech Corp.
  Reference: Daimaru Kogyo Ltd. Electronics Dept. (TEL: Tokyo 03-3820-7112)
  Electronics 2nd Dept. (TEL: Osaka 06-6244-6672)
- For development tools made by third parties, refer to **78K/0 Series Selection Guide (U11126E)**.
- The host machine corresponding to each software package is as follows:

Host Machine / [OS] / Software	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT Compatible Machines [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS (RISC)™ [NEWS-OS™]
RA78K/0	○Note	○
CC78K/0	○Note	○
ID78K0-NS	○	—
SM78K0	○	—
RX78K/0	○Note	○
MX78K0	○Note	○

Note This software is based on DOS.

Drawing for Conversion Adapter (TGF-080RAP)

Figure A-1. TGF-080RAP Drawing (for Reference Only)



ITEM	MILLIMETERS	INCHES
A	20.65	0.813
B	14.1	0.555
C	0.8x15=12	0.031x0.591=0.472
D	0.8	0.031
E	16.4	0.646
F	18.8	0.740
G	21.2	0.835
H	23.6	0.929
I	10.0	0.394
J	12.4	0.488
K	14.8	0.583
L	17.2	0.677
M	0.8x23=18.4	0.031x0.906=0.724
N	20.5	0.807
O	27.05	1.065
P	0.8	0.031
Q	C 2.0	C 0.079
R	18.65	0.734
S	13.35	0.526
T	1.325	0.052
U	19.75	0.778
V	1.125	0.044
W	23.55	0.927
X	27.05	1.065
Y	10.6	0.417
Z	17.1	0.673

ITEM	MILLIMETERS	INCHES
a	20.65	0.813
b	14.40	0.567
c	18.8	0.740
d	7.7	0.303
e	ϕ5.3	ϕ0.209
f	5.0	0.197
g	4-ϕ1.3	4-ϕ0.051
h	1.8	0.071
i	9.5	0.374
j	ϕ3.55	ϕ0.140
k	ϕ0.9	ϕ0.035
l	ϕ0.3	ϕ0.012
m	(16.95)	(0.667)
n	7.35	0.289
o	1.2	0.047
p	1.85	0.073
q	3.5	0.138
r	2.0	0.079
s	0.25	0.010
t	13.6	0.535
u	1.2	0.047
v	2.4	0.094
w	2.7	0.106

TGF-080RAP-G0E

note: Product by TOKYO ELETECH CORPORATION.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780973 Subseries User's Manual	U12406E	U12406J
μPD780973(A) Preliminary Product Information	U12759E	U12759J
μPD78F0974 Preliminary Product Information	This manual	U12646J
78K/0 Series User's Manual Instruction	U12326E	U12326J
78K/0 Series Instruction Table	–	U10903J
78K/0 Series Instruction Set	–	U10904J
μPD780973 Subseries Special Function Register Table	–	U12748J

Development Tools Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	U13034E	U13034J
IE-78K0-NS		Planned	Planned
IE-780974-NS-EM1		Planned	Planned
SM78K0 System Simulator (Windows Based)	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS Based	Reference	–	U11151J
ID78K0 Integrated Debugger Windows Based	Guide	U11649E	U11649J
ID78K0 Integrated Debugger PC Based	Reference	U11539E	U11539J

Embedded Software Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real Time OS	Fundamentals	U11537E	U11537J
	Installation	U11536E	U11536J
OS for 78K/0 Series MX78K0	Fundamental	U12257E	U12257J

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grade on NEC Semiconductor Devices	C11531E	C11531J
Reliable Quality Maintenance on NEC Semiconductor Devices	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Review of Quality and Reliability Handbook	–	C12769J
Microcomputer Product Series Guide	–	U11416J

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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