

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F0964 is a member of the μPD780964 Subseries of the 78K/0 Series that substitute flash memory for the internal ROM of the μPD780964.

Since it is possible to perform program write operation while mounted on a board, it is suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

μPD780924, 780964 Subseries User's Manual	: In preparation
78K/0 Series User's Manual Instructions	: IEU-1372

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 32 Kbytes
- Internal high-speed RAM: 1024 bytes^{Note}
- Operable in the same supply voltage range as the mask ROM version (V_{DD} = 2.7 to 5.5 V)

Note The capacities of the flash memory and internal high-speed RAM can be changed with the internal memory size switching register (IMS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0964 AND MASK ROM VERSIONS.**

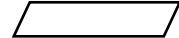
ORDERING INFORMATION


Part Number	Package
μPD78F0964CW	64-pin plastic shrink DIP (750 mil)
μPD78F0964GC-AB8	64-pin plastic QFP (14 x 14 mm)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

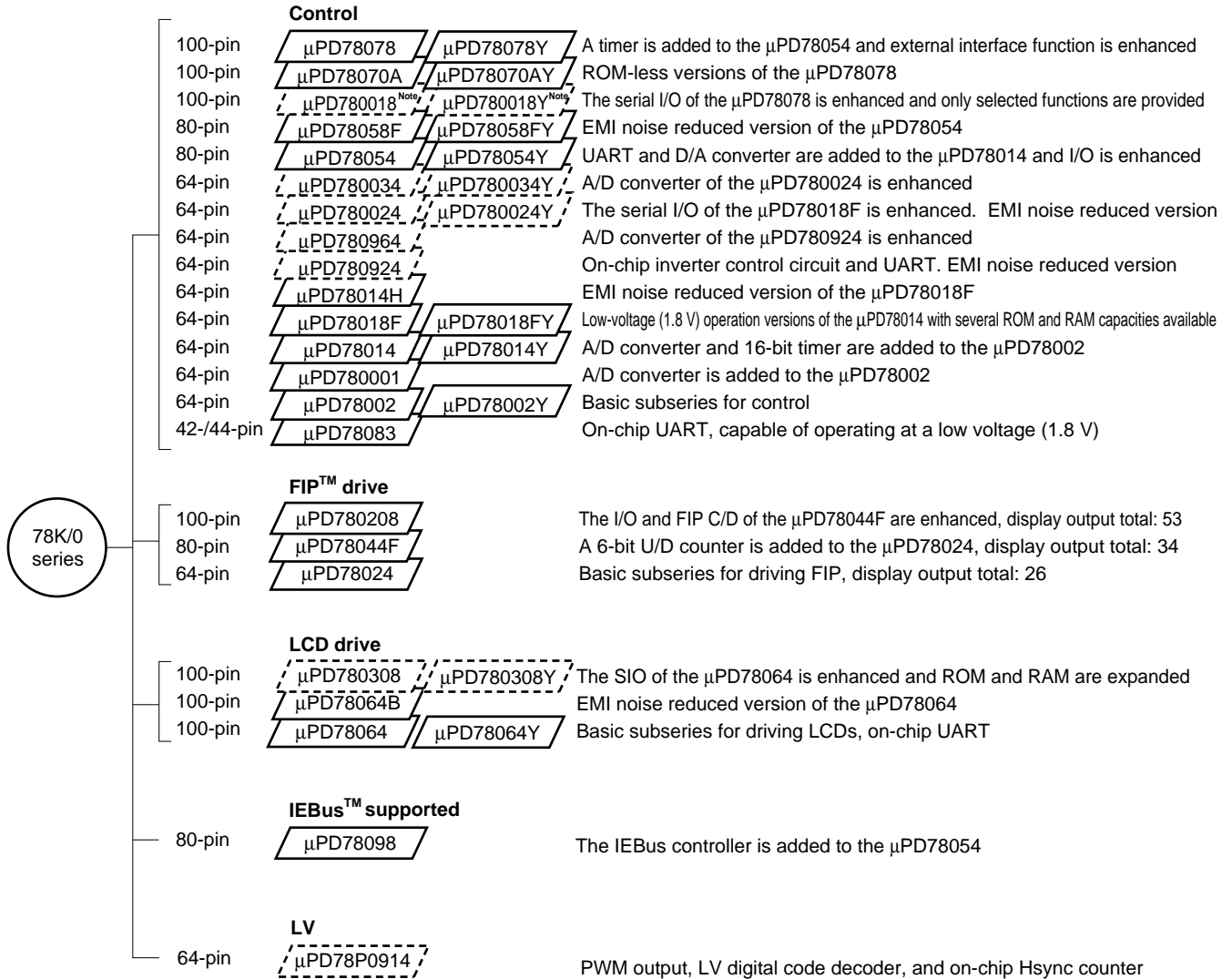
78K/0 SERIES DEVELOPMENT

The 78K/0 Series product line-up is shown below. Subseries names are shown inside frames.

 Products in mass production

 Products under development

Y subseries products are compatible with I²C bus.



Note Under planning

The table below shows the main differences between subseries.

Functions Subseries		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	VDD MIN. Value	External Expansion	
			8-bit	16-bit	Watch	WDT								
For control	μPD78078	32 K to 60 K	4ch	1ch	1ch	1ch	8ch	—	2ch	3ch (UART: 1ch)	88	1.8 V	Available	
	μPD78070A	—								61	2ch (Time division 3-wire : 1ch)			88
	μPD780018	48 K to 60 K	2ch	—	—	—	3ch (UART: 1ch)	69	2.0 V					
	μPD78058F													
	μPD78054	16 K to 60 K	8 K to 32 K	—	8ch	—	3ch (Time division UART : 1ch)	51	1.8 V					
	μPD780034	8 K to 32 K								—	8ch	2ch (UART : 2ch)		47
	μPD780024	8 K to 32 K		3ch	Note	—	8ch	—	8ch	—				
	μPD780964	8 K to 32 K									2ch	1ch		1ch
	μPD780924	8 K to 32 K		8 K to 60 K	—	—	—	—	2.7 V					
	μPD78014H	8 K to 60 K								8 K to 32 K	—	—		—
	μPD78018F	8 K to 60 K		8 K to 32 K	—	—	—	—	53					
	μPD78014	8 K to 32 K								8 K	—	—		—
	μPD780001	8 K		8 K to 16 K	—	—	1ch	—	—					
	μPD78002	8 K to 16 K								8 K	—	—		1ch
μPD78083	8 K	2ch	1ch	1ch	1ch	8ch	—	—	2ch				74	
μPD780208	32 K to 60 K									16 K to 40 K	24 K to 32 K	2ch		1ch
μPD78044F	16 K to 40 K	2ch	1ch	1ch	1ch	8ch	—	—	3ch (Time division UART: 1ch)				57	
μPD78024	24 K to 32 K									2ch	1ch	1ch		1ch
μPD780308	48 K to 60 K	32 K	2ch	1ch	1ch	1ch	8ch	—	—				3ch (Time division UART: 1ch)	
μPD78064B	32 K									16 K to 32 K	2ch	1ch		1ch
μPD78064	16 K to 32 K													
IEBus support	μPD78098	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	—	2ch	3ch (UART: 1ch)	69	2.7 V	Available	
For LV	μPD78P0914	32 K	6ch	—	—	1ch	8ch	—	—	2ch	54	4.5 V	Available	

Note 10-bit timer: one channel

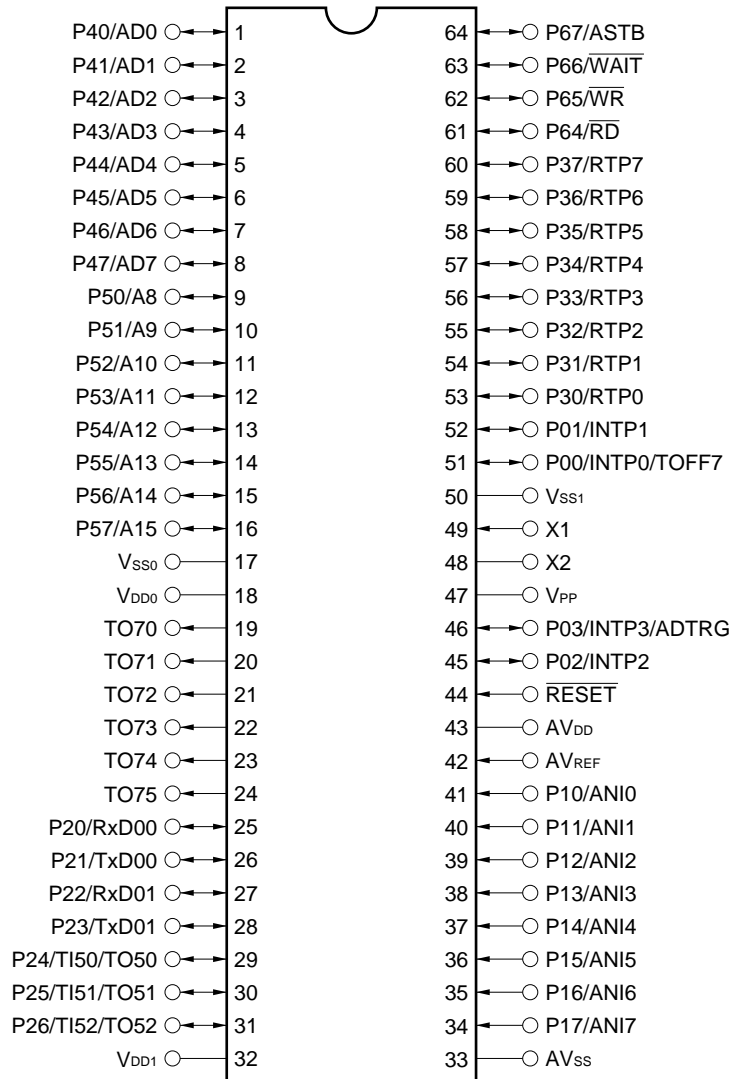
FUNCTION OVERVIEW

Item		Functions
Internal memory	Flash memory	32 Kbytes ^{Note}
	High-speed RAM	1024 bytes ^{Note}
Memory space		64 Kbytes
General-purpose register		8 bits x 32 registers (8 bits x 8 registers x 4 banks)
Instruction cycle		On-chip instruction execution time variable function 0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38-MHz operation with system clock)
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total : 47 • CMOS inputs : 8 • CMOS I/Os : 39
Real-time output ports		10 bits x 1 or 4 bits x 2
A/D converter		<ul style="list-style-type: none"> • 8-bit resolution x 8 channels • Power supply voltage: AV_{DD} = 2.7 to 5.5 V
Serial interface		UART x 2 channels
Timer		<ul style="list-style-type: none"> • 8-bit timer/event counter : 3 channels • 10-bit timer : 1 channel • Watchdog timer : 1 channel
Timer output		9 (8-bit PWM output x 3 and inverter control output x 6)
Vectored interrupt	Maskable	Internal: 12, external: 4
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V _{DD} = 2.7 to 5.5 V
Operating ambient temperature		T _A = -40 to +85 °C
Package		<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 x 14 mm)

Note The capacities of the flash memory and internal high-speed RAM can be changed with the internal memory size switching register (IMS).

PIN CONFIGURATION (Top View)

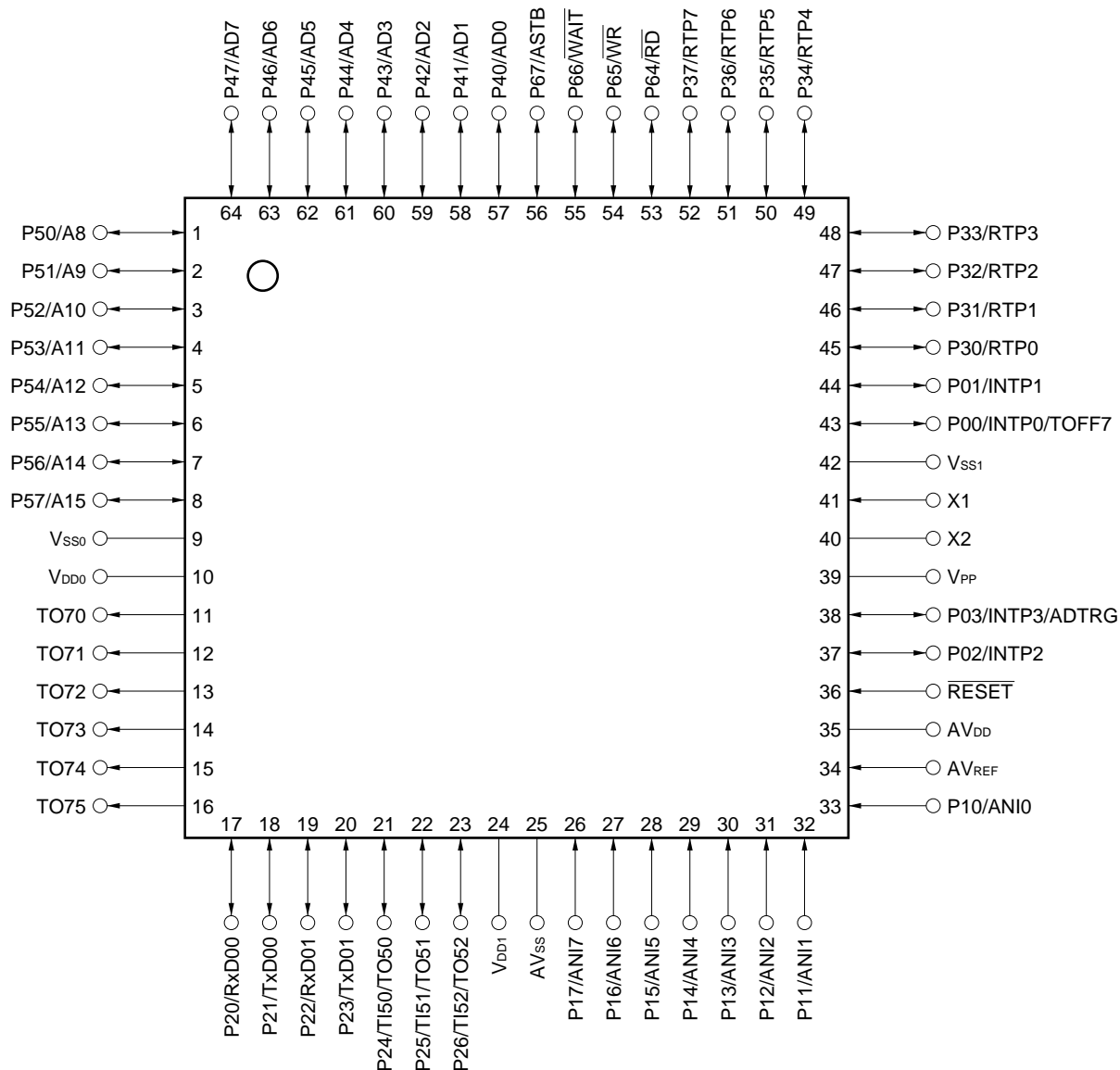
- 64-Pin Plastic Shrink DIP (750 mil)
μPD78F0964CW



- Cautions**
1. In the normal operation mode, connect the V $_{PP}$ pin to V $_{SS0}$ directly.
 2. Connect the AV $_{DD}$ pin to V $_{DD0}$.
 3. Connect the AV $_{SS}$ pin to V $_{SS0}$.

Remark When the μPD78F0964 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V $_{DD0}$ and V $_{SS1}$ individually and connecting V $_{SS0}$ and V $_{SS1}$ to different ground lines, is recommended.

• 64-Pin Plastic QFP (14 x 14 mm)
μPD78F0964GC-AB8

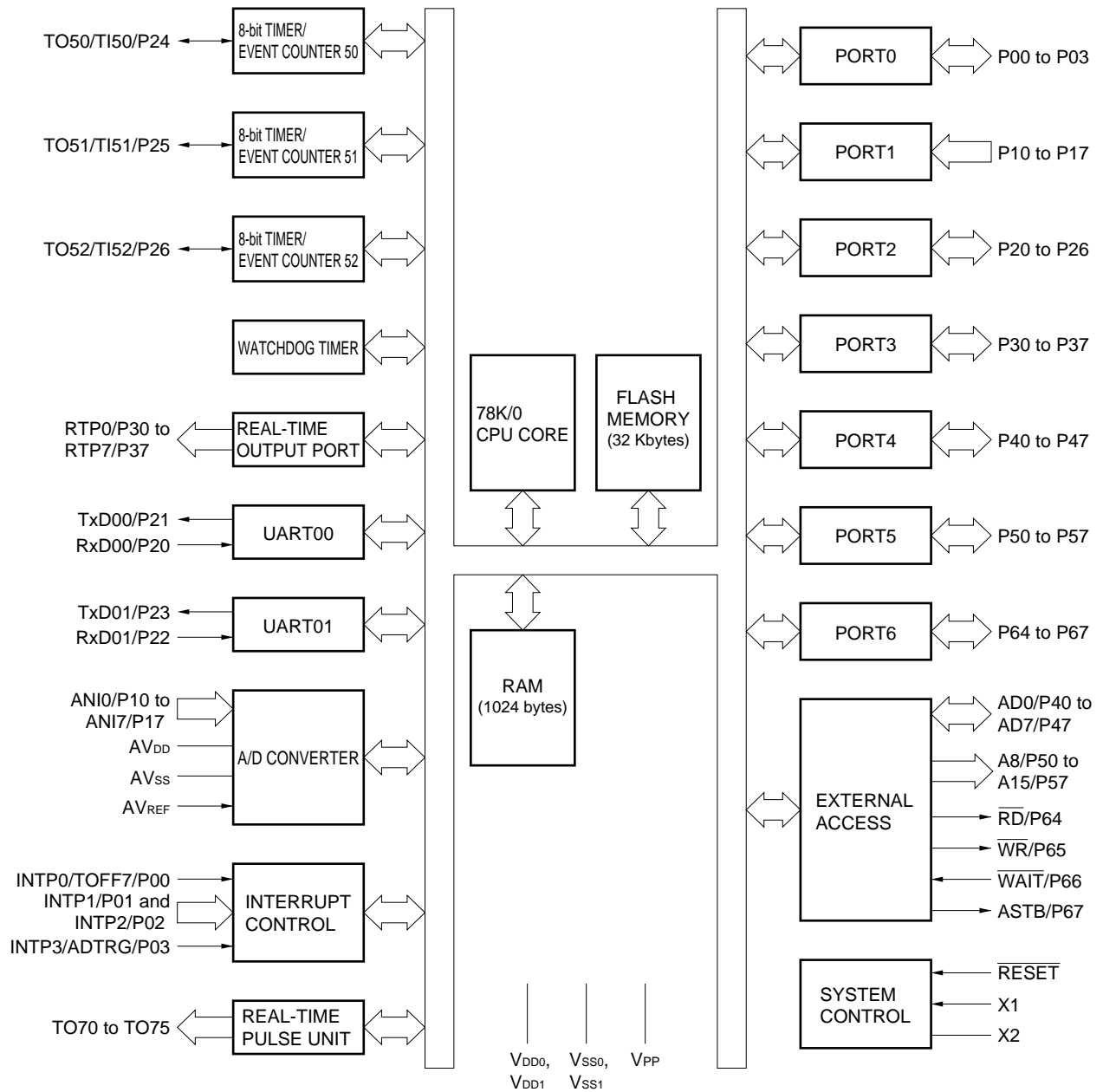


- Cautions**
1. In the normal operation mode, connect the V_{PP} pin to V_{SS0} directly.
 2. Connect the AV_{DD} pin to V_{DD0}.
 3. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD78F0964 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{SS1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15	: Address Bus	\overline{RD}	: Read Strobe
AD0 to AD7	: Address/Data Bus	RESET	: Reset
ADTRG	: AD Trigger Input	RTP0 to RTP7	: Real-time Port
ANI0 to ANI7	: Analog Input	RxD00, RxD01	: Receive Data
ASTB	: Address Strobe	TI50 to TI52	: Timer Input
AVDD	: Analog Power Supply	TO50 to TO52,	
AVREF	: Analog Reference Voltage	TO70 to TO75	: Timer Output
AVSS	: Analog Ground	TOFF7	: Timer Output Off
INTP0 to INTP3	: Interrupt From Peripherals	TxD00, TxD01	: Transmit Data
P00 to P03	: Port 0	VDD0, VDD1	: Power Supply
P10 to P17	: Port 1	VPP	: Programming Power Supply
P20 to P26	: Port 2	VSS0, VSS1	: Ground
P30 to P37	: Port 3	\overline{WAIT}	: Wait
P40 to P47	: Port 4	WR	: Write Strobe
P50 to P57	: Port 5	X1, X2	: Crystal
P64 to P67	: Port 6		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78F0964 AND MASK ROM VERSIONS	11
2. PIN FUNCTION LIST	12
2.1 Port Pins	12
2.2 Non-Port Pins	13
2.3 Recommended Connection of Unused Pins	14
3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)	15
4. FLASH MEMORY PROGRAMMING	16
4.1 Selection of Transmission Method	16
4.2 Functions of Flash Memory Programming	17
4.3 Connection of Flashpro	17
5. PACKAGE DRAWINGS	18
APPENDIX A. DEVELOPMENT TOOLS	20
APPENDIX B. RELATED DOCUMENTS	22

[MEMO]

1. DIFFERENCES BETWEEN μPD78F0964 AND MASK ROM VERSIONS

The μPD78F0964 is a product with a flash memory which enables on-board reading, erasing and rewriting of programs.

Except for flash memory specifications, the same functions as those of mask ROM versions can be obtained by setting the internal memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory version (μPD78F0964) and mask ROM versions (μPD780961, 780962, 780963, 780964).

Table 1-1. Differences between μPD78F0964 and Mask ROM Versions

Item	μPD78F0964	Mask ROM Versions
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacities	32 Kbytes	μPD780961: 8 Kbytes μPD780962: 16 Kbytes μPD780963: 24 Kbytes μPD780964: 32 Kbytes
Internal high-speed RAM capacities	1024 bytes	μPD780921: 512 bytes μPD780922: 512 bytes μPD780923: 1024 bytes μPD780924: 1024 bytes
Internal ROM and internal high-speed RAM capacities variable/not variable with internal memory size switching register.	Variable ^{Note}	Not variable
TEST pin	Not provided	Provided
Vpp pin	Provided	Not provided
Electrical specifications	Refer to the data sheet of individual products.	

Note Flash memory is set to 32 Kbytes and internal high-speed RAM is set to 1024 bytes by $\overline{\text{RESET}}$ input.

2. PIN FUNCTION LIST

2.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	INTP0/TOFF7
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1. 8-bit input only port.	Input	ANI0 to ANI7
P20	I/O	Port 2. 7-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	RxD00
P21				TxD00
P22				RxD01
P23				TxD01
P24				TI50/TO50
P25				TI51/TO51
P26				TI52/TO52
P30 to P37	I/O	Port 3. 8-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	AD0 to AD7
P50 to P57	I/O	Port 5. 8-bit I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	A8 to A15
P64	I/O	Port 6. 4-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	\overline{RD}
P65				\overline{WR}
P66				\overline{WAIT}
P67				ASTB

2.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input that can specify the effective edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TOFF7
INTP1			Input	P01
INTP2			Input	P02
INTP3			Input	P03/ADTRG
TI50	Input	External count clock input to timer (TM50).	Input	P24/TO50
TI51		External count clock input to timer (TM51).	Input	P25/TO51
TI52		External count clock input to timer (TM52).	Input	P26/TO52
TO50	Output	Timer (TM50) output.	Input	P24/TI50
TO51		Timer (TM51) output.	Input	P25/TI51
TO52		Timer (TM52) output.	Input	P26/TI52
RTP0 to RTP7	Output	Real-time output port that outputs pulses in synchronization with trigger signals outputs from the real-time pulse unit.	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output.	Input	P21
TxD01			Input	P23
RxD00	Input	Asynchronous serial interface serial data input.	Input	P20
RxD01			Input	P22
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	External trigger signal input to the A/D converter.	Input	P03/INTP3
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control.	Hi-Z	–
TOFF7	Input	Timer output (TO70 to TO75) stop interrupt input.	Input	P00/INTP0
AD0 to AD7	I/O	Lower address/data bus when memory is expanded externally.	Input	P40 to P47
A8 to A15	Output	Upper address bus when memory is expanded externally.	Input	P50 to P57
\overline{RD}	Output	Strobe signal output for external memory read operation.	Input	P64
\overline{WR}		Strobe signal output for external memory write operation.	Input	P65
\overline{WAIT}	Input	Wait insertion when accessing external memory.	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory.	Input	P67
AV _{REF}	Input	A/D converter reference voltage input.	–	–
AV _{DD}	–	A/D converter analog power supply. Connect to V _{DD0} .	–	–
AV _{SS}	–	A/D converter ground potential. Connect to V _{SS0} .	–	–
\overline{RESET}	Input	System reset input.	–	–
X1	Input	Crystal connection for system clock oscillation.	–	–
X2	–		–	–
V _{DD0}	–	Positive power supply for ports.	–	–
V _{SS0}	–	Ground potential for ports.	–	–
V _{DD1}	–	Positive power supply except for ports.	–	–
V _{SS1}	–	Ground potential except for ports.	–	–
V _{PP}	–	High voltage application during program write/verify. In the normal mode, connect to V _{SS0} directly.	–	–

2.3 Recommended Connection of Unused Pins

The recommended connections of unused pins are shown in Table 2-1.

Table 2-1. Recommended Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins		
P00/INTP0/TOFF7	I/O	Individually connect to V _{SS0} via a resistor.		
P01/INTP1				
P02/INTP2				
P03/INTP3/ADTRG				
P10/ANI0 to P17/ANI7	Input	Individually connect to V _{DD0} or V _{SS0} via a resistor.		
P20/RxD00	I/O			
P21/TxD00				
P22/RxD01				
P23/TxD01				
P24/TI50/TO50				
P25/TI51/TO51				
P26/TI52/TO52				
P30/RTP0 to P37/RTP7				
P40/AD0 to P47/AD7				
P50/A8 to P57/A15				
P64/RD				
P65/WR				
P66/WAIT				
P67/ASTB				
TO70 to TO75			Output	Open
AV _{DD}			-	Connect to V _{DD0} .
AV _{REF}				Connect to V _{SS0} .
AV _{SS}				
V _{PP}	Connect to V _{SS0} directly.			

3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This register is set by software not to use a part of internal memory. The memory mapping can be made the same as that of mask ROM versions with different types of internal memory (ROM and RAM).

IMS is set with 8-bit memory manipulation instructions.

IMS is set to C8H by RESET input.

Figure 3-1. Format of Internal Memory Size Switching Register

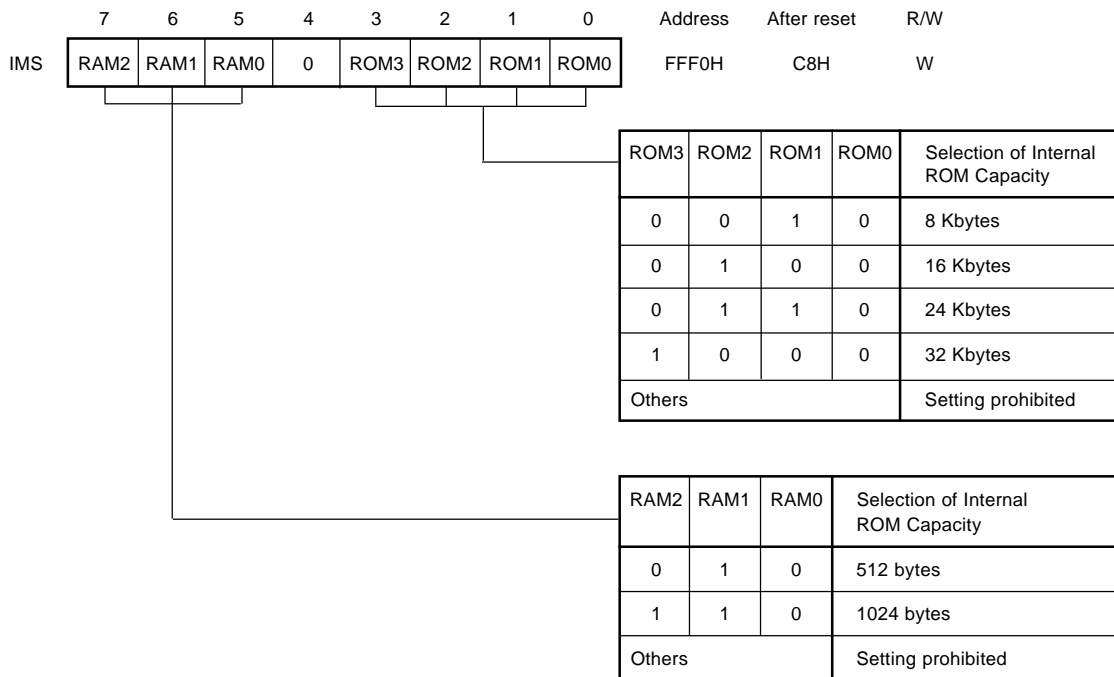


Table 3-1 shows the IMS settings value to make the memory mapping the same as those of mask ROM versions.

Table 3-1. Set Value of Internal Memory Size Switching Register

Target Mask ROM Versions	IMS Setting Value
μPD780961	42H
μPD780962	44H
μPD780963	C6H
μPD780964	C8H

4. FLASH MEMORY PROGRAMMING

Writing to the flash memory can be performed without removing the memory from the target system. Writing is performed connecting the Flashpro to the host machine and the target system.

Remark Flashpro is a product of Naitou Densai Machidaseisakusho Co., LTD.

4.1 Selection of Transmission Method

Writing to flash memory is performed using the Flashpro with a serial transmission method. The transmission methods is selected from those listed in Table 4-1 to perform write operation. Figure 4-1 shows the format to select the transmission mode. Each transmission method is selected according to the number of Vpp pulses shown in Table 4-1.

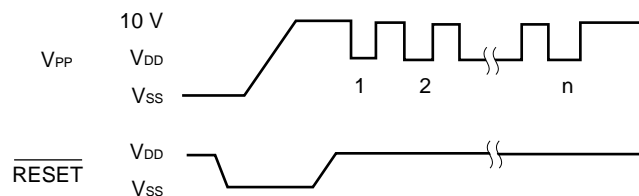
Table 4-1. List of Transmission Methods

Transmission Method	Number of Channels	Pins	Number of V _{PP} Pulses
UART	2	RxD00/P20 TxD00/P21	8
		RxD01/P22 TxD01/P23	9
Pseudo 3-wire mode ^{Note}	2	P24/TI50/TO50 (Serial data input) P25/TI51/TO51 (Serial data output) P26/TI52/TO52 (Serial clock input)	12
		P34/RTP4 (Serial data input) P35/RTP5 (Serial data output) P36/RTP6 (Serial clock input)	13

Note Serial transmission is performed by controlling ports with software.

Caution Always select the transmission method according to the number of Vpp pulses shown in Table 4-1.

Figure 4-1. Format of Transmission Method Selection



4.2. Flash Memory Programming Functions

Operations such as writing to flash memory are performed by various commands/data transmission and reception operations according to the selected transmission method. Table 4-2 shows major functions of flash memory programming.

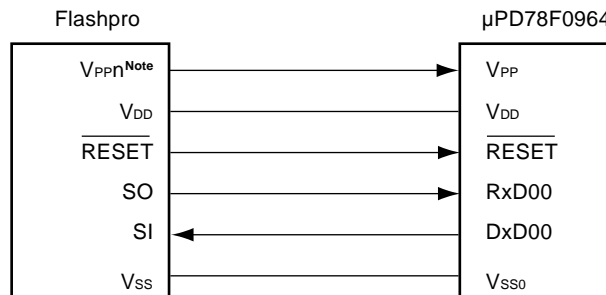
Table 4-2. Major Functions of Flash Memory Programming

Function	Description
One shot erase	Erases the contents of the entire memory.
One shot blank check	Checks that the entire memory has been deleted.
Data write	Performs writing to flash memory according to the write start address and the number of the data to be written (the number of bytes).
One shot verify	Compares the contents of the entire memory and the input data.

4.3 Connection of Flashpro

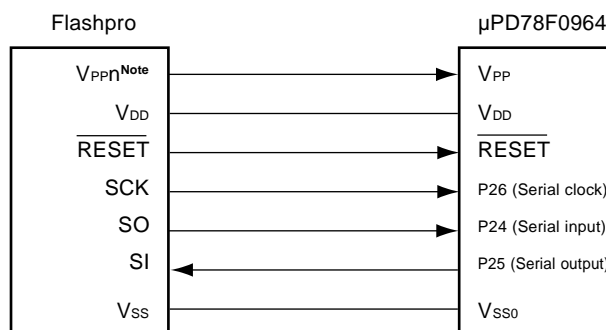
The connection of the Flashpro and the μPD78F0964 differs according to the transmission method. The connection for each transmission method is shown in Figures 4-2, 4-3, and 4-4, respectively.

Figure 4-2. Connection of Flashpro for UART Method (UART00)



Note n = 1, 2

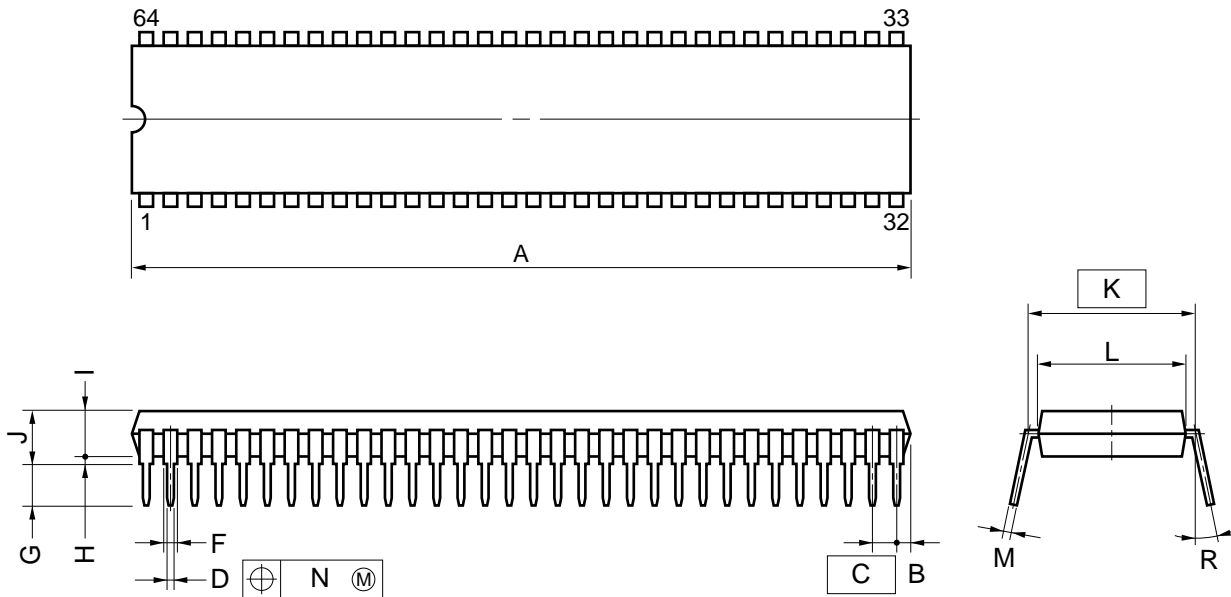
Figure 4-3. Connection of Flashpro for Pseudo 3-Wire Method (Port 2)



Note n = 1, 2

5. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



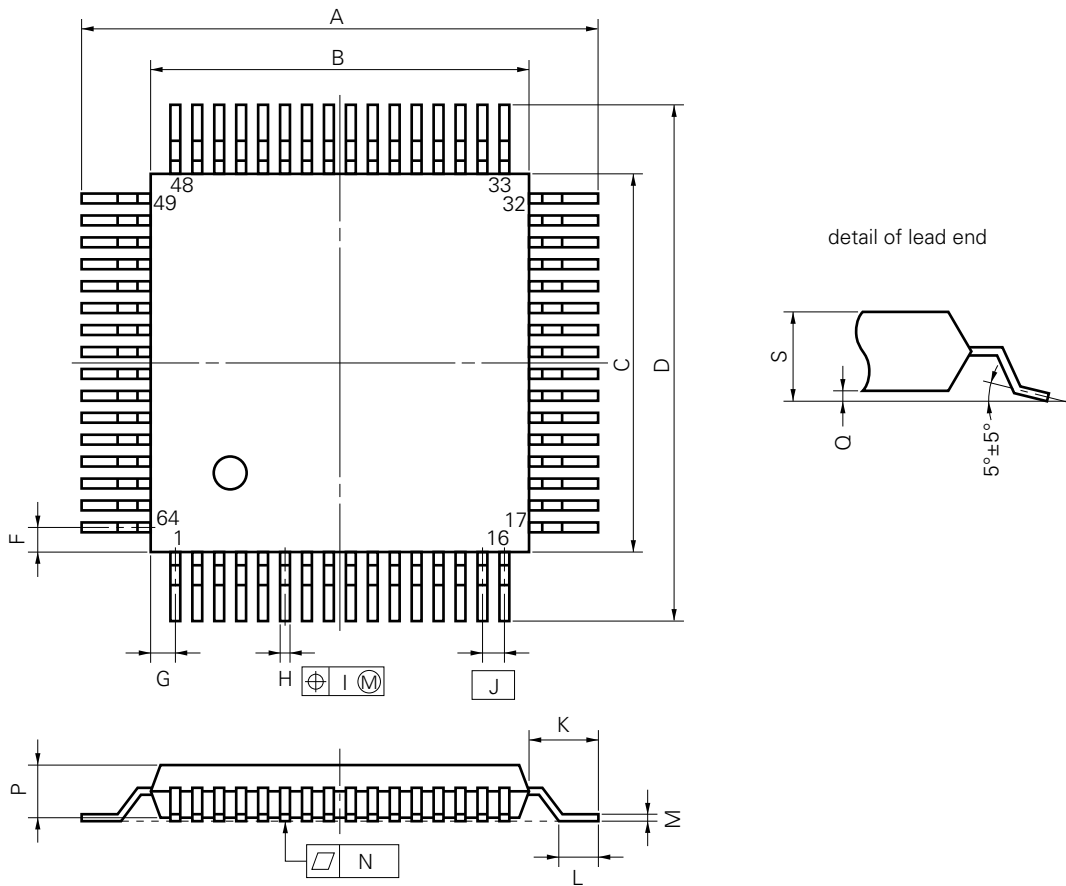
NOTE

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-3

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780964 Subseries.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 Series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 Series common C compiler package
DF780964 Notes 1, 2, 3, 4, 8	μPD780964 Subseries common device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 Series common C compiler library source file

Flash Memory Writing Tools

Flashpro	Dedicated flash memory programmer. The Flashpro is a product of Naitou Densei Machida seisakusho Co., Ltd.
PA-FLASH64CW (temporary name) Note 8 PA-FLASH64GC (temporary name) Note 8	Adapters to write data to the flash memory Products of Naitou Densei Machidaseisakusho Co., Ltd.

Debugging Tools

IE-780000-SL (temporary name) Note 8	75XL, 78K/0S, 78K/0, and 78K/IV Series common in-circuit emulator
IE-78K0-SL-EM (temporary name) Note 8	78K/0 Series common CPU core board
IE-780964-SL-EM1 (temporary name) Note 8	Probe board to emulate μPD780964 Subseries products
EP-64CW-SL (temporary name) Note 8	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-64GC-SL (temporary name) Note 8	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Socket to be mounted on target system board created for the 64-pin plastic QFP (GC-AB8 type)
SM78K0 Notes 5, 6, 7	78K/0 Series common system simulator
ID78K0 Notes 4, 5, 6, 7	IE-780000-SL integrated debugger
DF780964 Notes 4, 5, 6, 7, 8	Device file common to μPD780964 Subseries

Real-Time OSs

RX78K/0 Notes 1, 2, 3, 4	78K/0 Series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 Series OS

Fuzzy Inference Development Support Systems

FE9000 Note 1 /FE9200 Note 6	Fuzzy knowledge data creation tool
FT9080 Note 1 /FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 Series (MS-DOS™) based

2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 Series 300™ (HP-UX™) based
4. HP9000 Series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 Series (EWS-UX/V) based
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Remark RA78K/0, CC78K/0, SM78K0, ID78K0, and RX78K/0 are used in combination with DF780964.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No.	
	English	Japanese
μPD780924, 780964 Subseries User's Manual	Planned	In preparation
μPD780961, 780962, 780963, 780964 Preliminary Product Information	Planned	U11879J
μPD78F0964 Preliminary Product Information	This document	U11956J
μPD780924, 780964 Subseries Special Function Register Table	—	Planned
78K/0 Series User's Manual Instructions	IEU-1372	IEU-849
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J

Development Tool Documents (User's Manuals)

Document Name		Document No.	
		English	Japanese
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	EEU-817
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC 78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	EEU-777
IE-780000-SL		Planned	Planned
IE-78K0-SL-EM		Planned	Planned
IE-780964-SL-EM1		Planned	Planned
EP-64CW-SL		Planned	Planned
EP-64GC-SL		Planned	Planned
SM78K0 System Simulator Windows-based	Reference	U10181E	U10181J
SM78K Series System Simulator	External parts user open interface specification	U10092E	U10092J
ID78K0 Integrated Debugger EWS-based	Reference	U11151E	U11151J
ID78K0 Integrated Debugger PC-based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows-based	Guide	U11649E	U11649J

Caution The above related documents are subject to change without notice. Be sure to use the latest documents when starting design.

Embedded Software Documents (User's Manuals)

Document Name		Document No.	
		English	Japanese
78K/0 Series Real-Time OS	Basics	—	U11537J
	Installation	—	U11536J
	Technical	—	U11538J
78K/0 Series OS MX78K0	Basics	EEU-1532	EEU-5010
Fuzzy Knowledge Data Creation Tool		EEU-1438	EEU-829
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-1444	EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-1441	EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-1458	EEU-921

Other Documents

Document Name		Document No.	
		English	Japanese
IC Package Manual		C10943X	
Semiconductor Device Mounting Technology Manual		C10535E	C10535J
Quality Grades on NEC Semiconductor Devices		C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System		C10983E	C10983J
Electrostatic Discharge (ESD) Test		—	MEM-539
Guide to Quality Assurance for Semiconductor Devices		MEI-1202	MEI-603
Microcomputer Product Series Guide		—	U11416J

Caution The above related documents are subject to change without notice. Be sure to use the latest documents when starting design.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)

Santa Clara, California
 Tel: 800-366-9782
 Fax: 800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
 Tel: 0211-65 03 02
 Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.

Milton Keynes, UK
 Tel: 01908-691-133
 Fax: 01908-670-290

NEC Electronics Italiana s.r.l.

Milano, Italy
 Tel: 02-66 75 41
 Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH

Benelux Office
 Eindhoven, The Netherlands
 Tel: 040-2445845
 Fax: 040-2444580

NEC Electronics (France) S.A.

Velizy-Villacoublay, France
 Tel: 01-30-67 58 00
 Fax: 01-30-67 58 99

NEC Electronics (France) S.A.

Spain Office
 Madrid, Spain
 Tel: 01-504-2787
 Fax: 01-504-2860

NEC Electronics (Germany) GmbH

Scandinavia Office
 Taebly, Sweden
 Tel: 08-63 80 820
 Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.

Hong Kong
 Tel: 2886-9318
 Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch
 Seoul, Korea
 Tel: 02-528-0303
 Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

United Square, Singapore 1130
 Tel: 253-8311
 Fax: 250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan
 Tel: 02-719-2377
 Fax: 02-719-5951

NEC do Brasil S.A.

Sao Paulo-SP, Brasil
 Tel: 011-889-1680
 Fax: 011-889-1689

The related documents in this publication may include preliminary versions. However, preliminary versions are not marked as such.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

M4 96.5

FIP and IEBus are trademarks of NEC Corporation.

MS-DOS and Windows are trademarks of Microsoft Corporation.

IBM DOS, PC/AT, and PC DOS are trademarks of International Business Machines Corporation.

HP9000 Series 300, HP9000 series 700, and HP-UX are trademarks of Hewlett-Packard Company.

SPARCstation is a trademark of SPARC International, Inc.

SunOS is a trademark of Sun Microsystems, Inc.

NEWS and NEWS-OS are trademarks of Sony Corporation.