PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

µPD78F0949

8-BIT SINGLE-CHIP MICROCONTROLLER

Description

The µPD78F0949 is a member of the 78K/0 series microcontrollers. Besides a high speed, high performance CPU, these microcontrollers have on-chip ROM, RAM, I/O ports, 8-bit resolution A/D converter, timer, CAN-interface, serial interface, interrupt control, LCD-controller/driver and various other peripheral hardware.

The µPD78F0949 device includes a FLASH EEPROM version which can operate in the same power supply voltage range as the mask ROM version.

The details of the functions are described in the following user manuals. Be sure to read it before starting design.

µPD780949, Subseries User's Manual : U12670EE
78K/0 Series User's Manual - Instructions : U12336EJ

Features

- Internal high capacity ROM and RAM

Item / Part Number	Program	Data Memory				Package
	Memory (ROM)	Internal High-Speed RAM	LCD Display RAM	Internal Expansion RAM	EEPROM	
µPD78F0949	60K bytes	1024 bytes	40 bytes	992 bytes	256 bytes	100-pin plastic QFP (fine pitch)

- External memory expansion
- Instruction execution time can be changed from high speed (0.25 µs) to ultra low speed
- I/O ports: 79 (N-ch open drain : 5)
- 8-bit resolution A/D converter : 8 channels
- Sound generator
- LCD-controller / driver
- CAN-Interface
- Serial interface : 3 channels
  - 2-wire mode : 1 channel
  - 3-wire mode : 1 channel
  - UART mode : 1 channel
- Timer : 6 channels
- Supply voltage : V_{DD} = 4.0 to 5.5 V

Application

Dashboard, climate controller, security unit etc.

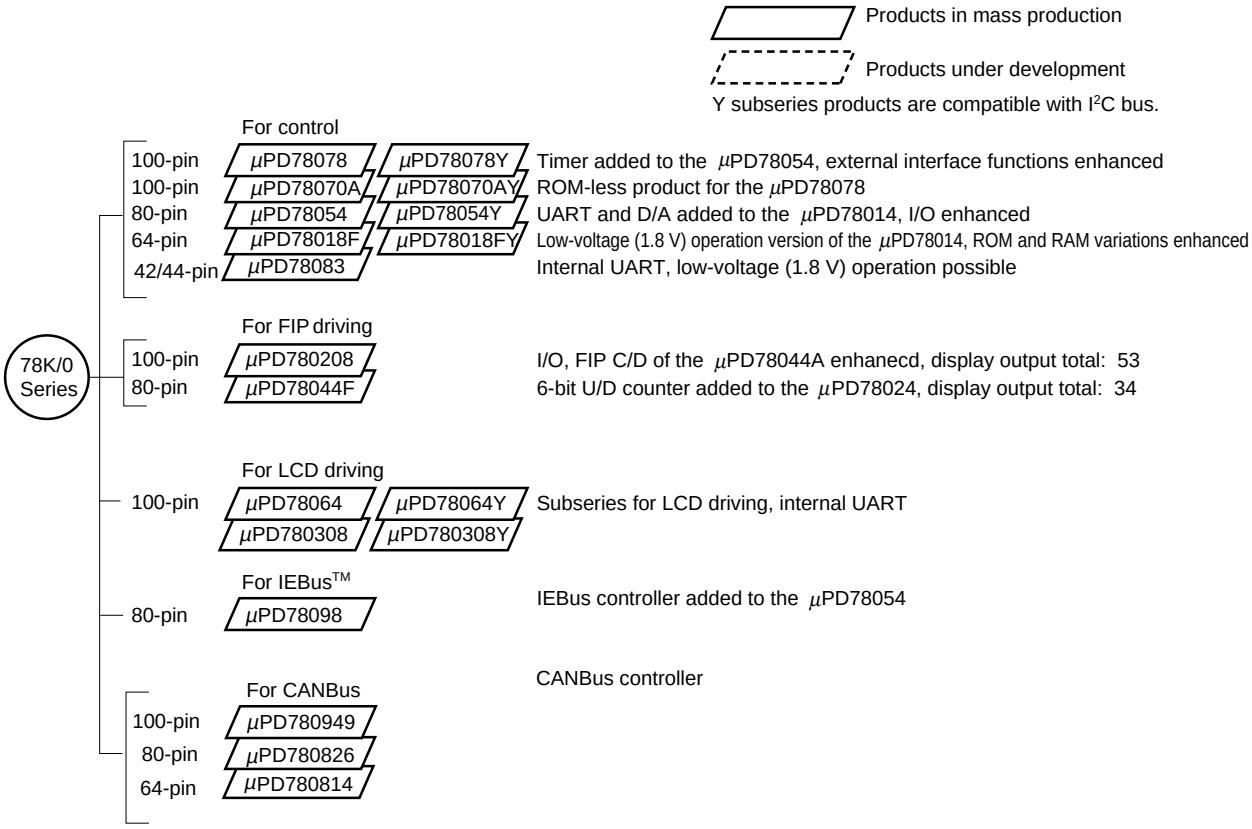
Document No. U13976EE1V0PM00
Date : February 1999

Ordering Information

Part Number	Package
μPD78F0949GF-3BA	100-pin plastic QFP (14 x 20 mm, resin thickness 2.7 mm)

78K/0 Series Development

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Overview of Functions

Item \ Part Number		μPD78F0949
Internal memory	ROM	60 Kbytes
	Internal high-speed RAM	1024 bytes
	LCD Display RAM	40 bytes
	Internal Expansion RAM	992 bytes
	EEPROM	256 bytes
Memory space		64 Kbytes
General registers		8 bits x 32 registers (8 bits x 8 registers x 4 banks)
Instruction cycle		On-chip instruction execution time selective function
	When main system clock selected	0,25 μs/0,5 μs/1 μs/2 μs/4 μs (at 8 MHz)
	When subsystem clock selected	122 μs (at 32.768 kHz)
Instruction set		• 16-bit operation • Multiplication/division (8 bits x 8 bits, 16 bits – 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD adjustment, etc.
I/O ports		Total : 79 • CMOS input : 8 • CMOS I/O : 71
A/D converter		• 8 bit resolution x 8 channels
Serial Interface		• 3-wire mode : 1 channel • 2-wire mode : 1 channel • UART mode : 1 channel
Timer		• 16 bit timer / event counter : 2 channels • 8 bit timer / event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		3 (16-bit PWM output x 1, 8-bit PWM output x 2)
Clock output		62,5 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 4 MHz, 8 MHz (at main system clock of 8.0 MHz)
CAN		1 channel
Vectored interrupts	Maskable interrupts	Internal : 22 External : 5
	Non-maskable interrupts	Internal : 1
	Software interrupts	Internal : 1
Supply voltage		V_{DD} = 4,0 V to 5,5 V
Package		100-pin plastic QFP (14 mm x 20 mm)

Major Changes

Page	Description
18	The internal high-speed RAM is 1024 x 8 bits

Note: The mark ★ shows major revised points.

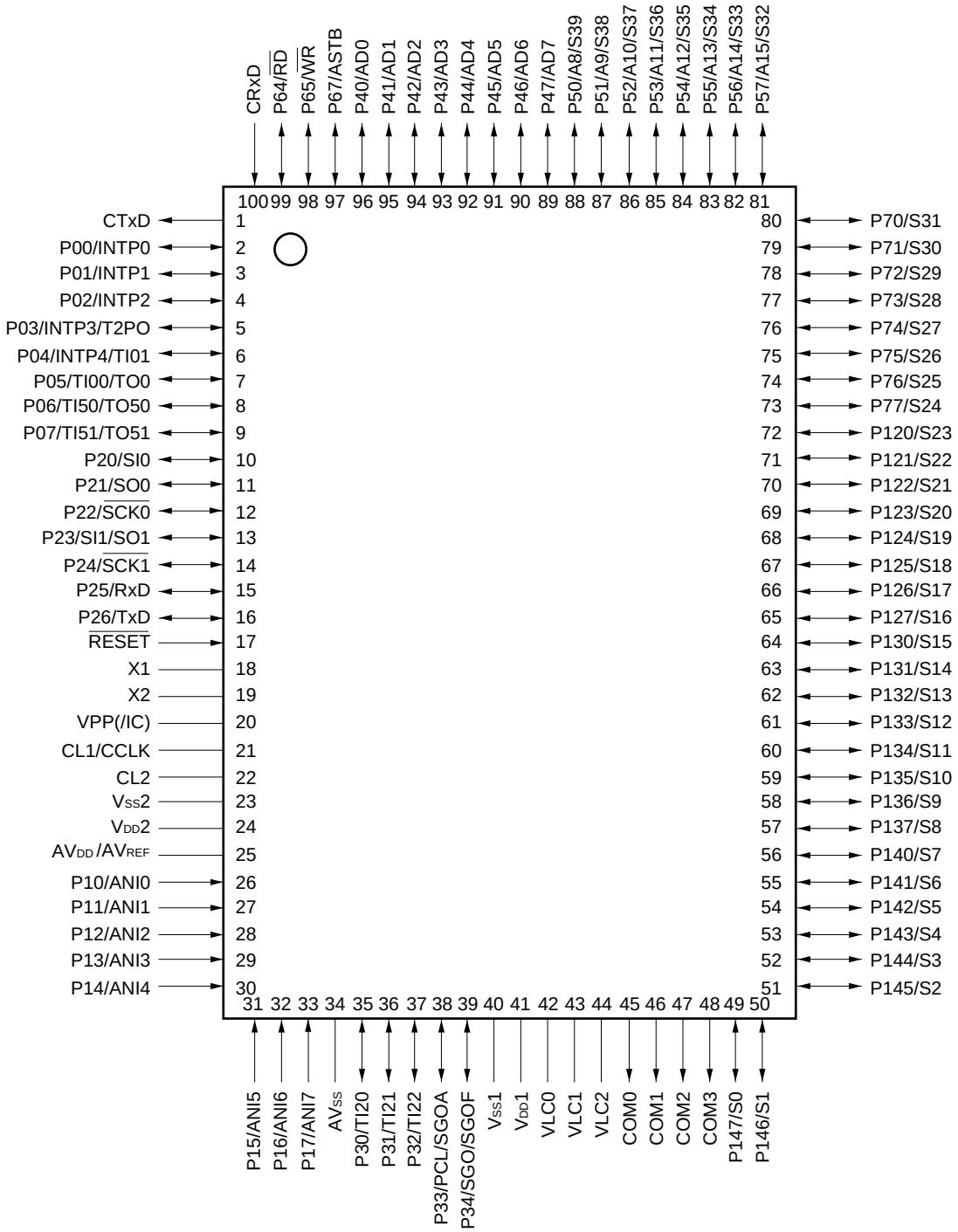
Contents

1. Pin Configuration (Top View)

⇑100-pin plastic QFP (14 x 20 mm)

μPD78F0949GF-3BA

Figure 1-1: Pin Configuration



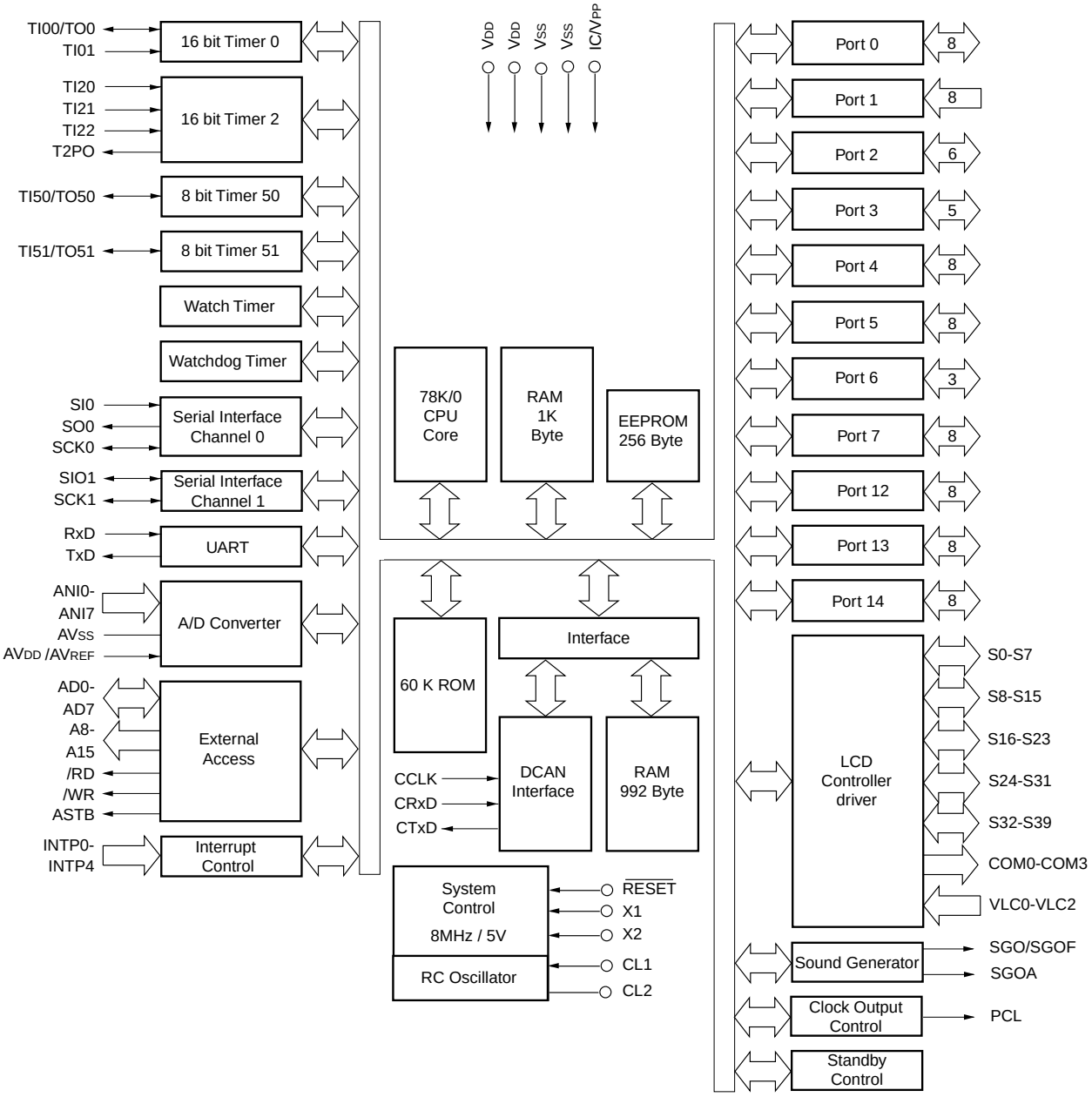
Cautions:
1. **Connect IC (internally connected) pin directly to V_{SS}.**
2. **AV_{SS} pin should be connected to V_{SS}.**
3. **AV_{DD} pin should be connected to V_{DD}.**

Pin Identifications

P00 to P07	:	Port0
P10 to P17	:	Port1
P20 to P26	:	Port2
P30 to P34	:	Port3
P40 to P47	:	Port4
P50 to P57	:	Port5
P64, P65, P67	:	Port6
P70 to P77	:	Port7
P120 to P127	:	Port12
P130 to P137	:	Port13
P140 to P147	:	Port14
INTP0 to INTP4	:	Interrupt from Peripherals
TI00, TI01, TI50, TI51	:	Timer Input
TI20 to TI22	:	Timer Input
TO0 , TO51, TO52	:	Timer Output
T2PO	:	Timer Output
CRxD	:	CAN Receive Data
CTxD	:	CAN Transmit Data
CCLK	:	CAN Clock
SI0	:	Serial Input
SO0	:	Serial Output
SIO1	:	Serial Input / Output
SCK0, SCK1	:	Serial Clock
RxD	:	Receive Data
TxD	:	Transmit Data
SGO	:	Sound Generator Output
SGOA	:	Sound Generator Amplitude
SGOF	:	Sound Generator Frequency
PCL	:	Programmable Clock Output
AD0 to AD7	:	Address / Data Bus
A8 to A15	:	Address Bus
RD	:	Read Strobe
WR	:	Write Strobe
ASTB	:	Address Strobe
S0 to S39	:	Segment Output
COM0 to COM3	:	Common Output
X1, X2	:	Crystal (Main System Clock)
CL1, CL2	:	RC (Subsystem Clock)
RESET	:	Reset
ANI0 to ANI7	:	Analog Input
AV_{SS}	:	Analog Ground
AV_{DD}/AV_{REF}	:	Analog Reference Voltage and Analog Power Supply
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power supply
V_{SS}	:	Ground
IC	:	Internally Connected

2. Block Diagram

Figure 2-1: Block Diagram



3. Pin Functions

3.1 Normal Operating Mode Pins / Pin Input/Output Types

Table 3-1: Pin Input/Output Types (1/2)

Input / Output	Pin Name	Function	Alternate Function	After Reset
Input / Output	P00	Port 0 8 bit input / output port Input / output mode can be specified bit-wise A pull-up resistor can be connected by software bit-wise.	INTP0	Input
	P01		INTP1	Input
	P02		INTP2	Input
	P03		INTP3/T2P0	Input
	P04		INTP4/TI01	Input
	P05		TI00/TO0	Input
	P06		TI50/TO50	Input
	P07		TI51/TO51	Input
Input	P10-P17	Port 1 8 bit input port Input mode can be specified bit-wise.	ANI0-ANI7	Input
Input / Output	P20	Port 2 7 bit input/output port Input / output mode can be specified bit-wise.	SI0	Input
	P21		SO0	Input
	P22		/SCK0	Input
	P23		SI/SO1	Input
	P24		/SCK1	Input
	P25		RxD	Input
	P26		TxD	Input
Input / Output	P30	Port 3 5 bit input / output port Input / output mode can be specified bit-wise A pull-up resistor can be connected by software bit-wise.	TI20	Input
	P31		TI21	Input
	P32		TI22	Input
	P33		PCL/SGOA	Input
	P34		SGO/SGOF	Input
Input/ Output	P40-P47	Port 4 8 bit input / output port Input / output mode can be specified bit-wise If used as an input port, a pull-up resistor can be connected by software .	AD0-AD7	Input
Input/ Output	P50-P57	Port 5 8 bit input / output port Input / output mode can be specified bit-wise This port can be used in External Memory Expansion Mode with the 4, 6 or 8 bit address by setting the Memory Expansion Mode Register Not for external memory expansion used ports can be used either for LCD or port function.	A8/S39-A15/S32	Input
Input / Output	P64	Port 6 3 bit input / output port input / output mode can be specified bit-wise	/RD	Input
	P65		/WR	Input
	P67		ASTB	Input

Table 3-1: Pin Input/Output Types (2/2)

Input / Output	Pin Name	Function	Alternate Function	After Reset
Input/ Output	P70-P77	Port 7 8 bit input / output port Input / output mode can be specified bit-wise A pull-up resistor can be connected by software. This port can be used as a segment signal output port or an I/O port in 1 bit units by setting the port function	S31-S24	Input
Input/ Output	P120-P127	Port 12 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as a segment signal output port or an I/O port in 8 bit units by setting the port function.	S23-S16	Input
Input/ Output	P130-P137	Port 13 8 bit input / output port Input / output mode can be specified bit-wise If used as an input port, a pull-up resistor can be connected by software This port can be used as a segment signal output port or an I/O port in 8 bit units by setting the port function.	S15-S8	Input
Input/ Output	P140-P147	Port 14 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as a segment signal output port or an I/O port in 8 bit units by setting the port function.	S7-S0	Input

3.2 Non-Port Pins

Table 3-2: Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function Pin
INTP0	Input	External interrupts with selectable valid edges (rising edge, falling edge, both rising and falling edges)	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/T2P0
INTP4				P04/TI01
SI0	Input	Serial interface serial data input	Input	P20
SI1				P23/SO1
SO0	Output	Serial interface serial data output	Input	P21
SO1				P23/SI1
$\overline{SCK0}$	Input/ Output	Serial interface serial clock input / output	Input	P22
$\overline{SCK1}$				P24
RxD	Input	Asynchronous serial interface data input	Input	P25
TxD	Output	Asynchronous serial interface data output	Input	P26
CRxD	Input	CAN serial data input	Input	-
CTxD	Output	CAN serial data output	Output	-
CCLK	Input	CAN serial clock input	-	CL1
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P05/TO0
TI01				P04/INTP4
TI20		Capture trigger input		P30
TI21		Capture trigger input		P31
TI22		Capture trigger input		P32
TI50		External count clock input to 8-bit timer (TM50)		P06/TO50
TI51		External count clock input to 8-bit timer (TM51)		P07/TO51
TO0	Output	16-bit timer output	Input	P05/TI00
T2P0		16-bit timer output		P03/INTP3
TO50		8-bit timer output (also used for PWM output)		P06/TI50
TO51		8-bit timer output (also used for PWM output)		P07/TI51
PCL	Output	Clock output (for main system clock trimming)	Input	P33/SGOA
AD0 to AD7	Input/ Output	Low-order address/data bus at external memory expansion	Input	P40 to P47
A8 to A15	Output	High-order address/data bus at external memory expansion	Input	P50 to P57 S39 to S32
$\overline{RD}$	Output	Strobe signal output for read operation from external memory	Input	P64
$\overline{WR}$		Strobe signal output for read operation from external memory		P65
ASTB	-	Strobe output externally latching address information output to ports 4, 5 to access external memory	Input	P67
S0 to S7	Output	Segment signal output of LCD controller / driver	Input	P147 to P140
S8 to S15				P137 to P130
S16 to S23				P127 to P120
S24 to S31				P77 to P70
S32 to S39				P57 to P50 A15 to A8

Table 3-2: Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function Pin
COM0-COM3	Output	Common signal output of LCD controller/driver	Output	-
$V_{LC}0$ to $V_{LC}2$	-	LCD drive voltage	-	-
SGO	Output	Sound generator output	Input	P34/SGOF
SGOA	Output	Sound generator amplitude output	Input	P33/PCL
SGOF	Output	Sound generator frequency output	Input	P34/SGO
ANI0 to ANI7	Input	A/D Converter analog input	Input	P10 – P17
AV_{DD}/AV_{REF}	-	A/D Converter reference voltage input and power supply	-	-
AV_{SS}	-	A/D Converter ground potential. Connect to V_{SS}.	-	-
$\overline{RESET}$	Input	System reset input	-	-
X1	-	Crystal connection for main system clock	-	-
X2	-		-	-
CL1	Input	RC connection for subsystem clock	-	CCLK
CL2	-		-	-
$V_{DD}1$, $V_{DD}2$	-	Positive power supply	-	-
$V_{SS}1$, $V_{SS}2$	-	Ground potential	-	-
V_{PP}	-	High voltage supply for flash programming (only flash version)	-	IC
IC	-	Internal connection. Connect directly to V_{SS} (only MaskROM version)	-	V_{PP}

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in the following table.

For the input/output circuit configuration of each type, see table.

Table 3-3: Types of Pin Input/Output Circuits (1/3)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00/INTP0	8-A	I/O	Connect to Vdd or Vss via a resistor individually
P01/INTP1			
P02/INTP2			
P03/INPT3/T2P0			
P04/INTP4/TI01			
P05/TI00/TO0			
P06/TI50/TO50			
P07/TI51/TO51			
P10/ANI0	11-B	I	Connect to Vdd or Vss via a resistor individually
P11/ANI1			
P12/ANI2			
P13/ANI3			
P14/ANI4			
P15/ANI5			
P16/ANI6			
P17/ANI7			
P20/SI0	10	I/O	Connect to Vdd or Vss via a resistor individually
P21/SO0			
P22/SCK0			
P23/SI1/SOA			
P24/SCK1			
P25/RxD	8		
P26/TxD	5		
P30/TI20	8	I/O	Connect to Vdd or Vss via a resistor individually
P31/TI21			
P32/TI22			
P33/PCL/SGOA	5		
P34/SGO/SGOF			
P40/AD0	5-A	I/O	Connect to Vdd or Vss via a resistor individually
P41/AD1			
P42/AD2			
P43/AD3			
P44/AD4			
P45/AD5			
P46/AD6			
P47/AD7			

Table 3-3: Types of Pin Input/Output Circuits (2/3)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P50/A8/S39	17	I/O	Connect to Vdd or Vss via a resistor individually
P51/A9/S38			
P52/A10/S37			
P53/A11/S36			
P54/A12/S35			
P55/A13/S34			
P56/A14/S33			
P57/A15/S32			
P64/$\overline{RD}$	5-A	I/O	Connect to Vdd or Vss via a resistor individually
P65/$\overline{WR}$			
P67/ASTB			
P70/S31	17-B	I/O	Connect to Vdd or Vss via a resistor individually
P71/S30			
P72/S29			
P73/S28			
P74/S27			
P75/S26			
P76/S25			
P77/S24			
P120/S23	17-C	I/O	Connect to Vdd or Vss via a resistor individually
P121/S22			
P122/S21			
P123/S20			
P124/S19			
P125/S18			
P126/S17			
P127/S16			
P130/S15	17-A	I/O	Connect to Vdd or Vss via a resistor individually
P131/S14			
P132/S13			
P133/S12			
P134/S11			
P135/S10			
P136/S9			
P137/S8			
P140/S7	17-A	I/O	Connect to Vdd or Vss via a resistor individually
P141/S6			
P142/S5			
P143/S4			
P144/S3			
P145/S2			
P146/S1			
P147/S0			

Table 3-3: Types of Pin Input/Output Circuits (3/3)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
COM0 – COM3	18	O	Leave open
$V_{LC}0$ – $V_{LC}2$	-	-	
CRxD	1	I	Connect to Vdd via a resistor individually
CTxD	2	O	Leave open
CL1/CCLK	-	-	Connect to Vdd or Vss via a resistor individually
CL2	-	-	Leave open
$\overline{\text{RESET}}$	1	I	-
AV_{DD}/AV_{REF}	-	-	Connect to V_{DD}
AV_{SS}	-	-	Connect to V_{SS}
IC	-	-	Connect directly to V_{SS}
V_{PP}			

Figure 3-1: Pin Input/Output Circuits (1/3)

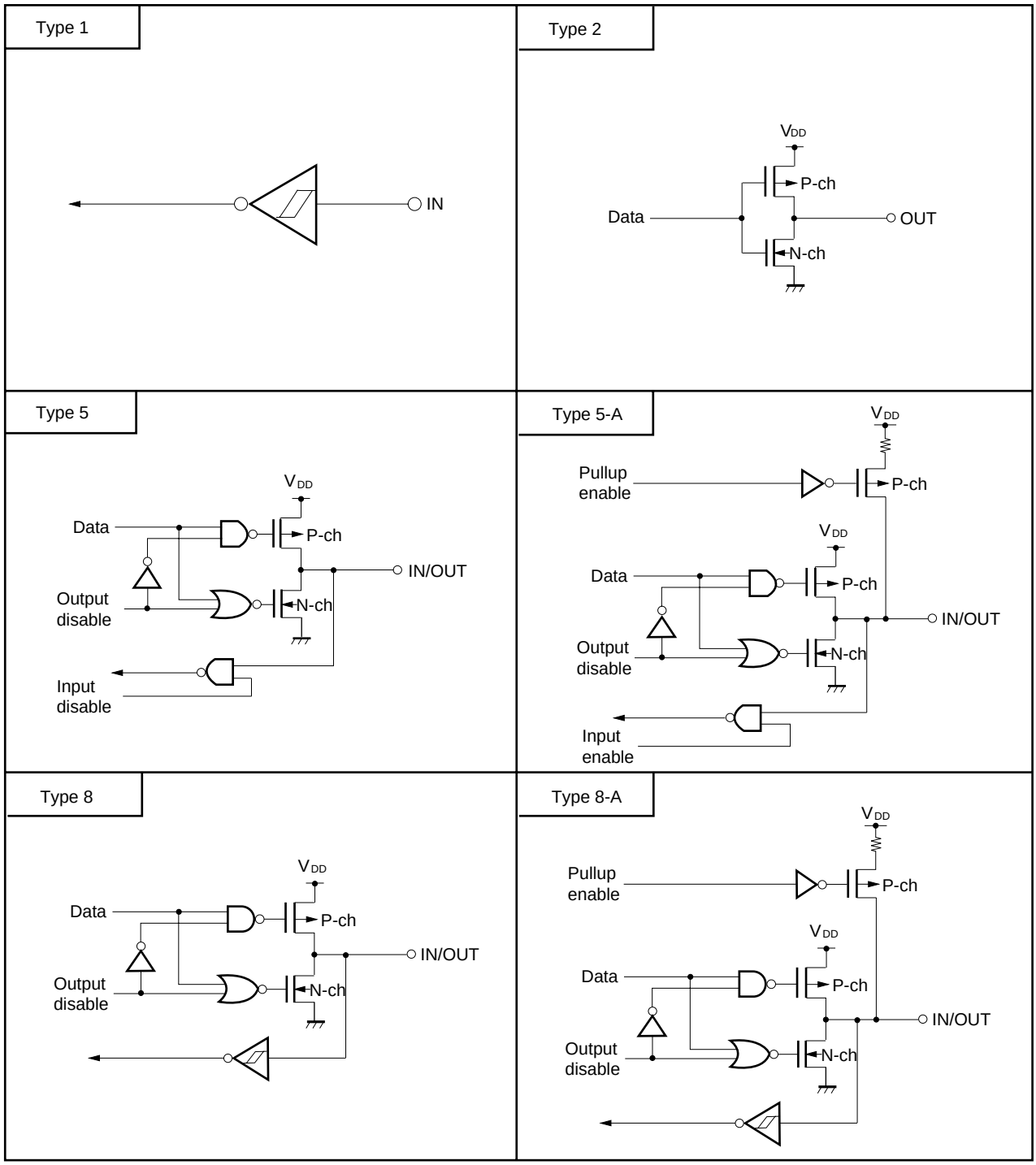


Figure 3-1: Pin Input/Output Circuits (2/3)

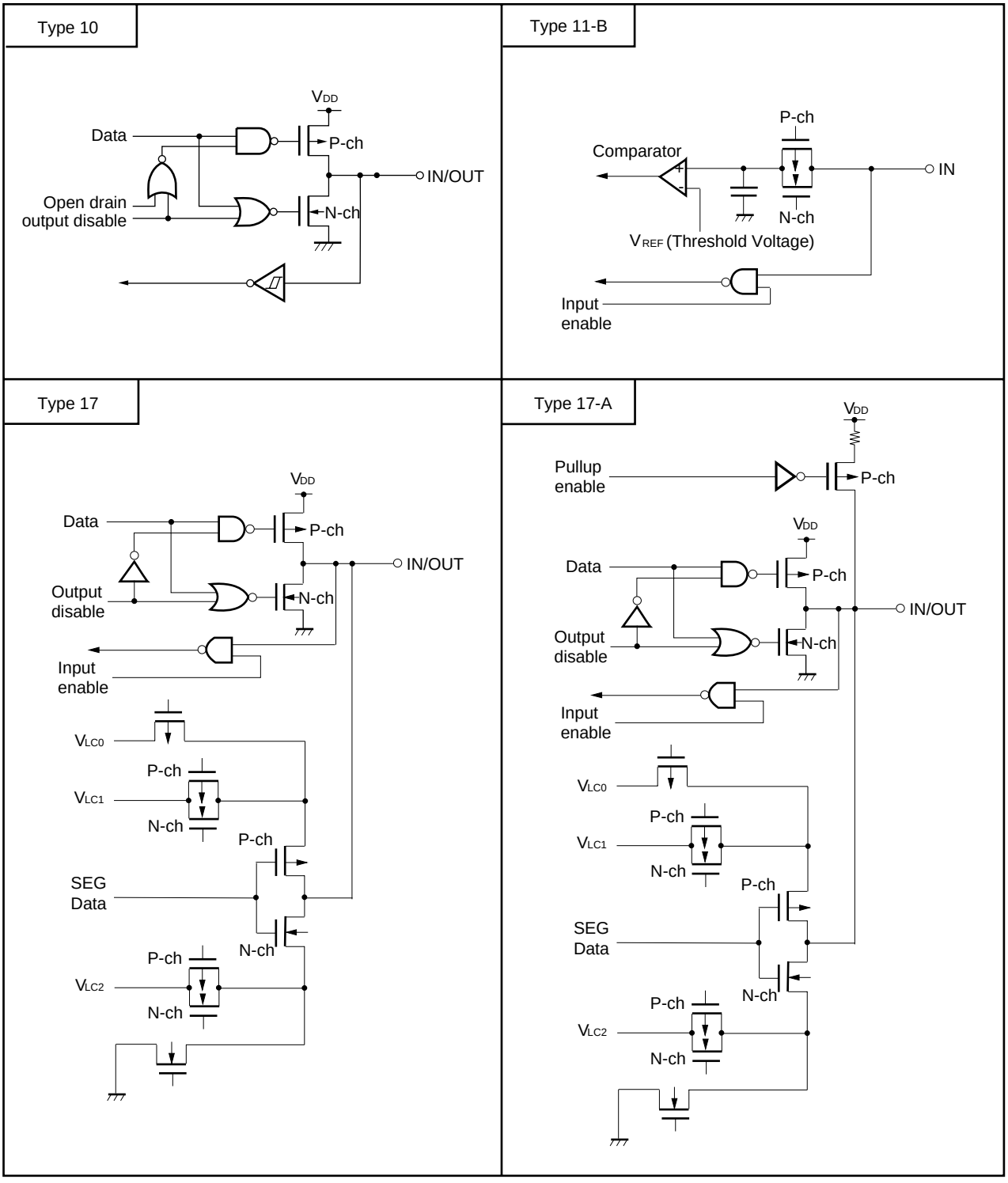
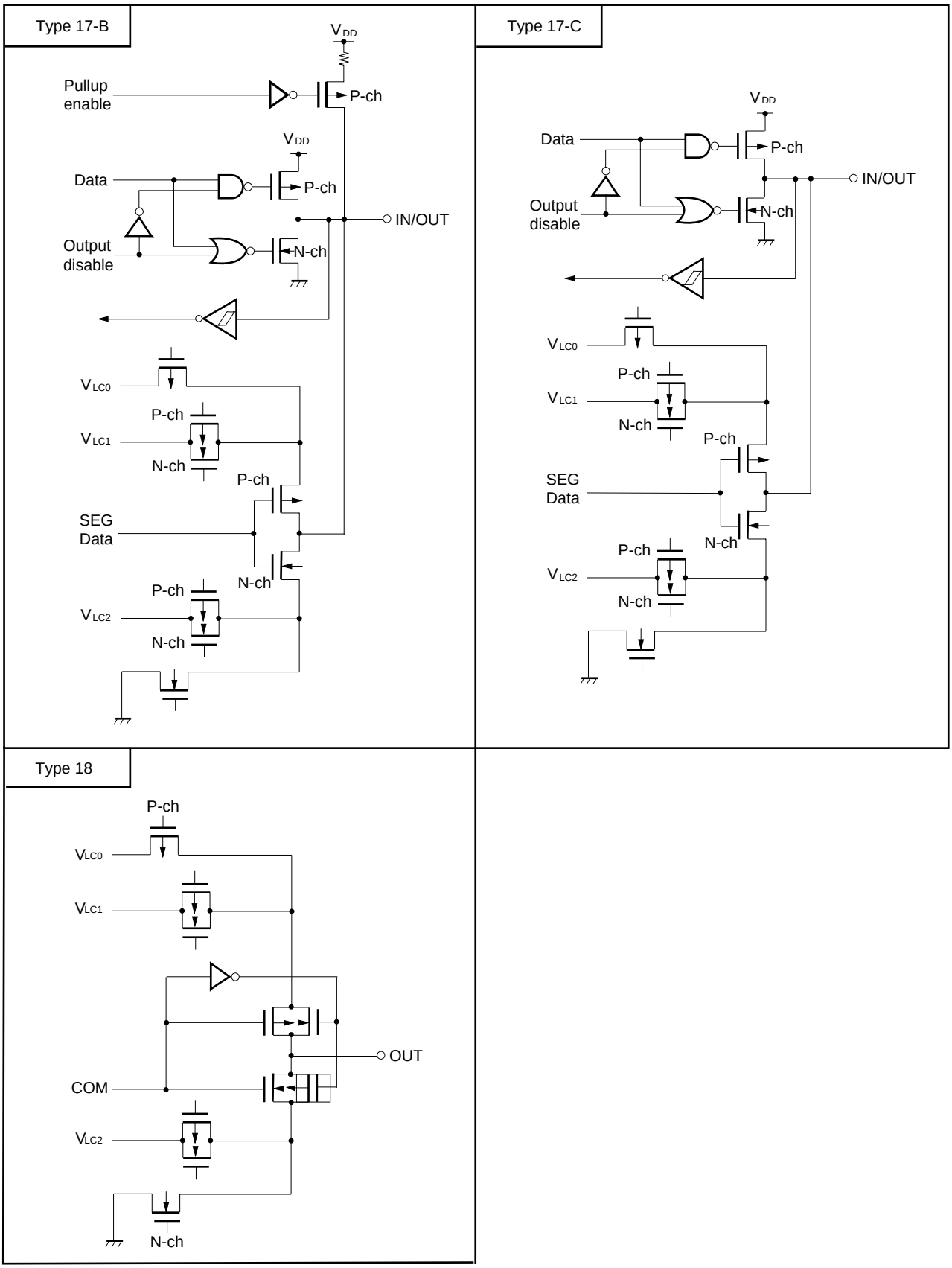


Figure 3-1: Pin Input/Output Circuits (3/3)



4. Flash Memory Programming

Writing to the flash memory can be performed without removing the memory from the target system. Writing is performed connecting the Flash Programmer to the host machine and the target system.

4.1 Selection of Transmission Method

Writing to flash memory is performed using the Flash Programmer with a serial transmission method. The transmission method is selected from those listed in Table 4-1 to perform write operation. Figure 4-1 shows the format to select the transmission mode. Each transmission method is selected according to the number of V_{PP} pulses shown in Table 4-1.

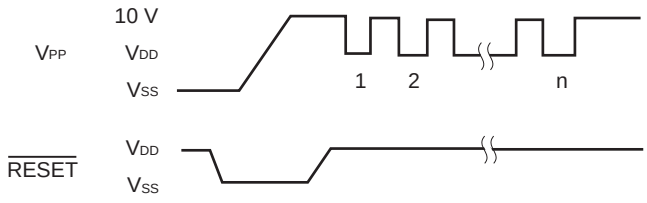
Table 4-1: List of Transmission Methods

Transmission Method	Number of Channels	Pins	Number of V_{PP} Pulses
3-Wire Mode	1	SI0/P20, SO0/P21, SCK/P22	0
UART Mode	1	RxD/P24, TxD/P25	8
Pseudo 3-Wire Mode Note	1	(Serial SI input)/P30	12
		(Serial SO output)/P31	
		(Serial SCK input)/P32	

Note: Serial transmission is performed by controlling ports with software.

Caution: Always select the transmission method according to the number of V_{PP} pulses shown in Table 4-1.

Figure 4-1: Format of Transmission Method Selection



4.2. Flash Memory Programming Functions

Operations such as writing to flash memory are performed by various commands/data transmission and reception operations according to the selected transmission method. Table 4-2 shows major functions of flash memory programming.

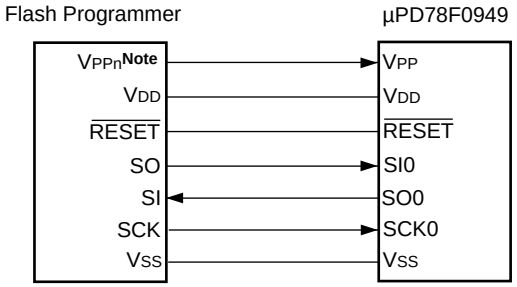
Table 4-2: Major Functions of Flash Memory Programming

Function	Description
Reset	Detects write stop and transmission synchronisation.
Batch verify	Compares entire memory contents and input data.
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs writing to flash memory according to write start address and umber of write data (bytes).
Continuous write	Performs successive write operations using the data input with high speed operation.
Status	Checks the current operation mode and operation end.
Oscillation frequency setting	Inputs the resonator oscillation frequency information.
Delete time setting	Inputs the memory delete time.
Baud rate setting	Sets the transmission rate when the UART method is used.
Silicon signature read	Outputs the device name, memory capacity, and device block information.

4.3 Connection of Flashpro

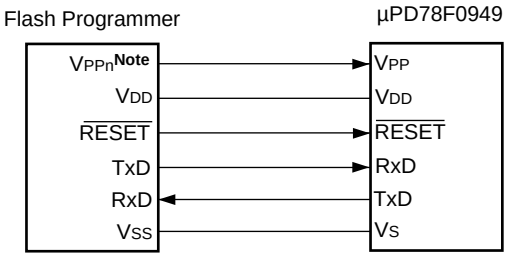
The connection of the Flash Programmer and the μPD78F0949 differs according to the transmission method. The connection for each transission method is shown in Figures 4-1, 4-2, and 4-3, respectively.

Figure 4-2: Connection of Flash Programmer for 3-Wire Method (SI030)



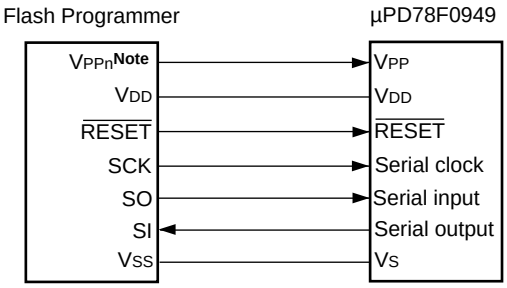
Note: n = 1, 2

Figure 4-3: Connection of Flash Programmer for UART Method (UART)



Note: n = 1, 2

Figure 4-4: Connection of Flash Programmer for Pseudo 3-Wire Method (Port)

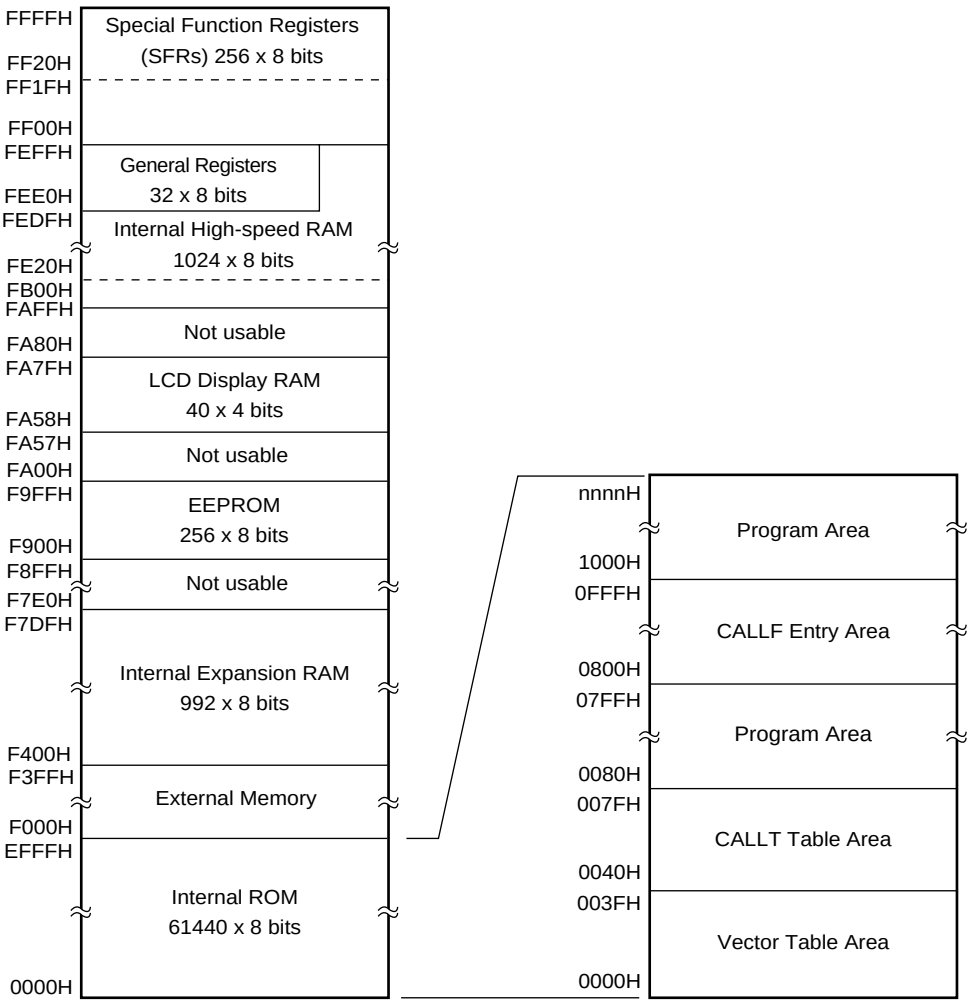


Note: n = 1, 2

5. Memory Space

The memory map of the μPD78F0949 is shown in Figure 5-1.

Figure 5-1: Memory Map



6. Peripheral Hardware Function

6.1 Ports

Input/output ports are classified into three types.

- CMOS input/output (Port 0, Port 2 to 5, P64, P65, P67, Port 7, Port 8, Port 12, Port 13, Port 14) : 71
- Input (P10 to P17) : 8

Total : 79

Table 6-1: Functions of Ports

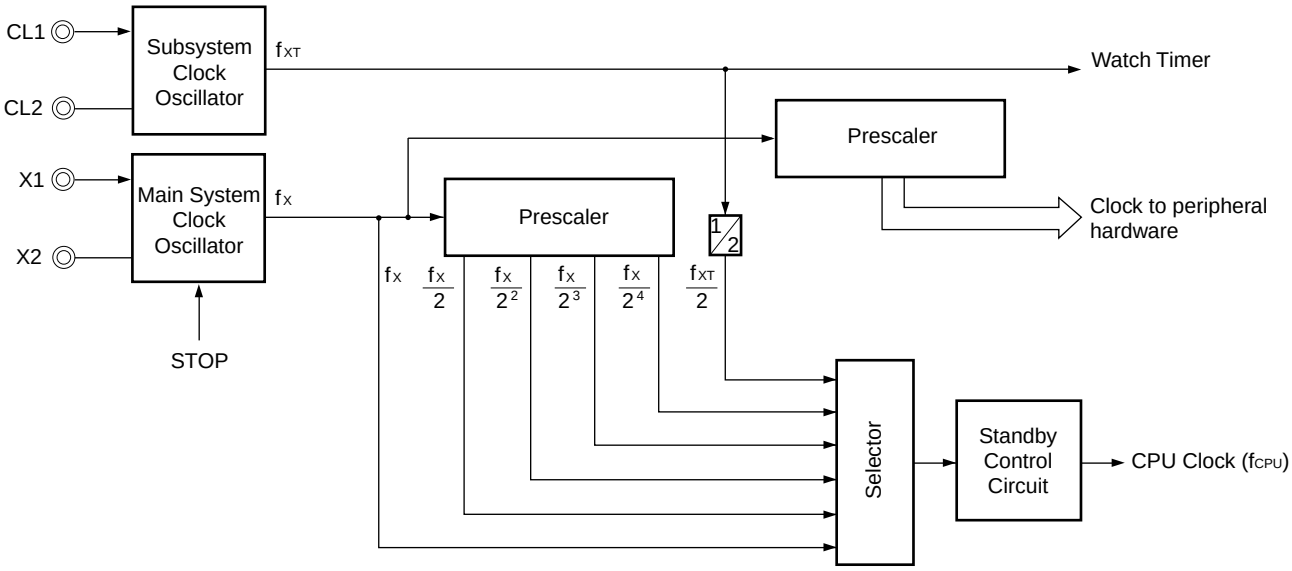
Port Name	Pin Name	Function
Port 0	P00 to P07	Input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be set bit-wise by software.
Port 1	P10 to P17	Input port.
Port 2	P20 to P26	Input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be set bit-wise by software to an open drain structure.
Port 3	P30 to P34	Input/output port. Input/output can be specified bit-wise.
Port 4	P40 to P47	Input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be set bit-wise by software..
Port 5	P50 to P57	Input/output port. Input/output can be specified bit-wise. When used as an output port, port function can be specified by software.
Port 6	P64, P65, P67	Input/output port. Input/output can be specified bit-wise.
Port 7	P70 to P77	Input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be set bit-wise by software. When used as an output port, port function can be specified by software.
Port 12	P120 to P127	Input/output port. Input/output can be specified bit-wise. When used as an output port, port function can be specified by software.
Port 13	P130 to P137	Input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be set bit-wise by software. When used as an output port, port function can be specified by software.
Port 14	P140 to P147	Input/output port. Input/output can be specified bit-wise.

6.2 Clock Generator

There are two kinds of clock generators: main system and subsystem clock generators.
It is possible to change the instruction execution time.

- 0.25 μs/0.5 μs/1 μs/2 μs/4 μs (at main system clock frequency of 8.0 MHz)
- 122 μs (at subsystem clock frequency of 32.768 kHz)

Figure 6-1: Clock Generator Block Diagram

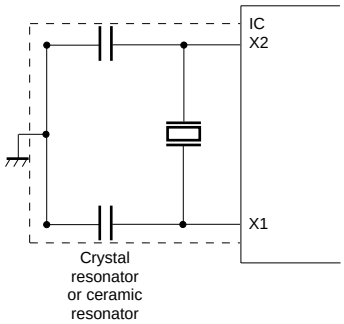


6.3 Main system clock oscillator

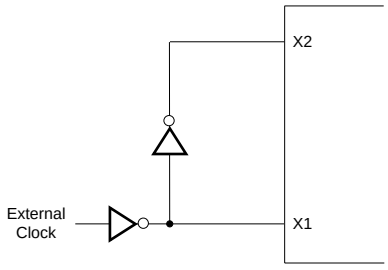
The main system clock oscillator oscillates with a crystal or a ceramic resonator connected to the X1 and X2 pins.

Figure 6-2: Oscillator Circuit

(a) Crystal and ceramic oscillation



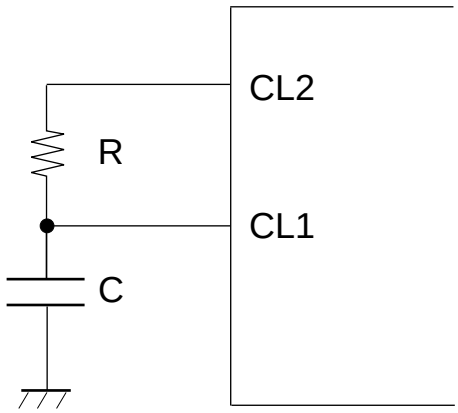
(b) External clock



6.4 Subsystem Clock Oscillator

Subsystem clock oscillator is for RC oscillation with very low frequency.

Figure 6-3: Oscillator Circuit



6.5 Timer/Event Counter

There are the following six timer/event counter channels:

- 16-bit timer/event counter : 2 channels
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 6-2: T ypes and Functions of Timer/Event Counters

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer	16-bit Timer
Type	Interval timer	2 channels	2 channels	1 channel	1 channel	1 channel
	External event counter	1 channel	2 channels	—	—	—
Function	Timer output	1 output	2 outputs	—	—	—
	PWM output	1 output	2 outputs	—	—	—
	Pulse with measurement	2 inputs	—	—	—	3 inputs
	Square wave output	1 output	2 outputs	—	—	—
	One-shot pulse output	1 output	—	—	—	—
	Interrupt request	2	2	2	1	4
	Test input	—	—	1	—	3

Figure 6-4: 16 bit Timer TM0

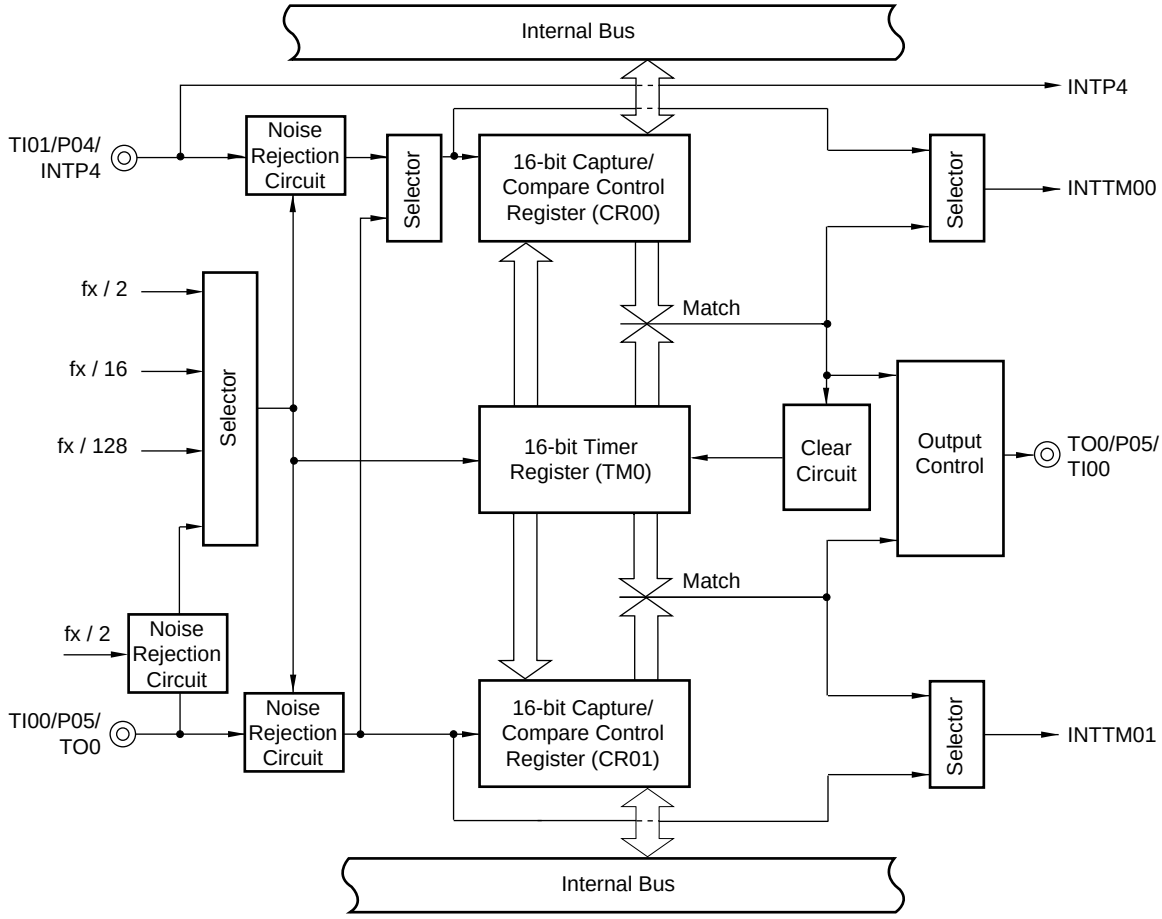
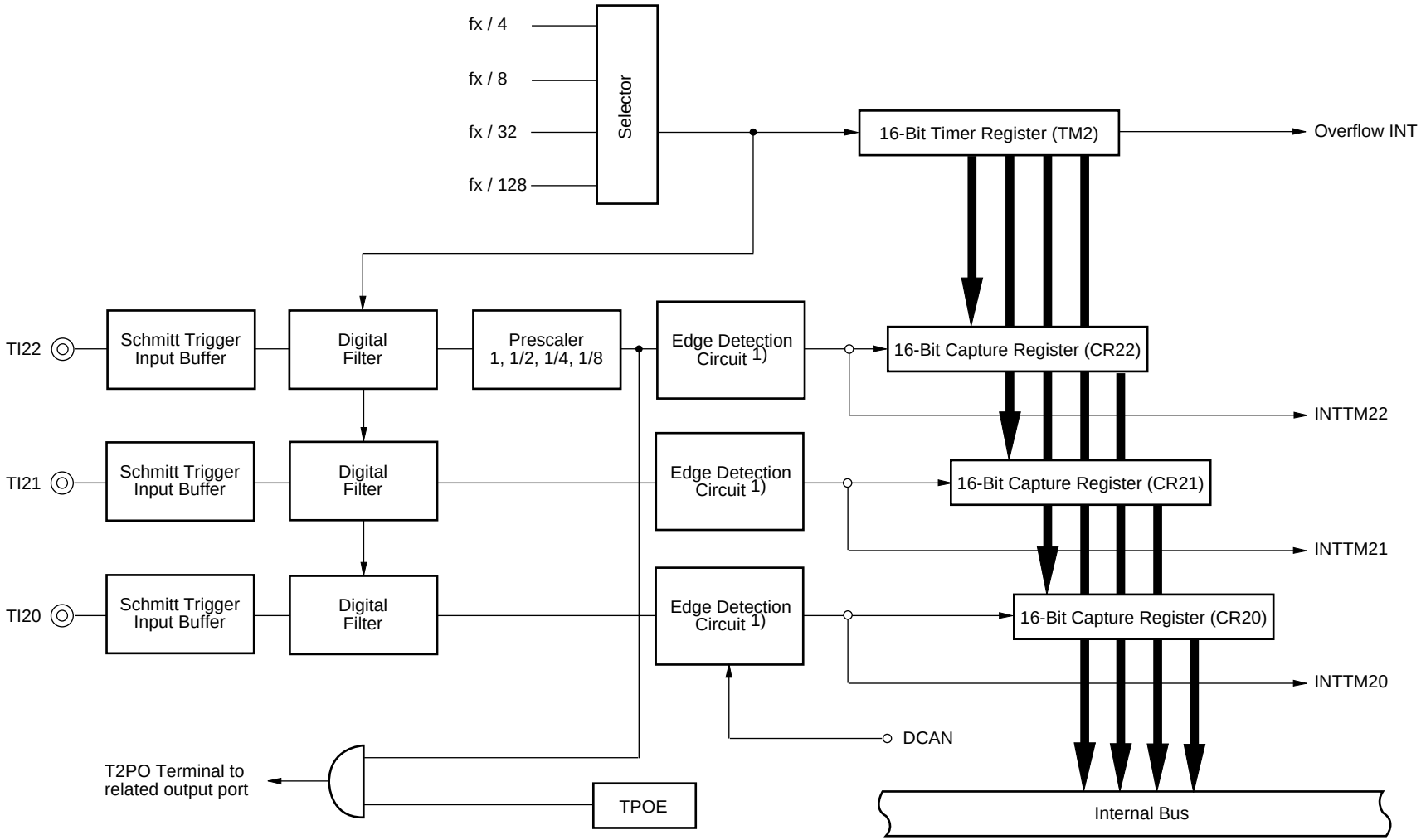


Figure 6-5: 16 Bit Timer TM2



1) Valid edge (rising edge, falling edge or both edges) is selectable via software

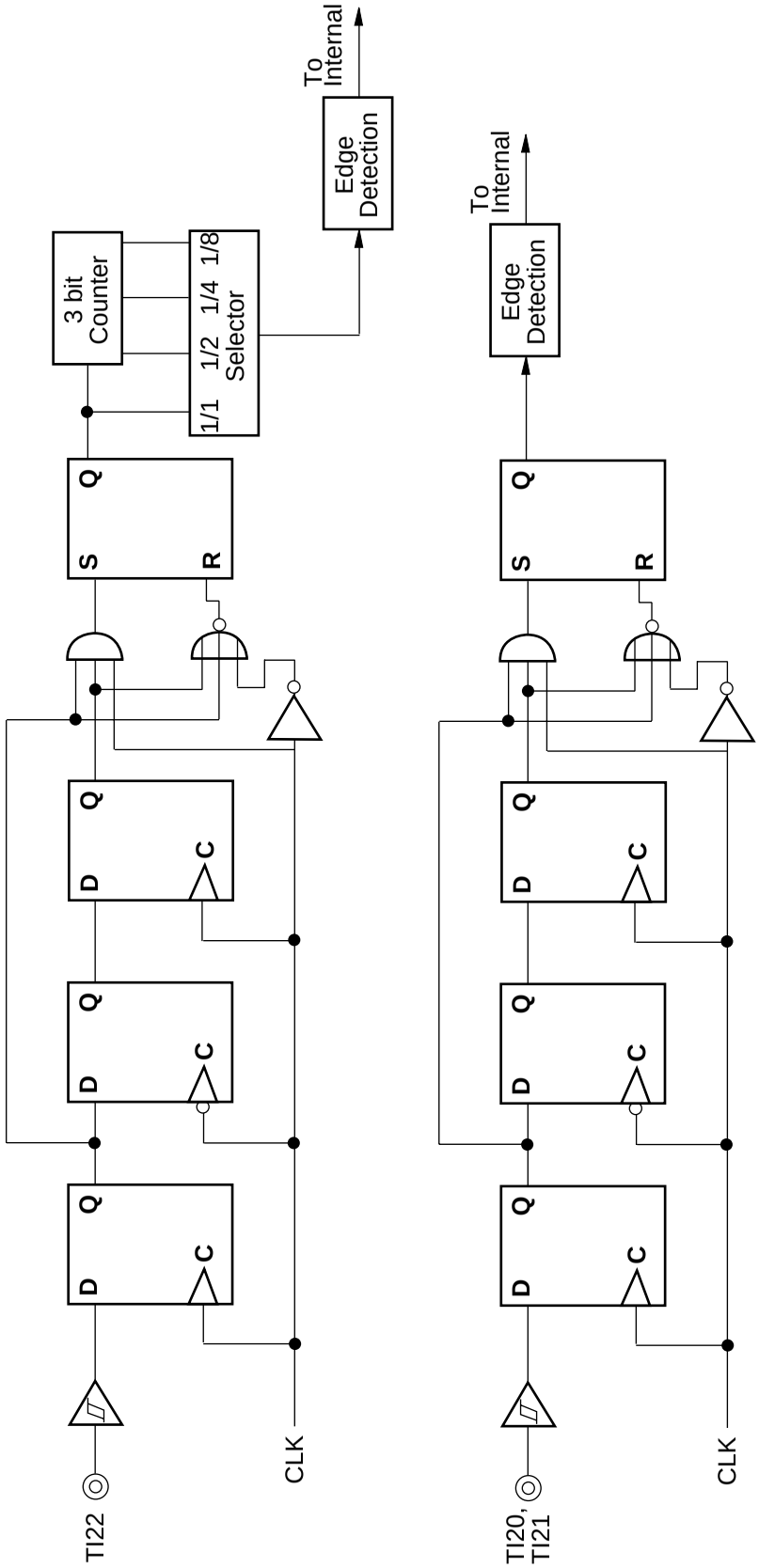


Figure 6-6: Digital Capture Input Filter

Figure 6-7: 8-Bit Timer/Event Counter 51 Block Diagram

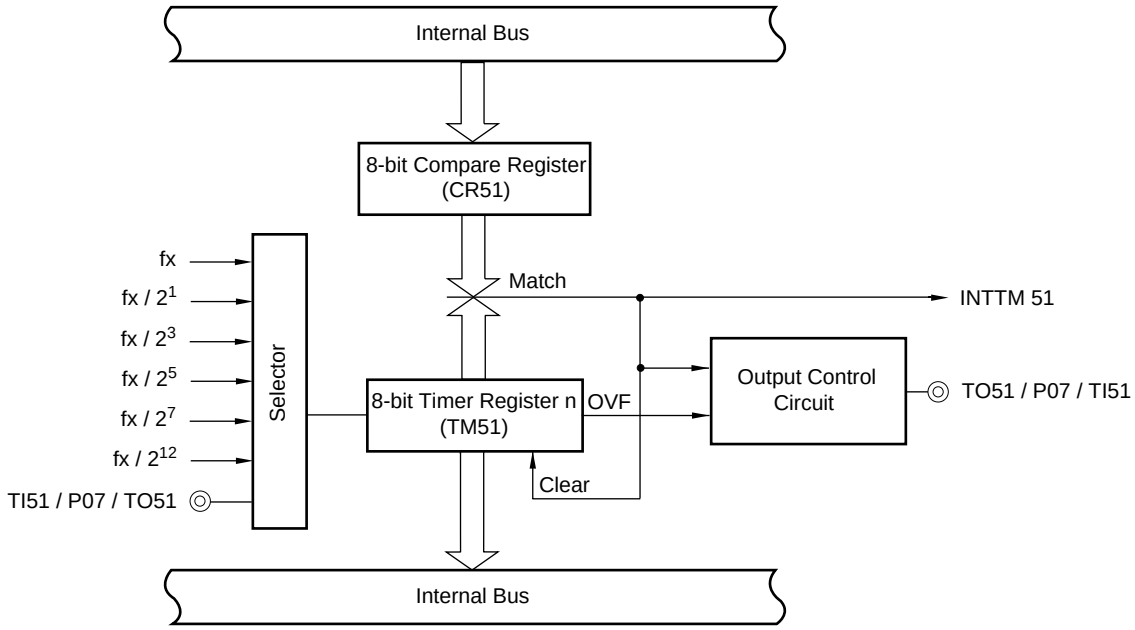


Figure 6-8: 8-Bit Timer/Event Counter 50 Block Diagram

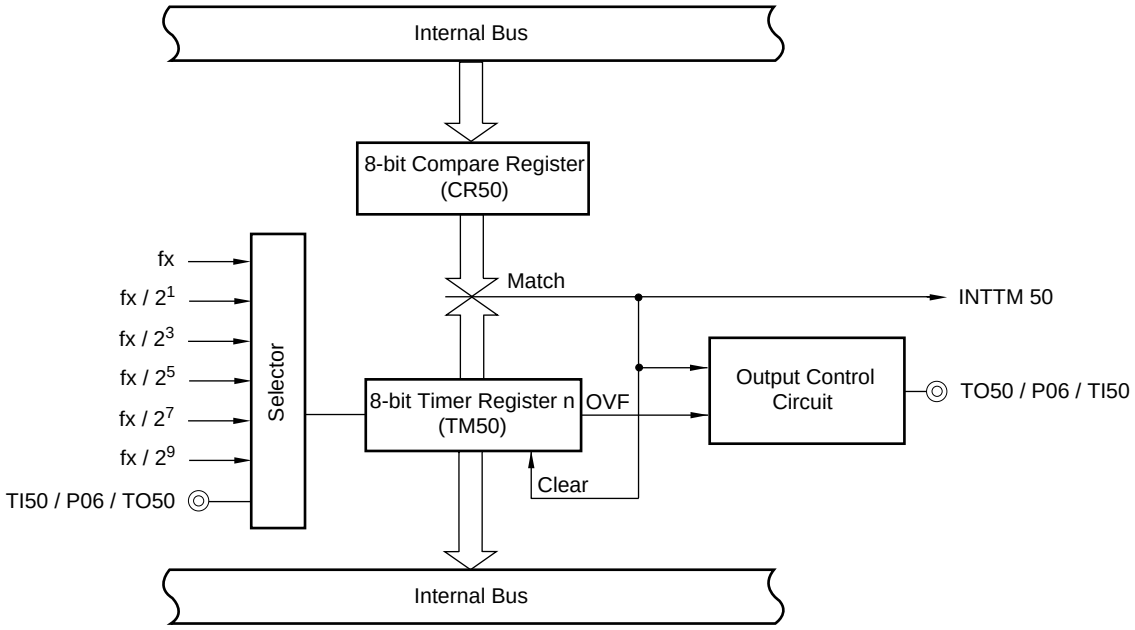


Figure 6-9: Watch Timer Block Diagram

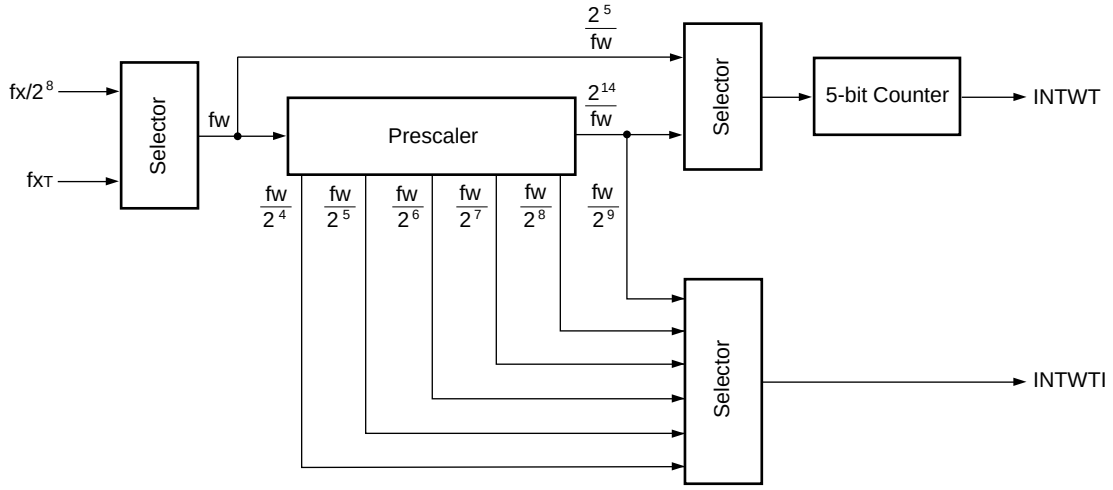
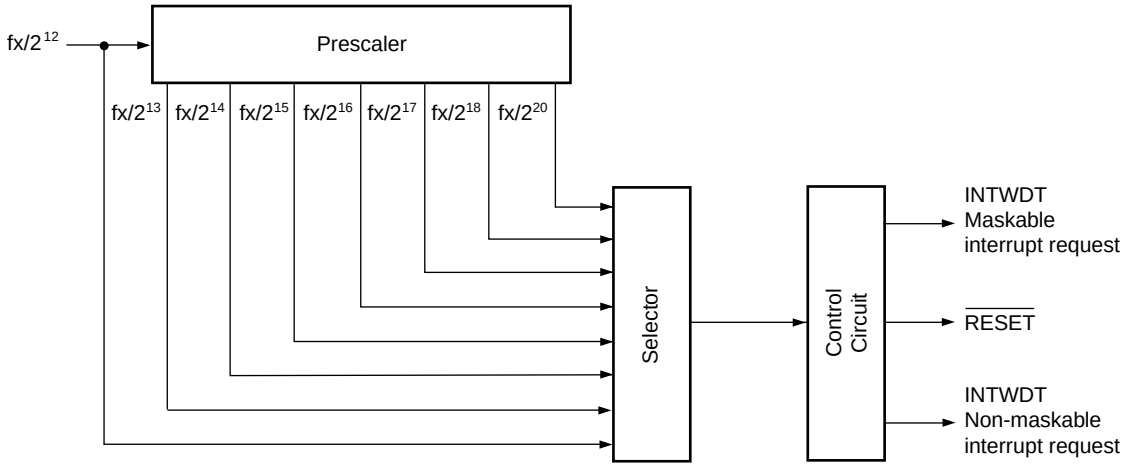


Figure 6-10: Watchdog Timer Block Diagram

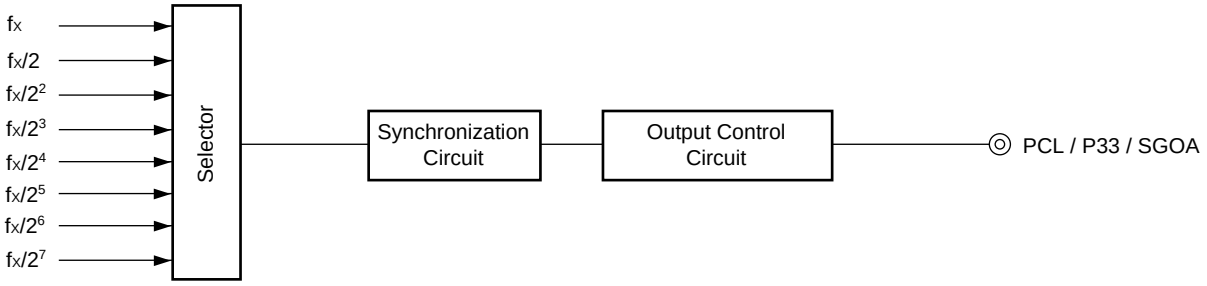


6.6 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 62.5 kHz/125 kHz/250 kHz/500 kHz/1 MHz/2 MHz/4 MHz/8 MHz (at main system clock frequency of 8.0 MHz)

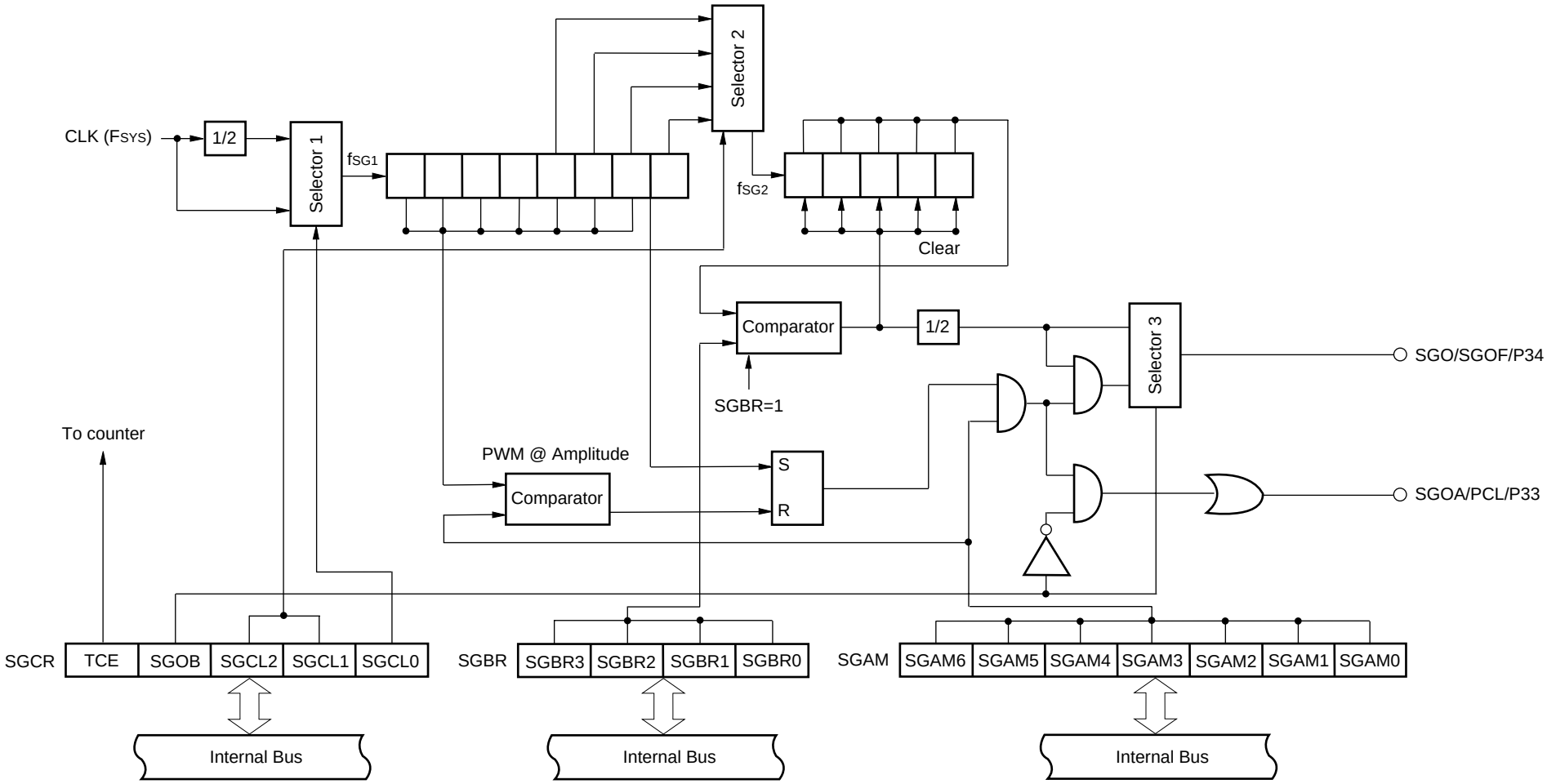
Figure 6-11: Clock Output Control Circuit Block Diagram



6.7 Sound Generator

The sound generator will produce sounds composed of a rectangular frequency signal and a PWM signal for volume control.

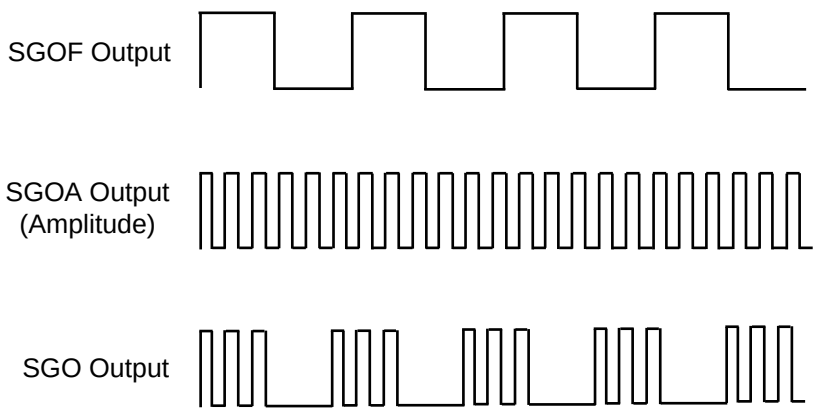
Figure 6-12: Block Diagram of the Sound Generator



The sound generator output is selectable as separate frequency-/volume-output SGOF/SGOA or as composed signal SGO.

The output signal at the composed output has the following principle shape:

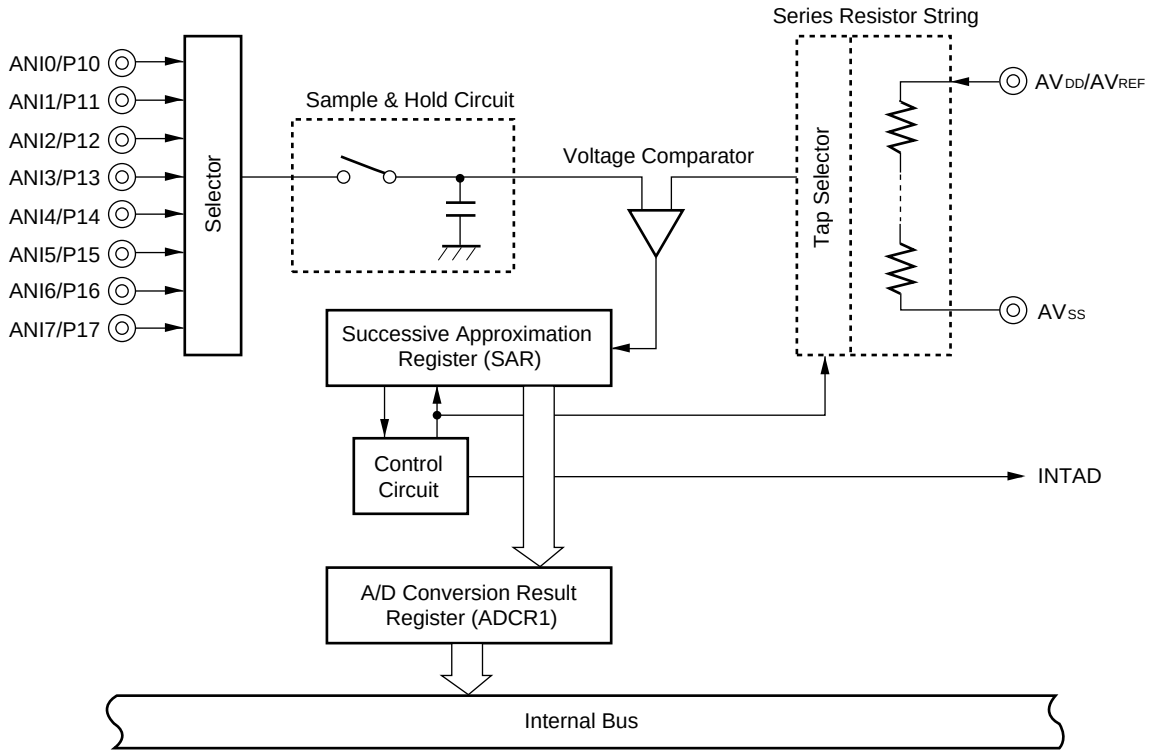
Figure 6-13: Composed Sound Generator Output SGO



6.8 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.
A/D conversion can be started by software.

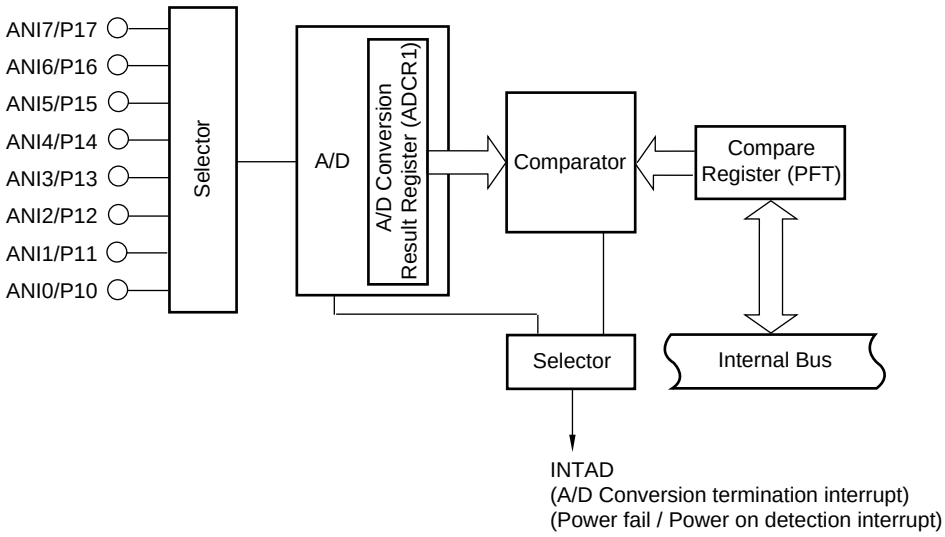
Figure 6-14: A/D Converter Block Diagram



6.9 Power Fail Detector

The block diagram of the power fail detector is shown in figure 6-15.

Figure 6-15: Block Diagram Power Fail Detector



6.10 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 6-3: Types and Functions of Serial Interfaces

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	○ (MSB first)	—	—
2-wire serial I/O mode	—	○ (MSB first)	—
Asynchronous serial interface (UART) mode	—	—	○(On-chip dedicated baud rate generator)

Figure 6-16: Serial Interface Channel 0 Block Diagram

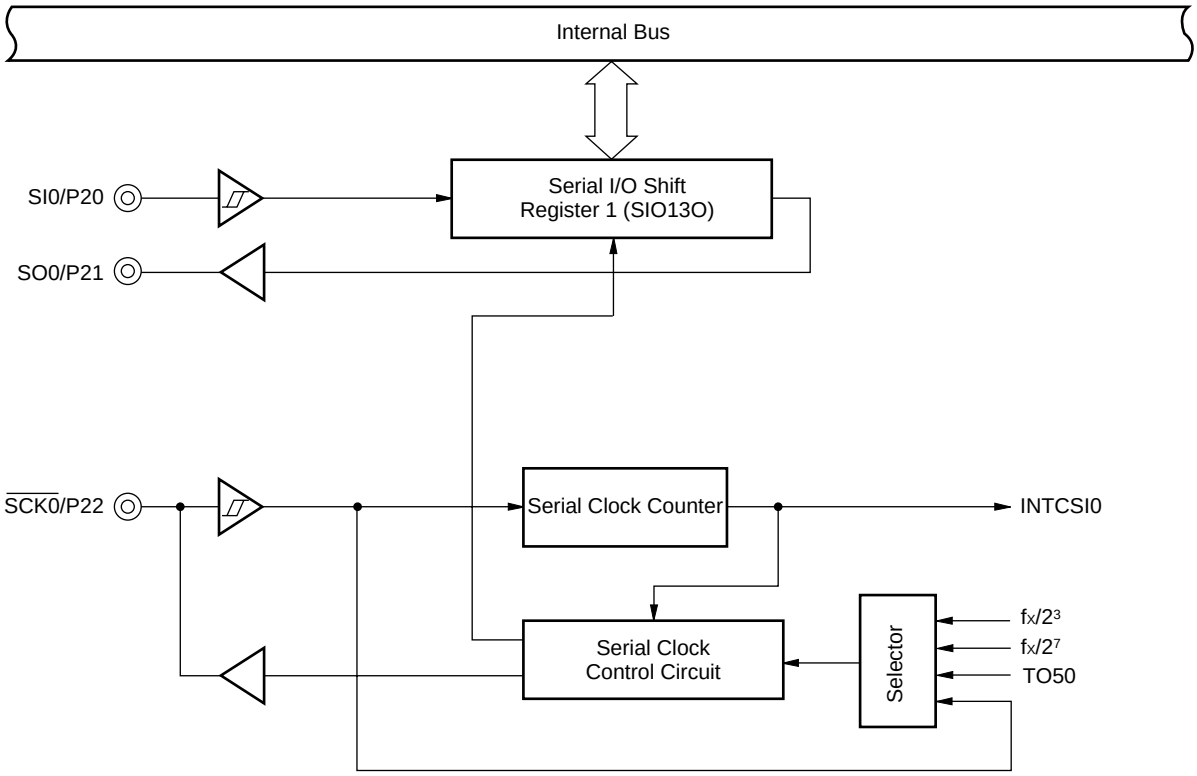


Figure 6-17: Serial Interface Channel 1 Block Diagram

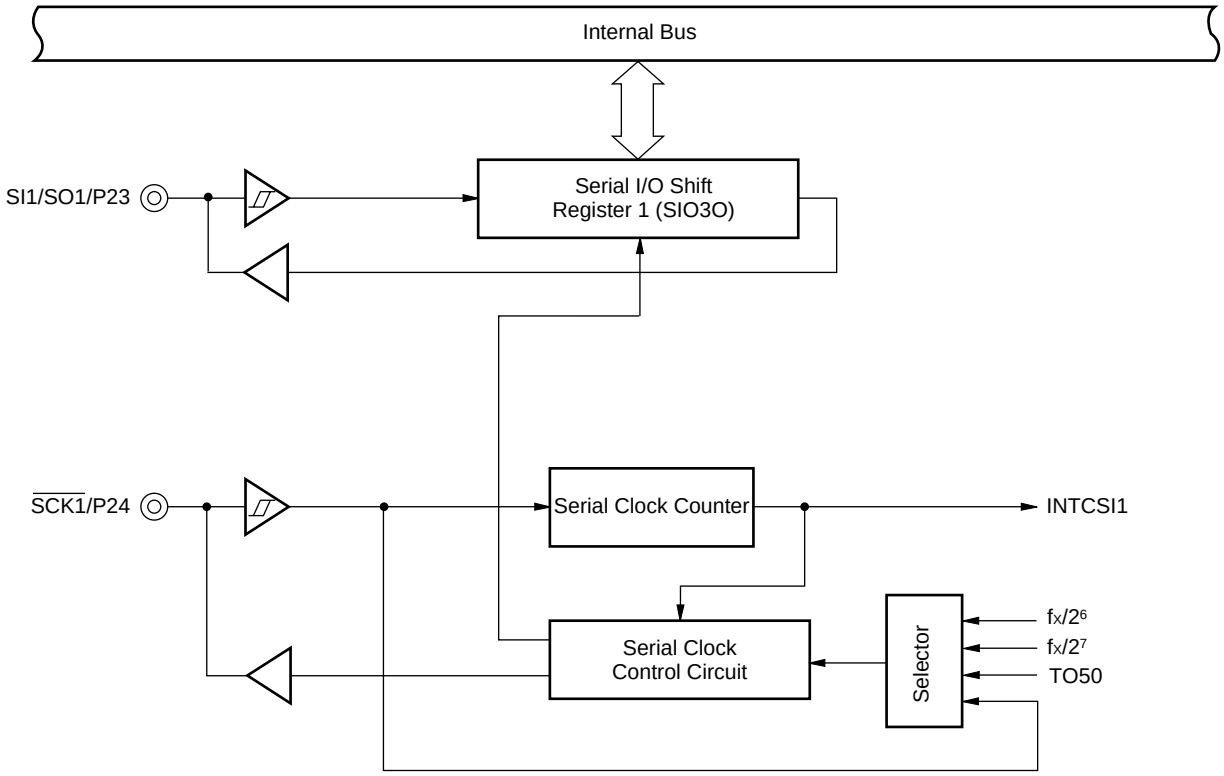
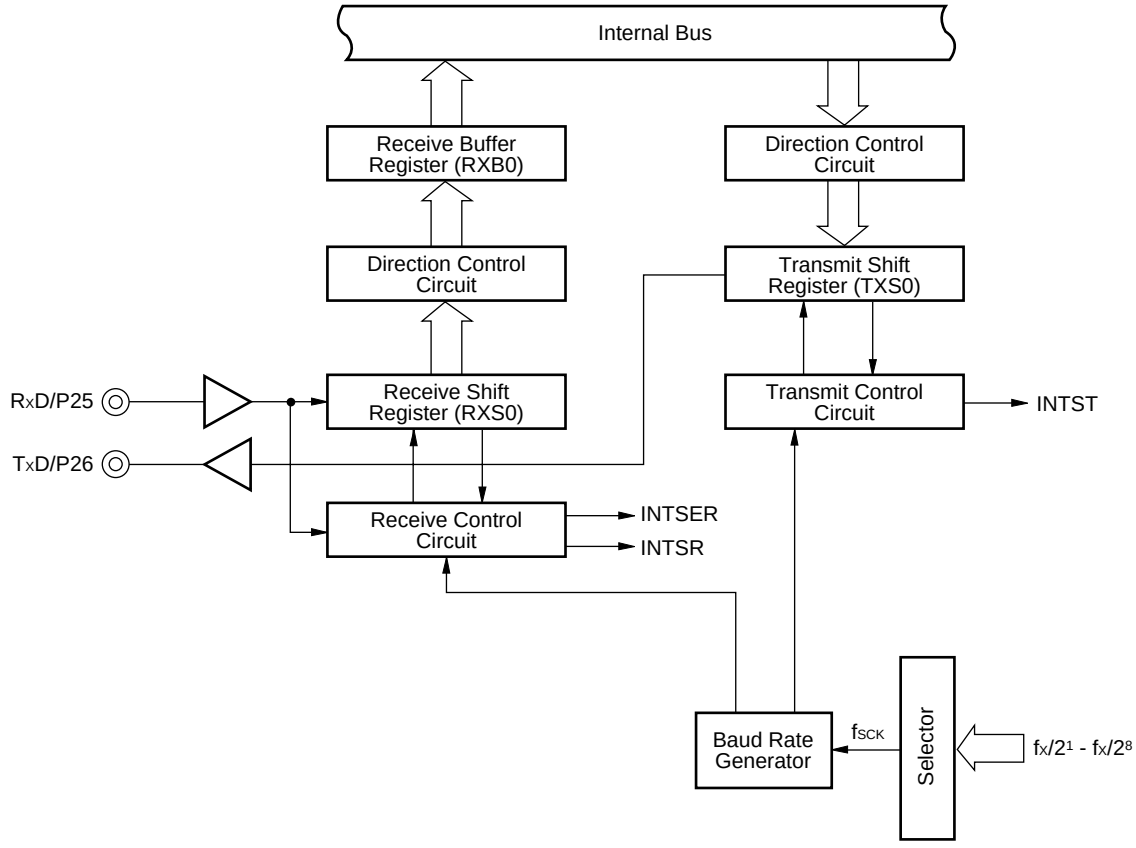


Figure 6-18: Serial Interface UART Block Diagram

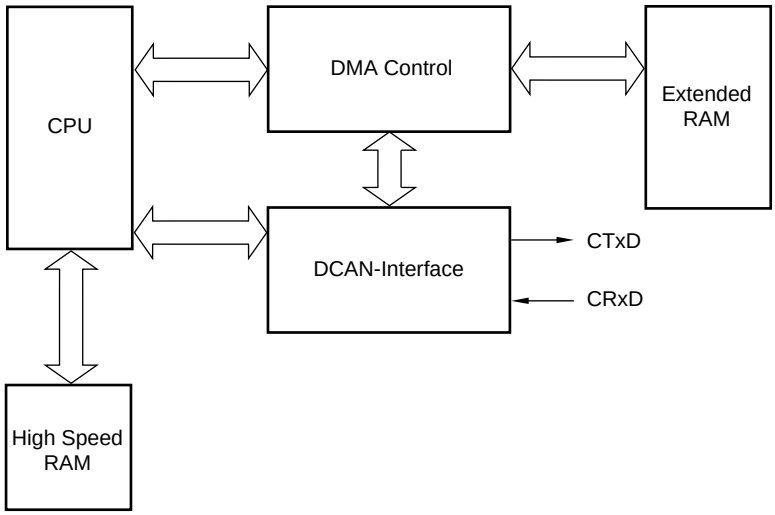


6.11 CAN-Bus Interface

The CAN-Bus Interface has the following functions:

- CAN 2.0 B protocol with active extended frame.
- The maximum Baud rate is 500 kB (@ 8 MHz clock).
- Receice messages will be stored in RAM area depending on message identifier, at which unused bytes can be used by CPU.
- Unique identifier for all 16 messages usable.
- Up to 2 transmit channels with masks.

Figure 6-19: CAN-Bus Interface

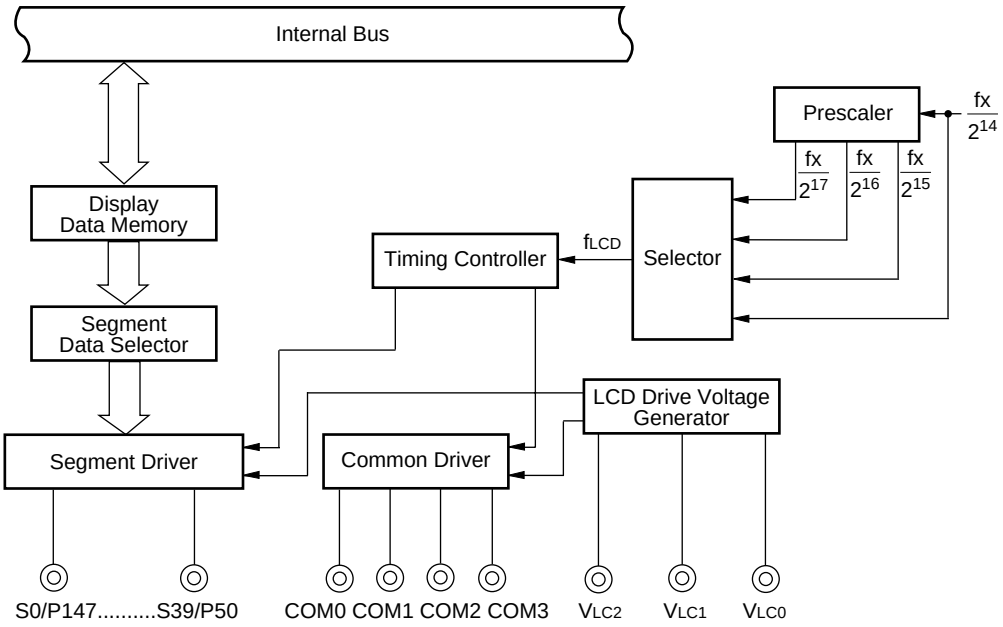


6.12 LCD Controller/Driver

Table 6-4: Display Mode Types and Maximum Number of Display Pixels

Bias Method	Time Multiplexing	Common Signal used	Maximum Number of Display Pixels
1/3	4	COM0 to COM3	160 (40 segments x 4 commons)
1/3	3	COM0 to COM2	120 (40 segments x 3 commons)
1/2	3	COM0 to COM2	120 (40 segments x 3 commons)
1/2	2	COM0 to COM1	80 (40 segments x 2 commons)
static	-	COM0, COM1, COM2, COM3	40 (40 segments x 1 common)

Figure 6-20: LCD Controller/Driver Block Diagram



7. Interrupt Functions and Test Functions

7.1 Interrupt Functions

A total of 29 interrupt functions are provided, divided into the following three types.

- Non-maskable interrupt : 1
- Maskable interrupt : 27
- Software interrupt : 1

Table 7-1: Interrupt Vector Table

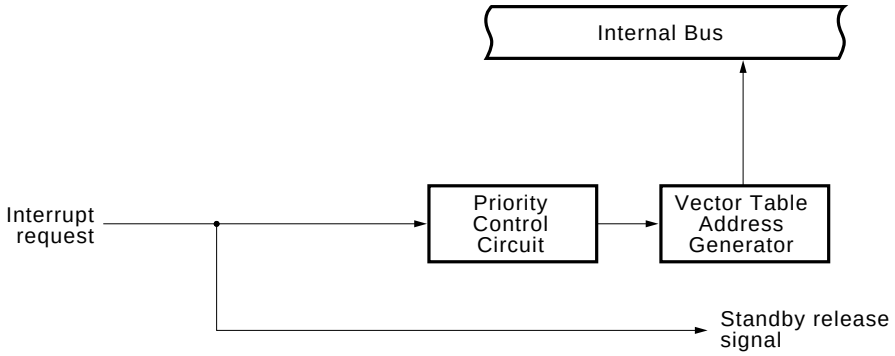
Maskability	Note 1 Interrupt Priority	Interrupt Source		Internal/ Vector	External Address	Note 2 Basic Structure Type
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (When the watchdog timer NMI is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (When the interval timer mode is selected)			(B)
	1	INTAD	End of A/D converter conversion		0006H	
	2	INTOVF	Overflow of 16-bit timer 2		0008H	
	3	INTTM20	Generation of 16-bit timer 2 capture register (CR20) match signal		000AH	
	4	INTTM21	Generation of 16-bit timer 2 capture register (CR21) match signal		000CH	
	5	INTTM22	Generation of 16-bit timer 2 capture register (CR22) match signal		000EH	
	6	INTP0	Pin input edge detection	External	0010H	(C)
	7	INTP1			0012H	
	8	INTP2			0014H	
	9	INTP3			0016H	
	10	INTP4			0018H	
	11	INTCE	CAN Error	Internal	001AH	(B)
	12	INTCR	CAN Receive		001CH	
	13	INTCT0	CAN Transmitbuffer 0		001EH	
	14	INTCT1	CAN Transmitbuffer 1		0020H	
	15	INTCSI0	End of serial interface channel 0 transfer		0022H	
	16	INTCSI1	End of serial interface channel 1 transfer		0024H	
	17	INTSER	Serial interface channel 1 UART reception error generation		0026H	
	18	INTSR	End of serial interface channel 1 UART reception		0028H	
	19	INTST	End of serial interface channel 1 UART transfer		002AH	
	20	INTTM00	Generation of 16-bit timer 0 capture/compare register (CR00) match signal		002CH	
	21	INTTM01	Generation of 16-bit timer 0 capture/compare register (CR01) match signal		002EH	
	22	INTTM50	Generation of 8-bit timer/event counter 50 match signal		0030H	
	23	INTTM51	Generation of 8-bit timer/event counter 51 match signal		0032H	
	24	INTWE	EEPROM write completion interrupt		0034H	
	25	INTWTI	Reference time interval signal from watch timer		0036H	
	26	INTWT	Reference time interval signal from watch timer			
Software	–	BRK_I	BRK instruction execution	Internal	003EH	(D)

Notes: **1.** Default priority is the priority order when several maskable interruptions are generated at the same time. 0 is the highest order and 20 is the lowest order.
2. Basic structure types (A) to (D) correspond to (A) to (D) in Figure 7-1.

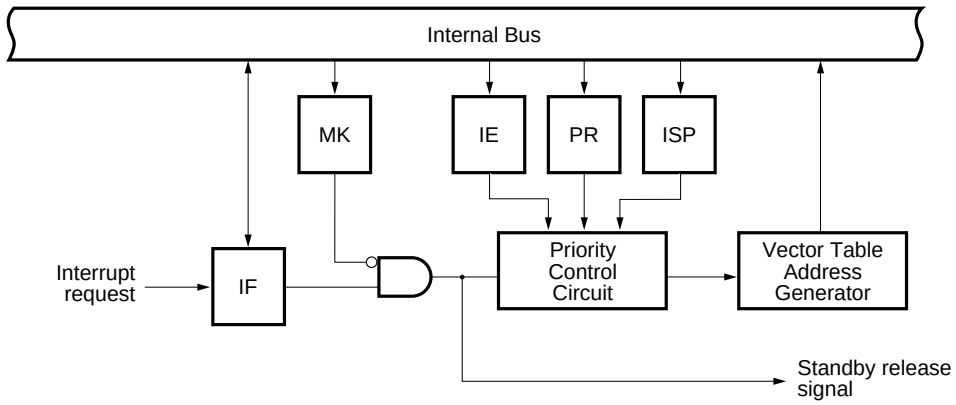
7.2 Interrupts

Figure 7-1: Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt

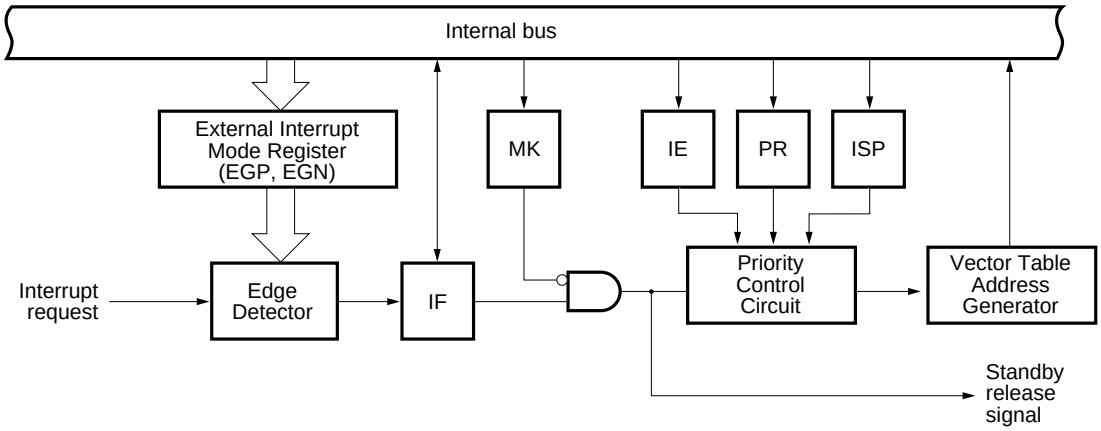
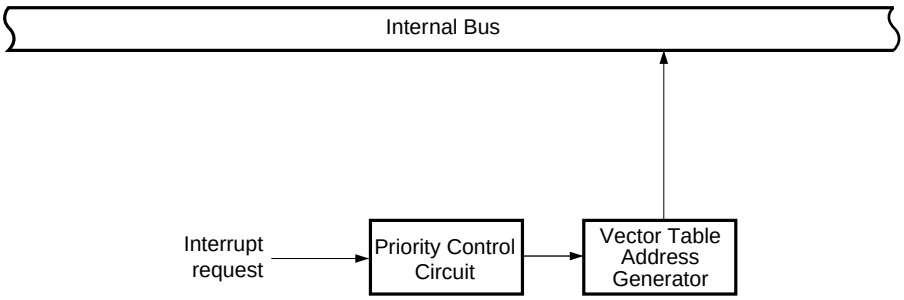


Figure 7-1: Interrupt Function Basic Configuration (2/2)

(D) Software interrupt



8. External Device Expansion Functions

The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. External devices connection uses ports 4 to 6.
The external device expansion function has the following mode:

- Multiplexed bus mode: External devices are connected by using a time-division multiplexed address /data bus. This mode is useful for reducing the number of ports used when external devices are connected.

9. EEPROM Function

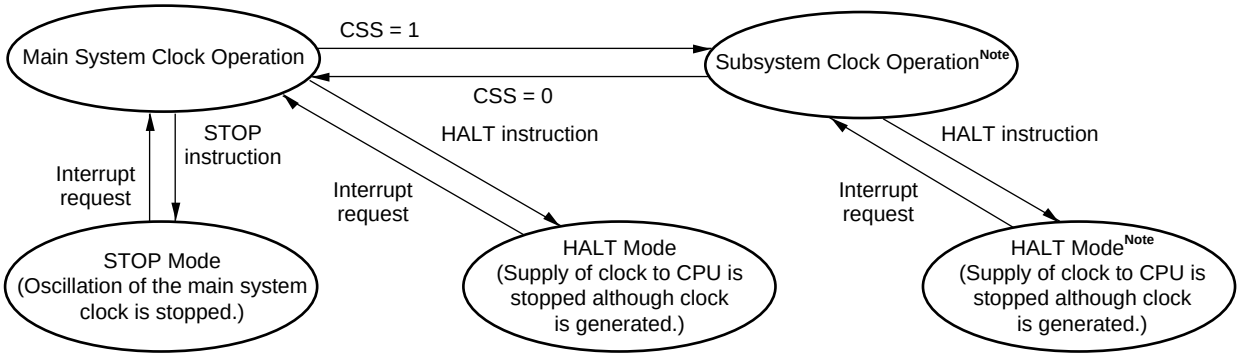
The μPD78F0949 incorporates not only a 2016 byte x 8-bit RAM but also 256 byte x 8-bit EEPROM (Electrically Erasable PROM) as data memory.
EEPROM, unlike static RAM, can retain its contents when the power is turned off. Unlike EPROM, it's contents can electrically be erased without using ultraviolet rays. EEPROM is manipulated by 8-bit memory manipulation instructions.

10. Standby Function

The standby function intends to reduce current consumption. It has the following two modes:

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used for extremely small power consumption.

Figure 10-1: Standby Function



Note: Current consumption is reduced by shutting off the main system clock.
If the CPU is operating on subsystemclock, shut off the main system clock by setting MCC.

Caution: When switching on the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to provide enough time for the generation to be stable with the program first.

11. Reset Function

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

12. Instruction Set

(1) 8-Bit Instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ.

Table 12-1: 8-Bit Instructions

1st Operand \ 2nd Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOVU	ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddrMOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP										DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note: Except r = A

(2) 16-Bit Instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW.

Table 12-2: 16-Bit Instructions

2nd Operand / 1st Operand	#word	AX	rp	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW[Note]						
SP	MOVW	MOVW						

Note: Only when rp = BC, DE, HL

(3) Bit Manipulation Instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR.

Table 12-3: Bit Manipulation Instructions

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ.

Table 12-4: Call Instructions/Branch Instructions

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP.

13. Electrical Specifications

Absolute Maximum Ratings (T_A = 25° C)

Table 13-1: Absolute Maximum Ratings

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			-0.3 to +6.0	V
	V_{PP}			-0.3 to +11.0	
	AV_{DD}			-0.3 to V_{DD} +0.3	
	AV_{SS}			-0.3 to +0.3	
Input voltage	V_I	P00 to P07, P10 to P17, P20 to P26, P30 to P34, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147, X1, X2, CL1, RESET		-0.3 to V_{DD} +0.3	
Output voltage	V_O			-0.3 to V_{DD} +0.3	
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} -0.3 to AV_{DD} +0.3	
High level output current	I_{OH}	1 pin (except P34)		-10	mA
		P34		-30	
		P00 to P07, P20 to P26, P30 to P33, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147, CTxD total		-30	
High level output Current	I_{OL} Note	1 pin (except P34)	Peak value	20	
			Effective value	10	
		P34	Peak value	30	
			Effective value	20	
		P00 to P07, P20 to P26, P30 to P33, P40 to P47, P64, P65, P67, CTxD total	Peak value	50	
		P40 to P47, P64, P65, P67, CTxD total	Effective value	20	
		P50 to P57, P70 to P77, P120 to P127, P130 to P137, P140 to P147 total	Peak value	50	
		P130 to P137, P140 to P147 total	Effective value	20	
Operating temperature	T_{OPT}			-40 to +85	°C
Storage temperature	T_{STG}			-65 to +150	

Note: Effective value should be calculated as follows: [Effective value] = [Peak value] x $\sqrt{duty}$

Caution: **Product quality may suffer if the absolute maximum ratings are exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Capacitance (T_A = 25° C, V_{DD} = V_{SS} = 0 V)

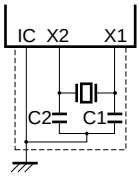
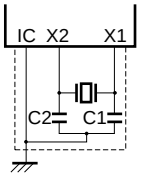
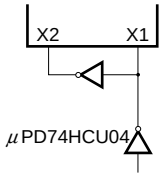
Table 13-2: Capacitance

Parameter	Symbol	Function		Min.	Typ	Max.	Unit
Input capacitance	C_{IN}	f = 1 MHz Other than measured pins: 0 V				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Other than measured pins: 0 V	P00 to P07, P10 to P17, P20 to P26, P30 to P33, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P100 to P103, P120 to P127, P130 to P137, P140 to P147			15	PF
			P34			30	pF

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Main System Clock Oscillation Circuit Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Table 13-3: Main System Clock Oscillation Circuit Characteristics

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) Note 1	V_{DD} = 4.0 to 5.5 V	4.0	8.0	8.38	MHz
		Oscillation stabilization time Note2	After V_{DD} reaches oscillator voltage range MIN. 4.0 V			10	ms
Crystal resonator		Oscillator frequency (fx) Note 1	V_{DD} = 4.0 to 5.5 V	4.0	8.0	8.38	MHz
		Oscillation stabilization time Note2	After V_{DD} reaches oscillator voltage range MIN. 4.0 V			10	ms
External clock		X1 input frequency (fx) Note 1	V_{DD} = 4.0 to 5.5 V	4.0	8.0	8.38	MHz
		X1 input high/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.0 to 5.5 V	55		125	ns

Notes: **1.** Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions: **1. When using the main system clock oscillation circuit, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillation circuit capacitor ground should always be the same as that of VSS.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillation circuit.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Recommended Oscillator Data

Table 13-3a: Main System Clock: Ceramic Resonator **(T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)**

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	
Murata Mfg. Co., Ltd.	CSA4.00MGA	4.0	30	30	0	
	CST4.00MGWA	4.0	30	30	0	built-in capacitor
	CSAC4.00MGCA	4.0	30	30	0	
	CSTCC4.00MGA	4.0	15	15	0	built-in capacitor
	CSA8.00MGA	8.0	30	30	0	
	CST8.00MGWA	8.0	30	30	0	built-in capacitor
	CSAC8.00MGCA	8.0	30	30	0	
	CSTCC8.00MGA	8.0	15	15	0	built-in capacitor
AVX – Kyocera Grp.	PBRC4.00BRVA	4.0	33	33	0	
	PBRC8.00BRVA	8.0	33	33	0	

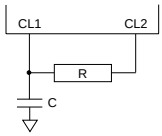
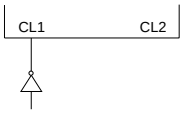
Table 13-3b: Main System Clock: Crystal Resonator **(T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)**

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	
Kinseki	CX-5FW 4MHz	4.0	10	10	8.2	
	HC-49/U-S 8MHz	8.0	8	8	0	
	CX-11F 8MHz	8.0	3.3	3.3	2.4	
NDK	AT-51	8.0	15	15	0	
KDS - Daishinku	AT-49	8.0	27	18	0	
SaRonix	HC49/U13	8.0	27	33	0	
	HC49/L	8.0	27	33	0	
	HC49/S	8.0	27	33	0	

Caution: The oscillator constants and oscillator voltage range indicate conditions for stable oscillation, but do not guarantee oscillation friquency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the oscillator in the actual circuit. Please contact directly the manufacturer of the resonator to be used.

Subystem Clock Oscillation Circuit Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Table 13-4: Subsystem Clock Oscillation Circuit Characteristics

Resonator	Recommended circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
RC osc.		Oscillator frequency (fxt) Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V R = 510 kΩ Note 2 C = 33 pF Note 2	32	40	80	kHz
External clock Note 3		CL1 Input frequency (fxt) Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V	4.0	8.0	8.38	MHz
		CL1 Input high/low level width (t_{XTH}, t_{XTL})	4.0 V ≤ V_{DD} ≤ 5.5 V	55		125	ns

Notes: 1. Only oscillator circuit characteristics are shown. Regarding instruction execute time, please refer to AC characteristics.
2. Reference data.
3. CAN operation with external clock.

Cautions: **1. When using the subsystem clock oscillation circuit, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillation circuit capacitor ground should always be the same as that of VSS.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillation circuit.**

2. The subsystem clock oscillation circuit is designed to be a circuit with a low amplification level, for low power consumption more prone to misoperation due to noise than that of the main system clock. Therefore, when using the subsystem clock, take special cautions for wiring methods.

DC Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Table 13-5: DC Characteristics

Parameter	Symbol	Conditions		MIN.	TYP	MAX	Unit
High-level input voltage	V_{IH1}	P00 to P07, P10 to P17, P20 to P26, P30 to P34, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	RESET, CRxD		0.8 V_{DD}			
	V_{IH4}	X1, X2, CL1		V_{DD} - 0.5			
Low-level input voltage	V_{IL1}	P00 to P07, P10 to P17, P20 to P26, P30 to P34, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147		0		0.3 V_{DD}	
	V_{IL2}	RESET, CRxD				0.2 V_{DD}	
	V_{IL4}	X1, X2, CL1		0		0.4	
High-level output voltage	V_{OH1}	P00 to P07, P10 to P17, P20 to P26, P30 to P34, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147	V_{DD} = 4.5 to 5.5 V I_{OH} = -1 mA	V_{DD} - 1.0			
	V_{OH3}	SGO	V_{DD} = 4.0 to 5.5 V I_{OH} = -20 mA	V_{DD} - 0.7			
Low-level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P26, P30 to P34, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147	V_{DD} = 4.0 to 5.5 V I_{OL} = 1.6 mA			0.4	
	V_{OL3}	SGO	V_{DD} = 4.5 to 5.5 V I_{OL} = 20 mA			0.7	
High-level input leakage current	I_{LIH1}	P00 to P07, P10 to P17, P20 to P26, P30 to P34, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2, CL1				20	
Low-level input leakage current	I_{LIL1}	P00 to P07, P10 to P17, P20 to P26, P30 to P34, P40 to P47, P50 to P57, P64, P65, P67, P70 to P77, P120 to P127, P130 to P137, P140 to P147	V_{IN} = 0 V			-3	
	I_{LIL2}	X1, X2, CL1				-20	
High-level output leakage current	I_{LOH}	V_{OUT} = V_{DD}				3	
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				-3	
Software pull-up resistor	R_2	V_{IN} = 0 V	4.5 V ≤ V_{DD} ≤ 5.5 V	10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

DC Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Mask ROM Version

Table 13-6: DC Characteristics Mask ROM Version

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Power supply [Note] current	I_{DD1}	8.0 MHz crystal oscillation operating mode (PCC = 00H)			9.5	tbd	mA
	I_{DD2}	8.0 MHz crystal oscillation HALT mode			1.2	tbd	mA
	I_{DD3}	RC oscillation operating mode (f_{XT} = 40 kHz)			180	tbd	μA
	I_{DD4}	RC oscillation HALT mode (f_{XT} = 40 kHz)			60	tbd	μA
	I_{DD5}	CL1 = V_{DD} STOP mode			1	tbd	μA

Note: The AV_{DD}/AV_{REF} current, port current (including a current flowing in the on-chip pull-up resistor), the LCD split resistors and the EEPROM access are not included.

Remarks: **1.** f_X: Main system clock oscillator frequency.
2. f_{XT}: Subsystem clock oscillator frequency.

DC Characteristics (T_A = -10 to +85° C, V_{DD} = 4.0 to 5.5 V)

LCD C/D Static Method

Table 13-7: DC Characteristics Static Method

Parameter	Symbol	Test Conditions		MIN	TYP	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD split resistor	R_{LCD}			5	15	45	kΩ
LCD output voltage deviation [Note] (common)	V_{ODC}	I_O = ± 5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD}	0		±0.2	V
LCD output voltage deviation [Note] (segment)	V_{ODS}	I_O = ± 1 μA		0		±0.2	

Note: The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDN}; n = 0, 1, 2).

LCD C/D 1/2 Bias Method

Table 13-8: DC Characteristics 1/2 Bias Method

Parameter	Symbol	Test Conditions		MIN	TYP	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD split resistor	R_{LCD}			5	15	45	kΩ
LCD output voltage deviation Note (common)	V_{ODC}	I_O = ± 5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} $V_{LCD}0 = V_{LCD}$ $V_{LCD}1 = V_{LCD}$ x 1/2 $V_{LCD}2 = V_{LCD}$ x 1/2	0		±0.2	V
LCD output voltage deviation Note (segment)	V_{ODS}	I_O = ± 1 μA		0		±0.2	

Note: The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDN}; n = 0, 1, 2).

LCD C/D 1/3 Bias Method

Table 13-9: DC Characteristics 1/3 Bias Method

Parameter	Symbol	Test Conditions		MIN	TYP	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD split resistor	R_{LCD}			5	15	45	kΩ
LCD output voltage deviation Note (common)	V_{ODC}	I_O = ± 5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} $V_{LCD}0 = V_{LCD}$ $V_{LCD}1 = V_{LCD}$ x 2/3 $V_{LCD}2 = V_{LCD}$ x 1/3	0		±0.2	V
LCD output voltage deviation Note (segment)	V_{ODS}	I_O = ± 1 μA		0		±0.2	

Note: The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDN}; n = 0, 1, 2).

AC Characteristics

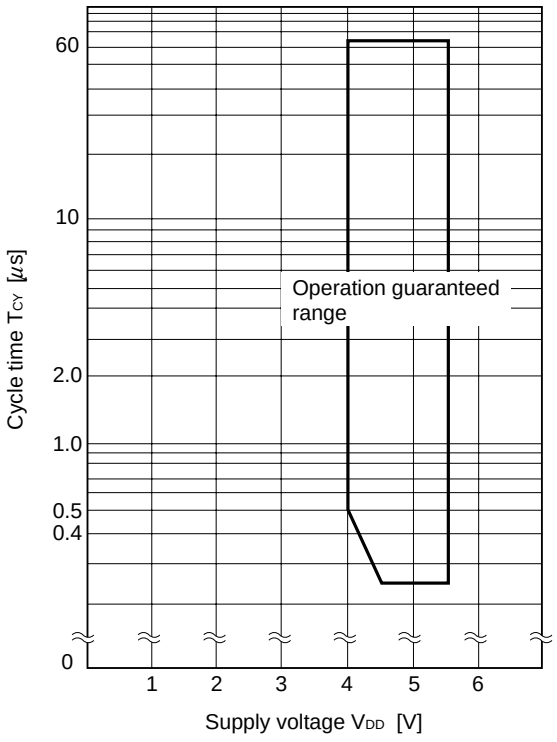
(1) Basic Operation (T_A = -40 to +85° C, V_{DD} = 4.0. to 5.5 V)

Table 13-10: AC Characteristics Basic Operation

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time Note1	T_{CY}	4.0 V ≤ V_{DD} ≤ 5.5 V fx=8.00 MHz	0.25		125	µs
TI50, TI51 input frequency	f_{TI5}		0		4	MHz
TI50, TI51 input high/low level width	t_{TIH5}, t_{TIL5}		100			ns
TI20, TI21, TI22 input high/low level width	t_{TIH2}, t_{TIL2}		3/ f_{SMP2} Note2			µs
TI00, TI01 input high/low level width	T_{CAPH}, T_{CAPL}		3/ f_{SMP0} Note3			µs
Interrupt input high/low level width	T_{INTH}, T_{INTL}	INTP0-4	1			µs
$\overline{\text{RESET}}$ low level width	t_{RSL}		10			µs

Notes:
1. The cycle time equals to the minimum instruction exection time.
   Example: 1 NOP instruction corresponds to 2 clock cycles (f_{CPU}) selected by the processor clock control register (PCC).
2. f_{SMP2} (sampling clock) = fx/4, fx/8, fx/32, fx/128
3. f_{SMP0} (sampling clock) = fx/2, fx/16, fx/128

Figure 13-1: T_{CY} vs V_{DD} (At fx = fx/2 main system clock operation)



(2) Read/Write Operation (T_A = -40 to +85° C, V_{DD} = 4.0. to 5.5 V)

Table 13-11: Read/Write Operation

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.3 t_{CY}		ns
Address setup time	t_{ADS}		20		
Address hold time	t_{ADH}		6		
Data input time from address	t_{ADD1}			2 t_{CY} - 54	
	t_{ADD2}			3 t_{CY} - 60	
Data input time from $\overline{RD}$ ↓	t_{RDD1}			2 t_{CY} - 87	
	t_{RDD2}			3 t_{CY} - 93	
Address output time from $\overline{RD}$ ↓	t_{RDAD}		0	100	
Read data hold time	t_{RDH}		0		
$\overline{RD}$ low-level width	t_{RDL1}		1.5 t_{CY} - 33		
	t_{RDL2}		2.5t_{CY} - 33		
Write data setup time	t_{WDS}		60		
Write data hold time	t_{WDH}		6		
WR low-level width	t_{WRL}		1.5 t_{CY} - 15		
$\overline{RD}$ ↓ delay time from ASTB ↓	t_{ASTRD}		6		
$\overline{WR}$ ↓ delay time from ASTB ↓	t_{ASTWR}		2 t_{CY} - 15		
ASTB ↑ delay time from $\overline{RD}$ ↑ at external fetch	t_{RDAST}		0.8 t_{CY} - 15	1.2 t_{CY}	
Address hold time from $\overline{RD}$ ↑ at external fetch	t_{RDADH}		0.8 t_{CY} - 15	1.2 t_{CY} + 30	
Write data output time from $\overline{RD}$ ↑	t_{RDWD}		40		
Write data output time from $\overline{WR}$ ↑	t_{WRDWD}		10	60	
Address hold time from $\overline{WR}$ ↑	t_{WRADH}		0.8 t_{CY} - 15	1.2 t_{CY} + 30	

Remarks: **1.** $t_{CY} = T_{CY}/4$

2. C_L = 100 pF (C_L are capacitances of AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, ASTB pin)

(3) Serial Interface (T_A = -40 to +85° C, V_{DD} = 4.0. to 5.5 V)

Table 13-12: 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK0}$ cycle time	T_{KCY1}		1000		ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 - 50		
SI0 setup time (to $\overline{SCK0}$) ↑	t_{SIK1}		100		
SI0 hold time (from $\overline{SCK0}$) ↑	t_{KSI1}		400		
SO0 output delay time (from $\overline{SCK0}$) ↓	t_{KSO1}	C = 100 pF [Note]		300	

Note: C is the load capacitance of SO0, $\overline{SCK0}$ output line

Table 13-13: 3-wire serial I/O mode ($\overline{SCK0}$... External clock output)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KSO1}		800		ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}		400		
SI0 setup time (to $\overline{SCK0}$) ↑	t_{SIK1}		100		
SI0 hold time (from $\overline{SCK0}$) ↑	t_{KSI1}		400		
SO0 output delay time (from $\overline{SCK0}$) ↓	t_{KSO1}	C = 100 pF [Note]		300	

Note: C is the load capacitance of SO0, $\overline{SCK0}$ output line.

Table 13-14: 2-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP	MAX	Unit
$\overline{SCK1}$ cycle time	t_{KCY5}	R = 1k Ω C = 100 pF Note		2000			ns
$\overline{SCK1}$ high -level width	t_{KH5}			t_{KCY5}/2 - 160			
$\overline{SCK1}$ low-level width	t_{KL5}			t_{KCY5}/2 - 160			
SI1 setup time (to $\overline{SCK1}$) ↑	t_{SIK5}			300			
SI1 hold time (from $\overline{SCK1}$) ↑	t_{KSI5}			600			
SO1 output delay time (from $\overline{SCK1}$) ↓	t_{KSO5}					300	

Note: R and C are the load resistance and load capacitance of the SI1/SO1 and $\overline{SCK1}$ output line.

Table 13-15: 2-wire serial I/O mode ($\overline{SCK1}$... External clock output)

Parameter	Symbol	Conditions		MIN.	TYP	MAX	Unit
$\overline{SCK1}$ cycle time	t_{KCY5}	R = 1k Ω C = 100 pF Note		2000			ns
$\overline{SCK1}$ high -level width	t_{KH5}			840			
$\overline{SCK1}$ low-level width	t_{KL5}			840			
SI1, SO1 setup time (to $\overline{SCK1}$) ↑	t_{SIK5}			300			
SI1, SO1 hold time (from $\overline{SCK1}$) ↑	t_{KSI5}			600			
SI1, SO1 output delay time (from $\overline{SCK1}$) ↓	t_{KSO5}					300	

Note: R and C are the load resistance and load capacitance of the SI1/SO1 and $\overline{SCK1}$ output line.

Table 13-16: UART Mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP	MAX.	Unit
Transfer rate					125	bps

Figure 13-2: AC Timing Test Points (excluding X1, CL1 inputs)

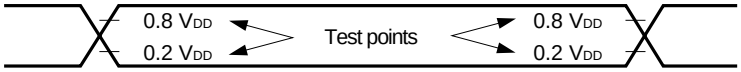


Figure 13-3: Clock Timing

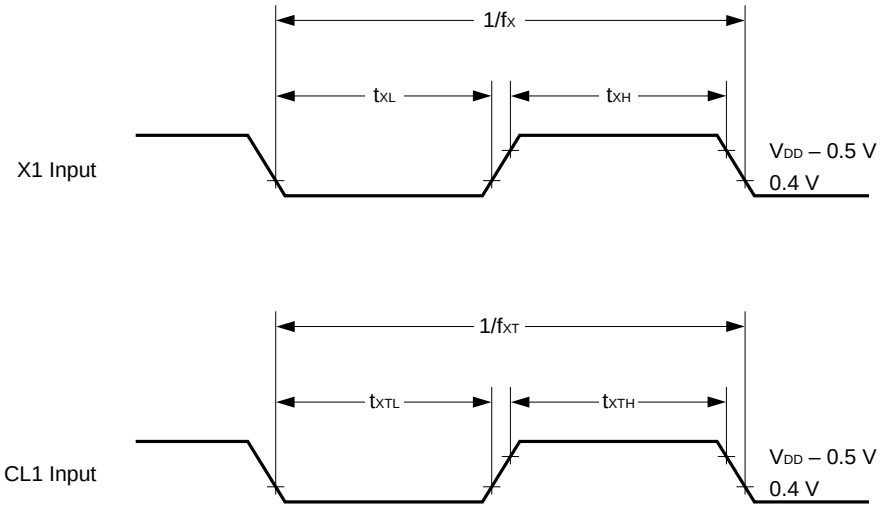
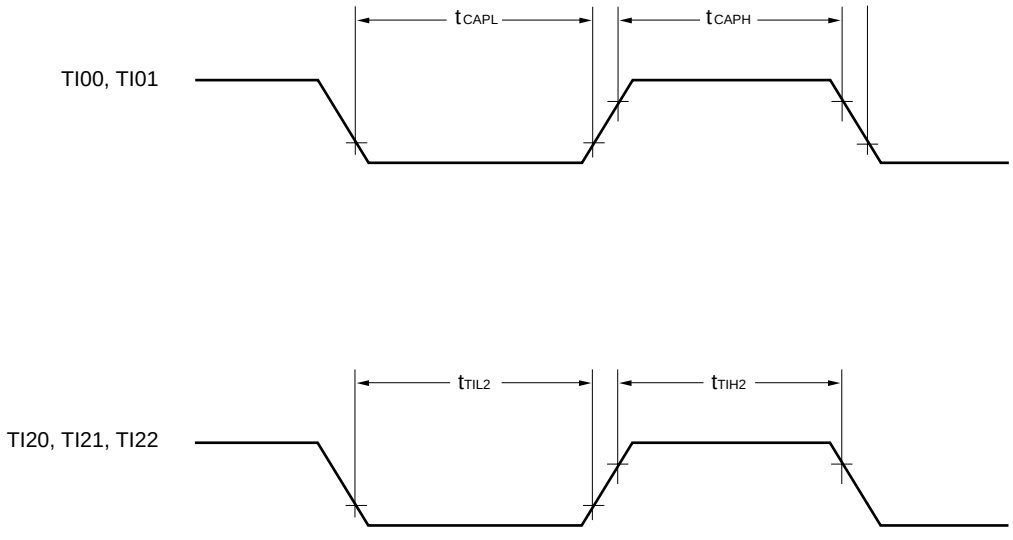


Figure 13-4: TI Timing



Read/Write Operation

Figure 13-5: External fetch (no wait)

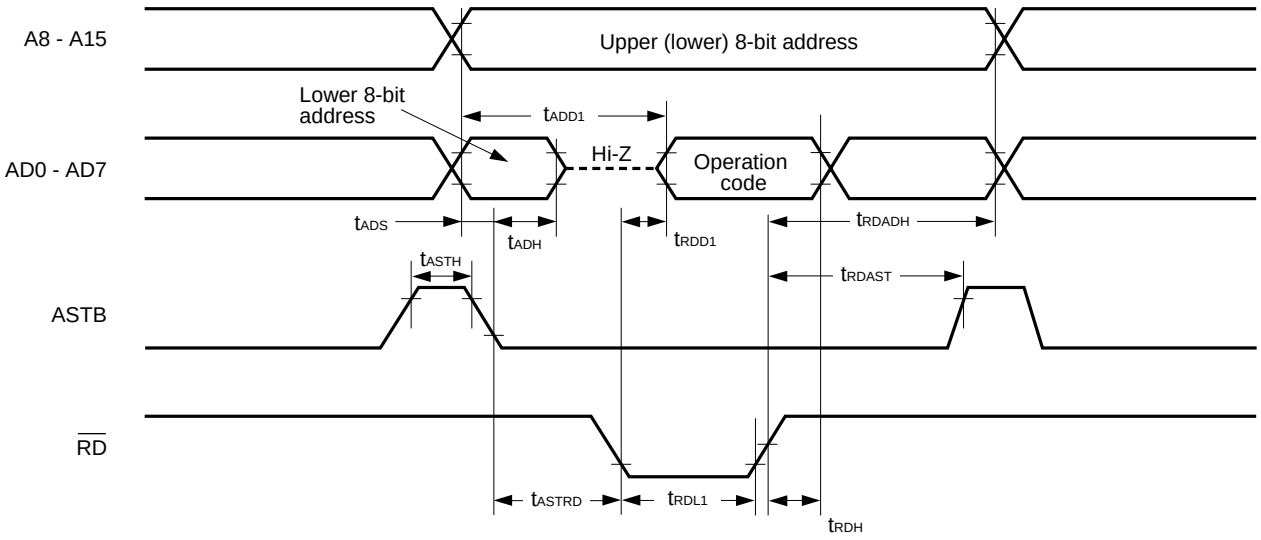


Figure 13-6: External fetch (wait insertion)

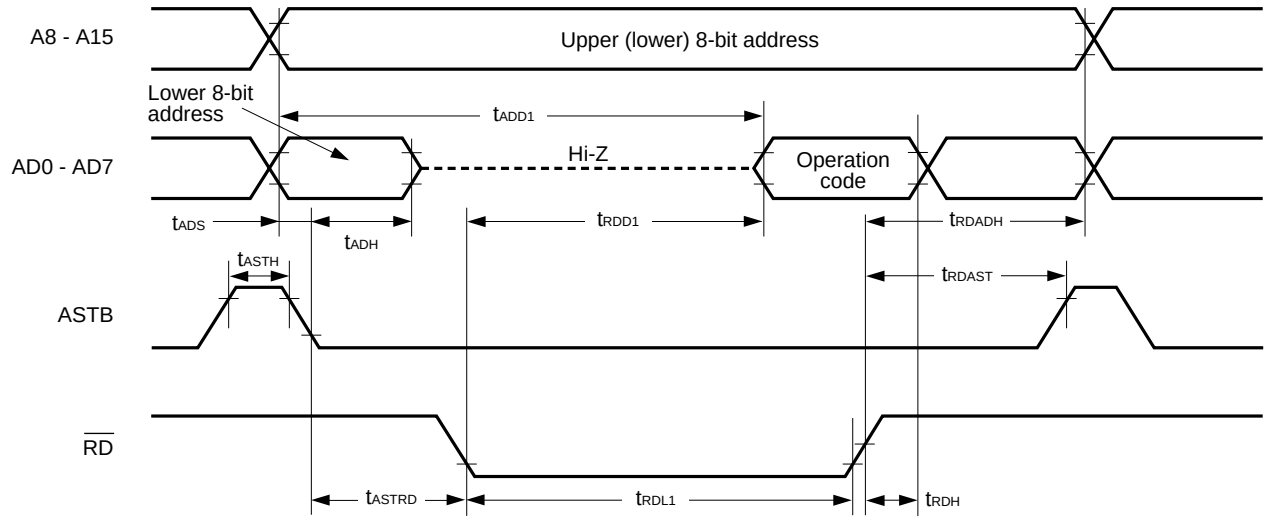


Figure 13-7: External data access (no wait)

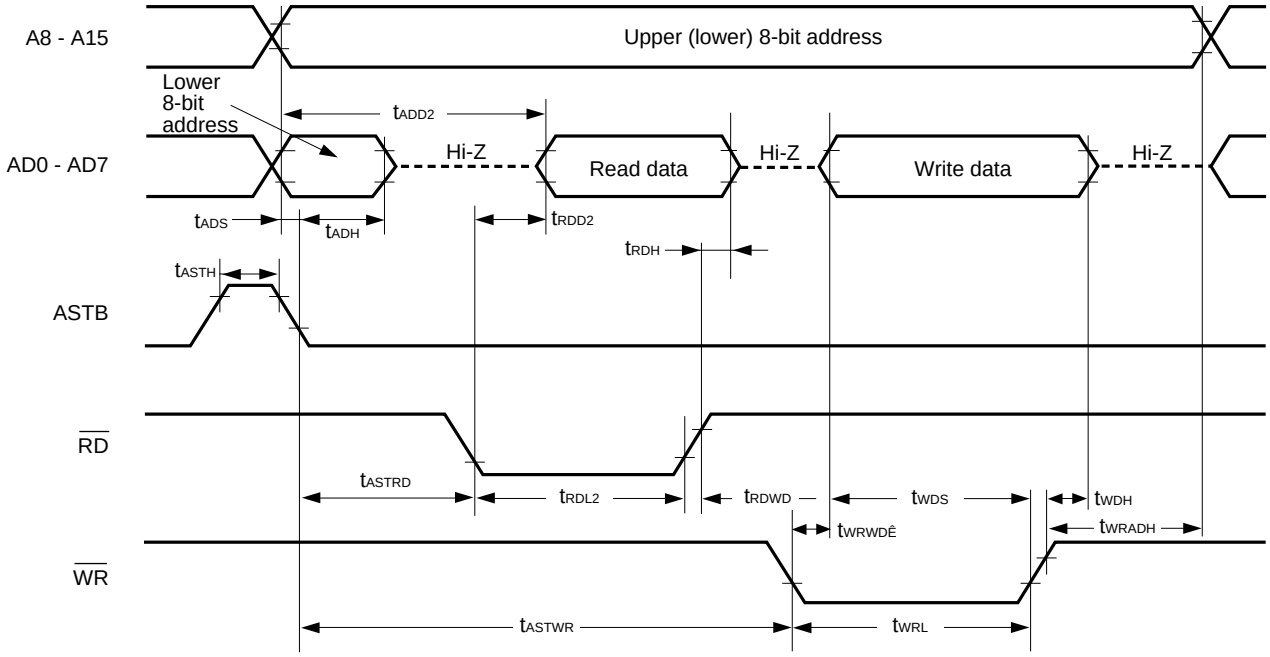
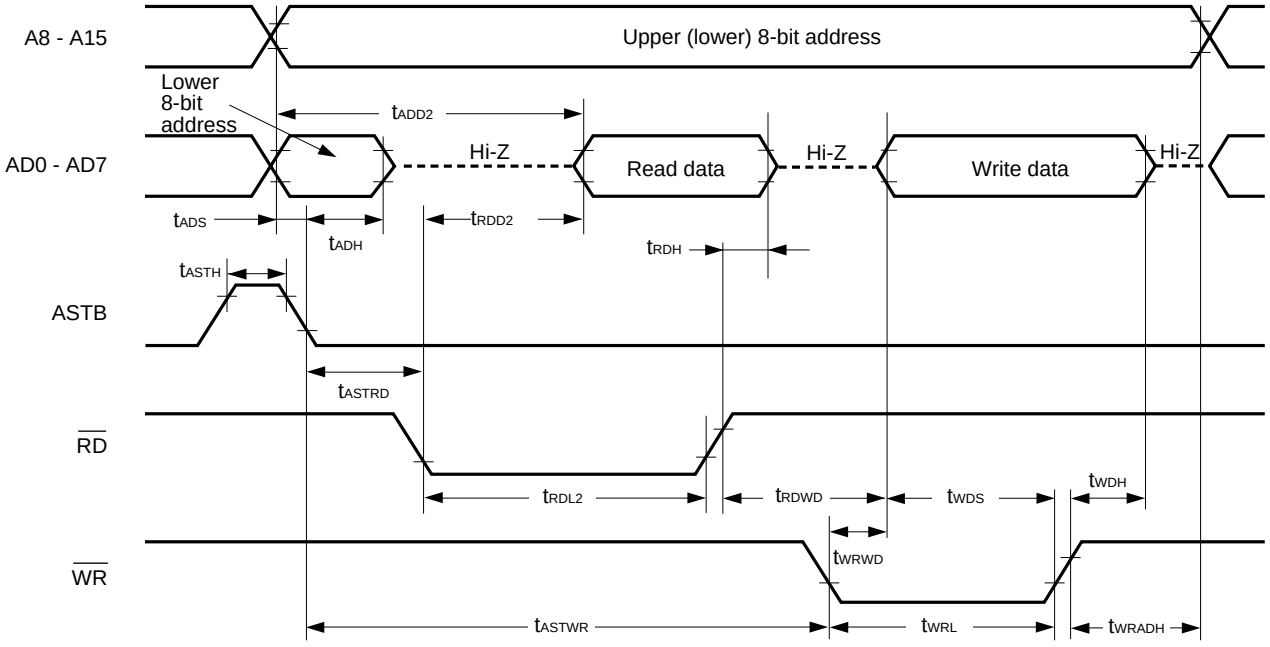
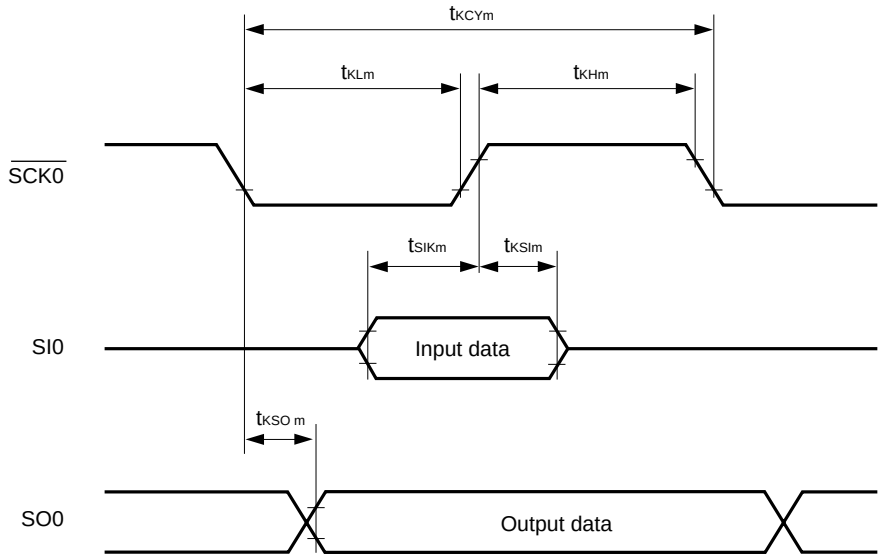


Figure 13-8: External data access (wait insertion)



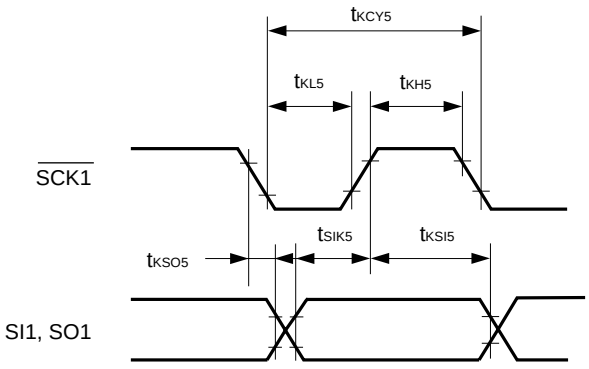
Serial Transfer Timing

Figure 13-9: 3-wire serial I/O mode



Remark: m=1

Figure 13-10: 2-wire serial I/O mode



A/D Converter Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} =0 V, fx = 8 MHz)

Table 13-17: A/D Converter Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error					± 0.6	%
Conversion time	t_{CONV}		15		40	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Reference voltage	AV_{DD} /AV_{REF}		4.0		V_{DD}	
Resistor string	R_{AIREF}	CS-bit = 1		21		kΩ

Note: Overall error excluding quantization error (± 1/2 LSB). It is indicated as a ratio to the full-scale value.

Remark: fx: Main system clock oscillation frequency

EEPROM Characteristics (T_A = -40 to +85° C, fx = 8.0 MHz)

Table 13-18: EEPROM Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Voltage range for R/W	V_{EERW}		4.0		5.5	V
Write time	t_{EEW}		3		6	ms
Erase/Write cycles	N_{EEWT}		100000			cycle
Additional current when EEPROM is erased/written	I_{EE-W}	V_{DD} = 5.0 V		1	tbd	mA

Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85° C)

Table 13-19: Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 4.0 V		1	30	μA
Release signal set time	t_{SREL}		0			μS
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt		**Note**		

Note: In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of 2^{12}/fx and 2^{14}/fx to 2^{17}/fx is possible

Remark: fx: Main system clock oscillation frequency

Figure 13-11: Data Retention Timing (STOP mode release by RESET)

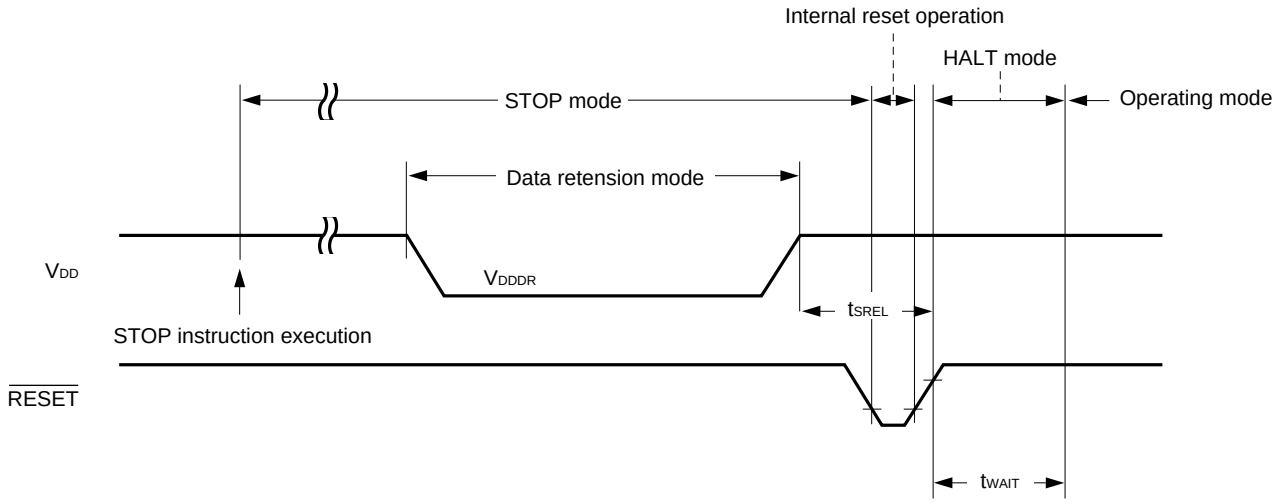


Figure 13-12: Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

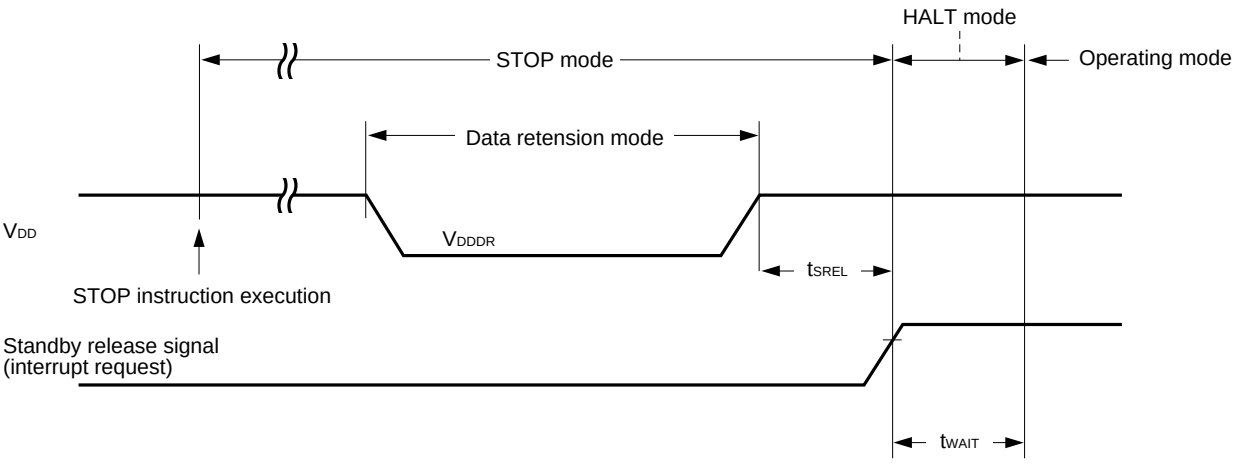


Figure 13-13: Interrupt Input Timing

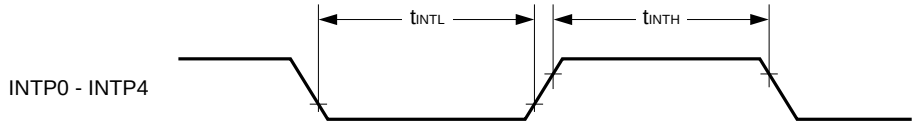
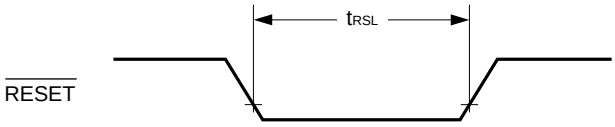
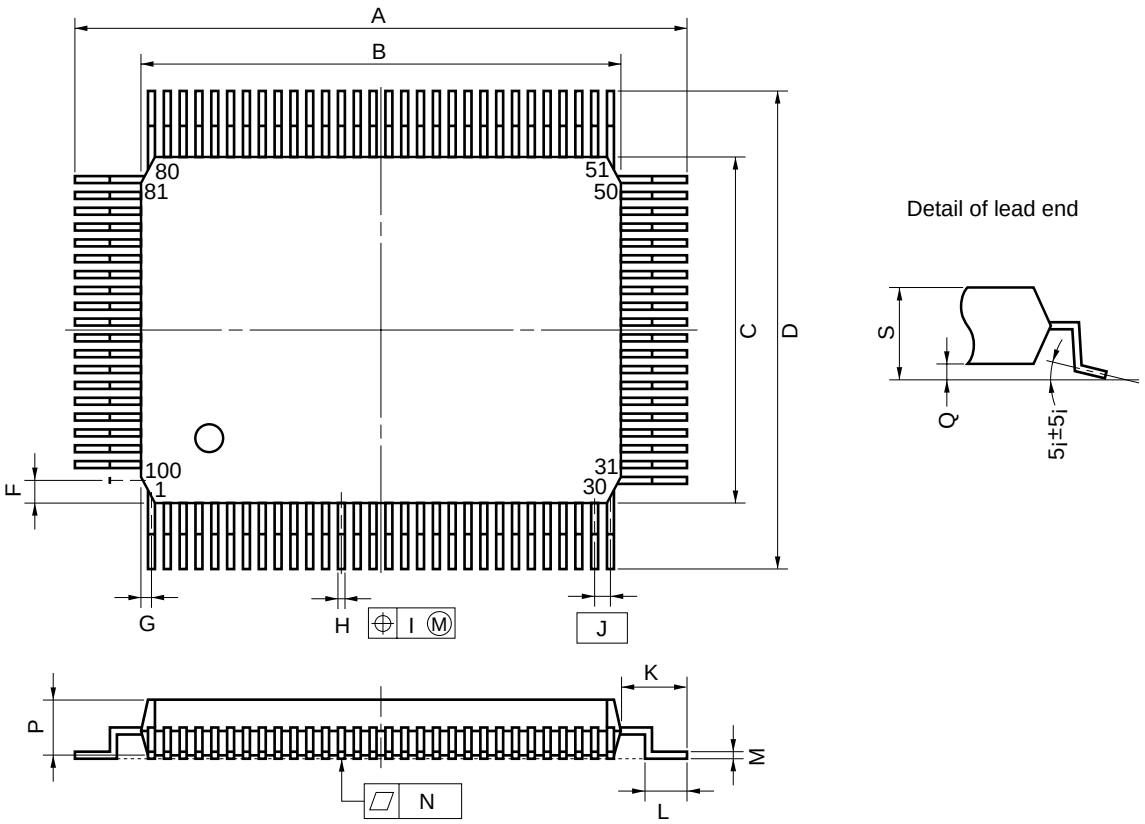


Figure 13-14: $\overline{\text{RESET}}$ Input Timing



14. Package Drawing

Figure 14-1: Package Drawing



P100GF-65-3BA1-2

Note:
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

Item	Millimeters	Inches
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark: The shape and material of the ES product is the same as the mass produced product.

15. Recommended Soldering Conditions

The µPD78F0949 should be soldered and mounted under the conditions in the table below. For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (IEI-1207)**.

For soldering methods and conditions other than those recommended below, consult our sales personnel.

µPD78F0949GF-xxx-3BA : 100-pin plastic QFP (14 x 20 mm)

Table 15-1: Surface Mounting Type Soldering Conditions

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235° C, Duration: 30 sec. max. (at 210° C or above). Number of times: twice max. <Precautions> (1) The second reflow schold be started after the first reflow device temperature has retumed to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215° C, Duration: 40 sec. max. (at 210° C or above). Number of times: twice max. <Precautions> (3) The second reflow schold be started after the first reflow device temperature has retumed to the ordinary state. (4) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Wave soldering	Soldering bath temperature: 260° C max. Duration: 10 sec. max. Number of times: once, Preheating temperature: 120° C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin temperature: 300° C max. Duration: 3 sec. max. (per device side).	-

Caution: Use of more than one soldering method should be avoided (exept in the case of pin part heating).

Appendix A. Development Tools

The following tools are available for system development using the μPD780948.

Language Processing Software

RA78K/0 Notes 1, 2, 3	Assembler package used in common for the 78K/0 series
CC78K/0 Notes 1, 2, 3	C compiler package used in common for the 78K/0 series
DF780949	Device file used for the μPD780949 subseries
CC78K/0-L Notes 1, 2, 3	C compiler library source file used in common for the 78K/0 series

PROM Writing Tools

Flashpro	Dedicated flash writer for micro controllers with on-chip flash memory
FA-100GF	Programmer adapter connected to the Flash-Pro

Debugging Tools

IE-78001-R-A	In-circuit emulator used in common for the 78K/0 series
IE-78001-R-BK	Break board used in common for the 78K/0 series
IE-70000-PC-IF-C	This adapter is required when using an IBM PC/AT or compatible as host machine
IE-780948-SL-EM1	Emulation board and probe board for the μPD780949 subseries
IE-780948-SL-EM4	
EP-100GF-SL	Emulation probe used in common for the μPD780949 subseries
SM78K0	System simulator used in common for the 78K/0 series
ID78K/0	Integrated debugger for the IE-78001-R-A
DF780949	Device file used for the μPD780949 subseries

Real-Time OS

RX78K/0 Notes 1, 2, 3	Real-time OS used for the 78K/0 series
MX78K0 Notes 1, 2, 3	OS used for the 78K/0 series

Fuzzy Interference Development Support System

FE9000 Note 1 /FE9200 Note 5	Fuzzy knowledge data creating tool
FT9080 Note 1 /FT9085 Note 2	Translator
FI78K0 Note 1, 2	Fuzzy interference module
FD78K0 Note 1, 2	Fuzzy interference debugger

Notes: **1.** Based on PC-9800 series (MS-DOS™)
2. Based on IBM PC/AT™ (PC DOS™)
3. Based on HP9000 series 300™, HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™), and EWS-4800 series (EWS-UX/V)
4. Based on PC-9800 series (MS-DOS + Windows™)
5. Based on IBM PC/AT (PC DOS + Windows)

Appendix B. Related Documents

Documents Related to Devices

Document	Document No.	
	Japanese	English
78K0 Series User's Manual-Instruction	IEU-849	IEU-1372
78K0 Series Instruction Table	IEM-5522	—
78K0 Series Instruction Set	IEM-5521	—
78K0 Series Application Note-Fundamental (III)	IEA-767	To be prepared

Documents on Development Tools (User's Manuals)

Document		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Reprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler Application Note	Programming Know-how	EEU-618	To be prepared
CC78K Series Library Source File		EEU-777	—
IE78001-R-A		EEU-810	U10057
IE-78001-R-BK		EEU-867	To be prepared
IE-780948-SL-EM1		EEU-978	U12412
IE-780948-SL-EM4		—	U12412
EP-100GF-SL		EEU-934	EEU-1522
SM78K0 System Simulator	Reference	—	U10181
IBM PC/AT (PC DOS) Base	External Port Specification	—	U10092
ID78K0 Integrated Debugger	Reference	—	U11539
IBM PC/AT (PC DOS) Base	Guide	—	U11649

Caution: The above documents are subject to change without notice. Be sure to use the latest documents for design or for any other similar purpose.

Documents on Embeded Software (User's Manuals)

Document		Document No.	
		Japanese	English
78K0 Series Real-time OS	Basic	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
78K0 Series OS MX78K0	Fundamental	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEA-862	EEU-1444
78K0 Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K0 Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Device Quality Assurance Guide	MEI-603	MEI-1202
Microcontroller-Related Product Guide - Third Party Products -	MEI-604	—

Caution: The above documents are subject to change without notice. Be sure to use the latest documents for design or for any other similar purpose.

Notes for CMOS Devices

① Precaution against ESD for Semiconductors

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② Handling of unused input pins for CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ Status before initialization of MOS devices

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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