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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# MOS INTEGRATED CIRCUIT

## $\mu$ PD78F0703AY, 78F0703AY(A)

### 8-BIT SINGLE-CHIP MICROCONTROLLER

The  $\mu$ PD78F0703AY is a product of the  $\mu$ PD780703AY Subseries in the 78K/0 Series.

The  $\mu$ PD78F0703AY has flash memory in place of the internal ROM of the  $\mu$ PD780703AY.

The flash memory incorporated enables program writing or erasing with the microcontroller mounted on the target board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

$\mu$ PD780703Y Subseries User's Manual: U15568E

78K/0 Series User's Manual Instruction: U12326E

#### FEATURES

- DCAN (Direct Storage Controller Area Network) controller
- Pin compatible with mask ROM versions (except  $V_{PP}$  pin)
- Flash memory: 59.5 KB
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 2048 bytes
- Buffer RAM for DCAN: 288 bytes
- Operable within the same supply voltage range as that of the mask ROM version ( $V_{DD} = 3.5$  to  $5.5$  V)

**Remark** For differences between the flash memory versions and mask ROM version, refer to **1. DIFFERENCES BETWEEN  $\mu$ PD78F0703AY AND MASK ROM VERSION.**

#### APPLICATIONS

Car audio systems, body control, etc.

#### ORDERING INFORMATION

Part Number	Package	Quality Grade
$\mu$ PD78F0703AYGC-8BT	80-pin plastic QFP (14 × 14)	Standard
$\mu$ PD78F0703AYGC(A)-8BT	80-pin plastic QFP (14 × 14)	Special

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

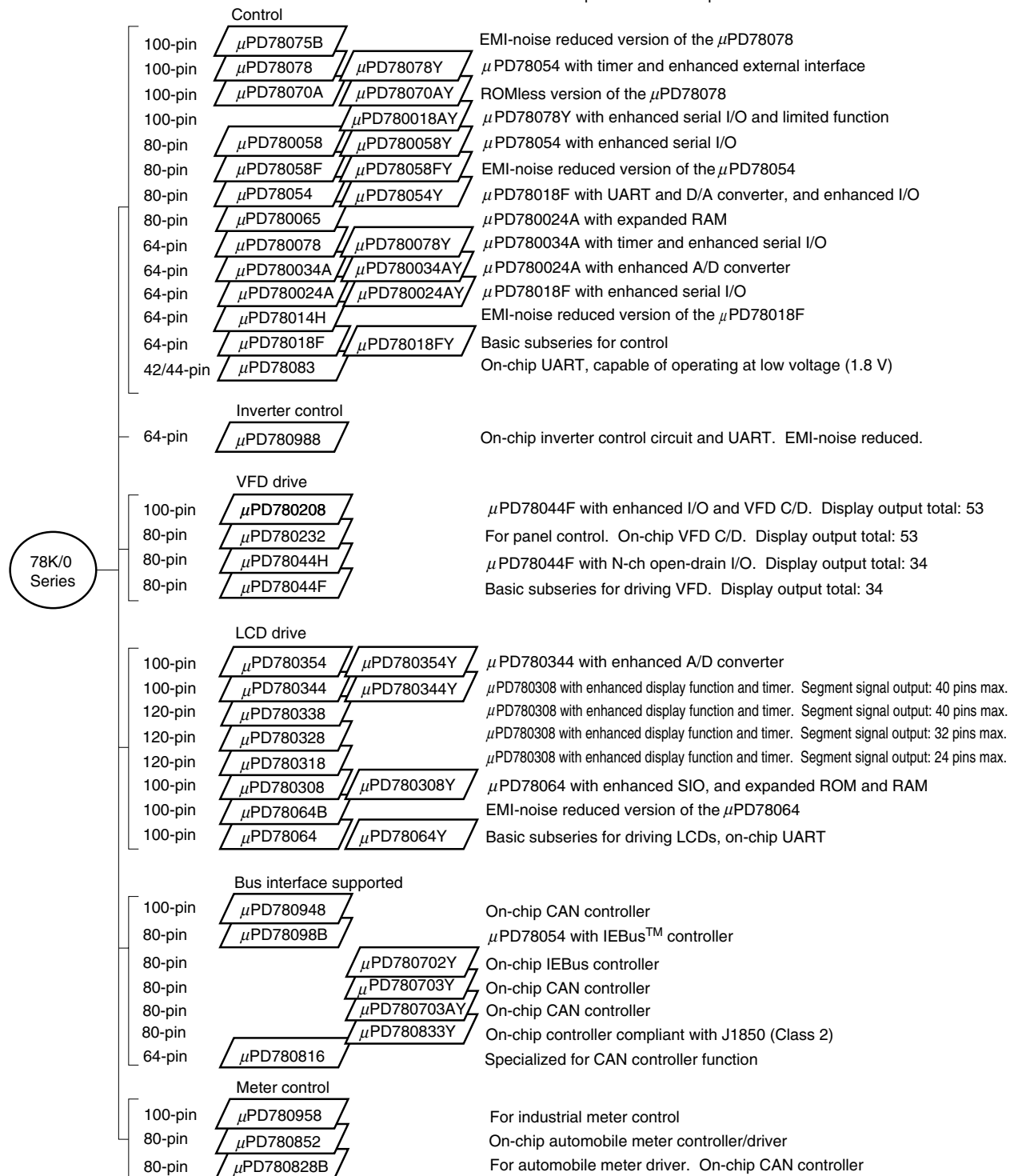
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★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Y subseries products are compatible with I<sup>2</sup>C bus.



**Remark** VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

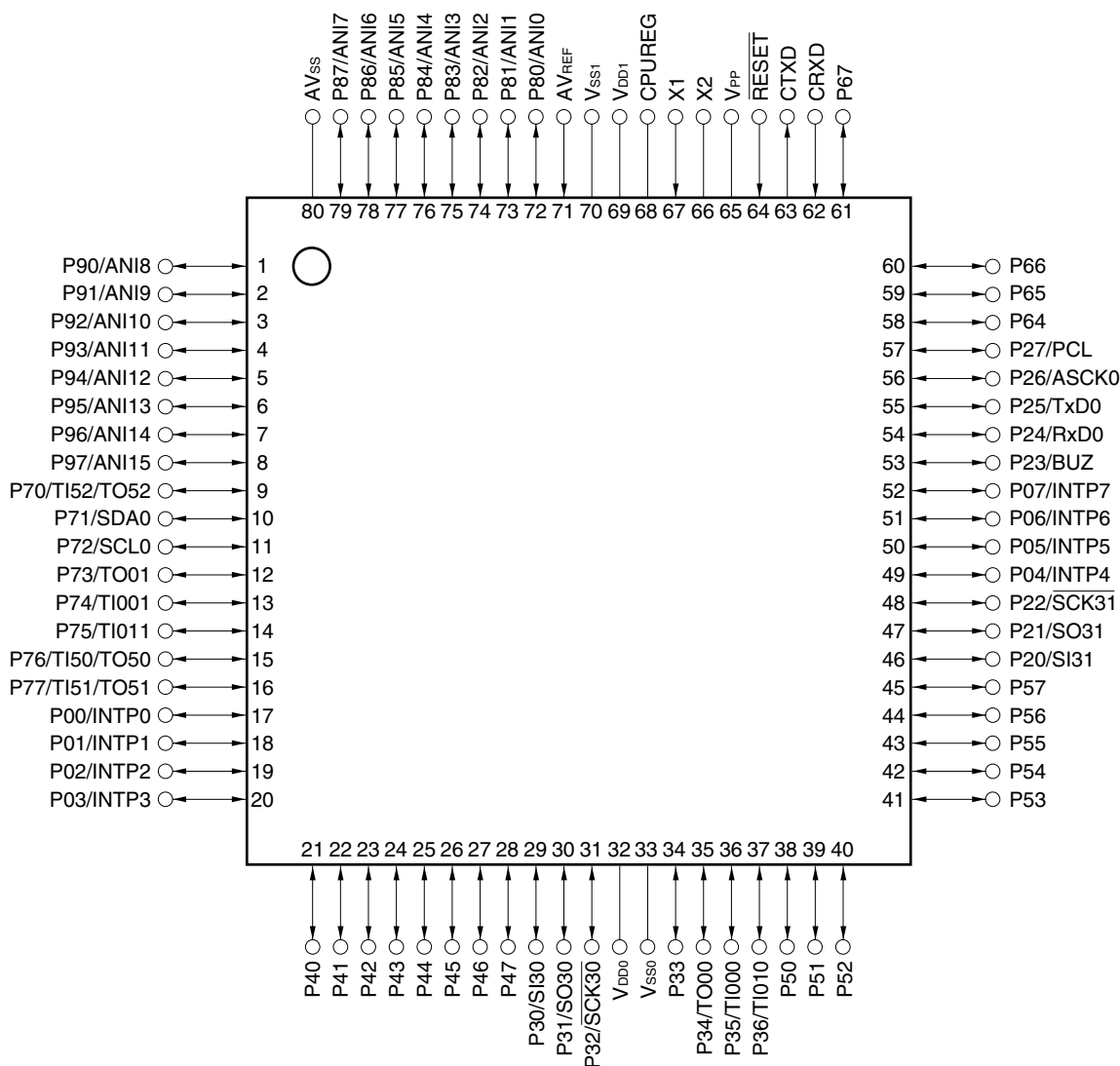
Function Subseries Name		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V <sub>DD</sub> MIN. Value	External Expansion			
			8-bit	16-bit	Watch	WDT										
Control	μPD78078Y	48 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch, I <sup>2</sup> C: 1 ch)	88	1.8 V	Yes			
	μPD78070AY	–									61	2.7 V				
	μPD780018AY	48 K to 60 K								2 ch	1 ch	1 ch		8 ch	–	2 ch
	μPD780058Y	24 K to 60 K	3 ch (time-division UART: 1ch, I <sup>2</sup> C: 1 ch)	68	1.8 V											
	μPD78058FY	48 K to 60 K	3 ch (UART: 1 ch, I <sup>2</sup> C: 1 ch)	69	2.7 V											
	μPD78054Y	16 K to 60 K			2.0 V											
	μPD780078Y	48 K to 60 K	2 ch	–	8 ch	–	4 ch (UART: 2 ch, I <sup>2</sup> C: 1 ch)	52	1.8 V							
	μPD780034AY	8 K to 32 K	1 ch	8 ch	–	3 ch (UART: 1 ch, I <sup>2</sup> C: 1 ch)	51									
	μPD780024AY															
	μPD78018FY	8 K to 60 K				2 ch (I <sup>2</sup> C: 1 ch)	53									
LCD drive	μPD780354Y	24 K to 32 K	4 ch	1 ch	1 ch	1 ch	–	8 ch	–	4 ch (UART: 1 ch, I <sup>2</sup> C: 1 ch)	66	1.8 V	–			
	μPD780344Y						8 ch	–								
	μPD780308Y	48 K to 60 K	2 ch	1 ch	1 ch	1 ch				3 ch (time-division UART: 1 ch, I <sup>2</sup> C: 1 ch)	57	2.0 V				
	μPD78064Y	16 K to 32 K								2 ch (UART: 1 ch, I <sup>2</sup> C: 1 ch)						
Bus interface supported	μPD780702Y	60 K	3 ch	2 ch	1 ch	1 ch	16 ch	–	–	4 ch (UART: 1 ch, I <sup>2</sup> C: 1 ch)	67	3.5 V	–			
	μPD780703Y	59.5 K														
	μPD780703AY	59.5 K														
	μPD780833Y	60 K									65	4.5 V				

## OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	Flash memory	59.5 KB
	High-speed RAM	1024 bytes
	Expansion RAM	2048 bytes
	Buffer RAM for DCAN	288 bytes
Minimum instruction execution time		On-chip minimum instruction execution time variable function • 0.25 μs/0.5 μs/1.00 μs/2.00 μs/4.00 μs (@ 8.00-MHz operation with system clock)
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction set		<ul style="list-style-type: none"> <li>• 16-bit operation</li> <li>• Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits)</li> <li>• Bit manipulation (set, reset, test, Boolean operation)</li> <li>• BCD adjust, etc.</li> </ul>
I/O ports		Total: 67 <ul style="list-style-type: none"> <li>• CMOS I/O: 56</li> <li>• TTL input/CMOS output: 8</li> <li>• N-ch open-drain I/O: 3</li> </ul>
A/D converter		<ul style="list-style-type: none"> <li>• 8-bit resolution × 16 channels</li> <li>• Power fail detection function</li> </ul>
Serial interface		<ul style="list-style-type: none"> <li>• 3-wire serial I/O mode: 2 channels</li> <li>• UART mode: 1 channel</li> <li>• I<sup>2</sup>C bus mode: 1 channel</li> </ul>
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter: 2 channels</li> <li>• 8-bit timer/event counter: 3 channels</li> <li>• Watch timer: 1 channel</li> <li>• Watchdog timer: 1 channel</li> </ul>
Timer output		5 (8-bit PWM output capable: 3)
Clock output		62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1.00 MHz, 2.00 MHz, 4.00 MHz, 8.00 MHz (@ 8.00-MHz operation with system clock)
Buzzer output		0.977 kHz, 1.95 kHz, 3.91 kHz, 7.81 kHz (@ 8.00-MHz operation with system clock)
DCAN controller		1 channel
Vectored interrupt sources	Maskable	Internal: 20, External: 8
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V <sub>DD</sub> = 3.5 to 5.5 V
Operating ambient temperature		T <sub>A</sub> = -40 to +85°C
Package		80-pin plastic QFP (14 × 14)

# PIN CONFIGURATION (Top View)

- 80-pin plastic QFP (14 × 14)  
μPD78F0703AYGC-8BT, 78F0703AYGC(A)-8BT



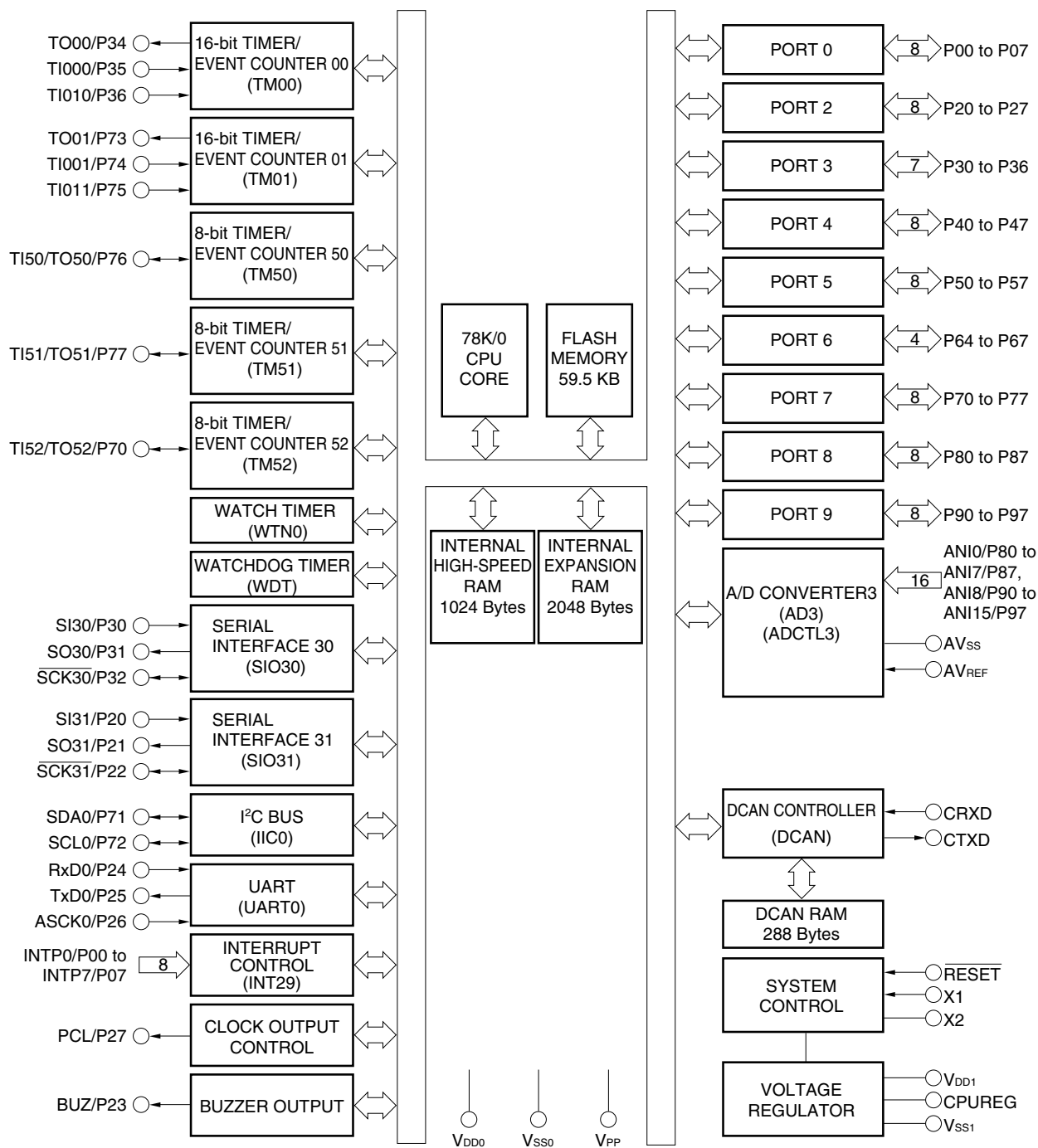
- Cautions**
- In normal operating mode, connect the VPP pin directly to VSS0 or VSS1.
  - Connect the AVSS pin to VSS0.
  - Connect the AVREF pin to VDD0.

**Remark** When the μPD78F0703AY is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to VDD0 and VDD1 individually and connecting VSS0 and VSS1 to different ground lines, is recommended.

ANI0 to ANI15:	Analog Input	PCL:	Programmable Clock
ASCK0:	Asynchronous Serial Clock	RESET:	Reset
AVREF:	Analog Reference Voltage	RxD0:	Receive Data (for UART0)
AVss:	Analog Ground	SCK30, SCK31:	Serial Clock (for SIO30, 31)
BUZ:	Buzzer Output	SCL0:	Serial Clock (for IIC0)
CPUREG:	Regulator for CPU Power Supply	SDA0:	Serial Data
CRXD:	CAN Receive Data	SI30, SI31:	Serial Input
CTXD:	CAN Transmit Data	SO30, SO31:	Serial Output
INTP0 to INTP7:	Interrupt for Peripherals	TI000, TI010, TI001,	
P00 to P07:	Port 0	TI011, TI50, TI51,	
P20 to P27:	Port 2	TI52:	Timer Input
P30 to P36:	Port 3	TO00, TO01, TO50,	
P40 to P47:	Port 4	TO51, TO52:	Timer Output
P50 to P57:	Port 5	TxD0:	Transmit Data (for UART0)
P64 to P67:	Port 6	VDD0, VDD1:	Power Supply
P70 to P77:	Port 7	VPP:	Programming Power Supply
P80 to P87:	Port 8	VSS0, VSS1:	Ground
P90 to P97:	Port 9	X1, X2:	Crystal



# BLOCK DIAGRAM



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# 1. DIFFERENCES BETWEEN μPD78F0703AY AND MASK ROM VERSION

The μPD78F0703AY is a product provided with flash memory, enabling writing, erasing, and rewriting of programs without being removed from the board.

Table 1-1 shows the differences between the flash memory version (μPD78F0703AY) and mask ROM version (μPD780703AY).

**Table 1-1. Differences Between μPD78F0703AY and Mask ROM Version**

Item	μPD78F0703AY	μPD780703AY
Internal ROM type	Flash memory	Mask ROM
Internal ROM capacity	59.5 KB	59.5 KB
IC pin	Not provided	Provided
V <sub>PP</sub> pin	Provided	Not provided
Electrical specifications	Refer to the data sheet of individual products.	

**Caution** The flash memory version and mask ROM version have different noise immunity and noise radiation characteristics. Do not use ES products for evaluation when considering switching from flash memory version to those using mask ROM upon the transition from preproduction to mass-production. CS products (mask ROM version) should be used in this case.

## 2. PIN FUNCTIONS

### 2.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00 to P07	Input/output	Port 0. 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	INTP0 to INTP7
P20	Input/output	Port 2. 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	SI31
P21					SO31
P22					$\overline{\text{SCK31}}$
P23					BUZ
P24					RxD0
P25					TxD0
P26					ASCK0
P27					PCL
P30	Input/output	Port 3. 7-bit input/output port. Input/output can be specified in 1-bit units.	An on-chip pull-up resistor can be specified by means of software.	Input	SI30
P31					SO30
P32					$\overline{\text{SCK30}}$
P33		N-ch open-drain input/output port (15-V withstand voltage). LEDs can be driven directly.			—
P34					TO00
P35		An on-chip pull-up resistor can be specified by means of software.			TI000
P36					TI010
P40 to P47	Input/output	Port 4. 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software. Interrupt request flag KRIF is set to 1 by falling edge detection.		Input	—
P50 to P57	Input/output	Port 5. 8-bit input/output port. TTL level input/CMOS output. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	—
P60 to P67	Input/output	Port 6. 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	—

## 2.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P70	Input/output	Port 7. 8-bit input/output port. Input/output can be specified in 1-bit units.	An on-chip pull-up resistor can be specified by means of software.	Input	TI52/TO52
P71			N-ch open-drain input/output port (5-V withstand voltage).		SDA0
P72					SCL0
P73			An on-chip pull-up resistor can be specified by means of software.		TO01
P74					TI001
P75					TI011
P76					TI50/TO50
P77					TI51/TO51
P80 to P87	Input/output	Port 8. 8-bit input/output port. Input/output can be specified in 1-bit units.		Input	ANI0 to ANI7
P90 to P97	Input/output	Port 9. 8-bit input/output port. Input/output can be specified in 1-bit units.		Input	ANI8 to ANI15

## 2.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP7	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00 to P07
SI30	Input	Serial interface serial data input	Input	P30
SI31				P20
SO30	Output	Serial interface serial data output	Input	P31
SO31				P21
SDA0	I/O	Serial interface serial data input/output	Input	P71
SCK30	I/O	Serial interface serial clock input/output	Input	P32
SCK31				P22
SCL0				P72
RxD0	Input	Serial data input for asynchronous serial interface	Input	P24
TxD0	Output	Serial data output for asynchronous serial interface	Input	P25
ASCK0	Input	Serial clock input for asynchronous serial interface	Input	P26
CRXD	Input	Data input of DCAN controller (DCAN)	Input	–
CTXD	Output	Data output of DCAN controller (DCAN)	Output	–
TI000	Input	External count clock input to 16-bit timer (TM00)	Input	P35
TI010		External count clock input to 16-bit timer (TM00)		P36
TI001		External count clock input to 16-bit timer (TM01)		P74
TI011		External count clock input to 16-bit timer (TM01)		P75
TI50		External count clock input to 8-bit timer (TM50)		P76/TO50
TI51		External count clock input to 8-bit timer (TM51)		P77/TO51
TI52		External count clock input to 8-bit timer (TM52)		P70/TO52
TO00	Output	16-bit timer (TM00) output	Input	P34
TO01		16-bit timer (TM01) output		P73
TO50		8-bit timer (TM50) output		P76/TO50
TO51		8-bit timer (TM51) output		P77/TO51
TO52		8-bit timer (TM52) output		P70/TO52
PCL	Output	Clock output	Input	P27
BUZ	Output	Buzzer output	Input	P23
ANI0 to ANI7	Input	A/D converter (AD3) analog input	Input	P80 to P87
ANI8 to ANI15				P90 to P97
AV <sub>REF</sub>	Input	A/D converter (AD3) reference voltage and analog power supply	–	–
AV <sub>SS</sub>	–	A/D converter (AD3) ground potential	–	–
X1	Input	Connecting crystal resonator for system clock oscillation	–	–
X2	–		–	–

## 2.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
$\overline{\text{RESET}}$	Input	System reset input	Input	—
CPUREG	—	Regulator for CPU power supply. Connect to $V_{SS0}$ or $V_{SS1}$ via a 0.1-μF capacitor.	—	—
$V_{DD0}$	—	Positive power supply for ports	—	—
$V_{DD1}$	—	Positive power supply (except ports and analog section)	—	—
$V_{SS0}$	—	Ground potential for ports	—	—
$V_{SS1}$	—	Ground potential (except ports and analog section)	—	—
$V_{PP}$	—	High voltage applied during program write/verify. Connect directly to $V_{SS0}$ or $V_{SS1}$ in normal operating mode.	—	—

### 2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1.

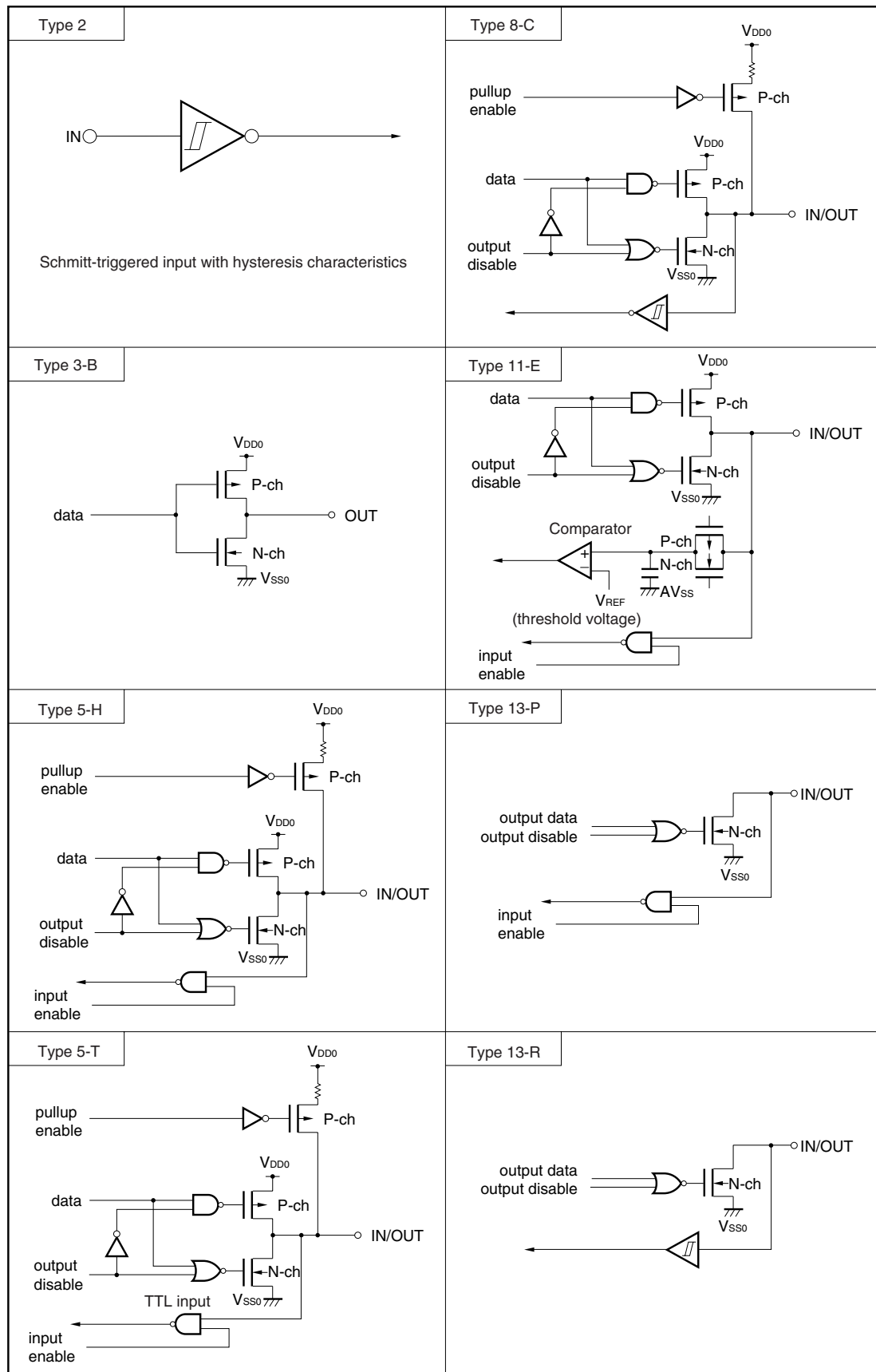
For the input/output circuit configuration of each type, refer to Figure 2-1.

**Table 2-1. Types of Pin Input/Output Circuits**

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P07/INTP7	8-C	Input/output	Independently connect to V <sub>SS0</sub> via a resistor.
P20/SI31			Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.
P21/SO31	5-H		
P22/SCK31			8-C
P23/BUZ			5-H
P24/RxD0			8-C
P25/TxD0			5-H
P26/ASCK0			8-C
P27/PCL			5-H
P30/SI30			8-C
P31/SO30			5-H
P32/SCK30			8-C
P33			13-P
P34/TO00	5-H		Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.
P35/TI000	8-C		
P36/TI010			
P40 to P47	5-H		Independently connect to V <sub>DD0</sub> via a resistor.
P50 to P57	5-T		Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.
P64 to P67	5-H		
P70/TI52/TO52			
P71/SDA0	13-R		Independently connect to V <sub>DD0</sub> via a resistor.
P72/SCL0			
P73/TO01	5-H		Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.
P74/TI001	8-C		
P75/TI011			
P76/TI50/TO50			
P77/TI51/TO51			
P80/ANI0 to P87/ANI7	11-E		
P90/ANI8 to P97/ANI15			
CRXD	2	Input	
CTXD	3-B	Output	Leave open.
RESET	2	Input	—
AV <sub>REF</sub>	—		Connect to V <sub>DD0</sub> .
AV <sub>SS</sub>		—	Connect to V <sub>SS0</sub> .
V <sub>PP</sub>			Connect directly to V <sub>SS0</sub> or V <sub>SS1</sub> .



Figure 2-1. Pin Input/Output Circuits



### 3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register used to disable a part of the internal memory by means of software.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$  input sets IMS to CFH.

**Caution** Use IMS with its default value (CFH). Do not set any other values for the IMS.

**Figure 3-1. Format of Internal Memory Size Switching Register (IMS)**

Address:	FFF0H	After reset:	CFH	R/W				
Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection	
1	1	0	1024 bytes	
Other than above			Setting prohibited	

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection	
1	1	1	1	59.5 KB	
Other than above				Setting prohibited	

#### 4. INTERNAL EXPANSION RAM SIZE SELECT REGISTER (IXS)

The internal expansion RAM size select register (IXS) selects the internal expansion RAM capacity.

IXS is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$  input sets IXS to 0CH.

**Caution** Set IXS to 08H as the default status of the program. Because IXS is set to 0CH at a reset, set it to 08H after a reset.

Figure 4-1. Format of Internal Expansion RAM Size Select Register (IXS)

Address: FFF4H

After reset: 0CH

R/W

Symbol

7

6

5

4

3

2

1

0

IXS

0

0

0

IXRAM4

IXRAM3

IXRAM2

IXRAM1

IXRAM0

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expansion RAM capacity selection
0	1	0	0	0	2048 bytes
Other than above					Setting prohibited

## 5. FLASH MEMORY PROGRAMMING

The flash memory can be written even while the device is mounted on the target system (on-board write). To write a program to the flash memory, connect the dedicated flash programmer (Flashpro III (model number: FL-PR3 and PG-FP3)/Flashpro IV (model number: FL-PR4 and PG-FP4)) to both the host machine and target system.

A program can also be written by using an adapter for flash memory writing, connected to the Flashpro III/Flashpro IV.

The  $\mu$ PD78F0703AY can also be programmed via self-programming of the flash memory.

**Remark** The FL-PR3 and FL-PR4 is manufactured by Naito Densai Machida Mfg. Co., Ltd.  
Contact: +81-45-475-4191

### 5.1 Selecting Communication Mode

The Flashpro III/Flashpro IV writes to flash memory by means of serial communication. The communication mode to be used for writing is selected from those listed in Table 5-1. To select a communication mode, use the format shown in Figure 5-1, according to the number of  $V_{PP}$  pulses listed in Table 5-1.

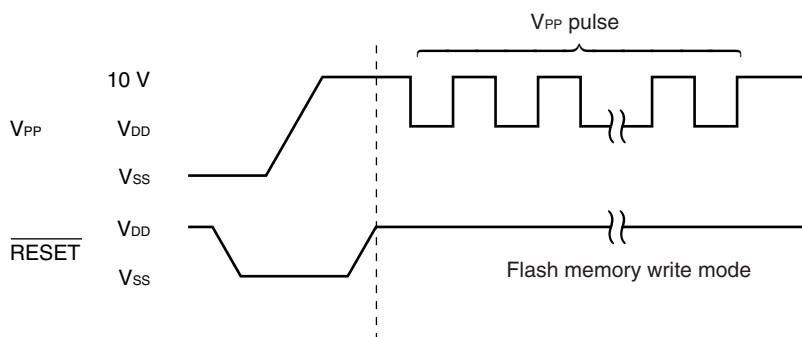
**Table 5-1. Communication Mode**

Communication Mode	Number of Channels	Pins Used <sup>Note</sup>	Number of $V_{PP}$ Pulses
3-wire serial I/O	2	SI30/P30 SO30/P31 $\overline{SCK30/P32}$	0
		SI31/P20 SO31/P21 $\overline{SCK31/P22}$	1

**Note** Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as immediately after reset. Therefore, all ports enter an output high-impedance state. If the external devices do not acknowledge an output high-impedance state, handling such as connecting to  $V_{DD}$  via a resistor or connecting to  $V_{SS}$  via a resistor is required.

**Caution** The communication mode must be selected by the number of  $V_{PP}$  pulses listed in Table 5-1.

**Figure 5-1. Communication Mode Selection Format**



## 5.2 Flash Memory Programming Function

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected communication mode. Table 5-2 lists the major flash memory programming functions.

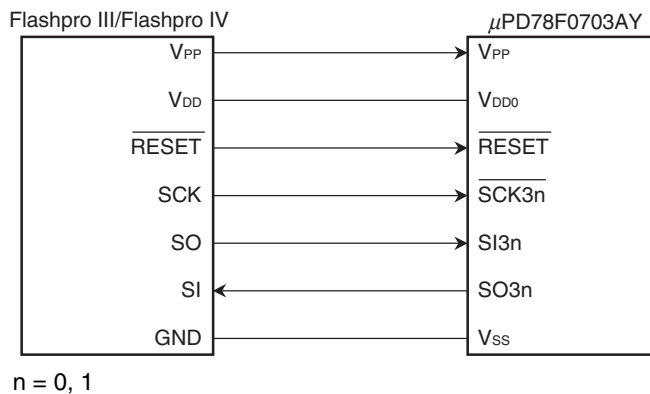
**Table 5-2. Major Functions of Flash Memory Programming**

Function	Description
Reset	Stops writing or detects communication synchronization.
Batch verify	Compares the entire contents of memory with the input data.
Batch internal verify	Compares the entire contents of memory in different modes.
Batch erase	Erases the entire contents of memory.
Batch blank check	Checks that the entire contents of memory have been erased.
High-speed write	Writes to the flash memory according to the specified write start address and number of data bytes to be written.
Continuous write	Continues writing based on the information input by using the high-speed write function.
Batch prewrite	Writes 00H into the entire contents of memory.
Status	Checks the current operating mode and whether the operation has ended.
Oscillation frequency setting	Inputs the frequency information of the resonator.
Erase time setting	Inputs the memory erase time.
Silicon signature read	Outputs the device name, memory capacity, and device block information.

## 5.3 Connecting Flashpro III/Flashpro IV

The connection between the Flashpro III/Flashpro IV and μPD78F0703AY varies according to the communication mode. Figure 5-2 shows the connection.

**Figure 5-2. Flashpro III/Flashpro IV Connection in 3-Wire Serial I/O Mode (SI03)**



## 6. SECURE FLASH SELF-PROGRAMMING WITH REAL-TIME SUPPORT

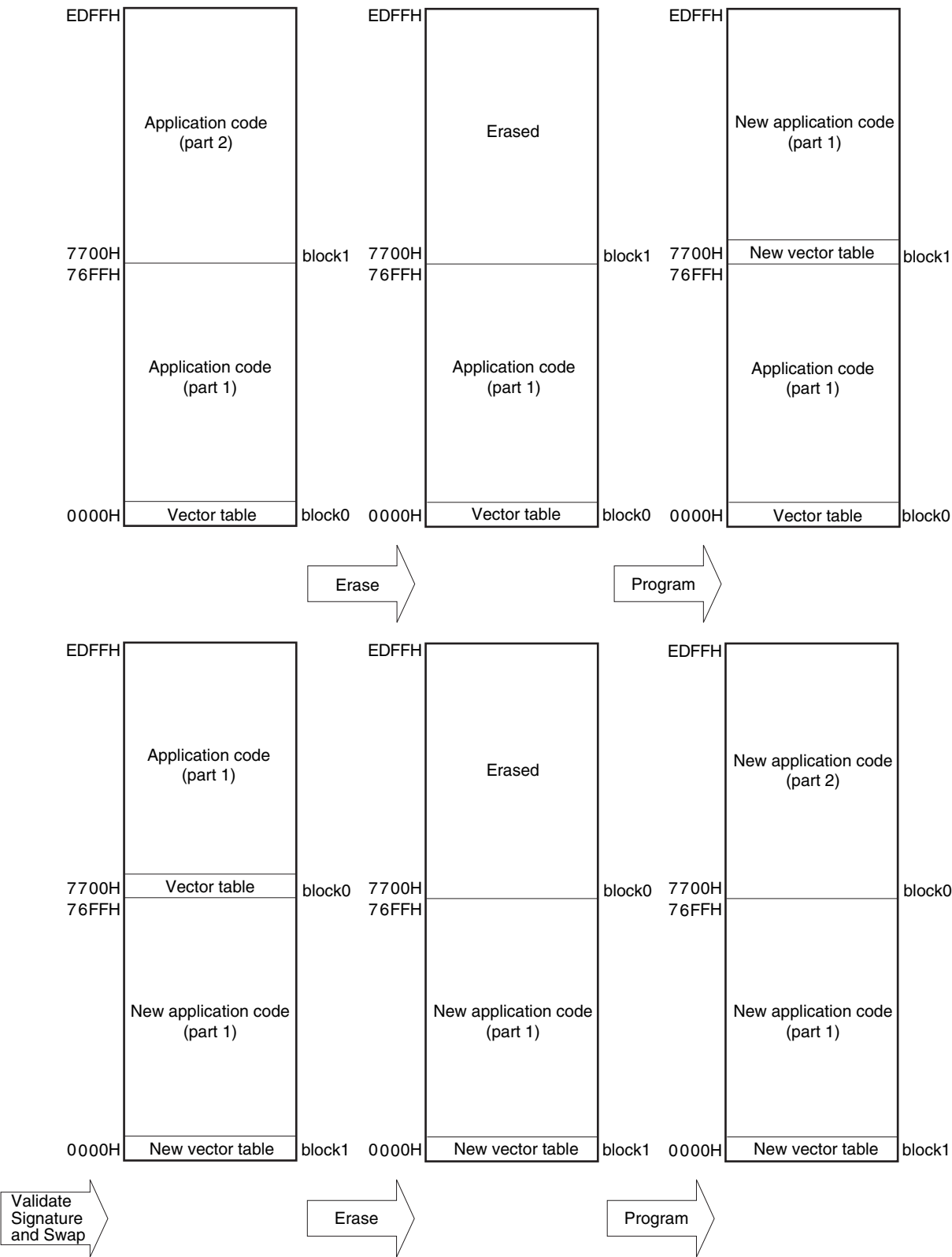
The  $\mu$ PD78F0703AY supports the self-programming of the flash memory by a program. The self-programming is implemented as secure self-programming in order to avoid a non-startup of the device after a power down behaviour. For the support of windows watchdogs or the notification on the CAN-bus during the self-programming of the device a real-time function for the handling of a task is implemented.

### 6.1 Self-programming of both Flash Memory Blocks with Block Swapping

The memory map of the  $\mu$ PD78F0703AY contains in user mode two 29.75 KB flash memory blocks from address 0000H onward. To erase and download the data and program the upper block, the routines residing in the lower block can be utilized and even after a power failure the lower block is present and valid.

To update the lower 29.75 KB block, the complete flash memory of the device needs to be programmed. At first the upper block is erased. As second the data of the new lower block is programmed into the upper block before the both blocks are internally swapped. Finally the former lower block is programmed with the remaining application data. This procedure allows to re-program both flash memory blocks (lower block and upper block) and to avoid a power failure.

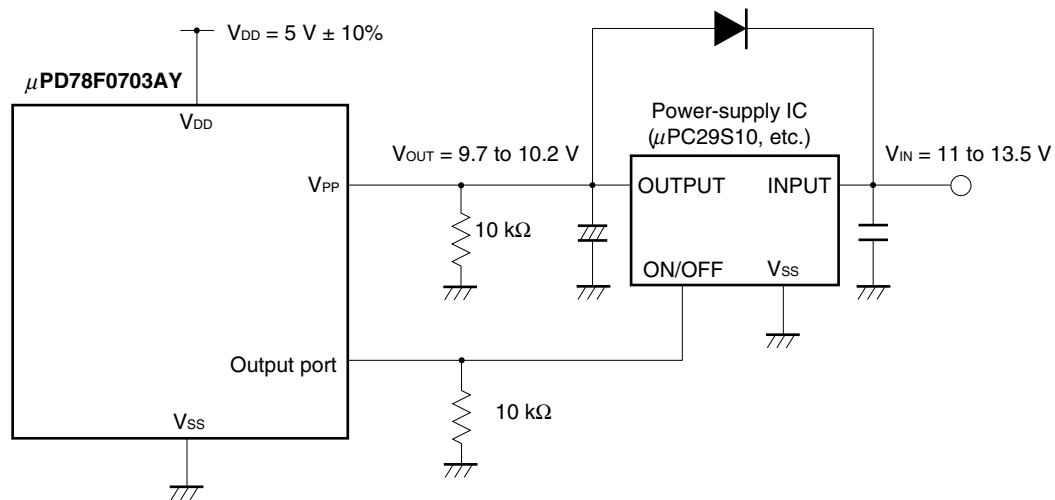
Figure 6-1. Memory Map for the Self-programming Function



## 6.2 Self-programming Circuit Requirements

Figure 6-2 shows the self-programming circuit requirements.

**Figure 6-2. Self-programming Circuit Requirements**





## 7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V <sub>DD</sub>	V <sub>DD</sub> = AV <sub>REF</sub>		−0.3 to +6.5	V
	AV <sub>REF</sub>				
	V <sub>PP</sub>	<b>Note 1</b>		−0.3 to +10.5	V
	AV <sub>SS</sub>			−0.3 to +0.3	V
Input voltage	V <sub>I1</sub>	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CRXD, X1, X2, RESET		−0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>I2</sub>	P33	N-ch open drain	−0.3 to +16.0	V
Output voltage	V <sub>O</sub>	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD		−0.3 to V <sub>DD</sub> + 0.3	V
Analog input voltage	V <sub>AN</sub>	P80 to P87, P90 to P97	Analog input pin	AV <sub>SS</sub> − 0.3 to AV <sub>REF</sub> + 0.3 and −0.3 to V <sub>DD</sub> + 0.3	V
Output current, high	I <sub>OH</sub>	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77, P80 to P87, P90 to P97, CRXD		−10	mA
		Total for all pins		−30	mA
Output current, low	I <sub>OL</sub> <sup>Note 2</sup>	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD	Peak value	20	mA
			rms value	10	mA
		P33	Peak value	30	mA
			rms value	15	mA
		Total for all pins	Peak value	100	mA
			rms value	60	mA
Operating ambient temperature	T <sub>A</sub>			−40 to +85	°C
★ Programming ambient temperature	T <sub>PRG</sub>			+10 to +40	°C
Storage temperature	T <sub>stg</sub>	Before 2000 hours elapses after flash memory programming was performed		−40 to +125	°C
		After flash memory programming was performed and 2000 hours or more has elapsed		−40 to +125	°C

(Refer to **Note** on the next page.)

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

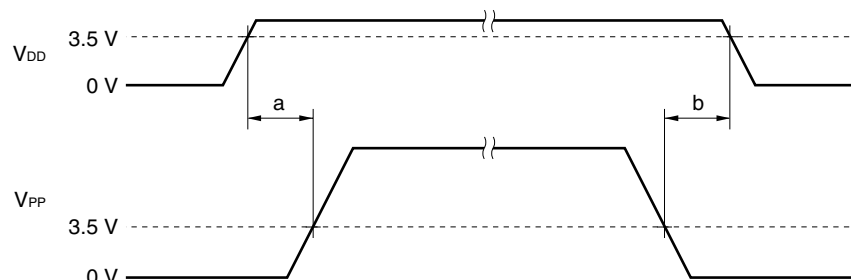
**Notes 1.** Make sure that the following conditions of the  $V_{PP}$  voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**

$V_{PP}$  must exceed  $V_{DD}$  10  $\mu$ s or more after  $V_{DD}$  has reached the lower-limit value (3.5 V) of the operating voltage range (1 ms if the supply voltage is dropped by the regulator) (see a in the figure below).

- **When supply voltage drops**

Raise  $V_{DD}$  10  $\mu$ s or more after  $V_{PP}$  falls below the lower-limit value (3.5 V) of the operating voltage range of  $V_{DD}$  (see b in the figure below).



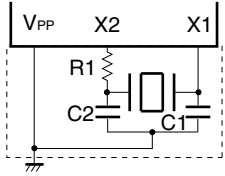
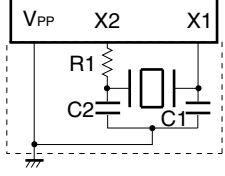
2. The rms value should be calculated as follows: [rms value] = [Peak value]  $\times \sqrt{\text{Duty}}$

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{IN}$	$f = 1 \text{ MHz}$ Other than measured pins: 0 V				15	pF
Output capacitance	$C_{OUT}$	$f = 1 \text{ MHz}$ Other than measured pins: 0 V				15	pF
Input/output capacitance	$C_{IO}$	$f = 1 \text{ MHz}$ Other than measured pins: 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97			15	pF
			P33			20	pF

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**System Clock Oscillator Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.5$  to  $5.5$  V)**

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency ( $f_x$ ) <sup>Note 1</sup>			8.00		MHz
		Oscillation stabilization time <sup>Note 2</sup>				10	ms
Ceramic resonator		Oscillation frequency ( $f_x$ ) <sup>Note 1</sup>			8.00		MHz
		Oscillation stabilization time <sup>Note 2</sup>				4	ms

**Notes** 1. Indicates only oscillator characteristics.

2. Time required to stabilize oscillation after reset or STOP mode release.

**Caution** When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as  $V_{SS1}$ .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

DC Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.5$  to  $5.5$  V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	$V_{IH1}$	P21, P23, P25, P27, P31, P34, P40 to P47, P64 to P67, P73, P80 to P87, P90 to P97		$0.7V_{DD}$		$V_{DD}$	V
	$V_{IH2}$	P00 to P07, P20, P22, P24, P26, P30, P32, P35, P36, P70 to P72, P74 to P77, CRXD, RESET		$0.8V_{DD}$		$V_{DD}$	V
	$V_{IH3}$	P50 to P57		2.3		$V_{DD}$	V
	$V_{IH4}$	P33	N-ch open drain	$0.7V_{DD}$		15.0	V
Input voltage, low	$V_{IL1}$	P21, P23, P25, P27, P31, P34, P40 to P47, P64 to P67, P73, P80 to P87, P90 to P97		0		$0.3V_{DD}$	V
	$V_{IL2}$	P00 to P07, P20, P22, P24, P26, P30, P32, P35, P36, P70 to P72, P74 to P77, CRXD, RESET		0		$0.2V_{DD}$	V
	$V_{IL3}$	P50 to P57		0		0.75	V
	$V_{IL4}$	P33	N-ch open drain	0		$0.3V_{DD}$	V
Output voltage, high	$V_{OH1}$	$I_{OH} = -1$ mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77, P80 to P87, P90 to P97, CTXD	$V_{DD} - 1.0$		$V_{DD}$	V
	$V_{OH2}$	$I_{OH} = -100$ $\mu$ A		$V_{DD} - 0.5$		$V_{DD}$	V
Output voltage, low	$V_{OL1}$	$I_{OL} = 15$ mA	P33		0.4	2.0	V
	$V_{OL2}$	$I_{OL} = 1.6$ mA	P71, P72			0.4	V
	$V_{OL3}$	$I_{OL} = 1$ mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77, P80 to P87, P90 to P97, CTXD			1.0	V
	$V_{OL4}$	$I_{OL} = 100$ $\mu$ A				0.5	V
Input leakage current, high	$I_{LIH1}$	$V_{IN} = V_{DD}$	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CRXD, RESET			3	$\mu$ A
	$I_{LIH2}$		X1			20	$\mu$ A
	$I_{LIH3}$	$V_{IN} = 15$ V	P33			80	$\mu$ A
Input leakage current, low	$I_{LIL1}$	$V_{IN} = 0$ V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P80 to P87, P90 to P97, CRXD, RESET			-3	$\mu$ A
	$I_{LIL2}$		X1			-20	$\mu$ A
	$I_{LIL3}$		P33 (except executing input instruction <sup>Note</sup> )			-3	$\mu$ A

**Note** During input instruction execution, a low-level input leakage current of  $-200$   $\mu$ A (MAX.) flows only for 1 clock (without wait).

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T<sub>A</sub> = −40 to +85°C, V<sub>DD</sub> = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub>	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD			3	μA
Output leakage current, low	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD			−3	μA
Software pull-up resistor	R <sub>1</sub>	V <sub>IN</sub> = 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77	15	30	90	kΩ
Power supply current <sup>Note 1</sup>	I <sub>DD1</sub>	8.00-MHz crystal oscillation operating mode			9.0	20	mA
	I <sub>DD2</sub>	8.00-MHz crystal oscillation HALT mode (DCAN operating) <sup>Note 2</sup>			1.6	3.0	mA
	I <sub>DD3</sub>	8.00-MHz crystal oscillation HALT mode (DCAN sleep mode) <sup>Note 2</sup>			700	1500	μA
	I <sub>DD4</sub>	STOP mode			1.5	30	μA

**Notes 1.** Refers to the current flowing to the V<sub>DD1</sub> pin. The current flowing to the A/D converter and on-chip pull-up resistor is not included.

**2.** Low-speed mode operation (when processor clock control register (PCC) is set to 04H). The current for peripheral circuit operation is not included.

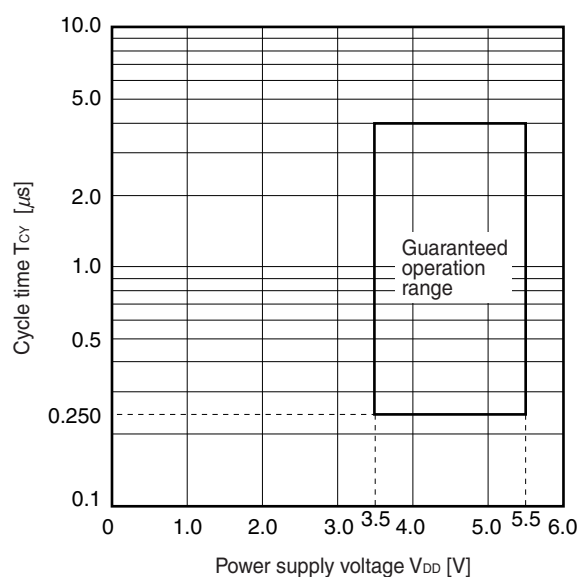
**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

## AC Characteristics

(1) Basic operation ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.5$  to  $5.5$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	$T_{CY}$	Operating with system clock ( $f_x = 8.00$ MHz)	0.250		4.00	$\mu\text{s}$
TI000, TI010, TI001, TI011 input high-/low-level width	$t_{T1H0}$ $t_{T1L0}$		$4/f_{sam} + 0.25^{\text{Note}}$			$\mu\text{s}$
TI50, TI51, TI52 input frequency	$f_{T15}$				2	MHz
TI50, TI51, TI52 input high-/low-level width	$t_{T1H5}$ $t_{T1L5}$		200			ns
Interrupt request input high-/low-level width	$t_{INTH}$ $t_{INTL}$	INTP0 to INTP7, P40 to P47	10			$\mu\text{s}$
RESET low-level width	$t_{RSL}$		10			$\mu\text{s}$

**Note** Selection of  $f_{sam} = f_x/2$ ,  $f_x/4$ ,  $f_x/64$  is possible with bits 0 and 1 (PRM0n0, PRM0n1) of prescaler mode register 0n (PRM0n). However, if the TI00n valid edge is selected as the count clock, the value becomes  $f_{sam} = f_x/8$  ( $n = 0, 1$ ).

T<sub>CY</sub> vs V<sub>DD</sub> (At system clock operation)

(2) Serial interface ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.5$  to  $5.5$  V)

(a) 3-wire serial I/O mode ( $\overline{\text{SCK30}}$  ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK30}}$ cycle time	$t_{\text{KCY1}}$		1.9			$\mu\text{s}$
$\overline{\text{SCK30}}$ high-/low-level width	$t_{\text{KH1}}$ $t_{\text{KL1}}$		$t_{\text{KCY1}}/2 - 50$			ns
SI30 setup time (to $\overline{\text{SCK30}}\uparrow$ )	$t_{\text{SIK1}}$		100			ns
SI30 hold time (from $\overline{\text{SCK30}}\uparrow$ )	$t_{\text{KSI1}}$		400			ns
SO30 output delay time from $\overline{\text{SCK30}}\downarrow$	$t_{\text{KSO1}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

**Note** C is the load capacitance of the  $\overline{\text{SCK30}}$  and SO30 output lines.

(b) 3-wire serial I/O mode ( $\overline{\text{SCK30}}$  ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK30}}$ cycle time	$t_{\text{KCY2}}$		800			ns
$\overline{\text{SCK30}}$ high-/low-level width	$t_{\text{KH2}}$ $t_{\text{KL2}}$		400			ns
SI30 setup time (to $\overline{\text{SCK30}}\uparrow$ )	$t_{\text{SIK2}}$		100			ns
SI30 hold time (from $\overline{\text{SCK30}}\uparrow$ )	$t_{\text{KSI2}}$		400			ns
SO30 output delay time from $\overline{\text{SCK30}}\downarrow$	$t_{\text{KSO2}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

**Note** C is the load capacitance of the SO30 output line.

**(c) 3-wire serial I/O mode ( $\overline{\text{SCK31}}$  ... Internal clock output)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK31}}$ cycle time	$t_{\text{KCY3}}$		1.9			$\mu\text{s}$
$\overline{\text{SCK31}}$ high-/low-level width	$t_{\text{KH3}}$ $t_{\text{KL3}}$		$t_{\text{KCY1}}/$ 2 – 50			ns
SI31 setup time (to $\overline{\text{SCK31}}\uparrow$ )	$t_{\text{SIK3}}$		100			ns
SI31 hold time (from $\overline{\text{SCK31}}\uparrow$ )	$t_{\text{KSI3}}$		400			ns
SO31 output delay time from $\overline{\text{SCK31}}\downarrow$	$t_{\text{KSO3}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

**Note** C is the load capacitance of the  $\overline{\text{SCK31}}$  and SO31 output lines.

**(d) 3-wire serial I/O mode ( $\overline{\text{SCK31}}$  ... External clock input)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK31}}$ cycle time	$t_{\text{KCY4}}$		800			ns
$\overline{\text{SCK31}}$ high-/low-level width	$t_{\text{KH4}}$ $t_{\text{KL4}}$		400			ns
SI31 setup time (to $\overline{\text{SCK31}}\uparrow$ )	$t_{\text{SIK4}}$		100			ns
SI31 hold time (from $\overline{\text{SCK31}}\uparrow$ )	$t_{\text{KSI4}}$		400			ns
SO31 output delay time from $\overline{\text{SCK31}}\downarrow$	$t_{\text{KSO4}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

**Note** C is the load capacitance of the SO31 output line.



**(e) UART mode (Dedicated baud rate generator output)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					62500	bps

**(f) UART mode (External clock input)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t <sub>KCY3</sub>		800			ns
ASCK0 high-/low-level width	t <sub>KH3</sub> , t <sub>KL3</sub>		400			ns
Transfer rate					78125	bps

**(g) I<sup>2</sup>C bus mode**

Parameter		Symbol	Standard Mode		High-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f <sub>SCL</sub>	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t <sub>BUF</sub>	4.7	—	1.3	—	μs
Hold time <sup>Note 1</sup>		t <sub>HD:STA</sub>	4.0	—	0.6	—	μs
SCL0 clock low-level width		t <sub>LOW</sub>	4.7	—	1.3	—	μs
SCL0 clock high-level width		t <sub>HIGH</sub>	4.0	—	0.6	—	μs
Start/restart condition setup time		t <sub>SU:STA</sub>	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	t <sub>HD:DAT</sub>	5.0	—	—	—	μs
	I <sup>2</sup> C bus		0 <sup>Note 2</sup>	—	0 <sup>Note 2</sup>	0.9 <sup>Note 3</sup>	μs
Data setup time		t <sub>SU:DAT</sub>	250	—	100 <sup>Note 4</sup>	—	ns
SDA0 and SCL0 signal rise time		t <sub>R</sub>	—	1000	—	300	ns
SDA0 and SCL0 signal fall time		t <sub>F</sub>	—	300	—	300	ns
Stop condition setup time		t <sub>SU:STO</sub>	4.0	—	0.6	—	μs
Spike pulse width controlled by input filter		t <sub>SP</sub>	—	—	0	50	ns
Capacitive load of each bus line		C <sub>b</sub>	—	400	—	400	pF

**Notes 1.** On start condition, the first clock pulse is generated after this period.

**2.** To fulfill undefined area of the SCL0 falling edge, it is necessary for the device to provide internally SDA0 signal (on V<sub>IHmin.</sub> of SCL0 signal) with at least 300 ns of hold time.

**3.** If the device does not extend the SCL0 signal low hold time (t<sub>LOW</sub>), only maximum data hold time t<sub>HD:DAT</sub> needs to be fulfilled.

**4.** The high-speed mode I<sup>2</sup>C bus is available in the standard mode I<sup>2</sup>C bus system. At this time, the conditions described below must be satisfied.

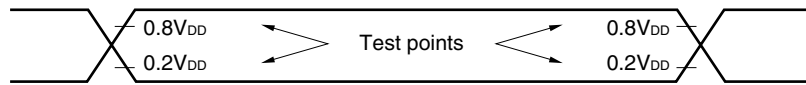
- If the device does not extend the SCL0 signal low state hold time

$$t_{SU:DAT} \geq 250 \text{ ns}$$

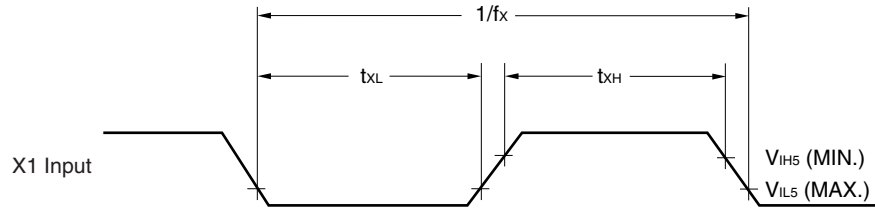
- If the device extends the SCL0 signal low state hold time

Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released (t<sub>Rmax.</sub> + t<sub>SU:DAT</sub> = 1000 + 250 = 1250 ns by standard mode I<sup>2</sup>C bus specification).

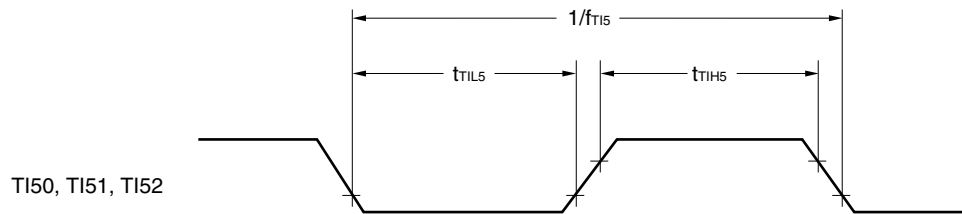
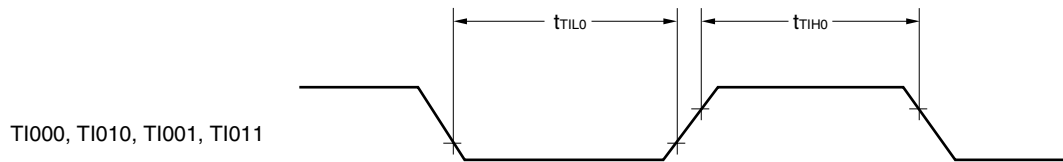
### AC Timing Test Points (excluding X1 input)



### Clock Timing

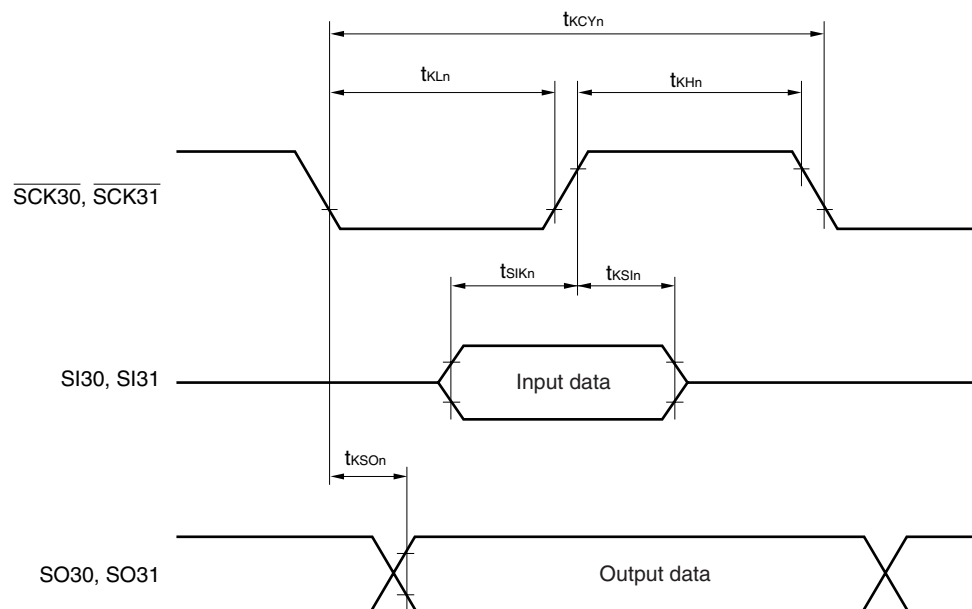


### TI Timing



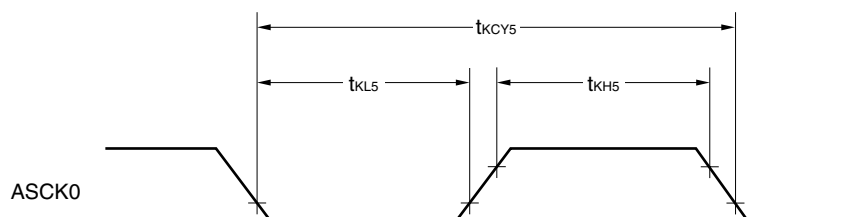
## Serial Transfer Timing

### 3-wire serial I/O mode:

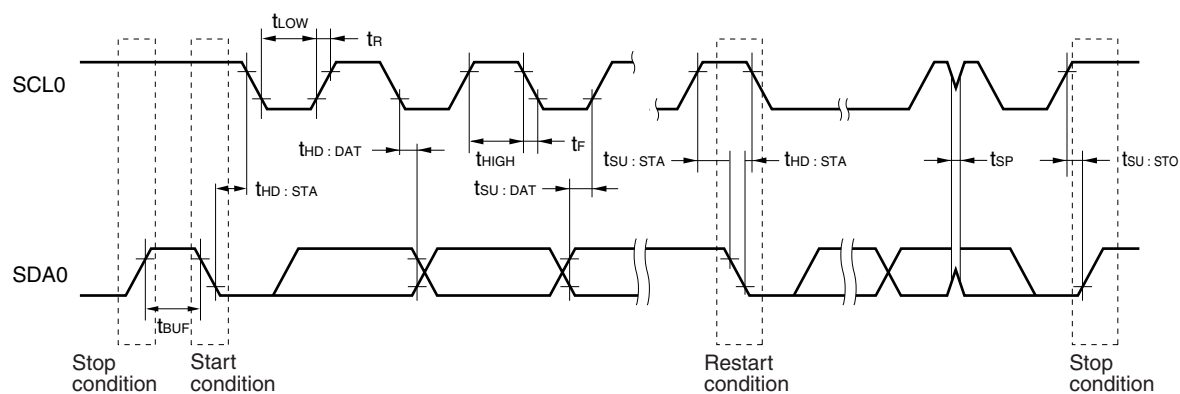


$n = 1 \text{ to } 4$

### UART mode (external clock input):



### I<sup>2</sup>C bus mode:



**DCAN Controller Characteristics** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.5$  to  $5.5$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$f_x = 8.00$ MHz			500	kbps

**A/D Converter Characteristics** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = AV_{REF} = 3.5$  to  $5.5$  V,  $V_{SS} = AV_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error <sup>Note</sup>					$\pm 0.6$	%FSR
Conversion time	$t_{CONV}$		14		100	$\mu\text{s}$
Analog input voltage	$V_{IAN}$		$AV_{SS}$		$AV_{REF}$	V
$AV_{REF}$ resistance	$R_{AIREF}$		4.0	8.0		$k\Omega$

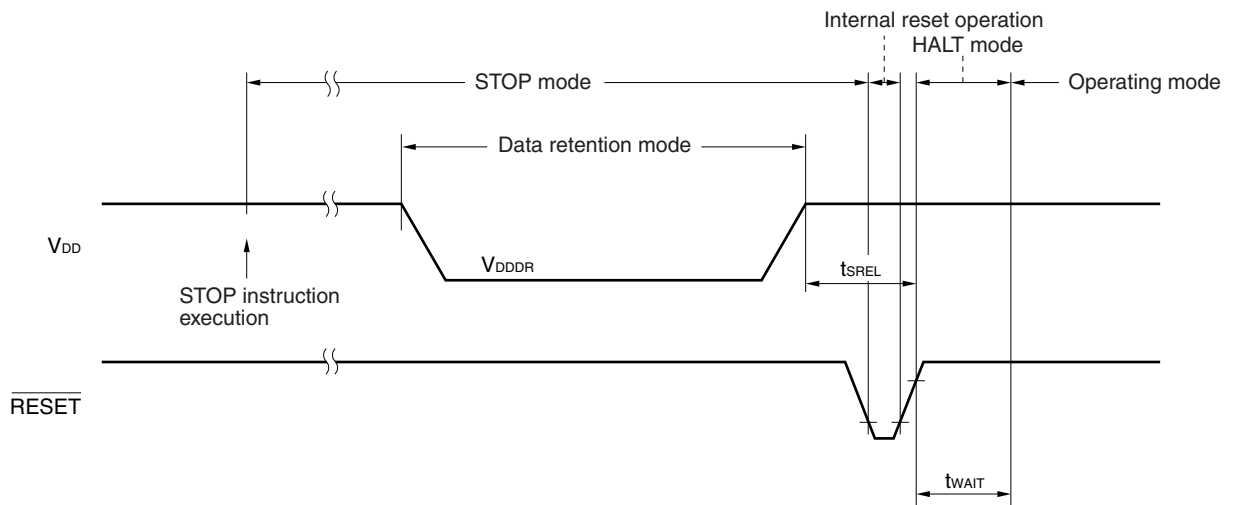
**Note** Excludes quantization error ( $\pm 0.2\%$ ). It is indicated as a ratio to the full-scale value.

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85°C)**

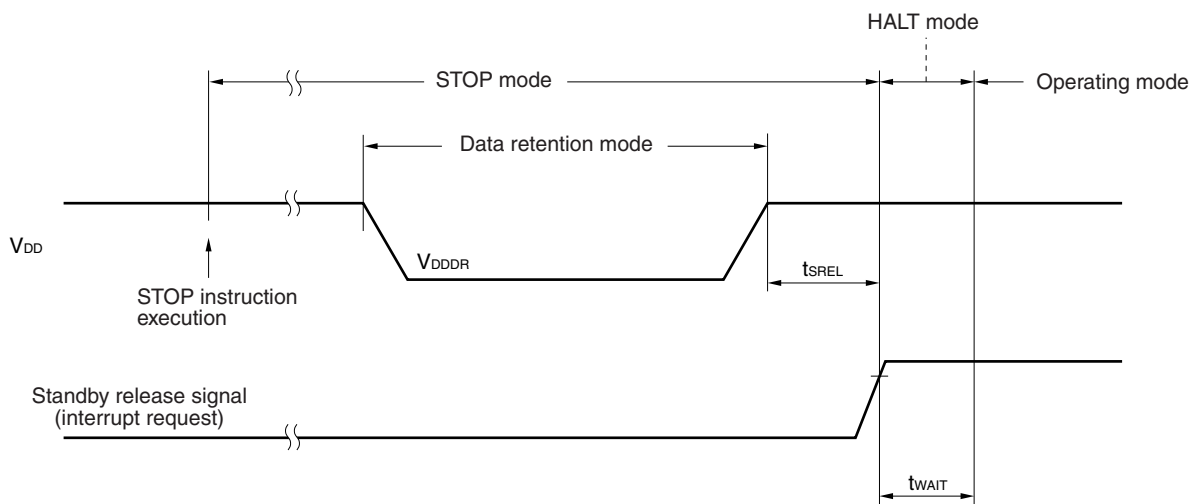
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V <sub>DDDR</sub>		2.0		5.5	V
Data retention power supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 2.0 V		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
★ Oscillation stabilization wait time	t <sub>WAIT</sub>	Release by $\overline{\text{RESET}}$		2 <sup>16</sup> /f <sub>x</sub>		s
		Release by interrupt request		Note		s

**Note** Selection of 2<sup>12</sup>/f<sub>x</sub>, 2<sup>14</sup>/f<sub>x</sub>, 2<sup>15</sup>/f<sub>x</sub>, and 2<sup>17</sup>/f<sub>x</sub> is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

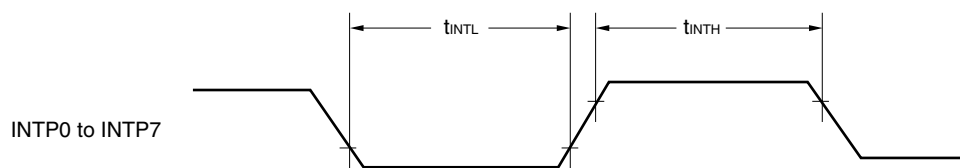
**Data Retention Timing (STOP mode release by  $\overline{\text{RESET}}$ )**



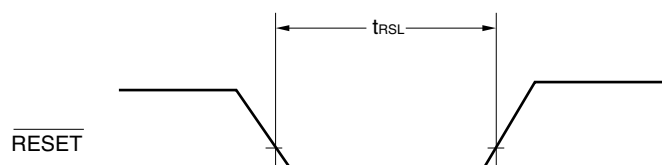
**Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)**



### Interrupt Request Input Timing



### $\overline{\text{RESET}}$ Input Timing



★ Flash Memory Programming Characteristics

(1) Basic characteristics

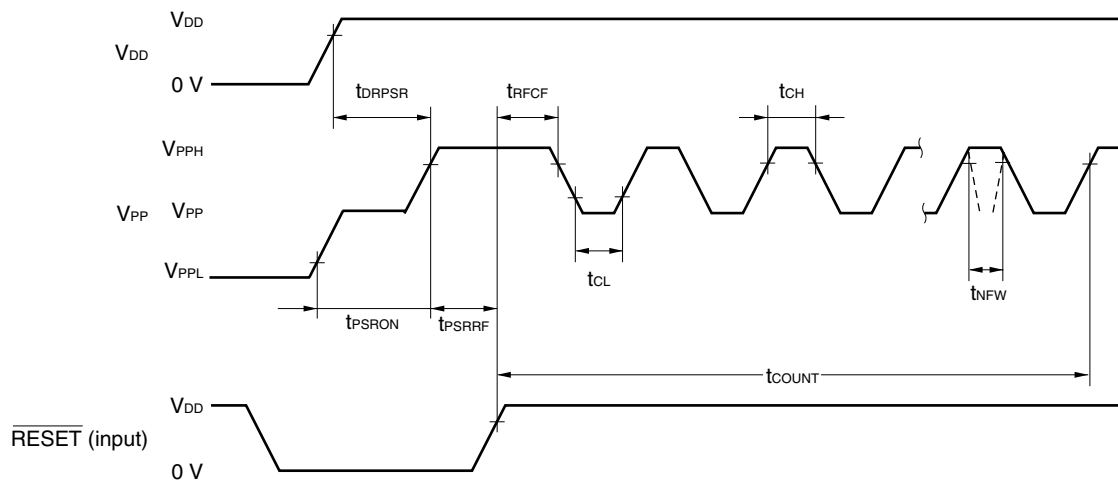
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	$f_X$		8.0		8.0	MHz
Supply voltage	$V_{DD}$		3.5		5.5	V
	$V_{PPL}$	When detecting $V_{PP}$ low level	0		$0.2 V_{DD}$	V
	$V_{PP}$	When detecting $V_{PP}$ high level	$0.8 V_{DD}$		$1.2 V_{DD}$	V
	$V_{PPH}$	When detecting $V_{PP}$ high voltage	9.7	10.0	10.3	V
$V_{DD}$ supply current	$I_{DD}$				50	mA
$V_{PP}$ supply current	$I_{PP}$	$V_{PP} = 10.0 \text{ V}$			100	mA
Write time (per byte)	$t_{WRT}$				500	$\mu\text{s}$
Number of rewriting times	$C_{WRT}$	$T_{PRG} = +10 \text{ to } +40 \text{ }^\circ\text{C}$			20	times
Erase time	$t_{ERASE}$				20	s

**Remark** For details of the input/output voltage and input/output leakage current, refer to DC Characteristics.

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$V_{PP}$ set time	$t_{PSRON}$	$V_{PP}$ high voltage	1.0			$\mu\text{s}$
$V_{PP}\uparrow$ set time from $V_{DD}\uparrow$	$t_{DRPSR}$	$V_{PP}$ high voltage	1.0			$\mu\text{s}$
$\overline{\text{RESET}}$ set time from $V_{PP}\uparrow$	$t_{PSRRF}$	$V_{PP}$ high voltage	1.0			$\mu\text{s}$
$V_{PP}$ count start time from $\overline{\text{RESET}}\uparrow$	$t_{RFCF}$		1.0			$\mu\text{s}$
Count execution time	$t_{COUNT}$				2.0	ms
$V_{PP}$ counter high-/low-level width	$t_{CH}, t_{CL}$		8.0			$\mu\text{s}$
$V_{PP}$ counter noise elimination width	$t_{NFW}$			40		ns

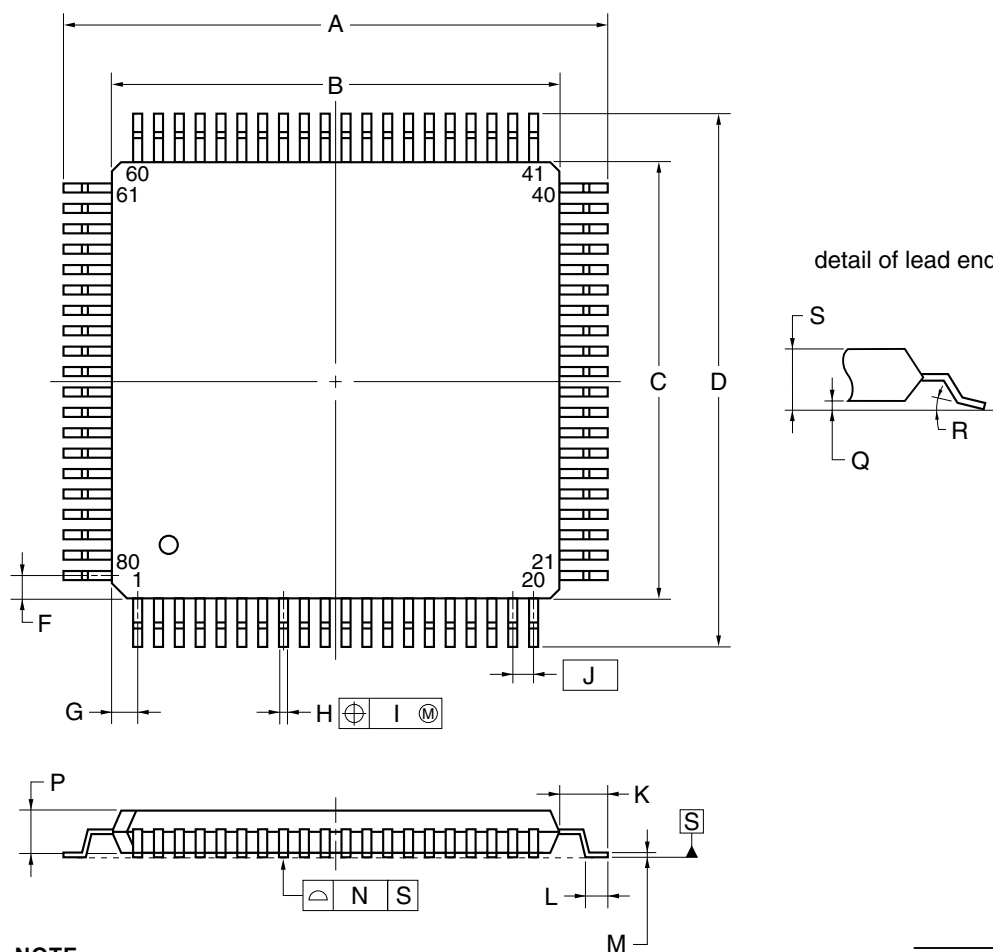
# Flash Write Mode Setting Timing





# 8. PACKAGE DRAWING

## 80-PIN PLASTIC QFP (14x14)



### NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	3° <sup>+7°</sup> <sub>-3°</sub>
S	1.70 MAX.

P80GC-65-8BT-1

## ★ 9. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

**Table 9-1. Surface Mounting Type Soldering Conditions**

- $\mu$ PD78F0703AYGC-8BT: 80-pin plastic QFP (14 x 14)
- $\mu$ PD78F0703AYGC(A)-8BT: 80-pin plastic QFP (14 x 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin low)	—

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution** Do not use different soldering methods together(except for partial heating).

## APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780703AY Subseries. Also refer to **(6) Cautions on Using Development Tools**.

### (1) Software Package

SP78K0	Software Package common to 78K/0 Series
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### (2) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780703Y	Device file for μPD780703AY Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

### (3) Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3, PG-FP3), Flashpro IV (Part No. FL-PR4, PG-FP4),	Dedicated flash programmer for microcomputers incorporating flash memory
FA-80GC	Adapter for flash memory writing used with connected to Flashpro III. 80-pin plastic QFP (GC-8BT type).

### (4) Debugging Tools

IE-78K0-NS(-A)	In-circuit emulator common to 78K/0 Series
IE-78K0-NS-PA	Performance board to enhance/expand functions of IE-78K0-NS
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter necessary when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable necessary when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter necessary when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using personal computer incorporating PCI bus as host machine
IE-780701-NS-EM1	Emulation board to emulate μPD780703AY Subseries
NP-80GC-TQ	Emulation probe for 80-pin plastic QFP (GC-8BT type)
NQPACK080SB	Socket for soldering on the target
YQPACK080SB	Adapter socket for connecting the probe to the NQPACK080SB
HQPACK080SB	Lid socket for connecting the device to the NQPACK080SB
YQSOCKET080SBF	Height adapter between the YQPACK080SB and the probe
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780703	Device file for μPD780703AY Subseries

(5) Real-time OS

RX78K0	Real-time OS for 78K/0 Series
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(6) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780703Y.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780703Y.
- The FL-PR3, FL-PR4, FA-80GC, and NP-80GC-TQ are products made by Naitou Densai Machidaseisakusho Co., Ltd. (TEL +81-45-475-4191).
- For third party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machine and OS suitable for each software are as follows:

Host Machine [OS]  Software	PC	EWS
	PC-9800 series [Japanese Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√ <sup>Note</sup>	√
CC78K0	√ <sup>Note</sup>	√
ID78K0-NS	√	—
ID78K0	√	—
SM78K0	√	—
RX78K0	√ <sup>Note</sup>	√

**Note** DOS-based software

## ★ APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

### • Documents Related to Devices

Document Name	Document No.
μPD780703Y Subseries User's Manual	U15568E
μPD780703Y, 780703Y(A) Data Sheet	U15344E
μPD780703AY, 780703AY(A) Data Sheet	U16539E
μPD78F0703Y, 78F0703Y(A) Data Sheet	U15345E
μPD78F0703AY, 78F0703AY(A) Data Sheet	This document
78K/0 Series User's Manual Instructions	U12326E

### • Documents Related to Development Software Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later	Operation (Windows Based)	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K Series Integrated Debugger Ver. 2.30 or Later	Operation (Windows Based)	U15185E
RX78K0 Real-Time OS	Fundamentals	U11537E
	Installation	U11536E
Project Manager Ver. 3.12 or Later (Windows Based)		U14610E

**Caution** The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

- Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0-NS In-Circuit Emulator	U13731E
IE-78K0-NS-A In-Circuit Emulator	U14889E
IE-78K0-NS-PA Performance Board	U16109E
IE-780701-NS-EM1	To be prepared

- Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer	U13502E
PG-FP4 Flash Memory Programmer	U15260E

- Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	<b>Note</b>
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

**Note** See the "Semiconductor Device Mount Manual" website.(<http://www.necel.com/pkg/en/mount/index.html>)

**Caution** The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[ MEMO ]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V<sub>DD</sub> or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

### [GLOBAL SUPPORT]

<http://www.necel.com/en/support/support.html>

#### NEC Electronics America, Inc. (U.S.)

Santa Clara, California  
Tel: 408-588-6000  
800-366-9782

#### NEC Electronics (Europe) GmbH

Duesseldorf, Germany  
Tel: 0211-65 03 01

- **Sucursal en España**  
Madrid, Spain  
Tel: 091-504 27 87
- **Succursale Française**  
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Tel: 01-30-67 58 00
- **Filiale Italiana**  
Milano, Italy  
Tel: 02-66 75 41
- **Branch The Netherlands**  
Eindhoven, The Netherlands  
Tel: 040-244 58 45
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Taeby, Sweden  
Tel: 08-63 80 820
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Taipei, Taiwan  
Tel: 02-2719-2377

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Tel: 6253-8311

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