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April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD78243, 78244

8-BIT SINGLE-CHIP MICROCOMPUTER

The information in this document is subject to change without notice.

Document No. IC-2774C
(O. D. No. IC-8070C)
Date Published February 1994 P
Printed in Japan


Phase-out/Discontinued

The uPD78243, 78244 is one of the 78K/II series products containing 512-byte EEPROM (electrically erasable programmable read-only memory). The 78K/II series provides 8-bit single chip microcomputers where 1M-byte memory space can be accessed by external expansion.

Please refer to the following User's Manual for details of functions explanation. Be sure to read the manual when starting design.

- uPD78244 Series User's Manual/Hardware: IEU-747
- 78K/II Series User's Manual/Instructions: IEU-754

FEATURES

o Pins are compatible with the uPD78213, 78214 pins

o High speed instruction execution (during 12-MHz operation):
333 ns (uPD78244), 500 ns (uPD78243)

o Internal EEPROM: 512 bytes (data memory area)
→ Automatic erasion and write function

o High performance interrupt controller

o A/D converter (8 bits x 8 channels)

o Number of I/O pins: 54 (uPD78244), 36 (uPD78243)

o Real-time output port (8 x 1 or 4 x 2)

o Serial interface: Two channels

o Timer/counter (16 x 1 and 8 x 3)

APPLICATIONS

Printers, Typewriters, Cameras, PPCs, FAXs, etc.

ORDERING INFORMATION

Ordering code	Package	Internal ROM	Internal RAM
uPD78243CW	64-pin plastic shrinked-dual in-line package (750 mil)	None	512
uPD78243GC-AB8	64-pin plastic quad-flat package (□ 14mm)	None	512
uPD78244CW-xxx	64-pin plastic shrinked-dual in-line package (750 mil)	16K	512
uPD78244GC-xxx-AB8	64-pin plastic quad-flat package (□ 14mm)	16K	512

Remarks: xxx is ROM code specification number.

QUALITY GRADE

Standard

Refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-620) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Function List

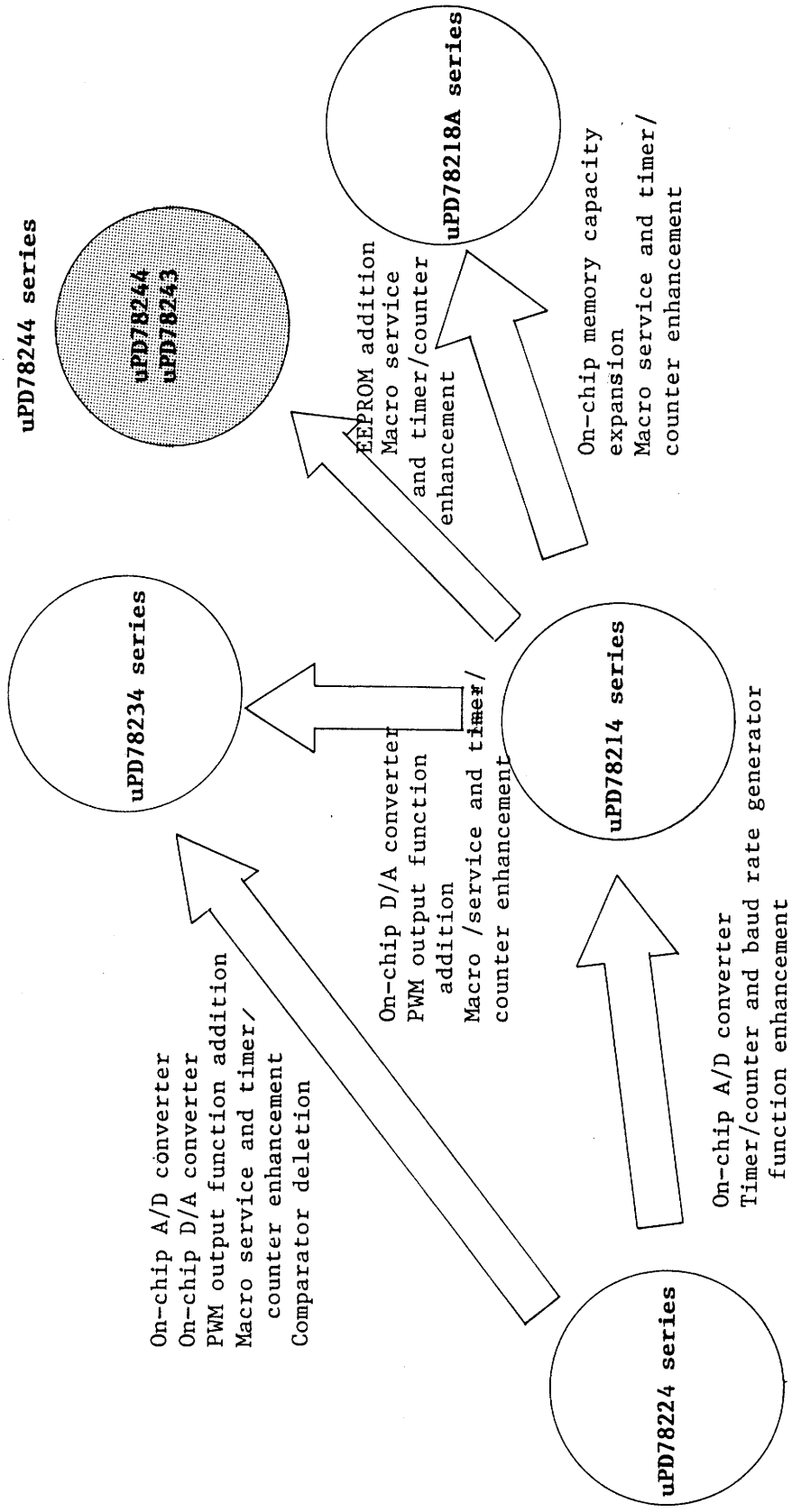
(1/2)

Parameter		uPD78243	uPD78244
No. of basic instructions (mnemonics)		65	
Minimum instruction execution time (during 12-MHz operation)		500ns	333ns
On-chip memory capacity	Mask ROM	None	16K bytes
	EEPROM	512 bytes	
	RAM	512 bytes	
Memory space		Program: 64K bytes Data: 1M bytes	
Number of I/O pins	Input	14	
	Output	12	
	Input/output	10	28
	Total	36	54
(Note) Pins with additional function	Pins with pull-up resistor	16	34
	LED direct drive output	—	16
	Transistor direct drive output	8	
ROMless mode setting		None	$\overline{EA}$ pin=low level
Real-time output port		4 bits x 2 or 8 bits x 1	
General purpose register		8 bits x 8 x 4 banks (memory mapping)	

Note: The pins with additional an function are contained in the I/O pins.

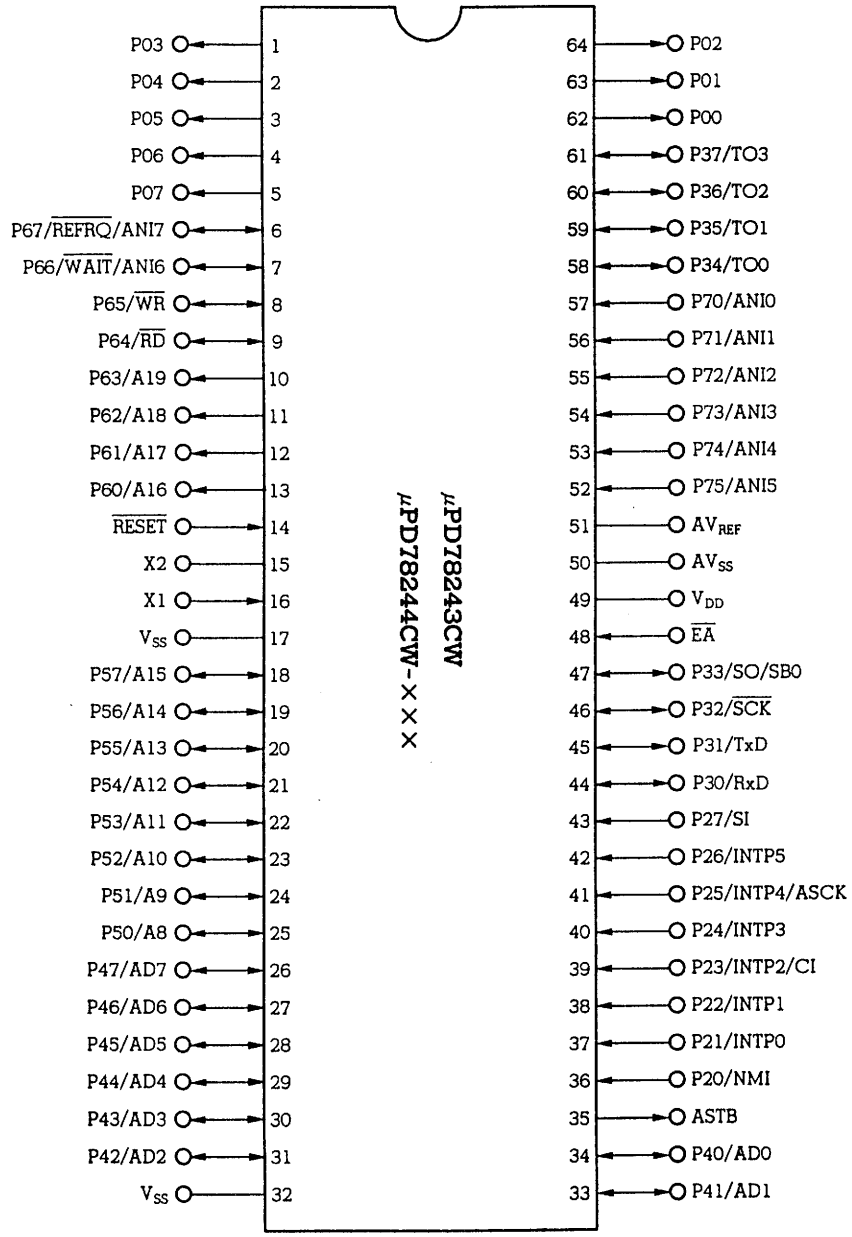
Parameter	Function		
Timer/counter	16-bit timer/counter	Timer register x 1 Capture register x 1 Compare register x 2	Pulse output enable (Toggle output PWM/PPG output One-shot pulse output)
	8-bit timer/counter 1	Timer register x 1 Capture/compare register x 1 Compare register x 1	Pulse output enable (real-time output: 4 bits x 2)
	8-bit timer/counter 2	Timer register x 1 Capture register x 1 Compare register x 2	Pulse output enable (Toggle output PWM/PPG output)
	8-bit timer/counter 3	Timer register x 1 Compare register x 1	
Serial interface	UART: One channel (containing a dedicated baud rate generator) CSI (3-line serial I/O, SBI): One channel		
A/D converter	8-bit resolution x 8 channels		
Interrupt	21 sources (seven external and 14 internal sources) + BRK instruction Two programmable priority levels Two processing modes (vectored interrupt and macro service)		
Instruction set	16-bit arithmetic and logical operation Multiplication and division (8 bits x 8 bits and 16 bits ÷ 8 bits) Bit manipulation BCD adjustment and others		
Package	64-pin plastic shrinked-dual-in-line package (750mil) 64-pin plastic quad-flat package (□ 14 mm)		

78K/II Product Development Chart



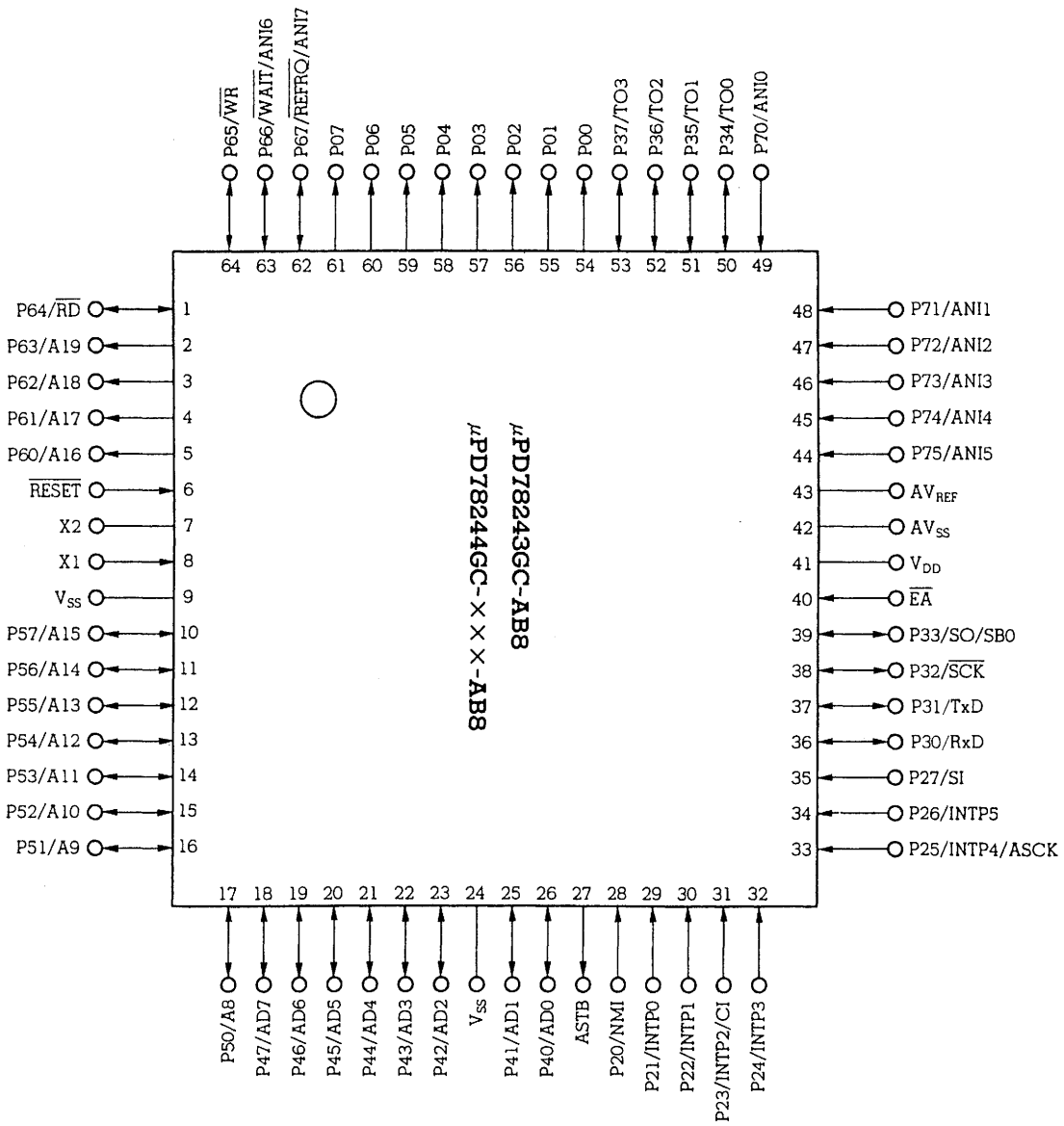
Pin Configuration (Top View)

64-pin plastic shrinked-dual-in-line package (750mil)



Remarks: The pins are compatible with the uPD78213CW, 78214CW pins.

64-pin plastic quad-flat package (□ 14mm)

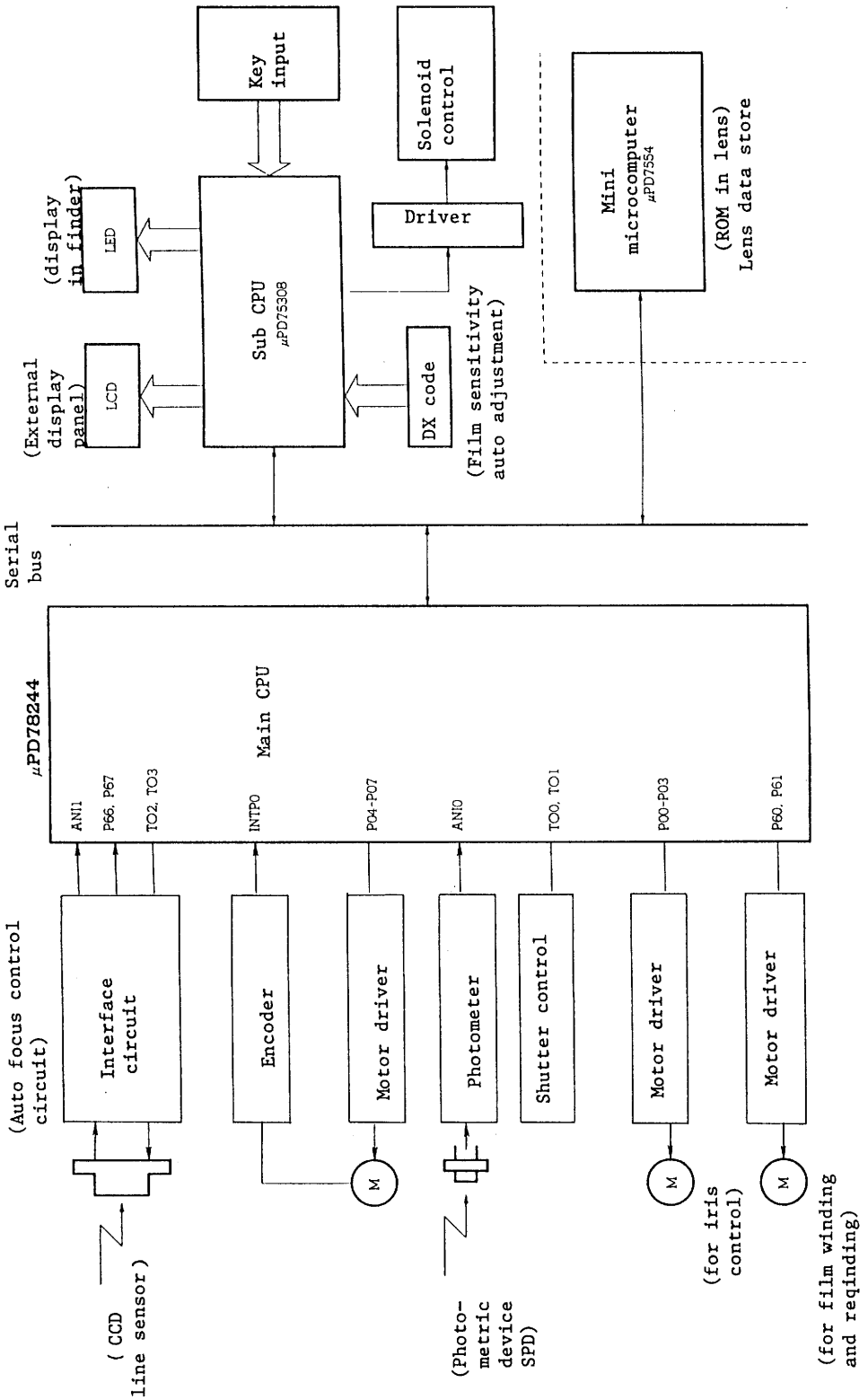


Remarks: The pins are compatible with the uPD78213GC, 78214GC pins.

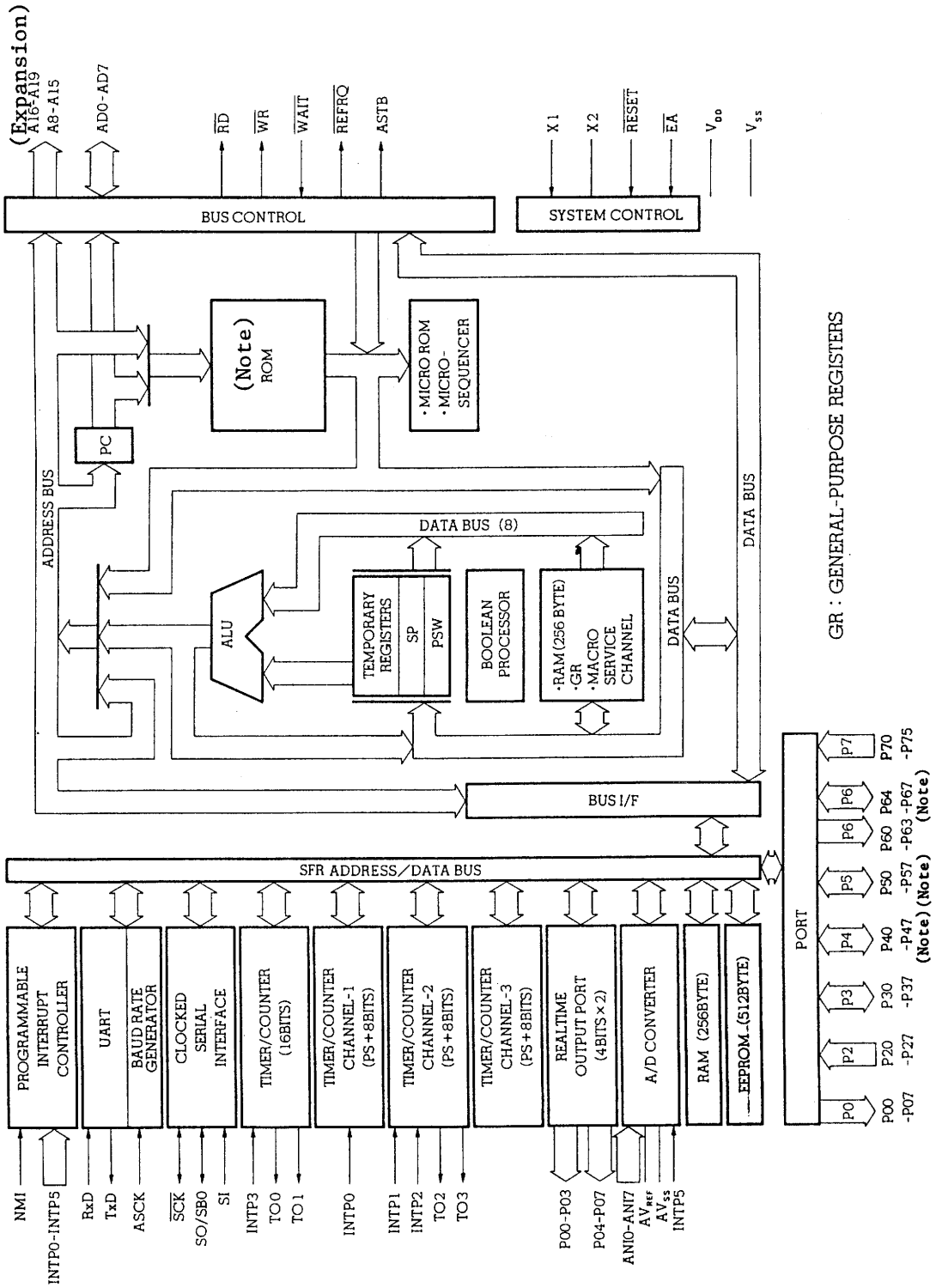
P00-P07	:	Port 0
P20-P27	:	Port 2
P30-P37	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P60-P67	:	Port 6
P70-P75	:	Port 7
TO0-TO3	:	Timer Output
CI	:	Clock Input
RxD	:	Receive Data
TxD	:	Transmit Data
$\overline{SCK}$	:	Serial Clock
ASCK	:	Asynchronous Serial Clock
SB0	:	Serial Bus
SI	:	Serial Input
SO	:	Serial Output
NMI	:	Non-maskable Interrupt
INTP0-INTP5	:	Interrupt From Peripherals
AD0-AD7	:	Address/Data Bus
A8-A19	:	Address Bus

$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
$\overline{REFRQ}$	:	Refresh Request
$\overline{RESET}$	:	Reset
X1, X2	:	Crystal
$\overline{EA}$	:	External Access
ANI0-ANI7	:	Analog Input
AV_{REF}	:	Reference Voltage
AV_{SS}	:	Analog Ground
V_{DD}	:	Power Supply
V_{SS}	:	Ground

System Configuration Example (auto focus single-lens reflex camera)



Internal Block Diagram



Note: uPD78243 does not contain internal ROM and P40-P47, P50-P57, P64 and P65.

CONTENTS

1. PIN FUNCTION

1.1 Ports (1/2)

Pin name	I/O	Dual function pin	Function
P00-P07	O	——	Port 0 (P0): Can be used as two 4-bit real-time output ports. Can drive transistors directly.
P20	I	NMI	Port 2 (P2): P20 cannot be used as a general purpose port pin (nonmaskable interrupt), but the input level can be checked by the interrupt routine. Internal pull-up resistor connection can be specified for P22-P27 in a batch (six bits) by software.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK	
P26		INTP5	
P27		SI	
P30	I/O	RxD	Port 3 (P3): The input/output mode can be specified bit-wise. Internal pull-up resistor connection can be specified bit-wise.
P31		TxD	
P32		$\overline{SCK}$	
P33		SO/SB0	
P34-P37		TO0-TO3	
(Note) P40-P47	I/O	AD0-AD7	Port 4 (P4) The input/output mode can be specified for eight bits in a batch. For P40-P47 in input mode, connection of internal pull-up resistor can be specified in batch by software. The port can drive LEDs directly.

Note: With the uPD78243, P40-P47, P50-P57, P64, and P65 cannot be used as ports.

1.1 Ports (2/2)

Pin name	I/O	Dual function pin	Function
(Note) P50-P57	I/O	A8-A15	Port 5 (P5): The input/output mode can be specified bit-wise. For P50-P57 in input mode, connection of internal pull-up resistor can be specified in batch by software. The port can drive LEDs directly.
P60-P63	O	A16-A19	Port 6 (P6): The input/output mode can be specified for P64-P67 bit-wise. Internal pull-up resistor connection can be specified for P64-P67 bit-wise.
P64(Note)	I/O	$\overline{RD}$	
P65(Note)		$\overline{WR}$	
P66		$\overline{WAIT}$/ANI6	
P67		$\overline{REFRQ}$/ANI7	
P70-P75	I	ANI0-ANI5	Port 7 (P7)

Note: With the uPD78243, P40-P47, P50-P57, P64, and P65 cannot be used as ports.

1.2 Pins other than Ports (1/2)

Pin name	I/O	Function	Dual function pin
TO0-TO3	O	Timer output	P34-P37
CI	I	Count clock input to 8-bit timer/counter 2	P23/INTP2
RxD	I	Serial data input (UART)	P30
TxD	O	Serial data output (UART)	P31
ASCK	I	Baud rate clock input (UART)	P25/INTP4
SB0	I/O	Serial data input/output (SBI)	P33/SO
SI	I	Serial data input (3-line serial I/O)	P27
SO	O	Serial data output (3-line serial I/O)	P33/SB0
$\overline{SCK}$	I/O	Serial clock input/output (SBI, 3-line serial I/O)	P32
NMI	I	External interrupt requests	P20
INTP0			P21
INTP1			P22
INTP2			P23/CI
INTP3			P24
INTP4			P25/ASCK
INTP5			P26

1.2 Pins other than Ports (2/2)

Pin name	I/O	Function	Dual function pin
AD0-AD7	I/O	Time-multiplexed address/data bus (external memory connection)	(Note) P40-P47
A8-A15	O	High-order address bus (external memory connection)	(Note) P50-P57
A16-A19	O	High-order address in address extension (external memory connection)	P60-P63
$\overline{RD}$	O	Read strobe to external memory	P64(Note)
$\overline{WR}$	O	Write strobe to external memory	P65(Note)
$\overline{WAIT}$	I	Wait insertion	P66/ANI6
ASTB	O	Address (A0-A7) latch timing output (when external memory is accessed)	–
$\overline{REFRQ}$	O	Refresh pulse output to external psudo-static memory	P67/ANI7
$\overline{RESET}$	I	Chip reset	–
X1	I	Crystal input for system clock oscillation (clock can also be input to X1)	–
X2	–		
$\overline{EA}$	I	ROMless operation indication (external access to the same space as internal ROM). With the uPD78244, set the $\overline{EA}$ pin high for use and with the uPD78243, set the $\overline{EA}$ pin low for use.	–
ANI0-ANI5	I	A/D converter analog voltage input	P70-P75
ANI6, ANI7			P66/$\overline{WAIT}$ P67/$\overline{REFRQ}$
AV_{REF}	–	A/D converter reference voltage application	–
AV_{SS}		A/D converter GND	–
V_{DD}		Positive power supply pin	
V_{SS}		GND pin	

Note: With the uPD78243, P40-P47, P50-P57, P64, and P65 cannot be used as ports.

1.3 Input/Output Circuits and Treatment of Unused Pins

Table 1-1 lists the pin input/output circuit types and the recommended conditions for unused pins. Fig. 1-1 shows the input/output circuit types.

Table 1-1 Pin Input/Output Circuit Types and Recommended Conditions for Unused Pins (1/2)

Pin	I/O circuit type	I/O	Recommended conditions for unused pins
P00-P07	4	O	No connection required
P20/NMI	2	I	Conenct to V_{DD} or V_{SS}
P21/INTP0			
P22/INTP1	2-A		Connect to V_{DD}
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK			
P26/INTP5			
P27/SI			
P30/RxD	5-A	I/O	Input : Conenct to V_{DD}. Output: Not connection required.
P31/TxD			
P32/$\overline{SCK}$	8-A		
P33/SB0/SO	10-A		
P34/TO0-P37/TO3	5-A		
P40/AD0-P47-AD7			
P50/A8-P57/A15			

Table 1-1 Pin Input/Output Circuit Types and Recommended Conditions for Unused Pins (2/2)

Pin	I/O circuit type	I/O	Recommended conditions for unused pins
P60/A16-P63/A19	4	O	No connection required
P64/$\overline{RD}$	5-A	I/O	Input : Connect to V_{DD} Output: No connection required
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/ANI6	11		Input : Connect to V_{DD} Output: No conenction required
P67/$\overline{REFRQ}$/ANI7			
P70/ANI0-P75/ANI5	9	I	Connect to V_{SS}
ASTB	4	O	No connection required
$\overline{RESET}$	2	I	—
$\overline{EA}$	1		
AV_{REF}	—		Connect to V_{SS} or V_{DD}
AV_{SS}			Connect to V_{SS}

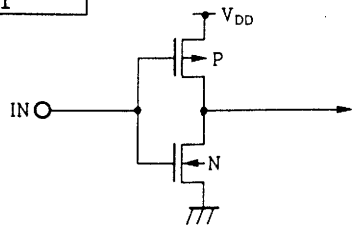
Note: When A/D conversion operation is being performed, do not apply any voltage outside the AV_{SS}-AV_{REF} range. The uPD78243, 78244 may be destroyed.

Caution: If the dual function pins used for both input and output mode is not defined, connect the pins to V_{DD} via serveral tens kΩ resistors (particularly when the reset input pin voltage exceeds the input low voltage when the power is turned on or when the input and output modes are changed by software.)

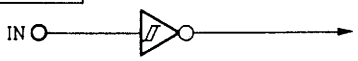
Remarks: The type numbers are standardized in the 78K series and are not necessarily serial numbers in each product (some circuit types are not contained).

Fig. 1-1 Pin Input/Output Circuits

Type 1

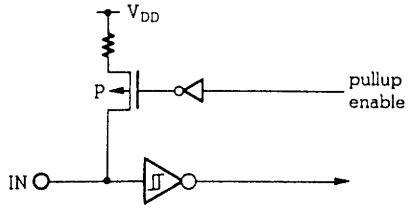


Type 2



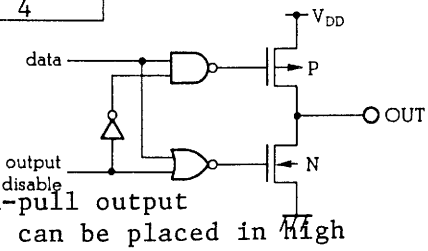
Schmitt trigger input having hysteresis characteristics.

Type 2-A



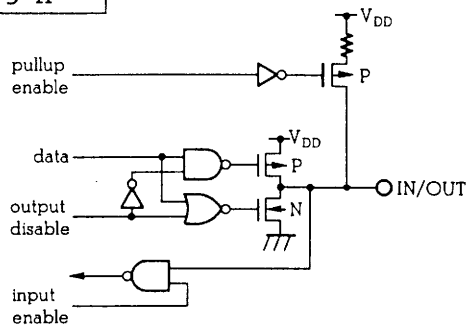
Schmitt trigger input having hysteresis characteristics.

Type 4

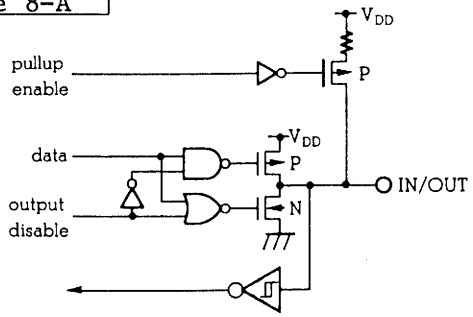


Push-pull output that can be placed in high impedence(both P-ch and N-ch off).

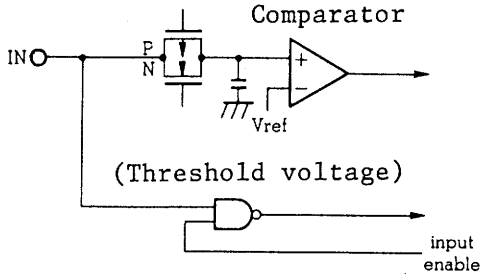
Type 5-A



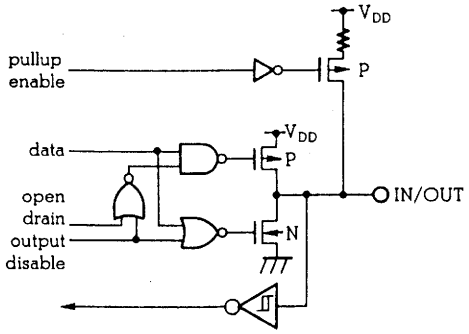
Type 8-A



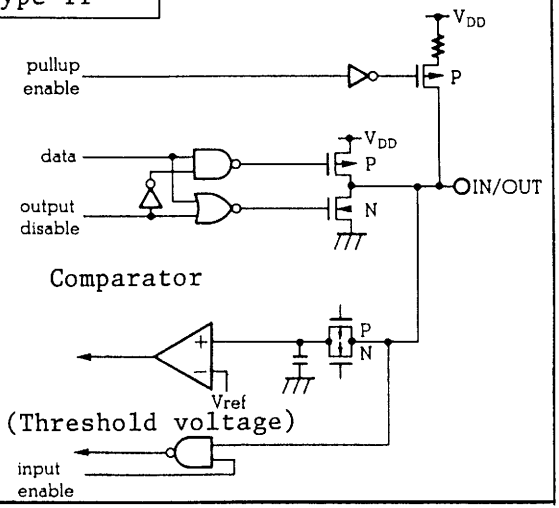
Type 9



Type 10-A



Type 11



2. INTERNAL BLOCK FUNCTION

2.1 Memory Space

The 1M-byte memory space can be accessed. Fig. 2-1 shows a memory map. Mapping the program memory varies depending on the state of the $\overline{EA}$ pin. The uPD78243 is used with $\overline{EA}$=L.

(1) uPD78243

The program memory is mapped in external memory (64256 bytes; 00000H-0FAFFH). This area can also be shared with the data memory.

The data memory consists of an internal EEPROM and an internal RAM.

The internal EEPROM area has a capacity of 512 bytes and is mapped in 0FB00H-0FCFFH.

The internal RAM also has a capacity of 512 bytes and is mapped in 0FD00H-0FEFFH.

In the 1M-byte extension mode, external memory (960K bytes, 10000H-FFFFFH) can be mapped as an extended data memory.

(2) uPD78244

The program memory is mapped in the 16K-byte internal ROM (00000H-03FFFH) and 47872-byte external memory (04000H-0FAFFH). The external memory is accessed in the external memory expansion mode. The area mapped in the external memory can also be used as data memory.

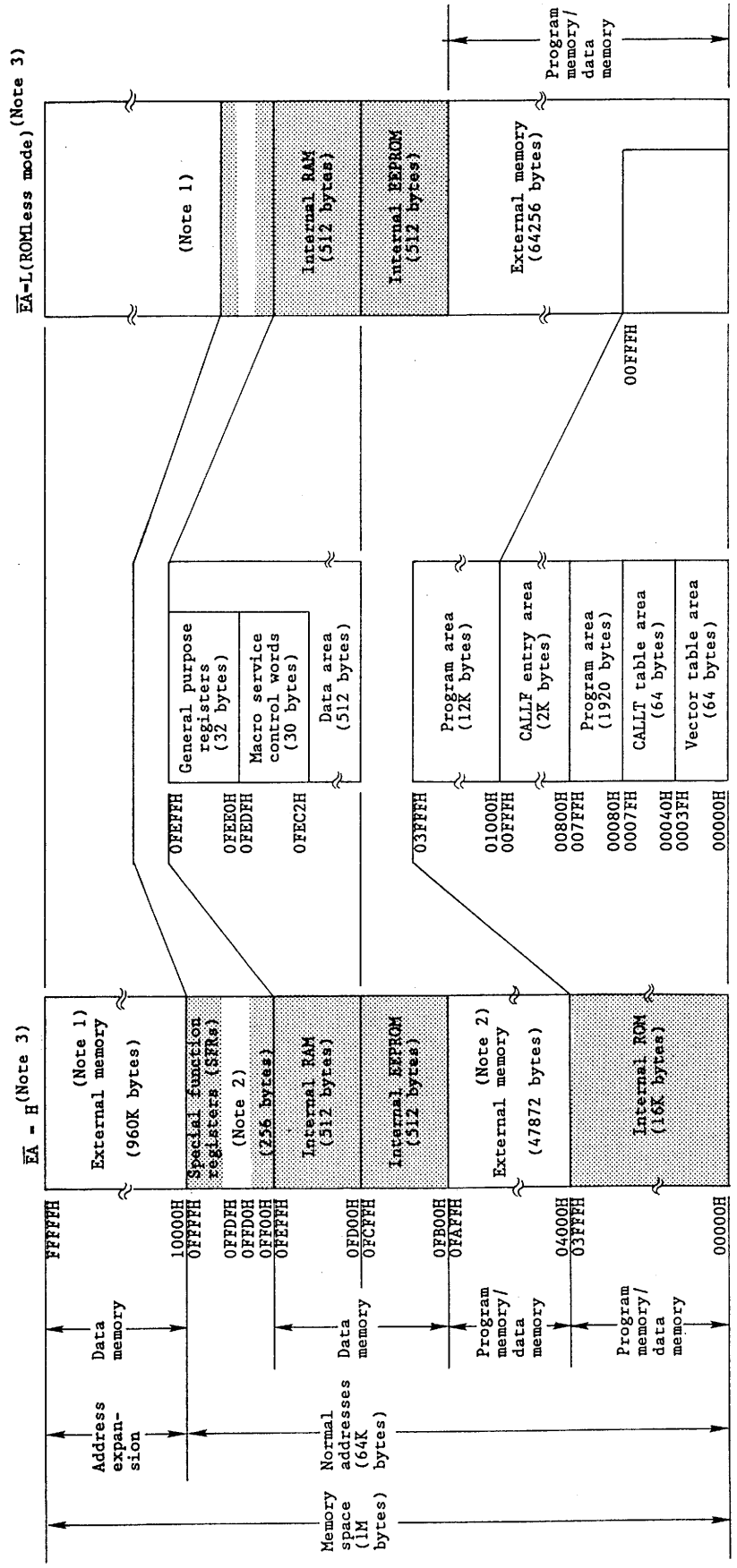
The data memory consists of internal EEPROM and internal RAM.

The internal EEPROM area has a 512-byte capacity and is mapped in 0FB00H-0FCFFH.

The internal RAM also has a 512-byte capacity and is mapped in 0FD00H-0FEFFH.

In the 1M-byte expansion mode, the 960K-byte external memory (10000H-FFFFFH) can be mapped as data memory expansion.

Fig. 2-1 Memory Map



Note 1: External memory is accessed in the 1M-byte expansion mode.

2: External memory is accessed in the external memory expansion mode.

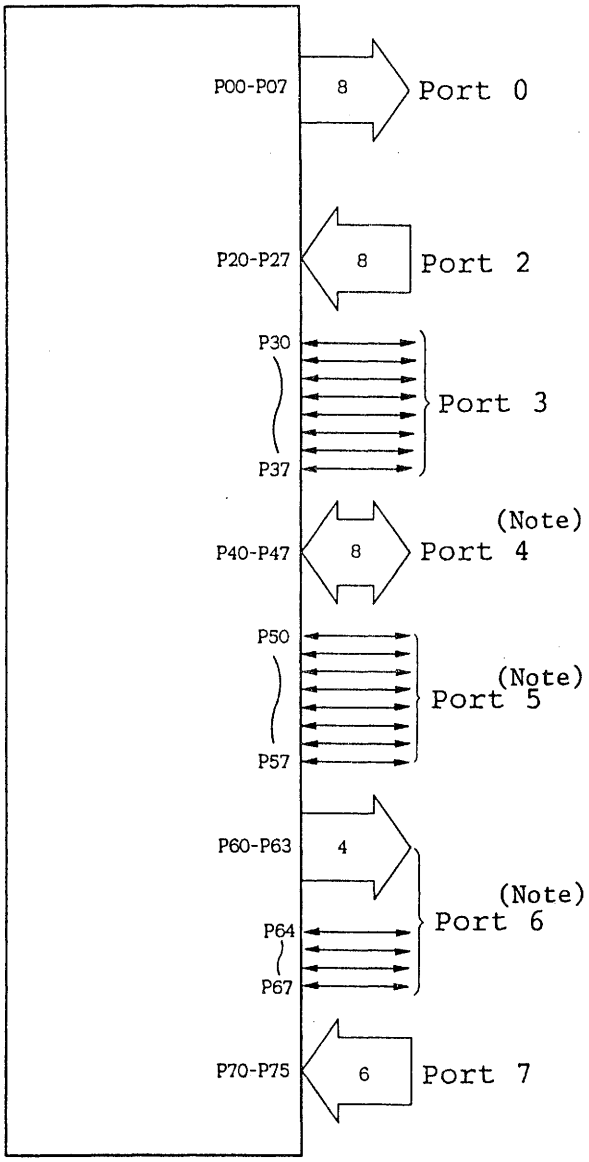
: Internal memory

3: The uPD78243 can only be used with $\overline{EA}$=L. The uPD78243 cannot be used with $\overline{EA}$=H.

2.2 Ports

The uPD78243, 78244 contains the ports as shown in Fig. 2-2 for various control purposes. Table 2-1 lists the port function. On-chip pull-up resistor connection can be specified for ports 2 to 6 in the input mode by software.

Fig. 2-2 Port Configuration



Note: With the uPD78243, P40-P47, P50-P57, P64, and P65 cannot be used as ports.

Table 2-1 Port Configuration

Name	Pin name	Function	Software pull-up specification
Port 0	P00-P07	Output mode or high impedance can be specified for eight bits in a batch. Port 0 can also operate as 4-bit real time output (P00-P03 and P04-P07). The port can drive transistors directly.	—
Port 2	P20-P27	Input port.	Six bits in a batch (P22-P27)
Port 3	P30-P37	Input or output mode can be specified bit-wise.	Input mode pins can be specified in a batch.
(Note) Port 4	P40-P47	Input or output mode can be specified for eight bits in a batch. The port can drive LED directly.	Eight bits in a batch
(Note) Port 5	P50-P57	Input or output mode can be specified bit-wise. The port can drive LEDs directly.	Input mode pins can be specified in a batch.
(Note) Port 6	P60-P63	Output port.	—
	P64-P67	Input or output mode can be specified bit-wise.	Input mode pins can be specified in a batch.
Port 7	P70-P75	Input port.	—

Note: With the uPD78243, P40-P47, P50-P57, P64, and P65 cannot be used as ports.

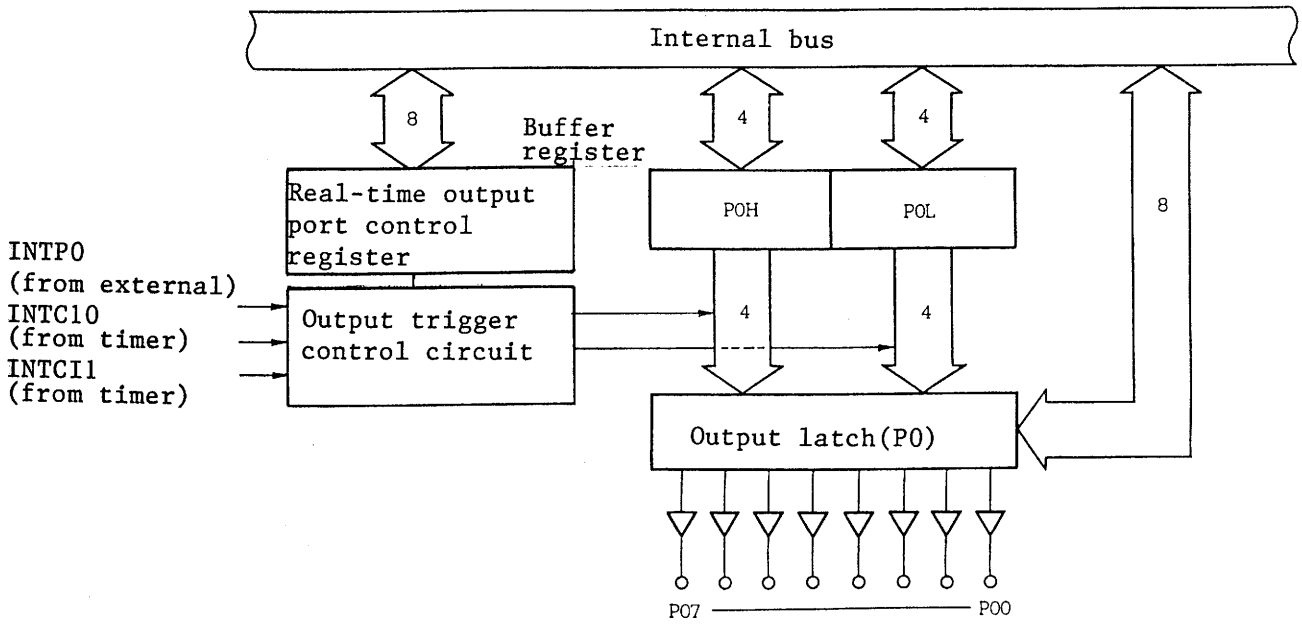
2.3 Real-Time Output Port

The real-time output port outputs data stored in a buffer in synchronization with a timer match interrupt or external interrupt to provide pulse output with no jitter.

Thus, it is appropriate for application to output any desired pattern at any desired intervals, such as open loop control of a stepping motor.

The real-time output port consists mainly of port 0 and a buffer register, as shown in Fig. 2-3.

Fig. 2-3 Real Time Output Port Block Diagram



2.4 Timer/Counter Units

One channel of the 16-bit timer/counter unit and three channels of the 8-bit timer/counter unit are contained.

Table 2-2 Timer/Counter Types and Function

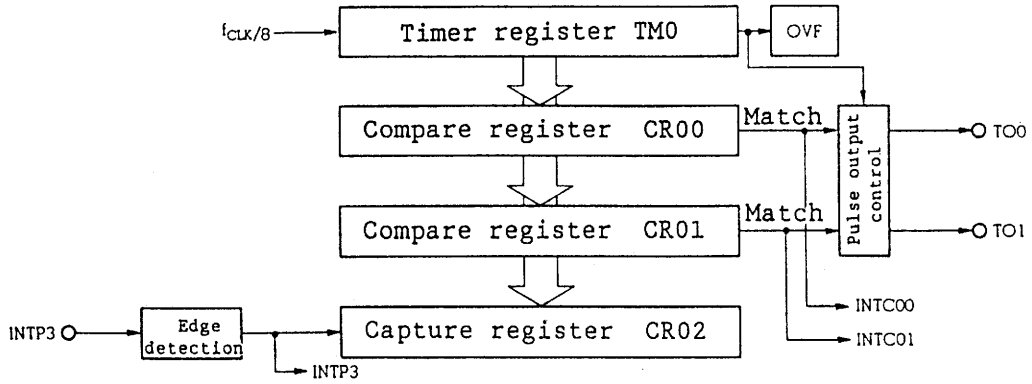
Type and function \ Unit		16-bit timer/counter	8-bit timer/counter1	8-bit timer/counter2	8-bit timer/counter3
Type	Interval timer	Two channels	Two channels	Two channels	One channel
	External event counter	-	-	o	-
	One-shot timer(Note)	-	-	o	-
Function	Timer output	Two channels	-	Two channels	-
	Toggle output	o	-	o	-
	PWM/PPG output	o	-	o	-
	One-shot pulse output(Note)	o	-	o	-
	Real-time output	-	o	-	-
	Pulse width measurement	o	o	o	-
	Number of interrupt requests	2	2	2	1
	Serial interface clock source	-	-	-	o

Note: Only 8-bit timer/counter 2 has the one-shot timer mode. The function of this mode differs from the 16-bit timer/counter one-shot pulse output function. Thus, the 16-bit timer/counter does not have the one-shot timer mode. The 16-bit timer/counter one-shot pulse output function is added from the uPD78213, 78214.

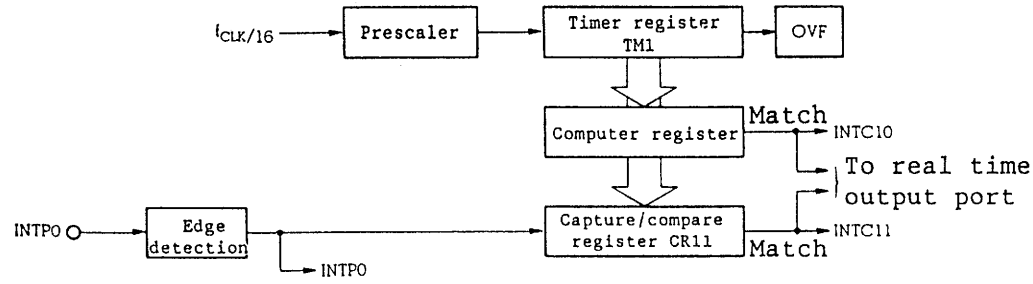
The timer/counter units support a total of seven interrupt requests, thus can be served as timers of seven channels.

Fig. 2-4 Timer/Counter Unit Block Diagram

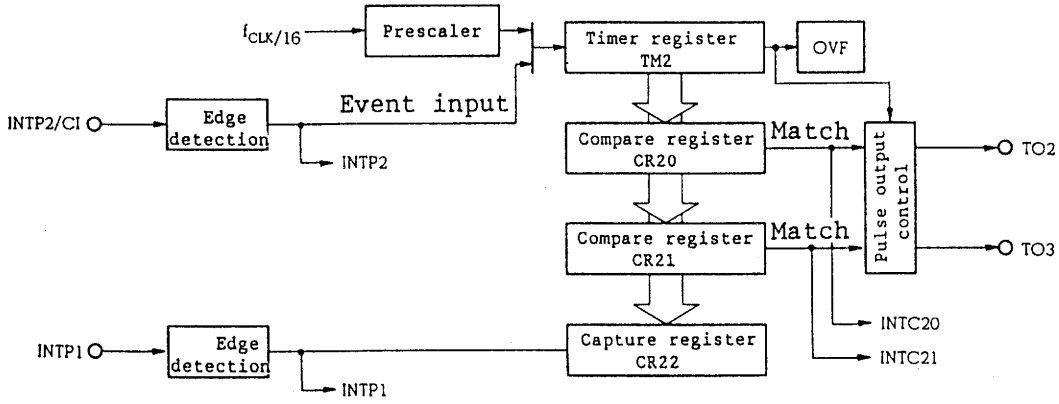
● 16-bit timer/counter unit



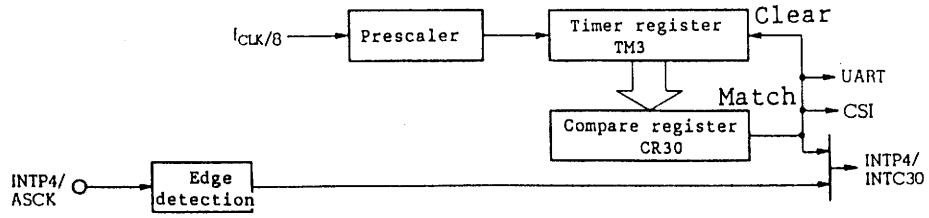
● 8-bit timer/counter unit 1



● 8-bit timer/counter unit 2



● 8-bit timer/counter unit 3



OVF: Overflow flag

2.5 A/D Converter

An analog/digital (A/D) converter which has eight multiplexed analog inputs (ANI0-ANI7) is contained.

The conversion system is successive approximation and the conversion result is retained in an 8-bit A/D conversion result register (ADCR). Thus, high-speed and high-precision conversion is made (the conversion time is about 30 us during 12-MHz operation).

A/D conversion operation is started in either of the following modes:

- o Hardware start: Conversion is started by trigger input (INTP5).
- o Software start: Conversion is started by setting a specific A/D converter mode register (ADM) bit.

After being started, the A/D conversion operation

- o Scan mode : More than one analog input is selected in sequence and conversion data from all pins is provided.

- o Select mode: Analog input is fixed to one pin and consecutive conversion value is provided.

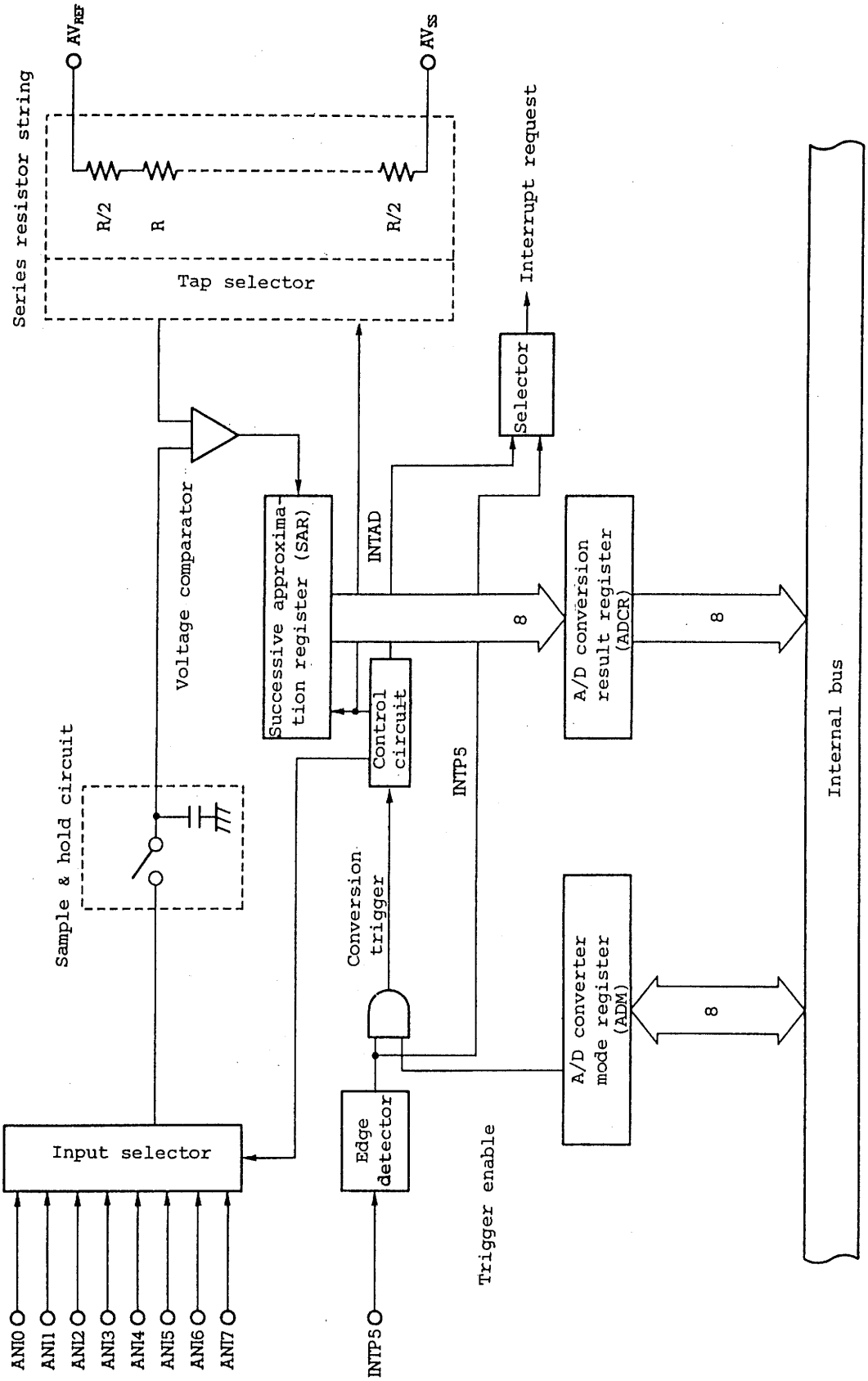
The modes and conversion operation stop are all specified in the ADM.

When the conversion result is transferred to the ADCR, interrupt request INTAD is generated (except in the select mode with software start). Thus, the conversion value can be transferred consecutively to memory by macro service.

Table 2-3 Modes Causing INTAD to Occur

	Scan mode	Select mode
Hardware start	o	o
Software start	o	-

Fig. 2-5 A/D Converter Block Diagram



2.6 Serial Interface

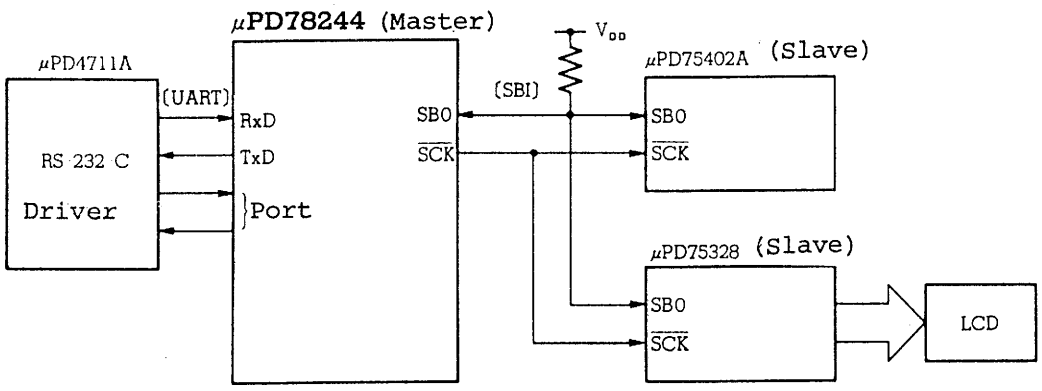
Two independent serial interface channels are contained.

- o Asynchronous serial interface (UART)
- o Clocked serial interface (CSI)
  - 3-line serial I/O
  - Serial bus interface (SBI)

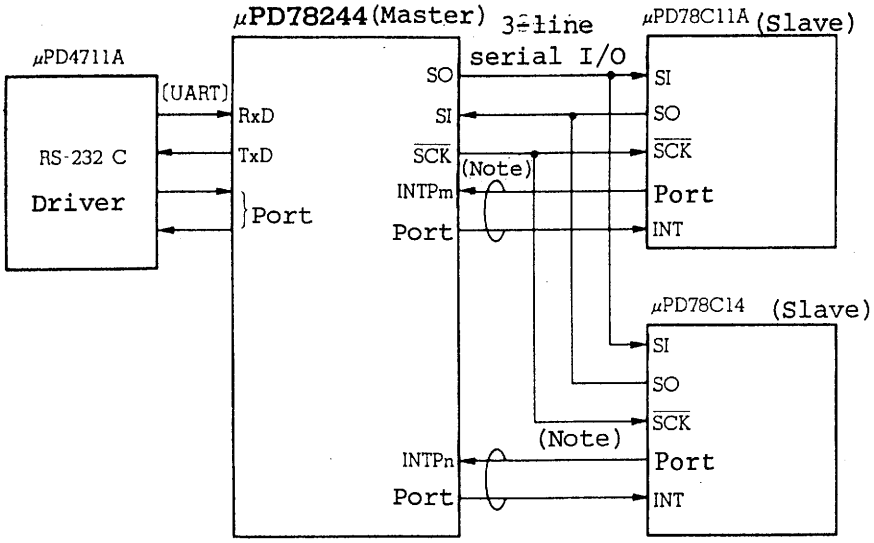
Thus, the uPD78243, 78244 can make communication with the system external and local communication in the system simultaneously (See Fig. 2-6).

Fig. 2-6 Serial Interface Example

(a) UART+SBI



(b) UART+3-line serial interface



Note: Handshaking lines

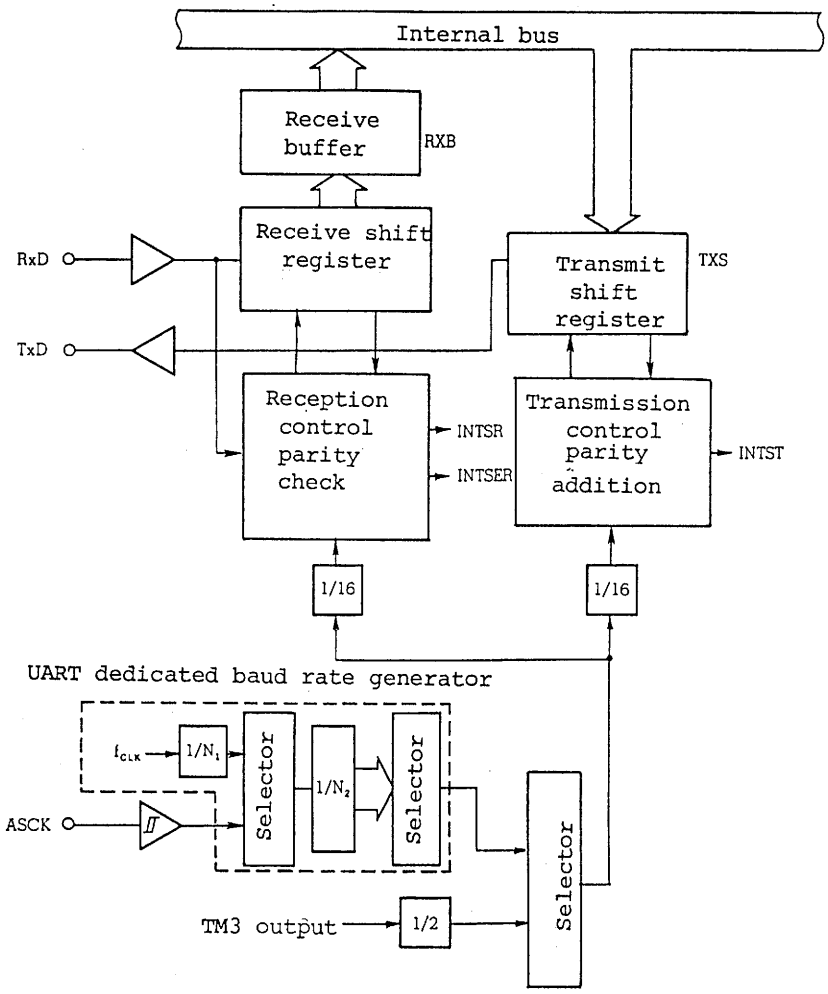
2.6.1 Asynchronous serial interface

The uPD78243, 78244 contains UART (Universal Asynchronous Receiver Transmitter) as an asynchronous serial interface where 1-byte data following a start bit is transmitted.

A baud rate generator dedicated to the UART is provided for communication covering a wide range of desired baud rates.
A baud rate can also be defined by dividing the input clock to the ASCK pin.

8-bit timer/counter 3 can also generate a baud rate.
The UART dedicated baud rate generator also provides the MIDI specification baud rate (31.25 kbps).

Fig. 2-7 Asynchronous Serial Interface Block Diagram

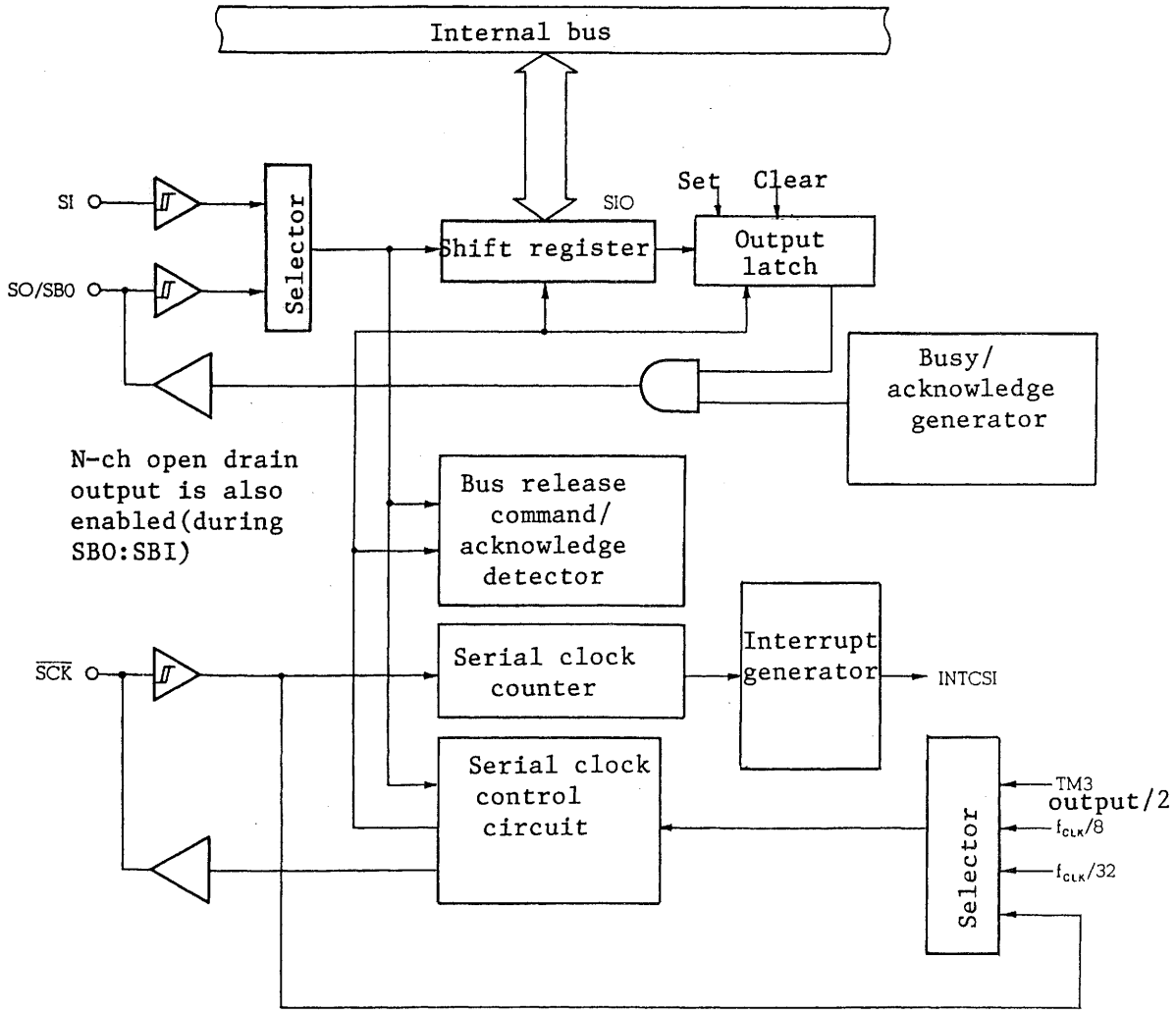


f_{CLK}: Internal system clock frequency (clock oscillation frequency/2)

2.6.2 Clocked serial interface

The master device activates serial clock and starts transmission. 1-byte data is transferred in synchronization with the serial clock.

Fig. 2-8 Clocked Serial Interface Block Diagram



f_{CLK}: Internal system clock frequency (clock oscillation frequency/2)

(1) 3-line serial I/O

The 3-line serial I/O is an interface for communication with a device containing the conventional clocked serial interface.

Basically, the three lines of serial clock ($\overline{SCK}$) and serial data (SI and SO) are used for communication. To connect the uPD78243, 78244 to a number of devices, handshaking lines are required.

(2) Serial bus interface (SBI)

The uPD78243, 78244 communicates with a number of devices on the two lines of serial clock ($\overline{SCK}$) and serial bus (SB0). The serial bus interface (SBI) is NEC format serial interface.

The master device outputs "address" from the SB0 pin to select the slave device to communicate with. Then, "command" and "data" are transferred between the master and slave.

2.7 EEPROM

512-byte EEPROM (Electrically Erasable Programmable Read-Only Memory) is contained in addition to 512-byte internal RAM as data memory. EEPROM can be read/written by a program. Unlike normal data memory, EEPROM can also retain data during power failure.

EEPROM is mapped in data memory space addresses 0FB00H-0FCFFH.

EEPROM contains a write dedicated timer. When data is written into EEPROM, the EEPROM contents are eased and the data is written automatically. The write operation is performed one byte at a time. The time required for the write is about 10 ms (about 5 ms of erasion time + about 5 ms of write time)

On-chip EEPROM read/write operation is performed in the same manner as on-chip RAM read/write operation. The memory contents can also be read during writing.

The following two interrupts occur from EEPROM:

(1) INTEPW (EEPROM write end interrupt)

Is an interrupt occurring when write into EEPROM is complete.

(2) INTEER (EEPROM write error interrupt)

Is an interrupt occurring when a write error into EEPROM occcurs.
The write error occurs in either of the following cases:

- When an EEPROM write instruction is executed during writing into EEPROM
- When EEPROM write is inhibited during writing into EEPROM

3. INTERNAL AND EXTERNAL CONTROL FUNCTION

3.1 Interrupts

Either of the interrupt request processing modes listed in Table 3-1 can be selected by a program.

Table 3-1 Interrupt Request Processing

Processing mode	Main part for processing	Processing	PC and PSW contents
Vectored interrupt	Software	Branch to service routine for execution (processing contents are as desired)	Saved and restored
Macro service	Firmware	Execution of data transfer between memory and I/O, etc., (processing contents are fixed)	Retained

3.1.1 Interrupt sources

The interrupt sources are seven external and 14 internal sources (21 totally) and BRK instruction execution, as listed in Table 3-2.

Two interrupt processing priority levels (high and low) can be set for nest control during interrupt processing and for discrimination between levels of interrupt requests occurring at a time. (See Fig. 3-1 and 3-2.) However, when a macro service is executed, interrupt requests are not pending and are always nested.

The default priorities are fixed processing priority levels of interrupt requests having the same priority level occurring at a time. (See Table 3-2.)

Table 3-2 Interrupt Sources (1/2)

Type	Default priority	Source		Internal/ external	Macro service
		Name	Trigger		
Software	—	BRK	Instruction execution	—	—
Nonmaskable		NMI	Pin input edge detection	External	
Maskable	0 (highest)	INTP0	" (TM1 capture trigger)		o
	1	INTP1	" (TM2 capture trigger)		
	2	INTP2	" (TM2 event counter input)		
	3	INTP3	" (TM0 capture trigger)		
	4	INTC00	TM0-CR00 match signal generation	Internal	
	5	INTC01	TM0-CR01 "		
	6	INTC10	TM1-CR10 "		
	7	INTC11	TM1-CR11 "		
	8	INTC21	TM2-CR21 "		
	9	INTP4	Pin input edge detection	External	
		INTC30	TM3-CR30 match signal generation	Internal	

Table 3-2 Interrupt Sources (2/2)

Type	Default priority	Source		Internal/ external	Macro service
		Name	Trigger		
Maskable	10	INTP5	Pin input edge detection	External	o
		INTAD	A/D converter conversion end (transfer to ADCR)	Internal	
	11	INTC20	TM2-CR20 match signal generation		
	12	INTSER	ASI reception error occurrence		-
	13	INTSR	ASI reception end		o
	14	INTST	ASI transmission end		
	15	INTCSI	CSI transfer end		
	16	INTEER	EEPROM write error occurrence		-
	17 (lowest)	INTEPW	EEPROM write completion		

TM0 : 16-bit timer
TM1-TM3: 8-bit timers
ASI : Asynchronous serial interface
CSI : Clocked serial interface

Fig. 3-1 Processing Example when Another Interrupt Request Occurs during Interrupt Processing

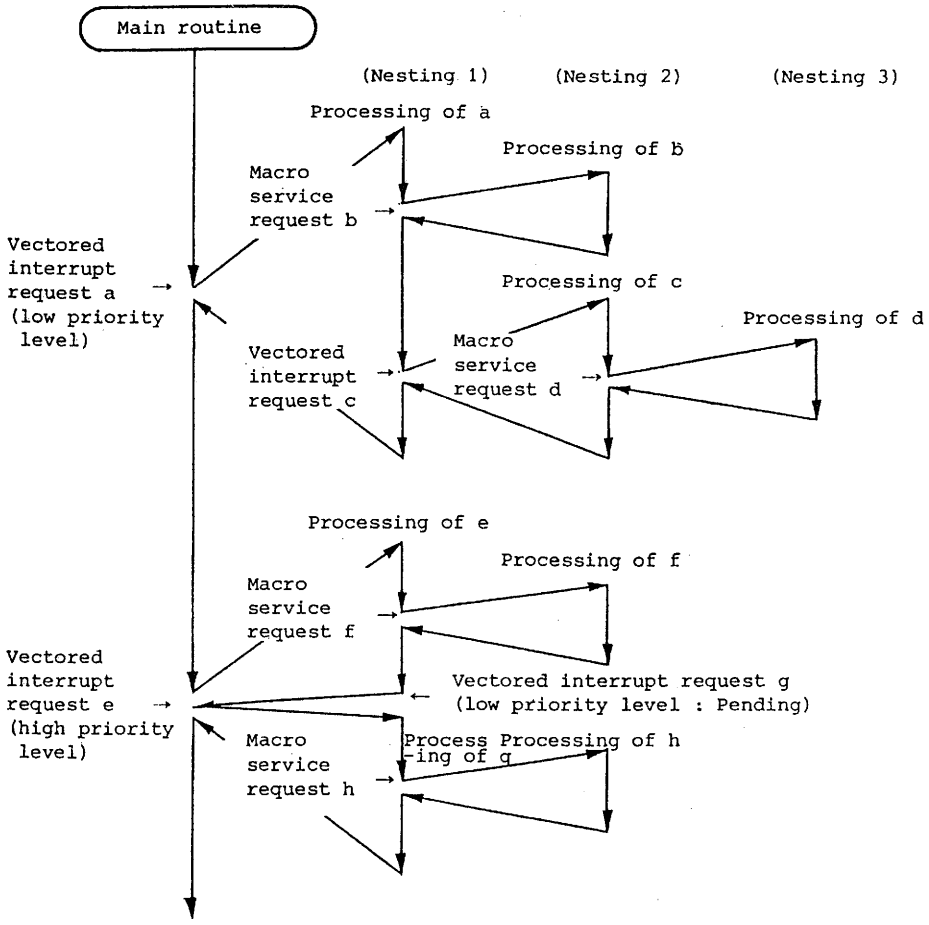
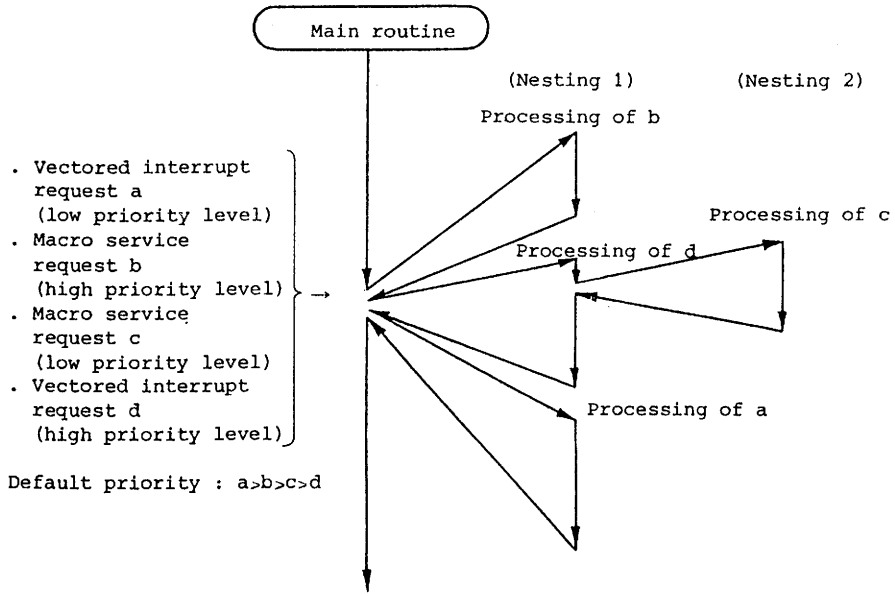


Fig. 3-2 Processing Example of Interrupt Requests Occurring Simultaneously



3.1.2 Vectored interrupt

A branch is taken to a specific interrupt service routine at the address addressed by the memory contents at the vector table address corresponding to each interrupt source.

The following are performed for the CPU to perform interrupt processing:

- At branch : CPU state (PC and PSW contents) is saved in a stack.
- At return : CPU state (PC and PSW contents) is restored from the stack.

To return from the interrupt service routine to the main routine, the RETI instruction is executed.

Table 3-3 Vector Table Addresses

Interrupt source	Vector table address
BRK	003EH
NMI	0002H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	0014H
INTC01	0016H
INTC10	0018H
INTC11	001AH
INTC21	001CH

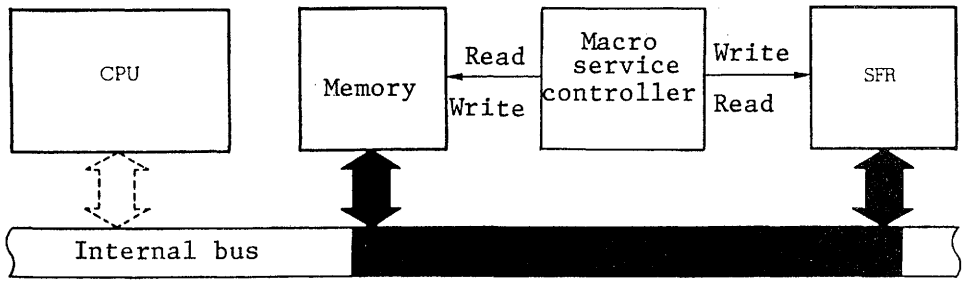
Interrupt source	Vector table address
INTP4	000EH
INTC30	
INTP5	0010H
INTAD	
INTC20	0012H
INTSER	0020H
INTSR	0022H
INTST	0024H
INTCSI	0026H
INTEER	0028H
INTEPW	002AH

3.1.3 Macro service

The macro service function transfers data between memory and a given special function register (SFR) without CPU intervention. The macro service controller accesses memory and SFR and directly transfers data without acquiring it.

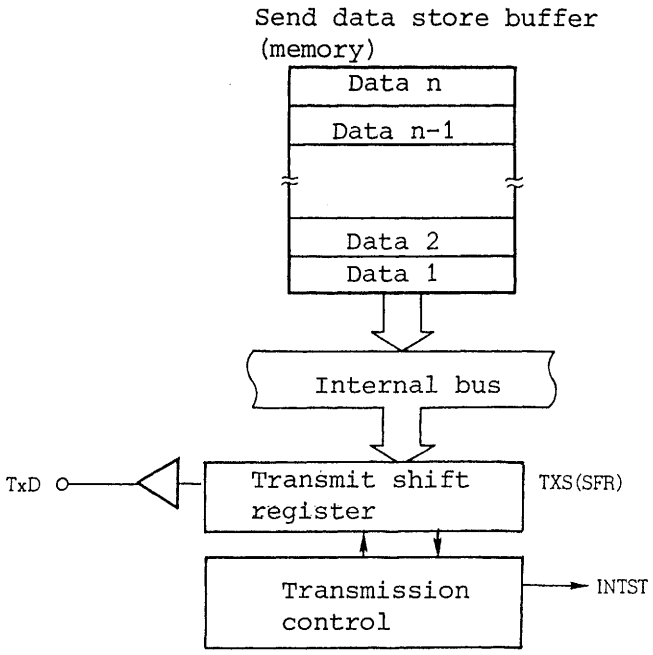
Data can be transferred at high speed because the CPU state is not saved or restored and data is not acquired.

Fig. 3-3 Macro Service



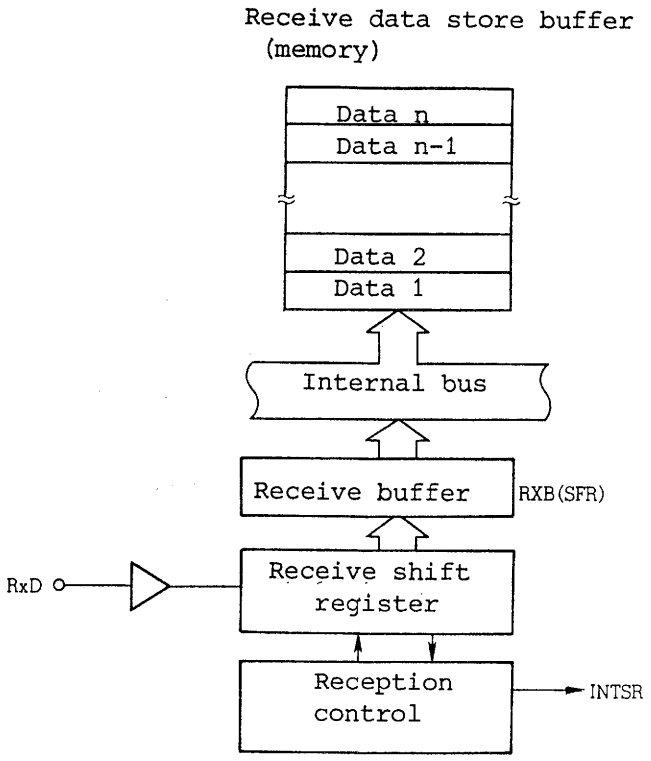
3.1.4 Macro service application examples

(1) Serial interface transmission operation



Each time macro service request INTST occurs, the next send data is transferred from memory to TXS. When data n (last byte) is transferred to TXS (when the send data store buffer becomes empty), vectored interrupt request INTST is generated.

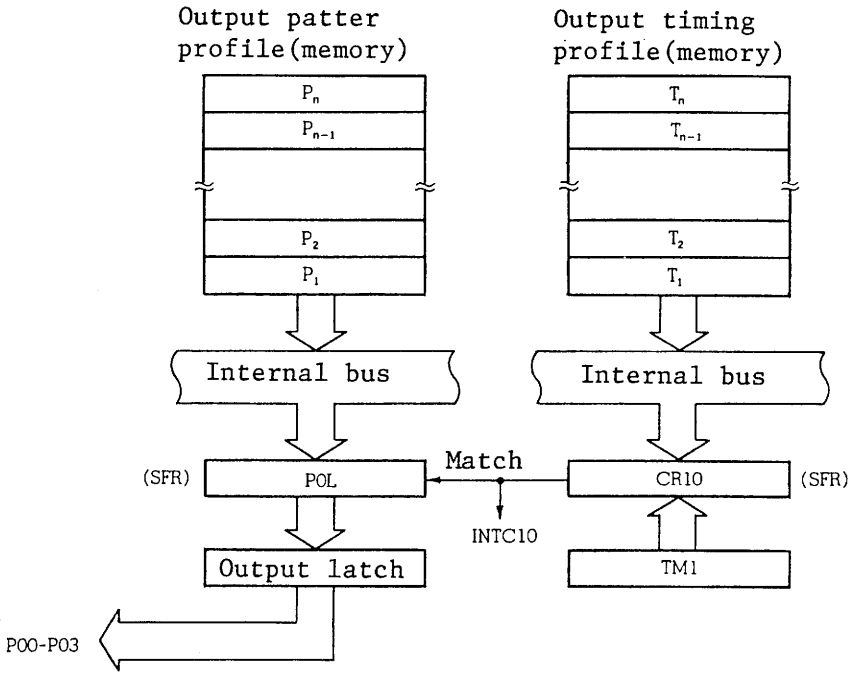
(2) Serial interface reception operation



Each time macro service request INTSR occurs, receive data is transferred from RXB to memory. When data n (last byte) is transferred to memory (when the receive data store buffer becomes full), vectored interrupt request INTSR is generated.

(3) Real-time output port

INTC10 and INTC11 are used as real-time output port output triggers. In macro service for them, the next output pattern and intervals can be set at the same time. Thus, INTC10 and INTC11 can be used to control two independent stepping motor subsystems. They are also applicable to PWM and DC motor control, etc.



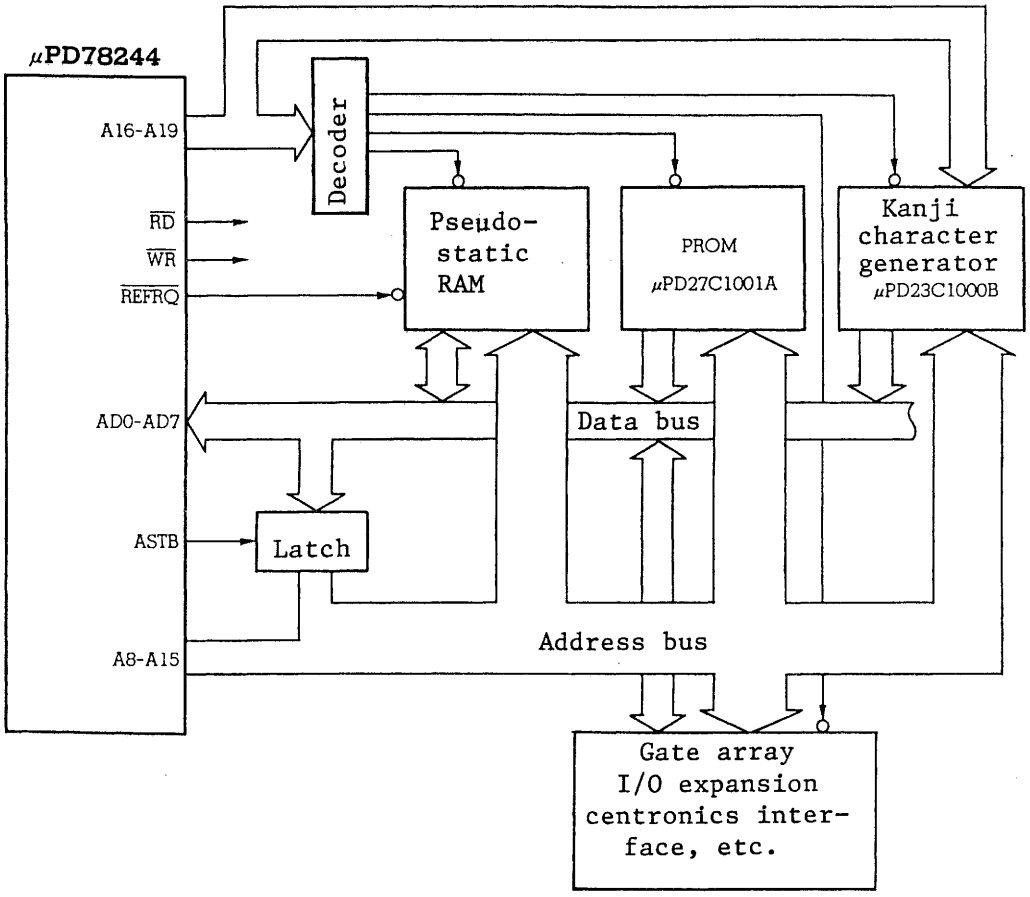
Each time macro service request INTC10 occurs, a pattern and timing are transferred to P0L and CR10 respectively. When the TM1 contents match the CR10 contents, the next INTC10 is generated and the P0L contents are sent to the output latch. When T_n (last byte) is transferred to CR10, vectored interrupt request INTC10 is generated.

Each time macro service request INTC11 occurs, the same operation is performed except that CR10 is CR11, P0L is P0H, or P00-P03 are P04-P07.

3.2 Local Bus Interface

External memory and I/O (memory-mapped I/O) can be connected to the uPD78243, 78244; the uPD78243, 78244 supports 1M-byte memory space. (See Fig. 2-1.)

Fig. 3-4 Local Bus Interface Example



3.2.1 Memory expansion

The following modes can be used as the memory expansion function:

- o External memory expansion mode: Program memory and data memory can be expanded to the external (47872 bytes). However, in the ROMless mode ($\overline{EA}$=L), the area can be used unconditionally.
- o 1M-byte expansion mode : Data memory can be expanded to the external (960K bytes) to provide 1M-byte memory space.

3.2.2 Programmable wait

Wait can be inserted in memory mapped in the normal address area (00000H-0FFFFH) and address expansion area (10000H-FFFFFH) independently. Thus, the lowering of the entire system's efficiency can be avoided although memory with different access time is connected.

3.2.3 Pseudo-static RAM refresh function

The following refresh operation is performed:

- o Pulse refresh : A refresh pulse is output to the $\overline{REFRQ}$ pin in synchronization with bus cycle.
- o Power-down self-refresh: In the standby mode, a low level is output to the $\overline{REFRQ}$ pin and the pseudo-static RAM contents are retained.

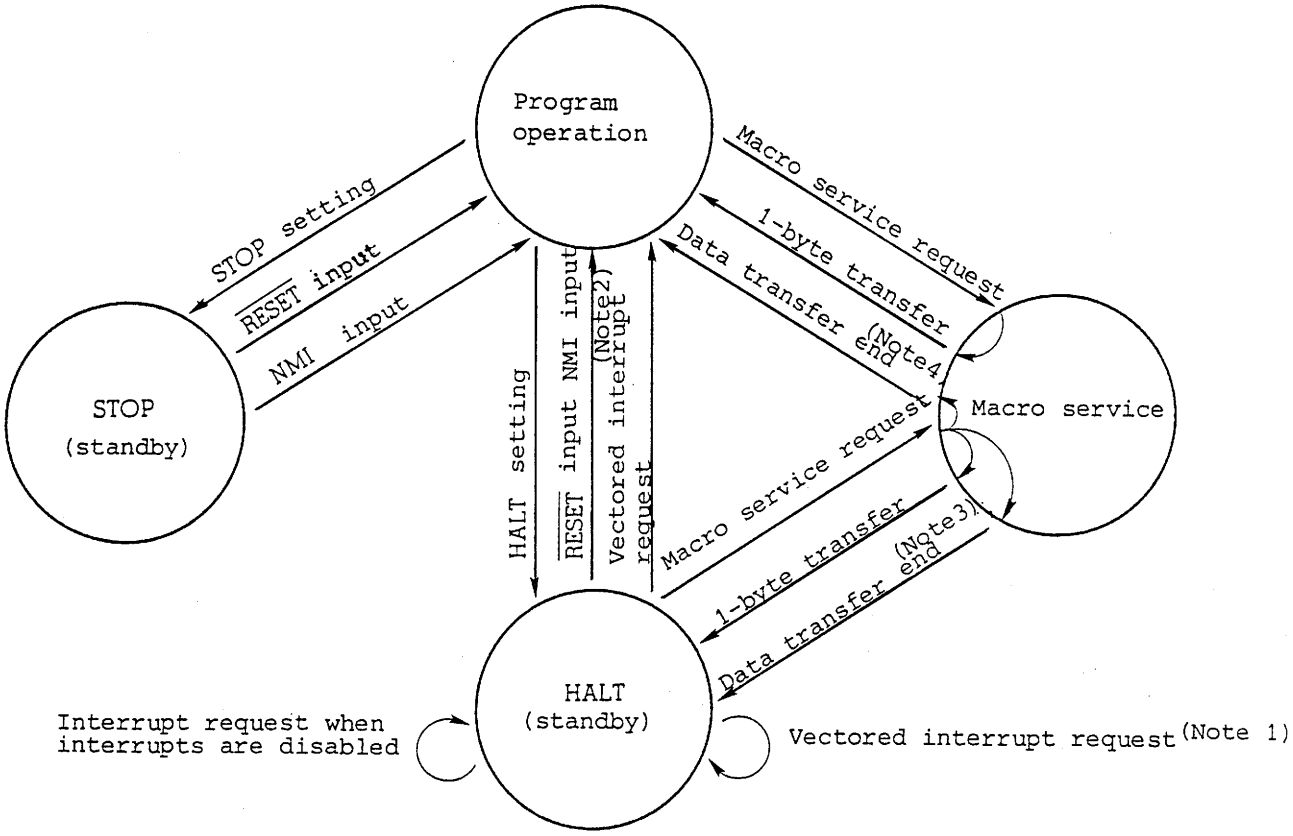
3.3 Standby

The standby function reduces chip power consumption. It provides the following modes:

- o HALT mode: Stops CPU operation clock. Average power consumption can be reduced by intermittent operation using the HALT mode and normal operation in combination.
- o STOP mode: Stops the oscillator. All operation in the chip is stopped and the chip consumes very little power with leakage current only.

The HALT mode and STOP mode are programmable.
Macro service can be started in the HALT mode.

Fig. 3-5 Standby State Transition



Note 1: Vectored interrupt request with a low priority level (interrupts with a low priority level are disabled when HALT is set).

2: Vectored interrupt request with a high priority level occurs or interrupt with a low priority level is enabled when HALT is set.

3: Macro service request with a low priority level (interrupts with a low priority level are disabled when HALT is set).

4: Macro service request with a high priority level is executed or interrupt with a low priority level is enabled when HALT is set.

3.4 Reset

When a low level is input to the $\overline{\text{RESET}}$ pin, the internal hardware is initialized (reset).

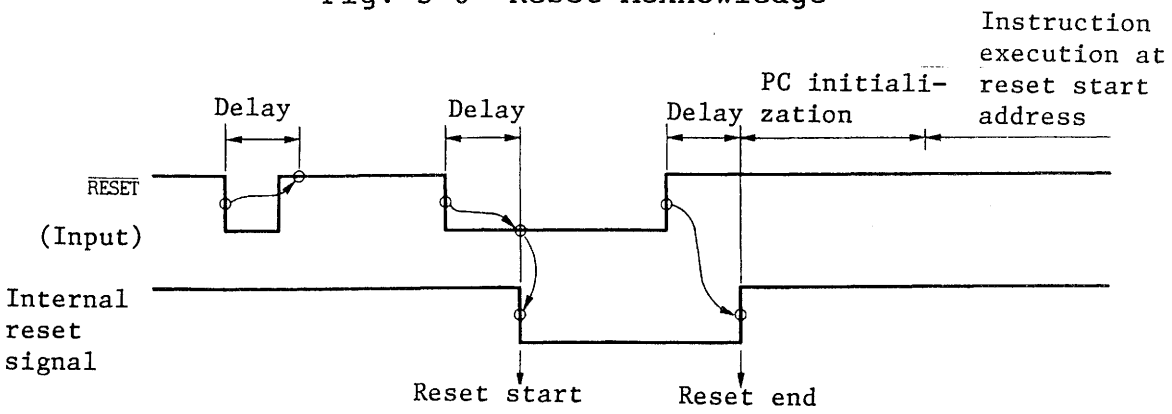
When the low-to-high transition of $\overline{\text{RESET}}$ input is made, the following data is set in the program counter (PC):

- o Low-order eight bits of PC : Contents of address 0000H
- o High-order eight bits of PC: Contents of address 0001H

Since program execution is started at the address addressed by the PC setup contents, reset start is enabled at any desired address.

Set the register contents by a program as required.
The $\overline{\text{RESET}}$ input circuit contains a noise eliminator to prevent a noise from causing an error. This noise eliminator is a sampling circuit using an analog delay.

Fig. 3-6 Reset Acknowledge



In reset operation when the power is turned on or the STOP mode is released, activate the $\overline{\text{RESET}}$ signal until the oscillation stable time (about 40 ms) elapses.

Fig. 3-7 Reset Operation when Power is Turned On

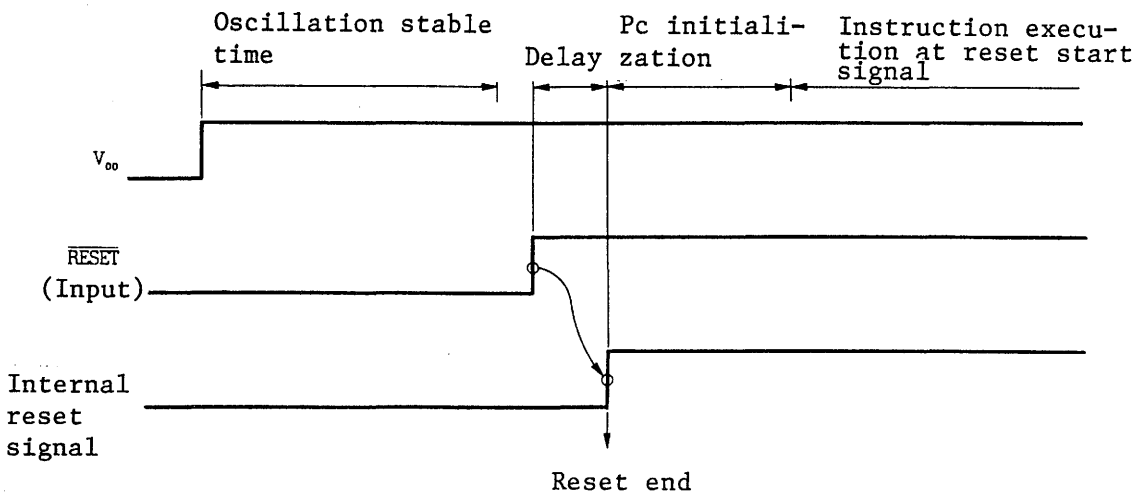


Table 3-4 Hardware State after Reset (1/2)

Hardware			State after reset
Program counter (PC)			Contents of reset vector table addresses 0000H and 0001H are set.
Stack pointer (SP)			Undefined
Program status word (PSW)			02H
ON-chip RAM	Data memory		Undefined(Note)
	General purpose registers (X, A, C, B, E, D, L, H)		
Port	Ports 0, 2-5, and 7		Undefined (high impedance)
	Port 6		x0H
Port mode registers		(PM0)	FFH
		(PM3, PM5)	FFH
		(PM6)	FxH
Port 3 mode control register (PMC3)			00H
Pull-up resistor option register (PU0)			00H
Memory expansion mode register (MM)			20H
Timer/ counter unit	16-bit timer/ counter	Timer (TM0)	0000H
		Compare registers (CR00, CR01)	Undefined
		Capture register (CR02)	
	8-bit timer/ counter	Timers (TM1, TM2, and TM3)	00H
		Compare registers (CR10, CR20, CR21, and CR30)	Undefined
		Capture register (CR22)	
		Capture/compare register (CR11)	
	Timer control registers (TMC0 and TMC1)		00H
	Timer output control register (TOC)		
	One-shot pulse output control register (OSPC)		
	Capture/compare control registers	(CRC0)	10H
		(CRC1, CRC2)	00H
	Prescaler mode registers (PRM0, PRM1)		00H
A/D converter	Mode register (ADM)		00H
	A/D conversion result register (ADCR)		Undefined

Note: When the STOP mode is released by inputting $\overline{\text{RESET}}$, the values before the STOP mode is set, are retained.

Table 3-4 Hardware State after Reset (2/2)

Hardware			State after reset
Serial interface	Mode register (CSIM)		00H
	Shift register (SIO)		Undefined
	Asynchronous mode register (ASIM)		80H
	Asynchronous status register (ASIS)		00H
	Serial bus control register (SBIC)		00H
	Serial receive buffer (RXB)		Undefined
	Serial transmit shift register (TXS)		Undefined
	Baud rate generator control register (BRGC)		00H
Real-time output port control register (RTPC)			00H
Programmable wait control register (PW)			80H
Refresh mode register (RFM)			00H
Interrupt	Interrupt request flag registers	(IF0L, IF0H)	00H
		(IF1L)	xxxx xx00B
	Interrupt mask register	(MK0L, MK0H)	FFH
		(MK1L)	xxxx xx11B
	Priority level specification flag registers	(PR0L, PR0H)	FFH
		(PR1L)	xxxx xx11B
	Interrupt service mode registers	(ISM0L, ISM0H)	00H
		(ISM1L)	xxxx xx00B
	Interrupt status register (IST)		00H
External interrupt mode registers (INTM0 and INTM1)			00H
Standby control register (STBC)			00H
EEPROM write control register (EWC)			0011 0100B

Phase-out/Discontinued

4. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP

Table 4-1 Instruction List of 8-bit Addressing

First operand \ Second operand	#byte	A	r r'	saddr saddr'	sfr	mem & mem	!addr16 &!addr16	PSW	n	(Note2) None
A	(Note1) ADD		MOV XCH	MOV XCH (Note1) ADD	MOV XCH (Note1) ADD	MOV XCH (Note1) ADD	MOV	MOV		
r	MOV		MOV XCH (Note1) ADD						ROR RORC ROL ROLC SHR SHL	MULU DIVUW INC DEC
rl										DBNZ
saddr	MOV (Note1) ADD	MOV		MOV XCH (Note1) ADD						INC DBNZ DEC
sfr	MOV (Note1) ADD	MOV								PUSH POP
mem &mem		MOV								
meml &meml										(Note3) ROR4 (Note3) ROL4
!addr16 &!addr16		MOV								
PSW	MOV	MOV								PUSH POP
STBC	MOV									

Note 1: ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.

2: The second operand does not exist or is not an operand address.

3: The instructions cannot be used for the EEPROM area.

(2) 16-bit instructions

MOVW, ADDW, SUBW, CMPW, INCW, DECW, SHRW, SHLW, PUSH, POP

Table 4-2 Instruction List of 16-bit Addressing

First operand \ Second operand	#word	AX	rp rp'	saddrp	sfrp	meml &meml	SP	n	None
AX	ADDW SUBW CMPW		ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW	MOVW		
rp	MOVW		MOVW					SHLW SHRW	INCW DECW PUSH POP
saddrp	MOVW	MOVW							
sfrp	MOVW	MOVW							
meml &meml		(Note) MOVW							
SP	MOVW	MOVW							INCW DECW

Note: The instructions cannot be used for the EEPROM.

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Table 4-3 Instruction List of Bit Manipulation Instruction Adressing

First operand \ Second operand	CY	A.bit	/A.bit	X.bit	/X.bit	saddr.bit	/saddr.bit	sfr.bit	/sfr.bit	PSW.bit	/PSW.bit	(Note) None
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	SET1
A.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
X.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
saddr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
sfr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
PSW.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR

Note: The second operand does not exist or is not an operand address.

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BT, BF, BTCLR, DBNZ, BL, BNC, BNL, BZ, BE, BNZ, BNE

Table 4-4 Instruction List of Call Instruction/ Branch Instruction

Instruction address operand	$addr16	!addr16	rp	!addr11	[addr5]
Basic instruction	BR BC(Note)	CALL BR	CALL BR	CALLF	CALLT
Multiple instruction	BT BF BTCLR DBNZ				

Note: BL, BNC, BNL, BZ, BF, BNZ, and BNE are the same as BC.

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, NOP, EI, DI, SEL

5. ELECTRIC CHARACTERISTICS

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Test condition	Ratings	Units
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	AV_{REF}		-0.5 to V_{DD}+0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input voltage	V_{I1}		-0.5 to V_{DD}+0.5	V
	V_{I2}	(Note)	-0.5 to AV_{REF}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output low current	I_{OL}	Per pin	15	mA
		Total, all outputs	100	mA
Output high current	I_{OH}	Per pin	-10	mA
		Total, all outputs	-50	mA
Operation temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

Note: Pins of P70/ANI0-P75/ANI5, P66/$\overline{\text{WAIT}}$/ANI6, and P67/$\overline{\text{REFRQ}}$/ANI7 are used as A/D converter input pins. However, the absolute maximum rating of V_{I1} must also be satisfied.

Caution: If even one parameter exceeds the absolute maximum rating, even instantaneously, the quality of the product may be damaged. The absolute maximum rating is a rated threshold value at which the product can be physically damaged. Be sure to use the product within the absolute maximum ratings.

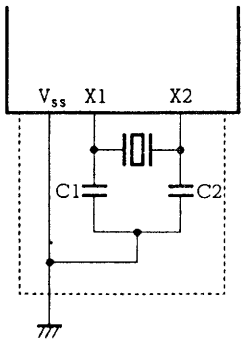
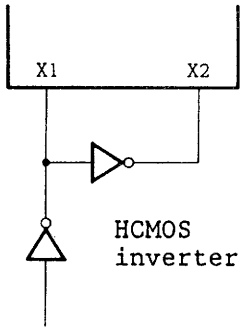
Operation conditions

Clock frequency	Operation temperature (T_{opt})	Power supply voltage(V_{DD})
4MHz≦f_{XX}≦12MHz	-10 to +70°C	+5V±10%

Capacitance (Ta=25°C, V_{DD}=V_{SS}=0 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Units
Input capacitance	C_I	f=1MHz Unmeasured pins returned to 0 V			20	pF
Output capacitance	C_O				20	pF
Input/output capacitance	C_{IO}				20	pF

Oscillator Characteristics (Ta=-40 to +85°C, V_{DD}=+5V±10%, V_{SS}=OV)

Resonator	Recommended constants	Item	MIN.	MAX.	Units
Ceramic oscillator or cristal resonator		Oscillation frequency (fxx)	4	12	MHz
External clock		X1 input frequency (fx)	4	12	MHz
		X1 input rise time/ fall time(t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH}, t_{WXL})	30	130	ns

Caution: To use the clock oscillator, wire the portions surrounded by [-----] to avoid wiring capacitance affection, etc., as follows:

- Make wiring as extremely short as possible.
- Do not cross the oscillator and any other signal line over each other.
- Do not put the oscillator near any line where high current fluctuates.
- Be sure to place oscillator capacitor ground point in the same potential as the V_{SS} pin.
  Do not connect to any ground pattern where high current flows.
- Do not take out any signal from the oscillator.

Recommended oscillator constants

Ceramic oscillator

Manufacturer	Frequency [MHz]	Product name	Recommended constants	
			C1[pF]	C2[pF]
MURATA	12	CSA12.0MTZ	30	30
		CST12.0MTW	Contained a condenser	

DC characteristics (Ta=-10°C to +70°C, V_{DD}=+5V±10%, V_{SS}=0 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Units
Input low voltage	V_{IL}		0		0.8	V
Input high voltage	V_{IH1}	Pins except for listed in Note 1 or 2	2.2		V_{DD}	V
	V_{IH2}	Pins listed in Note 1	2.2		AV_{REF}	V
	V_{IH3}	Pins listed in Note 2	$0.8V_{DD}$		V_{DD}	V
Output low voltage	V_{OL1}	I_{OL}=2.0mA			0.45	V
	V_{OL2}	I_{OL}=8.0mA (Note 3)			1.0	V
Output high voltage	V_{OH1}	I_{OH}=-1.0mA	V_{DD}-1.0			V
	V_{OH2}	I_{OH}=-100uA	V_{DD}-0.5			V
	V_{OH3}	I_{OH}=-5.0mA (Note 4)	2.0			V
X1 input low current	I_{IL}	$0 \leq V_I \leq V_{IL}$			-100	uA
X1 input high current	I_{IH}	$V_{IH3} \leq V_I \leq V_{DD}$			100	uA
Input leakage current	I_{LI}	$0V \leq V_I \leq V_{DD}$			±10	uA
Output leakage current	I_{LO}	$0\ V \leq V_O \leq V_{DD}$			±10	uA
AV_{REF} current	AI_{REF}	Operation mode fxx=12MHz		1.5	5.0	mA
V_{DD} supply current power	I_{DD1}	Operation mode fxx=12MHz		20	40	mA
	I_{DD2}	HALT mode fxx=12MHz		7	20	mA
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode V_{DDDR}=2.5V		2	20	uA
		STOP mode V_{DDDR}=5V±10%		5	50	uA
Pull-up resistor	R_L	V_I=0 V	15	40	80	kΩ
EEPROM write voltage		4MHz≦fxx≦12MHz	4.5		5.5	V

Notes 1: Pins of P70/ANI0-P75/ANI5, P66/$\overline{WAIT}$/ANI6, and P67/$\overline{REFRQ}$/ANI7 except are used as A/D converter input pins.

2: X1, X2, $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0, and $\overline{EA}$ pins.

3: P40/AD0-P47/AD7 and P50/A8-P57/A15 pins.

4: P00-P07 pins.

AC characteristics (Ta=-10°C to +70°C, V_{DD}=+5V±10%, V_{SS}=0 V)

Read/write operation (1/2)

Parameter	Symbol	Test condition	MIN.	MAX.	Units
X1 input clock cycle time	t_{CYX}		82	250	ns
Address setup time to ASTB ↓	t_{SAST} *		52		ns
Address hold time from ASTB ↓ (Note)	t_{HSTA}		25		ns
Address hold time from $\overline{RD}$ ↑	t_{HRA}		30		ns
Address hold time from $\overline{WR}$ ↑	t_{HWA}		30		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR} *		129		ns
Address float time $\overline{RD}$ ↓	t_{FAR} *		11		ns
Address → data input time	t_{DAID} *	Wait count=0		228	ns
ASTB ↓ → data input time	t_{DSTID}*	Wait count=0		181	ns
$\overline{RD}$ ↓ → data input time	t_{DRID} *	Wait count=0		100	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR} *		52		ns
Data hold time from $\overline{RD}$ ↑	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA} *		124		ns
$\overline{RD}$ ↑ → ASTB ↑ delay time	t_{DRST} *		124		ns
$\overline{RD}$ low level width	t_{WRL} *	Wait count=0	124		ns
ASTB high level width	t_{WSTH} *		52		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW} *		129		ns
ASTB ↓ → data output time	t_{DSTOD}*			142	ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			60	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW1}*	When refresh is disabled.	52		ns
	t_{DSTW2}*	When refresh is enabled.	129		ns
Data setup time to $\overline{WR}$ ↑	t_{SODWR}*	Wait count=0	146		ns
Data setup time to $\overline{WR}$ ↓	t_{SODWF}*	When refresh is enabled.	22		ns
Data hold time from $\overline{WR}$ ↑ (Note)	t_{HWOD}		20		ns
$\overline{WR}$ ↑ → ASTB ↑ delay time	t_{DWST} *		42		ns
$\overline{WR}$ low level width	t_{WWL1} *	Wait count=0 when refresh is disabled.	196		ns
	t_{WWL2} *	Wait count=0 when refresh is enabled.	114		ns
Address → $\overline{WAIT}$ ↓ input time	t_{DAWT} *			146	ns
ASTB ↓ → $\overline{WAIT}$ ↓ input time	t_{DSTWT}*			84	ns

Note: The hold time contains the V_{0H}, V_{0L} holding time under the load conditions of C_L=100 pF and R_L=2kΩ.

Remarks 1: The numeric values listed in the table are values when f_{XX}=12 MHz and C_L=100 pF.

2: For the parameters with an asterisk under Symbol, also see T_{CYX}-dependent Bus Timing Definition.

Read/write operation (2/2)

Parameter		Symbol	Test condition	MIN.	MAX.	Units
ASTB↓ → $\overline{WAIT}$ retention time		t_{HSTWT} *	External wait count=1	174		ns
ASTB↓ → $\overline{WAIT}$↑ delay time		t_{DSTWTH}*	External wait count=1		273	ns
$\overline{RD}$↓ → $\overline{WAIT}$↓ input time		t_{DRWTL} *			22	ns
$\overline{RD}$↓ → $\overline{WAIT}$ retention time		t_{HRWT} *	External wait count=1	87		ns
$\overline{RD}$↓ → $\overline{WAIT}$↑ delay time		t_{DRWTH} *	External wait count=1		186	ns
$\overline{WAIT}$↑ → data input time		t_{DWTID} *			62	ns
$\overline{WAIT}$↑ → $\overline{WR}$↑ delay time		t_{DWTW} *		154		ns
$\overline{WAIT}$↑ → $\overline{RD}$↑ delay time		t_{DWTR} *		72		ns
$\overline{WR}$↓ → $\overline{WAIT}$↓ input time (when refresh is disabled)		t_{DWWTL} *			22	ns
$\overline{WR}$↓ → $\overline{WAIT}$ retention time	When refresh is disabled	t_{HWWT1} *	External wait count=1	87		ns
	When refresh is enabled	t_{HWWT2} *	External wait count=1	5		ns
$\overline{WR}$↓ → $\overline{WAIT}$↑ delay time	When refresh is disabled	t_{DWWTH1}*	External wait count=1		186	ns
	When refresh is enabled	t_{DWWTH2}*	External wait count=1		104	ns
$\overline{RD}$↑ → $\overline{REFRQ}$↓ delay time		t_{DRRFQ} *		154		ns
$\overline{WR}$↑ → $\overline{REFRQ}$↓ delay time		t_{DWRFQ} *		72		ns
$\overline{REFRQ}$ low level width		t_{WRFQL} *		120		ns
$\overline{REFRQ}$↑ → ASTB↑ delay time		t_{DRFQST}*		280		ns

Remarks 1: The numeric values in the table apply when f_{XX}=12 MHz and C_L=100 pF.

2: For the parameters with an asterisk under the Symbol, also see t_{CYX}-dependent Bus Timing Definition.

Serial operation

Parameter	Symbol	Test condition		MIN.	MAX.	Units
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		us
		Output	Internal divide by 16	1.3		us
			Internal divide by 64	5.3		us
Serial clock low level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal divide by 16	556		ns
			Internal divide by 64	2.5		us
Serial clock high level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal divide by 16	556		ns
			Internal divide by 64	2.5		us
SI, SBO setup time to $\overline{SCK}\uparrow$	t_{SSSK}			150		ns
SI, SBO hold time from $\overline{SCK}\uparrow$	t_{HSSK}			400		ns
SO/SBO output delay time from $\overline{SCK}\downarrow$	t_{DSBSK1}	CMOS push-pull output (3-line serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open drain output (SBI mode), R_L=1kΩ		0	800	ns
SBO high hold time from $\overline{SCK}\uparrow$	t_{HSBSK}	SBI mode		4		t_{CYX}
SBO low setup time to $\overline{SCK}\downarrow$	t_{SSBSK}			4		t_{CYX}
SBO low level width	t_{WSBL}			4		t_{CYX}
SBO high level width	t_{WSBH}			4		t_{CYX}

Remarks: The numeric values listed in the table are values when f_{XX}=12 MHz and C_L=100 pF.

Other operations

Parameter	Symbol	Test condition	MIN.	MAX.	Units
NMI low level width	t_{WNIL}		10		us
NMI high level width	t_{WNIH}		10		us
INTP0-INTP5 low level width	t_{WITL}		24		t_{CYX}
INTP0-INTP5 high level width	t_{WITH}		24		t_{CYX}
$\overline{\text{RESET}}$ low level width	t_{WRSL}		10		us
$\overline{\text{RESET}}$ high level width	t_{WRSH}		10		us

External clock timing

Parameter	Symbol	Test condition	MIN.	MAX.	Units
X1 input low level width	t_{WXL}		30	130	ns
X1 input high level width	t_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D converter characteristics (Ta=-10°C to +70°C, V_{DD}=+5V±10%, V_{SS}=AV_{SS}=0 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Units
Resolution			8			bit
(Note 1) Total error		4.0V≦AV_{REF}≦V_{DD}			0.4	%
		3.6V≦AV_{REF}≦V_{DD}			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	82ns≦t_{CYX}<125ns When ADM FR bit is 0	360			t_{CYX}
		125ns≦t_{CYX}<250ns When ADM FR bit is 1	240			t_{CYX}
Sampling time	t_{SAMP}	82ns≦t_{CYX}<125ns When ADM FR bit is 0	72			t_{CYX}
		125ns≦t_{CYX}<250ns When ADM FR bit is 1	48			t_{CYX}
Analog input voltage	V_{IAN}		-0.3		AV_{REF}+0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		3.6		V_{DD}	V
AV_{REF} current	AI_{REF}	fxx=12MHz		1.5	5.0	mA
		(Note 2)		0.2	1.5	mA

Notes 1: It does not contain a quantization error. It is represented by a ratio to the full scale value.

2: When the ADM register CS bit is 0.

t_{CYX}-dependent bus timing definition (1/2)

Parameter	Symbol	Test condition	MIN./MAX.	12MHz	Units
X1 input clock cycle time	t_{CYX}		MIN	82	ns
Address setup time to ASTB↓	t_{SAST}	t_{CYX}-30	MIN.	52	ns
Address hold time from $\overline{RD}$↑	t_{HRA}		MIN.	30	ns
Address hold time from $\overline{WR}$↑	t_{HWA}		MIN.	30	ns
Address → $\overline{RD}$↓ delay time	t_{DAR}	$2t_{CYX}$-35	MIN.	129	ns
Address float time to $\overline{RD}$↓	t_{FAR}	t_{CYX}/2-30	MIN.	11	ns
Address → data input time	t_{DAID}	(4+2n)t_{CYX}-100	MAX.	228(Note)	ns
ASTB↓ → data input time	t_{DSTID}	(3+2n)t_{CYX}-65	MAX.	181(Note)	ns
$\overline{RD}$↓ → data input time	t_{DRID}	(2+2n)t_{CYX}-64	MAX.	100(Note)	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}	t_{CYX}-30	MIN.	52	ns
$\overline{RD}$ → address active time	t_{DRA}	$2t_{CYX}$-40	MIN.	124	ns
$\overline{RD}$↑ → ASTB↑ delay time	t_{DRST}	$2t_{CYX}$-40	MIN.	124	ns
$\overline{RD}$ low level width	t_{WRL}	(2+2n)t_{CYX}-40	MIN.	124(Note)	ns
ASTB high level width	t_{WSTH}	t_{CYX}-30	MIN.	52	ns
Address → $\overline{WR}$↓ delay time	t_{DAW}	$2t_{CYX}$-35	MIN.	129	ns
ASTB↓ → data output time	t_{DSTOD}	t_{CYX}+60	MAX.	142	ns
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW1}	t_{CYX}-30 (When refresh is disabled.)	MIN.	52	ns
	t_{DSTW2}	$2t_{CYX}$-35 (When refresh is enabled.)	MIN.	129	ns
Data setup time to $\overline{WR}$↑	t_{SODWR}	(3+2n)t_{CYX}-100	MIN.	146(Note)	ns
Data setup time to $\overline{WR}$↓	t_{SODWF}	t_{CYX}-60 (When refresh is enabled.)	MIN.	22	ns
$\overline{WR}$↑ → ASTB↑ delay time	t_{DWST}	t_{CYX}-40	MIN.	42	ns
$\overline{WR}$ low level width	t_{WWL1}	(3+2n)t_{CYX}-50 (When refresh is disabled.)	MIN.	196(Note)	ns
	t_{WWL2}	(2+2n)t_{CYX}-50 (When refresh is enabled.)	MIN.	114(Note)	ns
Address → $\overline{WAIT}$↓ input time	t_{DAWT}	3t_{CYX}-100	MAX.	146	ns
ASTB↓ → $\overline{WAIT}$↓ input time	t_{DSTWT}	$2t_{CYX}$-80	MAX.	84	ns

Remarks: n denotes the number of wait states.

Note: When n=0.

t_{CYX}-dependent bus timing definition (2/2)

Parameter		Symbol	Test condition	MIN./MAX.	12MHz	Units
ASTB ↓ → $\overline{WAIT}$ retention time		t_{HSTWT}	$2Xt_{CYX}+10$	MIN.	174 (Note)	ns
ASTB ↓ → $\overline{WAIT}$ ↑ delay time		t_{DSTWTH}	$2(1+X)t_{CYX}-55$	MAX.	273 (Note)	ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time		t_{DRWTL}	$t_{CYX}-60$	MAX.	22	ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ retention time		t_{HRWT}	$(2X-1)t_{CYX}+5$	MIN.	87 (Note)	ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↑ delay time		t_{DRWTH}	$(2X+1)t_{CYX}-60$	MAX.	186 (Note)	ns
$\overline{WAIT}$ ↑ → data input time		t_{DWTID}	$t_{CYX}-20$	MAX.	62	ns
$\overline{WAIT}$ ↑ → $\overline{WR}$ ↑ delay time		t_{DWTW}	$2t_{CYX}-10$	NIM.	154	ns
$\overline{WAIT}$ ↑ → $\overline{RD}$ ↑ delay time		t_{DWTR}	$t_{CYX}-10$	MIN.	72	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↓ input time (when refresh is disabled)		t_{DWWTL}	$t_{CYX}-60$	MAX.	22	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ retention time	When refresh is disabled	t_{HWWT1}	$(2X-1)t_{CYX}+5$	MIN.	87 (Note)	ns
	When refresh is enabled	t_{HWWT2}	$2(X-1)t_{CYX}+5$	MIN.	5 (Note)	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↑ dely time	When refresh is disabled	t_{DWWTH1}	$(2X+1)t_{CYX}-60$	MAX.	186 (Note)	ns
	When refresh is enabled	t_{DWWTH2}	$2Xt_{CYX}-60$	MAX.	104 (Note)	ns
$\overline{RD}$ ↑ → $\overline{REFRQ}$ ↓ delay time		t_{DRRFQ}	$2t_{CYX}-10$	MIN.	154	ns
$\overline{WR}$ ↑ → $\overline{REFRQ}$ ↓ delay time		t_{DWRFQ}	$t_{CYX}-10$	MIN.	72	ns
$\overline{REFRQ}$ low level width		t_{WRFQL}	$2t_{CYX}-44$	MIN.	120	ns
$\overline{REFRQ}$ ↑ → ASTB ↑ delay time		t_{DRFQST}	$4t_{CYX}-48$	MIN.	280	ns

Remarks 1: X: Number of external wait cycles (1, 2, ...)

2: $t_{CYX} \fallingdotseq 82ns$ (f_{XX}=12MHz)

3: n denotes the number of wait cycles.

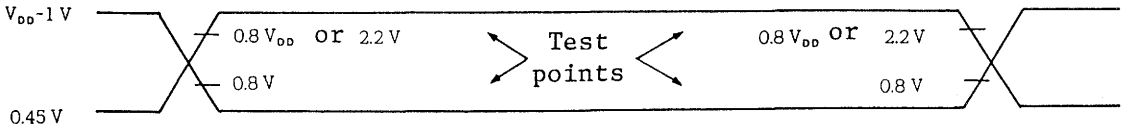
Note: When X=1.

Data retention characteristics (Ta = -10°C to 70°C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Units
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR}=2.5V		2	20	uA
		V_{DDDR}=5V±10%		5	50	uA
V_{DD} rise time	t_{RVD}		200			us
V_{DD} fall time	t_{FVD}		200			us
V_{DD} retention time from STOP mode setting	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stable wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic oscillator	5			ms
Input low voltage	V_{IL}	Specific pins(Note)	0		0.1 V_{DDDR}	V
Input high voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

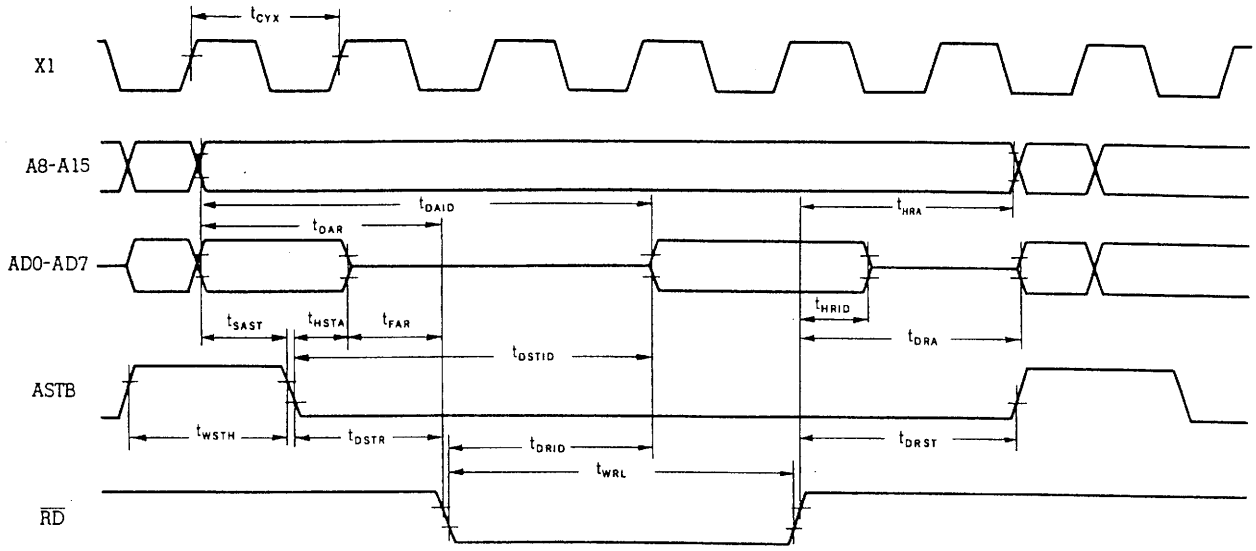
Note: $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ pins

AC Timing Test Points

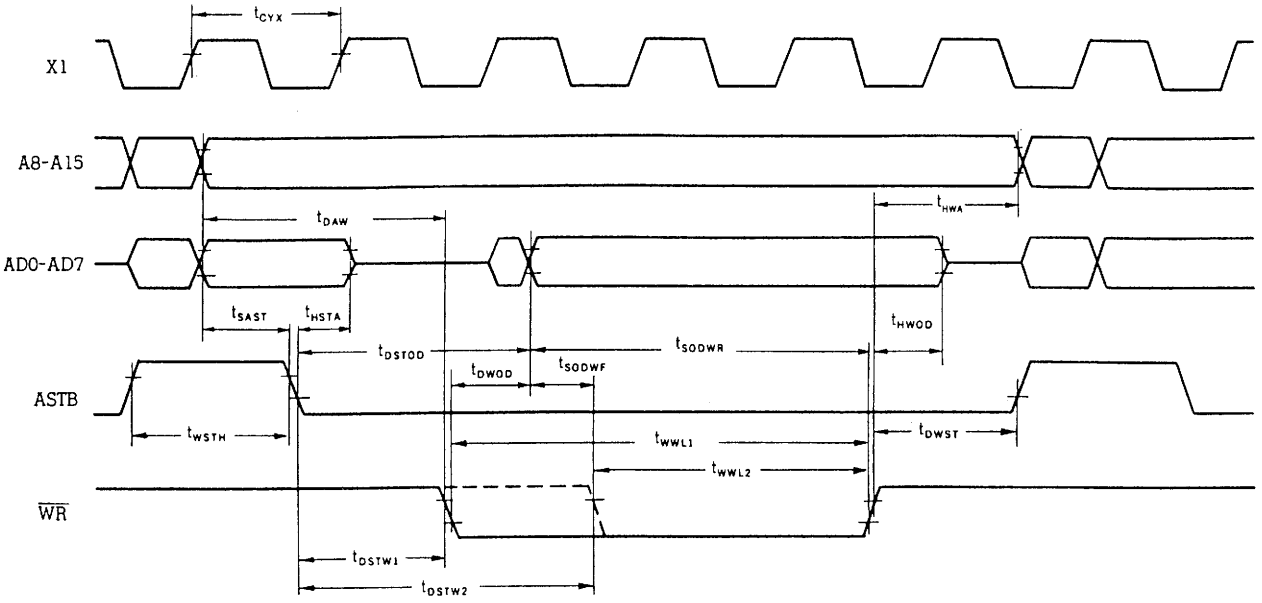


Timing Waveforms

Read operation

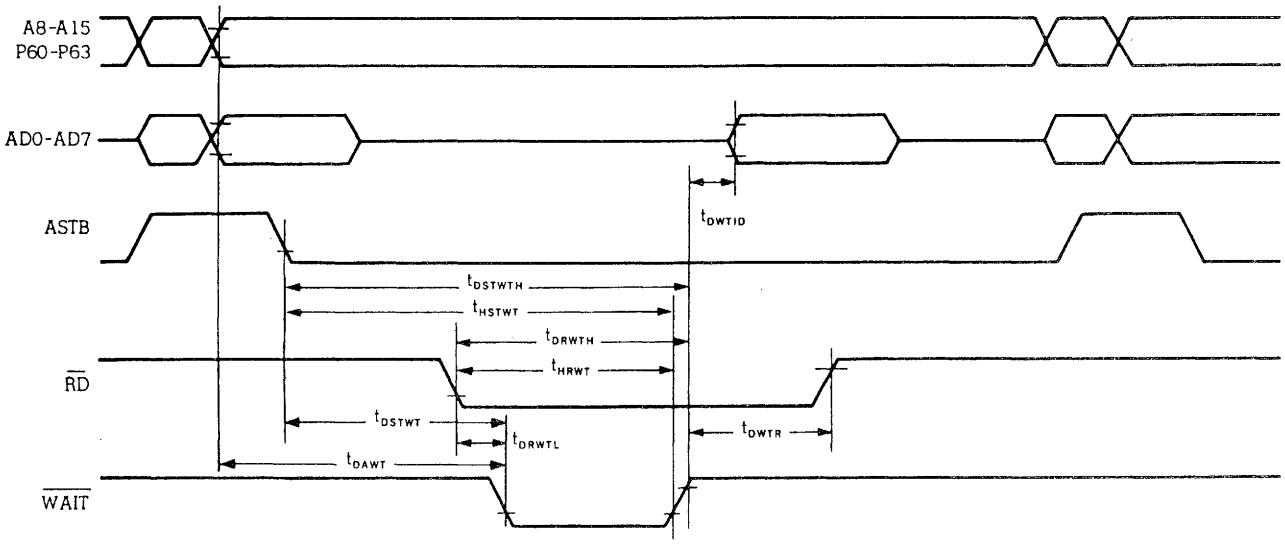


Write operation

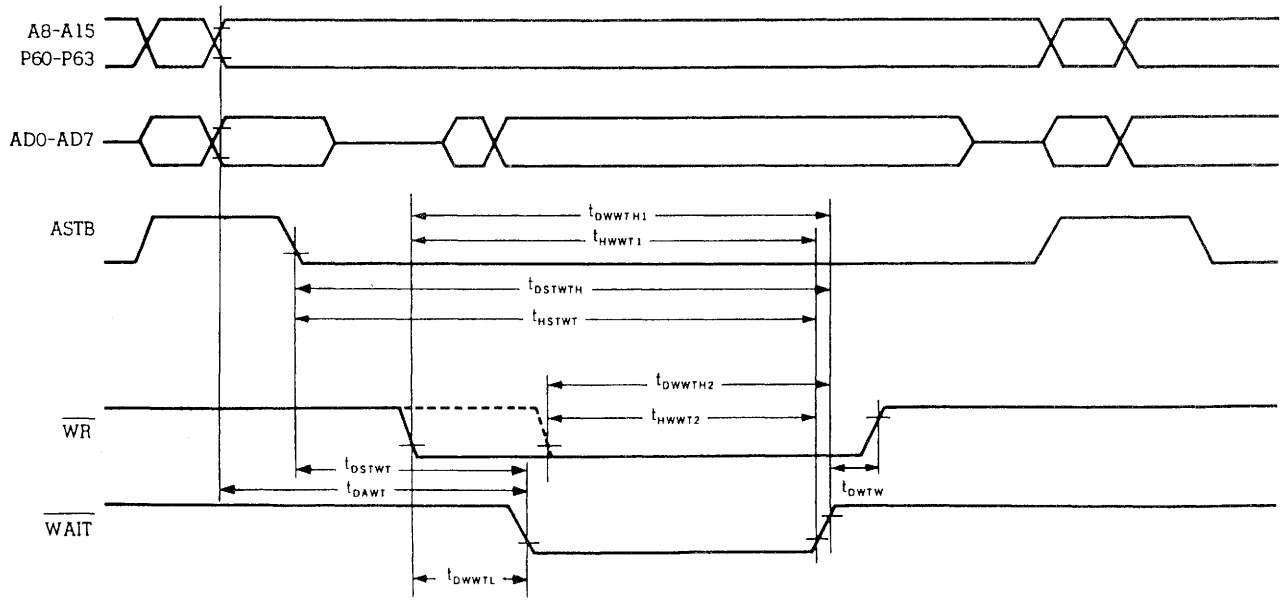


External WAIT Signal Input Timing

Read operation

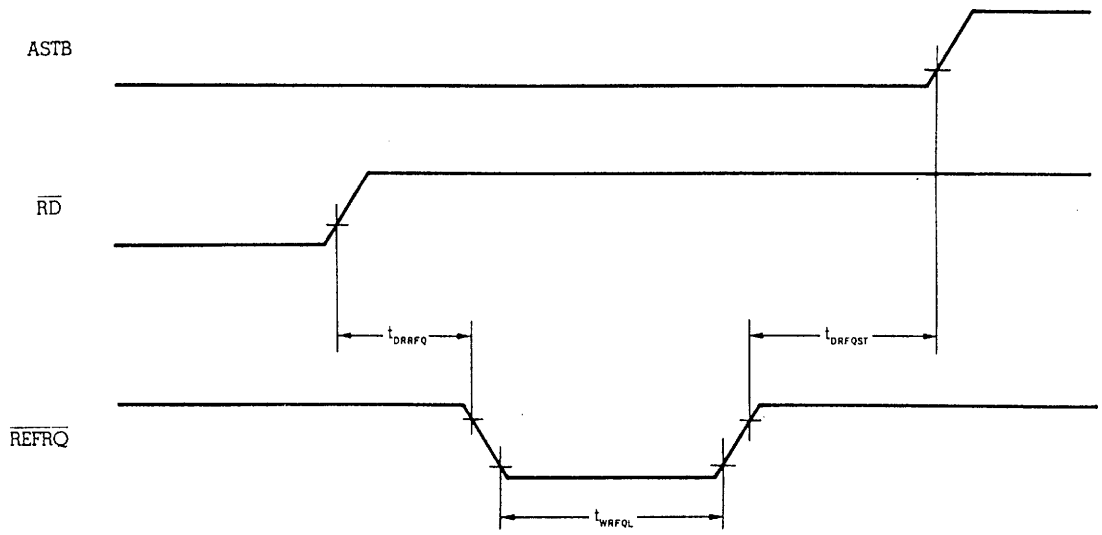


Write operation

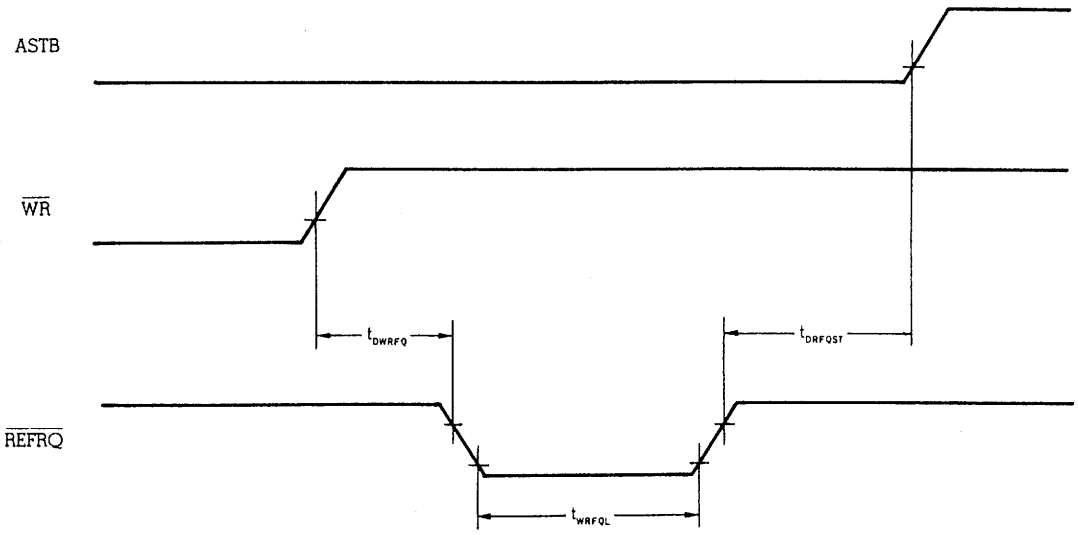


Refresh Timing Waveforms

Refresh after read

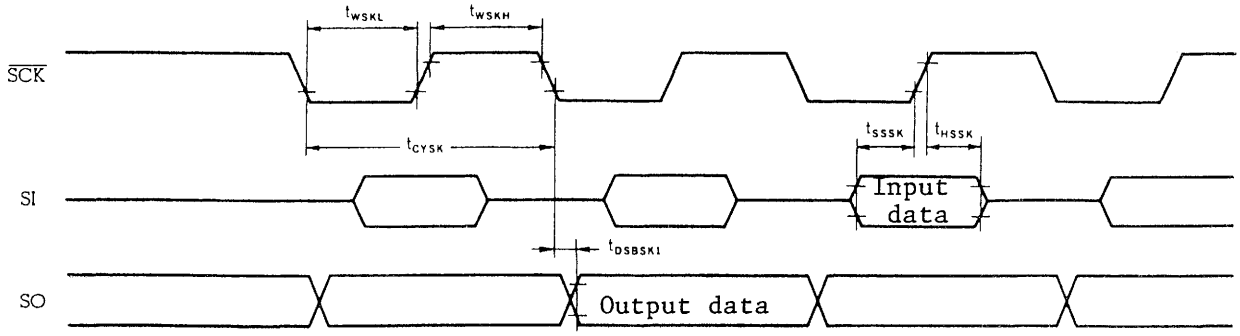


Refresh after write



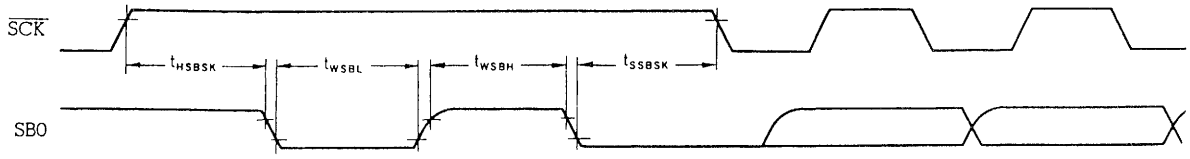
Serial Operation

3-line serial I/O mode

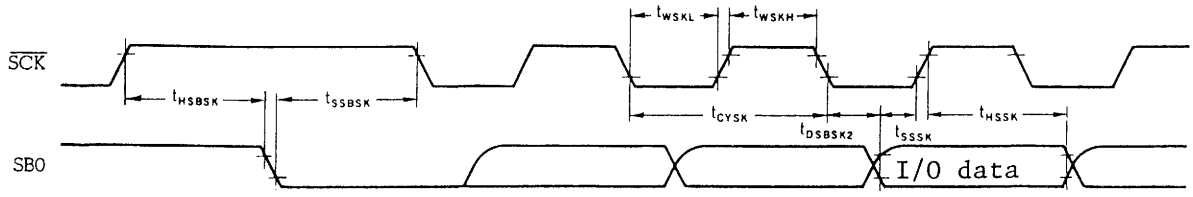


SBI Mode

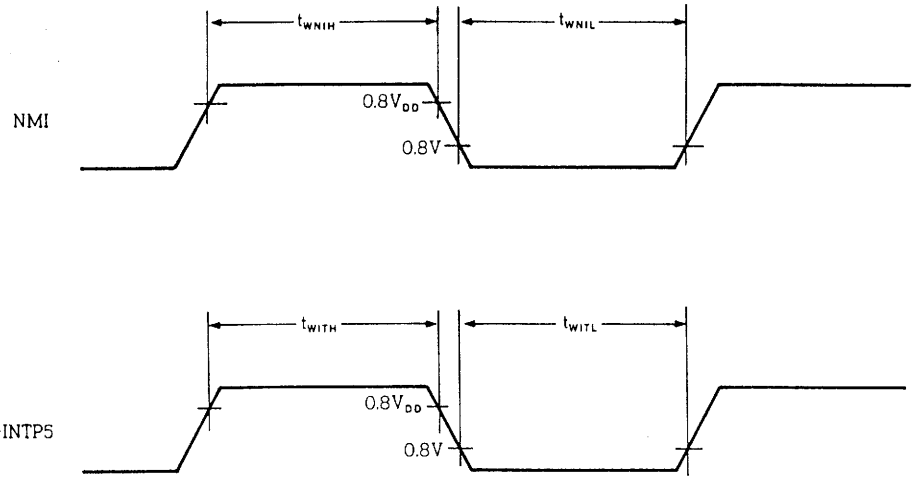
Bus release signal transfer



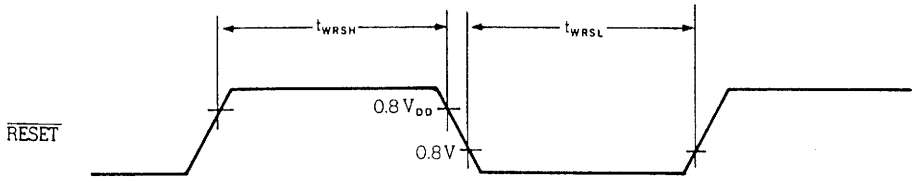
Command signal transfer



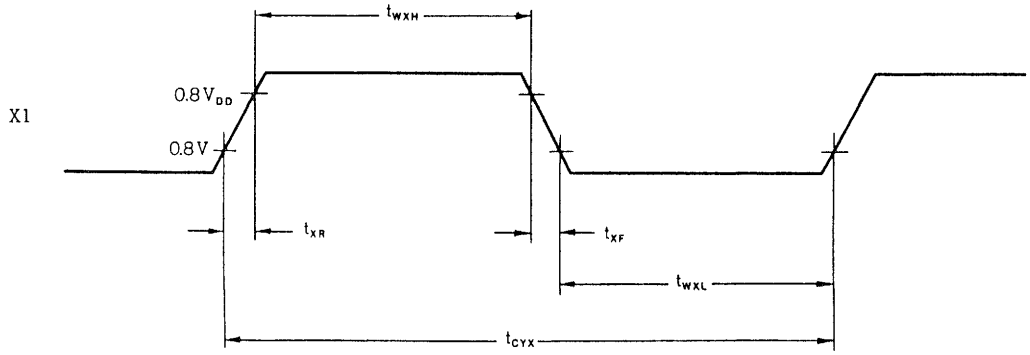
Interrupt Input Timing



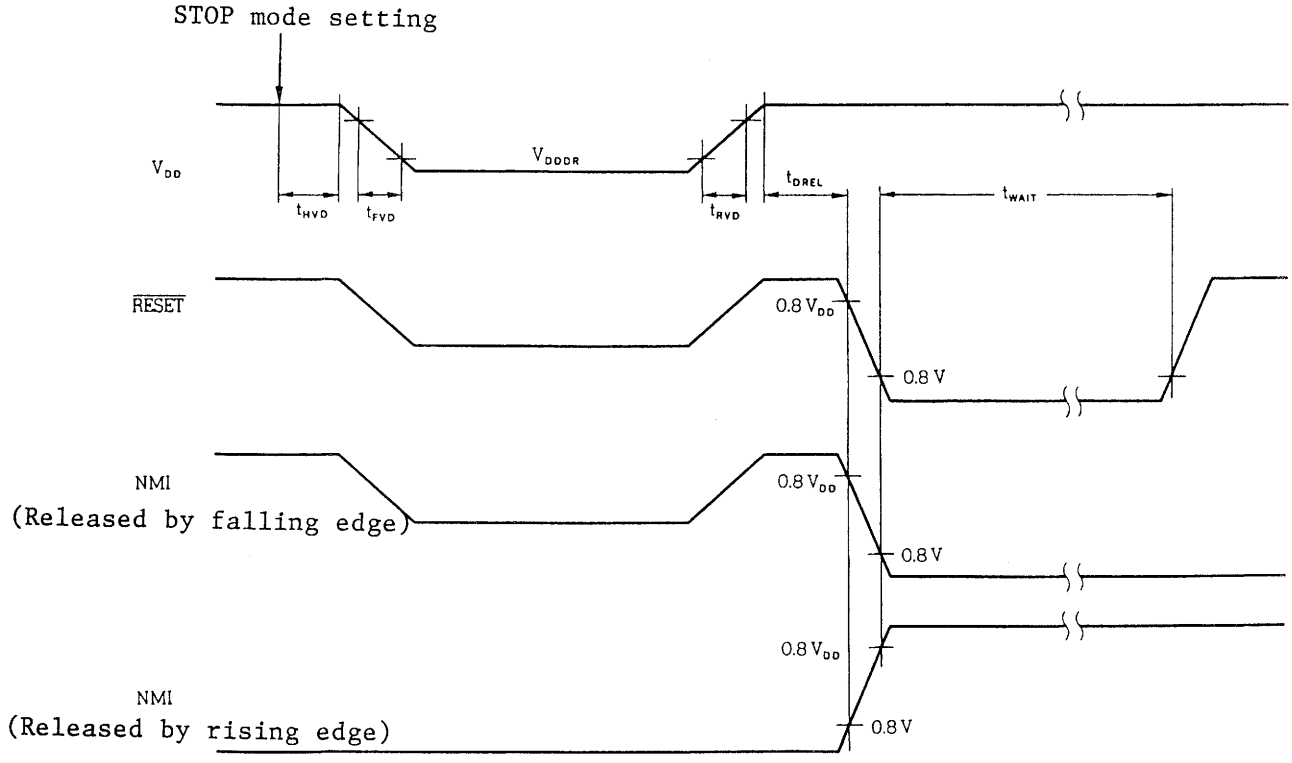
Reset Input Timing



External Clock Timing



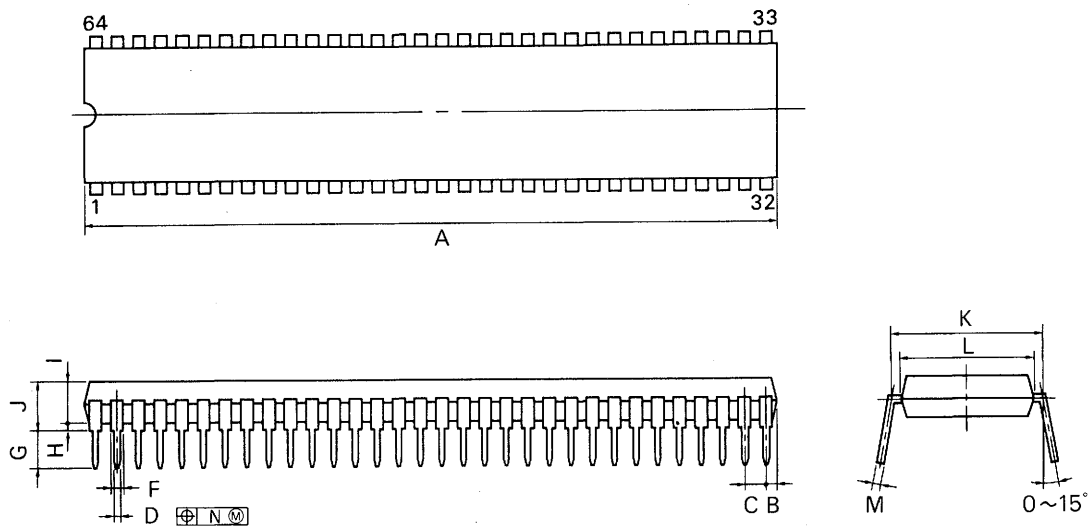
Data Retention Characteristics



Phase-out/Discontinued

6. PACKAGE INFORMATION

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

NOTES

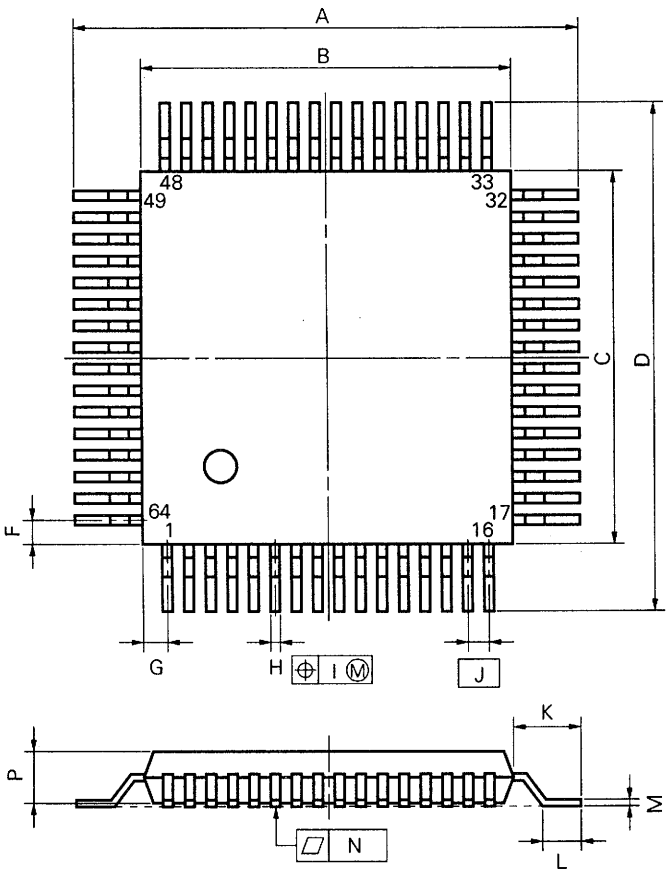
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

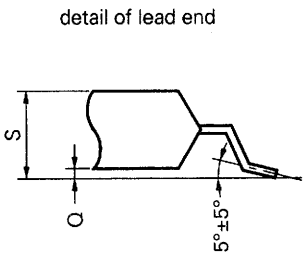
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

Phase-out/Discontinued

64 PIN PLASTIC QFP (□14)





P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

7. RECOMMENDED CONDITIONS FOR SOLDERING

Solder the product under the recommended conditions listed below.

For details of the recommended conditions for soldering, refer to the Information: **Semiconductor Device Mount Manual (IEI-616).**

Consult the NEC sales person about soldering methods and soldering conditions other those than listed below.

Table 7-1 Recommended Condition for Surface Mount Type

uPD78243GC-AB8, 78244GC-xxx-AB8: 64-pin plastic QFP (□14mm)

Soldering method	Soldering conditions	Recommended condition symbol
Infrared reflow	Package peak temperature: 230°C, Time: Within 30s (at 210°C or higher), Count: Once, Limited number of days: Two days(Note) (after the days, prebake is required at 125°C for 16 hours)	IR30-162-1
VPS	Package peak temperature: 215°C, Time: Within 40s (at 200°C or higher), Count: Once, Limited number of days: Two days(Note) (after the days, prebake is required at 125°C for 16 hours)	VP15-162-1
Wave soldering	Soldering tank temperature: 260°C or less, Time: Within 10s, Count: Once, Preheating temperature: 120°C MAX. (package surface temperature), Limited number of days: Two days(Note) (after the days, prebake is required at 125°C for 16 hours)	WS60-162-1
Pin part heating	Pin part temperature: 300°C, Time: Within 3s (per frame of device)	——

Note: It is the number of storage days under the storage conditions of 25°C and 65%RH or less after the dry pack is opened.

Caution: Do not use the soldering methods together (except the pin part heating).

Table 7-2 Soldering Conditions for Insertion Type

uPD78243CW, 78244CW-xxx: 64-pin plastic shrinked-dual-in-line package (750mil)

Soldering method	Soldering conditions
Wave soldering (lead part only)	Soldering tank temperature: 260°C or less, Time: Within 10s
Pin part heating	Pin part temperature: 260°C or less, Time: Within 10s

Caution: Apply wave soldering only to the lead part and be careful so as not to bring solder injection directly into contact with the package.

Information

The product contains a soldering recommended condition improvement product.
(Improvement contents: Infrared ray reflow peak temperature extension (235°C), count twice, lessening of the number of limited days, etc.)
For details, ask the NEC sales person.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are provided for system development using the uPD78243, 78244:

Language Processor Software

RA78K/II(Note 1, 2)	Assembler package common to 78K/II series
CC78K/II(Note 1, 2)	C compiler package common to 78K/II series
CC78K/II-L(Note 1, 2)	C compiler library source file common to 78K/II series

PROM Wite Tool

PG-1500	PROM programmer
PG-1500 controller(Note 1)	PG-1500 control program

Debug Tool

IE-78240-R-A IE-78240-R(Note 3)	In-circuit emulator common to uPD78244 series
IE-78200-R-BK	Break board common to 78K/II series
IE-78240-R-EM IE-78200-R-EM(Note 3)	uPD78244 series equivalent emulation board
EP-78240CW-R EP-78210CW(Note 3) EP-78240GC-R EP-78210GC(Note 3)	Emulation probe common to uPD78244 series
EV-9200GC-64	Socket mounted on user system board prepared for 64-pin plastic QFP
SD78K/II(Note 1)	IE-78240-R-A screen debugger
DF78240(Note 1)	uPD78244 series device file

Real-Time OS

RX78K/II(Note1, 2)	Real-time OS common to 78K/II series

Fuzzy Inference Development Support System

FE9000(Note 1)	Fuzzy knowledge data preparation tool
FT9080(Note 1)	Translator
FI78K/II(Note 1)	Fuzzy inference module
FD78K/II(Note 1, 4)	Fuzzy inference debugger

Note 1: PC-9800 series (MS-DOS™) base, IBM PC/AT™ (PC DOS™) base

2: HP9000 series 300™ (HP-UX™) base, SPARCstation™ (Sun OS™) base, EWS-4800 series™ (EWS-UX/V™) base

3: The products are not manufactured at present and therefore cannot be purchased.

4: Under development.

Remarks: For development tools developed by third parties, refer to the 78K/II Series development Tool Selection Guide (EF-231).

APPENDIX B RELATED DOCUMENTS

• Documents Related to Device

Title		Doc. No.
uPD78244 series user's manual: Hardware		IEU-747
78K/II series user's manual: Instruction		IEU-754
78K/II series application note	Basic	IEA-607
	Application	IEA-700
	Floating point arithmetic program	IEA-686
78K/II series selection guide		IF-304
78K/II series instruction quick reference		IEM-5101
78K/II series instruction set		IEM-5102
uPD78244 series special function register quick reference		IEM-5528

• Documents Related to Development Tools (User's Manual)

Title		Doc. No.
RA78K series assemble package	Operation	EEU-809
	Language	EEU-815
RA78K series structured assembler preprocessor		EEU-817
CC78K series C compiler	Operation	EEU-656
	Language	EEU-655
CC78K series library source file		EEU-777
PG-1500 PROM programmer		EEU-651
PG-1500 controller		EEU-704
IE-78240-R-A in-circuit emulator		EEU-796
IE-78240-R in-circuit emulator	Hardware	EEU-705
	Software	EEU-706
SD78K/II screen debugger	Preliminary	EEU-841
	Reference	EEU-813
78K/II series development tool selection guide		EF-231

• Documents Related to Build-in Software (User's Manual)

Title		Doc. No.
RX78K/II real-time OS	Basic	EEU-910
	Installation	EEU-884
	Debugger	EEU-895
	Technical	EEU-885
Fuzzy knowledge data preparation tool		EEU-829
78K/0, 78K/II, 87AD series fuzzy inference development support system	Translator	EEU-862
78K/II series fuzzy inference development support system	Fuzzy inference module	EEU-860
78K/II series fuzzy inference debugger		EEU-917

• Documents related to device

Title	Doc. No.
QTOP microcomputer pamphlet	IB-5040
Package manual	IEI-635
Semiconductor mount technology manual	IEI-616
Quality grades on NEC semiconductor devices	IEI-620
NEC semiconductor device reliability/quality control system	IEM-5068
Electrostatic discharge (ESD) test	MEM-539
Guide to quality assurance for semiconductor devices	MEI-603
Microcomputer-related product guide - Third party products	MEI-604

Remarks: The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.

General Cautions on CMOS Devices

① Measures for Static Electricity (for general MOSs)

Caution: To handle MOS devices, be sure to protect against static electricity.

Strong static electricity may cause gate insulation of MOS devices to be destroyed. To transport or store a MOS devices, use a conductive tray, the magazine case used for the shipment package by NEC, or a conductive buffer material or metal case. In an assembly step, ground MOS devices. Do not leave MOS devices on a plastic plate. Also handle boards on which CMOS devices are mounted in one of the manners described above.

② Treatment for Unused Input (only for CMOSs)

Caution: Fix input levels of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to the CMOS device input, intermediate level input is caused by a source such as noise and internal through current flows, which may cause an error to occur. Fix the input level with a pull-up or pull-down resistor. If the possibility that an unused pin may become output (the timing is not defined) is considered, it is effective to connect each via a resistor to V_{DD} or GND.

For the products for which "Treatment for unused pins" is described in the document, follow the description.

③ State before Initialization (for general MOSs)

Caution: When power is turned on, the initial state of MOS devices is undefined.

Since the characteristics are determined by ion implementation amount at molecular level, etc., the initial state is beyond management of the production process. The pin output state, input/output setting, and register contents when power is turned on are not guaranteed. However, the items defined in reset operation and mode setting are guaranteed after these operations.

After turning on power of devices having the reset function, first execute a reset operation.

Phase-out/Discontinued

〔MEMO〕

uPD78244 is manufactured and sold under license from BULL CP8 Corporation with respect to the EEPROM on-chip microcomputer patent. The product cannot be used for IC card (SMART CARD).

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