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RENESAS

Phase-out/Discontinued

MOS INTEGRATED CIRCUIT

μPD78146, 78148

8 BIT SINGLE-CHIP MICROCOMPUTER

The μPD78148, with on-chip peripheral hardware, can be used in VCRs and other devices that require digital servo control with software.

The μPD78P148, with the one-time PROM or EPROM, is also available, which can operate in the same range of the power supply voltage as the mask ROM product. The development tools are also provided for the μPD78148.

The following user's manual completely describes the functions of the μPD78148. Be sure to read it before designing an application system.

μPD78148 User's Manual: IEU-1319

FEATURES

- Mass-storage program memory
  μPD78146 ROM: 24K bytes, RAM: 688 bytes
  μPD78148 ROM: 32K bytes, RAM: 816 bytes
- I/O lines: 76
- On-chip peripheral hardware suitable for VCR servo control
  - Super timer unit
  - Real-time output ports: 18
  - High-precision A/D converter: 15 channels
  - Multiplier
  - Clock operation by the subsystem clock
  - Serial interface: 2 channels
  - Hardware for receiving remote control signals
  - Operational amplifiers: 2
- Built-in powerful interrupt functions providing two service modes
  - Vectored interrupt function/Macro service function

APPLICATIONS

System/servo controlling of separate VCRs and camcorders)

ORDERING INFORMATION

Part number	Package
μPD78146GF-xxx-3BA	100-pin plastic QFP (14 × 20 mm)
μPD78148GF-xxx-3BA	100-pin plastic QFP (14 × 20 mm)

Remark: xxx: ROM code number

Unless otherwise specified (for functions), the description of the μPD78148 applies to the μPD78146.

Document No. U10221EJ3V0DS00 (3rd edition)
(Previous No. IC-2919)
Date Published September 1995 P
Printed in Japan

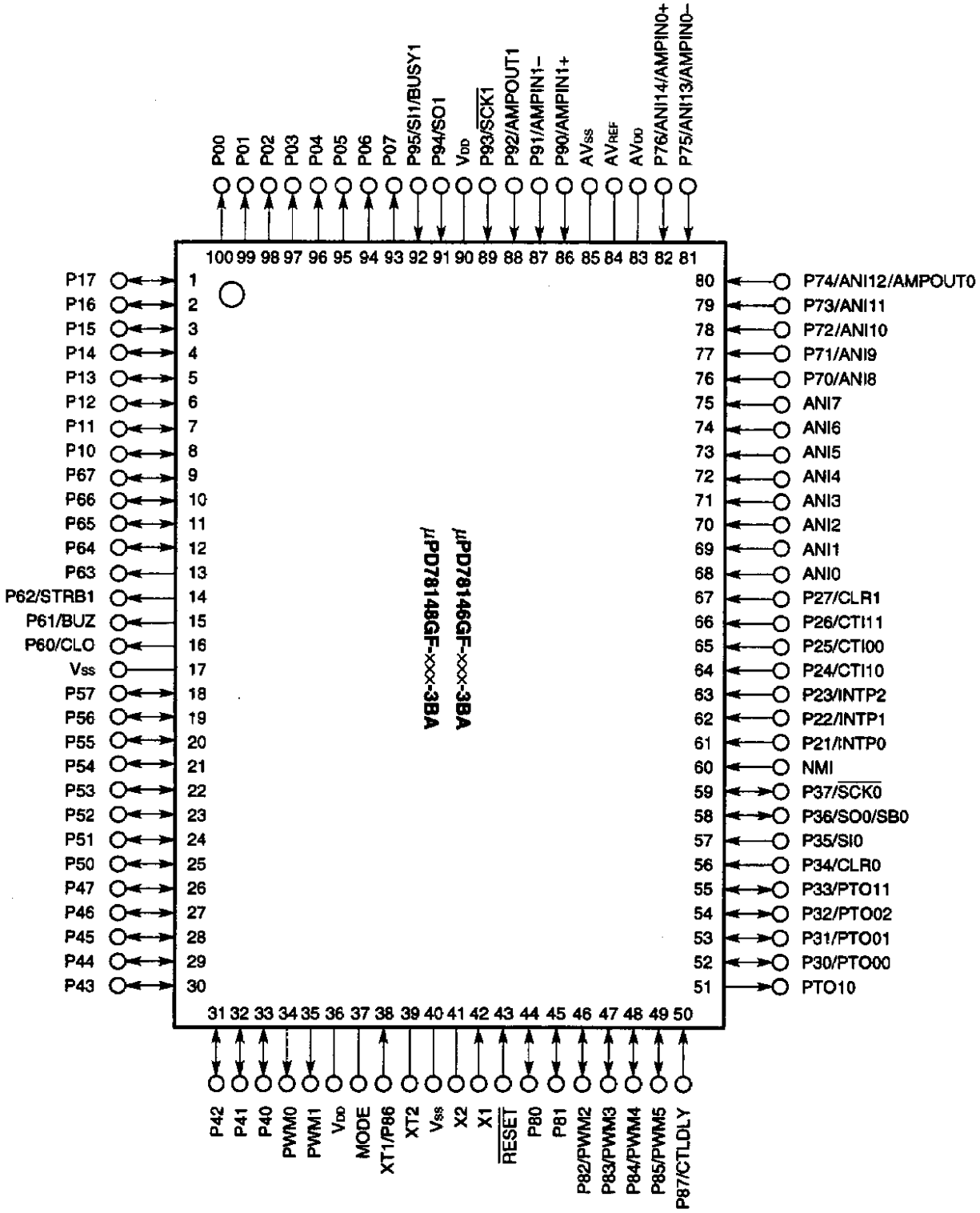
Major changes in this revision are indicated by stars (★) in the margins.

FUNCTIONAL OVERVIEW

Item \ Product		μPD78146	μPD78148
Number of basic instructions		64	
Minimum instruction execution time		0.33 μs (when the microcomputer operates at 12 MHz)	
Internal memory	ROM	24K bytes (24576 × 8 bits)	32K bytes (32768 × 8 bits)
	RAM	688 bytes	816 bytes
General register		8 bits × 8 × 4 banks (memory mapping)	
Instruction set		• 16-bit addition, subtraction, comparison • Signed multiplication (signed 16 bits × unsigned 8 bits) • Unsigned multiplication/division (16 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (transfer, Boolean operation, set, reset, test)	
I/O line		76 in total • Input port : 24 (10 ports can also be used as A/D converter input or analog pins for operational amplifiers.) • Output port : 12 • I/O port : 40	
Super timer unit		• Timer : 16 bits × 3 8 bits × 3 • Counter : 22-bit free running counter (FRC) × 1 6-bit up/down counter (UDC) × 1 • Capture register : 22 bits × 2 16 bits × 3 8 bits × 2 • Compare register : 16 bits × 7 8 bits × 3 • PWM output : 12 bits × 2 (carrier frequency: 46.9/23.4 kHz) 14 bits × 1 (carrier frequency: 5.9 kHz) 8 bits × 3 (carrier frequency: 5.9 kHz)	
Multiplier		Signed 16 bits × signed 16 bits. Operation time: 2.67 μs (when the microcomputer operates at 12 MHz)	
Real-time output port		• Timer-connected port output function • 18 built-in ports in total • The timer for an output trigger can be selected.	
Serial interface		2 built-in channels • SIO0 : Either NEC format serial bus interface (SBI) or 3-wire serial interface can be selected. • SIO1 : Only a 3-wire serial interface is specified. The automatic data send/receive function is provided. (Send/receive buffer: 48 bytes)	
A/D converter		8-bit resolution × 15 inputs (7 inputs can also be used as input ports.)	
Analog circuit		2 operational amplifiers (Each amplifier can be used separately.)	
Interrupt		• Interrupt source: 25 (5 external and 20 internal) • One of the two service modes can be selected (vectored interrupt/macro service).	
Clock		• Dual clock configuration (Either a main system clock or subsystem clock can be selected.) • Can perform counting in the standby mode.	
Standby		STOP/HALT mode	
Pull-up resistor		48, built-in (The use of built-in pull-up resistors can be specified by software.)	

PIN CONFIGURATION (Top View)

100-pin plastic QFP

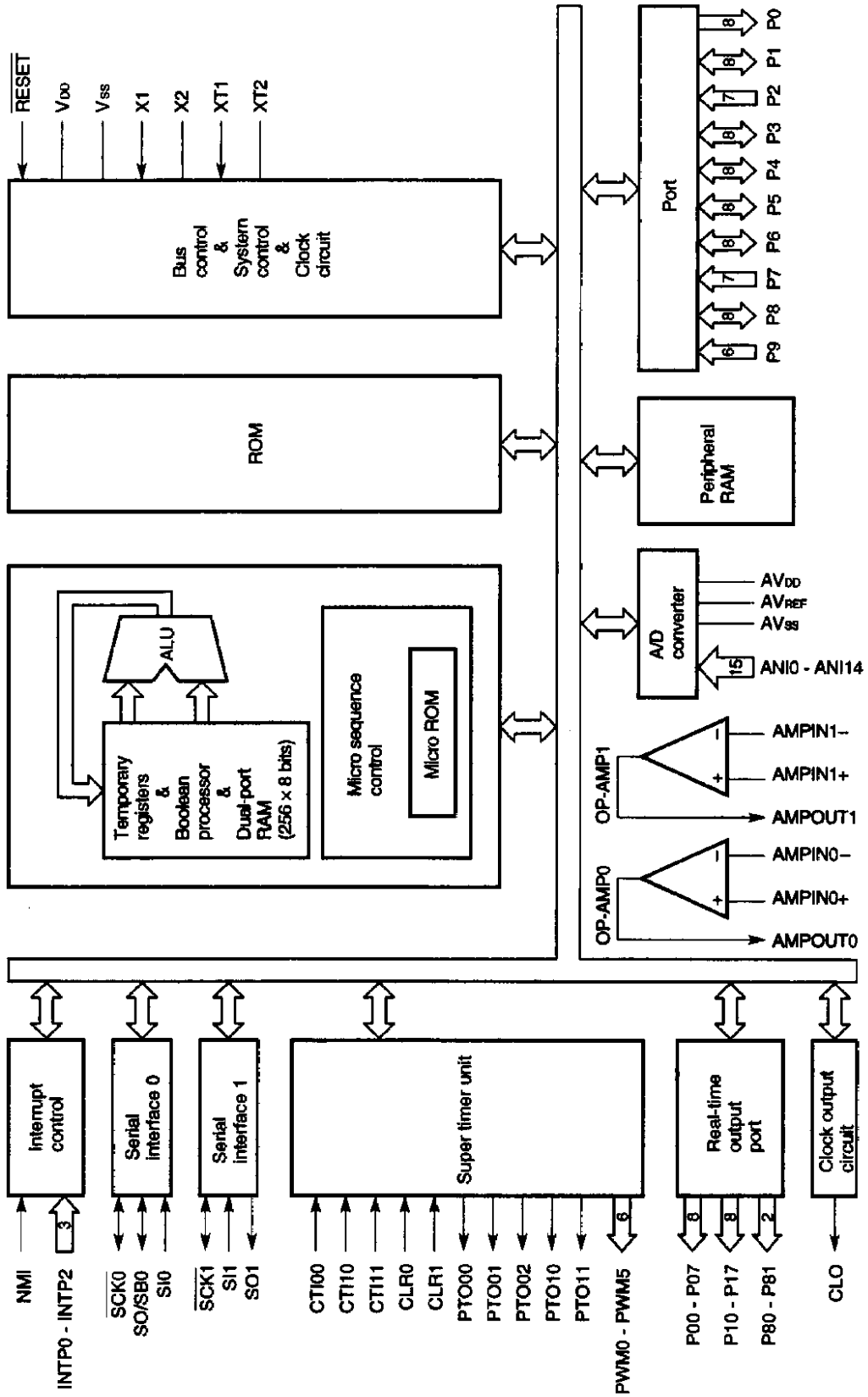


Caution Fix the MODE pin at the ground level.

P00 - P07 : Port 0
P10 - P17 : Port 1
P21 - P27 : Port 2
P30 - P37 : Port 3
P40 - P47 : Port 4
P50 - P57 : Port 5
P60 - P67 : Port 6
P70 - P76 : Port 7
P80 - P87 : Port 8
P90 - P95 : Port 9
PWM0 - PWM5 : Pulse width modulation output 0 - 5
CTI00, CTI10, CTI11
: Capture trigger input 00, 10, 11
CLR0, CLR1 : Timer clear input 0, 1
PTO00 - PTO02, PTO10, PTO11
: Programmable timer output 00 - 02, 10, 11
SI0, SI1 : Serial input 0, 1
SO0, SO1 : Serial output 0, 1
SB0 : Serial bus 0
$\overline{SCK0}$, $\overline{SCK1}$: Serial clock 0, 1
STRB1 : Serial data transfer strobe 1

CTLDLY : Control delay input
ANI0 - ANI14 : Analog input 0 - 14
AMPIN0–, AMPIN1–
: Analog amplifier 0, 1 input (–)
AMPIN0+, AMPIN1+
: Analog amplifier 0, 1 input (+)
AMPOUT0, 1 : Analog amplifier 0, 1 output
NMI : Nonmaskable interrupt
INTP0 - INTP2 : Interrupt from peripherals 0 - 2
CLO : Clock output
BUZ : Buzzer clock
AV_{REF} : Analog reference voltage
AV_{DD} : Analog power supply
AV_{SS} : Analog ground
X1, X2 : Crystal 1, 2 (Main system clock)
XT1, XT2 : Crystal 1, 2 (Subsystem clock)
$\overline{RESET}$: Reset
V_{DD} : Power supply
V_{SS} : Ground
MODE : Mode select

BLOCK DIAGRAM



Phase-out/Discontinued

CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin	I/O	Dual-function pin	Function
P00 - P07	O	–	Port 0 (P0): • Can be specified to output or high impedance in units of 8 bits. • Also function as an 8 bits × 1 or 4 bits × 2 real-time output port.
P10 - P17	I/O	–	Port 1 (P1): • Can be specified to input or output bit by bit. • Can directly drive LED. • The use of built-in pull-up resistors can be specified by software (P10 - P17). • Can be specified as a real-time output port bit by bit.
P21	I	INTP0	Port 2 (P2): • The use of built-in pull-up resistors can be specified by software (P22 - P27).
P22		INTP1	
P23		INTP2	
P24		CTI10	
P25		CTI00	
P26		CTI11	
P27		CLR1	
P30	I/O	PTO00	Port 3 (P3): P30 - P33 : I/O port (Can be specified to input or output bit by bit.) P34, P35 : Input port P36, P37 : I/O port (Can be specified to input or output bit by bit.) • The use of built-in pull-up resistors can be specified by software (P30 - P37).
P31		PTO01	
P32		PTO02	
P33		PTO11	
P34	I	CLR0	
P35		SI0	
P36	I/O	SO0/SB0	
P37		$\overline{SCK0}$	
P40 - P47	I/O	–	Port 4 (P4): • Can be specified to input or output in units of 8 bits. • Can directly drive LED. • The use of built-in pull-up resistors can be specified by software (P40 - P47) .
P50 - P57	I/O	–	Port 5 (P5): • Can be specified to input or output bit by bit. • Can directly drive LED. • The use of built-in pull-up resistors can be specified by software (P50 - P57).

PORT PINS (2/2)

Pin	I/O	Dual-function pin	Function
P60	O	CLO	Port 6 (P6): P60 - P63 : Output port P64 - P67 : I/O port (Can be specified to input or output bit by bit.) • The use of built-in pull-up resistors can be specified by software (P64 - P67).
P61		BUZ	
P62		STRB1	
P63		–	
P64	I/O	–	
P65			
P66, P67		–	
P70	I	ANI8	Port 7 (P7)
P71		ANI9	
P72		ANI10	
P73		ANI11	
P74		AMPOUT0/ANI12	
P75		AMPIN0–/ANI13	
P76		AMPIN0+/ANI14	
P80	I/O	–	Port 8 (P8): P80 - P85 : I/O port (Can be specified to input or output bit by bit.) P86, P87 : Input port • The use of built-in pull-up resistors can be specified by software (P80 - P85). • P80 and P81 can be specified as a real-time output port bit by bit.
P81			
P82		PWM2	
P83		PWM3	
P84		PWM4	
P85		PWM5	
P86	I	XT1	
P87		CTLDLY	
P90	I	AMPIN1+	Port 9 (P9)
P91		AMPIN1–	
P92		AMPOUT1	
P93		$\overline{SCK1}$	
P94		SO1	
P95		SI1	

1.2 NON-PORT PINS (1/2)

Pin	I/O	Dual-function pin	Function
PWM0, PWM1	O	–	Super timer unit PWM output
PWM2 - PWM5	O	P82 - P85	Super timer unit PWM output
CLR0	I	P34	Super timer unit input
CTI00		P25	
CLR1		P27	
CTI10		P24	
CTI11		P26	
PTO00	O	P30	Super timer unit output
PTO01		P31	
PTO02		P32	
PTO10		–	
PTO11	O	P33	Super timer unit output Can output the drive waveform corresponding to VISS/VASS postwriting.
SI0	I	P35	Serial data input 0
SO0	I/O	P36/SB0	Serial data output 0 (3-wire serial I/O mode)
SB0	I/O	P36/SO0	Serial data input/output 0 (SBI mode)
$\overline{SCK0}$	I/O	P37	Serial clock input/output 0
SI1	I	P95	Serial data input 1
SO1	O	P94	Serial data output 1
$\overline{SCK1}$	I/O	P93	Serial clock input/output 1
STRB1	O	P62	Strobe output during automatic SIO1 data transfer
NMI	I	–	Non-maskable interrupt request input
INTP0 - INTP2	I	P21 - P23	External interrupt request input
CTLDLY	–	P87	External time constant circuit connection: The external time constant circuit of CR is connected to this pin when PTO11 is used as VISS/VASS postwriting.
CLO	–	P60	Clock output

NON-PORT PINS (2/2)

Pin	I/O	Dual-function pin	Function
ANI0 - ANI7	Analog input	–	Analog signal input to A/D converter
ANI8 - ANI11		P70 - P73	
ANI12		P74/AMPOUT0	
ANI13		P75/AMPIN0-	
ANI14		P76/AMPIN0+	
AMPIN0–	Analog input	P75/ANI13	Inverted input to operational amplifier 0
AMPIN0+		P76/ANI14	Uninverted input to operational amplifier 0
AMPOUT0	O	P74/ANI12	Operational amplifier 0 output
AMPIN1–	Analog input	P91	Inverted input to operational amplifier 1
AMPIN1+		P90	Uninverted input to operational amplifier 1
AMPOUT1	O	P92	Operational amplifier 1 output
$\overline{\text{RESET}}$	I	–	Reset input
BUZ	O	P61	Buzzer output
AV_{DD}	–	–	Positive power supply of an analog circuit
AV_{SS}	–	–	Ground potential of an analog circuit
AV_{REF}	–	–	Reference voltage input to A/D converter
X1	I	–	Crystal connection for main system clock oscillation.
X2	–		
XT1	I	P86	Crystal connection for subsystem clock oscillation.
XT2	–	–	Crystal connection for clock oscillation
V_{DD}	–	–	Positive power supply of a digital circuit
V_{SS}	–	–	Ground potential of a digital circuit
MODE	–	–	Fixed at the ground level

1.3 INPUT/OUTPUT CIRCUITS AND CONNECTION OF UNUSED PINS

Table 1-1 and Fig. 1-1 show simplified pin input/output circuits.

Table 1-1 I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins

Pin	I/O circuit type	Recommended connection of unused pins
P00 - P07	4	Open
P10 - P17	5-A	Input : Connected to V_{DD} via pull-up resistor Output : Open
P21	2	Connected to V_{DD}
P22 - P27	2-A	
P30 - P33	5-A	Input : Connected to V_{DD} via pull-up resistor Output : Open
P34, P35	2-A	Connected to V_{DD}
P36	10-A	Input : Connected to V_{DD} via pull-up resistor Output : Open
P37	8-A	
P40 - P47	5-A	Input : Connected to V_{DD} via pull-up resistor Output : Open
P50 - P57		
P60 - P63	3	Open
P64 - P67	5-A	Input : Connected to V_{DD} via pull-up resistor Output : Open
P70 - P76	9	Connected to V_{SS}
P80 - P85	5-A	Input : Connected to V_{DD} via pull-up resistor Output : Open
P86	1	Connected to V_{SS} (Bit 6 of the clock control register is reset.)
P87	1	Connected to V_{DD}
P90 - P92	1	Connected to V_{SS}
P93, P94	8	Connected to V_{DD} via pull-up resistor
P95	2	Connected to V_{DD}
PWM0, PWM1	3	Open
PTO10		
ANI0 - ANI7	7	Connected to V_{SS}
$\overline{\text{RESET}}$	2	–
AV_{REF}	–	Connected to V_{SS}
AV_{SS}		

Fig. 1-1 Pin Input/Output Circuits (1/2)

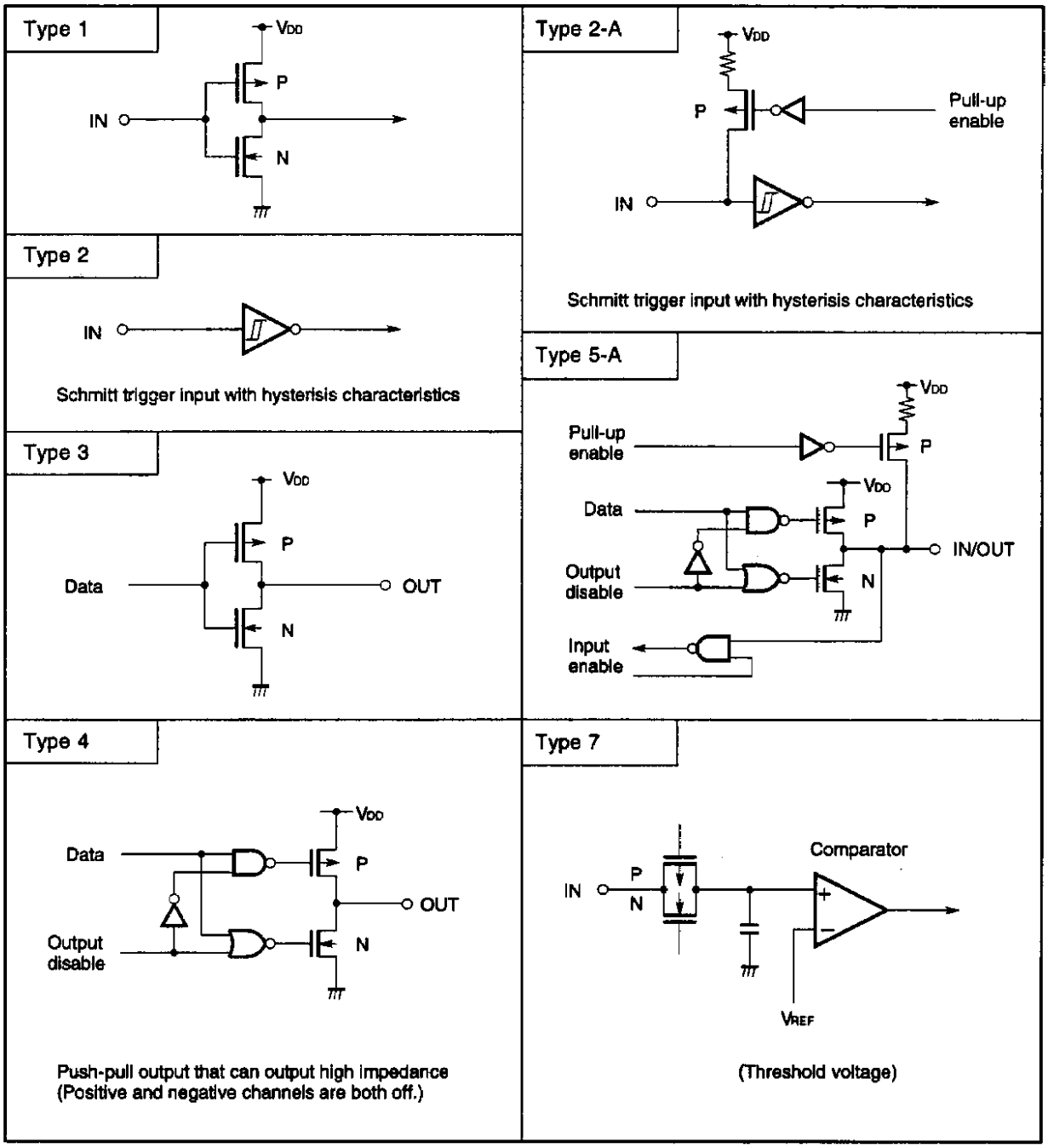
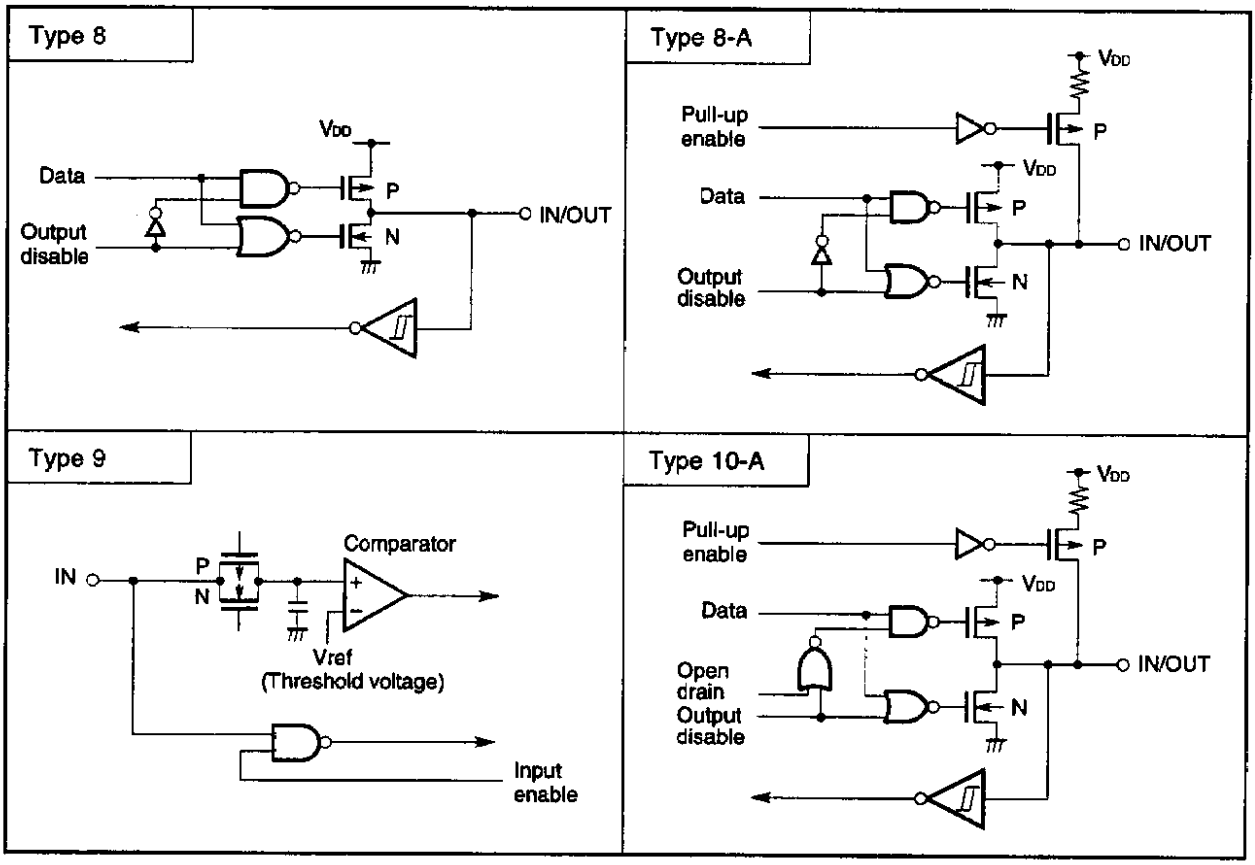


Fig. 1-1 Pin Input/Output Circuits (2/2)



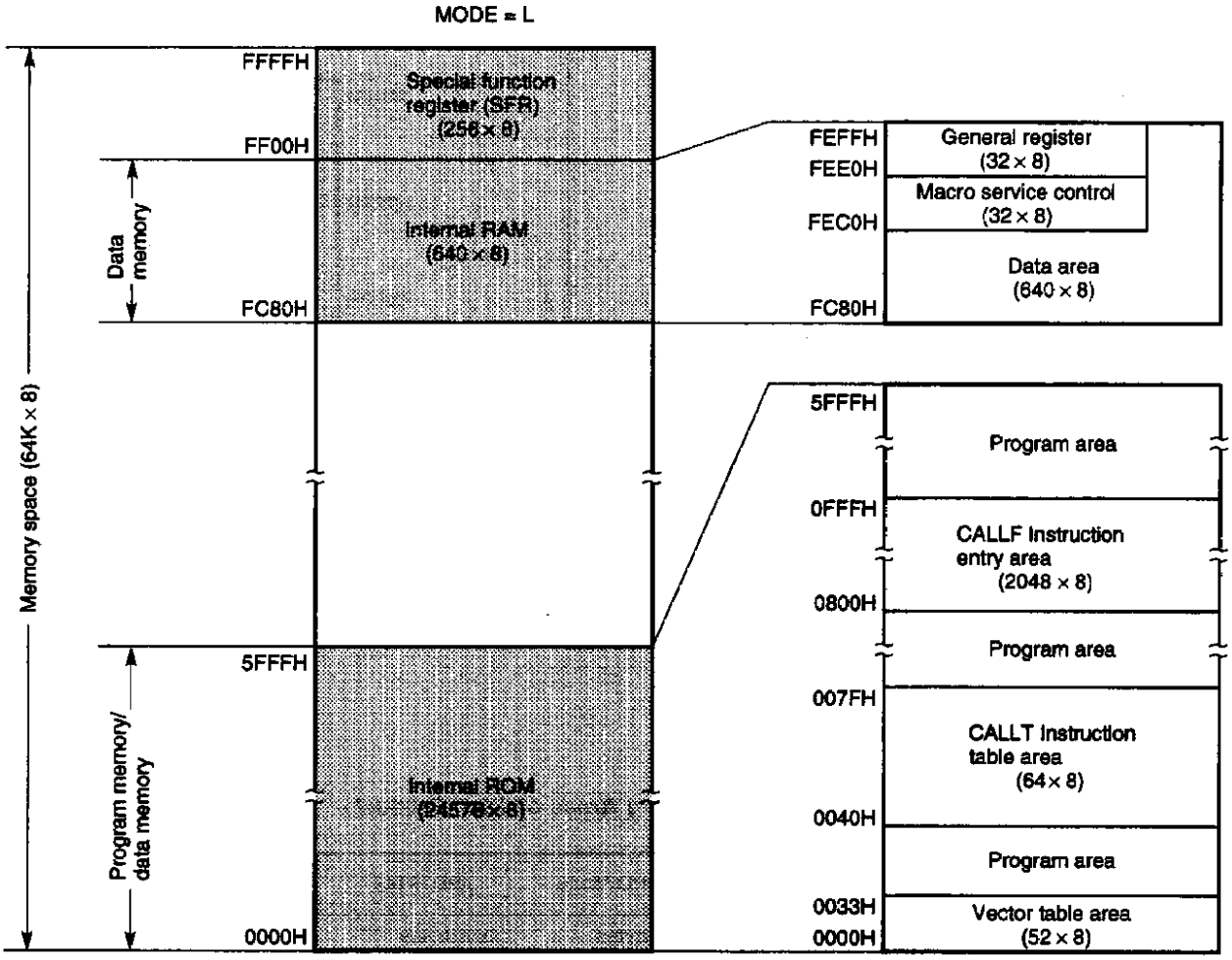
2. CPU ARCHITECTURE

2.1 MEMORY SPACE

Fig. 2-1 and 2-2 show the memory space of the μPD78146 and μPD78148 respectively.

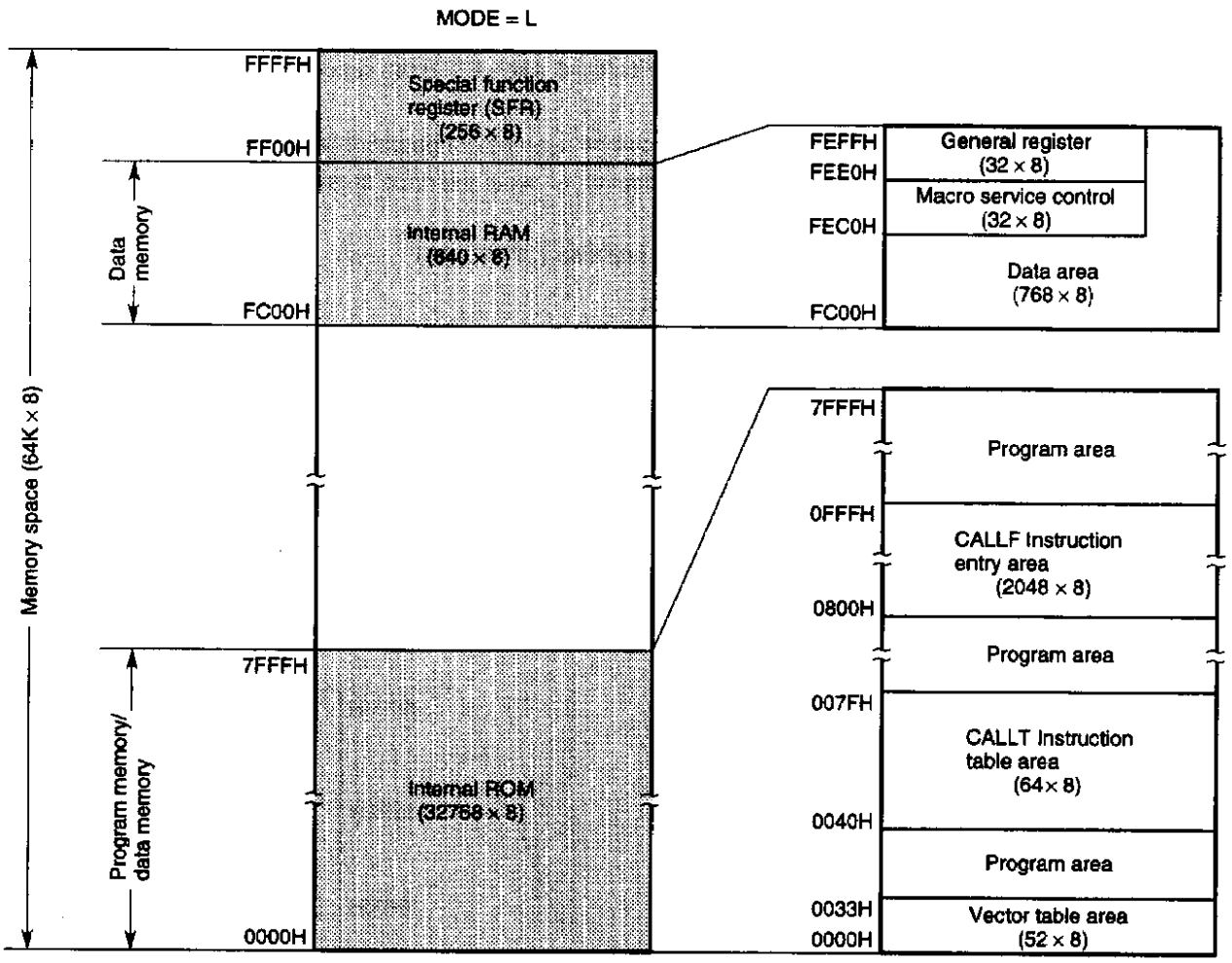
Remark Forty-eight bytes from FF90H to FFBFH can be used as peripheral RAM when they are not used as a buffer for automatic transmission and reception of serial interface channel 1.

Fig. 2-1 Memory Map (μPD78146)



Shaded portions indicate internal memory.

Fig. 2-2 Memory Map (μPD78148)



Shaded portions indicate internal memory.

Table 2-1 Memory Areas of Each Product

Item \ Product	μPD78146	μPD78148
Internal ROM	24K bytes (0000H - 5FFFH)	32K bytes (0000H - 7FFFH)
Internal RAM	688 bytes (FC80H - FEFFH)	816 bytes (FC00H - FEFFH)

2.2 PROCESSOR REGISTER

Registers of the μPD78148 are classified into three groups according to their functions:

- Control register
- General register
- Special function register (SFR)

2.2.1 Control Register

The control register group controls the program sequence, status, and stack memory. There are three control register:

- Program counter (PC) : 16-bit register
- Program status word (PSW) : 8-bit register
- Stack pointer (SP) : 16-bit register

Fig. 2-3, 2-4, and 2-5 show the configuration of each register.

Fig. 2-3 Configuration of Program Counter (PC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Fig. 2-4 Configuration of Program Status Word (PSW)

	7	6	5	4	3	2	1	0
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY

CY.....Carry flag
ISP.....Interrupt priority status flag
RBS0, RBS1.....Register bank selection flag
AC.....Auxiliary carry flag
Z.....Zero flag
IE.....Interrupt request enable flag

Fig. 2-5 Configuration of Stack Pointer (SP)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

2.2.2 General Register

The general register group of the μPD78148 consists of four banks of general registers. Each bank consists of eight 8-bit registers, so there are 32 registers in total. A pair of 8-bit registers can function as a 16-bit register pair.

The general register group is mapped into addresses from FEE0H to FEFFH of the internal RAM space.

Fig. 2-6 shows the configuration of the general register and Table 2-2 shows the correspondence between function names and absolute names.

Fig. 2-6 Configuration of General Register

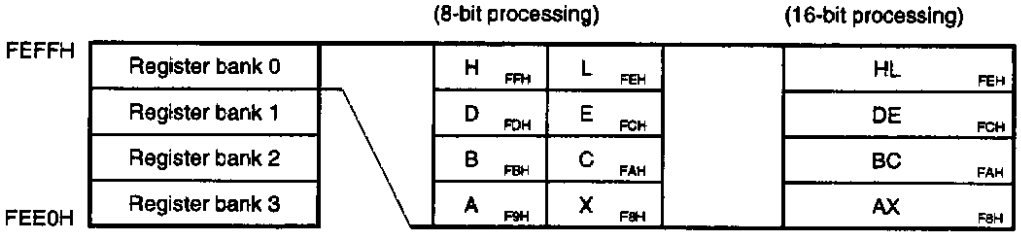


Table 2-2 Correspondence between Function Names and Absolute Names

Function name	Absolute name
X	R0
A	R1
C	R2
B	R3
E	R4
D	R5
L	R6
H	R7

Function name	Absolute name
AX	RP0
BC	RP1
DE	RP2
HL	RP3

2.2.3 Special Function Register (SFR)

The special function register group consists of the registers to which special functions are given such as mode register of the peripheral hardware.

This register group is assigned to the 256-byte space from FF00H to FFFFH. Short direct memory addressing can be applied to the 32-byte area from FF00H to FF1FH, allowing short-word data processing.

Forty-eight bytes from FF90H to FFBFH are used as a buffer for automatic transmission and reception of serial interface channel 1. The area can be accessed in the same way as for peripheral RAM. In SFR addressing, the area cannot be accessed.

Bit manipulation, arithmetic/logical, and move instructions can be executed in all the areas.

Table 2-3 lists the special function registers (SFRs). The items in Table 2-2 mean:

- Abbreviation ..... A symbol indicating the address of a built-in special function register
  This can be specified in the operand field of an instruction.
- R/W ..... Indicates whether data can be read from the special function register and/or data can be written into the register.
  R/W: Can be read and written.
  R : Can be read. (The bits of the register can be tested.)
  W : Can be written.
- Manipulation bit unit ..... Indicates the unit of bits that can be manipulated at one time.
  The SFR which can be manipulated in units of 16 bits can be specified in the sfrp operand. An even address is specified for the address specification.
  The SFR which can be manipulated bit by bit can be specified by a bit manipulation instruction.
- After reset ..... Indicates the status of each register after the $\overline{\text{RESET}}$ input.

Cautions 1. The addresses to which a special function register is not assigned in the area from FF00H to FFFFH can not be accessed.

2. Do not write data into the register which is only used for data reading. If an attempt is made to write data into such registers, the internal circuit may not operate normally.

Table 2-3 Special Function Registers (SFRs) (1/4)

Address	Special function register (SFR) name	Abbreviation	R/W	Manipulation bit unit			After reset
				1	8	16	
FF00H	Port 0	P0	R/W	O	O	–	Undefined
FF01H	Port 1	P1		O	O		
FF02H	Port 2	P2	R	O	O	–	
FF03H	Port 3	P3	R/W	O	O		
FF04H	Port 4	P4		O	O	–	
FF05H	Port 5	P5		O	O		
FF06H	Port 6	P6		O	O	–	F0H
FF07H	Port 7	P7	R	O	O	–	Undefined
FF08H	16-bit timer 0 compare register 0	CR00	R/W	–	–	O	Undefined
FF09H				–	–		
FF0AH	16-bit timer 0 compare register 1	CR01		–	–	O	
FF0BH				–	–		
FF0CH	16-bit timer 0 compare register 2	CR02		–	–	O	
FF0DH				–	–		
FF0EH	16-bit timer 1 compare register 0	CR10		–	–	O	
FF0FH				–	–		
FF10H	16-bit timer 1 compare register 1	CR11		–	–	O	
FF11H				–	–		
FF12H	16-bit timer 1 compare register 2	CR12	R	–	–	O	
FF13H				–	–		
FF14H	16-bit FRC capture register 0	CPT0		–	–	O	
FF15H				–	–		
FF16H	16-bit FRC capture register 1	CPT1		–	–	O	
FF17H				–	–		
FF18H	22-bit FRC capture register 2 (Bits 2 to 17)	CPT2H	R	–	–	O	Undefined
FF19H				–	–		
FF1AH	22-bit FRC capture register 3 Note (Bits 2 to 17)	CPT3H		–	–	O	
FF1BH				–	–		
FF1CH	22-bit FRC capture register 2 (Bits 0, 1, and 18 to 21)	CPT2L		O	O	–	
FF1DH	Prescaler mode register 3	PRM3	R/W	O	O	–	0××××000
FF1EH	16-bit timer 2 compare register	CR20		–	–	O	Undefined
FF1FH				–	–		

Note Address of six low-order bits is FF42H.

Table 2-3 Special Function Registers (SFRs) (2/4)

Address	Special function register (SFR) name	Abbreviation	R/W	Manipulation bit unit			After reset
				1	8	16	
FF20H	Port 0 mode register	PM0	W	–	O	–	FFH
FF21H	Port 1 mode register	PM1		–	O	–	
FF23H	Port 3 mode register	PM3		–	O	–	
FF25H	Port 5 mode register	PM5		–	O	–	
FF26H	Port 6 mode register	PM6		–	O	–	F0H
FF28H	Port 8 mode register	PM8	W	–	O	–	FFH
FF2CH	Multiplicand/multiplication result register	MULL	R/W	–	–	O	Undefined
FF2DH				–	–		
FF2EH	Multiplicator/multiplication result register	MULH		–	–	O	
FF2FH				–	–		
FF30H	16-bit timer register 0	TM0	R	–	–	O	Undefined for up to 16 clocks Cleared to 0 after 17th clock
FF31H				–	–		
FF32H	16-bit timer register 1	TM1		–	–	O	
FF33H				–	–		
FF34H	22-bit free running counter	FRC	R	–	–	O	Undefined for up to 16 clocks Cleared to 0 after 17th clock
FF35H				–	–		
FF36H	16-bit timer register 2	TM2	R	–	–	O	Undefined for up to 16 clocks Cleared to 0 after 17th clock
FF37H				–	–		
FF38H	Timer control register 0	TMC0	R/W	–	O	–	00H
FF39H	Timer control register 1	TMC1	R/W	–	O	–	00H
FF3AH	Capture mode register	CPTM	R/W	–	O	–	30H
FF3BH	7-bit counter register	TM6	R	–	O	–	Undefined
FF3CH	6-bit counter register	TM7		–	O	–	
FF3DH	8-bit timer register 3 Note	TM3	R/W	–	O	–	
FF3EH	8-bit timer 3 compare register	CR30	R/W	–	O	–	Undefined
FF3FH	8-bit timer 3 capture register	CPT30	R	–	O	–	Undefined
FF40H	Register for optional pull-up register	PUO	R/W	O	O	–	00H
FF41H	Port 1 mode control register	PMC1	R/W	O	O	–	00H
FF42H	22-bit FRC capture register 3 (bits 0, 1, and 18 to 21)	CPT3L	R	O	O	–	Undefined
FF43H	Port 3 mode control register	PMC3	R/W	O	O	–	30H
FF44H	16-bit timer 1 compare register 3	CR13		–	–	O	Undefined
FF45H				–	–		
FF46H	Port 1 buffer register	P1L		O	O	–	
FF47H	Port 1 buffer register	P1H		O	O	–	
FF48H	Port 8 mode control register	PMC8		O	O	–	C0H
FF49H	Port 9 mode control register	PMC9	W	–	O	–	27H

Note TM3 can only be read. Writing on TM3 clears TM3 to 00H.

Table 2-3 Special Function Registers (SFRs) (3/4)

Address	Special function register (SFR) name	Abbreviation	R/W	Manipulation bit unit			After reset
				1	8	16	
FF4AH	Port 0 buffer register	P0L	R/W	O	O	–	Undefined
FF4BH	Port 0 buffer register	P0H		O	O	–	
FF4CH	Real-time output port control register	RTPC		O	O	–	00H
FF4DH	Trigger source selection register	TRGS	R/W	O	O	–	00H
FF4EH	Port 8 buffer register	P8L		O	O	–	Undefined
FF4FH	Clock mode register	WM		O	O	–	0×××0×00
FF50H	Input control register	ICR	W	–	O	–	00H
FF51H	Up/down counter count register	UDC	R/W	–	O	–	Undefined
FF52H	Capture compare control register	CRC	W	–	O	–	00H
FF53H	Event divider control register	EDVC	W	–	O	–	Undefined
FF54H	Event counter compare register 1	ECC1		–	O	–	Undefined
FF55H	Event counter compare register 0	ECC0		–	O	–	Undefined
FF56H	Event counter	EC	R	–	O	–	Undefined
FF57H	Prescaler 4 mode register	PRM4	R/W	O	O	–	00H
FF58H	Timer 0 output mode register	TOM0	W	–	O	–	××000000
FF59H	Timer 0 output control register	TOC0	W	–	O	–	00H
FF5AH	Timer 1 output mode register	TOM1	W	–	O	–	80H
FF5BH	Timer 1 output control register	TOC1	R/W[Note]	–	O	–	00H
FF5CH	8-bit timer register 4	TM4	R	–	O	–	Cleared for 16th clock
FF5DH	8-bit timer 4 capture compare register	CR40	R/W	O	O	–	Undefined
FF5EH	8-bit timer register 5	TM5	R	–	O	–	Cleared for 16th clock
FF5FH	8-bit timer 5 compare register	CR50	R/W	O	O	–	Undefined
FF60H	Port 8	P8	R/W	O	O	–	Undefined
FF61H	Port 9	P9	R	O	O	–	
FF62H	Amplifier mode register	AMPM	W	–	O	–	00H
FF63H	Up/down counter compare register	UDCC	W	–	O	–	Undefined
FF64H	A/D conversion mode register 0	ADM0	R/W	O	O	–	00H
FF65H	A/D conversion mode register 1	ADM1	R/W	O	O	–	01H
FF66H	A/D conversion result register 0	ADCR0	R	–	O	–	Undefined
FF67H	A/D conversion result register 1	ADCR1	R	–	O	–	Undefined
FF70H	PWM control register 0	PWMC0	R/W	O	O	–	05H
FF71H	PWM control register 1	PWMC1	W	–	O	–	40H
FF72H	PWM0 modulo register	PWM0	W	–	–	O	Undefined
FF73H				–	–		
FF74H	PWM1 modulo register	PWM1		–	–	O	
FF75H				–	–		

Note Only bit 0 of TOC1 can be read.

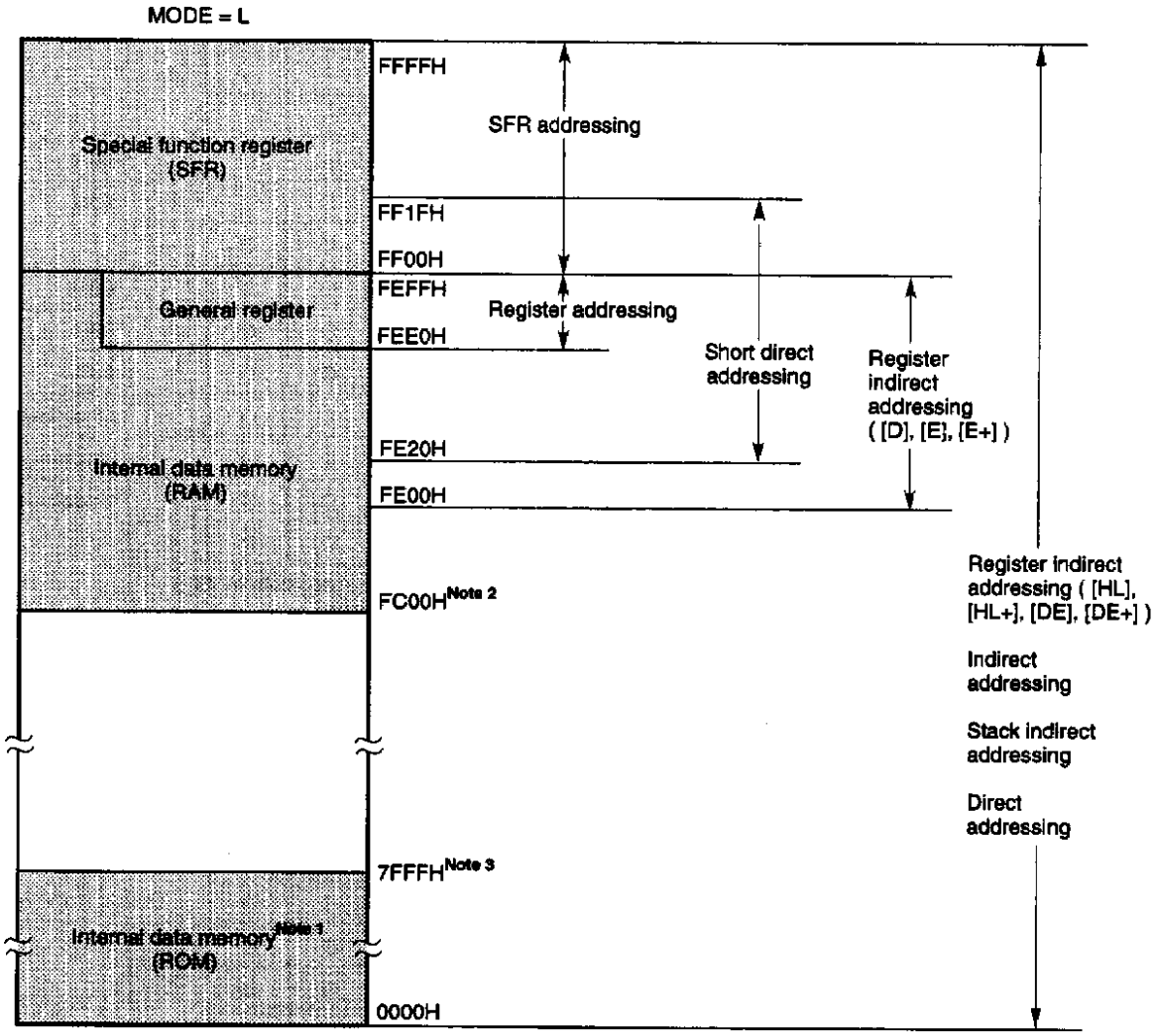
Table 2-3 Special Function Registers (SFRs) (4/4)

Address	Special function register (SFR) name	Abbreviation		R/W	Manipulation bit unit			After reset
					1	8	16	
FF76H	PWM2 modulo register	PWM2		W	–	O	–	Undefined
FF77H	PWM3 modulo register	PWM3			–	O	–	
FF7AH	PWM4 modulo register	PWM4			–	O	–	
FF7BH	8-bit timer 4 capture register	CR41		R	–	O	–	Undefined
FF7CH	PWM5 modulo register	PWM5		W	–	–	O	
FF7DH					–	–		
FF7EH	Timer control register 2	TMC2			–	O	–	00H
FF7FH	Clock output mode register	CLOM		R/W	O	O	–	00H
FF80H	Serial interface mode 0 register	CSIM0			O	O	–	
FF81H	Serial interface mode 1 register	CSIM1		R/W	O	O	–	00H
FF82H	Serial bus interface control register	SBIC		R/W	O	O	–	00H
FF84H	Automatic transfer control register 1	ADTC1		R/W	O	O	–	00H
FF85H	Automatic transfer pointer 1	ADTP1			O	O	–	Undefined
FF86H	Serial shift register 0	SIO0		R/W	O	O	–	Undefined
FF87H	Serial shift register 1	SIO1		R/W	O	O	–	Undefined
FF90H to FFBFH	SIO1 buffer area/general RAM	–		R/W	O	O	O	
					Access impossible by SFR addressing			
FFC0H	Standby control register	STBC		R/W	–	O	–	0000×000
FFC4H	Memory mapping register	MM		W	–	O	–	A0H
FFE0H	Interrupt request flag register	IF0L	IF0	R/W	O	O	O	00H
FFE1H		IF0H			O	O		
FFE2H		IF1L			O	O	–	
FFE4H	Interrupt mask register	MK0L	MK0		O	O	O	FFH
FFE5H		MK0H			O	O		
FFE6H		MK1L			O	O	–	
FFE8H	Priority specification flag register	PR0L	PR0		O	O	O	
FFE9H		PR0H			O	O		
FFEAH		PR1L			O	O	–	
FFECH	Interrupt service mode register	ISM0L	ISM0		O	O	O	00H
FFEDH		ISM0H			O	O		
FFEEH		ISM1L			O	O	–	
FFF4H	External interrupt mode register	INTM0		R/W	O	O	–	50H
FFF5H	External capture mode register	INTM1			O	O	–	01H
FFFBH	Clock control register	CC		R/W	O	O	–	00H

2.3 DATA MEMORY ADDRESSING

Fig. 2-7 shows the data memory map of the μPD78148 and the applied addressing scheme. With these various addressing, μPD78148 programs can be coded efficiently.

Fig. 2-7 Memory Map and Addressing of Data Memory



Notes 1. Do not place the stack pointer in the SFR area or ROM area.

2. FC80H for μPD78146

3. 5FFFH for μPD78146

Shaded portions indicate internal memory.

Caution Forty-eight bytes from FF90H to FFBFH are used as a buffer for automatic transmission and reception of serial interface channel 1. This area can be accessed in the same way as for peripheral RAM. In SFR addressing, the area cannot be accessed.

3. PERIPHERAL HARDWARE FUNCTIONS

3.1 PORT FUNCTIONS

The μPD78148 is provided with the ports shown Fig. 3-1, which enable a wide variety of control capabilities. Table 3-1 indicates the functions of the ports. The use of a built-in pull-up resistor can be specified by software.

Fig. 3-1 Port Configuration

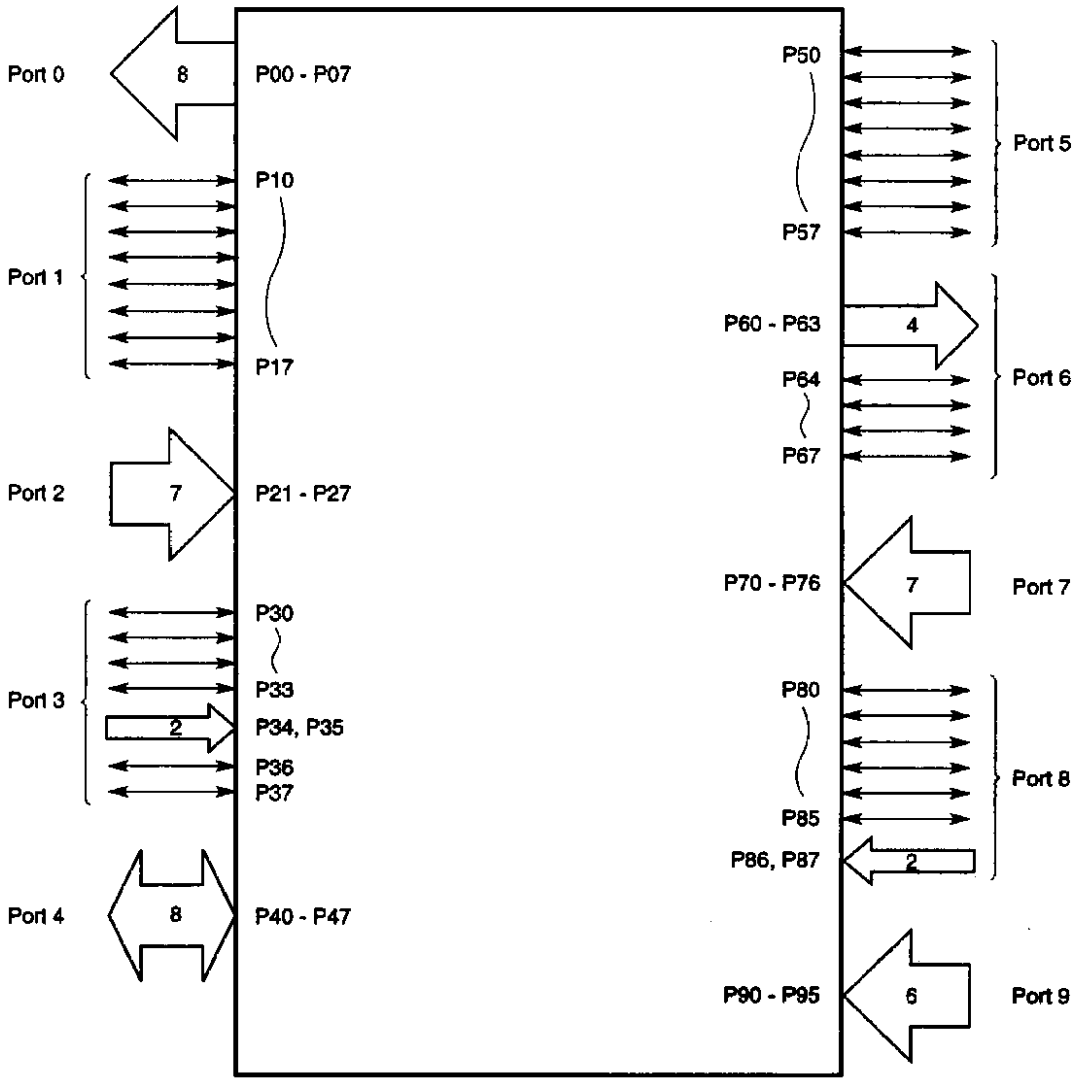


Table 3-1 Port Functions

Port	Pin	I/O	Function
Port 0	P00 - P07	Output	8-bit output port • Also functions as a real-time output port. • Specifiable in units of 8 bits for output or high impedance • Capable of direct transistor drive
Port 1	P10 - P17	I/O	8-bit I/O port • Also functions as a real-time output port. • Specifiable for input or output bit by bit. • Can directly drive an LED.
Port 2	P21	Input	7-bit input port • Also functions as external interrupt pins and timer input pins.
	P22 - P27	Input	
Port 3	P30 - P33	I/O	8-bit I/O port • Also functions as timer output pins and a serial I/O pin (SIO0). • Allows input or output to be specified bit by bit for P30 - P33, P36, and P37.
	P34, P35	Input	
	P36, P37	I/O	
Port 4	P40 - P47	I/O	8-bit I/O port • Specifiable for input or output in units of 8 bits. • Can directly drive an LED.
Port 5	P50 - P57	I/O	8-bit I/O port • Specifiable for input or output bit by bit. • Can directly drive an LED.
Port 6	P60 - P63	Output	8-bit I/O port • Allows input or output to be specified bit by bit for P64 - P67.
	P64 - P67	I/O	
Port 7	P70 - P76	Input	7-bit input port • Also functions as analog input pins and operational amplifier (AMP0) I/O pins.
Port 8	P80 - P85	I/O	8-bit I/O port • Also functions as a real-time output port, PWM output pins, and subsystem clock. • Allows input or output to be specified bit by bit for P80 - P85.
	P86, P87	Input	
Port 9	P90 - P95	Input	6-bit input port • Also functions as operational amplifier (AMP1) I/O pins and a serial I/O pin (SIO1).

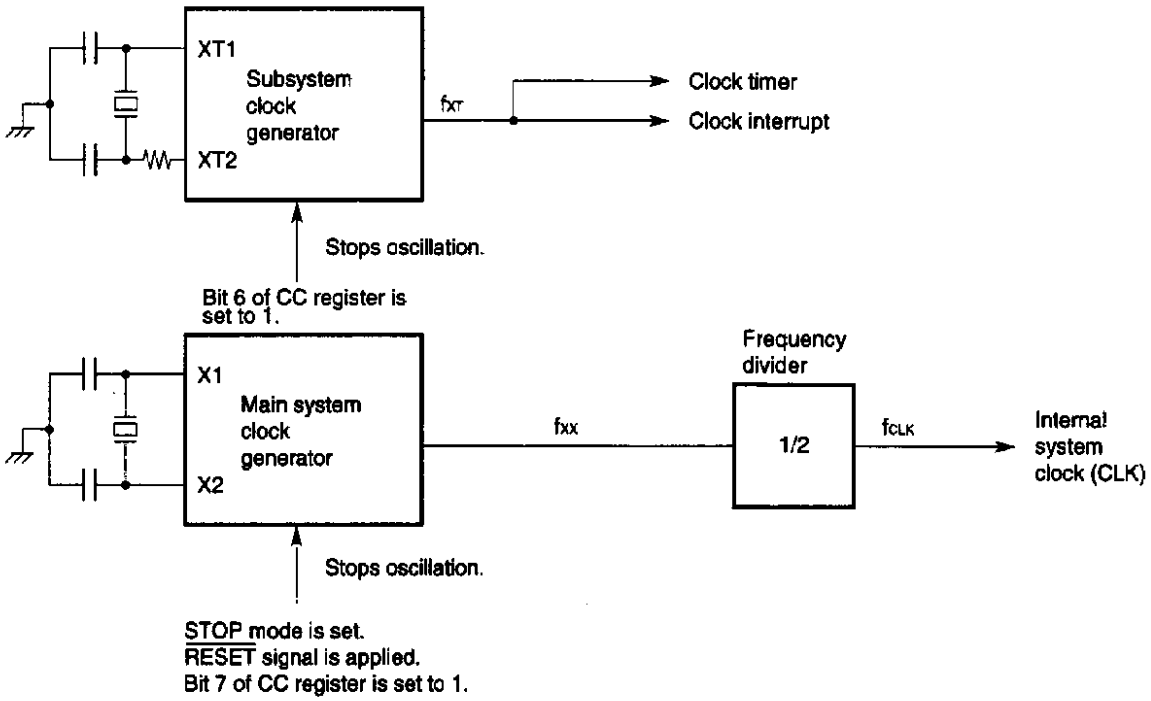
Caution Those ports that allow the specification of a pull-up resistor on a bit-by-bit basis can contain a pull-up resistor only in the input mode.

3.2 CLOCK GENERATOR

The clock generator generates and controls an internal system clock (CLK) supplied to the CPU.

The clock generator is configured as shown in Fig. 3-2.

Fig. 3-2 Block Diagram of the Clock Generator ★



Remarks 1. fXX : Crystal oscillator frequency of the main system clock

2. fXT : Crystal oscillator frequency of the subsystem clock

3. fCLK: Internal system clock frequency

The main system clock generator oscillates with a crystal or ceramic resonator connected to the X1 and X2 pins.

The system clock generator stops oscillation when the standby mode (STOP) is set, a $\overline{\text{RESET}}$ signal is applied, or bit 7 of the clock control register is set.

The subsystem clock generator oscillates with a crystal connected to the XT1 and XT2 pins.

The subsystem clock generator stops oscillation when bit 6 of the clock control register is set; the setting of the STOP mode or $\overline{\text{RESET}}$ signal input has no effect.

The subsystem clock is used mainly for the clock circuit and an interrupt (INTW) generated at regular intervals.

The frequency divider divides a system clock generator output signal (fXX, fXT) by two to produce an internal system clock (fCLK).

Fig. 3-3 shows the external circuitry of the main system clock generator. Fig. 3-4 shows the external circuitry of the subsystem clock generator.

Fig. 3-3 External Circuitry of the Main System Clock Generator

(a) Crystal/ceramic oscillator

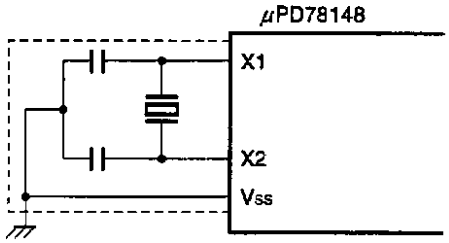
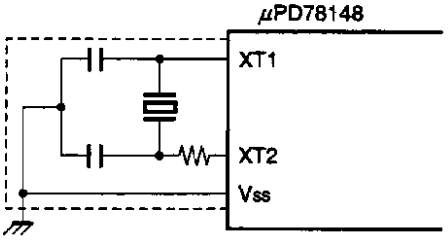


Fig. 3-4 External Circuitry of the Subsystem Clock Generator

(a) Crystal oscillator



Caution When using the main system clock generator and subsystem clock generator, run wires in broken lines ( ) in Figs. 3-3 and 3-4 according to the following rules to avoid adverse effects caused by stray capacitance or other factors:

- **Connect components as short as possible.**
- **Never cause the wires to cross other signal lines or run near a line carrying a large varying current.**
- **Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as Vss at all times. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

Note, in particular, that the subsystem clock generator is a low-amplification circuit for reduced current consumption.

3.3 REAL-TIME OUTPUT PORT (RTP)

A real-time output port (RTP) consists of two buffers: a port output latch and buffer register.

A real-time output function is available which, upon generation of a timer interrupt or external interrupt, transfers data in the buffer register by hardware to the output latch for output. A port used for this function is called an RTP.

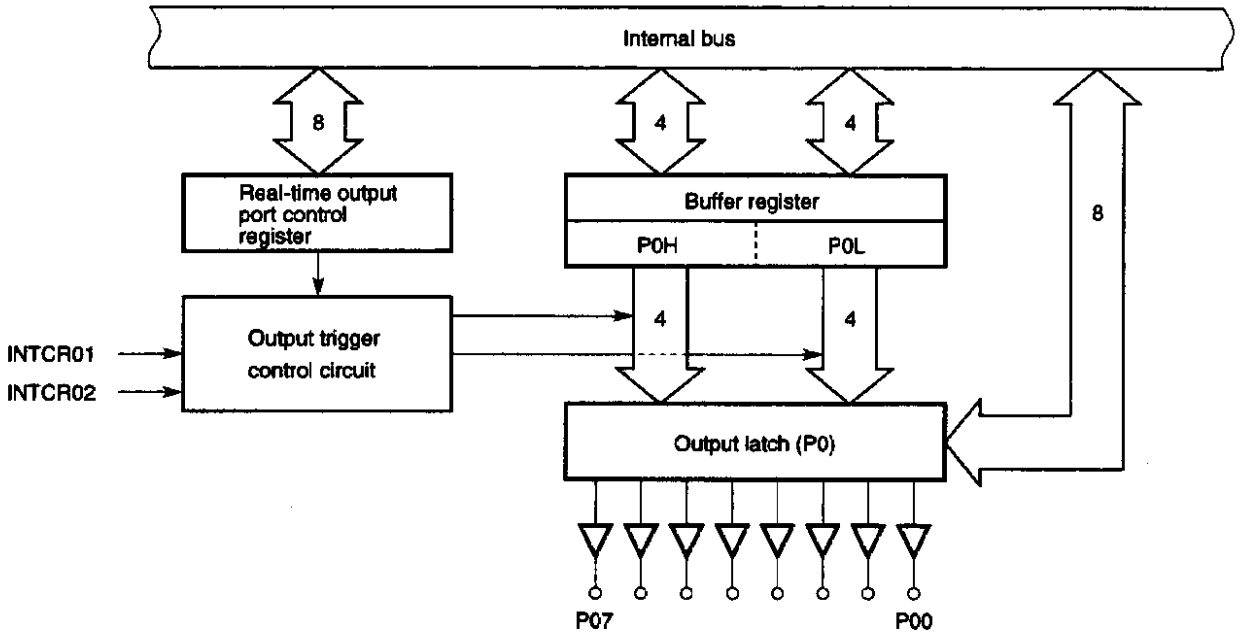
The μPD78148 contains the real-time output ports listed in Table 3-2.

Table 3-2 RTP Bit Configuration

	Number of real-time output data bits	Number of bits specifiable as RTP
RTP0	4 bits × 2 channels 8 bits × 1 channel	In unit of 4 bits
RTP1	4 bits × 2 channels	Bit by bit
RTP8	2 bits × 1 channel	

Figs. 3-5 to 3-7 show the block diagrams of RTP0, RTP1 and RTP8. Fig. 3-8 shows the types of RTP output trigger sources.

Fig. 3-5 Block Diagram of RTP0



Remark INTCR01, INTCR02 : Signal issued when the contents of the 16-bit timer 0 (TM0) and compare register (CR01, CR02) match

Fig. 3-6 Block Diagram of RTP1

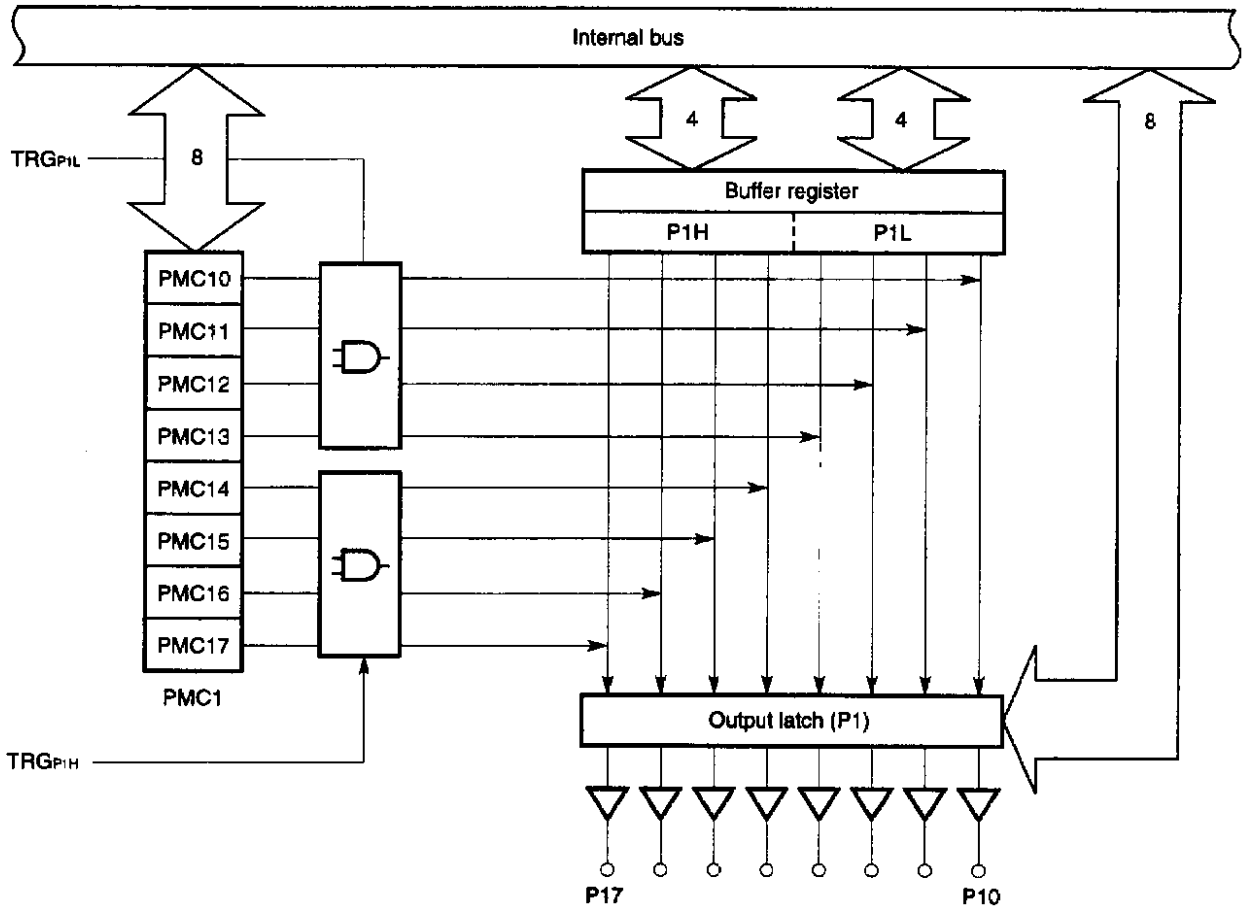


Fig. 3-7 Block Diagram of RTP8

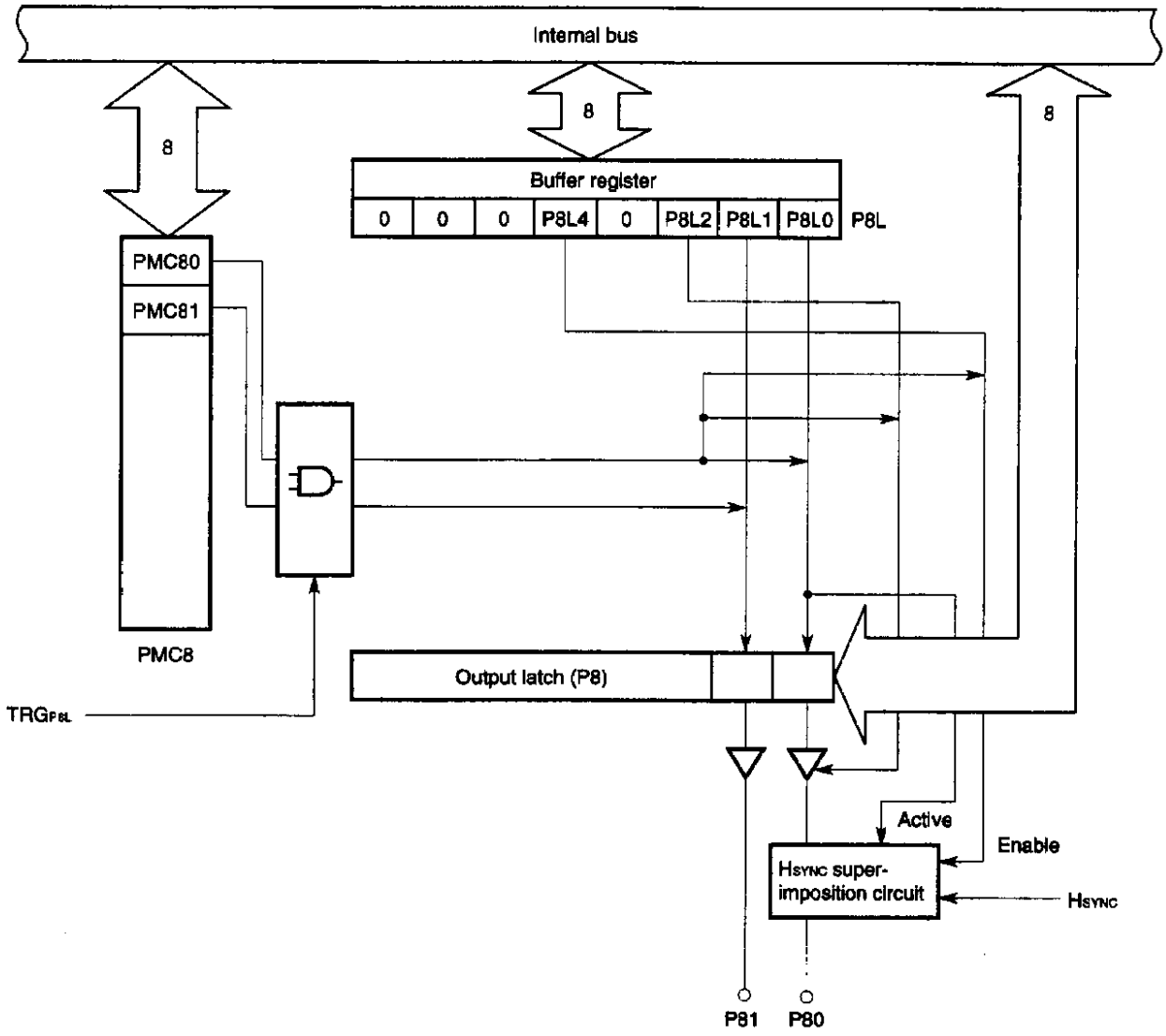
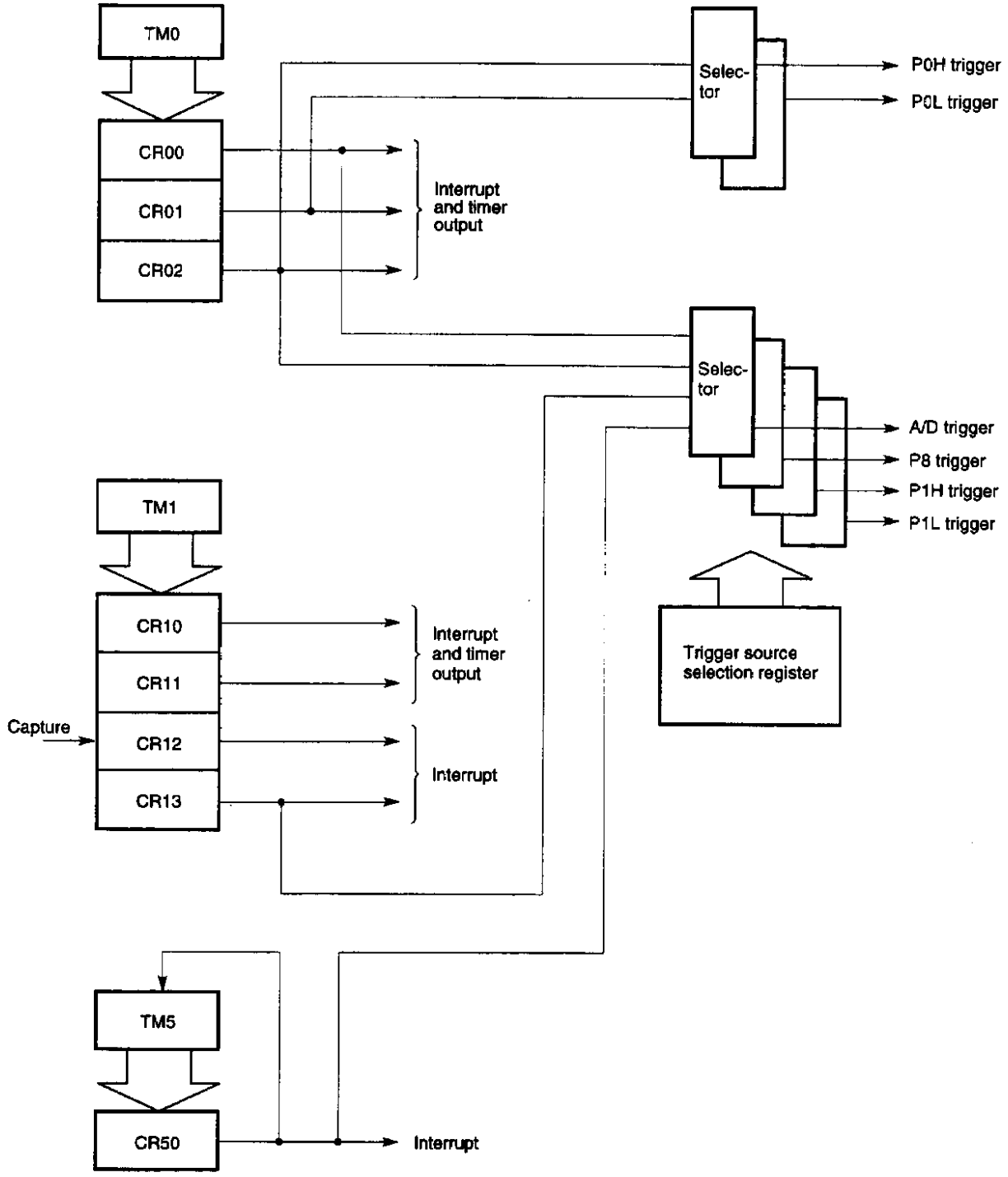


Fig. 3-8 Types of RTP Output Trigger Sources

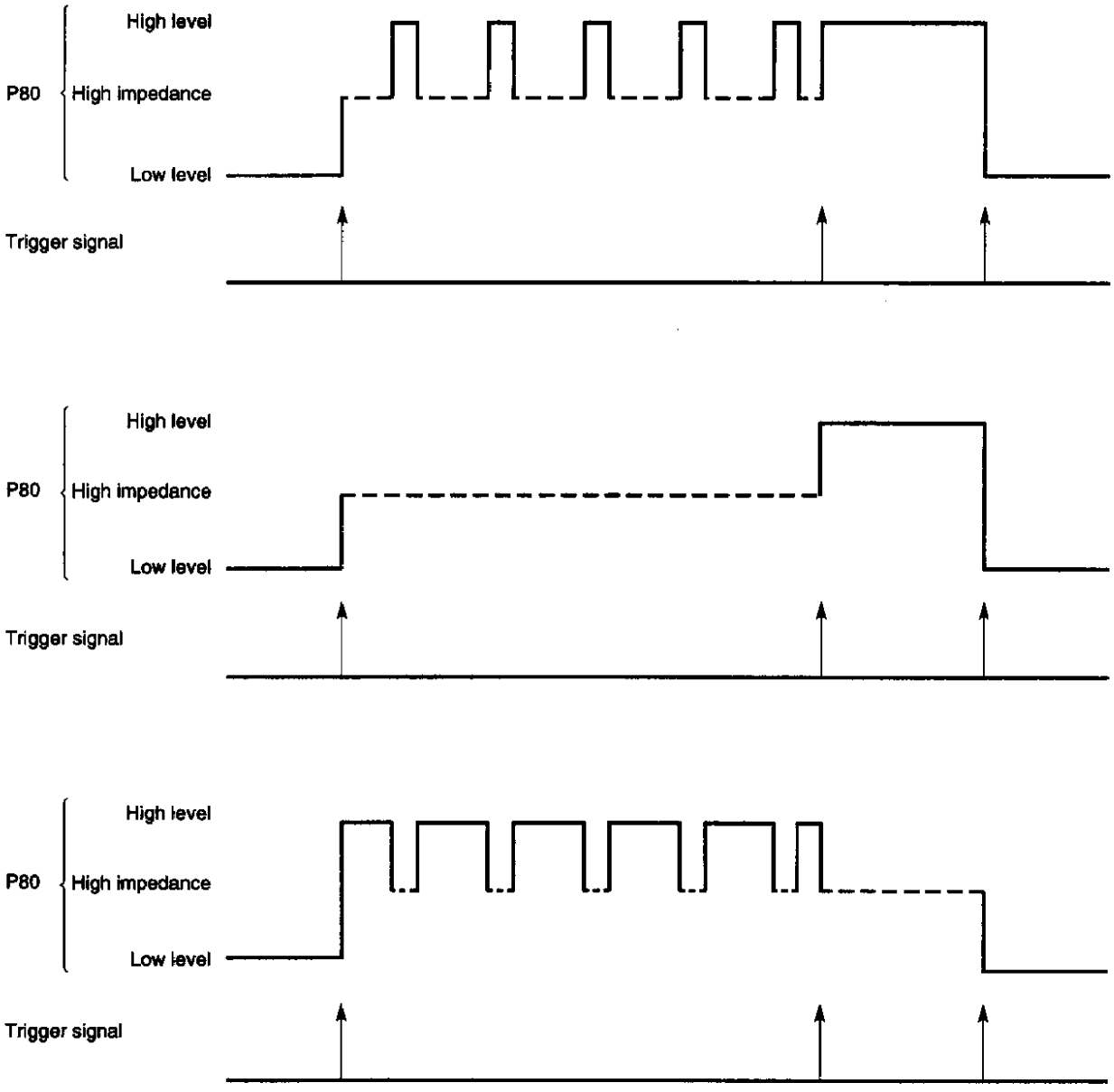


For RTP1 or RTP8, an arbitrary output trigger can be selected from INTCR00, INTCR02, INTCR13, and INTCR50.

RTP8 allows the value of the low level, high level, or high impedance to be output in the real-time mode. Furthermore, RTP8 allows a horizontal synchronizing signal to be superimposed, so that RTP8 can be used to generate a pseudo vertical synchronizing signal.

Fig. 3-9 indicates an RTP8 operation timing chart.

Fig. 3-9 RTP8 Operation Timing



3.4 SERIAL INTERFACE

The μPD78148 contains two channels (channels 0 and 1) for a serial interface:

Channel 0: Three-wire serial interface, Serial bus interface (SBI)
Channel 1: Three-wire serial interface with an automatic transfer function

- **Three-wire serial interface**
  The three-wire serial interface mode enables 8-bit data transfer using three lines: serial clock ($\overline{SCK0}$, $\overline{SCK1}$), serial data input (SI0, SI1), and serial output (SO0, SO1). This interface is useful for connecting a display controller and peripheral I/O device containing the conventional clock synchronous serial interface.

- **Serial bus interface (SBI)**
  The serial bus interface mode enables 8-bit data transfer to and from more than one device by using two lines: serial clock ($\overline{SCK0}$) and serial data bus (SB0). Following the NEC original format, transferred data can be identified as an "address", "command", or "data" by serial data manipulation.

- **Three-wire serial interface with automatic transfer function**
  This interface mode has an automatic transfer function added to a three-wire serial interface mode that transfers 8-bit data by using three lines (serial clock ($\overline{SCK1}$), serial data input (SI1), and serial output (SO1)).
  The automatic transfer function sends and receives up to 48-byte data. With this function, data can be transferred by hardware to and from a device for on-screen display (OSD) or a device containing a display controller/driver, independently of the CPU. Thus, loads on software can be reduced.

Fig. 3-10 shows the block diagram of channel 0, and Fig. 3-11 shows the block diagram of channel 1.

Fig. 3-10 Block Diagram of Serial Interface Channel 0

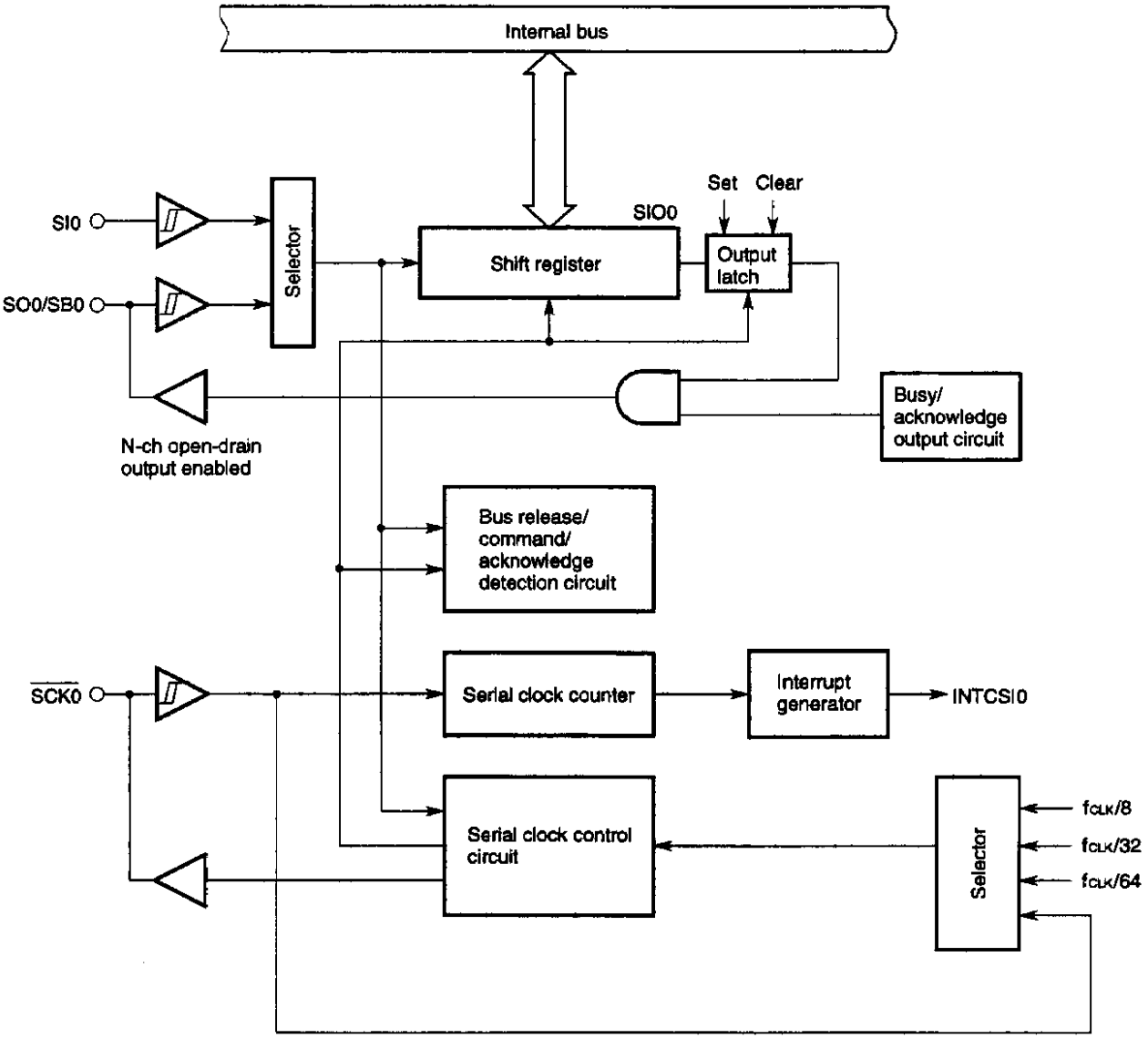
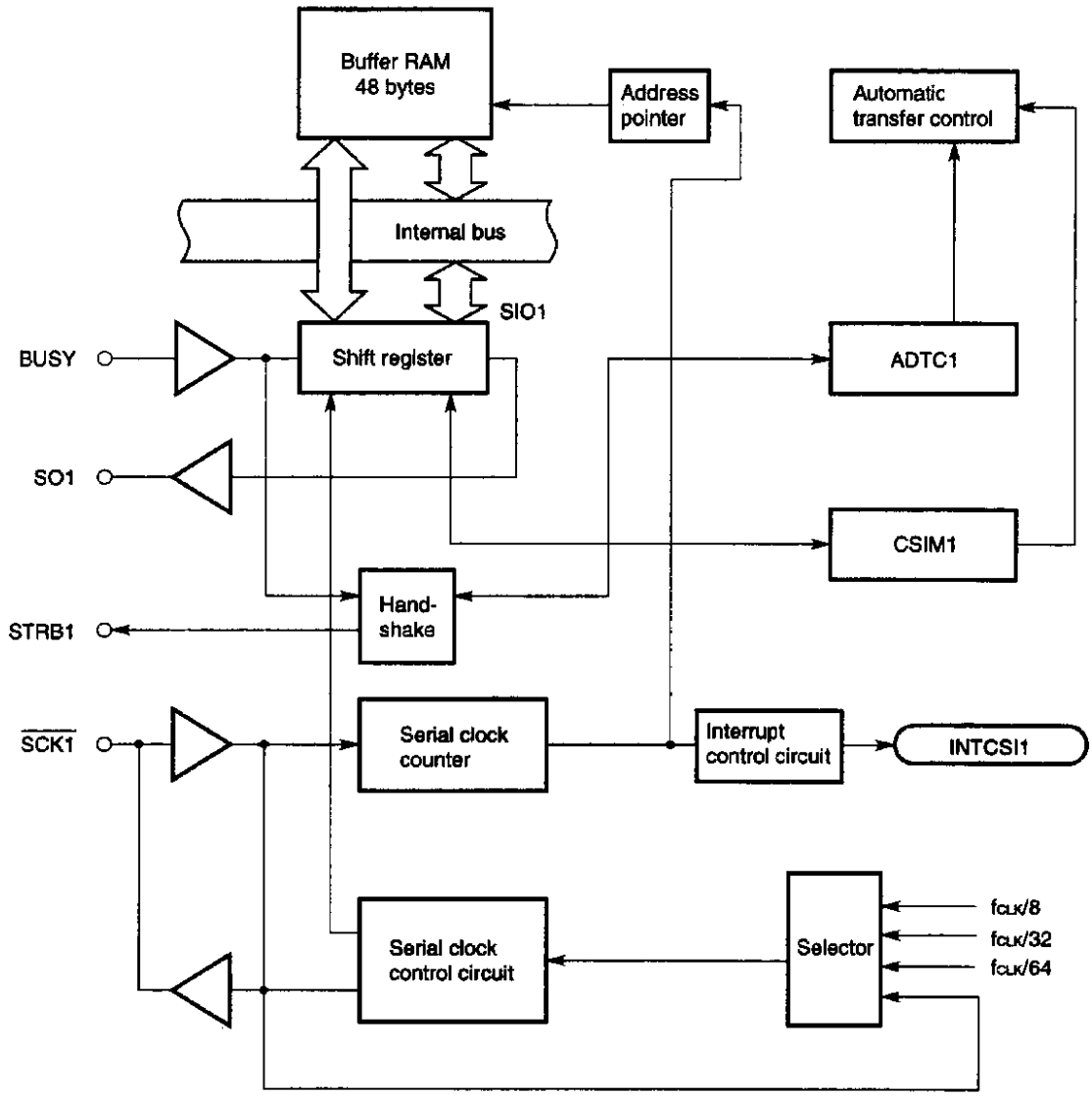


Fig. 3-11 Block Diagram of Serial Interface Channel 1



3.5 SUPER TIMER UNIT

The μPD78148 contains a super timer unit which consists of the following timer units.

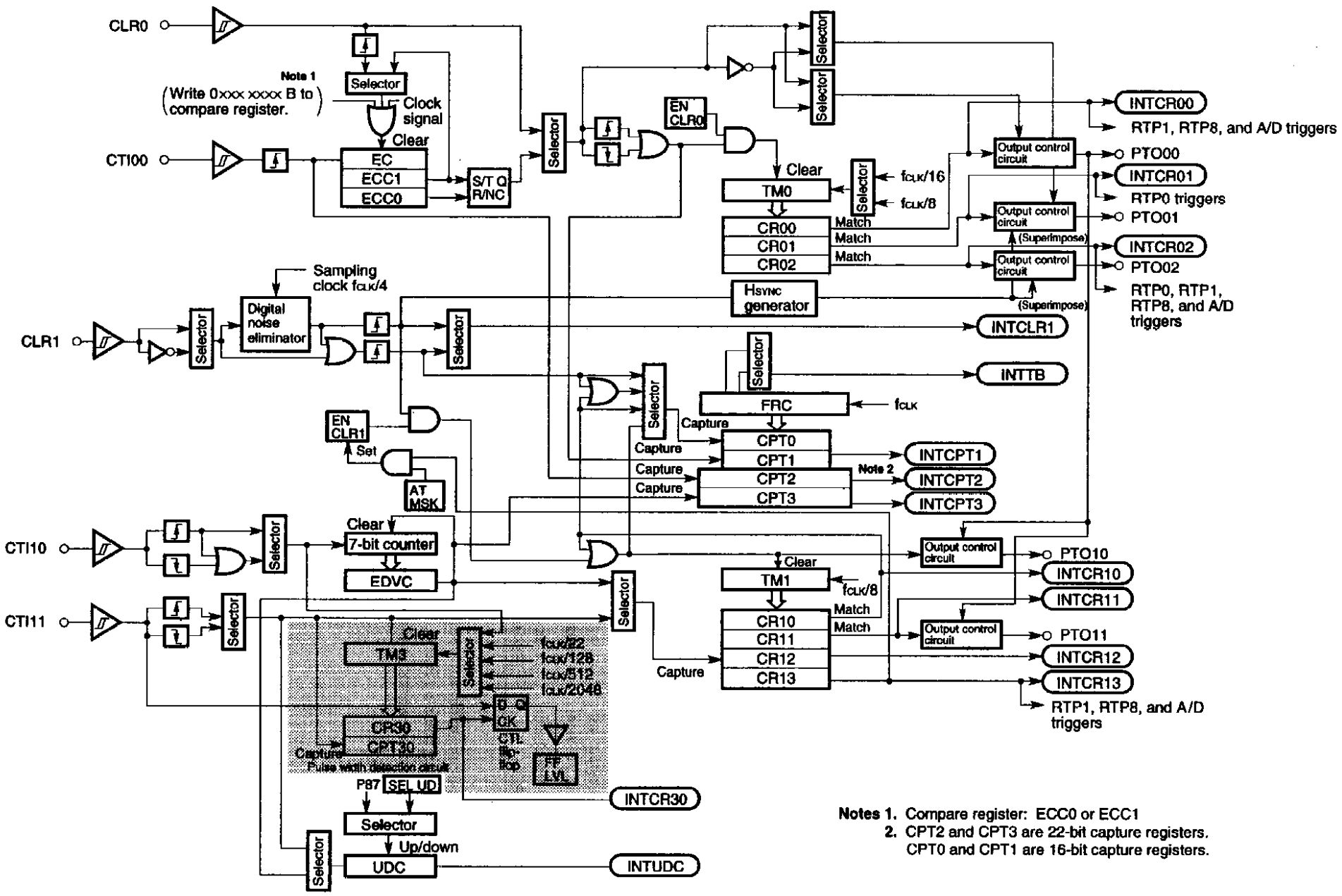
Table 3-3 Components of the Super Timer Unit

Unit name	Timer/counter	Register	Remarks
Timer 0	16-bit timer × 1 (TM0)	• 16-bit compare register × 3	Contains a 6-bit event counter. Contains H_{SYNC} generator.
Free running counter	22-bit counter × 1 (FRC)	• 22-bit capture register × 2 • 16-bit capture register × 2	Contains a digital noise eliminator. ($\overline{V_{SYNC}}$ separation circuit)
Timer 1	16-bit timer × 1 (TM1)	• 16-bit compare register × 3 • 16-bit capture register × 1	7-bit event divider × 1 Contains a VISS/VASS detection circuit.
	8-bit count register × 1 (TM3)	• 8-bit compare register × 1 • 8-bit capture register × 1	
Timer 2	16-bit timer × 1 (TM2)	• 16-bit compare register × 1	Usable as an interval timer
Timer 4	8-bit timer × 1 (TM4)	• 8-bit capture/compare register × 1 • 8-bit capture register × 1	Applicable as remote controller signal reception (capture function using INTP2)
Timer 5	8-bit timer × 1 (TM5)	• 8-bit compare register × 1	Usable as a real-time output port output trigger and A/D conversion start trigger
Up/down counter	6-bit up/down counter (UDC)	• 6-bit compare register × 1	Usable as a real-time counter
PWM output unit (PWM0, PWM1)	12-bit counter × 1 (PWM0)	• 16-bit modulo register × 1 (with higher 12 bits used)	Variable active level of output Carrier frequency selectable (23.4 kHz/46.9 kHz)
	12-bit counter × 1 (PWM1)	• 16-bit modulo register × 1 (with higher 12 bits used)	
PWM output unit (PWM2 - PWM4)	8-bit counter × 3 (PWM2 - PWM4)	• 8-bit modulo register × 3	Carrier frequency: 5.9 kHz
PWM output unit (PWM5)	14-bit counter × 1 (PWM5)	• 16-bit modulo register × 1 (with higher 14 bits used)	Carrier frequency: 5.9 kHz 14-bit precision PWM pulse

The most significant feature of the super timer unit of the μPD78148 includes timer 0 (TM0), the free running counter (FRC), and timer 1 (TM1).

Fig. 3-12 shows the configuration of these timer units. The timer units facilitate VCR index search and servo control using software.

Fig. 3-12 Block [illegible], Timer 1, and Free Running Counter



Notes 1. Compare register: ECC0 or ECC1
2. CPT2 and CPT3 are 22-bit capture registers.
CPT0 and CPT1 are 16-bit capture registers.

3.5.1 Super Timer Unit Function

(1) Timer 0 unit (TM0): 16-bit timer

Timer 0 is a timer unit suitable for pulse output timing control. By using an external input signal as a trigger, TM0 enables the timing of pulse output to be delayed by programming. Three channels of pulse output are available, and can be used, for example, for VCR sound and video head switching signals.

A timer count clock can be selected from $f_{CLK}/8$ and $f_{CLK}/16$.

Timer 0 can be used as an output trigger for real-time output ports 0, 1, and 8, and a conversion trigger for A/D converter 1.

(2) Timer 1 unit (TM1): 16-bit timer

Timer 1 is a timer unit for generating a reference signal for internal processing. Timer 1 can be used for various applications such as pulse output and reference signal generation using external trigger input. Timer 1 also allows programmable delay pulse output as with timer 0. Timer 1 contains timer 3 (TM3), which is an 8-bit timer. Timer 3 can be used for external pulse width detection and period measurement.

Timer 1 contains a function that releases a timer 1 clear input (ENCLR1) mask when timer 1 and CR13 match, so that a malfunction due to $\overline{V_{SYNC}}$ noise can be prevented by hardware.

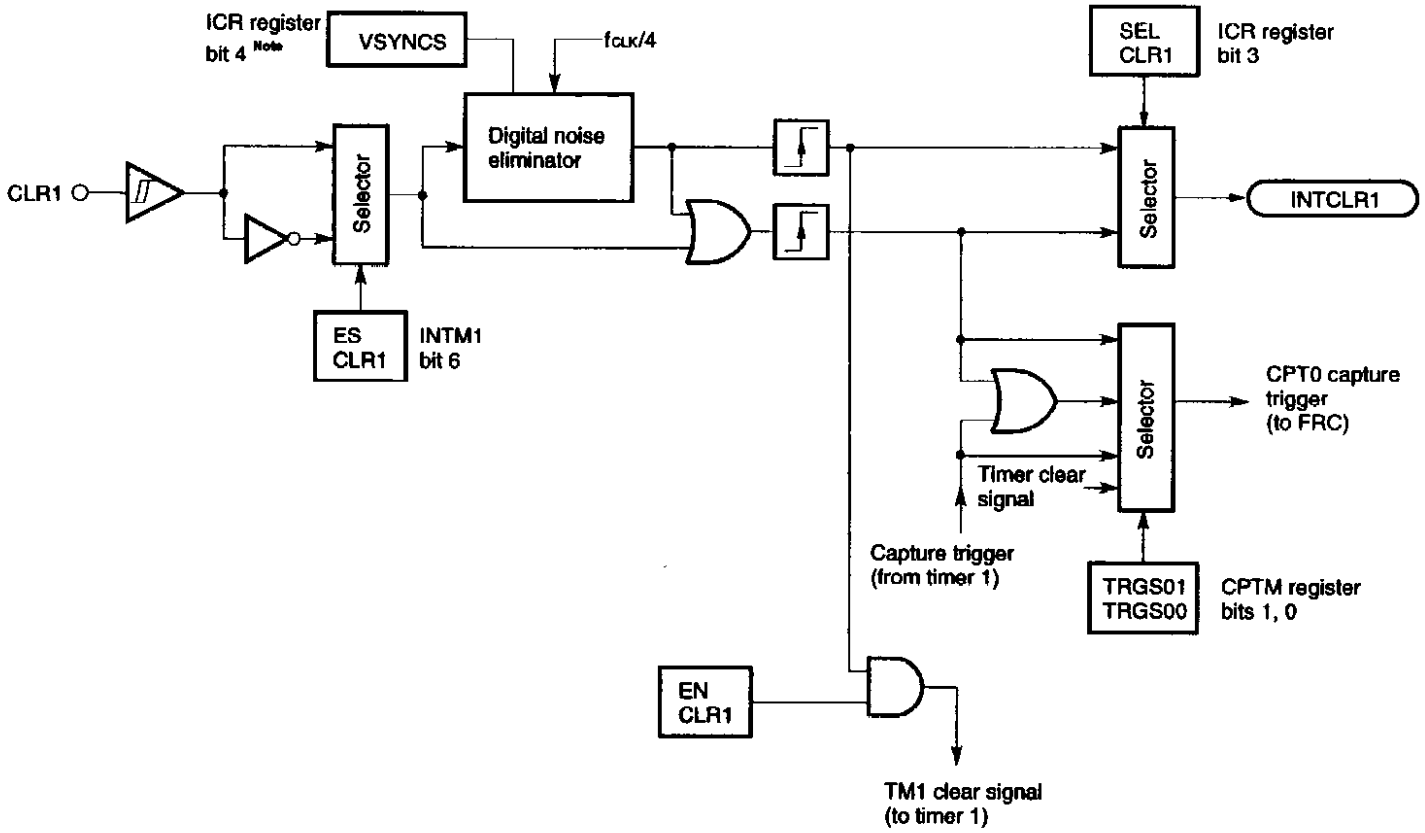
Timer 1 can be used as an output trigger for real-time output port 1 and a conversion trigger for A/D converter 1.

(3) Free running counter unit (FRC): 22-bit counter

The free running counter can be used for external pulse period measurement. This unit contains four capture registers, so that period measurements can be performed for four triggers in parallel. Since a 22-bit counter is used for this unit, a high-precision phase and speed detection is possible for a capstan and VCR drum rotating at high speed.

This unit contains a digital noise eliminator ($\overline{V_{SYNC}}$ frequency separator) and allows a choice between two elimination pulse widths, so that $\overline{V_{SYNC}}$ can be separated from a composite synchronizing signal with an extensive distortion. Fig. 3-13 shows the configuration of CLR1 input section.

Fig. [illegible] of CLR1 Input Section★



Note Noise is eliminated when it has narrower width than specified.
This bit is used to specify one of the following pulse widths:

- $4/f_{CLK} \times 19$ or smaller
- $4/f_{CLK} \times 31$ or smaller

(4) Timer 2 unit (TM2): 16-bit timer

Timer 2 is a general-purpose 16-bit timer unit. When the contents of the compare register match the contents of timer 2, timer 2 is automatically cleared, and functions as an interval timer to initiate an interrupt at the same time.

(5) Timer 4 unit (TM4): 8-bit timer

Timer 4 is an 8-bit timer unit with a prescaler. Timer 4 contains a capture/compare register and a capture register, and generates an interrupt when a capture occurs or a comparison finds a match.
This unit can be used, for example, to decode a remote controller signal.

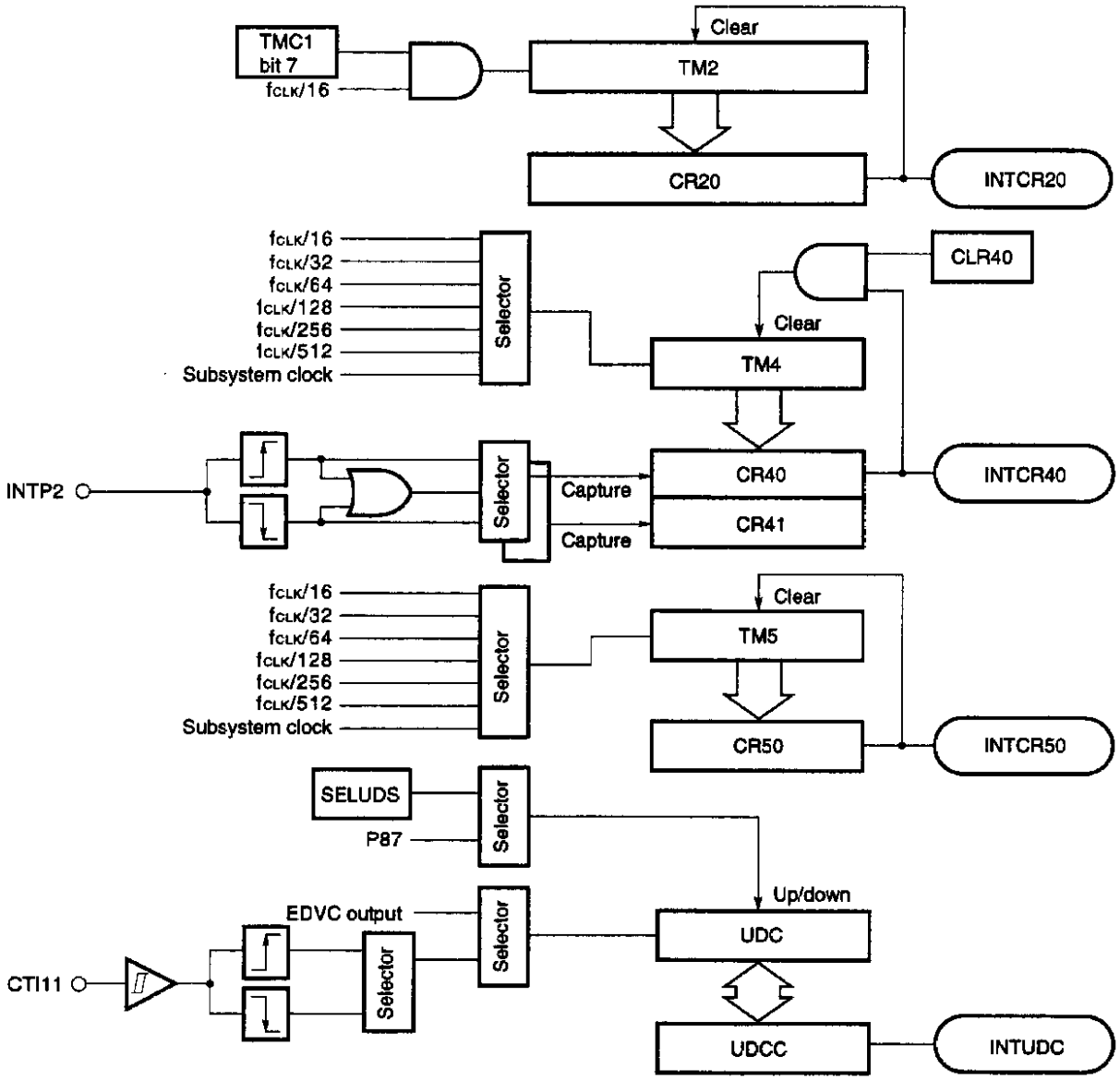
(6) Timer 5 unit (TM5): 8-bit timer

Timer 5 is a general-purpose 8-bit timer unit with a prescaler. When the contents of the compare register match the contents of timer 5, timer 5 is automatically cleared, and functions as an interval timer to initiate an interrupt at the same time.

(7) Up/down counter (UDC)

The up/down counter is a 6-bit up/down counter that counts up or down on a valid edge of the CTI11 input pulse signal. By using this counter, a linear tape counter for a VCR can be built which counts the number of PBCTL signals.

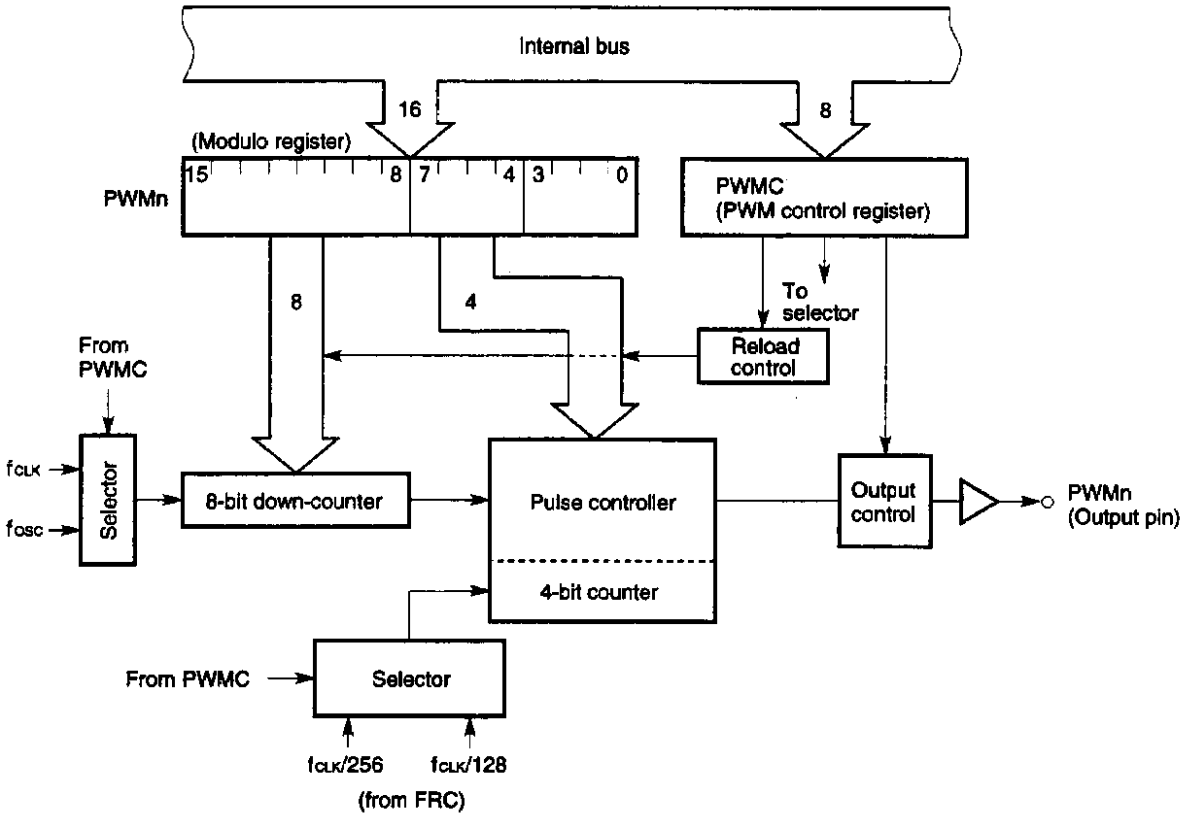
Fig. 3-14 Block Diagrams of Timer 2, Timer 4, Timer 5, and Up/Down Counter★



(8) PWM output units (PWM0, PWM1): 12-bit PWM

The PWM0 or PWM1 unit is a pulse width modulation (PWM) output unit with a 12-bit precision. A carrier frequency of 23.4 kHz or 46.9 kHz can be selected. The output of these units is most suitable for DC motor speed control.

Fig. 3-15 Block Diagram of the PWM Output Units (PWM0, PWM1) (n = 0, 1)

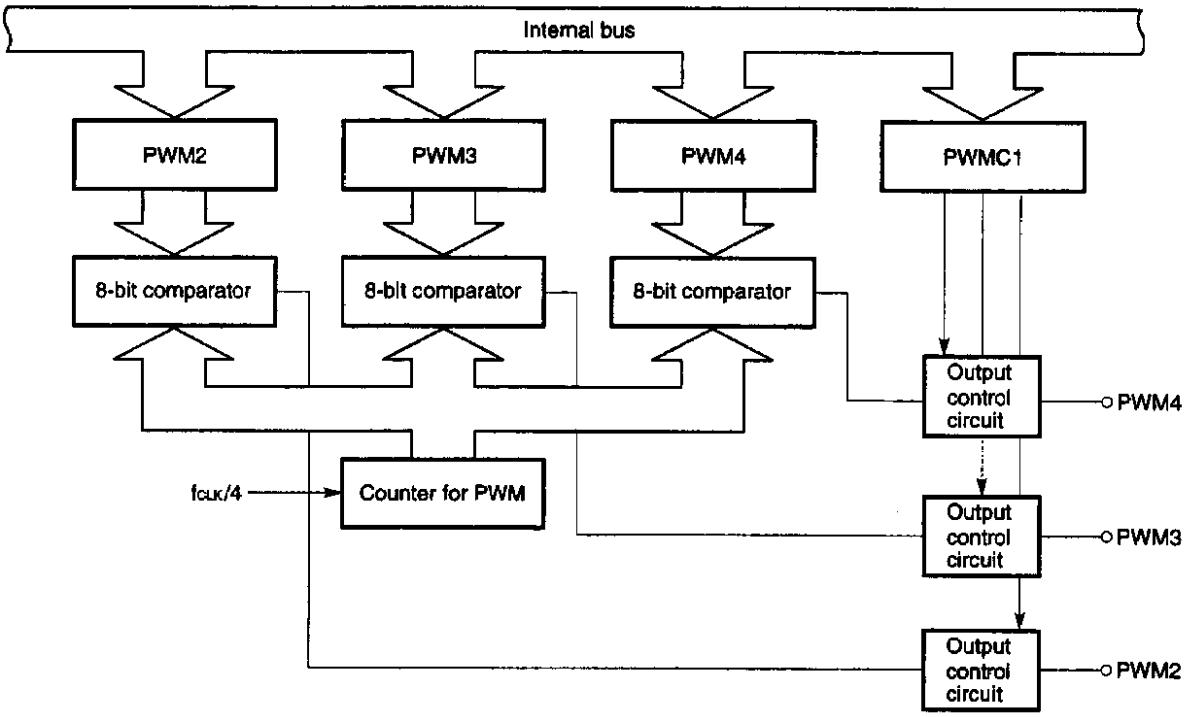


Remark $f_{CLK} = f_{OSC}/2$

(9) PWM output units (PWM2 - PWM4): 8-bit PWM

These units are PWM output units with an 8-bit precision. The carrier frequency is 5.9 kHz. These units can be used for general-purpose analog output.

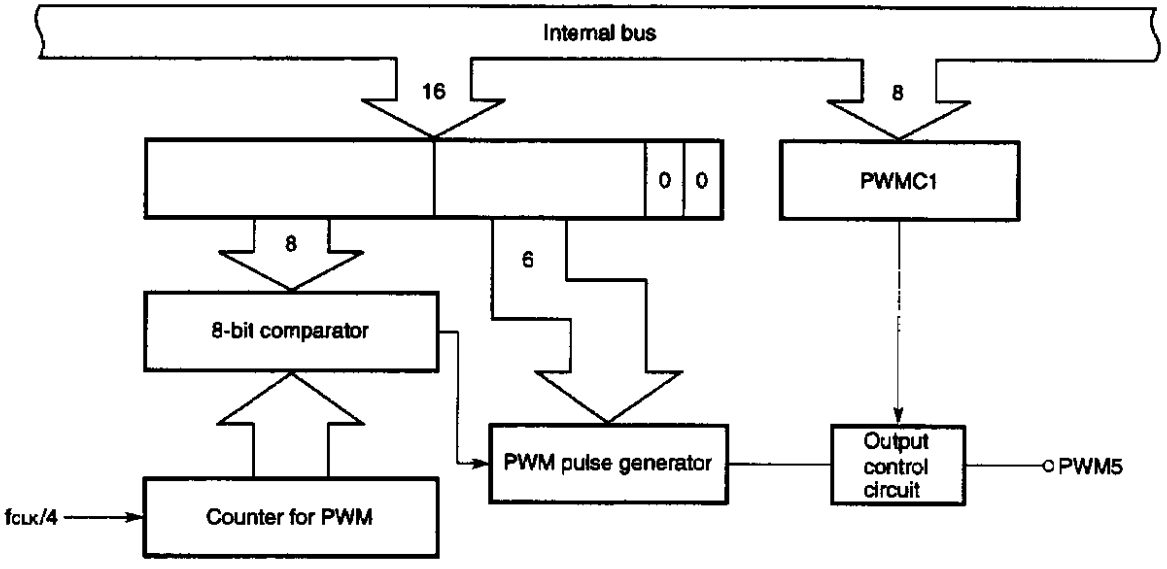
Fig. 3-16 Block Diagram of the PWM Output Units (PWM2 - PWM4)



(10) PWM output unit (PWM5): 14-bit PWM

This unit is a PWM output unit with a 14-bit precision. The carrier frequency is 5.9 kHz. This unit can be used for an output application where high-precision analog voltage is required as in the case of a voltage synthesizer.

Fig. 3-17 Block Diagram of the PWM Output Unit (PWM5)



(11) RECCTL write circuit

The PTO10 and PTO11 output pins of the super timer unit can be used to write a RECCTL signal.

Two modes are available. One is the REC mode used to write a CTL signal, and the other is the rewrite mode used for rewriting.

In the rewrite mode, the drive state can be gradually shifted so that not rising edges but falling edges only of the CTL signal are subject to rewriting.

Fig. 3-18 Block Diagram of the RECCTL Write Circuit

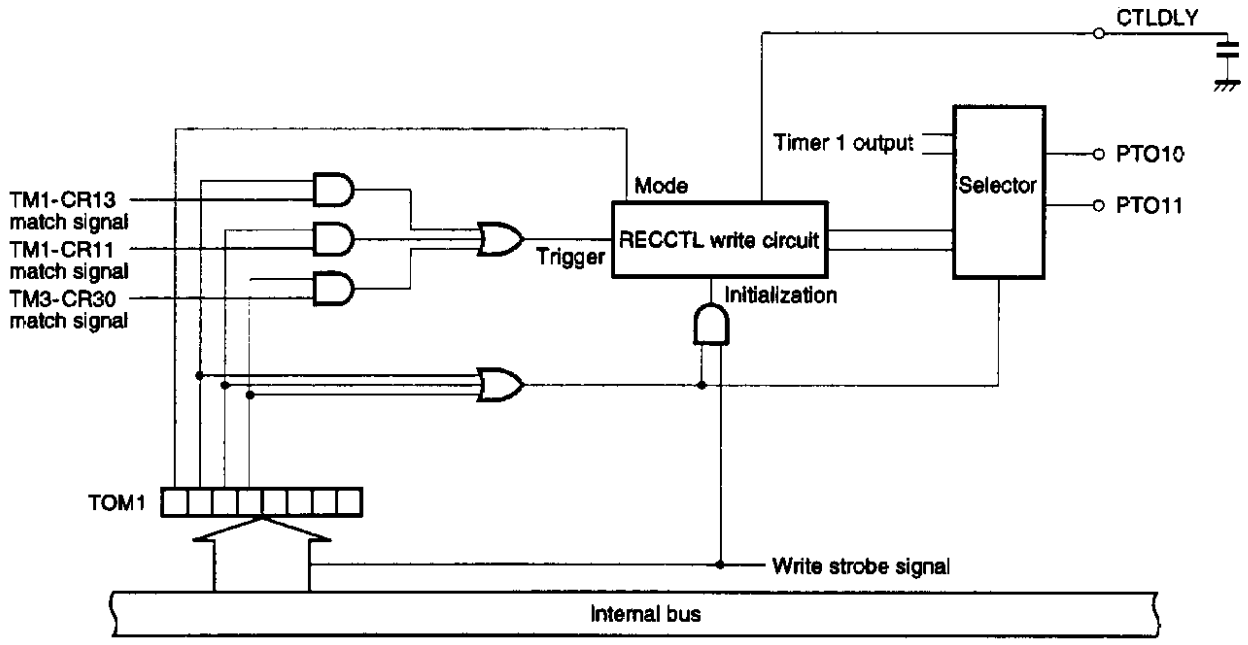


Fig. 3-19 Timing of RECCTL Write

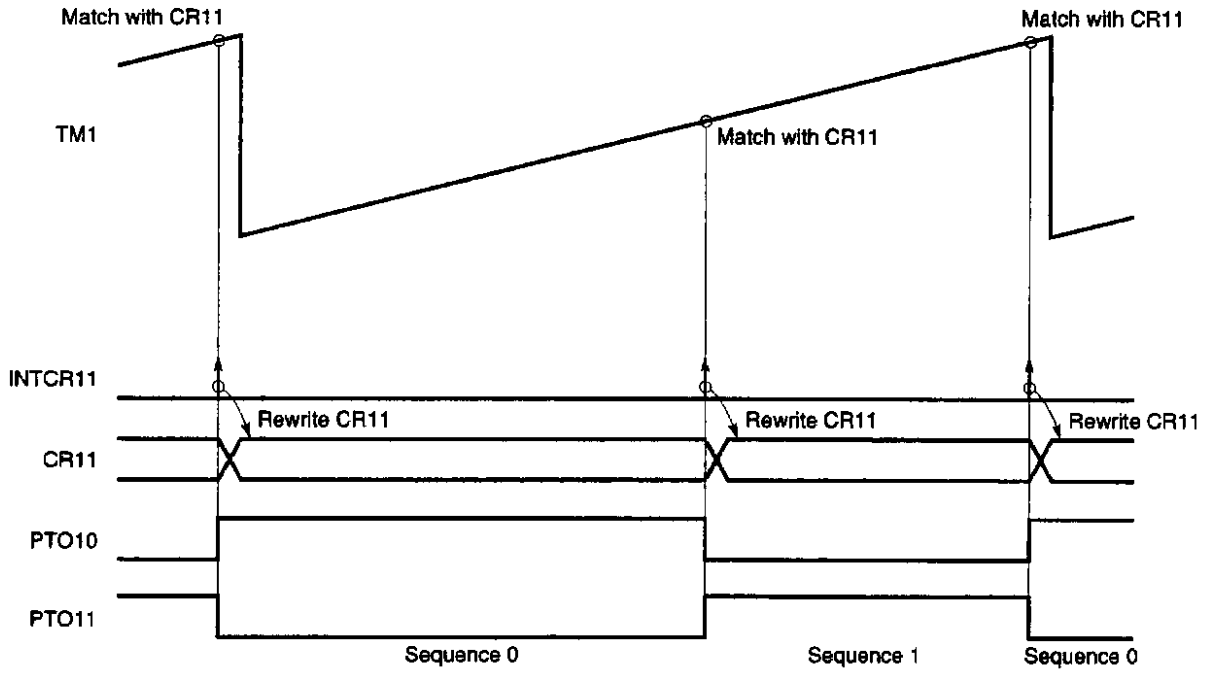
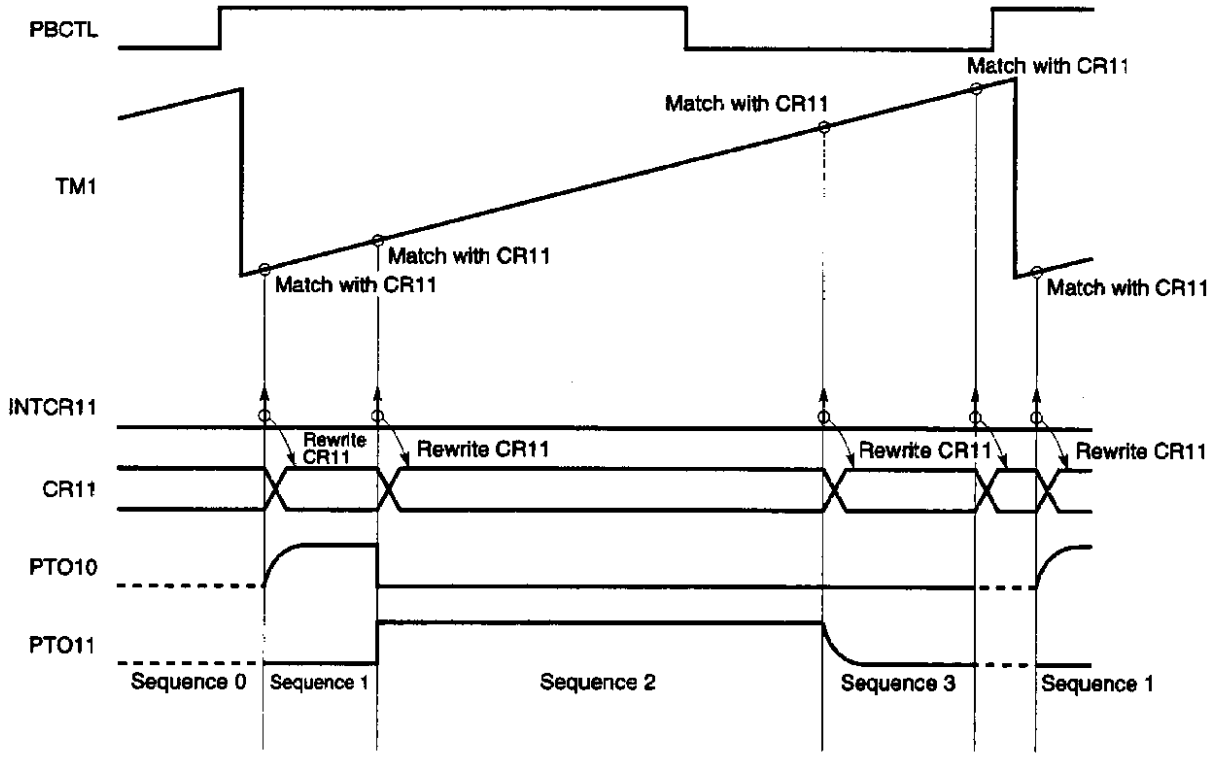


Fig. 3-20 Timing of RECCTL Rewrite



3.6 ANALOG CIRCUITRY

3.6.1 A/D Converter

The μPD78148 contains a fast, high-accuracy 8-bit analog-to-digital (A/D) converter with 15 multiplexed analog inputs (ANI0 to ANI14). Fig. 3-21 shows the block diagram of the A/D converter.

The μPD78148 contains two A/D conversion mode registers (ADM0, ADM1) and two A/D conversion result registers (ADCR0, ADCR1), so that the A/D converter can be treated as two independent A/D converters.

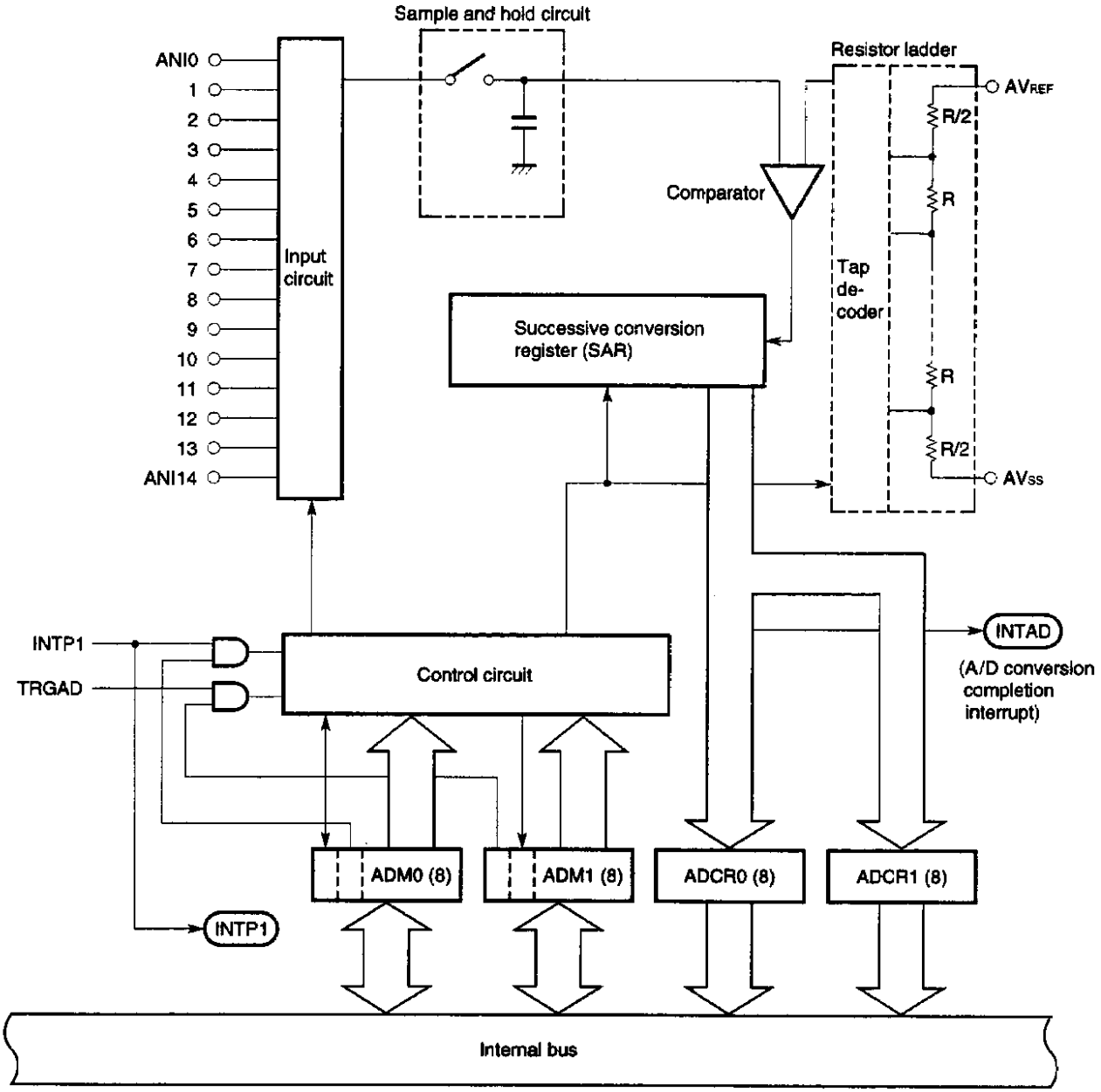
The A/D converter uses the success approximation system.

The A/D converter has two operation modes: the select mode and scan mode. The select mode converts analog input on a particular pin continuously. The scan mode converts multiple analog inputs sequentially. Furthermore, A/D conversion can be started in phase with an external interrupt request signal.

Conversion requires 20 μs (at 12 MHz).

Caution Never apply voltage exceeding the reference voltage for A/D converter (AV_{REF}) to the ANI0 to ANI14 pins in any circumstance.

Fig. 3-21 Block Diagram of the A/D Converter



3.6.2 Operational Amplifier

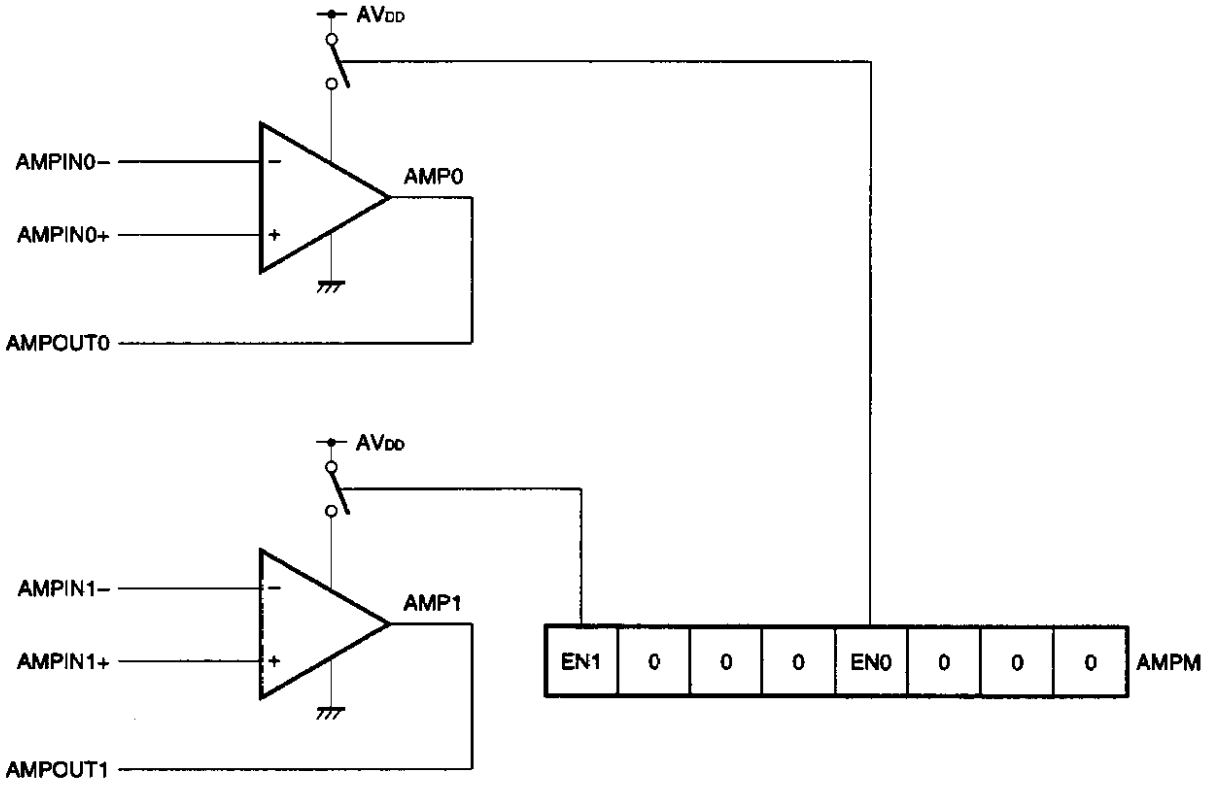
The μPD78148 contains two operational amplifiers. Each operational amplifier has an inverting input pin, non-inverting input pin, and output pin.

Whether to operate the operational amplifiers can be set using a mode register, allowing software control over the operational amplifiers.

If reduced current consumption is required as in the case of the standby mode, the operational amplifiers are to be set to the non-operation mode.

Fig. 3-22 shows the block diagram of the operational amplifiers.

Fig. 3-22 Block Diagram of the Operational Amplifiers



3.7 CLOCK FUNCTION

The μPD78148 contains a clock function that divides a clock timer overflow signal by hardware. The subsystem clock[Note] is used for the clock.

This clock function operates independently of the CPU, so the clock function can operate even if the CPU is placed in the standby mode (STOP mode) or reset state. In addition, the clock function allows a low-voltage operation with V_{DD} = 2.0 V.

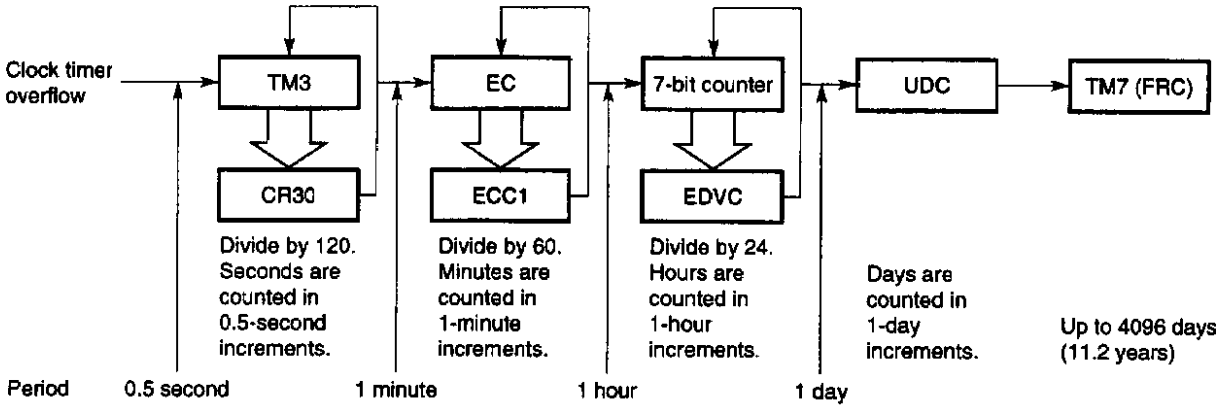
This means that by placing the CPU in the standby mode or reset state, a clock operation with low voltage and low current consumption can be implemented.

The clock function allows count operation for about 10 years.

Note The μPD78148 contains a frequency divider which divides the frequency of the subsystem clock and generates signals at the same interval. When the divider divides the frequency of the clock at 32.768 kHz (source oscillation of the subsystem clock), the divider expends one clock (about 30.5 μs) from when it overflows until it clears its count. Therefore, INTW interrupt generation takes about 30.5 μs more time per 0.5 second. Tune the oscillator frequency of the subsystem clock to 32.770 kHz. ★

Fig. 3-23 shows the block diagram of the clock function.

Fig. 3-23 Block Diagram of the Clock Function



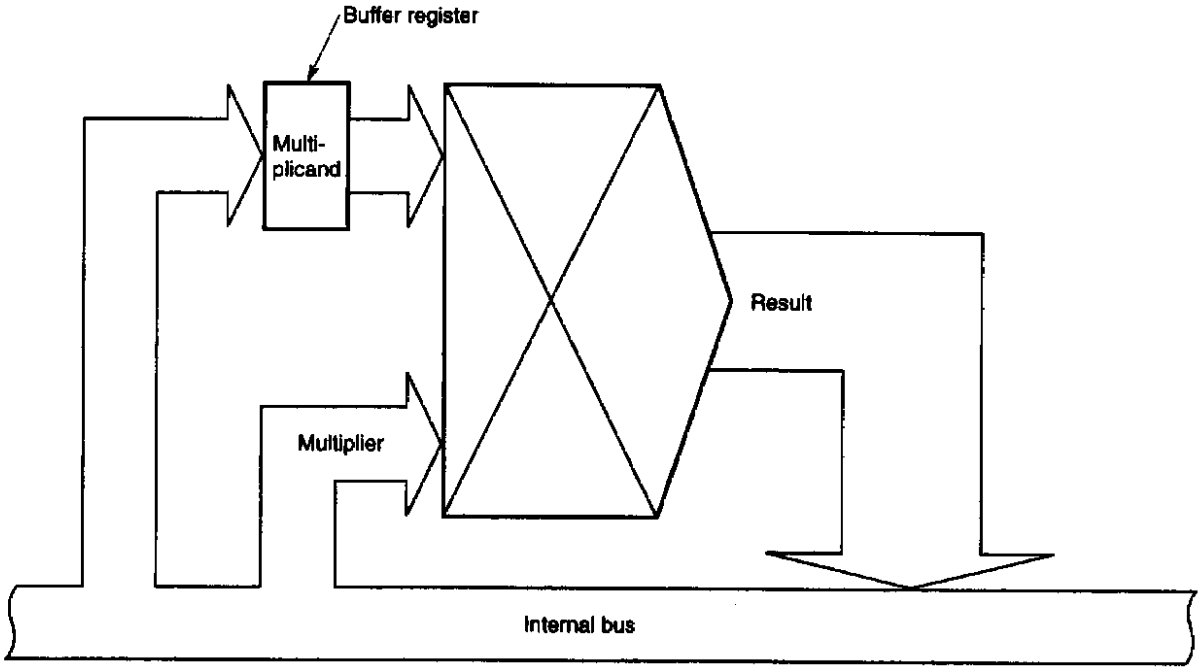
3.8 MULTIPLIER

The μPD78148 contains a high-speed multiplier that performs a multiplication (16-bit complement by 16-bit complement) by hardware.

The multiplier can extensively reduce digital filter operation time for servo control (operation time: 2.67 μs).

Fig. 3-24 shows the block diagram of the multiplier.

Fig. 3-24 Block Diagram of the Multiplier



4. INTERRUPT FUNCTIONS

The μPD78148 has a powerful interrupt function that can handle up to 25 interrupt requests (internal and external). Processing for each interrupt request is divided into two processing modes, vectored interrupt handling and macro service, one of which can be selected by software.

4.1 VECTORED INTERRUPT AND MACRO SERVICE

(1) Vectored interrupt

When an interrupt is accepted, the interrupt service routine is executed according to the data contained in the vector table area. The data indicates the start address of the interrupt service routine created by the user. In the vectored interrupt of the μPD78148, two priority levels can be specified by software. This facilitates the control of multiple interrupts.

(2) Macro service

When an interrupt is accepted, a service set beforehand by firmware is executed.
The following macro services are provided.

- Data transfer mode in which data is transferred between the memory and the special function register (SFR)
- Real-time output port control mode in which the real-time output port 0 can be controlled easily
- Counter mode in which the number of interrupt occurrence is counted
- Data pattern identification mode in which data string from external source is identified

Since these services are not performed via the CPU, the CPU statuses (such as SP and PSW) need not be saved and returned. Thus, CPU service time is greatly improved.

4.2 INTERRUPT SOURCES

Table 4-1 lists the interrupt request sources of the μPD78148. An interrupt vector table is assigned to each source. All the maskable interrupts are provided with macro service routines.

Table 4-1 Interrupt Request Sources

Type	Default priority	Interrupt source		Macro service	Vectors table address
		Name	Trigger		
Nonmaskable	–	NMI	Pin input edge detection	Not provided	0002H
Maskable	0 (highest)	INTP0	Pin input edge detection	Provided	0004H
	1	INTCPT3	EDVC output signal (CPT3 capture)		0006H
	2	INTCPT2	CTI00 pin input edge detection (CPT2 capture)		0008H
	3	INTCR12	CTI11 pin input edge detection/EDVC output signal (CPT12 capture)		000AH
	4	INTCR00	TM0-CR00 match signal		000CH
	5	INTCLR1	CLR1 pin input edge		000EH
	6	INTCR10	TM1-CR10 match signal		0010H
	7	INTCR01	TM0-CR01 match signal		0012H
	8	INTCR02	TM0-CR02 match signal		0014H
	9	INTCR11	TM1-CR11 match signal		0016H
	10	INTCPT1	Pin input edge detection/EC output signal (CPT1 capture)		0018H
	11	INTCR20	TM2-CR20 match signal		001AH
	12	INTCSI0	Serial transfer end (Serial interface channel 0)		001CH
	13	INTTB	Time base from FRC		001EH
	14	INTAD	A/D converter 0 conversion end		0020H
	15	INTP2	Pin input edge detection		0022H
	16	INTUDC	Up/down counter overflow		0024H
	17	INTCR30	TM3-CR30 match signal		0026H
	18	INTCR40	TM4-CR40 match signal		0028H
	19	INTCR50	TM5-CR50 match signal		002AH
	20	INTCR13	TM1-CR13 match signal		002CH
	21	INTCSI1	Serial transfer end (Serial interface channel 1)		002EH
	22	INTW	Clock timer overflow		0030H
	23 (lowest)	INTP1	Pin input edge detection		0032H

EDVC : Event divider compare register
EC : Event counter
CTI00, CTI11, CLR1 : Capture trigger inputs
TM× : Timers 1 to 5
CR×× : Compare registers 00, 01, 02, 10, 11, 20, 30, 40, 50
FRC : Free running counter

Remark The default priority indicates the priority used when two or more interrupts occur simultaneously.

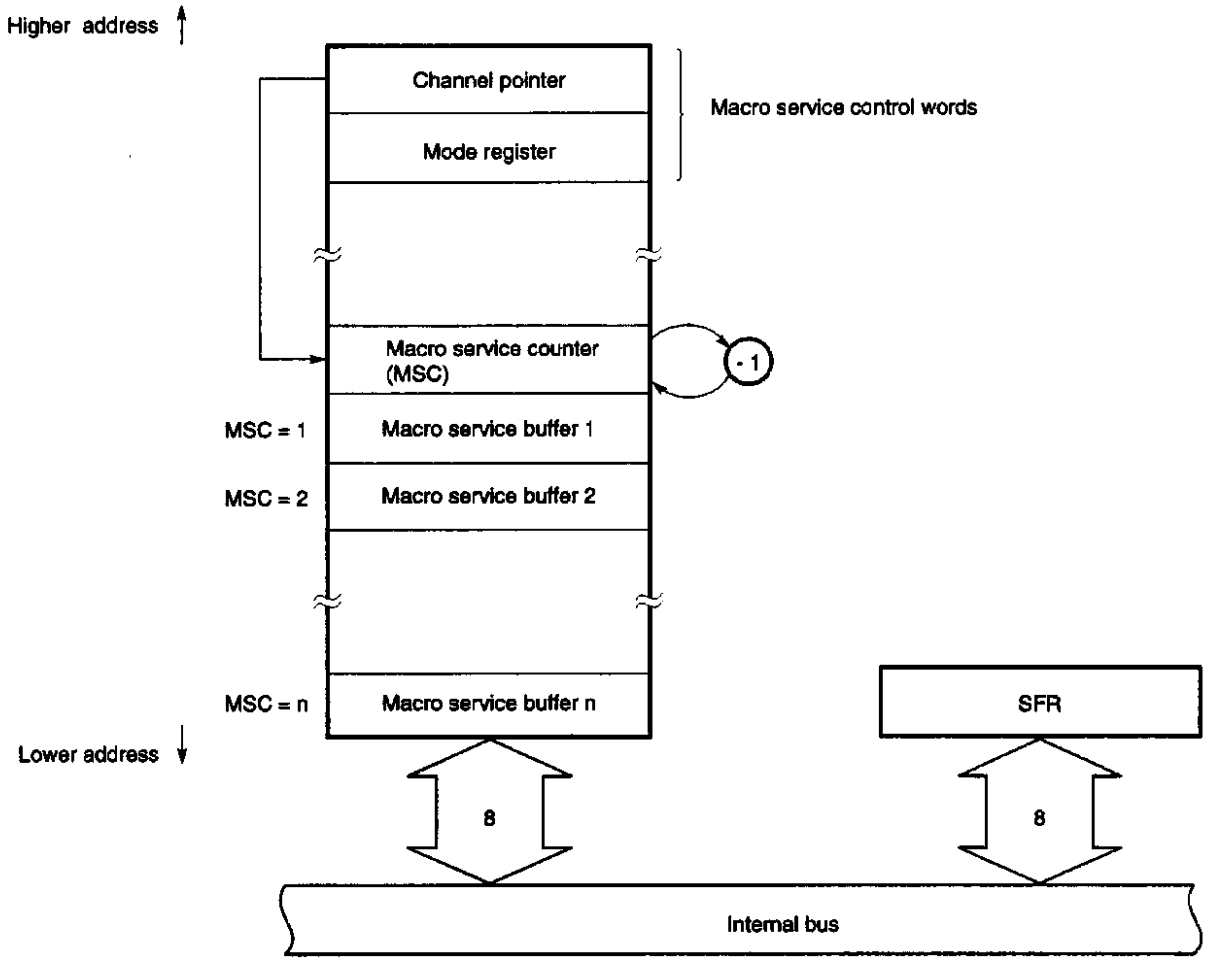
4.3 MACRO SERVICE FUNCTIONS

One of the interrupt processing functions of the μPD78148 is a built-in macro service function set by the firmware. There are four kinds of macro service function, each of which can be selected by software.

(1) Data transfer mode

When an interrupt occurs, 8-bit data is transmitted between the SFR corresponding to the interrupt and data memory. The address stored in data memory changes every time an interrupt occurs, so that consecutive data can be transmitted. The address in data memory (one from FE00H to FEFFH) and the number of transfer are controlled by software. After the specified number of transfer is completed, a vectored interrupt occurs.

Fig. 4-1 Addressing in Data Transfer Mode



The address of the macro service buffer (low-order 8 bits)
= (The contents of the channel pointer) - (The contents of the macro service counter)

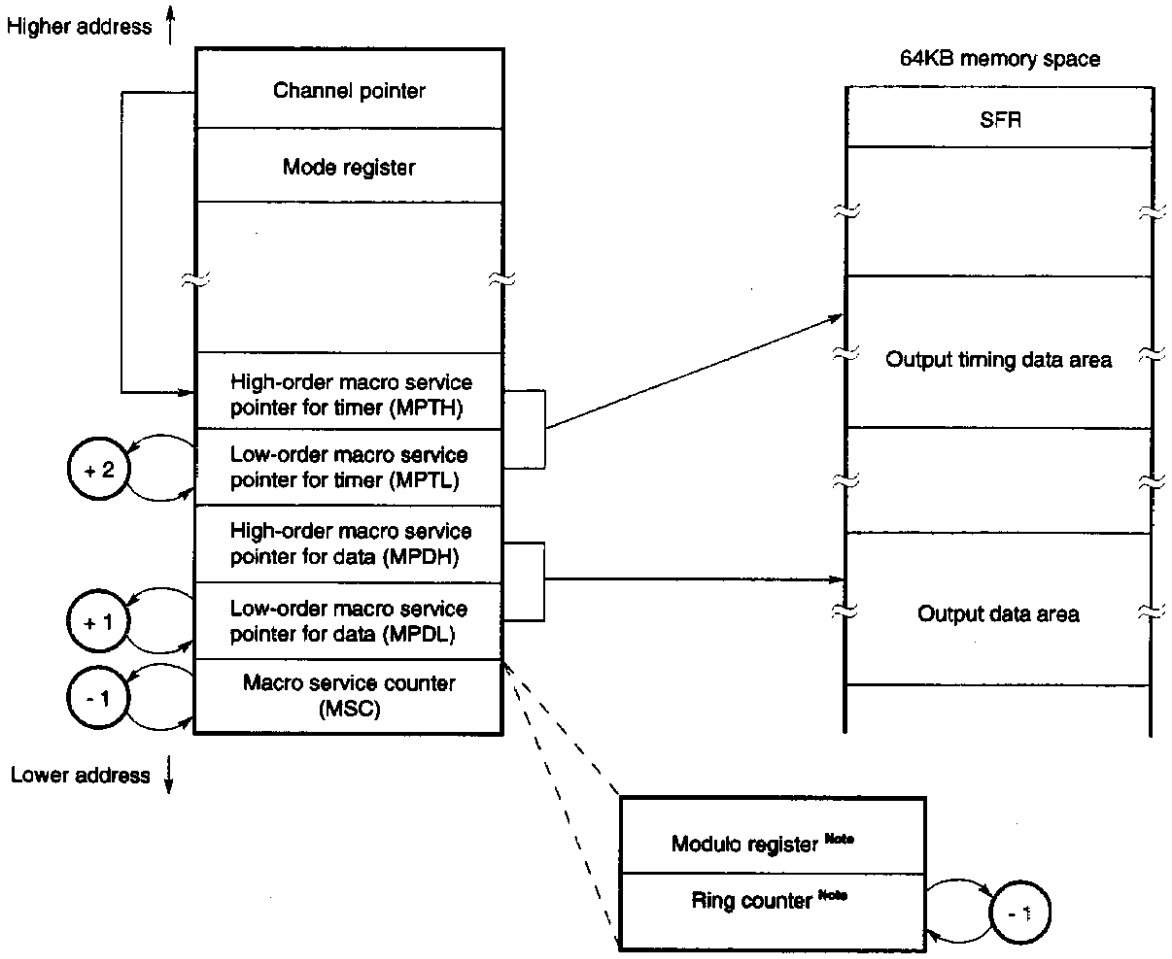
(2) Real-time output port 0 control mode

This macro service is effective when two output triggers of the real-time output port 0, INTCR01 and INTCR02, occur. Whenever one of them occurs, the output pattern profile is transmitted to the buffer registers (P0L, P0H), and the output timing profile is transmitted to the compare register (CR01 or CR02).

After the data transfer of each profile is completed, a vectored interrupt occurs.

This macro service enables various application such as the control of two stepping motors independently, or control of the PWM output or the output of the Head switching signal of the VCR.

Fig. 4-2 Addressing in Real-Time Output Port 0 Control Mode



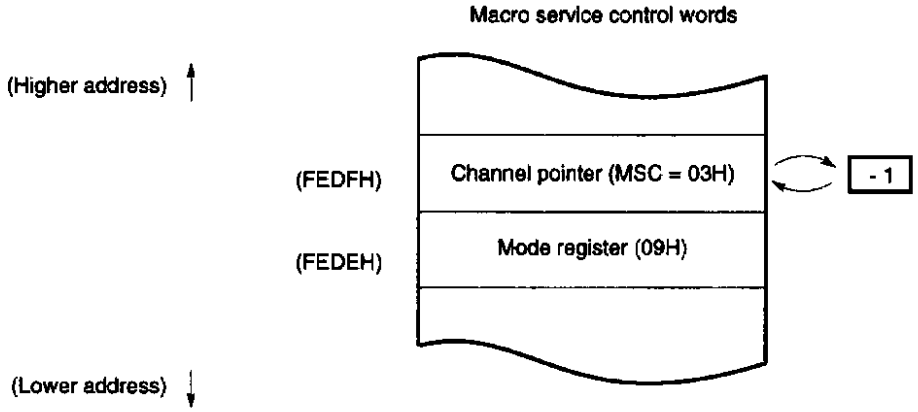
Note The modulo register and ring counter are both created only when ring control is used. When the ring counter goes to zero, the contents of the modulo register are reloaded.

(3) Counter mode

This mode decrements the macro service counter (MSC) according to an interrupt occurrence. This can be used to count the number of interrupt occurrence or to divide an interrupt.

When the counter reaches 0, a vectored interrupt occurs.

Fig. 4-3 Example of Operation in Counter Mode



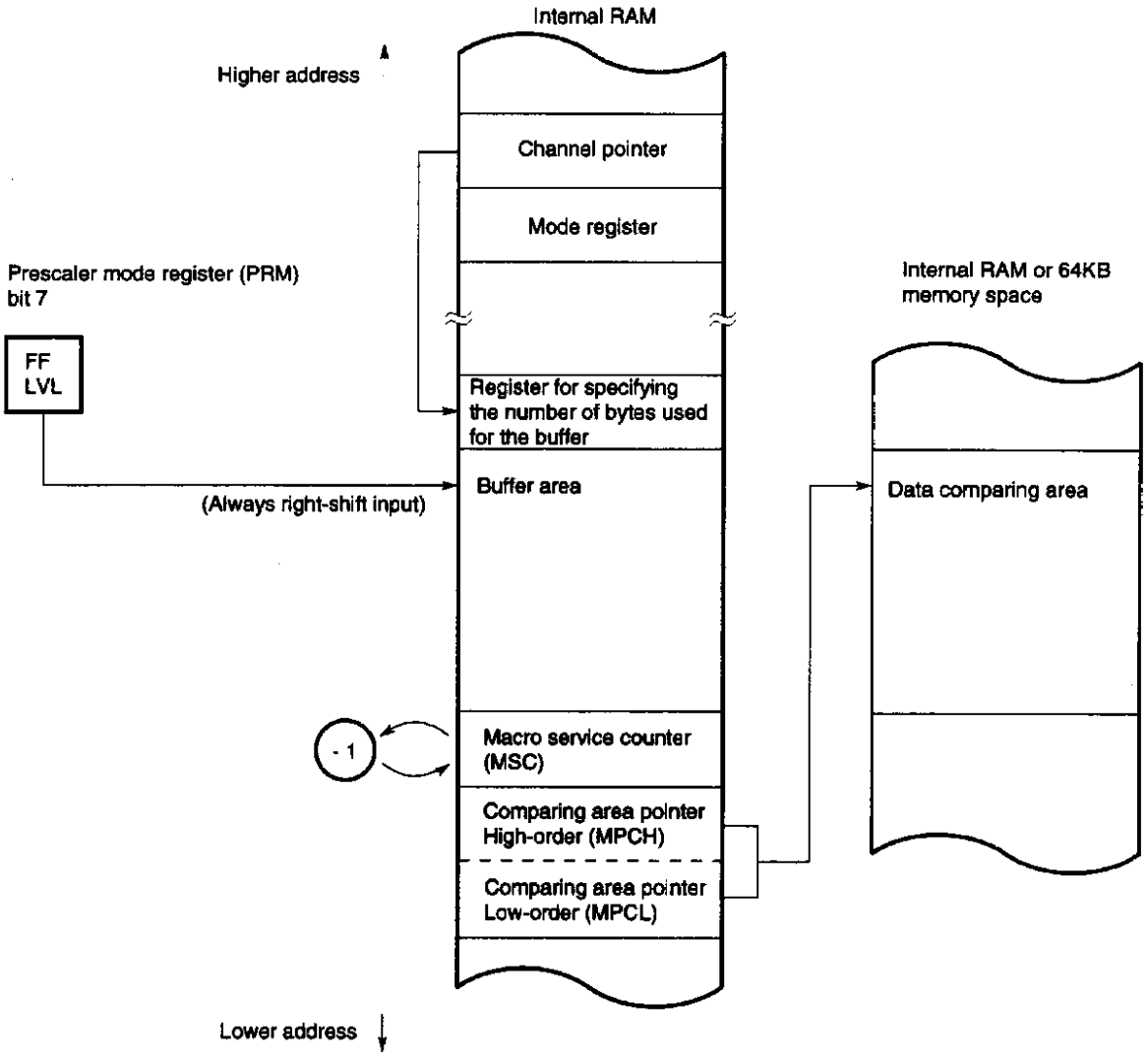
(4) **Data pattern identification mode** (VCR index search control etc.)

This macro service transfers the data from the control flip-flop (CTL flip-flop) to the buffer area when INTCR12 or INTCR30 occurs. Then, the buffer area stores the transferred data by shifting it to the right. And if stored data in the buffer area matches the data in the comparing area which is set beforehand, a vectored interrupt occurs (data pattern identification function).

This macro service can be applicable to easy control of the index search of a VCR. It can also be used to issue a vectored interrupt whenever a number of data storing specified by software is reached. In this case, data of the buffer area and data of the comparing area need not match.

Caution Storing of data to the buffer area is fixed to right shift.

Fig. 4-4 Addressing in Data Pattern Identification Mode



4.3.1 Macro Service Modes and Interrupt Requests

The macro service mode depends upon the type of interrupt request source. Table 4-2 lists the correspondence between the macro service modes and interrupt request sources.

Table 4-2 Macro Service Modes and Interrupt Request Sources

Macro service mode	Interrupt request source which can process the corresponding macro service
Data transfer mode	INTCSI0 INTCSI1 INTAD INTCR30 INTCR40 INTCR50 INTUDC
Real-time output port 0 control mode	INTCR01 INTCR02
Counter mode	All maskable interrupt requests
Data pattern identification mode	INTCR12 INTCR30

5. STANDBY FUNCTION

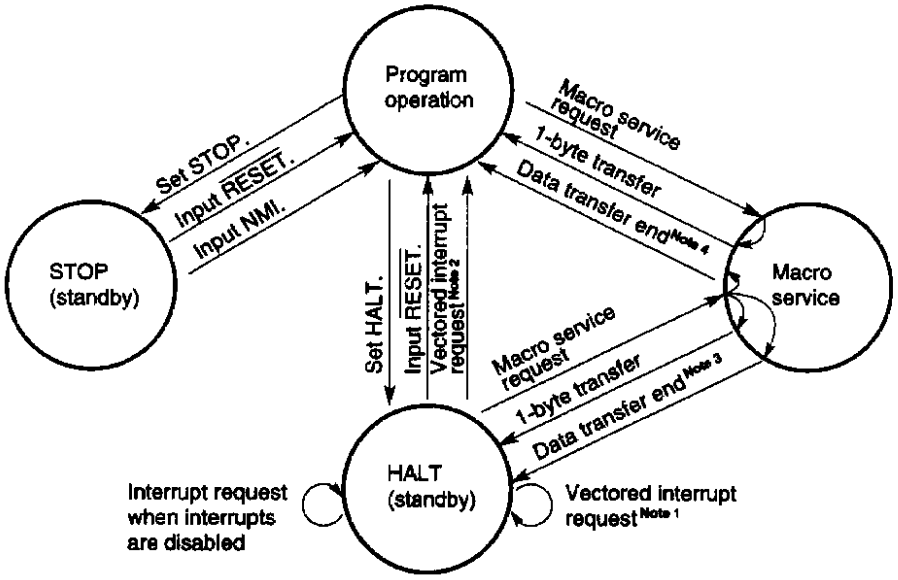
The μPD78148 provides a standby function for reduced system power consumption. The standby function has two modes.

- HALT mode..... This mode stops the CPU operation clock. The total power consumption can be reduced by combining the HALT mode with the normal operation mode.
  When the subsystem clock is used as the CPU clock, the HALT mode, with main system clock generation stopped, can further reduce power consumption.

- STOP mode ..... This mode stops the main system clock generator, thus terminating the operation of the entire system.
  This mode achieves such very low power consumption that only leakage currents are allowed. The subsystem clock is not stopped. In this mode, the clock function alone operates.

These modes are programmable.

Fig. 5-1 Standby State Transition



Notes 1. Vectored interrupt request with a low priority level (with low priority level interrupts disabled in the HALT mode)

2. Vectored interrupt request with a high priority level, or when low priority level interrupts are enabled in the HALT mode

3. In the case of a macro service with a low priority level (with low priority level interrupts disabled in the HALT mode)

4. In the case of a macro service with a high priority level, or when low priority level interrupts are enabled in the HALT mode

6. RESET FUNCTION

When the low level signal is applied to the $\overline{\text{RESET}}$ input pin, the system is reset and each hardware component is put in the status indicated in Table 6-1. The main system clock unconditionally stops oscillation.

When the signal applied to the $\overline{\text{RESET}}$ input pin goes from low to high, the reset state is released. After a time required for settling oscillation (about 22 ms when the microcomputer operates at 12 MHz), the contents of a reset vector table are loaded into the program counter (PC). Then a branch to the address set in the PC occurs, and program execution starts at the branch destination address. So a reset operation can be started at an arbitrary address.

The $\overline{\text{RESET}}$ input pin contains a noise eliminator using analog delays to prevent malfunctions due to noise.

Fig. 6-1 Accepting a Reset Signal

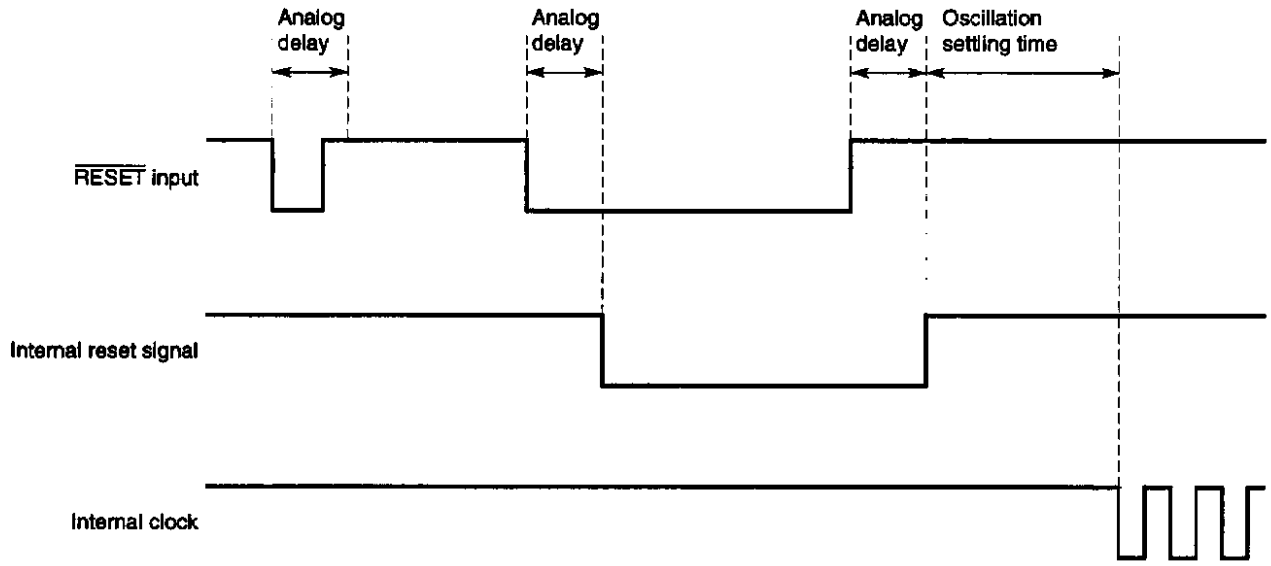


Table 6-1 Hardware Statuses during and after Reset

Hardware		Status during reset ($\overline{RESET}$ = L)	Status after reset ($\overline{RESET}$ = H)
Main system clock generator		Stops oscillation.	Starts oscillation.
Subsystem clock generator		Not affected by resetting	
Program counter (PC)		Undefined	Sets the reset vector table value.
Stack pointer (SP)		Undefined	
Program status word (PSW)		Initialized to 02H	
Internal RAM		Undefined. However, if the standby state is released by resetting, the value before the standby state is set is preserved.	
I/O line		Sets the input buffer and output buffer to off.	High-impedance. However, the low-level is output on P60 - 63.
Clock timer		Not affected by resetting	
Super timer unit	TM3, EC TM6, UDC TM7	Not affected by resetting when the clock function mode is set. When the clock function mode is not set, the super timer unit is initialized by resetting.	
Other than above		Initialized to specified state[Note]	
Analog circuit		Cuts off current paths.	Initialized to specified state[Note]
Other hardware		Initialized to specified state[Note]	

Note See **Table 2-3.**

7. OPERATIONS OF INSTRUCTIONS

(1) Operand notation and coding format

Operands are coded in the operand field of each instruction as listed in the coding column of the table below. For details of the operand format, refer to the relevant assembler specifications. When several coding forms are presented, any one of them is selected. Uppercase letters and the symbols, +, #, !, $, /, and [ ], are keywords and must be written as they are. These symbols have the following meanings.

- + : Auto increment
- # : Immediate data
- ! : Address by immediate addressing
- $: Address by relative addressing
- / : Bit inversion
- [ ] : Indirect addressing

For immediate data, an appropriate numeric or label must be written. The symbols +, #, !, $, /, and [ ] must not be omitted when describing labels.

Notation	Description
r, r'	X(R0), A(R1), C(R2), B(R3), E(R4), D(R5), L(R6), H(R7)
r1	A, B
r2	B, C
r3	D, E, E+
r4	D, E
rp, rp'	AX(RP0), BC(RP1), DE(RP2), HL(RP3)
sfr	Special function register abbreviation
sfrp	Special function register abbreviation (16-bit manipulation register)
saddr	FE20H - FF1FH Immediate data or label
saddrp	FE20H - FF1EH Immediate data or label (for 16-bit manipulation)
laddr16	0000H - FFFFH Immediate data or label: Immediate addressing
$addr16	0000H - FFFFH Immediate data or label: Relative addressing
addr11	800H - FFFH Immediate data or label
addr5	40H - 7EH Immediate data (bit 0 = 0, however) or label
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
n	3-bit immediate data (0 to 7)
RBn	RB0 - RB3

Remarks 1. Absolute names (R0 to R7 and RP0 to RP3) can be specified in r, r', rp, and rp', as well as functional names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

2. Immediate addressing is effective for entire address spaces. Relative addressing is effective for the locations within a displacement range of −128 to +127 from the starting address of the next instruction.

(2) Legend

A	:	Register A; 8-bit accumulator
X	:	Register X
B	:	Register B
C	:	Register C
D	:	Register D
E	:	Register E
H	:	Register H
L	:	Register L
R0 - R7	:	Register 0 to register 7 (absolute name)
AX	:	Register pair (AX); 16-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
RP0 - RP3	:	Register pair 0 to register pair 3 (absolute name)
PC	:	Program counter
SP	:	Stack pointer
PSW	:	Program status word
CY	:	Carry flag
AC	:	Auxiliary carry flag
Z	:	Zero flag
RBS0 - RBS1	:	Register bank select flag
IE	:	Interrupt request enable flag
STBC	:	Standby control register
( )	:	Contents of memory at an address enclosed in parentheses or at the address specified by a register enclosed in parentheses
xxH	:	Hexadecimal number
x_H, x_L	:	Eight high-order bits and eight low-order bits of 16-bit register pair

7.1 INSTRUCTION SET (ALPHABETICAL ORDER)

Instruction		Instruction		Instruction	
ADD	A, saddr	BF	PSW.bit, $addr16	DEC	r
ADD	A, sfr	BF	saddr.bit, $addr16	DEC	saddr
ADD	A, #byte	BF	sfr.bit, $addr16	DECW	rp
ADD	A, [DE]	BF	X.bit, $addr16	DI	
ADD	A, [HL]	BL	$addr16	DIVUW	r
ADD	A, [r4]	BNC	$addr16	EI	
ADD	A, word [r1]	BNE	$addr16	INC	r
ADD	r, r	BNL	$addr16	INC	saddr
ADD	saddr, #byte	BNZ	$addr16	INCW	rp
ADD	sfr, #byte	BR	rp	MOV	A, PSW
ADDC	A, saddr	BR	!addr16	MOV	A, r
ADDC	A, sfr	BR	$addr16	MOV	A, saddr
ADDC	A, #byte	BT	A.bit, $addr16	MOV	A, sfr
ADDC	A, [DE]	BT	PSW.bit, $addr16	MOV	A, word [r1]
ADDC	A, [HL]	BT	saddr.bit, $addr16	MOV	A, [DE]
ADDC	A, [r4]	BT	sfr.bit, $addr16	MOV	A, [DE+]
ADDC	A, word [r1]	BT	X.bit, $addr16	MOV	A, [HL]
ADDC	r, r	BTCLR	A.bit, $addr16	MOV	A, [HL+]
ADDC	saddr, #byte	BTCLR	PSW.bit, $addr16	MOV	A, [r3]
ADDC	sfr, #byte	BTCLR	saddr.bit, $addr16	MOV	A, !addr16
ADDW	AX, rp	BTCLR	sfr.bit, $addr16	MOV	PSW, A
ADDW	AX, saddrp	BTCLR	X.bit, $addr16	MOV	PSW, #byte
ADDW	AX, sfrp	BZ	$addr16	MOV	r, r
ADDW	AX, #word	CALL	!addr16	MOV	r, #byte
ADJBA		CALL	rp	MOV	saddr, A
ADJBS		CALLF	!addr11	MOV	saddr, #byte
AND	A, saddr	CALLT	[addr5]	MOV	sfr, A
AND	A, sfr	CLR1	A.bit	MOV	sfr, #byte
AND	A, #byte	CLR1	CY	MOV	STBC, #byte
AND	A, [DE]	CLR1	PSW.bit	MOV	word [r1], A
AND	A, [HL]	CLR1	saddr.bit	MOV	[DE], A
AND	A, [r4]	CLR1	sfr.bit	MOV	[DE+], A
AND	A, word [r1]	CLR1	X.bit	MOV	[HL], A
AND	saddr, #byte	CMP	A, saddr	MOV	[HL+], A
AND	sfr, #byte	CMP	A, sfr	MOV	[r3], A
AND	r, r	CMP	A, #byte	MOV	!addr16, A
AND1	CY, A.bit	CMP	A, [DE]	MOVW	AX, saddrp
AND1	CY, PSW.bit	CMP	A, [HL]	MOVW	AX, sfrp
AND1	CY, saddr.bit	CMP	A, [r4]	MOVW	AX, SP
AND1	CY, sfr.bit	CMP	A, word [r1]	MOVW	rp, rp
AND1	CY, X.bit	CMP	r, r	MOVW	rp, #word
AND1	CY, /A.bit	CMP	saddr, # byte	MOVW	saddrp, AX
AND1	CY, /PSW.bit	CMP	sfr, #byte	MOVW	saddrp, #word
AND1	CY, /saddr.bit	CMPW	AX, rp	MOVW	sfrp, AX
AND1	CY, /sfr.bit	CMPW	AX, saddrp	MOVW	sfrp, #word
AND1	CY, /X.bit	CMPW	AX, sfrp	MOVW	SP, AX
BC	$addr16	CMPW	AX, #word	MOVW	SP, #word
BE	$addr16	DBNZ	r2, $addr16	MOV1	A.bit, CY
BF	A.bit, $addr16	DBNZ	saddr, $addr16	MOV1	CY, A.bit

Instruction	Instruction	Instruction
MOV1 CY, PSW.bit	OR1 CY, /X.bit	SUBC A, #byte
MOV1 CY, saddr.bit	PUSH PSW	SUBC A, [DE]
MOV1 CY, sfr.bit	PUSH rp	SUBC A, [HL]
MOV1 CY, X.bit	POP PSW	SUBC A, [r4]
MOV1 PSW.bit, CY	POP rp	SUBC A, word [r1]
MOV1 saddr.bit, CY	RET	SUBC r, r
MOV1 sfr.bit, CY	RETI	SUBC saddr, #byte
MOV1 X.bit, CY	ROL r, n	SUBC sfr, #byte
MULSWr	ROLC r, n	SUBW AX, rp
MULUWr	ROL4 [r4]	SUBW AX, saddrp
NOP	ROR r, n	SUBW AX, sfrp
NOT1 A.bit	RORC r, n	SUBW AX, #word
NOT1 CY	ROR4 [r4]	XCH A, r
NOT1 PSW.bit	SEL RBn	XCH A, saddr
NOT1 saddr.bit	SET1 A.bit	XCH A, sfr
NOT1 sfr.bit	SET1 CY	XCH A, [DE]
NOT1 X.bit	SET1 PSW.bit	XCH A, [HL]
OR A, saddr	SET1 saddr.bit	XCH A, [r4]
OR A, sfr	SET1 sfr.bit	XCH A, word [r1]
OR A, #byte	SET1 X.bit	XOR A, saddr
OR A, [DE]	SHL r, n	XOR A, sfr
OR A, [HL]	SELW rp, n	XOR A, #byte
OR A, [r4]	SHR r, n	XOR A, [DE]
OR A, word [r1]	SHRW rp, n	XOR A, [HL]
OR r, r	SUB A, saddr	XOR A, [r4]
OR saddr, #byte	SUB A, sfr	XOR A, word [r1]
OR sfr, #byte	SUB A, #byte	XOR r, r
OR1 CY, A.bit	SUB A, [DE]	XOR saddr, #byte
OR1 CY, PSW.bit	SUB A, [HL]	XOR sfr, #byte
OR1 CY, saddr.bit	SUB A, [r4]	XOR1 CY, A.bit
OR1 CY, sfr.bit	SUB A, word [r1]	XOR1 CY, PSW.bit
OR1 CY, X.bit	SUB r, r	XOR1 CY, saddr.bit
OR1 CY, /A.bit	SUB saddr, #byte	XOR1 CY, sfr.bit
OR1 CY, /PSW, bit	SUB sfr, #byte	XOR1 CY, X.bit
OR1 CY, /saddr.bit	SUBC A, saddrp	
OR1 CY, /sfr.bit	SUBC A, sfr	

Caution Refer to *μPD78148 User's Manual* (IEU-1319) or *μPD78148 Instruction Set* (IEM-5536) for the details of the instructions.

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	$\|V_{DD} - AV_{DD}\| \le 0.5$ V	−0.5 to +7.0	V
	AV_{DD}		−0.5 to +7.0	V
	AV_{REF}	$V_{DD} \ge AV_{DD}$	−0.5 to AV_{DD} + 0.3	V
		$V_{DD} < AV_{DD}$	−0.5 to V_{DD} + 0.3	V
	AV_{SS}		−0.5 to +0.5	V
Input voltage	V_I		−0.5 to V_{DD} + 0.5	V
Analog input voltage (ANI0 - ANI14)	V_{IAN}	$V_{DD} \ge AV_{DD}$	−0.5 to AV_{DD} + 0.5	V
		$V_{DD} < AV_{DD}$	−0.5 to V_{DD} + 0.5	V
Output voltage	V_O		−0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	1 pin	15	mA
		Total of all output pins	100	mA
High-level output current	I_{OH}	1 pin	−10	mA
		Total of all output pins	−50	mA
Operating ambient temperature	T_A		−10 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

OPERATING CONDITIONS

Clock frequency	Operating ambient temperature (T_A)	Supply voltage (V_{DD})
4 MHz ≤ f_{XX} ≤ 12 MHz	−10 °C to +70 °C	+4.5 V to +5.5 V
32 kHz ≤ f_{XT} ≤ 35 kHz		+2.0 V to +5.5 V (For clock operation only) ★

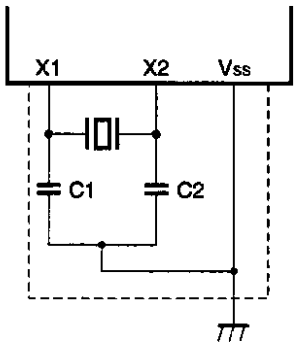
Note For clock operation only

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f_C = 1 MHz 0 V on pins other than measured pins			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

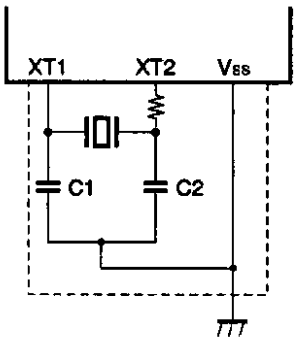
OSCILLATOR CHARACTERISTICS (MAIN CLOCK)

(T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Crystal		Oscillation frequency (f_{XX})	4	12	MHz

OSCILLATOR CHARACTERISTICS (SUBCLOCK)

(T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 2.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Crystal		Oscillation frequency (f_{XT})	32	35	kHz

Caution When using the main system clock generator and subsystem clock generator, run wires in broken lines ( ) shown in the above figures according to the following rules to avoid adverse effects caused by stray capacitance or other factors:

- **Connect components as short as possible.**
- **Never cause the wires to cross other signal lines or run near a line carrying a large varying current.**
- **Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS} at all times. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

Note, in particular, that the subsystem clock generator is a low-amplification circuit for reduced current consumption.

DC CHARACTERISTICS (T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Pins other than those shown in Note 1		2.2		V_{DD}	V
	V_{IH2}	Pins shown in Note 1 Note 2		0.8V_{DD}		V_{DD}	V
Low-level output voltage	V_{OL1}	I_{OL} = 2.0 mA				0.45	V
	V_{OL2}	I_{OL} = 8.0 mA Note 3				1.0	V
High-level output voltage	V_{OH1}	I_{OH} = −1.0 mA		V_{DD} − 1.0			V
	V_{OH2}	I_{OH} = −100 μA		V_{DD} − 0.5			V
	V_{OH3}	I_{OH} = −5.0 mA Note 4		2.0			V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
AV_{REF} current	AI_{REF}				0.2	1.0	mA
V_{DD} supply current	I_{DD1}	Operating mode, f_{XX} = 12 MHz			30	50	mA
	I_{DD2}	HALT mode, f_{XX} = 12 MHz			7	30	mA
Data retention voltage	V_{DDDR}	STOP mode		2.0			V
Data retention current Note 5, Note 6	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15	70	μA
			When the subclock does not operate		0.5	40	μA
		STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	14.0	μA
			When the subclock does not operate		0.3	8.0	μA
		STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	9.0	μA
			When the subclock does not operate		0.2	6.0	μA
Pull-up resistor	R_L	V_I = 0 V		15	30	80	kΩ

Notes 1. Pins X1, X2, $\overline{\text{RESET}}$, NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI0, P36/SO0/SB0, P37/$\overline{\text{SCK0}}$, P93/$\overline{\text{SCK1}}$, P95/SI1, and MODE

2. When using the XT1/P86 pin for input, disconnect the clock noise eliminator and feedback resistor.

3. Pins P10 - P17, P40 - P47, P50 - P57

4. Pins P00 - P07

5. Current through the AV_{REF} pin is excluded.

6. When the subclock is not operating in the STOP mode, disconnect the feedback resistor and clock noise eliminator, and connect the XT1 pin to V_{DD}.

DC CHARACTERISTICS (T_A = +25 °C, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Data retention current Note 1, Note 2	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15.0	40.0	μA
			When the subclock does not operate		0.5	10.0	μA
		STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	10.0	μA
			When the subclock does not operate		0.3	5.0	μA
		STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	7.0	μA
			When the subclock does not operate		0.2	4.0	μA

Notes 1. Current through the AV_{REF} pin is excluded.

2. When the subclock is not operating in the STOP mode, disconnect the feedback resistor and clock noise eliminator and connect the XT1 pin to V_{DD}.

SERIAL INTERFACE (T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

(1) Channel 0

Parameter	Symbol	Condition		Min.	Max.	Unit
Serial clock cycle time	t_{CYSK0}	Input	External clock	1.0		μs
		Output	f_{CLK} divided by 8	1.3		μs
			f_{CLK} divided by 32	5.3		μs
Serial clock low-level width	t_{WSKL0}	Input	External clock	420		ns
		Output	f_{CLK} divided by 8	556		ns
			f_{CLK} divided by 32	2.5		μs
Serial clock high-level width	t_{WSKH0}	Input	External clock	420		ns
		Output	f_{CLK} divided by 8	556		ns
			f_{CLK} divided by 32	2.5		μs
SI0, SB0 setup time (before $\overline{SCK0}$ ↑)	t_{SSSK0}			150		ns
SI0, SB0 hold time (after $\overline{SCK0}$ ↑)	t_{HSSK0}			400		ns
SO0, SB0 output delay time (from $\overline{SCK0}$ ↓)	$t_{DSBSK01}$	CMOS push-pull output (three-wire serial I/O mode)		0	300	ns
	$t_{DSBSK02}$	Open-drain output (SBI mode), R_L = 1 kΩ		0	800	ns
SB0 high hold time (after $\overline{SCK0}$ ↑)	t_{HSBSK0}	SBI mode		4t_{CYX}		ns
SB0 low setup time (before $\overline{SCK0}$ ↓)	t_{SSBSK0}			4t_{CYX}		ns
SB0 low-level width	t_{WSBL0}			4t_{CYX}		ns
SB0 high-level width	t_{WSBH0}			4t_{CYX}		ns

Remarks 1. The values listed in the above table are obtained when f_{XX} = 12 MHz and C_L = 100 pF.

★ **2.** f_{CLK} indicates the internal system clock (f_{XX} divided by 2).

★ **3.** t_{CYX} = 1/f_{XX}

(2) Channel 1

Parameter	Symbol	Condition		Min.	Max.	Unit
Serial clock cycle time	t_{CYSK1}	External clock input	Automatic transfer	17t_{CYX}		ns
			Three-wire	13t_{CYX}		ns
		Output	f_{CLK} divided by 8	1.3		μs
			f_{CLK} divided by 32	5.3		μs
			f_{CLK} divided by 64	10.6		μs
Serial clock low-level width	t_{WSKL1}	External clock input	Automatic transfer	5t_{CYX}		ns
			Three-wire	5t_{CYX}		ns
		Output	f_{CLK} divided by 8	620		ns
			f_{CLK} divided by 32	2.6		μs
			f_{CLK} divided by 64	5.3		μs
Serial clock high-level width	t_{WSKH1}	External clock input	Automatic transfer	9t_{CYX}		ns
			Three-wire	5t_{CYX}		ns
		Output	f_{CLK} divided by 8	620		ns
			f_{CLK} divided by 32	2.6		μs
			f_{CLK} divided by 64	5.3		μs
SI1 setup time (before $\overline{SCK1}$ ↑)	t_{SSSK1}			100		ns
SI1 hold time (after $\overline{SCK1}$ ↑)	t_{HSSK1}			400		ns
SO1 output delay time (from $\overline{SCK1}$ ↓)	t_{DSBSK1}			0	300	ns
$\overline{SCK1}$(8) ↑ → STRB1 ↑	t_{DSTRB1}			t_{WSKH1}	t_{CYSK1}	
Strobe signal high-level width	t_{WSTRB1}			t_{CYSK1} − 30	t_{CYSK1} + 30	ns
BUSY1 setup time referred to BUSY1 detection	t_{SBUSY1}			100		ns
BUSY1 hold time referred to BUSY1 detection	t_{HBUSY1}			100		ns
BUSY inactive → $\overline{SCK1}$(1) ↓	t_{LBUSY1}				t_{CYSK1} + t_{WSKH1}	

Remarks 1. The values listed in the above table are obtained when f_{XX} = 12 MHz and C_L = 100 pF.

2. f_{CLK} indicates the internal system clock (f_{XX} divided by 2). ★

3. $t_{CYX} = 1/f_{XX}$ ★

4. The parenthesized number as in $\overline{SCK1}$(n) indicates that n−1 $\overline{SCK1}$ pulses precede this particular $\overline{SCK1}$(n) pulse.

5. $\overline{BUSY1}$ is detected when (n+2) × t_{CYSK1} has passed after $\overline{SCK1}$(8) ↑ (n = 0, 1, ···).

OTHER OPERATIONS (T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter		Symbol	Condition	Min.	Max.	Unit
CTI00, CTI10, CTI11 low-level width		t_{WCTL}		4t_{CYX}		ns
CTI00, CTI10, CTI11 high-level width		t_{WCTH}		4t_{CYX}		ns
CLR1 low-level width		t_{WCR1L}	Digital noise eliminator not used	4t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 0	160t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 1	256t_{CYX}		ns
CLR1 high-level width		t_{WCR1H}	Digital noise eliminator not used	4t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 0	160t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 1	256t_{CYX}		ns
Digital noise eliminator	Removed pulse width	t_{WSEP}	ICR bit 4 = 0		152t_{CYX}	ns
			ICR bit 4 = 1		248t_{CYX}	ns
	Passed pulse width		ICR bit 4 = 0	160t_{CYX}		ns
			ICR bit 4 = 1	256t_{CYX}		ns
H_{SYNC} synchronization time (CLR1 ↑ → H_{SYNC} ↓)		t_{DHS}	ICR bit 4 = 0	772t_{CYX}	778t_{CYX}	ns
			ICR bit 4 = 1	760t_{CYX}	766t_{CYX}	ns
★ H_{SYNC} cycle time		t_{CYCHS}	When f_{XX} is 12 MHz	63.5		μs
★ H_{SYNC} active level width		t_{WHS}	When f_{XX} is 12 MHz	5		μs
NMI low-level width		t_{WNIL}		10		μs
NMI high-level width		t_{WNIH}		10		μs
INTP0 - INTP2 low-level width		t_{WIPL}		4t_{CYX}		ns
INTP0 - INTP2 high-level width		t_{WIPH}		4t_{CYX}		ns
$\overline{RESET}$ low-level width		t_{WRSL}		10		μs

CLOCK OUTPUT OPERATION (T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Formula	Min.	Max.	Unit
CLO cycle time	t_{CYCL}		333	2667	ns
CLO low-level width	t_{CLL}	t_{CYCL}/2 ±50	116	1384	ns
CLO high-level width	t_{CLH}	t_{CYCL}/2 ±50	116	1384	ns
CLO rising time	t_{CLR}			50	ns
CLO falling time	t_{CLF}			50	ns

Remark The values in the table are obtained when f_{XX} = 12 MHz and C_L = 100 pF.

DATA MEMORY LOW-VOLTAGE DATA RETENTION CHARACTERISTICS

(T_A = −10 °C to +70 °C, AV_{SS} = V_{SS} = AV_{REF} = 0 V)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DDDR}	STOP mode Note 1		2.0		5.5	V
Data retention current Note 2, Note 3	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15.0	70.0	μA
			When the subclock does not operate		0.5	40.0	μA
		STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	14.0	μA
			When the subclock does not operate		0.3	8.0	μA
		STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	9.0	μA
			When the subclock does not operate		0.2	6.0	μA
Data retention current Note 2, Note 3 (T_A = 25 °C)	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15.0	40.0	μA
			When the subclock does not operate		0.5	10.0	μA
		STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	10.0	μA
			When the subclock does not operate		0.3	5.0	μA
		STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	7.0	μA
			When the subclock does not operate		0.2	4.0	μA
V_{DD} rising time	t_{RVD}			200			μs
V_{DD} falling time	t_{FVD}			200			μs
V_{DD} retention time (referred to STOP mode setting)	t_{HVD}			0			ms
STOP release signal input time	t_{DREL}			0			ms
Low-level input voltage	V_{IL}	Specified pins Note 4		0		0.1V_{DDDR}	V
High-level input voltage	V_{IH}			0.9V_{DDDR}		V_{DDDR}	V

Notes 1. The voltage to keep the subclock operating is lower than the data retention voltage.

2. Current through the AV_{REF} pin is excluded.
3. When using the XT1/P86 pin for input, disconnect the feedback resistor and clock noise eliminator.
4. Pins NMI, $\overline{\text{RESET}}$, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI0, P36/SO0/SB0, P37/$\overline{\text{SCK0}}$, P93/$\overline{\text{SCK1}}$, P95/SI1, MODE, and P86/XT1 (when the subclock is not operating)

CLOCK FUNCTION (T_A = −10 °C to +70 °C, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage to keep the subclock operating	V_{DDXT}		2.0			V
Operating voltage for hardware clock function	V_{DDW}		2.0			V

FLAG FOR DETECTING A BREAK OF SUBCLOCK OPERATION
(T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Time duration detected as a break of oscillating	T_{OSCF}		45			μs

A/D CONVERTER CHARACTERISTICS
(T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = +5.0 V ±10 %, 3.8 V ≤ AV_{REF} ≤ V_{DD}, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution			8			bit
Total error		4.0 V ≤ AV_{REF} ≤ V_{DD}			0.4	%
		3.8 V ≤ AV_{REF} ≤ V_{DD}			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	ADM0 bit 4 = 0 Note	360t_{CYX}			ns
		ADM0 bit 4 = 1 Note	240t_{CYX}			ns
Sampling time	t_{SAMP}	ADM0 bit 4 = 0 Note	72t_{CYX}			ns
		ADM0 bit 4 = 1 Note	48t_{CYX}			ns
Analog input voltage	V_{IAN}		−0.3		AV_{REF} + 0.3	V
Reference voltage	AV_{REF}		3.8		V_{DD}	V
AV_{REF} current	AI_{REF}			0.2	1.0	mA

Note The time specified by ADM0 is used even for conversion with ADM1.

CHARACTERISTICS OF THE OPERATIONAL AMPLIFIERS

(T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Open-loop gain	A_V		60			dB
Voltage range for common-mode input	V_{ICM}		0.5		3.3	V
Input offset voltage	V_{OS}			±10	±20	mV
High-level output current	I_{OHOP}	V_{DD} = 5.0 V, V_{OH} = V_{DD}/2	−4.0	−12.0		mA
Low-level output current	I_{OLOP}	V_{DD} = 5.0 V, V_{OL} = V_{DD}/2	50	130		μA
Slew rate	+			1		V/μs
	−			−4		V/ms
Common-mode rejection ratio	CMRR		60			dB
Supply-voltage rejection ratio	PSRR		60			dB
Unity-gain frequency	f_O		1			MHz

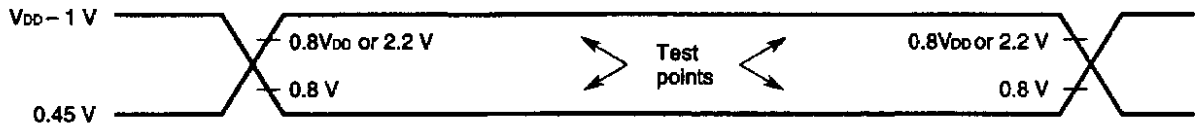
Caution For stable operation, do not decrease the operational amplifier gain below 20 dB.

RECCTL WRITE CIRCUIT (T_A = −10 °C to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CTLDLY charge current	I_{OHCTL}	V_{DD} = 5.0 V V_{OH} = 0 V	−500	−900	−1300	μA
CTLDLY discharge current	I_{OLCTL}	V_{DD} = 5.0 V V_{OL} = 5.0 V	1300	2200	3200	μA
PTO10, PTO11 high-level output current	I_{OHPTO}	V_{DD} = 5.0 V V_{OH} = 0 V	−6	−12	−22	mA

Caution When a 1-μF capacitor is connected, the time constant for PTO10 or PTO11 is 2 to 5 ms.

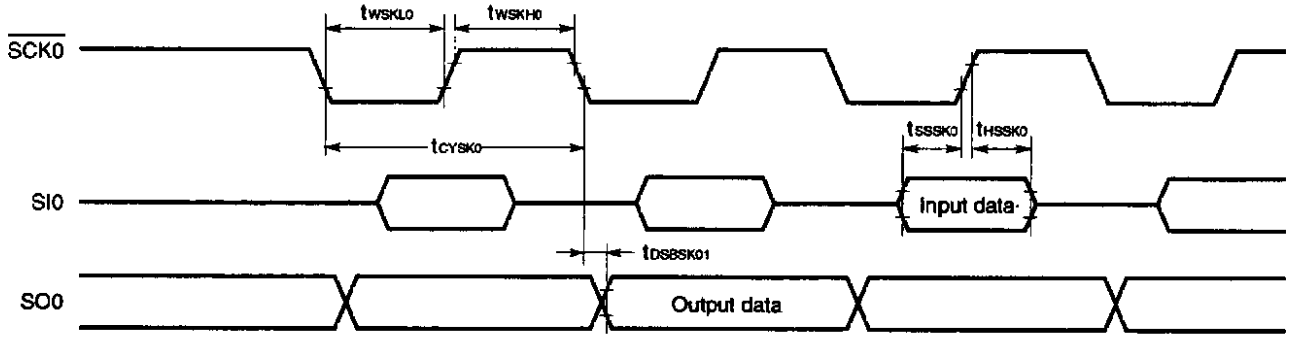
AC Timing Test Points



TIMING WAVEFORM

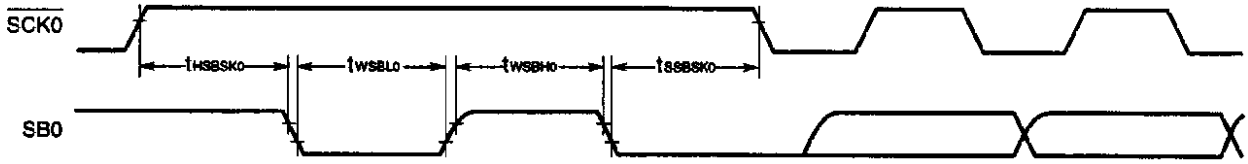
Serial Operation (SIO0)

Three-wire serial I/O mode:

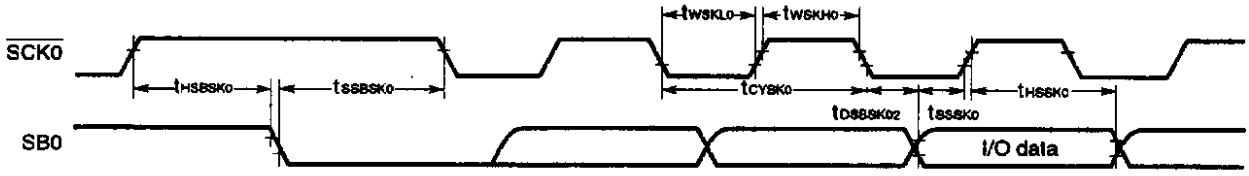


SBI Mode

Bus release signal transfer:

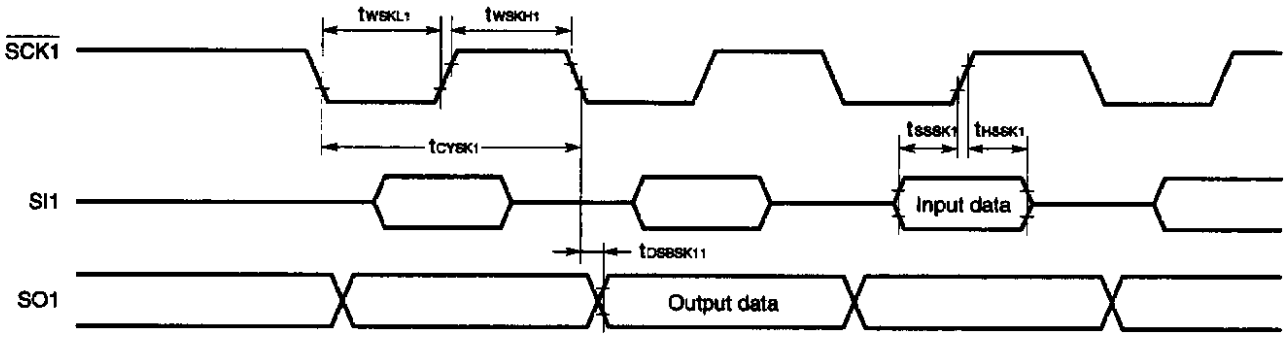


Command signal transfer:



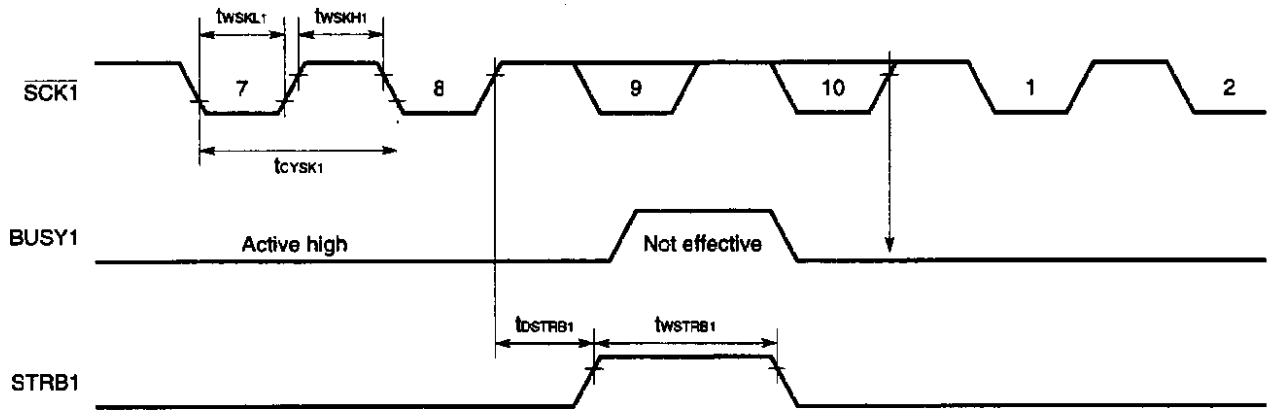
Serial Operation (SIO1)

Three-wire serial I/O mode:

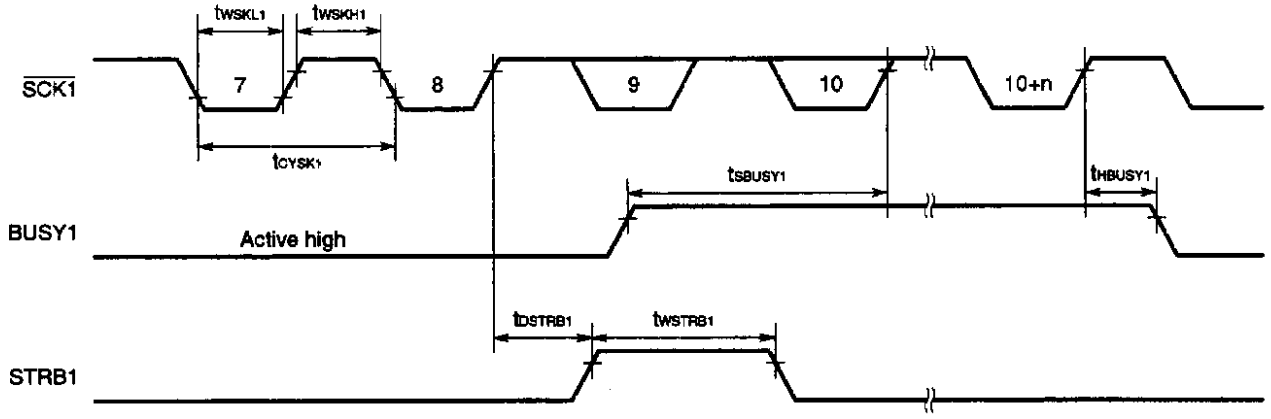


Automatic Transfer Mode (Internal Clock)

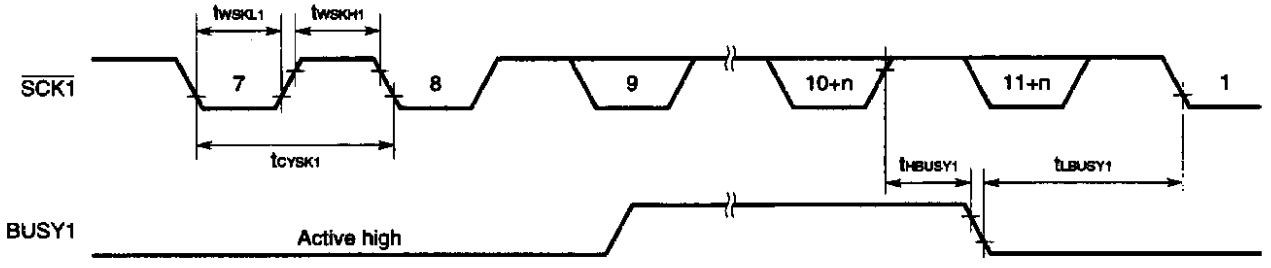
Without busy-state processing



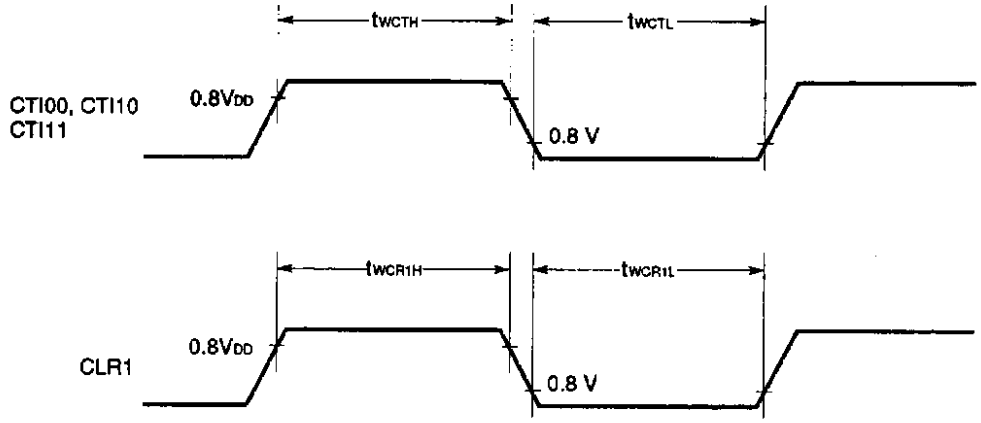
When the busy-state processing continues



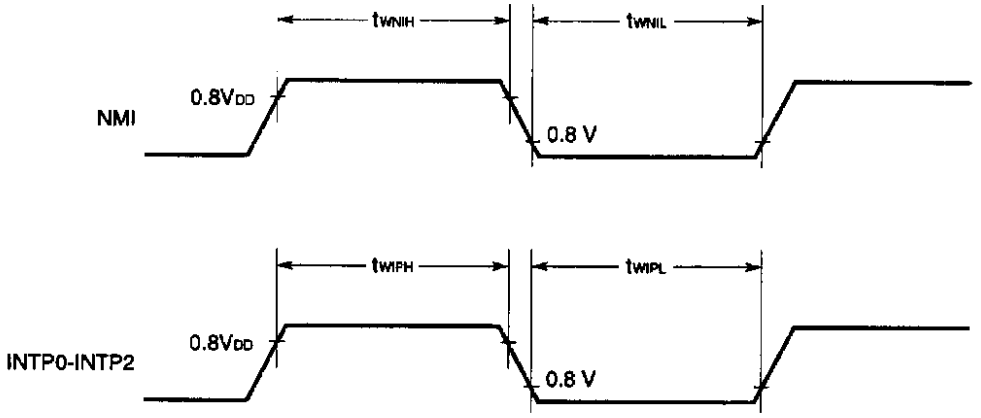
When the busy-state processing ends



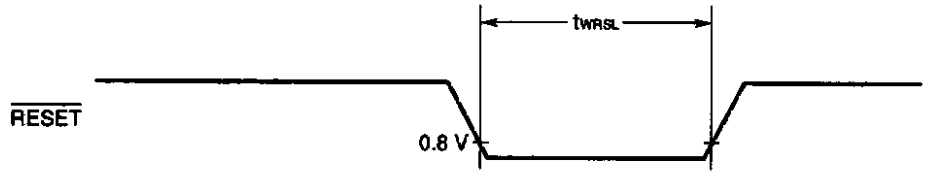
Super Timer Unit Input Timing



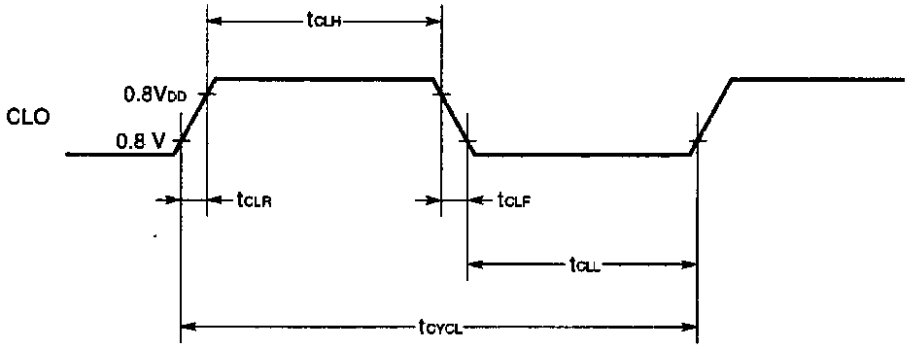
Interrupt Input Timing



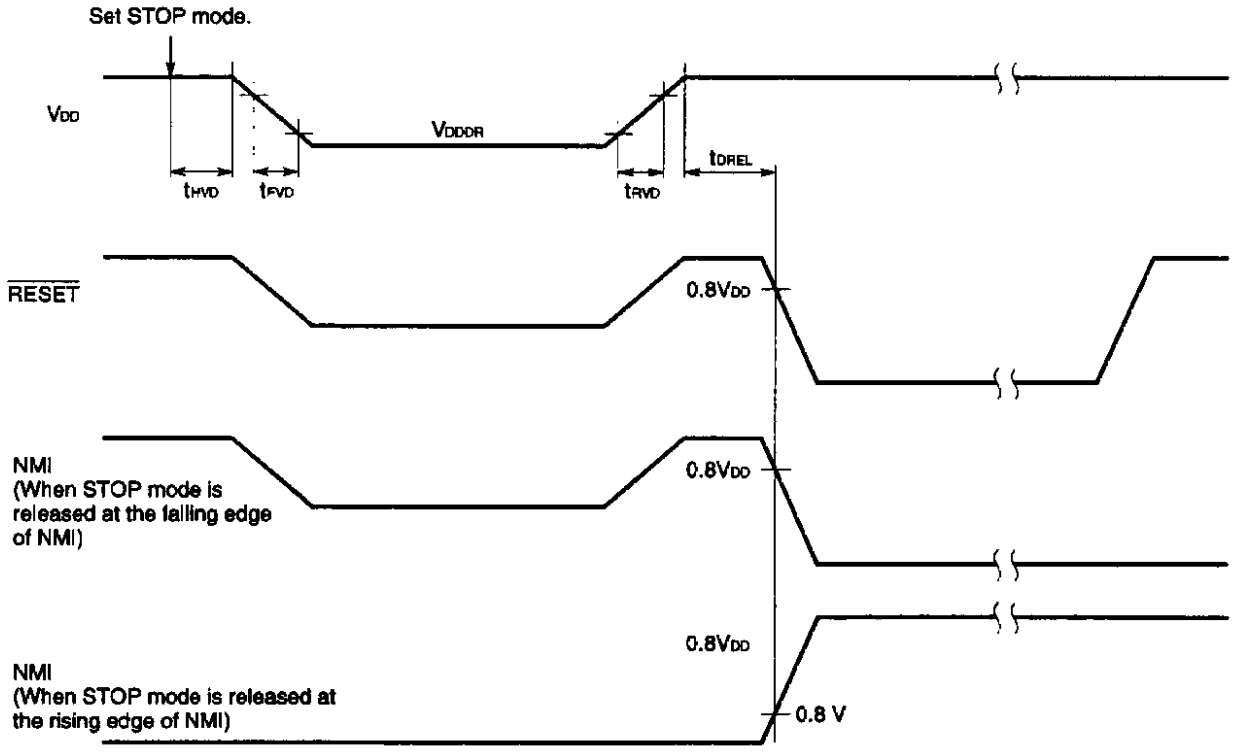
Reset Input Timing



Clock Output Timing



Data Retention Timing



9. EXAMPLE OF SYSTEM CONFIGURATION

Phase-out/Discontinued

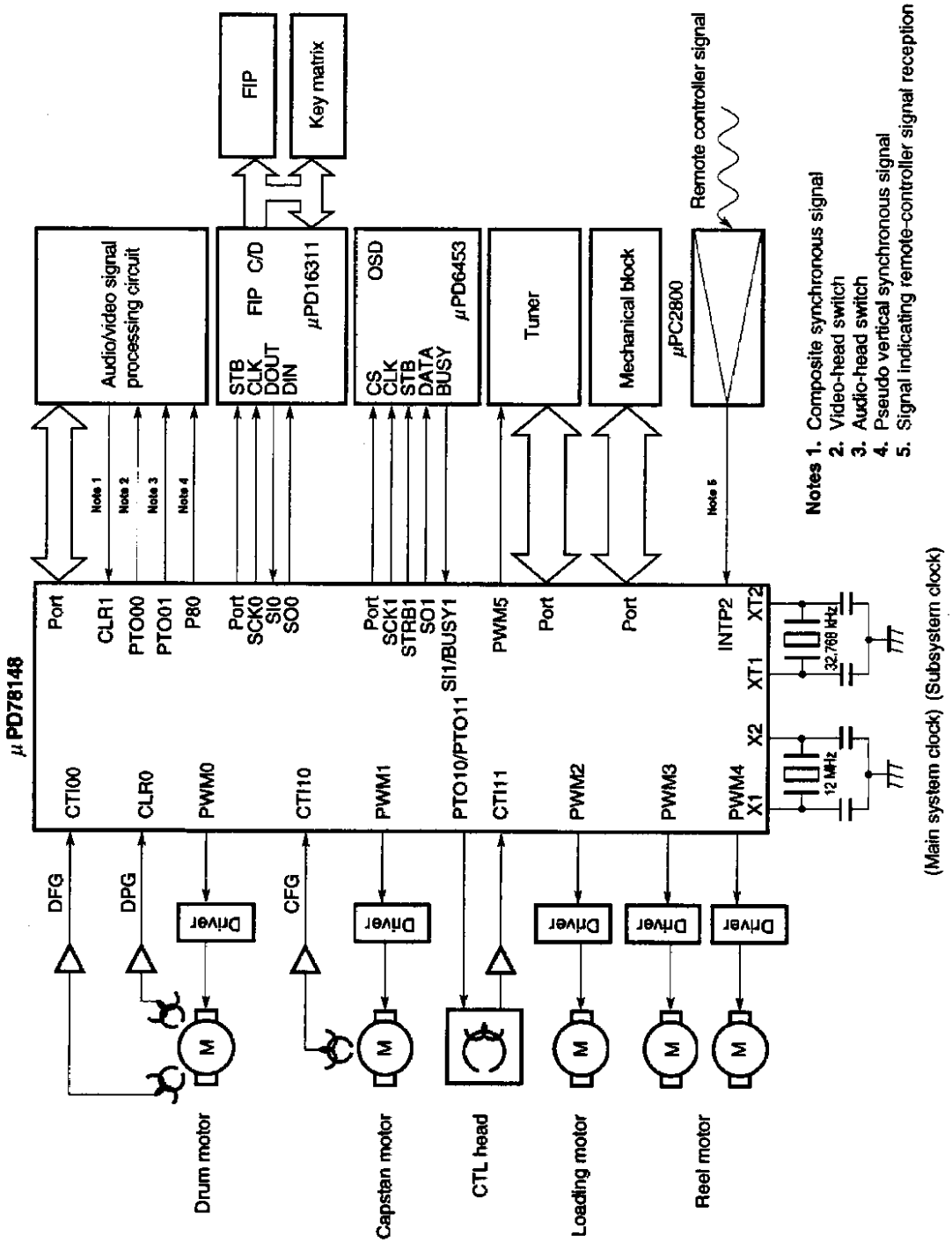
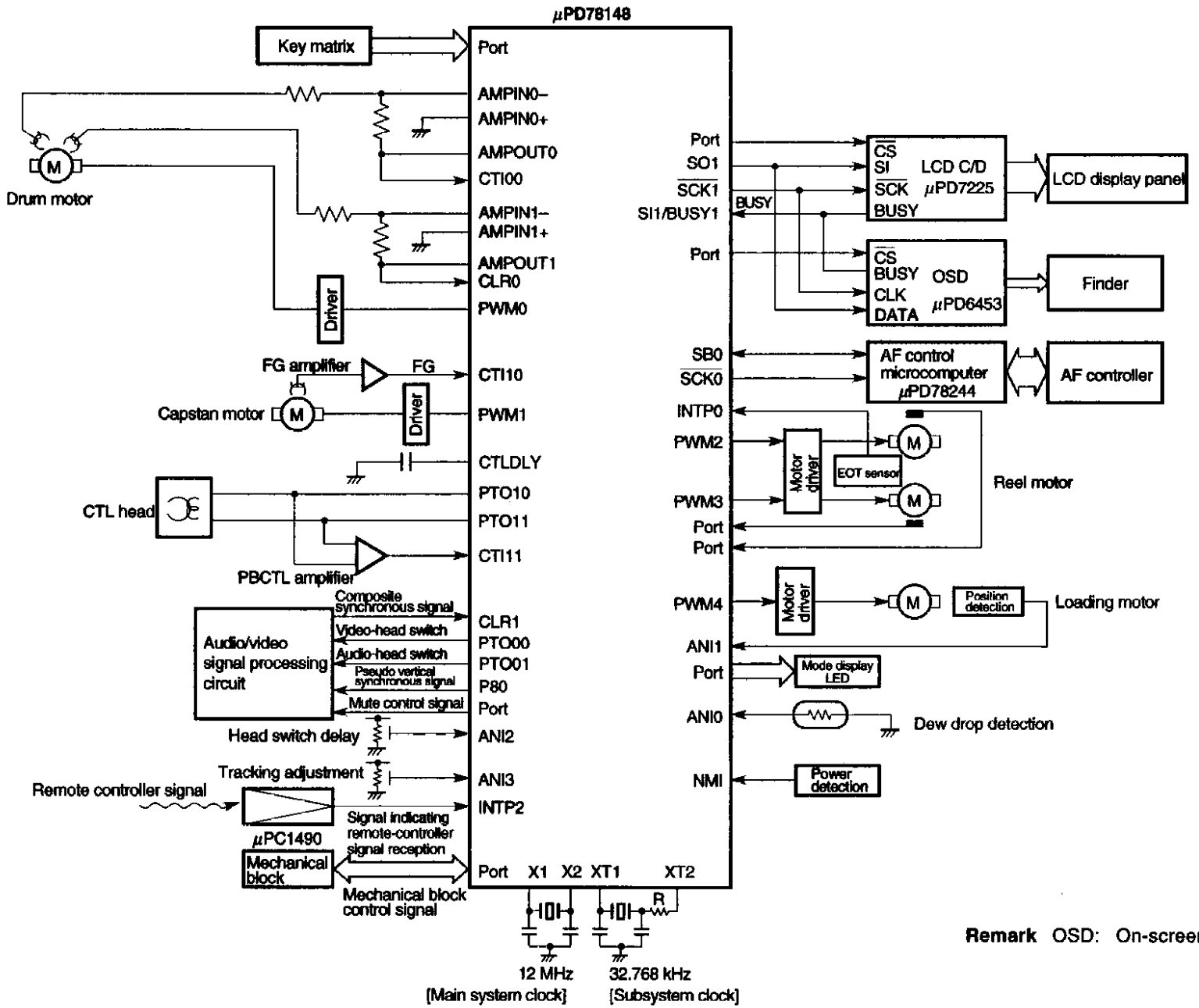


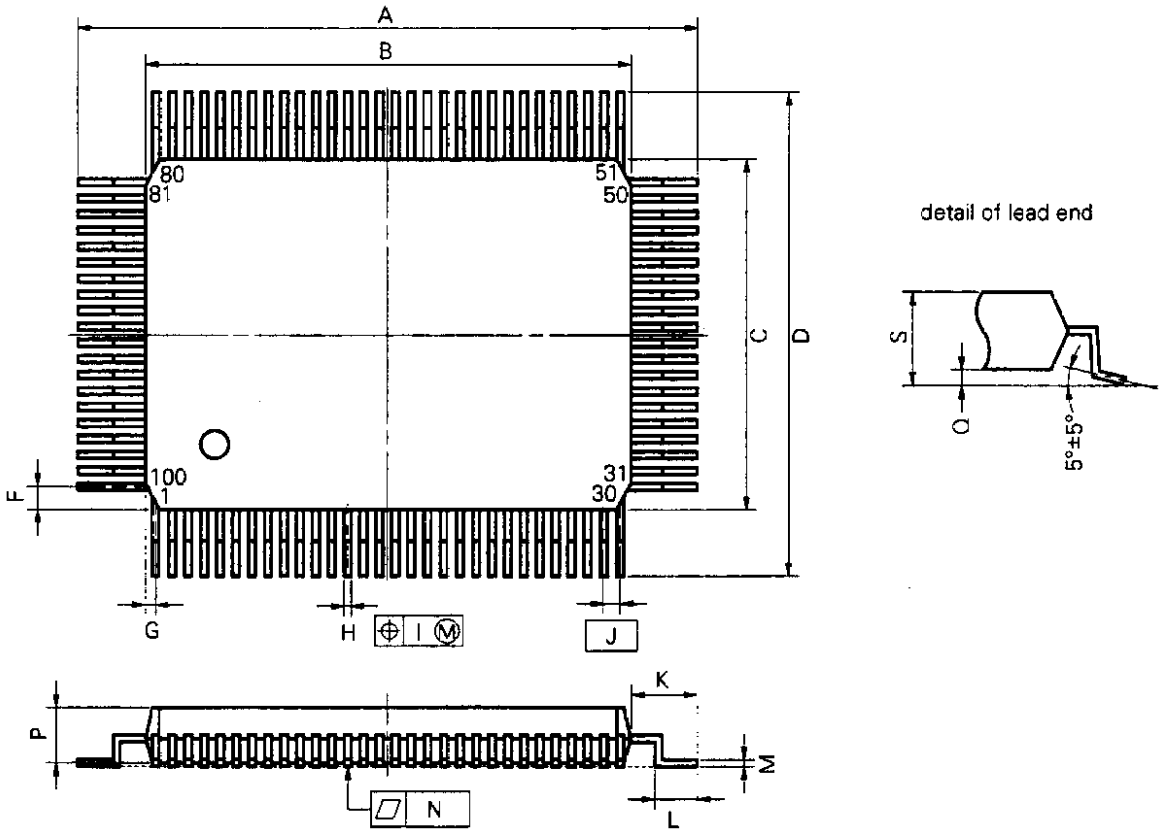
Fig. 9-2 Application to Camcorders



Remark OSD: On-screen display

10. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

11. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For the details of the recommended soldering conditions refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 11-1 Soldering Conditions for Surface-Mount Devices ★

μPD78146GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)
μPD78148GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-207-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-207-2
Wave soldering	Temperature in the soldering vessel: 260 °C or less Soldering time: 10 seconds or less Number of soldering process: 1 Preheating temperature: 120 °C max. (measured on the package surface) Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.)	WS60-207-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for each side of device)	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

APPENDIX A DIFFERENCE BETWEEN μPD78148 AND RELATED PRODUCTS (μPD78146, μPD78P148, AND μPD78138)

Function		μPD78146	μPD78148	μPD78P148	μPD78138
Minimum instruction execution time		0.33 μs (when the microcomputer operates at 12 MHz)			
ROM type		Mask ROM		PROM	Mask ROM
ROM capacity		24K bytes	32K bytes		
RAM capacity		688 bytes[Note 1]	816 bytes[Note 1]		640 bytes
I/O	Port	76[Note 2]			58
	A/D	15			8
	Others	6 (for operational amplifier I/O)			0
Real-time output port		18 (Output trigger timer can be selected.)			8 (Output trigger timer only is set.)
Super timer unit	Timer	• 16 bits × 3 • 8 bits × 3			• 16 bits × 3 • 7 bits × 1
	Counter	• 22-bit free running counter × 1 • 6-bit up/down counter × 1			• 18-bit free running counter × 1
	Capture register	• 22 bits × 2 • 16 bits × 3 • 8 bits × 2			• 18 bits × 1 • 16 bits × 4 • 7 bits × 1
	Compare register	• 16 bits × 7 • 8 bits × 3			• 16 bits × 6 • 7 bits × 1
	PWM output	• 12 bits × 2 channels (carrier frequency: 46.9 kHz/23.4 kHz) • 14 bits × 1 channel (carrier frequency: 5.9 kHz) • 8 bits × 3 channels (carrier frequency: 5.9 kHz)			• 12 bits × 2 channels (carrier frequency: 46.9 kHz/23.4 kHz)
Multiply instructions		• MULUW: 16 bits (absolute value) × 8 bits (absolute value) • MULSW: 16 bits (complement) × 8 bits (absolute value)			
Multiplier		16 bits (complement) × 16 bits (complement) Operation time: 2.67 μs			–
A/D converter		8-bit resolution × 15 channels (7 channels can also be used as ports.)			8-bit resolution × 8 channels
Serial interface		2 channels	• Channel 0: Either 3-wire SIO or SBI can be selected. • Channel 1: Only 3-wire SIO is set. 48-byte automatic data send/receive function is provided.	1 channel	Either 3-wire SIO or SBI can be selected.
Analog circuit		2 operational amplifiers are provided.			–
Interrupt	External	5			5
	Internal	20			12
Package		100-pin plastic QFP (0.65 mm pitch, 14 × 20 mm) 100-pin ceramic WQFN (14 × 20 mm) (μPD78P148 only)			80-pin plastic QFP (0.8 mm pitch, 14 × 20 mm)
$\overline{V_{SYNC}}$ separator		Removed pulse width: Either 12.7 μs or 20.7 μs can be selected.			Removed pulse width: Either 5.3 μs or 12.0 μs can be selected.
Remote controller signal reception circuit		8-bit timer 4 (TM4) is provided.			–
Clock function		The clock function of hardware is provided.			–

Notes 1. Total of dual-port RAM (256 bytes) and peripheral RAM.

2. 10 port pins are also used for analog input to the A/D converter or as analog pins for the operational amplifiers.

APPENDIX B DEVELOPMENT TOOLS

The following tools are provided for developing a system that employs the μPD78146 and μPD78148.

[Hardware]

IE-78140-R	In-circuit emulator applicable for the μPD78146, μPD78148, and μPD78P148. For debugging, connect the emulator to the host machine. The connection of the emulator to the host machine enables symbolic debugging and object file transfer between the emulator and the host machine, thus enhancing debugging efficiency. The emulator has two RS-232-C serial interfaces channels. It can be connected to PROM programmer PG-1500. It also has the Centronics interface so that an object file and symbol file can be downloaded at high speed.
EP-78140GF-R	Emulation probe for the μPD78146, μPD78148, and μPD78P148. A 100-pin conversion socket, EV-9200GF-100, is suppiled with the emulation probe, enabling easy development of a system.
EV-9200GF-100	Conversion socket produced for the 100-pin plastic QFP (14 × 20 mm excluding the leads). This socket is mounted on the PC board of the user system. The socket is used together with the EP-78140GF-R.
EV-9900	Jig used for removing the μPD78P148K from the EV-9200GF-100
PG-1500	A PROM programmer. Programs can be written into PROMs in a stand-alone mode or by remote control from a host machine when this programmer is connected with the accessory board and optional programmer adapter. Products programmable with the PG-1500 are commonly used PROMs (256K-bit to 4M-bit) and single chip microcomputers containing PROM.
PA-78P148K	PROM programmer adapter for the μPD78P148. The adapter is used with the PG-1500.

[Software]

RA78K/I relocatable assembler	This relocatable assembler can be used for all 78K/I series emulators. With its macro functions, it allows the user to improve program development efficiency. A structured-programming assembler is also provided, which enables explicit description of program control structures. This assembler greatly improves productivity in program production and maintenance.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS™ Ver. 3.30 to Ver. 5.00A Note	3.5-inch 2HD	μS5A13RA78K1
			5.25-inch 2HD	μS5A10RA78K1
★	IBM PC/AT™ or compatibles	See "OS for IBM PC".	5.25-inch 2HC	μS7B10RA78K1
IE-78130-R control program (IE controller)	This control program allows the user to control the IE-78130-R from the host machine. Its automatic command execution function ensures more efficient debugging.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS Ver. 3.30 to Ver. 5.00A Note	3.5-inch 2HD	μS5A13IE78130
			5.25-inch 2HD	μS5A10IE78130
★	IBM PC/AT or compatibles	See "OS for IBM PC".	5.25-inch 2HC	μS7B10IE78130
PG-1500 controller	This program enables the host machine to control the PG-1500 under the serial interface and parallel interface.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS Ver. 3.30 to Ver. 5.00A Note	3.5-inch 2HD	μS5A13PG1500
			5.25-inch 2HD	μS5A10PG1500
★	IBM PC/AT or compatibles	See "OS for IBM PC".	3.5-inch 2HD	μS7B13PG1500
			5.25-inch 2HC	μS7B10PG1500

Note These software products cannot use the task swap function, which is available in MS-DOS Ver. 5.00 and Ver. 5.00A.

Remark The operation of software products that include the assembler and IE controller is guaranteed only under the OSs on the corresponding host machines described above.

OS for IBM PC

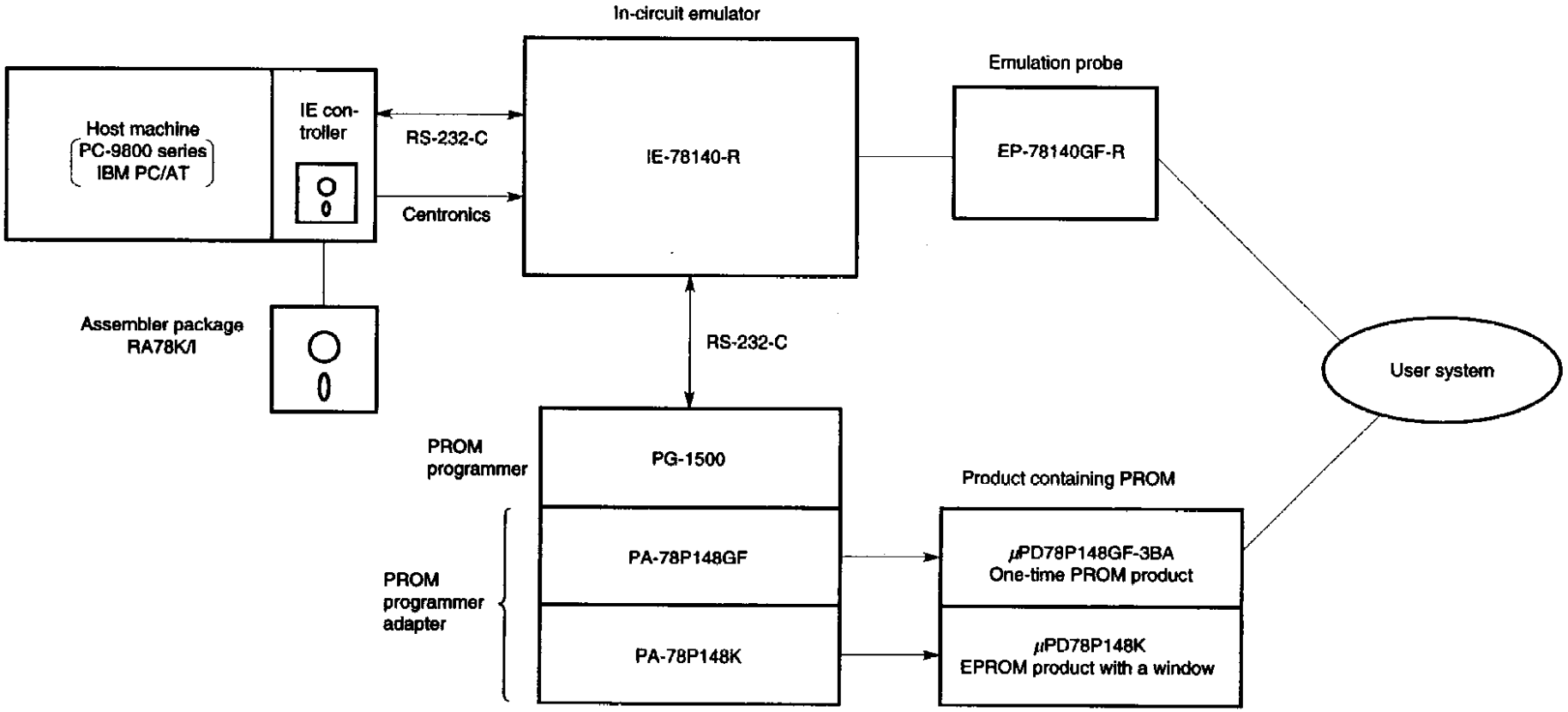
The following operating systems are supported for IBM PC.

OS	Version
PC DOS™	Ver. 3.1 to Ver. 6.3
	J6.1/V[Note] to J6.3/V[Note]
IBM DOS™	J5.02/V[Note]
MS-DOS	Ver. 5.0 to Ver. 6.2
	5.0/V[Note] to 6.2/V[Note]

Note Supports English mode only.

Caution These software products cannot use the task swap function, which is available in Ver. 5.00 and after.

Phase-out/Discontinued



Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

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