NEC

MOS INTEGRATED CIRCUIT

μPD780961, 780962, 780963, 780964

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD780961, 780962, 780963, and 780964, which are members of the μPD780964 subseries of the 78K/0 series, are suited to control general-purpose inverters.

Compared to the conventional μPD78014 subseries or μPD78018F subseries products, EMI (Electro Magnetic Interface) noise is reduced for the μPD780924 subseries products.

A flash memory version, the μPD78F0964, that can operate within the same power supply voltage range as the mask ROM version, and various development tools are also provided.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

μPD780924, 780964 Subseries User's Manual : In preparation

78K/0 Series User's Manual Instructions : IEU-1372

FEATURES

- Internal ROM and RAM

Item / Part Number	Program memory (ROM)	Data memory (internal high-capacity RAM)	Package
μPD780961	8 Kbytes	512 bytes	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 x 14 mm)
μPD780962	16 Kbytes		
μPD780963	24 Kbytes	1024 bytes	
μPD780964	32 Kbytes		

- External memory expansion space: 48 Kbytes
- Minimum instruction execution time: 0.24 μs (@ f_X = 8.38-MHz operation)
- I/O ports: 47
- 10-bit resolution A/D converter: eight channels
- Serial interface: two channels
- Timer: Five channels
- Power supply voltage: V_{DD} = 2.7 to 5.5 V

APPLICATIONS

Motor control for inverter-type air conditioners, washing machines, etc.

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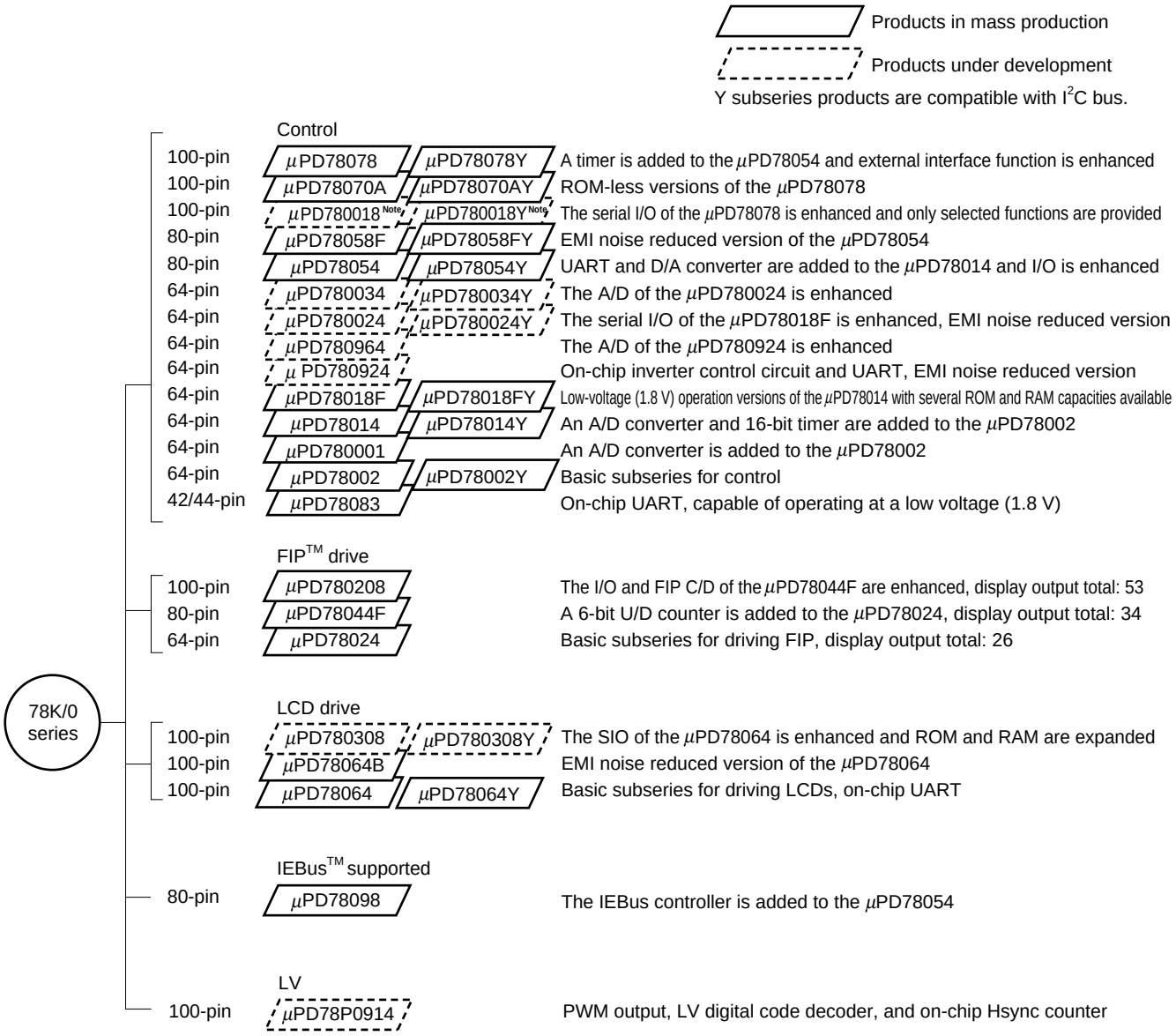
ORDERING INFORMATION

Part Number	Package
μPD780961CW-×××	64-pin plastic shrink DIP (750 mil)
μPD780962CW-×××	64-pin plastic shrink DIP (750 mil)
μPD780963CW-×××	64-pin plastic shrink DIP (750 mil)
μPD780964CW-×××	64-pin plastic shrink DIP (750 mil)
μPD780961GC-×××-AB8	64-pin plastic QFP (14 x 14 mm)
μPD780962GC-×××-AB8	64-pin plastic QFP (14 x 14 mm)
μPD780963GC-×××-AB8	64-pin plastic QFP (14 x 14 mm)
μPD780964GC-×××-AB8	64-pin plastic QFP (14 x 14 mm)

Remark xxx indicates the ROM code suffix.

78K/0 SERIES DEVELOPMENT

The 78K/0 series product line-up is shown below. Subseries names are shown inside frames.



Note Under planning

The table below shows the main differences between subseries.

Subseries \ Functions		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
For control	μPD78078	32 K to 60 K	4ch	1ch	1ch	1ch	8ch	—	2ch	3ch (UART: 1ch)	88	1.8 V	Available
	μPD78070A	—									61	2.7 V	
	μPD780018	48 K to 60 K							—	2ch	88		
	μPD78058F		2ch						2ch	3ch (UART : 1ch)	69		
	μPD78054	16 K to 60 K										2.0 V	
	μPD780034	8 K to 32 K					—	8ch	—		51	1.8 V	
	μPD780024						8ch	—					
	μPD780964		3ch	**Note**	—		—	8ch		2ch (UART : 2ch)	47	2.7ch	
	μPD780924						8ch	—					
	μPD78018F	8 K to 60 K	2ch	1ch	1ch					2ch	53	1.8 V	
	μPD78014	8 K to 32 K										2.7 V	
	μPD780001	8 K		—	—					1ch	39		—
	μPD78002	8 K to 16 K			1ch		—				53		Available
	μPD78083				—		8ch			1ch (UART : 1ch)	33	1.8 V	—
For FIP drive	μPD780208	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	—	—	2ch	74	2.7 V	—
	μPD78044F	16 K to 40 K									68		
	μPD78024	24 K to 32 K									54		
For LCD drive	μPD780308	48 K to 60 K	2ch	1ch	1ch	1ch	8ch	—	—	3ch (UART: 1ch)	57	1.8 V	—
	μPD78064B	32 K								2ch (UART : 1ch)		2.0 V	
	μPD78064	16 K to 32 K											
IEBus support	μPD78098	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	—	2ch	3ch (UART: 1ch)	69	2.7 V	Available
For LV	μPD78P0914	32K	6ch	—	—	1ch	8ch	—	—	2ch	54	4.5 V	Available

Note 10-bit timer: one channel

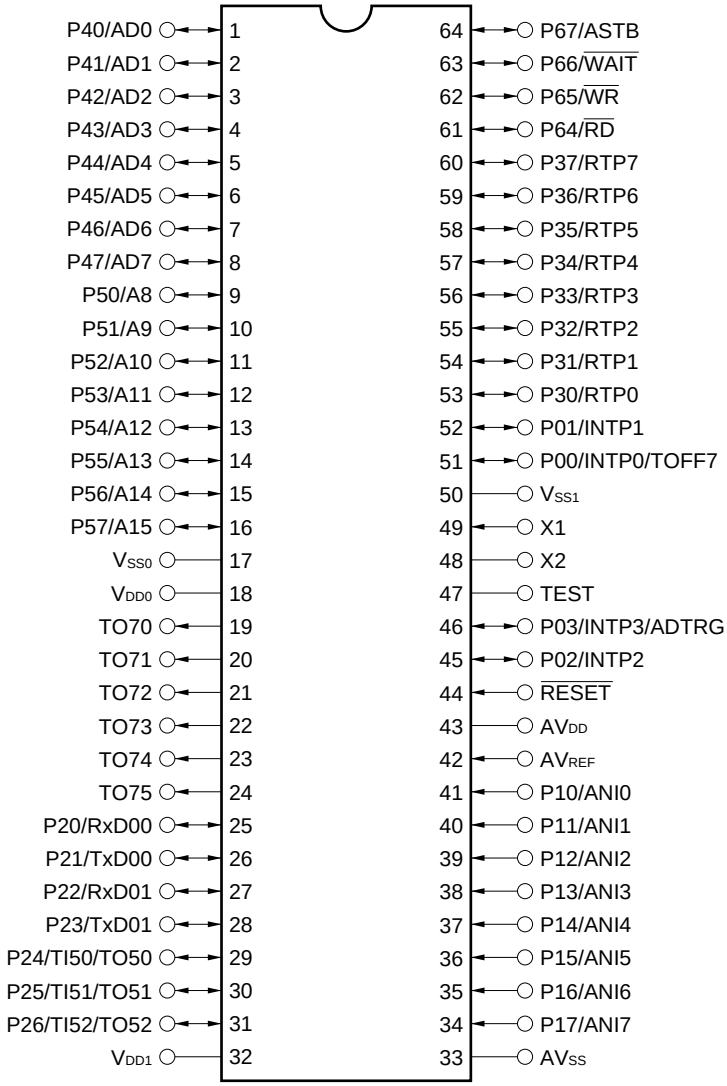
FUNCTION OVERVIEW

Item \ Product Name		μPD780961	μPD780962	μPD780963	μPD780964
Internal memory	ROM	8 Kbytes	16 Kbytes	24 Kbytes	32 Kbytes
	Internal high-speed RAM	512 bytes		1024 bytes	
Memory space		64 Kbytes			
General-purpose register		8 bits x 32 registers (8 bits x 8 registers x 4 banks)			
Instruction cycle		On-chip instruction execution time variable function 0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38-MHz operation with system clock)			
Instruction set		• 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.			
I/O ports		Total : 47 • CMOS inputs : 8 • CMOS I/Os : 39			
Real-time output ports		8 bits x 1 or 4 bits x 2			
A/D converter		• 8-bit resolution x 8 channels • Power supply voltage: AV_{DD} = 2.7 to 5.5 V			
Serial interface		UART x 2 channels			
Timer		• 16-bit timer/event counter : 3 channels • 10-bit timer : 1 channel • Watchdog timer : 1 channel			
Timer output		9 (8-bit PWM output x 3, and inverter control output x 6)			
Vectored interrupt	Maskable interrupts	Internal: 12, external: 4			
	Non-maskable interrupt	Internal: 1			
	Software interrupt	1			
Power supply voltage		V_{DD} = 2.7 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85 °C			
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 x 14 mm)			

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **64-Pin Plastic Shrink DIP (750 mil)**
  μPD780961CW-×××, 780962CW-×××, 780963CW-×××, 780964CW-×××

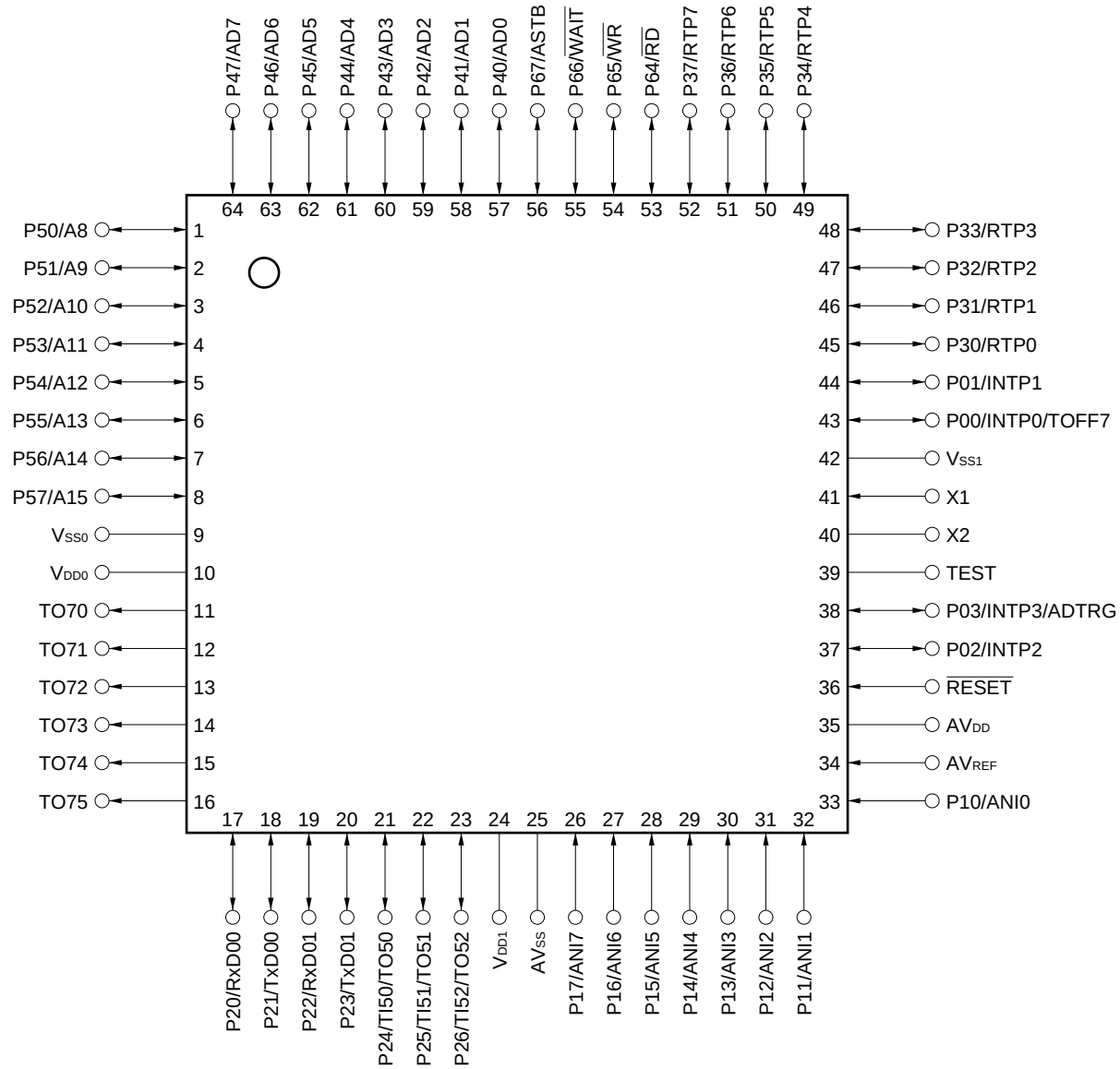


Cautions 1. Connect the TEST pin to V_{SS0} directly.
2. Connect the AV_{DD} pin to V_{DD0}.
3. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780961, 780962, 780963, or 780964 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{SS1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-Pin Plastic QFP (14 x 14 mm)**

  μPD780961GC-×××-AB8, 780962GC-×××-AB8, 780963GC-×××-AB8, 780964GC-×××-AB8



Cautions 1. Connect the TEST pin to V_{SS0} directly.

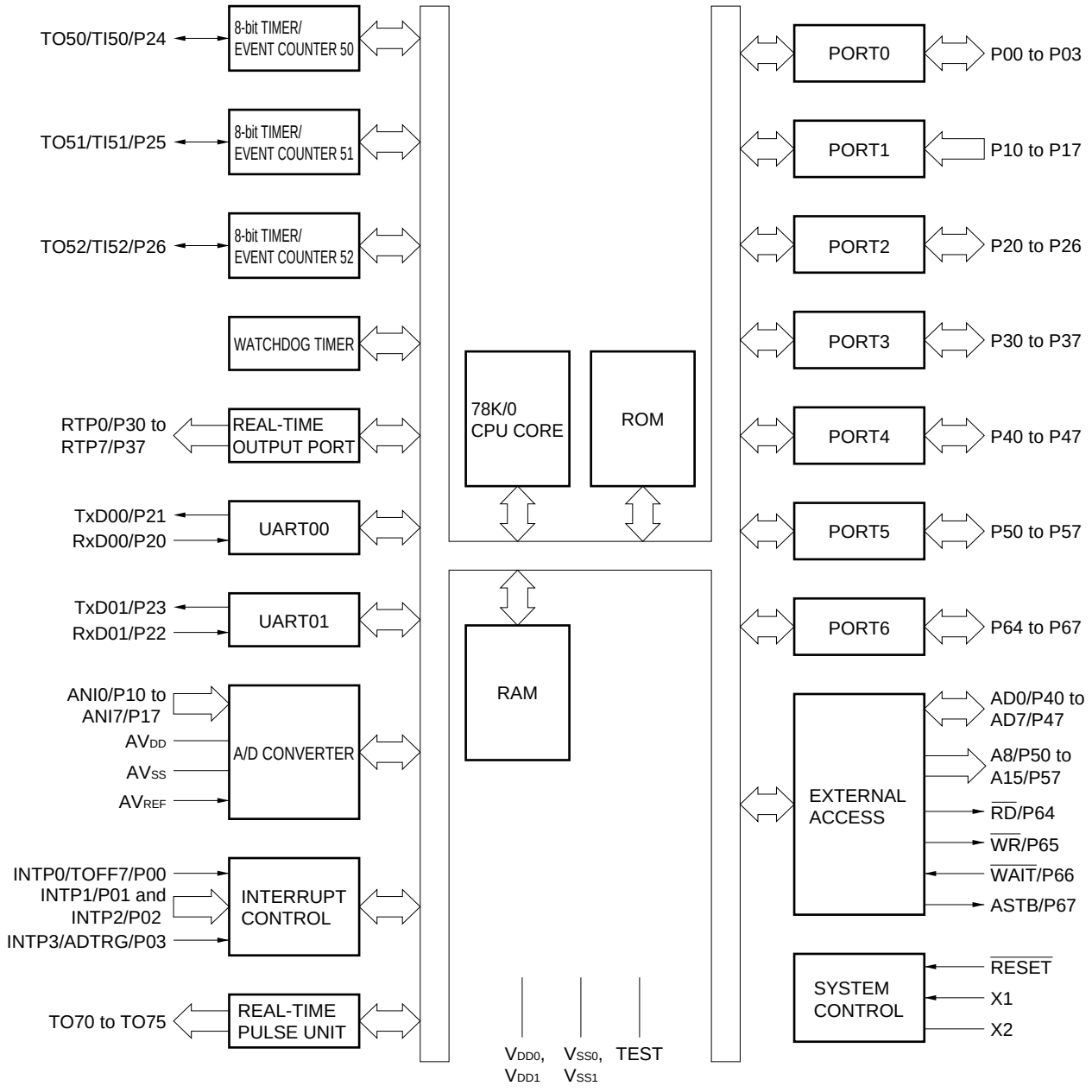
2. Connect the AV_{DD} pin to V_{DD0}.

3. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780961, 780962, 780963, or 780964 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{SS1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15	:	Address Bus
AD0 to AD7	:	Address/Data Bus
ADTRG	:	AD Trigger Input
ANI0 to ANI7	:	Analog Input
ASTB	:	Address Strobe
AV_{DD}	:	Analog Power Supply
AV_{REF}	:	Analog Reference Voltage
AV_{SS}	:	Analog Ground
INTP0 to INTP3	:	Interrupt From Peripherals
P00 to P03	:	Port 0
P10 to P17	:	Port 1
P20 to P26	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P64 to P67	:	Port 6
$\overline{RD}$	:	Read Strobe
$\overline{RESET}$	:	Reset
RTP0 to RTP7	:	Real-time Port
RxD00, RxD01	:	Receive Data
TEST	:	Test
TI50 to TI52	:	Timer Input
TO50 to TO52, TO70 to TO75	:	Timer Output
TOFF7	:	Timer Output Off
TxD00, TxD01	:	Transmit Data
V_{DD0}, V_{DD1}	:	Power Supply
V_{SS0}, V_{SS1}	:	Ground
$\overline{WAIT}$	:	Wait
$\overline{WR}$	:	Write Strobe
X1, X2	:	Crystal

2. BLOCK DIAGRAM



Remark Internal ROM and RAM capacity varies depending on the product.

3. PIN FUNCTION LIST

3.1 PORT PINS

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	INTP0/TOFF7
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1. 8-bit input only port.	Input	ANI0 to ANI7
P20	I/O	Port 2. 7-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	RxD00
P21				TxD00
P22				RxD01
P23				TxD01
P24				TI50/TO50
P25				TI51/TO51
P26				TI52/TO52
P30 to P37	I/O	Port 3. 8-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	AD0 to AD7
P50 to P57	I/O	Port 5. 8-bit I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. When used as an input port, an on-chip pull-up resistor can be connected by software..	Input	A8 to A15
P64	I/O	Port 6. 4-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	$\overline{RD}$
P65				$\overline{WR}$
P66				$\overline{WAIT}$
P67				ASTB

3.2 NON PORT PINS

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input that can specify the effective edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TOFF7
INTP1			Input	P01
INTP2			Input	P02
INTP3			Input	P03/ADTRG
TI50	Input	External count clock input to timer (TM50).	Input	P24/TO50
TI51		External count clock input to timer (TM51).	Input	P25/TO51
TI52		External count clock input to timer (TM52).	Input	P26/TO52
TO50	Output	Timer (TM50) output.	Input	P24/TI50
TO51		Timer (TM51) output.	Input	P25/TI51
TO52		Timer (TM52) output.	Input	P26/TI52
RTP0 to RTP7	Output	Real-time output port that outputs pulses in synchronization with trigger signals outputs from the real-time pulse unit.	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output.	Input	P21
TxD01			Input	P23
RxD00	Input	Asynchronous serial interface serial data input.	Input	P20
RxD01			Input	P22
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	External trigger signal input to the A/D converter.	Input	P03/INTP3
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control.	Hi-Z	–
TOFF7	Input	Timer output (TO70 to TO75) stop interrupt input.	Input	P00/INTP0
AD0 to AD7	I/O	Lower address/data bus when memory is expanded externally.	Input	P40 to P47
A8 to A15	Output	Upper address bus when memory is expanded externally.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for external memory read operation.	Input	P64
$\overline{WR}$		Strobe signal output for external memory write operation.	Input	P65
$\overline{WAIT}$	Input	Wait insertion when accessing external memory.	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory.	Input	P67
AV_{REF}	Input	A/D converter reference voltage input.	–	–
AV_{DD}	–	A/D converter analog power supply. Connect to V_{DD0}.	–	–
AV_{SS}	–	A/D converter ground potential. Connect to V_{SS0}.	–	–
$\overline{RESET}$	Input	System reset input.	–	–
X1	Input	Crystal connection for system clock oscillation.	–	–
X2	–		–	–
V_{DD0}	–	Positive power supply for ports.	–	–
V_{SS0}	–	Ground potential for ports.	–	–
V_{DD1}	–	Positive power supply except for ports.	–	–
V_{SS1}	–	Ground potential except for ports.	–	–
TEST	–	Test mode set pin. Connect to V_{SS0} directly.	–	–

3.3 RECOMMENDED CONNECTION OF UNUSED PINS

The recommended connections of unused pins are shown in Table 3-1.

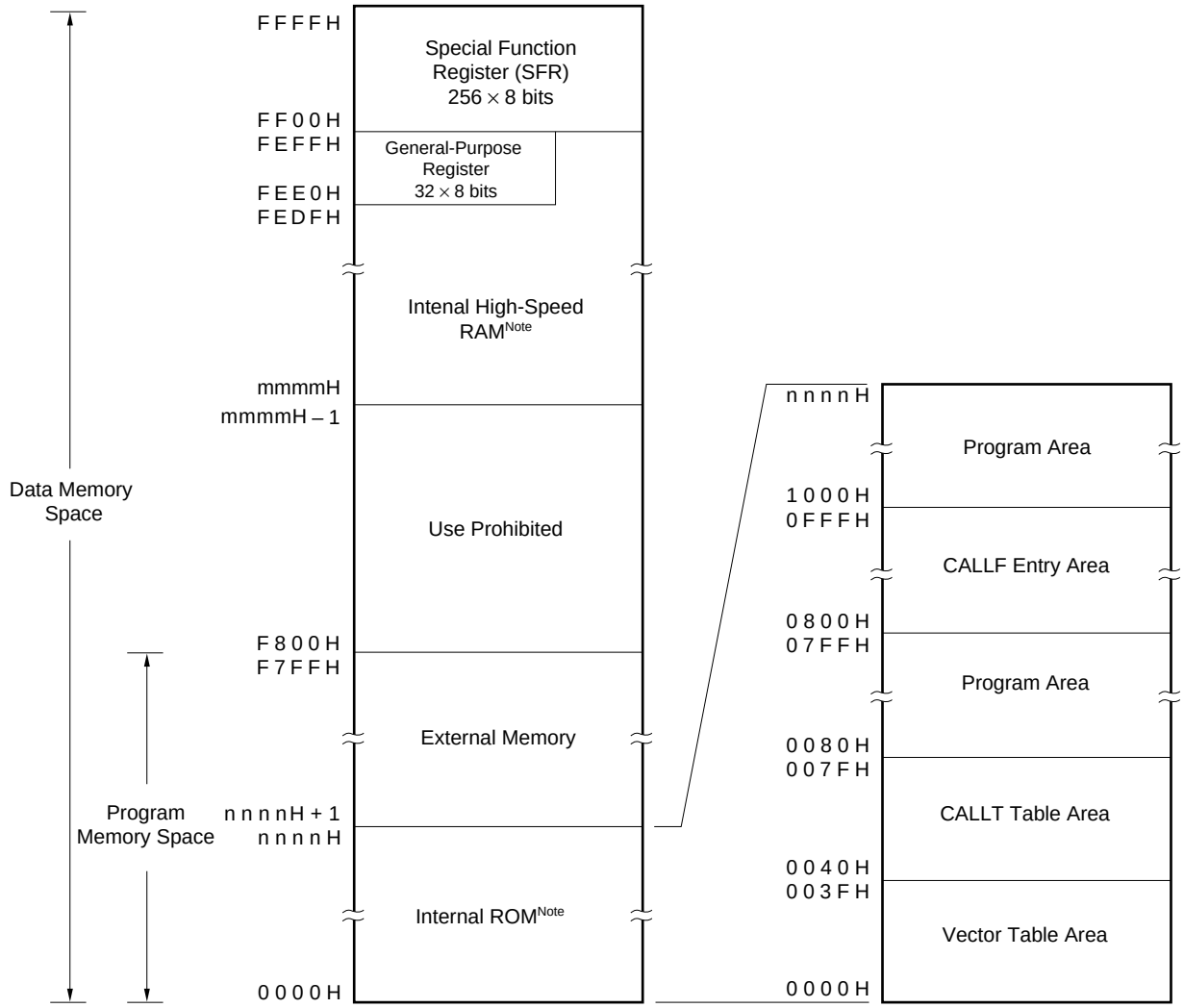
Table 3-1. Recommended Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
P00/INTP0/TOFF7	I/O	Individually connect to V_{SS0} via a resistor.
P01/INTP1		
P02/INTP2		
P03/INTP3/ADTRG		
P10/ANI0 to P17/ANI7	Input	Individually connect to V_{DD0} or V_{SS0} via a resistor.
P20/RxD00	I/O	
P21/TxD00		
P22/RxD01		
P23/TxD01		
P24/TI50/TO50		
P25/TI51/TO51		
P26/TI52/TO52		
P30/RTP0 to P37/RTP7		
P40/AD0 to P47/AD7		
P50/A8 to P57/A15		
P64/$\overline{RD}$		
P65/$\overline{WR}$		
P66/$\overline{WAIT}$		
P67/ASTB		
TO70 to TO75	Output	Open
AV_{DD}	–	Connect to V_{DD0}.
AV_{REF}		Connect to V_{SS0}.
AV_{SS}		
TEST		Connect to V_{SS0} directly.

4. MEMORY SPACE

The memory map of the μPD780961, 780962, 780963, and 780964 is shown in Figure 4-1.

Figure 4-1. Memory Map



Note The internal ROM and internal high-speed RAM capacity differ depending on the product (see the table below).

Product Name	Intenal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD780961	1FFFH	FD00H
μPD780962	3FFFH	
μPD780963	5FFFH	FB00H
μPD780964	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

Two kinds of I/O ports are provided.

- CMOS input (Port 1) : 8
- CMOS input/output (Port 0, ports 2 to 6) : 39

Total : 47

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P01 to P03	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 1	P10 to P17	Input only port.
Port 2	P20 to P26	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 3	P30 to P37	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 4	P40 to P47	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 5	P50 to P57	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software. LEDs can be driven directly.
Port 6	P64 to P67	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.

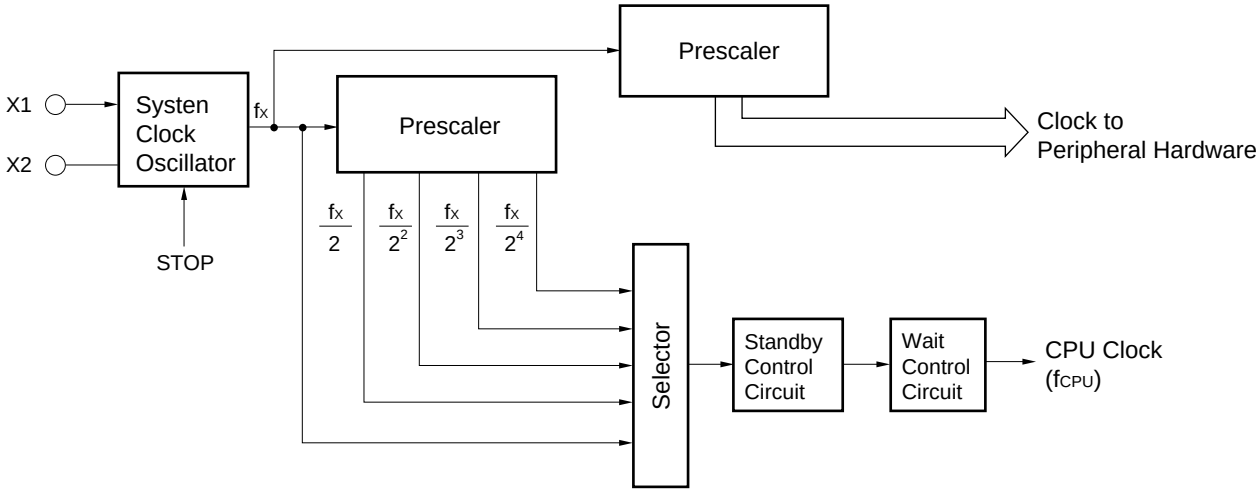
5.2 CLOCK GENERATOR

A system clock generator is incorporated.

The instruction exection time can be changed.

- 0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38-MHz operation with system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTERS

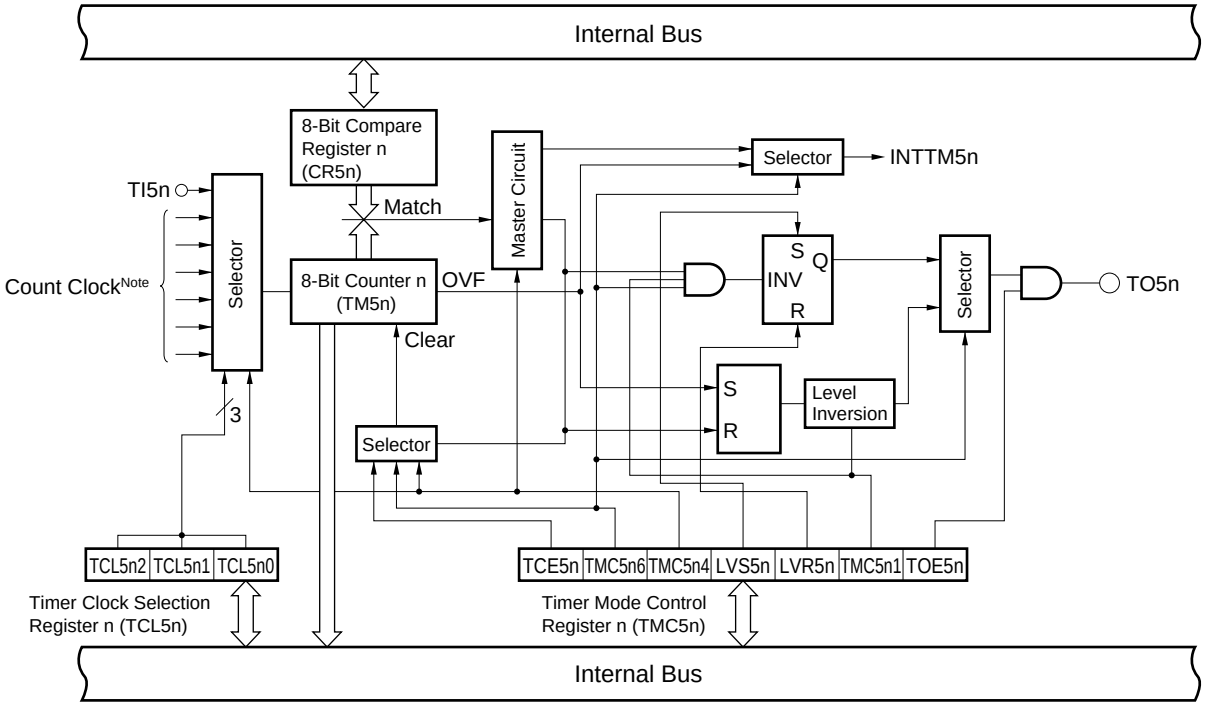
Five timer/event counter channels are incorporated.

- 8-bit timer/event counter : 3 channels
- 10-bit timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		8-bit Timer/Event Counter	10-bit Timer	Watchdog Timer
Type	Interval timer	3 channels	1 channel	1 channel
	External event counter	3 channels	–	–
Functions	Timer output	3 outputs	6 outputs	–
	PWM output	3 outputs	–	–
	Square wave output	3 outputs	–	–
	Interrupt request	3	1	1

Figure 5-2. 8-Bit Timer/Event Counter Block Diagram



Note Count clock differs depending on the timer

TM50 : $f_X/2$, f_X2^3, f_X2^5, f_X2^7, f_X2^9, f_X^{11}

TM51 : f_X, $f_X/2$, f_X2^2, f_X2^3, f_X2^4, f_X2^5

TM52 : f_X2^4, f_X2^5, f_X2^6, f_X2^7, f_X2^8, f_X2^9

Remark n = 0 to 2

Figure 5-3. 10-bit Timer Block Diagram

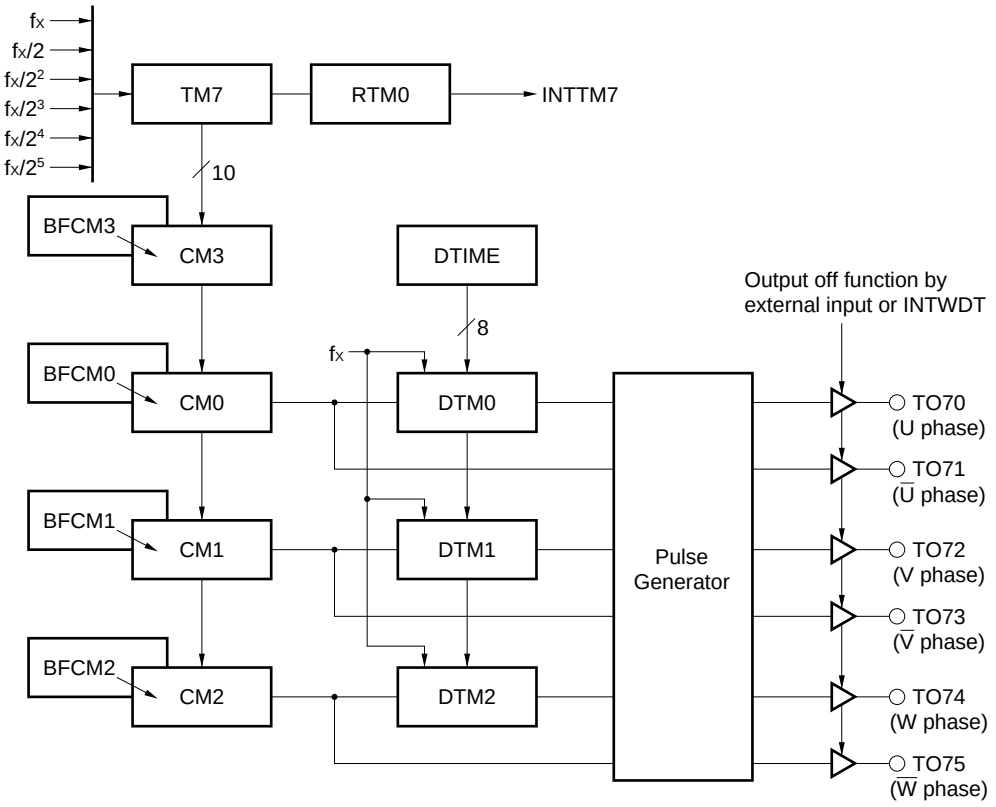
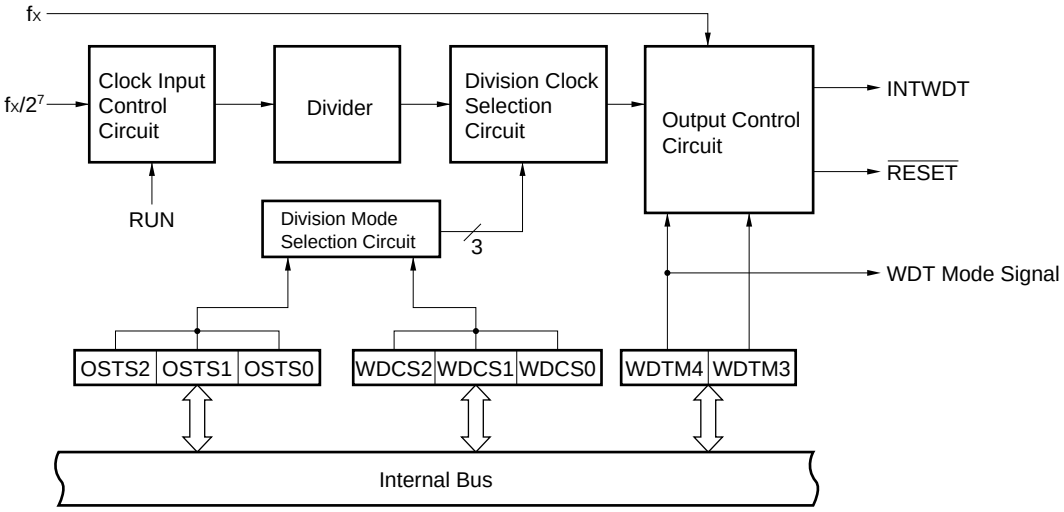


Figure 5-4. Watchdog Timer Block Diagram

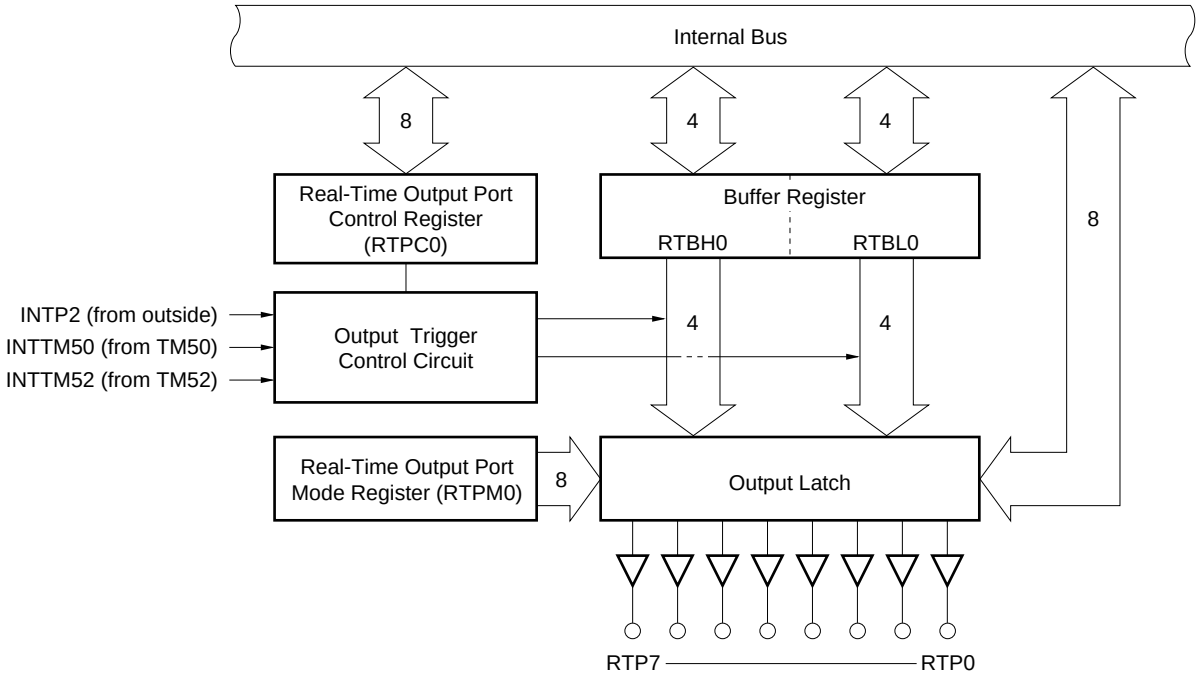


5.4 REAL-TIME OUTPUT PORT

The real-time output port outputs data stored in buffers in synchronization with match interrupts of 8-bit timer/event counters (TM50 and TM52) or external interrupts, enabling to output pulses without jitter.

Therefore, the real-time output method is suited for applications which output given patterns at set intervals.

Figure 5-5. Real-Time Output Port Block Diagram

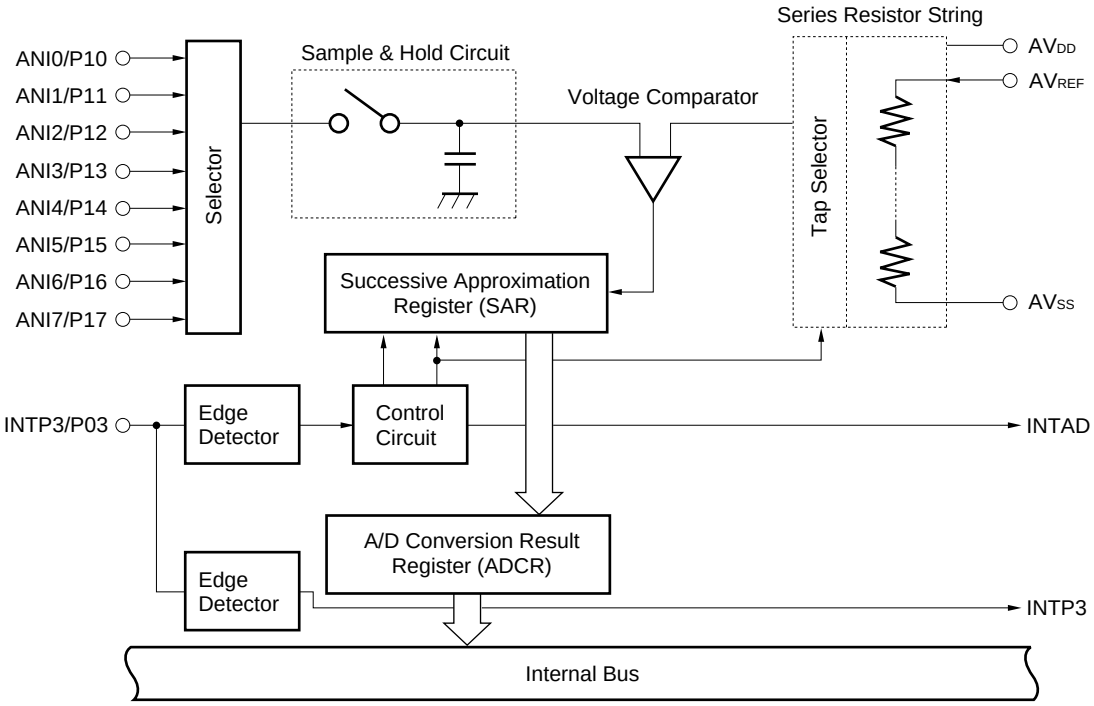


5.5 A/D CONVERTER

Eight 10-bit resolution A/D converter channels are incorporated.
A/D conversion by the following two methods.

- Hardware start
- Software start

Figure 5-6. A/D Converter Block Diagram



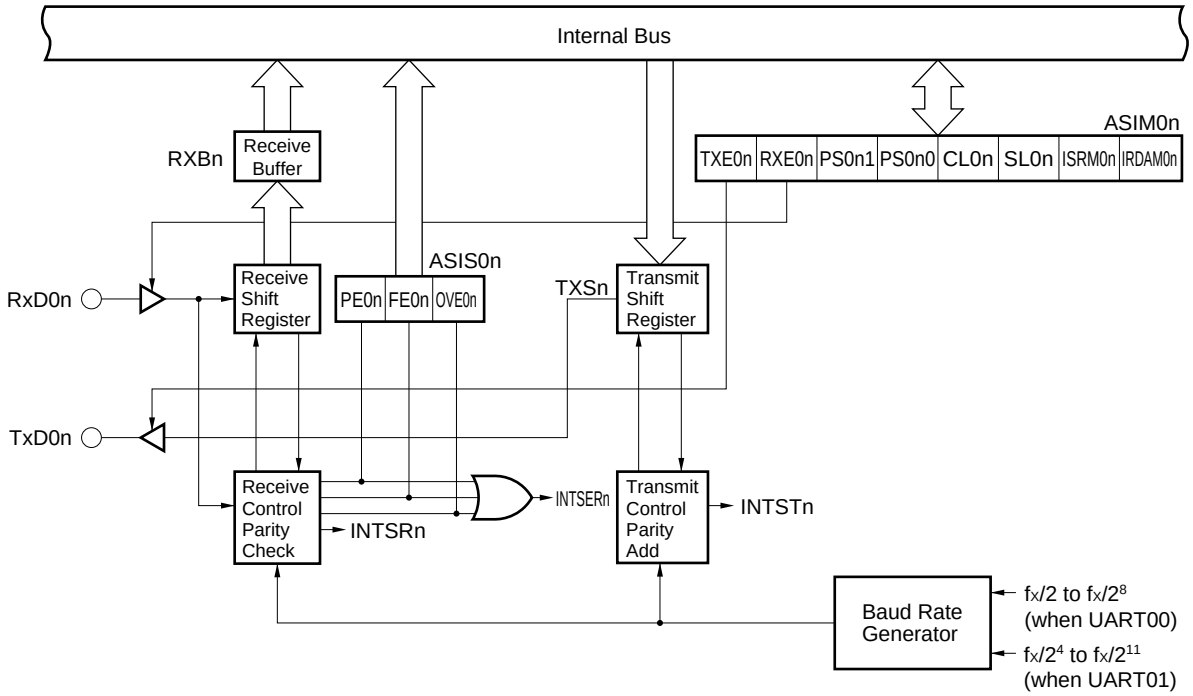
5.6 SERIAL INTERFACE

Two independent serial interface channels (UART00 and UART01) are incorporated.

Each serial interface incorporates a baud-rate generator. Therefore, it is possible to set a serial transfer rate that is independent of the operating clock frequency.

The serial transfer rate can be set from 75 to 76800 bps (@ fx = 8.38-MHz operation) by setting the mode register.

Table 5-7. Serial Interface Block Diagram



Remark n = 0, 1

6. INTERRUPT FUNCTIONS

There are 18 interrupt functions of three different kinds as shown below.

- Non-maskable interrupt : 1
- Maskable interrupts : 16
- Software interrupt : 1

Table 6-1. Interrupt Source List

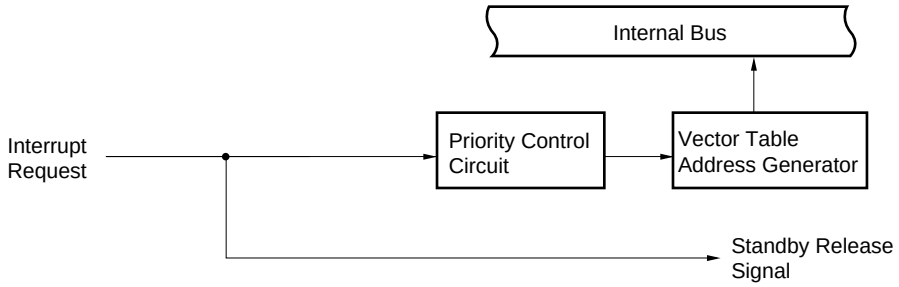
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuratin Type Note 2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (when non-maskable interrupt is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTTM7	TM7 under flow	Internal	000EH	(B)
	6	INTSER0	UART00 receive error generation		0010H	
	7	INTSR0	UART00 receive termination		0012H	
	8	INTST0	UART00 transmit termination		0014H	
	9	INTSER1	UART01 receive error generation		0016H	
	10	INTSR1	UART01 receive termination		0018H	
	11	INTST1	UART01 transmit termination		001AH	
	12	INTTM50	TM50 and CR50 match signal generation		001CH	
	13	INTTM51	TM51 and CR51 match signal generation		001EH	
	14	INTTM52	TM52 and CR52 match signal generation		0020H	
	15	INTAD0	A/D conversion termination		0022H	
Software	—	BRK	BRK instruction execution	—	003EH	(D)

Notes 1. The default priority is the priority applicable when more than one maskable interrupt is generated. 0 is the highest priority and 15, the lowest.

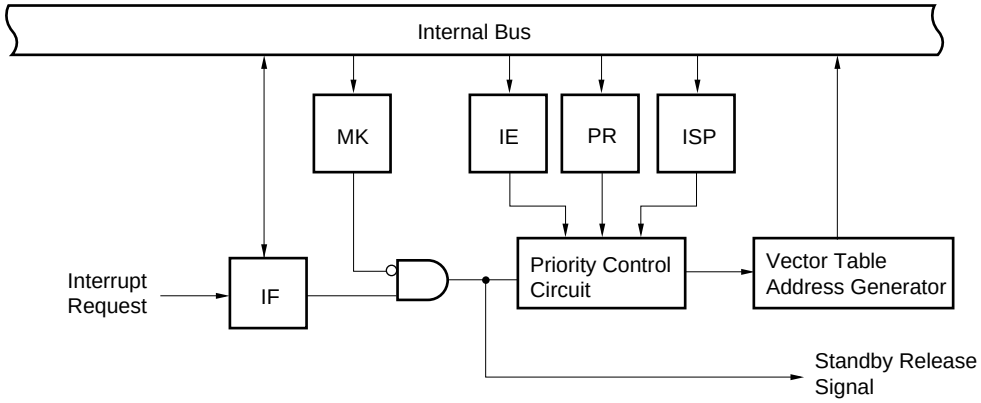
2. Basic configuration types (A) to (D) correspond to (A) to (D) on the next page.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External Maskable Interrupt

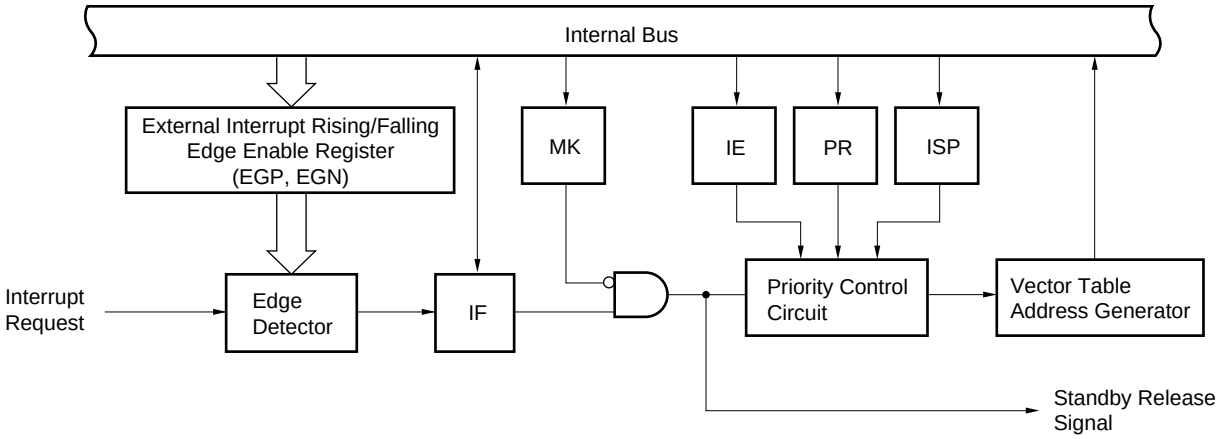
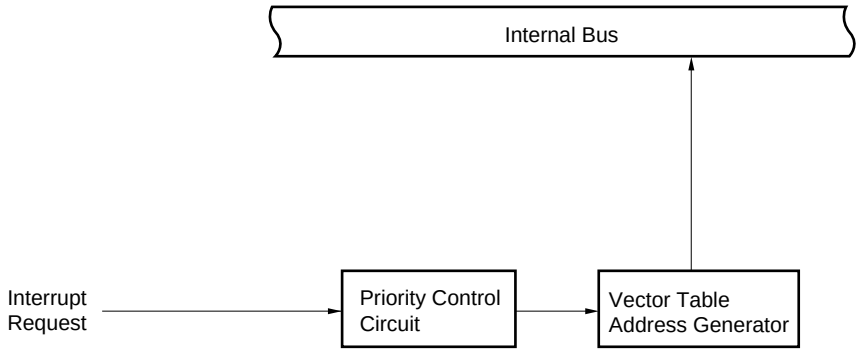


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) Software Interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTION

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

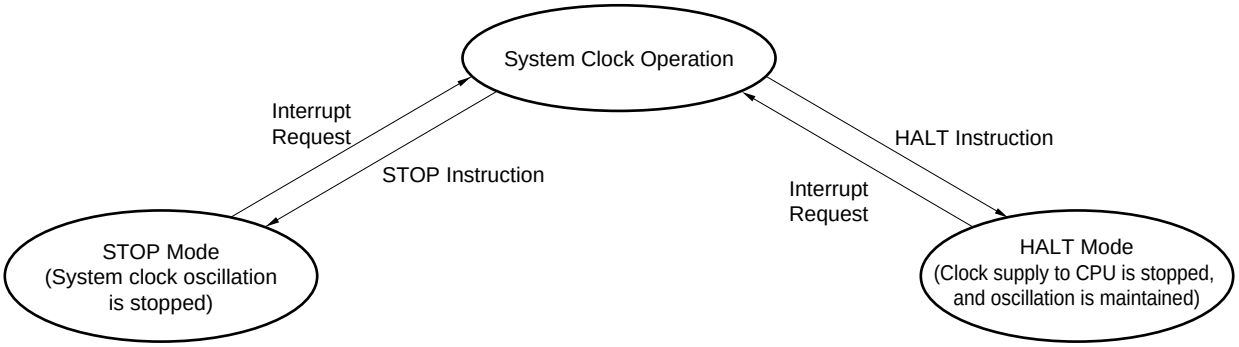
Ports 4 to 6 are used for connection with external devices.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current consumption.

- HALT mode : The CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The system clock oscillation is stopped. The whole operation by the system clock is stopped, so that the system operates with ultra-low power dissipation.

Figure 8-1. Standby Functions



9. RESET FUNCTIONS

There are the following two reset methods.

- External reset by $\overline{\text{RESET}}$ input.
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r=A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL.

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

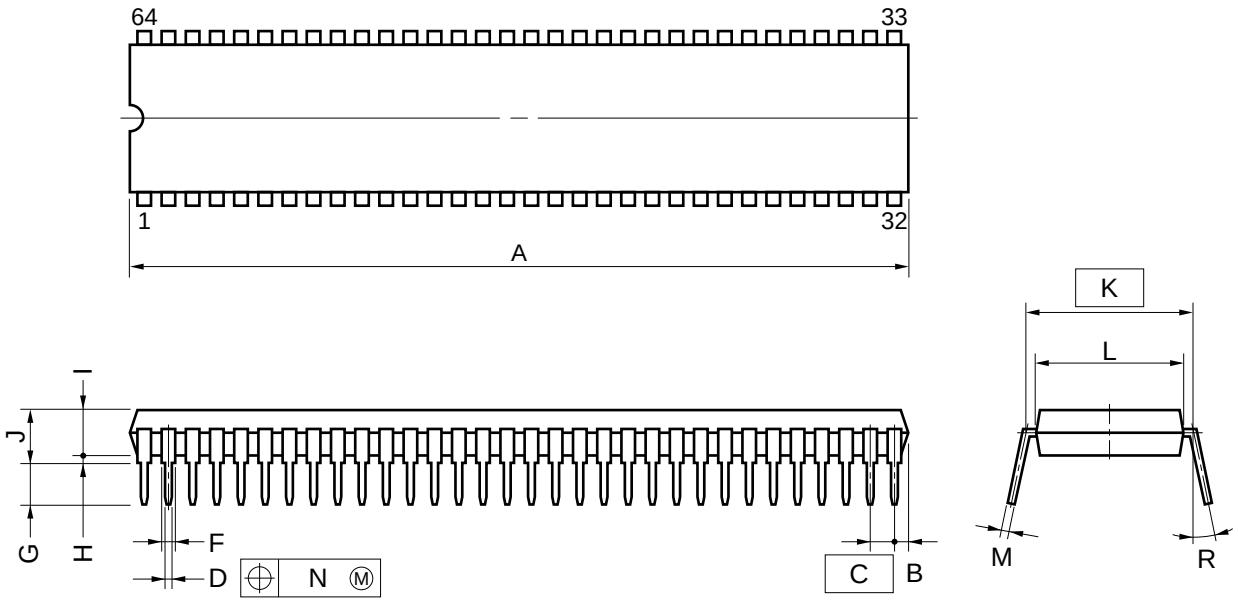
2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT,BF,BTCLR, DBNZ

(5) Other Instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



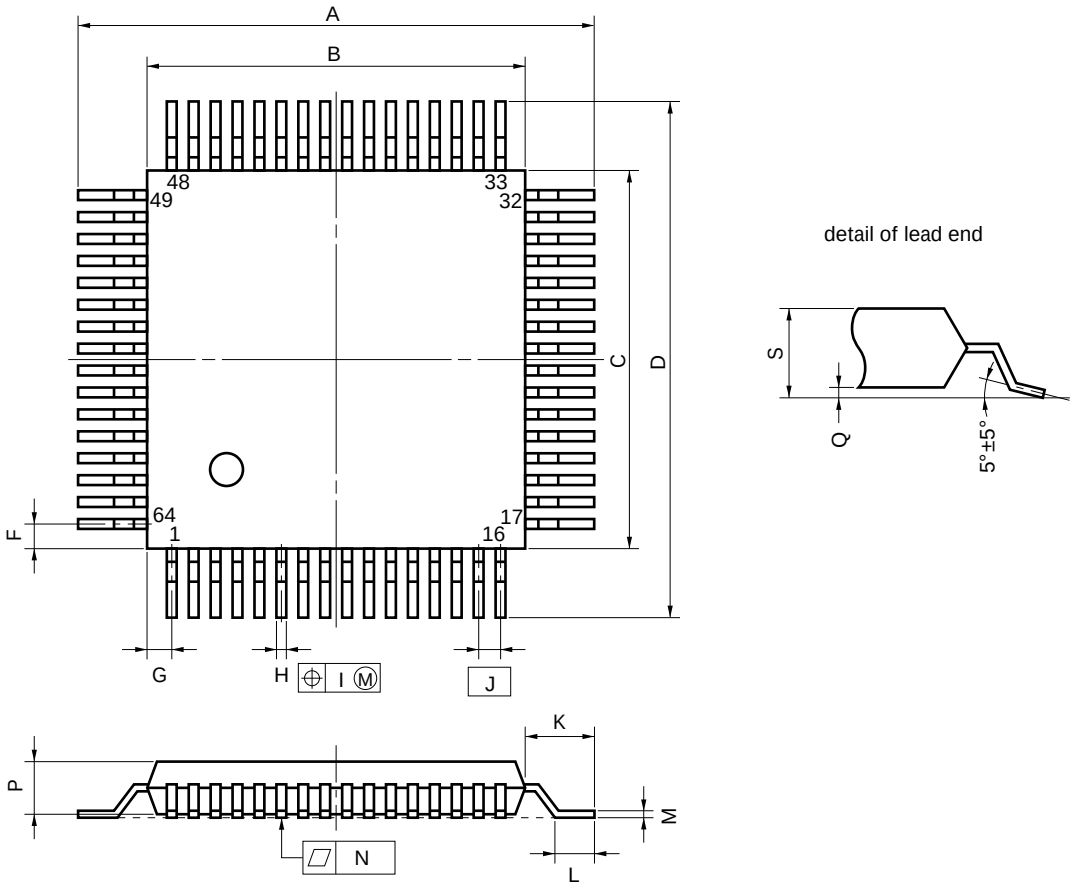
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)



P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780964 subseries.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 series common C compiler package
DF780964 Notes 1, 2, 3, 4, 8	μPD780964 subseries common device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 series common C compiler library source file

Flash Memory Writing Tools

Flashpro	Dedicated flash memory writer. The Flashpro is a product of Naito Densei Machida Mfg. Co., Ltd.
PA-FLASH64CW (temporary name) Note 8 PA-FLASH64GC (temporary name) Note 8	Adapter to write data to the flash memory The adapter for flash writing is a product of Naito Densei Machida Mfg. Co., Ltd.

Debugging Tools

IE-780000-SL (temporary name) Note 8	75XL, 78K/0S, 78K/0, and 78K/IV series common in-circuit emulator
IE-78K0-SL-EM (temporary name) Note 8	78K/0 series common CPU core board
IE-780964-SL-EM1 (temporary name) Note 8	Probe board to emulate μPD780964 subseries products
EP-64CW-SL (temporary name) Note 8	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-64GC-SL (temporary name) Note 8	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Socket to be mounted on target system board created for the 64-pin plastic QFP (GC-AB8 type)
SM78K0 Notes 5, 6, 7	78K/0 series common system simulator
ID78K0 Notes 4, 5, 6, 7	IE-780000-SL integrated debugger
DF780964 Notes 4, 5, 6, 7, 8	Device file common to μPD780964 subseries

Real-Time OSs

RX78K/0 Notes 1, 2, 3, 4	78K/0 series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 series OS

Fuzzy Inference Development Support Systems

FE9000 Note 1/FE9200 Note 6	Fuzzy knowledge data creation tool
FT9080 Note 1/FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Remark RA78K/0, CC78K/0, SM78K0, ID78K0, and RX78K/0 are used in combination with DF780964.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No.	
	English	Japanese
μPD780924, 780964 Subseries User's Manual	Planned	Planned
μPD780961, 780962, 780963, 780964 Preliminary Product Information	This manual	U11804J
μPD78F0964 Preliminary Product Information	Planned	Planned
μPD780924, 780964 Subseries Special Function Register Table	—	Planned
78K/0 Series User's Manual Instructions	IEU-1372	IEU-849
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J

Development Tool Documents (User's Manuals)

Document Name		Document No.	
		English	Japanese
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	EEU-817
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC 78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	EEU-777
IE-780000-SL		Planned	Planned
IE-78K0-SL-EM		Planned	Planned
IE-780964-SL-EM1		Planned	Planned
EP-64CW-SL		Planned	Planned
EP-64GC-SL		Planned	Planned
SM78K0 System Simulator Windows-based	Reference	U10181E	U10181J
SM78K Series System Simulator	External parts user open interface specification	U10092E	U10092J
ID78K0 Integrated Debugger EWS-based	Reference	U11151E	U11151J
ID78K0 Integrated Debugger PC-based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows-based	Guide	U11649E	U11649J

Caution The above related documents are subject to change without notice. Be sure to use the latest documents when starting design.

Embedded Software Documents (User's Manuals)

Document Name		Document No.	
		English	Japanese
78K/0 Series Real-Time OS	Basic	—	U11537J
	Installation	—	U11536J
	Technical	—	U11538J
78K/0 Series OS MX78K0	Basics	EEU-1532	EEU-5010
Fuzzy Knowledge Data Creation Tool		EEU-1438	EEU-829
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-1444	EEU-862
78K/0 Series Fuzzy Inference Development Suport System Fuzzy Inference Module		EEU-1441	EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-1458	EEU-921

Other Documents

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Electrostatic Discharge (ESD) Test	IEI-1201	MEM-539
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	MEI-603
Microcomputer Product Series Guide Other manufacturers	—	U11416J

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[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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