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RENESAS

MOS INTEGRATED CIRCUIT

μPD78052,78053,78054,78055,78056,78058

8-BIT SINGLE-CHIP MICROCONTROLLERS

Phase-out/Discontinued

DESCRIPTION

The μPD78052, 78053, 78054, 78055, 78056 and 78058 are μPD78054 Subseries products of the 78K/0 Series.

A variety of peripheral functions such as an 8-bit resolution A/D converter, 8-bit resolution D/A converter, timer, serial interface, real-time output port and interrupt functions are included on chip.

The μPD78P054 and 78P058, one-time PROM or EPROM products that can be operated in the same supply voltage range as the mask ROM versions, and various development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD78054, 78054Y Subseries User's Manual: U11747E
78K/0 Series User's Manual Instructions: U12326E

FEATURES

- High-capacity on-chip ROM & RAM

Item / Part Number	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	Internal Buffer RAM	Internal Expansion RAM	
μPD78052	16 KB	512 bytes	32 bytes	None	• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78053	24 KB	1024 bytes			
μPD78054	32 KB				
μPD78055	40 KB				
μPD78056	48 KB				
μPD78058	60 KB			1024 bytes	

- External memory expansion space: 64 KB
- Minimum instruction execution time can be changed from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 69 (N-ch open drain: 4)
- 8-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- Serial interface: 3 channels
- Timer: 5 channels
- Supply voltage: V_{DD} = 2.0 to 6.0 V

APPLICATIONS

Cellular phones, pagers, printers, AV equipment, air-conditioners, cameras, PPCs, fuzzy-logic home appliances, vending machines, etc.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. U12327EJ5V0DS00 (5th edition)
Date Published February 2000 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

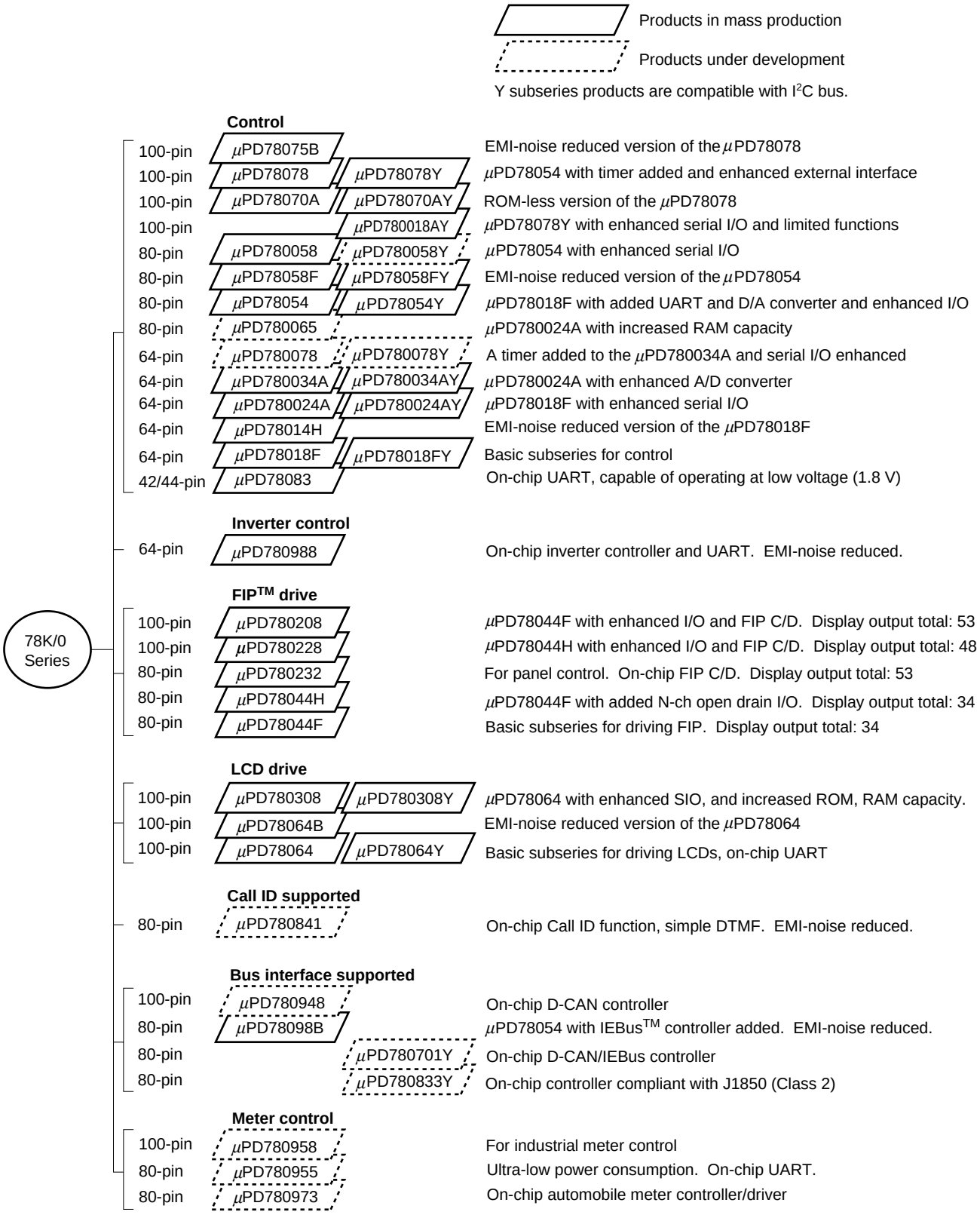
ORDERING INFORMATION

Part Number	Package
μPD78052GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD78052GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78053GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD78053GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78054GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD78054GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78055GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD78055GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78056GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD78056GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78058GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD78058GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Remark ××× indicates ROM code suffix.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32K to 40K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48K to 60K											
	μPD78070A	—									61	2.7 V	
	μPD780058	24K to 60K	2 ch							3 ch (time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48K to 60K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16K to 60K										2.0 V	
	μPD780065	40K to 48K							—	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48K to 60K		2 ch			—	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8K to 32K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	—					
	μPD78014H									2 ch	53		
	μPD78018F	8K to 60K											
	μPD78083	8K to 16K		—	—					1 ch (UART: 1 ch)	33		—
Inverter control	μPD780988	16K to 60K	3 ch	**Note**	—	1 ch	—	8 ch	—	3 ch (UART: 2 ch)	47	4.0 V	√
FIP drive	μPD780208	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780228	48K to 60K	3 ch	—	—					1 ch	72	4.5 V	
	μPD780232	16K to 24K					4 ch			2 ch	40		
	μPD78044H	32K to 48K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16K to 40K								2 ch			
LCD drive	μPD780308	48K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (time division UART: 1 ch)	57	2.0 V	—
	μPD78064B	32K								2 ch (UART: 1 ch)			
	μPD78064	16K to 32K											
Call ID supported	μPD780841	24K to 32K	2 ch	—	1 ch	1 ch	2 ch	—	—	2 ch (UART: 1 ch)	61	2.7 V	—
Bus interface supported	μPD780948	60K	2 ch	2 ch	1 ch	1 ch	8 ch	—	—	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40K to 60K		1 ch					2 ch		69	2.7 V	—
Meter control	μPD780958	48K to 60K	4 ch	2 ch	—	1 ch	—	—	—	2 ch (UART: 1 ch)	69	2.2 V	—
	μPD780955	40K	6 ch	1 ch			1 ch			2 ch (UART: 2 ch)	50	2.2 V	
	μPD780973	24K to 32K	3 ch		1 ch		5 ch			2 ch (UART: 1 ch)	56	4.5 V	

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

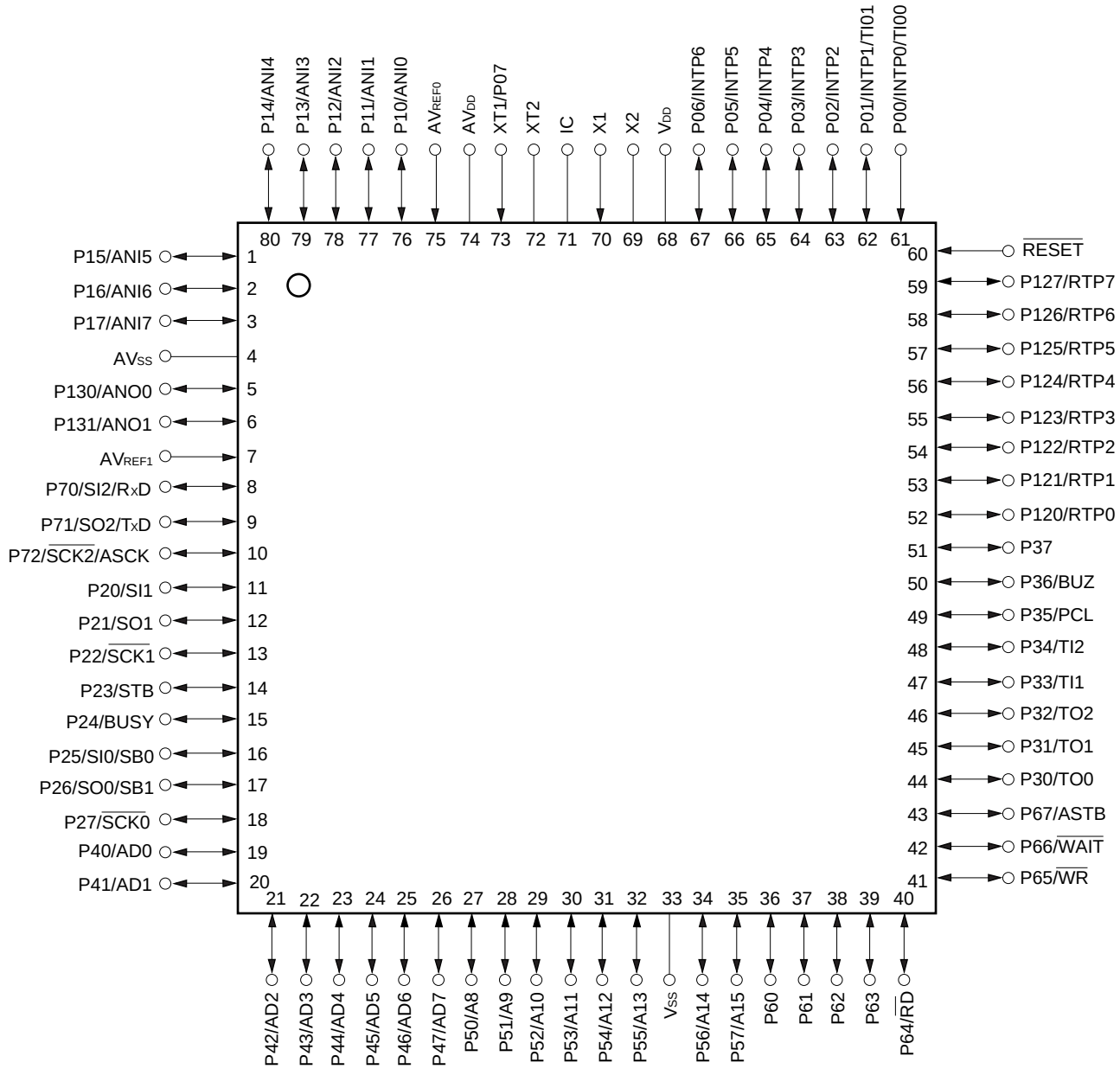
OVERVIEW OF FUNCTIONS

Item \ Part Number		μPD78052	μPD78053	μPD78054	μPD78055	μPD78056	μPD78058
Internal Memory	ROM	16 KB	24 KB	32 KB	40 KB	48 KB	60 KB
	High-speed RAM	512 bytes	1024 bytes				
	Buffer RAM	32 bytes					
	Expansion RAM	None					1024 bytes
Memory space		64 KB					
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)					
Minimum instruction execution time		On-chip minimum instruction execution time variable function					
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz operation)					
	When subsystem clock is selected	122 μs (@ 32.768 kHz operation)					
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD correction, etc.					
I/O ports		Total: 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O: 4					
A/D converter		• 8-bit resolution × 8 channels					
D/A converter		• 8-bit resolution × 2 channels					
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel • 3-wire serial I/O mode (automatic data transmit/receive function for up to 32 bytes provided on chip): 1 channel • 3-wire serial I/O/UART mode selectable: 1 channel					
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel					
Timer outputs		3 (14-bit PWM output × 1)					
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (@ 5.0 MHz operation with main system clock) 32.768 kHz (@ 32.768 kHz operation with subsystem clock)					
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (@ 5.0 MHz operation with main system clock)					
Vectored interrupt sources	Maskable	Internal: 13, external: 7					
	Non-maskable	Internal: 1					
	Software	1					
Test inputs		Internal: 1, external: 1					
Supply voltage		V_{DD} = 2.0 to 6.0 V					
Operating ambient temperature		T_A = –40 to +85°C					
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)					

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD78052GC-×××-8BT, 78053GC-×××-8BT, 78054GC-×××-8BT, 78055GC-×××-8BT,
  μPD78056GC-×××-8BT, 78058GC-×××-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
  μPD78052GK-×××-BE9, 78053GK-×××-BE9, 78054GK-×××-BE9, 78055GK-×××-BE9,
  μPD78056GK-×××-BE9, 78058GK-×××-BE9



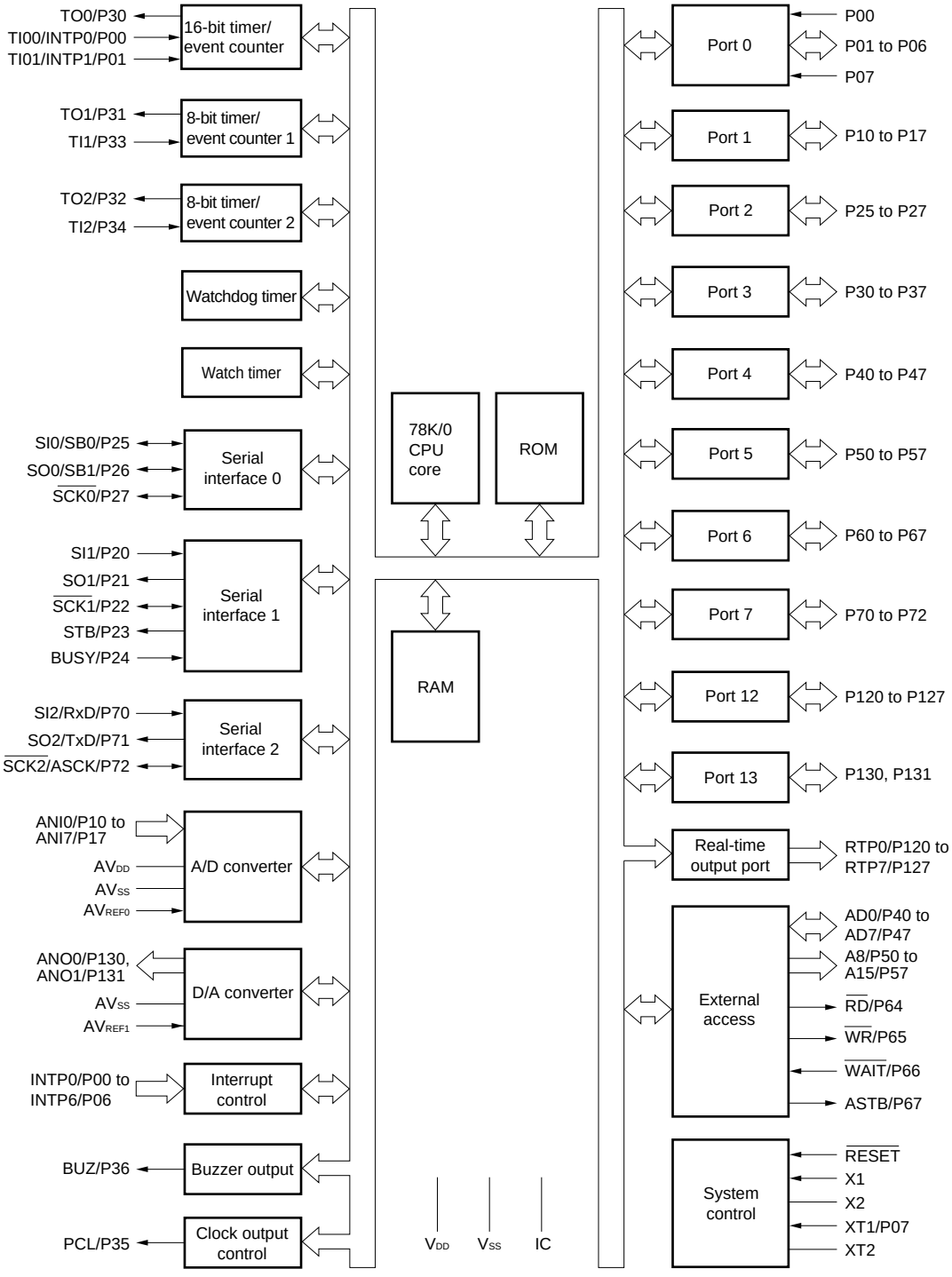
Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

A8 to A15:	Address Bus
AD0 to AD7:	Address/Data Bus
ANI0 to ANI7:	Analog Input
ANO0, ANO1:	Analog Output
ASCK:	Asynchronous Serial Clock
ASTB:	Address Strobe
AV_{DD}:	Analog Power Supply
AV_{REF0}, AV_{REF1}:	Analog Reference Voltage
AV_{SS}:	Analog Ground
BUSY:	Busy
BUZ:	Buzzer Clock
IC:	Internally Connected
INTP0 to INTP6:	External Interrupt Input
P00 to P07:	Port0
P10 to P17:	Port1
P20 to P27:	Port2
P30 to P37:	Port3
P40 to P47:	Port4
P50 to P57:	Port5
P60 to P67:	Port6
P70 to P72:	Port7
P120 to P127:	Port12
P130, P131:	Port13
PCL:	Programmable Clock
$\overline{RD}$:	Read Strobe
$\overline{RESET}$:	Reset
RTP0 to RTP7:	Real-Time Output Port
$\overline{RxD}$:	Receive Data
$\overline{SB0}$, $\overline{SB1}$:	Serial Bus
SCK0 to SCK2:	Serial Clock
SI0 to SI2:	Serial Input
SO0 to SO2:	Serial Output
STB:	Strobe
TI00, TI01:	Timer Input
TI1, TI2:	Timer Input
TO0 to TO2:	Timer Output
TxD:	Transmit Data
V_{DD}:	Power Supply
$\overline{V_{SS}}$:	Ground
$\overline{WAIT}$:	Wait
$\overline{WR}$:	Write Strobe
X1, X2:	Crystal (Main System Clock)
XT1, XT2:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 8-bit I/O port	Input only	Input	INTP0/TI00
P01	I/O		Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	I/O	Port 1 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software[Note 2].		Input	ANI0 to ANI7
P20	I/O	Port 2 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	I/O	Port 3 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	I/O	Port 4 8-bit I/O port. Input/output can be specified in 8-bit units. When used as an input port, a pull-up resistor can be specified by means of software. The test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P07/XT1 pin as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1. Do not use the on-chip feedback resistor of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as A/D converter analog input pins, set port 1 to the input mode. At this time, pull-up resistors are automatically disconnected.

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P50 to P57	I/O	Port 5 8-bit I/O port. LEDs can be driven directly. Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software.		Input	A8 to A15
P60	I/O	Port 6 8-bit I/O port. Input/output can be specified in 1-bit units.	N-ch open-drain I/O port. An on-chip pull-up resistor can be specified by the mask option. LEDs can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, a pull-up resistor can be specified by means of software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	I/O	Port 7 3-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120 to P127	I/O	Port 12 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software.		Input	RTP0 to RTP7
P130, P131	I/O	Port 13 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, a pull-up resistor can be specified by means of software.		Input	ANO0, ANO1

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial interface serial data input/output	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial interface serial clock input/output	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
RxD	Input	Asynchronous serial interface serial data input	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1)		P33
TI2		External count clock input to the 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP7	Output	Real-time output port from which data is output in synchronization with a trigger	Input	P120 to P127
AD0 to AD7	I/O	Lower address/data bus for expanding memory externally	Input	P40 to P47
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{WR}$		Strobe signal output for writing to external memory		P65

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input	—	—
AV_{REF1}	Input	D/A converter reference voltage input	—	—
AV_{DD}	—	A/D converter analog power supply. Connect to V_{DD}.	—	—
AV_{SS}	—	Ground potential of A/D converter and D/A converter. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{SS}	—	Ground potential	—	—
IC	—	Internally connected. Connect directly to V_{SS}.	—	—

★ 3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Types of Pin Input/Output Circuits (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0/TI00	2	Input	Connect to V_{SS} .
P01/INTP1/TI01	8-A	I/O	Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD}.
P10/ANI0 to P17/ANI7	11	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Input: Independently connect to V_{DD} via a resistor. Output: Leave open.
P50/A8 to P57/A15	5-A		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P60 to P63	13-B		Input: Independently connect to V_{DD} via a resistor. Output: Leave open.
P64/$\overline{RD}$	5-A		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 3-1. Types of Pin Input/Output Circuits (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P70/SI2/RxD	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0 to P127/RTP7	5-A	I/O	
P130/ANO0, P131/ANO1	12-A	I/O	Input: Independently connect to V_{SS} via a resistor. Output: Leave open[Note].
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
IC			Connect directly to V_{SS}.

Note Output a low level.

Figure 3-1. Pin Input/Output Circuits (1/2)

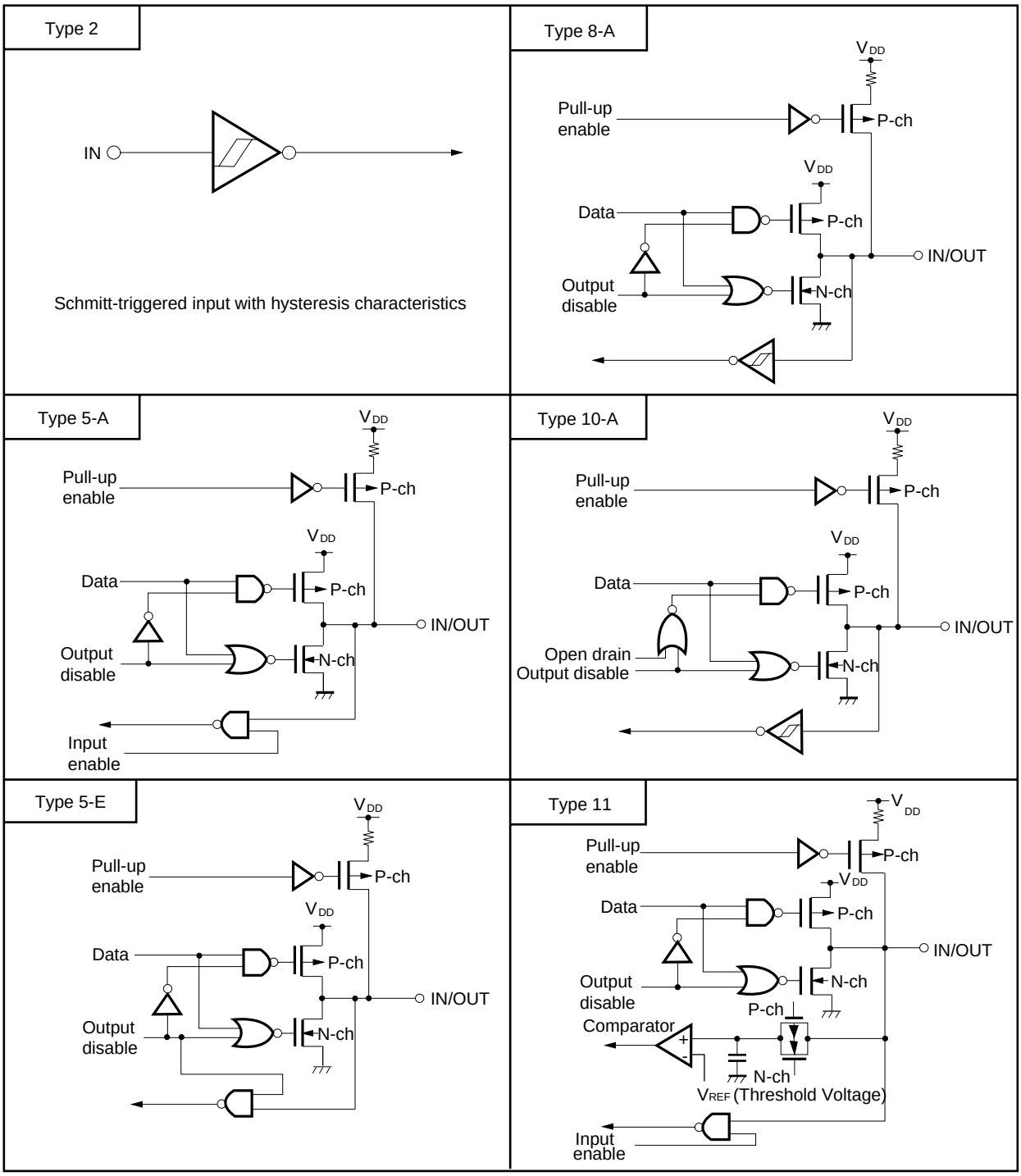
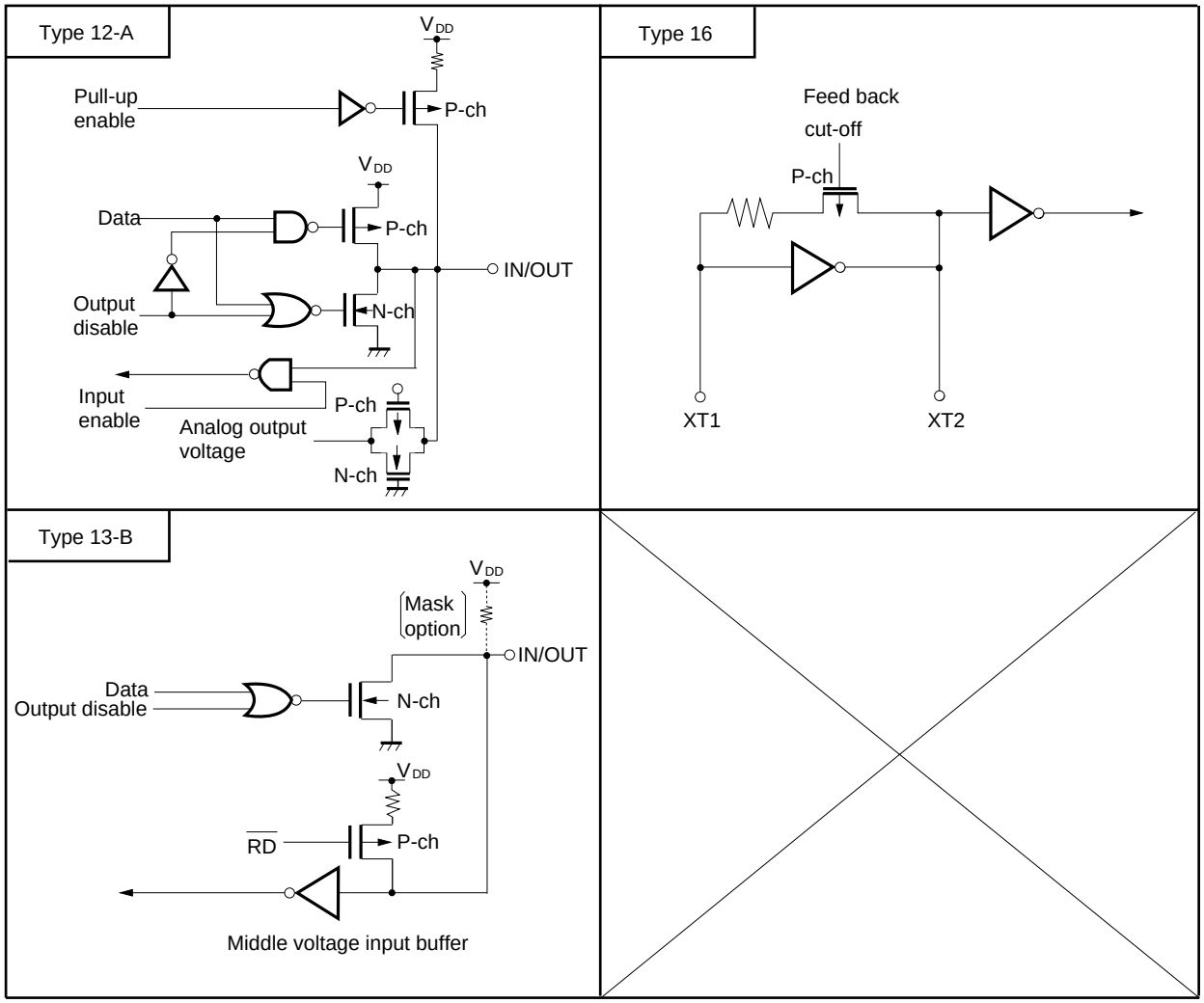


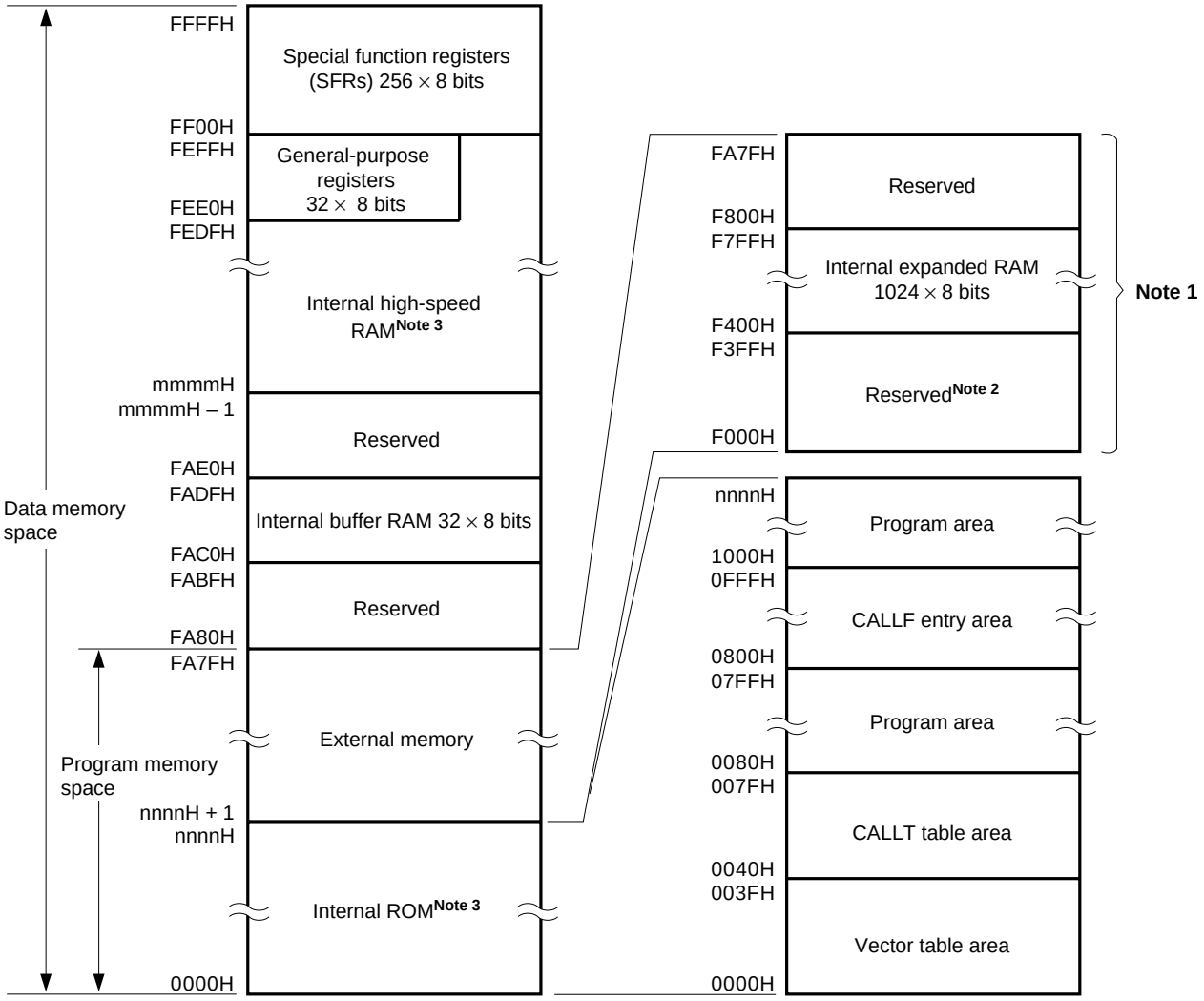
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the μPD78052/78053/78054/78055/78056/78058 memory map.

Figure 4-1. Memory Map



Notes 1. μPD78058 only

2. If external device expansion functions are to be employed for the μPD78058, set the size of internal ROM to 56 KB or below using the memory size switching register (IMS).

3. The internal ROM capacity and internal high-speed RAM capacity differ depending on the product (see the following table).

Part Number	Last Address of Internal ROM nnnnH	First Address of Internal High-Speed RAM mmmmH
μPD78052	3FFFH	FD00H
μPD78053	5FFFH	FB00H
μPD78054	7FFFH	
μPD78055	9FFFH	
μPD78056	BFFFH	
μPD78058	EFFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following three types of I/O ports are available.

- CMOS input (P00, P07): 2
- CMOS I/O (P01 to P06, port 1 to port 5, P64 to P67, port 7, port 12, port 13): 63
- N-ch open-drain I/O (P60 to P63): 4

Total: 69

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00, P07	Input-only
	P01 to P06	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 1	P10 to P17	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 3	P30 to P37	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 4	P40 to P47	I/O port. Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. The test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.
Port 6	P60 to P63	N-ch open-drain I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by the mask option. LEDs can be driven directly.
	P64 to P67	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 7	P70 to P72	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 12	P120 to P127	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 13	P130, P131	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.

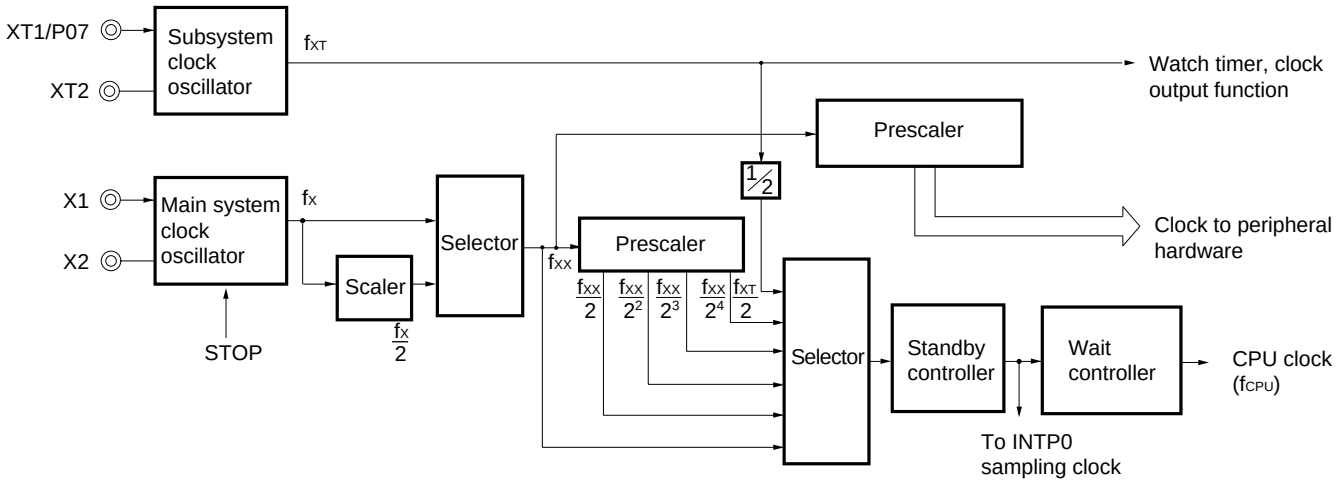
5.2 Clock Generator

Two types of generators, a main system clock generator and a subsystem clock generator, are available.

The minimum instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0 MHz operation with main system clock)
- 122 μs (@32.768 kHz operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

The μPD78052/78053/78054/78055/78056/78058 incorporate a 5-channel timer/event counter.

- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 2 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Operation of Timer/Event Counter

	16-Bit Timer/Event Counter	8-Bit Timer/Event Counter	Watch Timer	Watchdog Timer
Operation mode				
Interval timer	1 channel	2 channels	1 channel	1 channel
External event counter	1 channel	2 channels	—	—
Function				
Timer output	1 output	2 outputs	—	—
PWM output	1 output	—	—	—
Pulse amplitude measurement	2 inputs			
Square wave output	1 output	2 outputs	—	—
One-shot pulse output	1 output	—	—	—
Interrupt source	2	2	1	1
Test input	—	—	1 input	—

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter

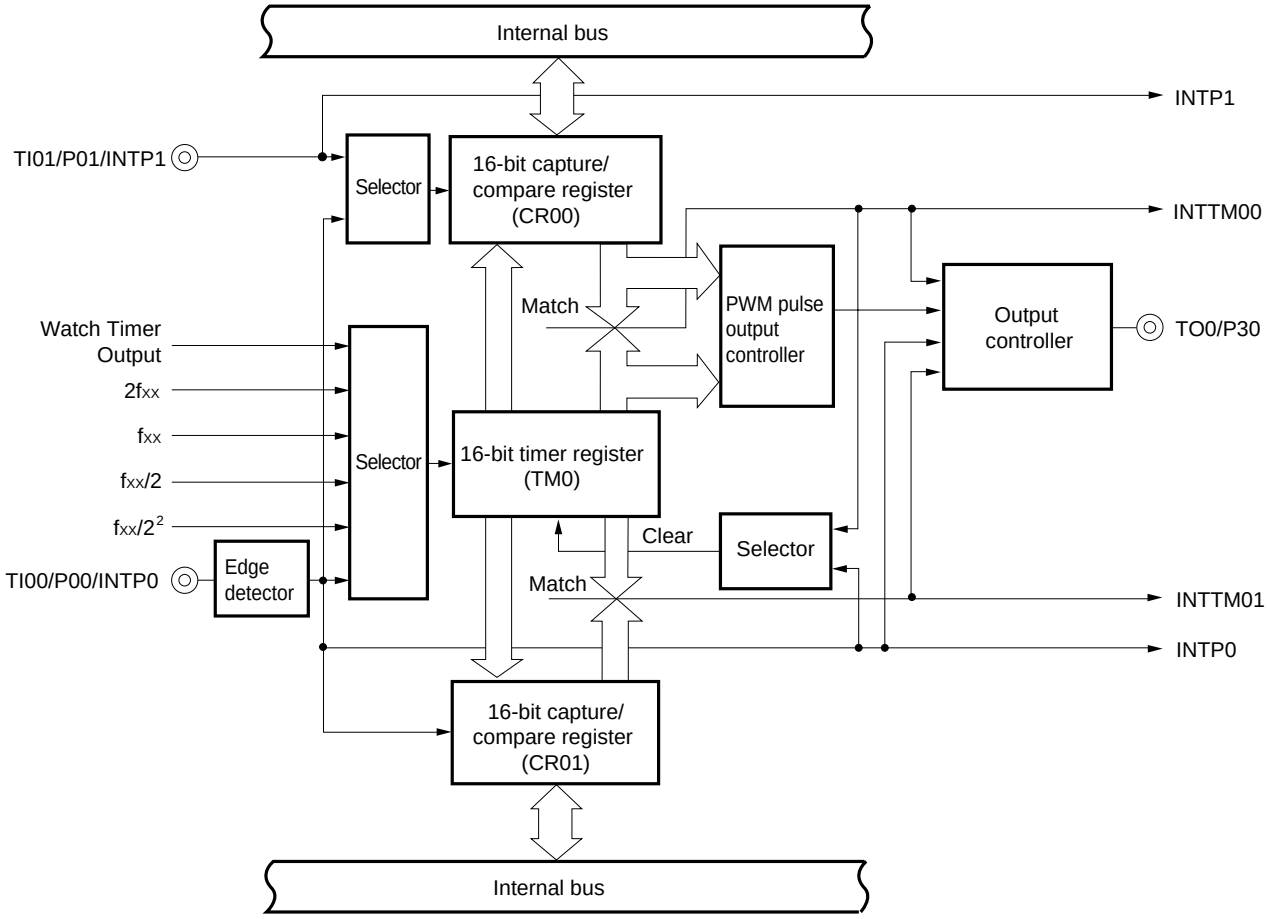


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter

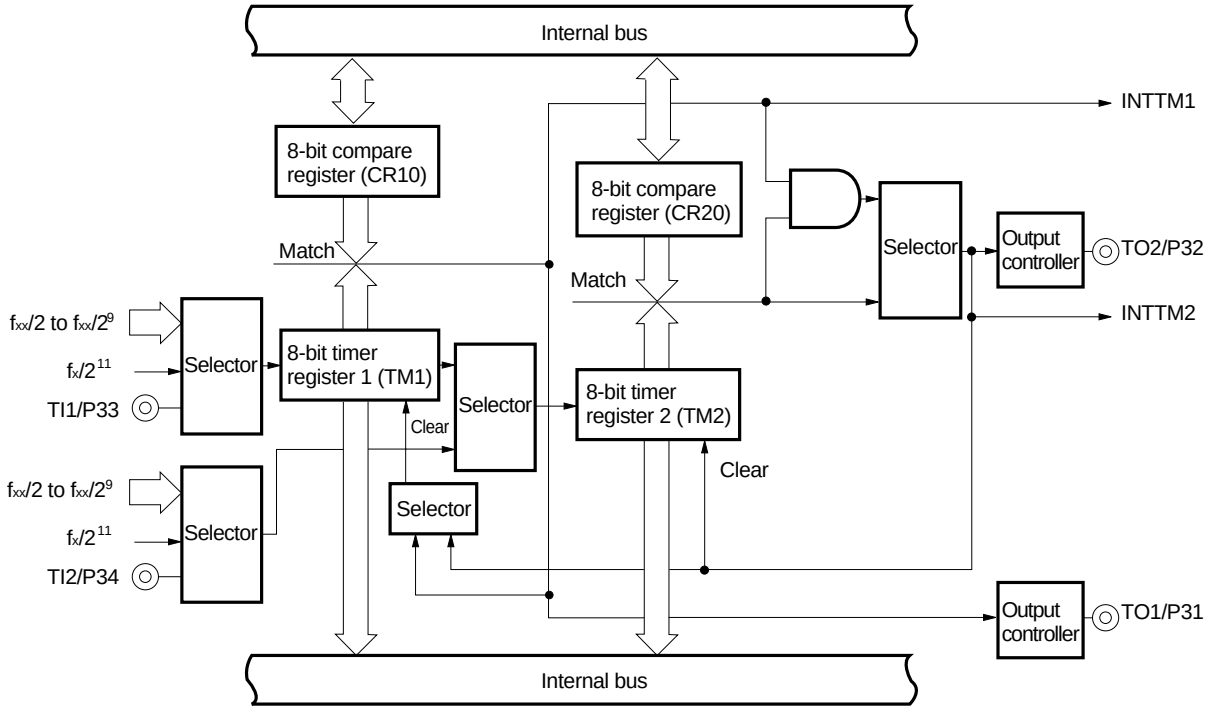


Figure 5-4. Watch Timer Block Diagram

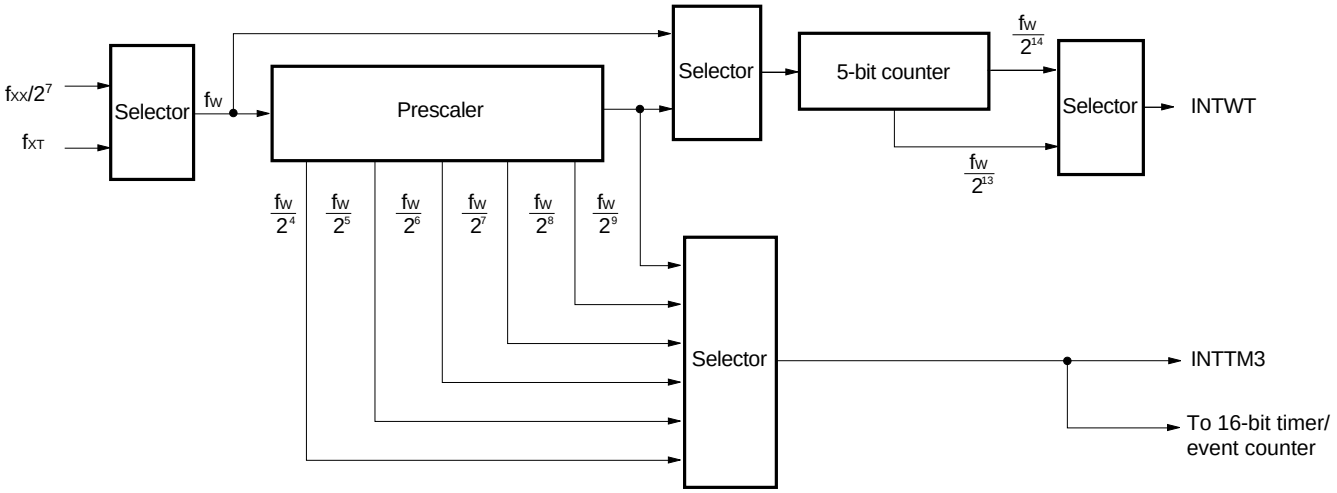
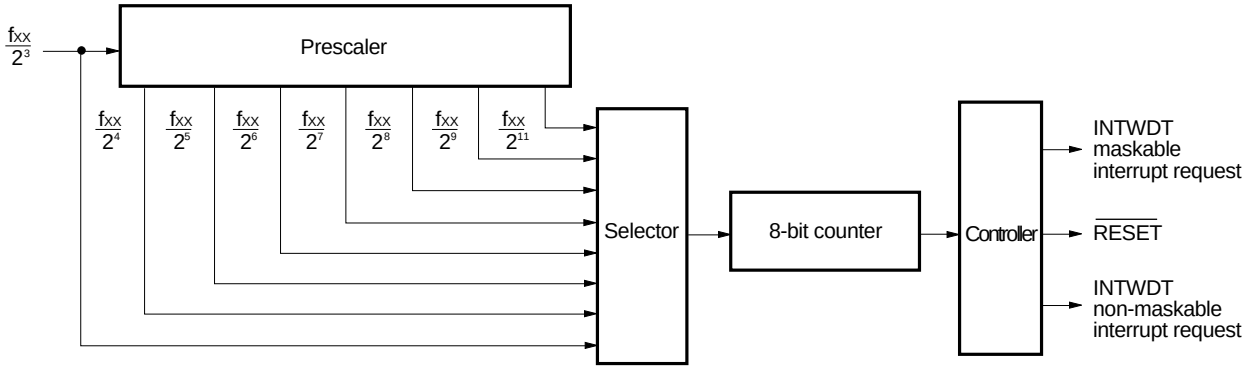


Figure 5-5. Watchdog Timer Block Diagram

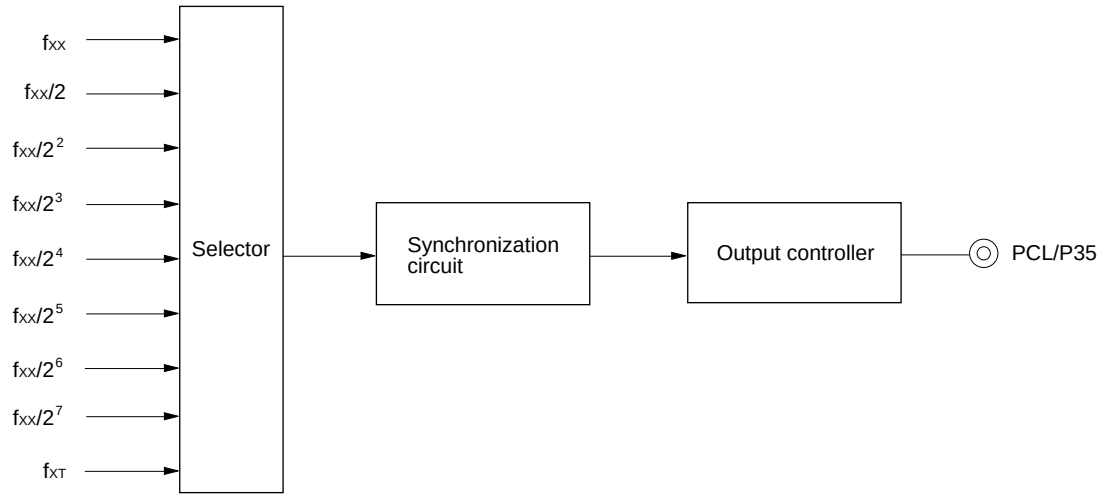


5.4 Clock Output Controller

Clocks with the following frequencies can be output as clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (@5.0 MHz operation with main system clock)
- 32.768 kHz (@32.768 kHz operation with subsystem clock)

Figure 5-6. Block Diagram of Clock Output Controller

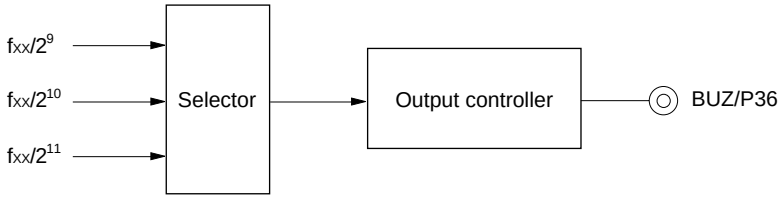


5.5 Buzzer Output Controller

Clocks with the following frequencies can be output as buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (@5.0 MHz operation with main system clock)

Figure 5-7. Block Diagram of Buzzer Output Controller



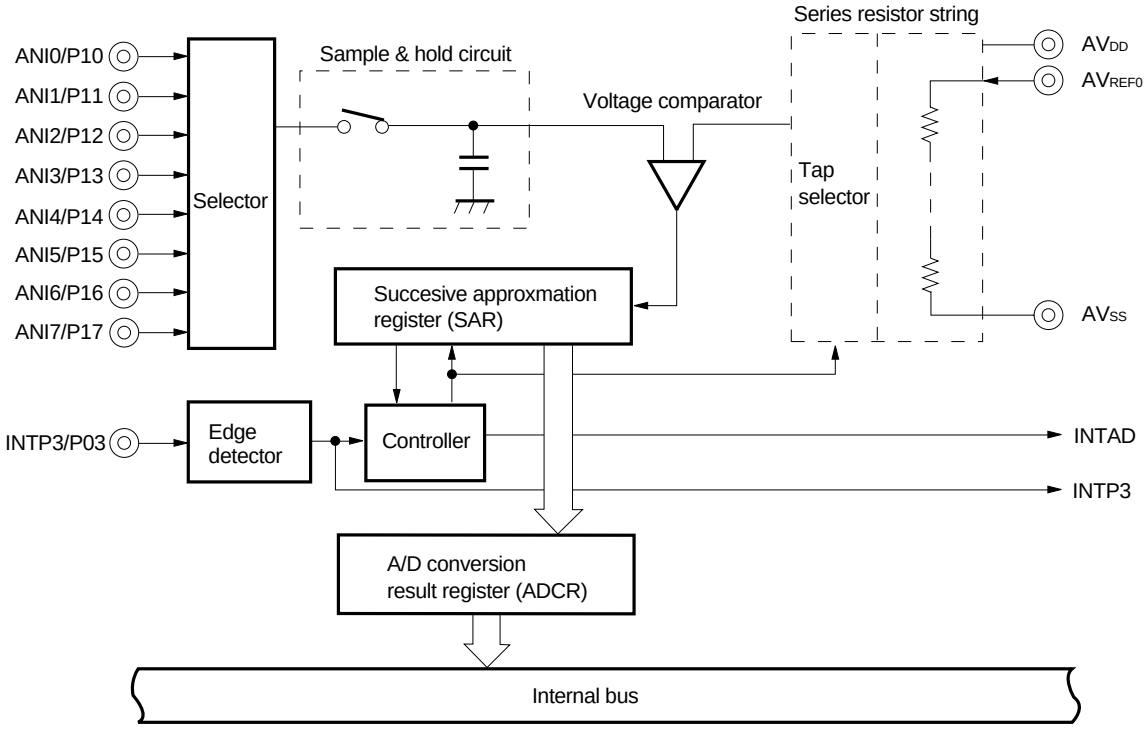
5.6 A/D Converter

An A/D converter consisting of eight 8-bit resolution channels is incorporated.

The following two A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram

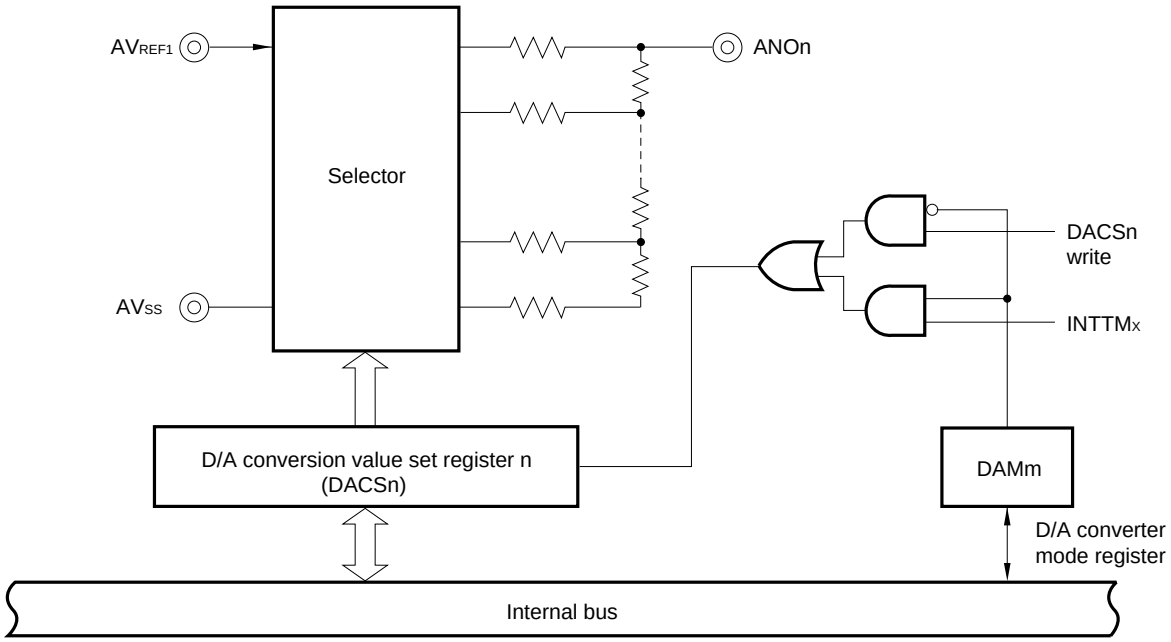


5.7 D/A Converter

A D/A converter consisting of two 8-bit resolution channels is available.

The conversion method is the R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1

m = 4, 5

x = 1, 2

5.8 Serial Interface

Three clocked serial interface channels are incorporated.

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	○(MSB/LSB first switching possible)	○ (MSB/LSB first switching possible)	○(MSB/LSB first switching possible)
3-wire serial I/O mode with automatic transmit/receive function	—	○ (MSB/LSB first switching possible)	—
SBI (serial bus interface) mode	○ (MSB first)	—	—
2-wire serial I/O mode	○ (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	○(On-chip dedicated baud rate generator)

Figure 5-10. Block Diagram of Serial Interface Channel 0

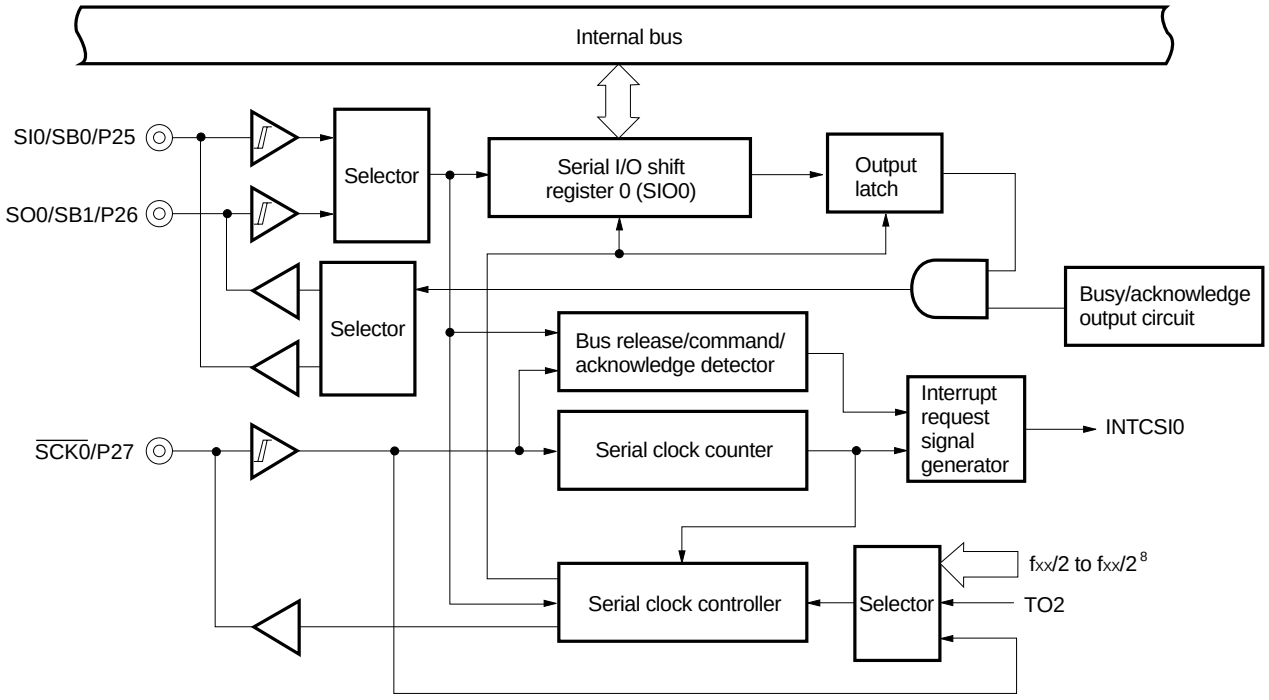


Figure 5-11. Block Diagram of Serial Interface Channel 1

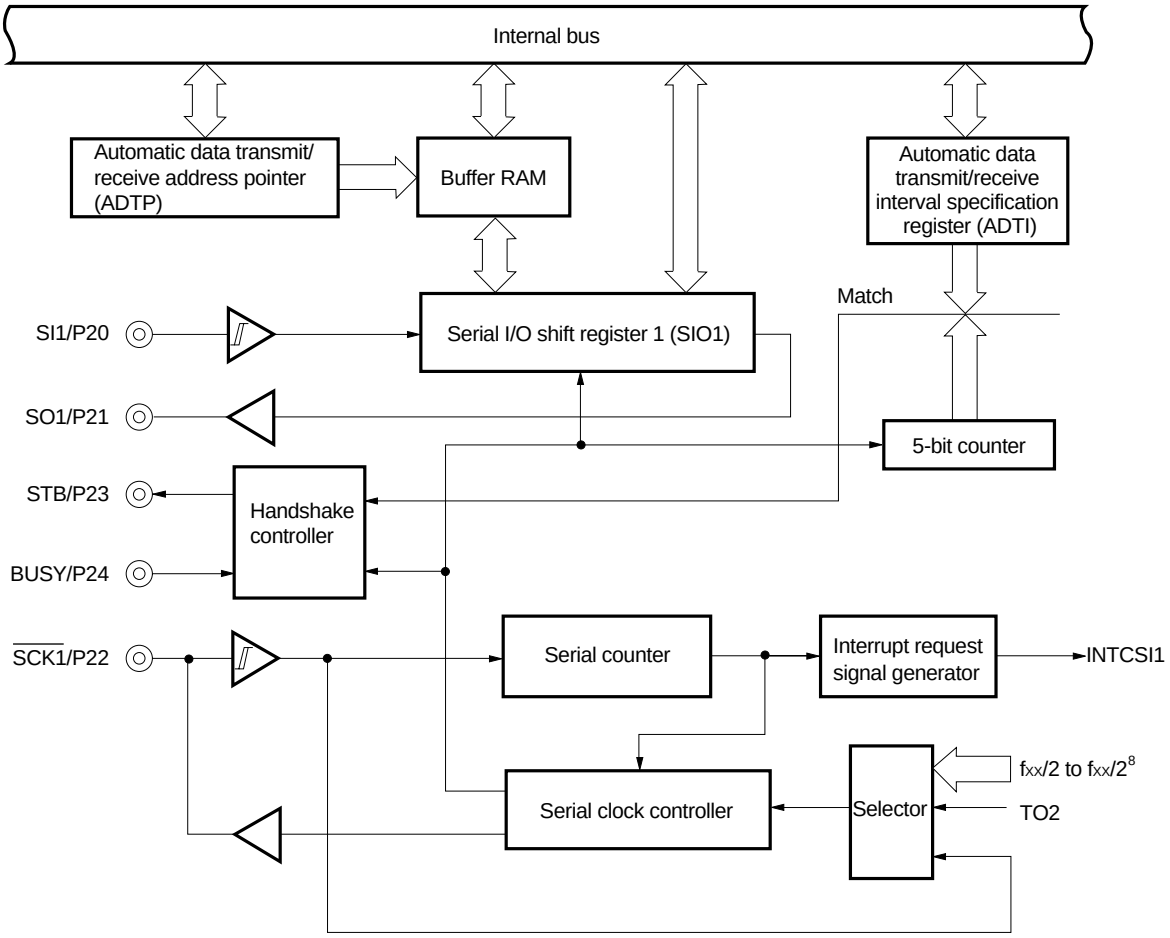
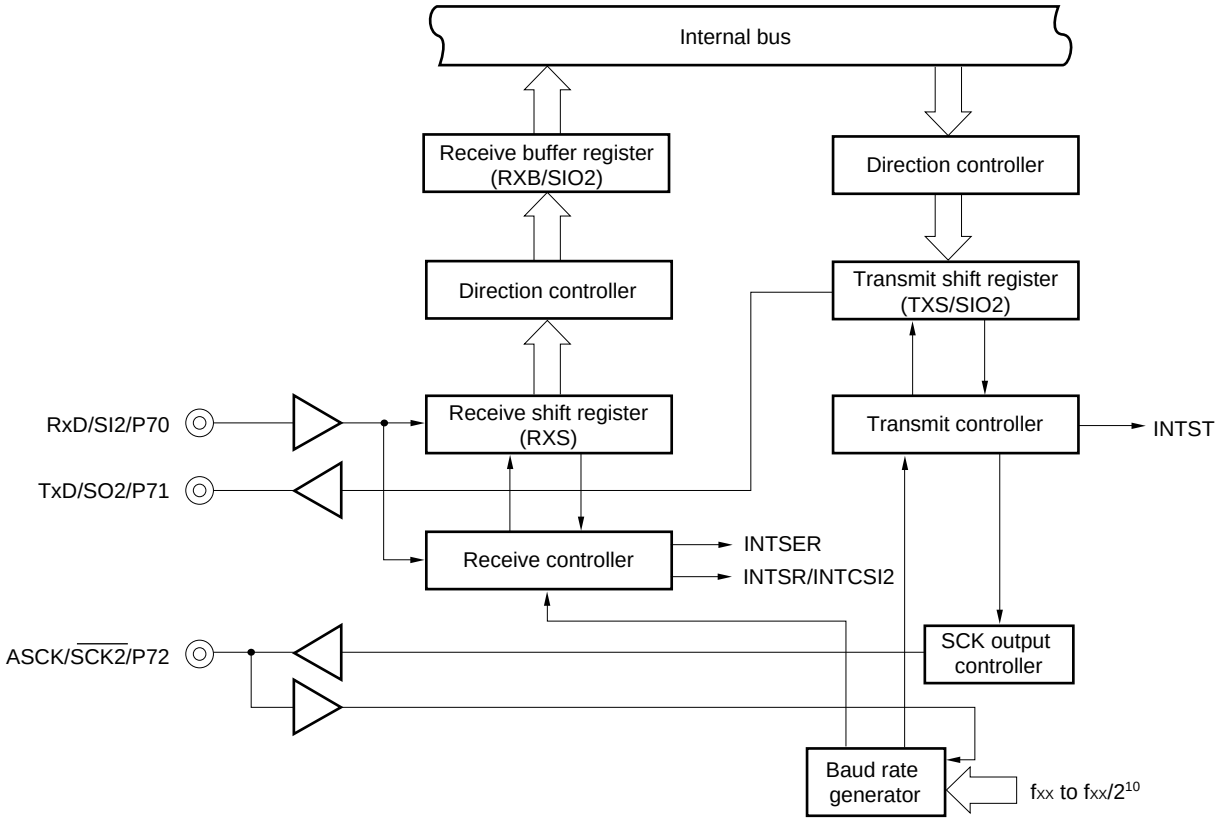


Figure 5-12. Block Diagram of Serial Interface Channel 2

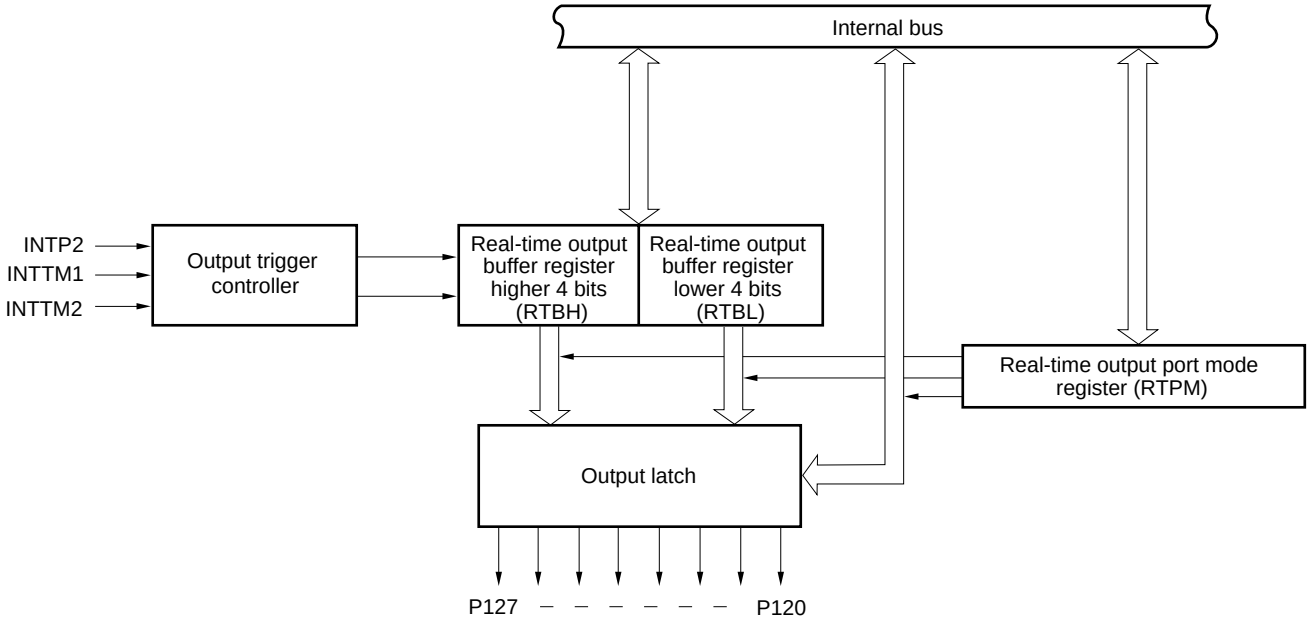


5.9 Real-Time Output Port

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt or external interrupt generation in order to output off-chip. This is a real-time output function. Pins used to output off-chip are called real-time output ports.

By using a real-time output port, a signal with no jitter can be output. This is most applicable to control of stepper motors, etc.

Figure 5-13. Block Diagram of Real-Time Output Port



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

A total of 22 interrupt sources are provided, divided into the following three types.

- Non-maskable: 1
- Maskable: 20
- Software: 1

The following table shows the interrupt source list.

Table 6-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	End of serial interface channel 1 transfer		0016H	
	10	INTSER	Occurrence of serial interface channel 2 UART reception error		0018H	
	11	INTSR	End of serial interface channel 2 UART reception		001AH	
		INTCSI2	End of serial interface channel 2 3-wire transfer			
	12	INTST	End of serial interface channel 2 UART transmission		001CH	

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 18 is the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Table 6-1. Interrupt Source List (2/2)

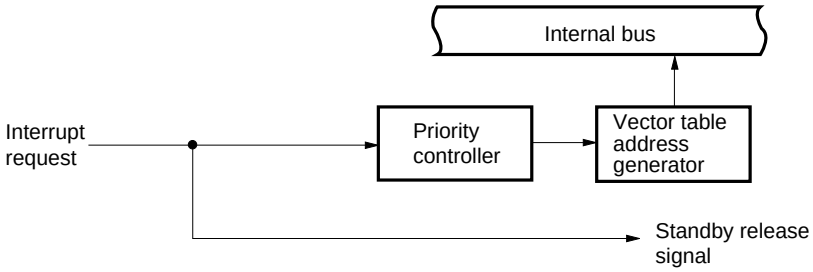
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	13	INTTM3	Reference time interval signal from watch timer	Internal	001EH	(B)
	14	INTTM00	Generation of match signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of match signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of match signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of match signal of 8-bit timer/event counter 2		0026H	
	18	INTAD	End of A/D conversion		0028H	
Software	—	BRK	BRK instruction execution	—	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 18 is the lowest.

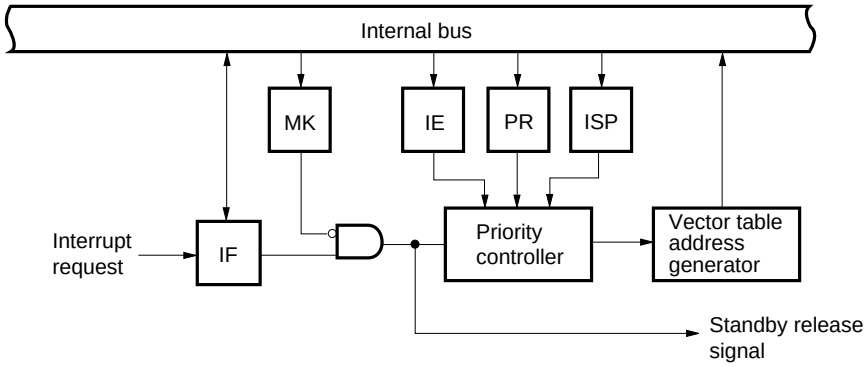
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

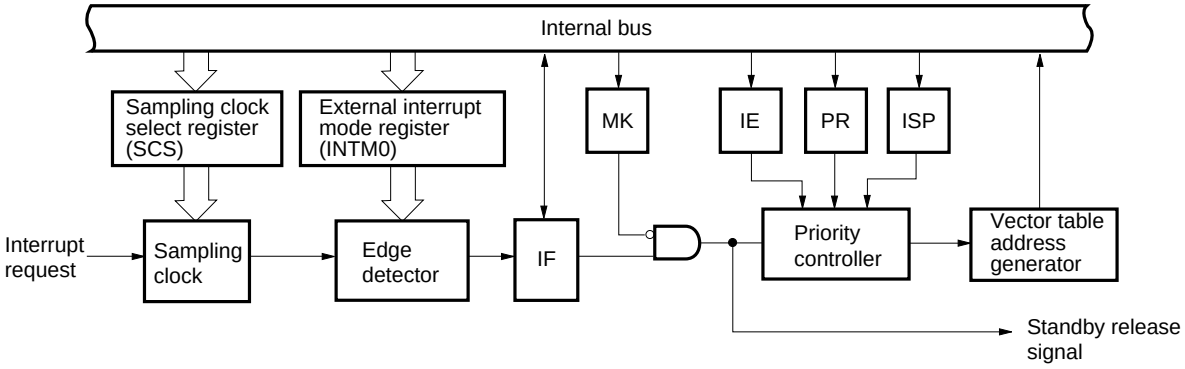
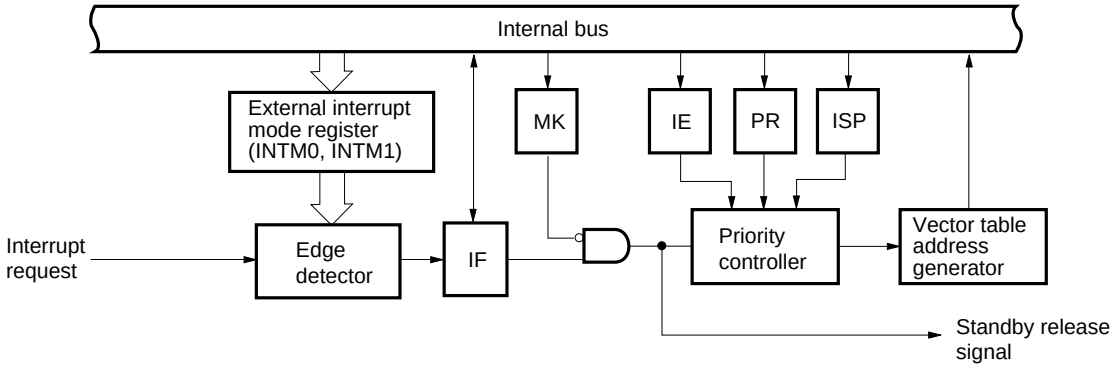
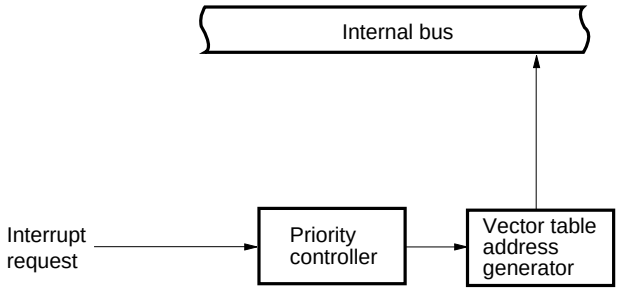


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

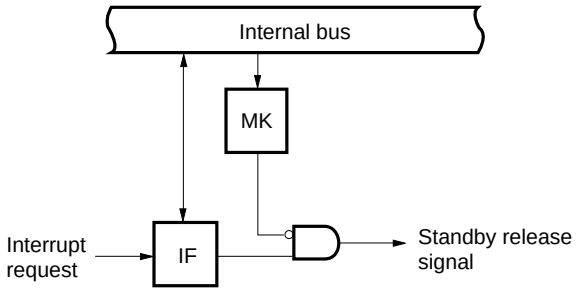
6.2 Test Functions

Table 6-2 shows the two test functions available.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Basic Configuration of Test Function



IF: Test input flag

MK: Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTION

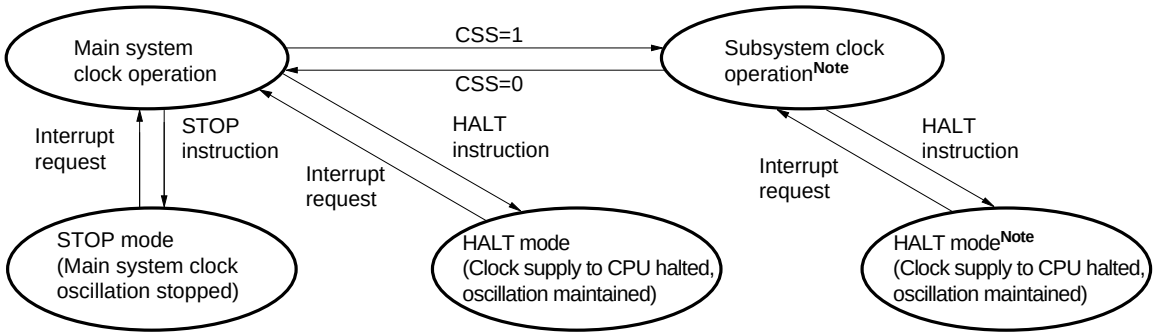
The external device expansion function is for the connection of external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operating clock is stopped.
  The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used, resulting in extremely small power consumption.

Figure 8-1. Standby Function



Note The current consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

9. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + Byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + Byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOV, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

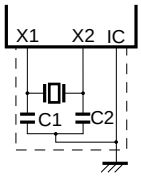
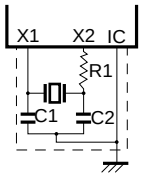
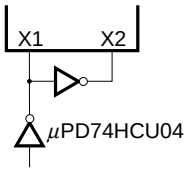
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch open drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P127		–15	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131		–15	mA
Output current, low	I_{OL}**Note**	Per pin	Peak value	30	mA
			rms value	15	mA
		Total for P50 to P55	Peak value	100	mA
			rms value	70	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			rms value	70	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131	Peak value	50	mA
			rms value	20	mA
		Total for P01 to P06, P30 to P37, P64 to P67, P120 to P127	Peak value	50	mA
			rms value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

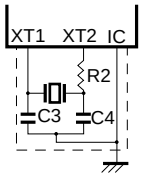
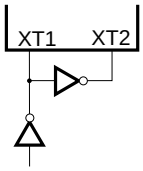
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

(1) μPD78052, 78053, 78054, 78055, 78056

Main system clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSA5.00MG	5.00	30	30	2.0	6.0	
	CST5.00MGW	5.00	On-chip	On-chip	2.0	6.0	On-chip capacitor
Kyocera Corp.	KBR-5.0MSA	5.00	33	33	2.0	6.0	Lead type
	KBR-5.0MKS	5.00	On-chip	On-chip	2.0	6.0	On-chip capacitor, lead type
	KBR-5.0MWS	5.00	On-chip	On-chip	2.0	6.0	On-chip capacitor, lead type
	PBRC 5.00A	5.00	33	33	2.0	6.0	Chip type
TDK Corp.	CCR4.0MC3	4.00	On-chip	On-chip	2.0	6.0	On-chip capacitor
	CCR5.0MC3	5.00	On-chip	On-chip	2.0	6.0	On-chip capacitor

Main system clock: Crystal resonator (T_A = –10 to +70°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Daishinku Corp.	SMD-49	3.579545	27	27	1.5	2.0	6.0

Subsystem clock: Crystal resonator (T_A = –10 to +70°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku Corp.	DT-38 (1TA252E00)	32.768	27	20	330	2.0	6.0

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. However, oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

(2) μPD78058

Main system clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Kyocera Corp.	PBRC4.19A	4.19	33	33	2.0	6.0	
	PBRC4.19B	4.19	On-chip	On-chip	2.0	6.0	On-chip capacitor
	KBR-4.19MSA	4.19	33	33	2.0	6.0	
	KBR-4.19MKS	4.19	On-chip	On-chip	2.0	6.0	On-chip capacitor
	PBRC4.91A	4.91	33	33	2.0	6.0	
	PBRC4.91B	4.91	On-chip	On-chip	2.0	6.0	On-chip capacitor
	KBR-4.91MSA	4.91	33	33	2.0	6.0	
	KBR-4.91MKS	4.91	On-chip	On-chip	2.0	6.0	On-chip capacitor

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. However, oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch open drain)	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 6.0 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V**Note**	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P60 to P63	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V**Note**	0		0.1V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 6.0 V, open drain, pulled-up (R = 1 KΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When using the P07/X1 pin as P07, the inverse phase of P07 should be input to XT2.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63			–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resistor Note 2	R_2	V_{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ

Notes 1. When pull-up resistors are not connected to P60 to P63 (specifiable by the mask option), a low-level input leakage current of –200 μA (MAX.) flows only for 1.5 clocks (without wait) after a read instruction has been executed to port 6 (P6) or port mode register 6 (PM6). At times other than this 1.5-clock interval, a –3 μA (MAX.) current flows.

2. A software pull-up resistor can be used only in the range of V_{DD} = 2.7 to 6.0 V.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note 2]	V_{DD} = 5.0 V ±10%[Note 5]		4	12	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.6	1.8	mA
			V_{DD} = 2.2 V ±10%[Note 6]		0.35	1.05	mA
		5.0 MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note 3]	V_{DD} = 5.0 V ±10%[Note 5]		6.5	19.5	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.8	2.4	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz)[Note 2]	V_{DD} = 5.0 V ±10%		1.4	4.2	mA
			V_{DD} = 3.0 V ±10%		0.5	1.5	mA
			V_{DD} = 2.2 V ±10%		280	840	μA
		5.0 MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz)[Note 3]	V_{DD} = 5.0 V ±10%		1.6	4.8	mA
			V_{DD} = 3.0 V ±10%		0.65	1.95	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ±10%		60	120	μA
			V_{DD} = 3.0 V ±10%		32	64	μA
			V_{DD} = 2.2 V ±10%		24	48	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	15	μA
			V_{DD} = 2.2 V ±10%		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor used	V_{DD} = 5.0 V ±10%		1	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
			V_{DD} = 2.2 V ±10%		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.2 V ±10%		0.05	10	μA

Notes 1. Refers to the current flowing to the V_{DD} and AV_{DD} pins. The current flowing to the A/D converter, D/A converter, and on-chip pull-up resistors are not included.

2. Operation with main system clock $f_{XX} = f_X/2$ (when the oscillation mode selection register (OSMS) is set to 00H)

3. Operation with main system clock $f_{XX} = f_X$ (when OSMS is set to 01H)

4. When the main system clock operation is stopped.

5. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

6. Low-speed mode operation (when PCC is set to 04H).

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock (f_{XX} = 2.5 MHz)Note 1	V_{DD} = 2.7 to 6.0 V	0.8		64	μs
					2.2		64	μs
			Operating with main system clock (f_{XX} = 5.0 MHz)Note 2	4.5 V ≤ V_{DD} ≤ 6.0 V	0.4		32	μs
				2.7 V ≤ V_{DD} < 4.5 V	0.8		32	μs
			Operating with subsystem clock		40Note 3	122	125	μs
	TI00, TI01, TI1, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		4	MHz
					0		275	kHz
★	TI00 input high-/low-level width	t_{TIH}, t_{TIL}	3.5 V ≤ V_{DD} ≤ 6.0 V		$2/f_{sam}$ + 0.1Note 4			μs
			2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$ + 0.2Note 4			μs
					$2/f_{sam}$ + 0.5Note 4			μs
★	TI01 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		10			μs
					20			μs
	TI1, TI2 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		100			ns
					1.8			μs
★	Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0	3.5 V ≤ V_{DD} ≤ 6.0 V	$2/f_{sam}$ + 0.1Note 4			μs
				2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$ + 0.2Note 4			μs
					$2/f_{sam}$ + 0.5Note 4			μs
			INTP1 to INTP6, KR0 to KR7	V_{DD} = 2.7 to 6.0 V	10			μs
					20			μs
	$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 6.0 V		10			μs
					20			μs

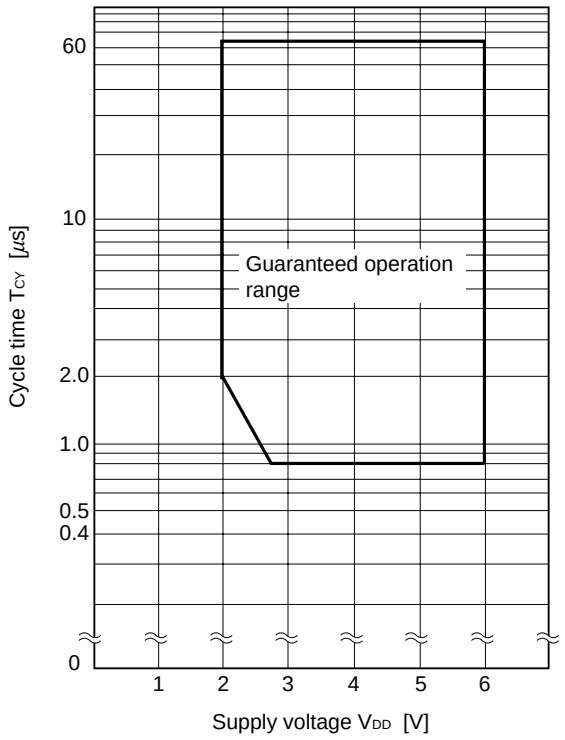
Notes 1. Operation with main system clock $f_{XX} = f_X/2$ (when the oscillation mode selection register (OSMS) is set to 00H)

2. Operation with main system clock $f_{XX} = f_X$ (when OSMS is set to 01H)

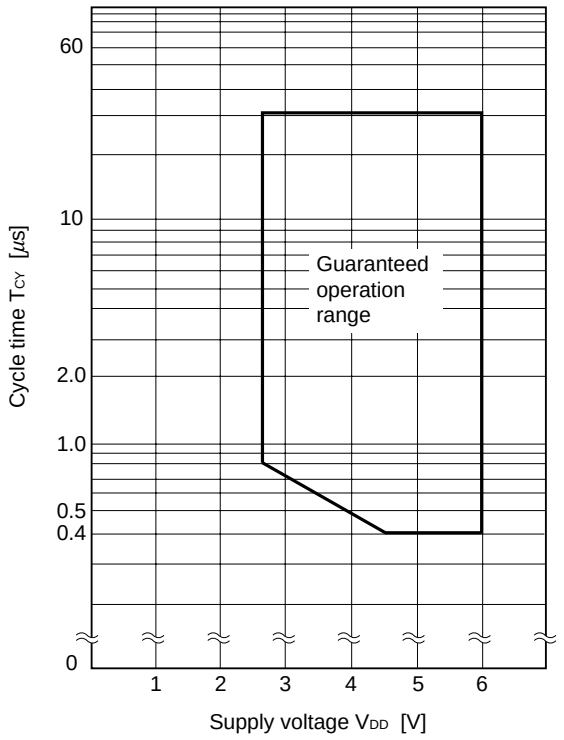
3. Value when an external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

4. Selection of $f_{sam} = f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$ is possible with bits 0 and 1 (SCS0, SCS1) of the sampling clock selection register (SCS) (when N= 0 to 4).

T_{CY} vs. V_{DD} ($f_{XX} = f_X/2$ main system clock operation)



T_{CY} vs. V_{DD} ($f_{XX} = f_X$ main system clock operation)



(2) Read/write operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 4.5 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY} - 50$		ns
Address setup time	t_{ADS}		$0.85t_{CY} - 50$		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85 + 2n)t_{CY} - 80$	ns
	t_{ADD2}			$(4 + 2n)t_{CY} - 100$	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY} - 100$	ns
	t_{RDD2}			$(2.85 + 2n)t_{CY} - 100$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2 + 2n)t_{CY} - 60$		ns
	t_{RDL2}		$(2.85 + 2n)t_{CY} - 60$		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			$0.85t_{CY} - 50$	ns
	t_{RDWT2}			$2t_{CY} - 60$	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			$2t_{CY} - 60$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15 + 2n)t_{CY}$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85 + 2n)t_{CY} - 100$		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		$(2.85 + 2n)t_{CY} - 60$		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		25		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$0.85t_{CY} + 20$		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		$0.85t_{CY} - 10$	$1.15t_{CY} + 20$	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t_{RDADH}		$0.85t_{CY} - 50$	$1.15t_{CY} + 50$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY} + 40$	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$1.15t_{CY} + 40$	$3.15t_{CY} + 40$	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$1.15t_{CY} + 30$	$3.15t_{CY} + 30$	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}	V_{DD} = 2.7 to 6.0 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address setup time	t_{ADS}	V_{DD} = 2.7 to 6.0 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address hold time	t_{ADH}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} – 10		ns
			0.37t_{CY} – 40		ns
Data input time from address	t_{ADD1}	V_{DD} = 2.7 to 6.0 V		(3 + 2n)t_{CY} – 160	ns
				(3 + 2n)t_{CY} – 320	ns
	t_{ADD2}	V_{DD} = 2.7 to 6.0 V		(4 + 2n)t_{CY} – 200	ns
				(4 + 2n)t_{CY} – 300	ns
Data input time from $\overline{RD}$↓	t_{RDD1}	V_{DD} = 2.7 to 6.0 V		(1.4 + 2n)t_{CY} – 70	ns
				(1.37 + 2n)t_{CY} – 120	ns
	t_{RDD2}	V_{DD} = 2.7 to 6.0 V		(2.4 + 2n)t_{CY} – 70	ns
				(2.37 + 2n)t_{CY} – 120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}	V_{DD} = 2.7 to 6.0 V	(1.4 + 2n)t_{CY} – 20		ns
			(1.37 + 2n)t_{CY} – 20		ns
	t_{RDL2}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} – 20		ns
			(2.37 + 2n)t_{CY} – 20		ns
Input time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{RDWT1}	V_{DD} = 2.7 to 6.0 V		t_{CY} – 100	ns
				t_{CY} – 200	ns
	t_{RDWT2}	V_{DD} = 2.7 to 6.0 V		2t_{CY} – 100	ns
				2t_{CY} – 200	ns
Input time from $\overline{WR}$↓ to $\overline{WAIT}$↓	t_{WRWT}	V_{DD} = 2.7 to 6.0 V		2t_{CY} – 100	ns
				2t_{CY} – 200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} – 60		ns
			(2.37 + 2n)t_{CY} – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} – 20		ns
			(2.37 + 2n)t_{CY} – 20		ns
Delay time from ASTB↓ to $\overline{RD}$↓	t_{ASTRD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} – 30		ns
			0.37t_{CY} – 50		ns
Delay time from ASTB↓ to $\overline{WR}$↓	t_{ASTWR}	V_{DD} = 2.7 to 6.0 V	1.4t_{CY} – 30		ns
			1.37t_{CY} – 50		ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from $\overline{RD}$↑ to ASTB↑ at external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ at external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} – 20		ns
			0.37t_{CY} – 40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 2.7 to 6.0 V	0	60	ns
			0	120	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 2.7 to 6.0 V	t_{CY}	t_{CY} + 60	ns
			t_{CY}	t_{CY} + 120	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{WTRD}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY} + 180	2.6t_{CY} + 180	ns
			0.63t_{CY} + 350	2.63t_{CY} + 350	ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{WTWR}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY} + 120	2.6t_{CY} + 120	ns
			0.63t_{CY} + 240	2.63t_{CY} + 240	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 6.0 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
Delay time from $\overline{SCK0}$↓ to SO0 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI3}			$t_{KCY3}/2$			ns
Delay time from $\overline{SCK0}\downarrow$ to SB0, SB1 output	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}\uparrow$	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(iv) SBI mode ($\overline{SCK0}$ ... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI4}			$t_{KCY4}/2$			ns
Delay time from $\overline{SCK0}\downarrow$ to SB0, SB1 output	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}\uparrow$	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 6.0 V	$t_{KCY5}/2 - 160$			ns
				$t_{KCY5}/2 - 190$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 6.0 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 6.0 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO5}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... Internal clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH6}	V_{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{SCK0}$ low-level width	t_{KL6}	V_{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 6.0 V	t_{KCY7}/2 – 50			ns
			t_{KCY7}/2 – 100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
Delay time from $\overline{SCK1}$↓ to SO1 output	t_{KSO7}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}		400			ns
Delay time from $\overline{SCK1}$↓ to SO1 output	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 6.0 V	$t_{KCY9}/2 - 50$			ns
			$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF[Note]			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	V_{DD} = 2.7 to 6.0 V	$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
			$t_{KCY9} - 60$		$t_{KCY9} + 60$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			200			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the load capacitance of the SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
Delay time from $\overline{SCK1}$↓ to SO1 output	t_{KSO10}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 6.0 V	t_{KCY7}/2 – 50			ns
			t_{KCY7}/2 – 100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI11}		400			ns
Delay time from $\overline{SCK2}$↓ to SO2 output	t_{KSO11}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO2 output line.

★ **(ii) 3-wire serial I/O mode ($\overline{SCK2}$ ... External clock input)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK12}		100			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI12}		400			ns
Delay time from $\overline{SCK2}$↓ to SO2 output	t_{KSO12}	C = 100 pF[Note]			300	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO2 output line.

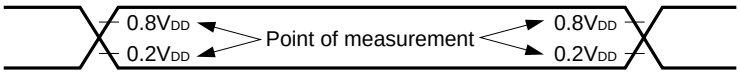
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
					19531	bps

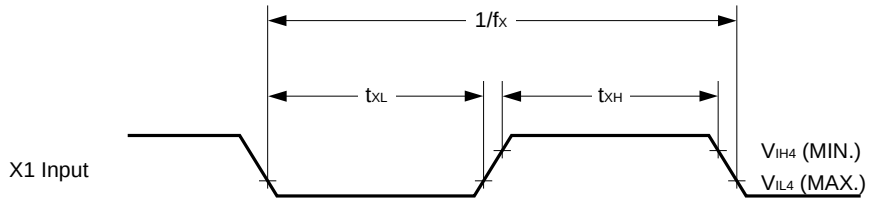
(iv) UART mode (External clock input)

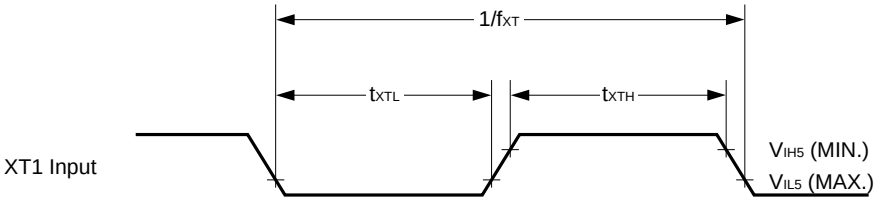
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
ASCK rise, fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 6.0 V, when not using external device expansion function.			1000	ns
					160	ns

AC Timing Measurement Points (Excluding X1, XT1 Input)

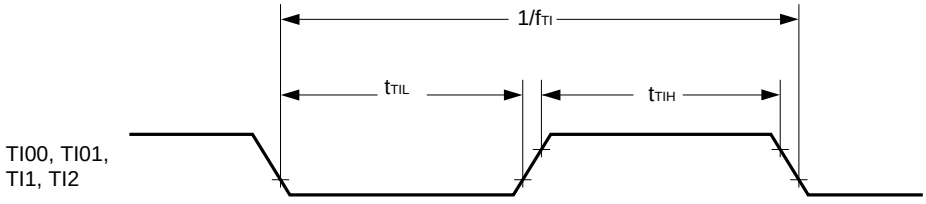


Clock Timing



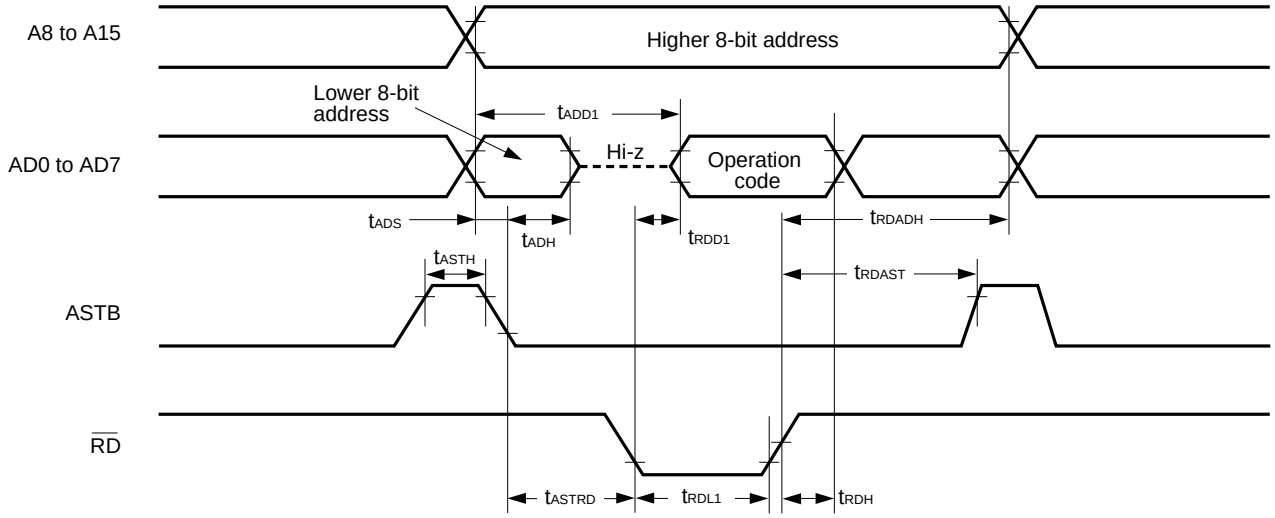


TI Timing

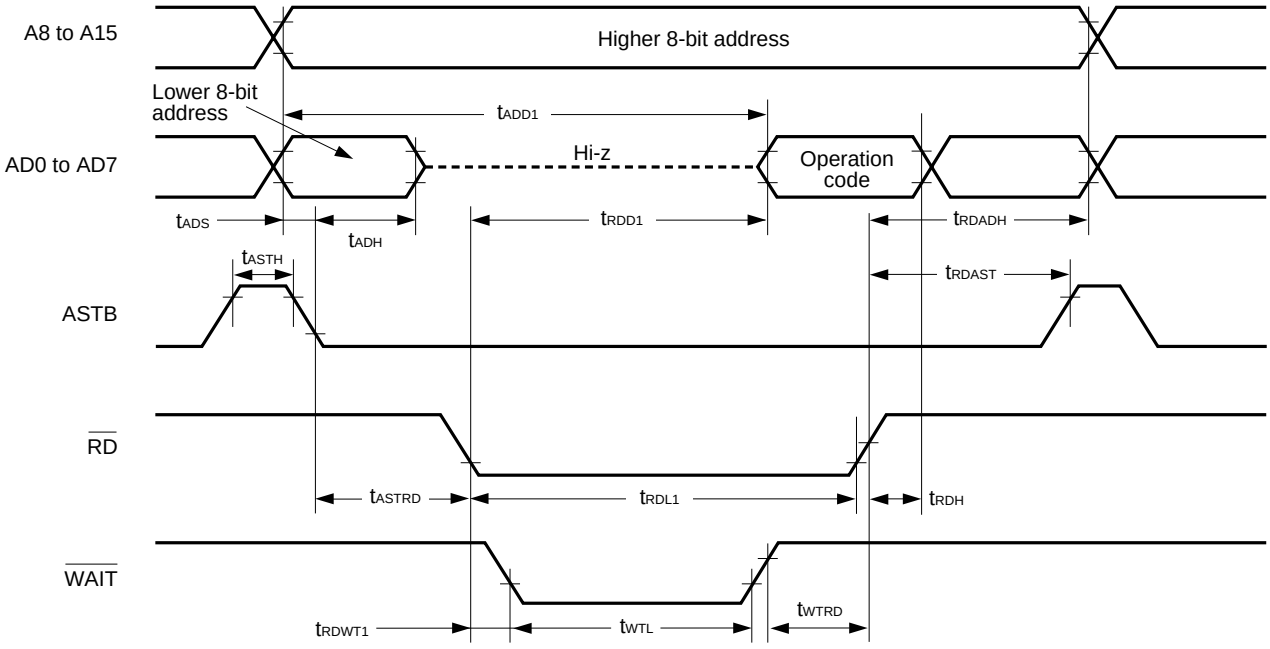


Read/Write Operation

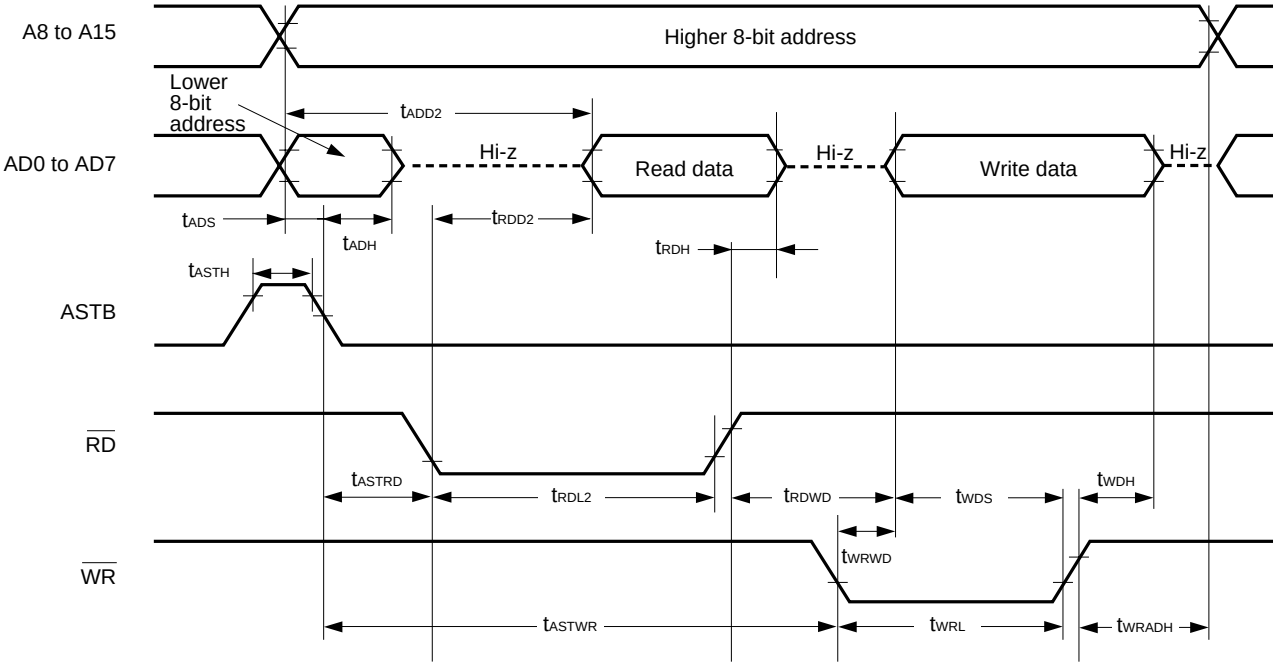
External fetch (no wait):



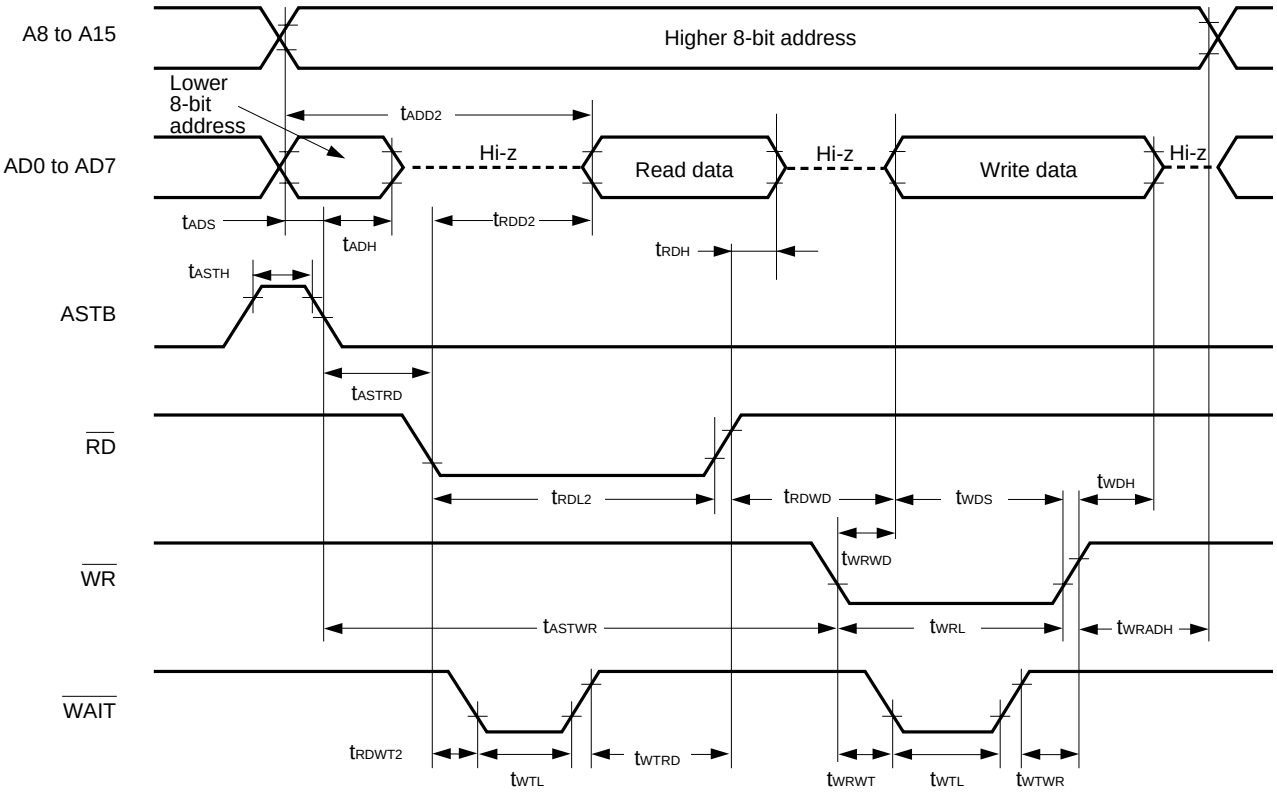
External fetch (wait insertion):



External data access (no wait):

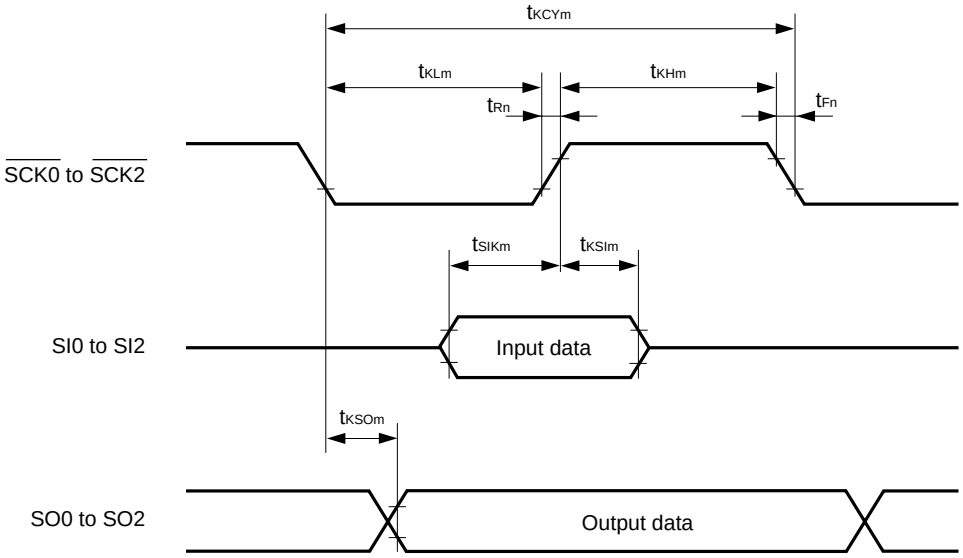


External data access (wait insertion):



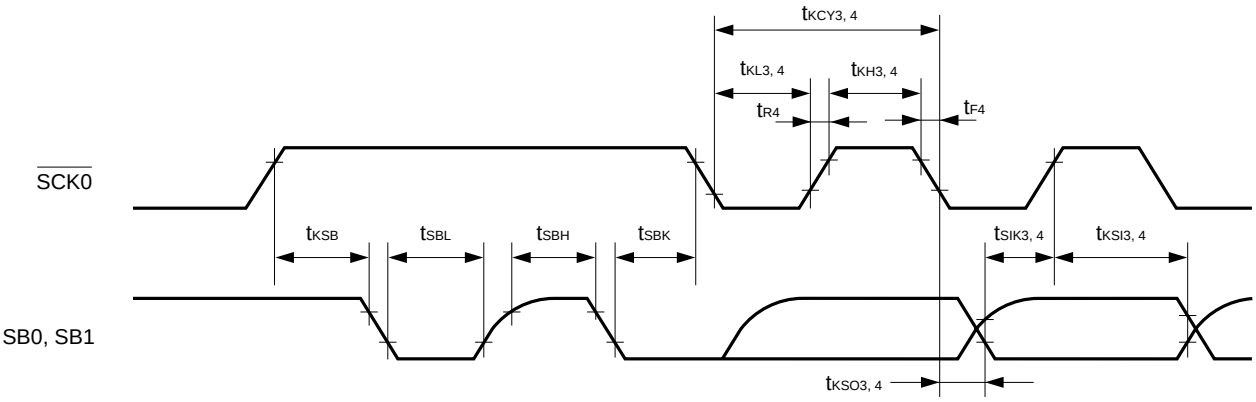
Serial Transfer Timing

3-wire serial I/O mode:

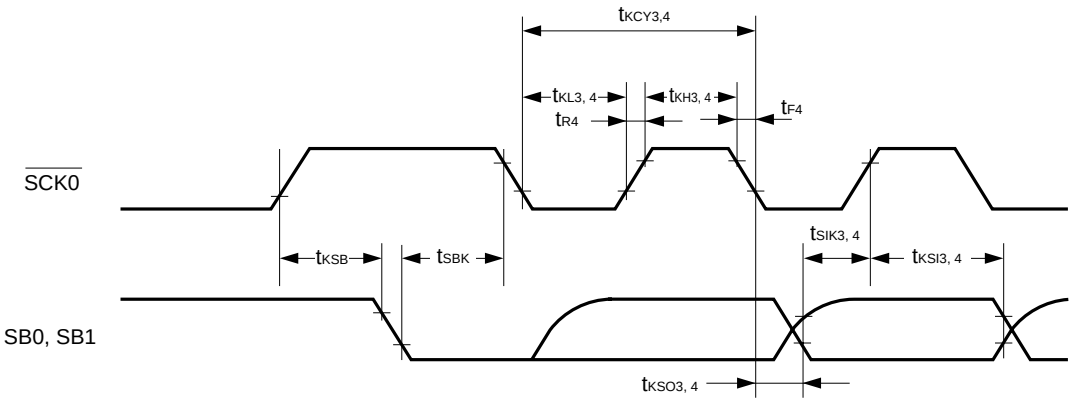


m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

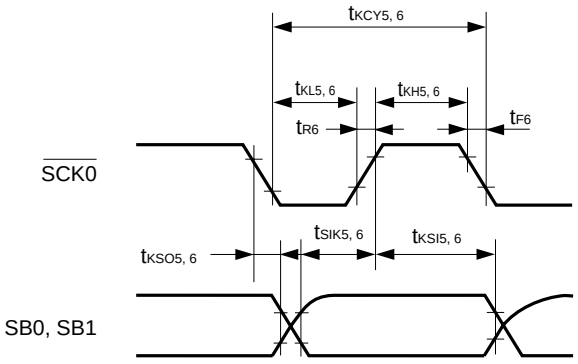
SBI mode (bus release signal transfer):



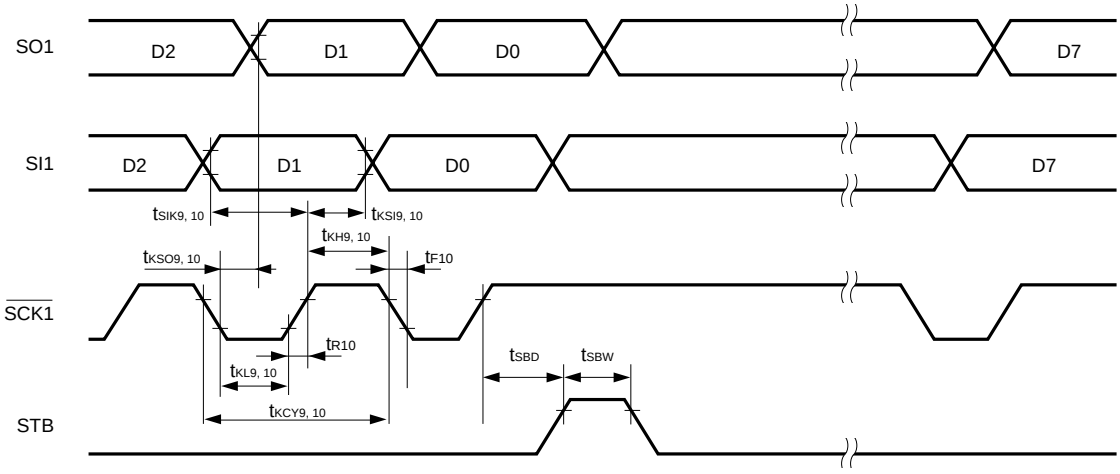
SBI mode (command signal transfer):



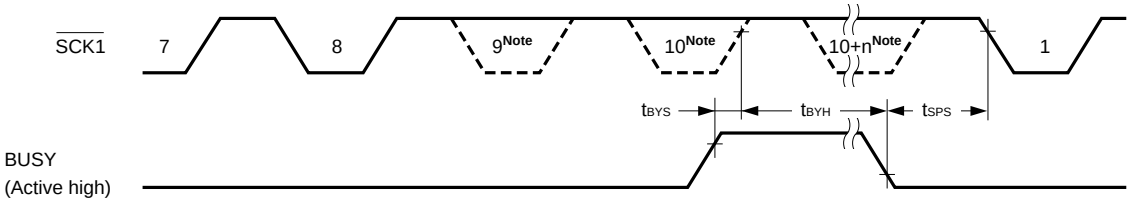
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:

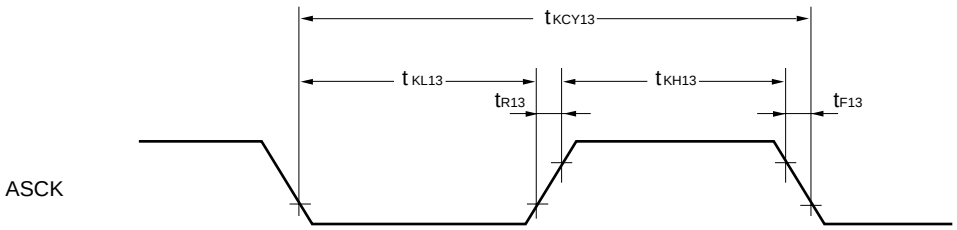


3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART mode (external clock input):



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			±0.6	%
		2.0 V ≤ AV_{REF0} < 2.7 V			±1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.0		AV_{DD}	V
Resistance between AV_{REF0} and AV_{SS}	R_{AIREF0}		4	14		kΩ

Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value.

Remark f_{XX}: Main system clock frequency (f_X or f_X/2)
f_X: Main system clock oscillation frequency

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error		R = 2 MΩ[Note 1]				1.2	%
		R = 4 MΩ[Note 1]				0.8	%
		R = 10 MΩ[Note 1]				0.6	%
Settling time		C = 30 pF[Note 1]	4.5 V ≤ AV_{REF1} ≤ 6.0 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			2.0 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_O	DACS0, DACS1 = 55H[Note 2]			10		kΩ
Analog reference voltage	AV_{REF1}			2.0		V_{DD}	V
★ Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]		4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance, respectively.
2. Value for one D/A converter channel

Remark DACS0 and DACS1: D/A conversion value setting registers 0 and 1

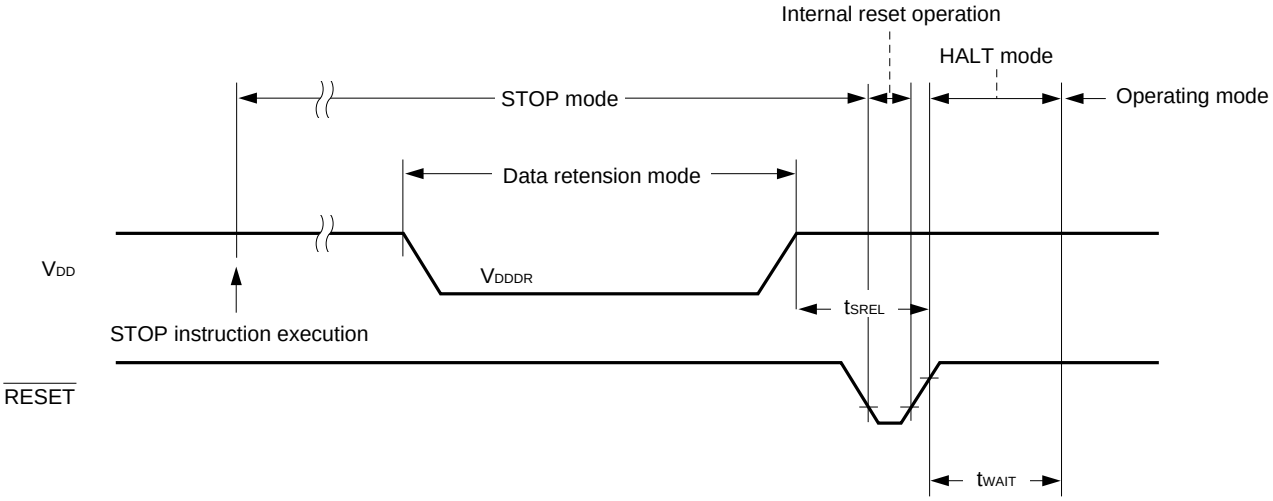
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		6.0	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V When the subsystem clock is unused (XT1 = V_{DD}) and the feed-back resistor is disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

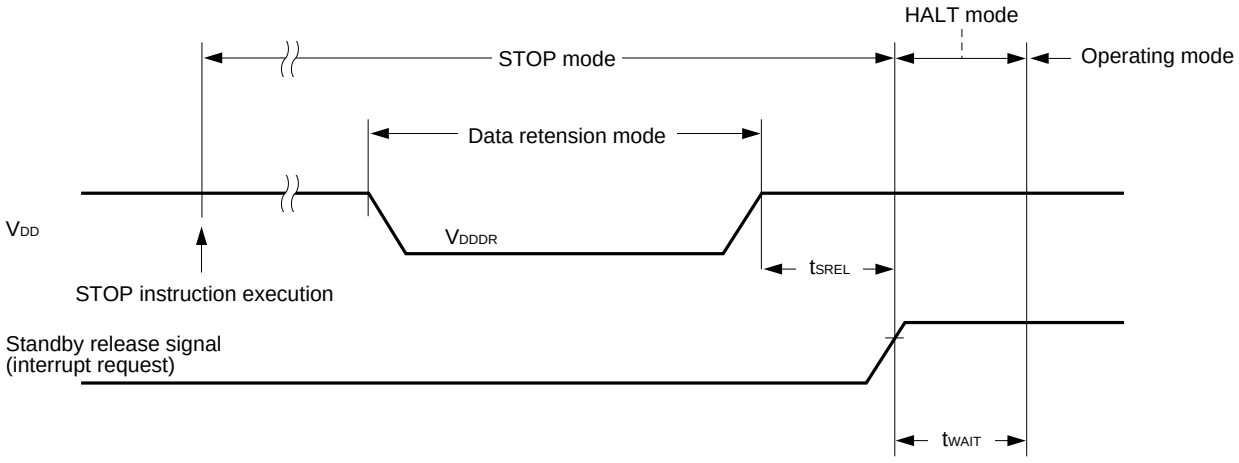
Note Selection of $2^{12}/f_{XX}$ and $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency

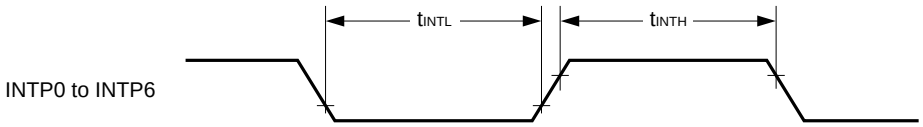
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



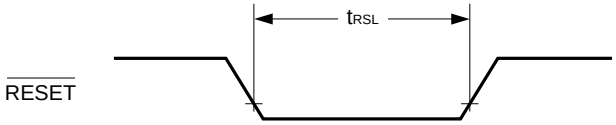
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

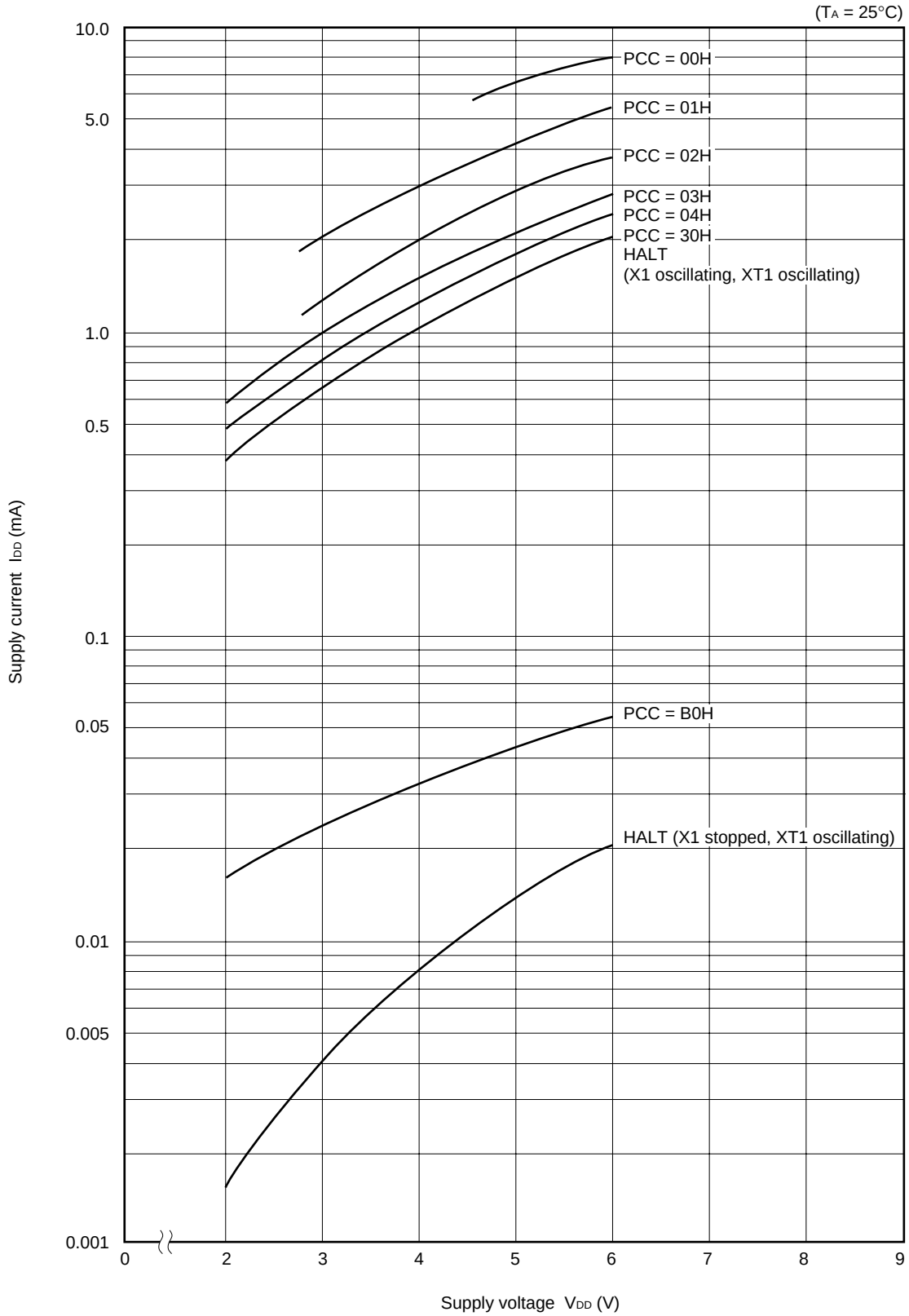


$\overline{\text{RESET}}$ Input Timing

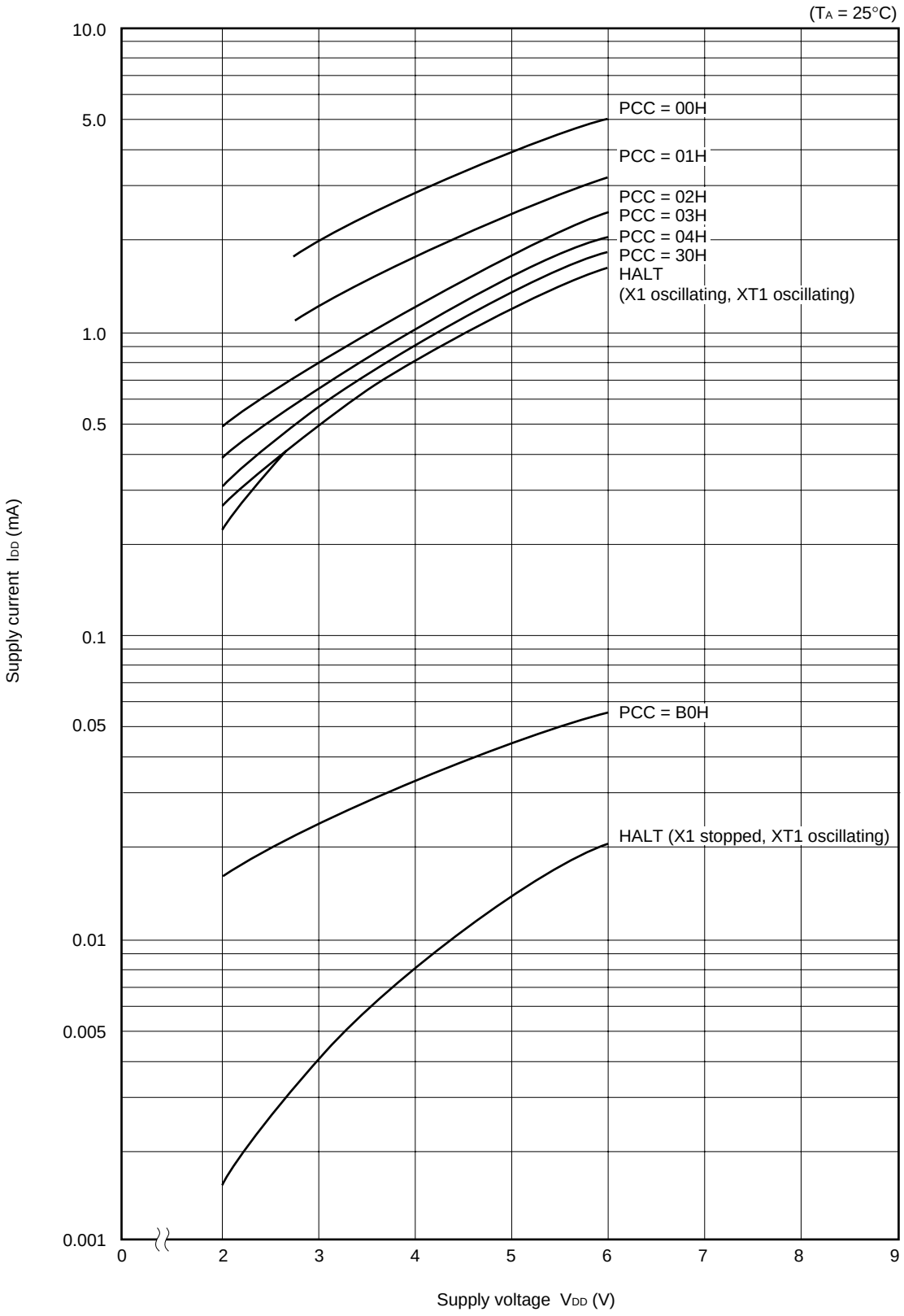


12. CHARACTERISTICS CURVES (REFERENCE VALUES)

I_{DD} vs. V_{DD} ($f_X = f_{XX}$ = 5.0 MHz)

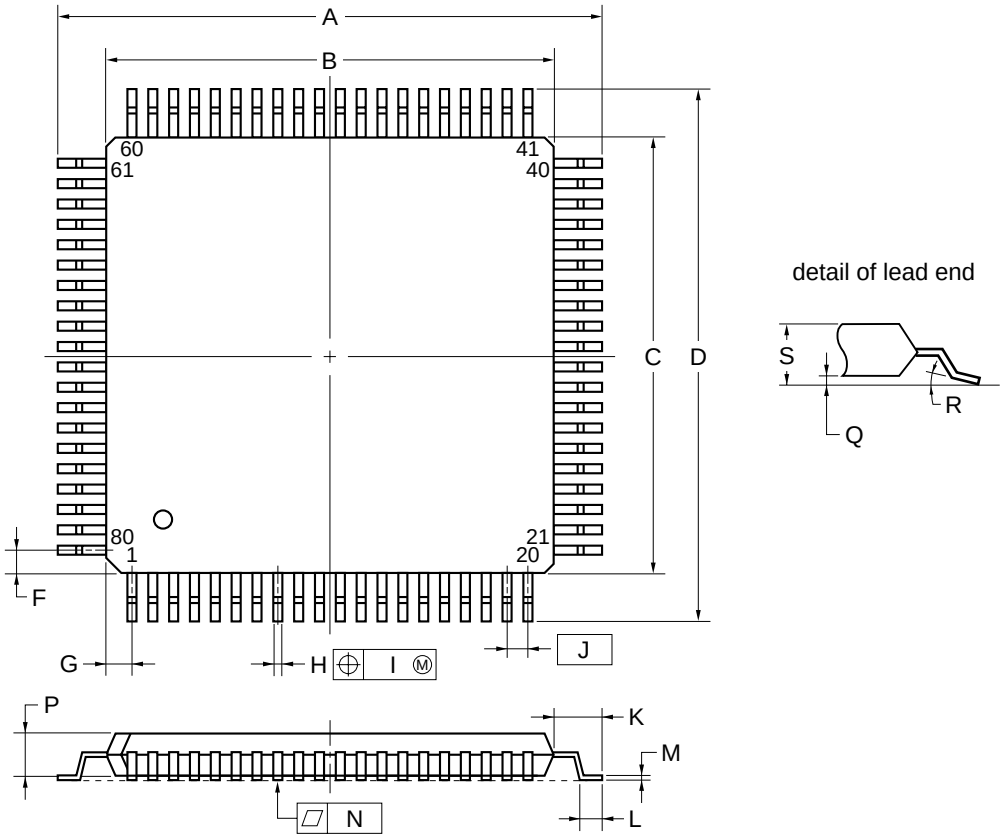


I_{DD} vs. V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)



13. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



NOTE

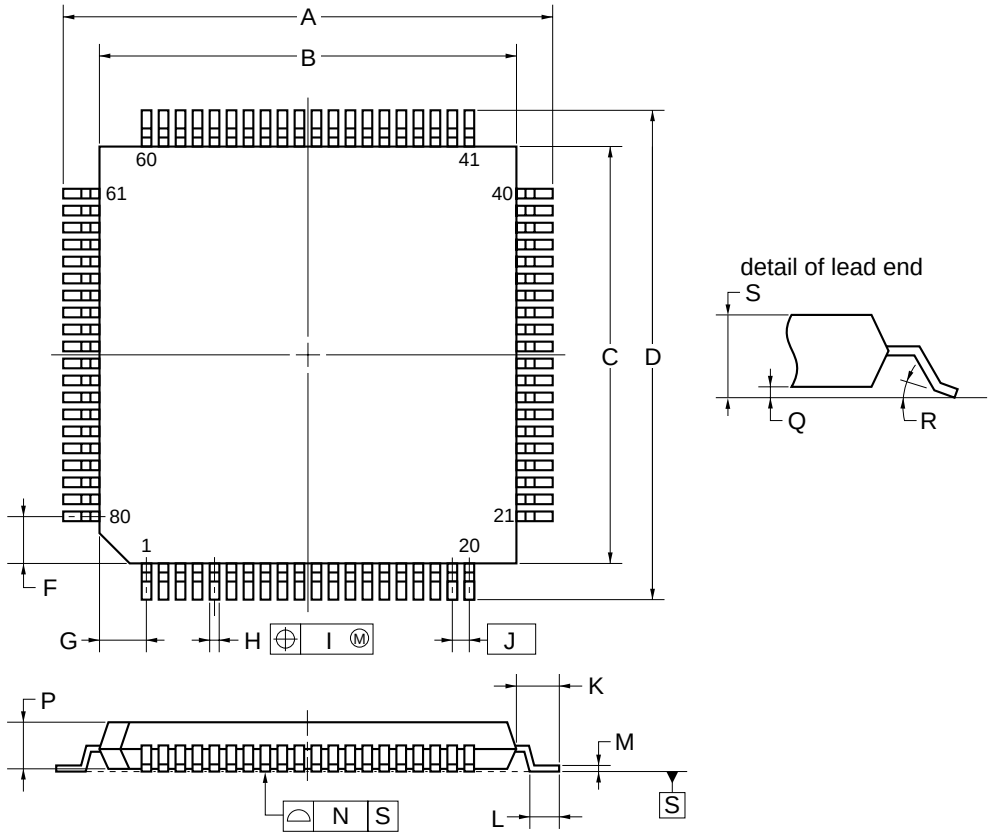
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

Remark Dimensions and materials of ES product are the same as those of mass-production products.

80 PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.00±0.20
B	12.00±0.20
C	12.00±0.20
D	14.00±0.20
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.05±0.07
Q	0.10±0.05
R	5°±5°
S	1.27 MAX.

P80GK-50-BE9-6

Remark Dimensions and materials of ES product are the same as those of mass-production products.

14. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD78052GC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD78053GC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD78054GC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD78055GC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD78056GC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD78058GC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice max.	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice max.	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial Heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

Table 14-1. Surface Mounting Type Soldering Conditions (2/2)

(2) μPD78052GK-×××-BE9: 80-pin plastic TQFP (12 × 12 mm)
μPD78053GK-×××-BE9: 80-pin plastic TQFP (12 × 12 mm)
μPD78054GK-×××-BE9: 80-pin plastic TQFP (12 × 12 mm)
μPD78055GK-×××-BE9: 80-pin plastic TQFP (12 × 12 mm)
μPD78056GK-×××-BE9: 80-pin plastic TQFP (12 × 12 mm)
μPD78058GK-×××-BE9: 80-pin plastic TQFP (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times max., Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times max., Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-3
Partial Heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

★ APPENDIX A. DEVELOPMENT TOOLS

The following support tools are available for system development using the μPD78054 Subseries.
Refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF78054	μPD78054 Subseries device file
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) PROM Writing Tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054GK PA-78P054KK-T	Programmer adapter connected to a PG-1500
PG-1500 controller	PG-1500 control program

(3) Debugging Tools

• When using in-circuit emulator IE-78K0-NS

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA[Note]	Performance board to enhance and expand the functions of IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 series PC (except notebook type) as the host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook type PC as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as the host machine
IE-70000-PCI-IF	Adapter necessary when using PC including PCI bus as the host machine
IE-780308-NS-EM1	Emulation board common to μPD780308 Subseries
NP-80GC NP-80GC-TQ	Emulation probe for 80-pin plastic QFP (GC-8BT type)
NP-80GK	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
EV-9200GC-80	Conversion socket to connect the NP-80GC and a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted
TGC-080SBP	Conversion socket to connect the NP-80GC-TQ and a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted
TGK-080SDW	Conversion adapter to connect the NP-80GK and a target system board on which an 80-pin plastic TQFP (GK-BE9 type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF78054	Device file for μPD78054 Subseries

Note Under development

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series PC (except notebook type) as the host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as the host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using PC including PCI bus as the host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as the host machine
IE-780308-NS-EM1 IE-780308-R-EM	Emulation board common to μPD780308 Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780308-NS-EM1 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
EV-9200GC-80	Conversion socket to connect the EP-78230GC-R and a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted
TGK-080SDW	Conversion adapter to connect the EP-78054GK-R and a target system board on which an 80-pin plastic TQFP (GK-BE9 type) can be mounted
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF78054	Device file for μPD78054 Subseries

(4) Real-Time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF78054.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and DF78054.
- The NP-80GC, NP-80GC-TQ, and NP-80GK are products of Naito Densei Machida Mfg. Co., Ltd. (TEL +81-44-822-3813). Consult an NEC sales representative regarding purchase of these products.
- The TGK-080SDW and TGC-080SBP are products of TOKYO ELETECH CORPORATION.
  For further information, contact: Daimaru Kogyo Ltd. Tokyo Electronics Department (TEL +81-3-3820-7112)
  Osaka Electronic Department (TEL +81-6-6244-6672)
- For third party development tools, refer to **78K/0 Series Selection Guide (U11126E)**.
- The host machines and operating systems suitable for each software are as follows.

Host Machine [OS] / Software	PC PC-9800 series [Windows™] IBM PC/AT compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√Note	√
CC78K/0	√Note	√
PG-1500 controller	√Note	—
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name		Document No. (English)	Document No. (Japanese)
μPD78054, 78054Y Subseries User's Manual		U11747E	U11747J
μPD78052, 78053, 78054, 78055, 78056, 78058 Data Sheet		This document	U12327J
μPD78P054, 78P058 Data Sheet		U10417E	U10417J
78K/0 Series User's Manual Instructions		U12326E	U12326J
78K/0 Series Instruction Set		—	U10904J
78K/0 Series Instruction Table		—	U10903J
μPD78054 Subseries Special Function Register Table		—	U10102J
78K/0 Series Application Note	Basic (III)	U10182E	U10182J
	Floating Point Arithmetic Programs	IEA-1289	U13482J

Documents Related to Development Tools (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K0 C Compiler Application Note	Programming Know-how	U13034E	U13034J
PG-1500 PROM Programmer		U11940E	U11940J
PG-1500 Controller PC-9800 Series (MS-DOS™) based		EEU-1291	EEU-704
PG-1500 Controller IBM PC Series (PC DOS™) based		U10540E	EEU-5008
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-EM		To be prepared	To be prepared
IE-780308-NS-EM1		To be prepared	To be prepared
IE-780308-R-EM		U11362E	U11362J
EP-78230		EEU-1515	EEU-985
EP-78054GK-R		EEU-1468	EEU-932
SM78K0 System Simulator Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger Windows based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows based	Guide	U11649E	U11649J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Other Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Microcomputer Product Series Guide	—	U11416J

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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