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## 4-BIT SINGLE-CHIP MICROCONTROLLERS

### DESCRIPTION

The  $\mu$ PD754264 is a 4-bit single-chip microcontroller which incorporates the EEPROM™ for key-less entry application.

It incorporates a  $32 \times 8$ -bit EEPROM, a CPU performing operation, a 4-Kbyte mask ROM to store software, a  $128 \times 4$ -bit RAM to store the operation data, an 8-bit resolution A/D converter, and a carrier generator which easily outputs waveforms for infrared remote controller.

The details of functions are described in the following user's manual. Be sure to read it before designing.

**$\mu$ PD754264 User's Manual: U12287E**

### FEATURES

- On-chip EEPROM:  $32 \times 8$  bits (mapped to the data memory)
- On-chip key return reset function for key-less entry
- On-chip low-voltage A/D converter ( $AV_{REF} = 1.8$  to  $6.0$  V), 8-bit resolution  $\times$  2 channels
- Low-voltage operation:  $V_{DD} = 1.8$  to  $6.0$  V
- Timer function (4 channels)
  - Basic interval timer/watchdog timer : 1 channel
  - 8-bit timer counter : 3 channels
- On-chip memory
  - Program memory (ROM)  
4096  $\times$  8 bits
  - Data memory (static RAM)  
128  $\times$  4 bits
- Instruction execution time variable function suited for high-speed operation and power saving.
  - 0.95, 1.91, 3.81, 15.3  $\mu$ s (@  $f_x = 4.19$ -MHz operation)
  - 0.67, 1.33, 2.67, 10.7  $\mu$ s (@  $f_x = 6.0$ -MHz operation)

### APPLICATIONS

Automotive appliances such as key-less entry, compact data carrier, etc.

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**ORDERING INFORMATION**

	Part Number	Package
	μPD754264GS-xxx-BA5	20-pin plastic SOP (300 mil, 1.27-mm pitch)
★	μPD754264GS-xxx-BA5-A	20-pin plastic SOP (300 mil, 1.27-mm pitch)

- Remarks** 1. Products with “-A” at the end of the part number are lead-free products.  
 2. xxx indicates ROM code suffix.

**Functional Outline**

Parameter		Function	
Instruction execution time		<ul style="list-style-type: none"> <li>• 0.95, 1.91, 3.81, 15.3 μs (@ fx = 4.19-MHz operation)</li> <li>• 0.67, 1.33, 2.67, 10.7 μs (@ fx = 6.0-MHz operation)</li> </ul>	
On-chip memory	Mask ROM	4096 × 8 bits (0000H-0FFFH)	
	RAM	128 × 4 bits (000H-07FH)	
	EEPROM	32 × 8 bits (400H-43FH)	
System clock oscillator		Crystal/ceramic oscillator	
General-purpose register		<ul style="list-style-type: none"> <li>• 4-bit operation: 8 × 4 banks</li> <li>• 8-bit operation: 4 × 4 banks</li> </ul>	
Input/output port	CMOS input	4	On-chip pull-up resistor can be specified by mask option.
	CMOS input/output	9	On-chip pull-up resistor connection can be specified by means of software.
	Total	13	
Start-up time after reset		2 <sup>17</sup> /fx, 2 <sup>15</sup> /fx, 2 <sup>13</sup> /fx (selected by mask option)	
Stand-by mode release time		2 <sup>20</sup> /fx, 2 <sup>17</sup> /fx, 2 <sup>15</sup> /fx, 2 <sup>13</sup> /fx (selected by the setting of BTM)	
Timer		4 channels <ul style="list-style-type: none"> <li>• 8-bit timer counter (can be used as 16-bit timer counter) : 3 channels</li> <li>• Basic interval/watchdog timer : 1 channel</li> </ul>	
A/D converter		8-bit resolution × 2 channels (1.8 V ≤ AVREF ≤ VDD)	
Bit sequential buffer		16 bits	
Vectored interrupt		External: 1, Internal: 5	
Test input		External: 1 (key return reset function available)	
Standby function		STOP/HALT mode	
Operating ambient temperature		TA = -40 to +85 °C	
Operating supply voltage		VDD = 1.8 to 6.0 V	
Package		20-pin plastic SOP (300 mil, 1.27-mm pitch)	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW) ..... 5

2. BLOCK DIAGRAM..... 6

3. PIN FUNCTION ..... 7

    3.1 Port Pins ..... 7

    3.2 Non-port Pins ..... 8

    3.3 Pin Input/Output Circuits ..... 9

    3.4 Recommended Connection of Unused Pins ..... 10

4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE ..... 11

    4.1 Difference between Mk I and Mk II Modes ..... 11

    4.2 Setting Method of Stack Bank Select Register (SBS) ..... 12

5. MEMORY CONFIGURATION ..... 13

6. EEPROM ..... 16

7. PERIPHERAL HARDWARE FUNCTIONS ..... 17

    7.1 Digital Input/Output Ports ..... 17

    7.2 Clock Generator ..... 17

    7.3 Basic Interval Timer/Watchdog Timer ..... 19

    7.4 Timer Counter ..... 20

    7.5 A/D Converter ..... 24

    7.6 Bit Sequential Buffer ..... 25

8. INTERRUPT FUNCTION AND TEST FUNCTION ..... 26

9. STANDBY FUNCTION ..... 28

10. RESET FUNCTION ..... 29

    10.1 Configuration and Operation Status of RESET Function ..... 29

    10.2 Watchdog Flag (WDF), Key Return Flag (KRF) ..... 33

11. MASK OPTION ..... 35

12. INSTRUCTION SETS ..... 36

13. ELECTRICAL SPECIFICATIONS ..... 45

14. CHARACTERISTICS CURVES (REFERENCE VALUES) ..... 55

15. PACKAGE DRAWINGS ..... 58

16. RECOMMENDED SOLDERING CONDITIONS ..... 59

**APPENDIX A. COMPARISON OF FUNCTIONS BETWEEN μPD754264 AND 75F4264 ..... 60**

**APPENDIX B. DEVELOPMENT TOOLS ..... 61**

**APPENDIX C. RELATED DOCUMENTS ..... 64**

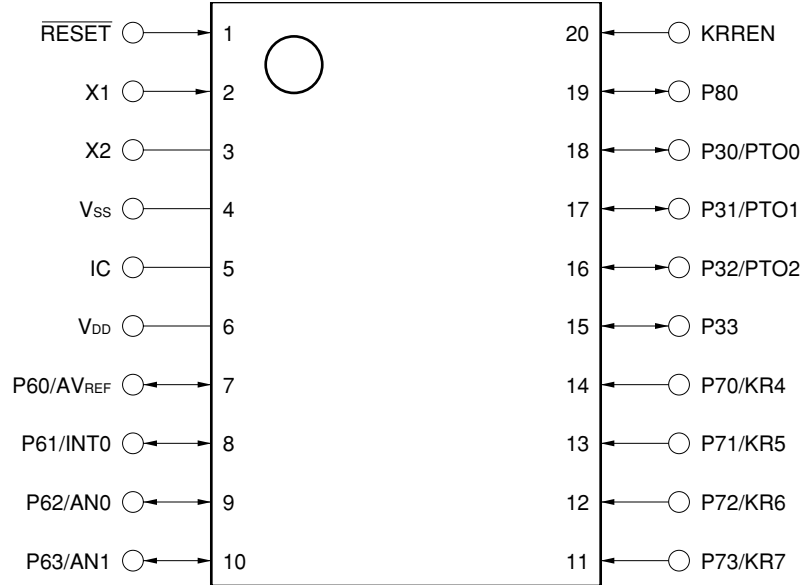
1. PIN CONFIGURATION (TOP VIEW)

- 20-pin Plastic SOP (300 mil, 1.27-mm pitch)

μPD754264GS-xxx-BA5

★

μPD754264GS-xxx-BA5-A

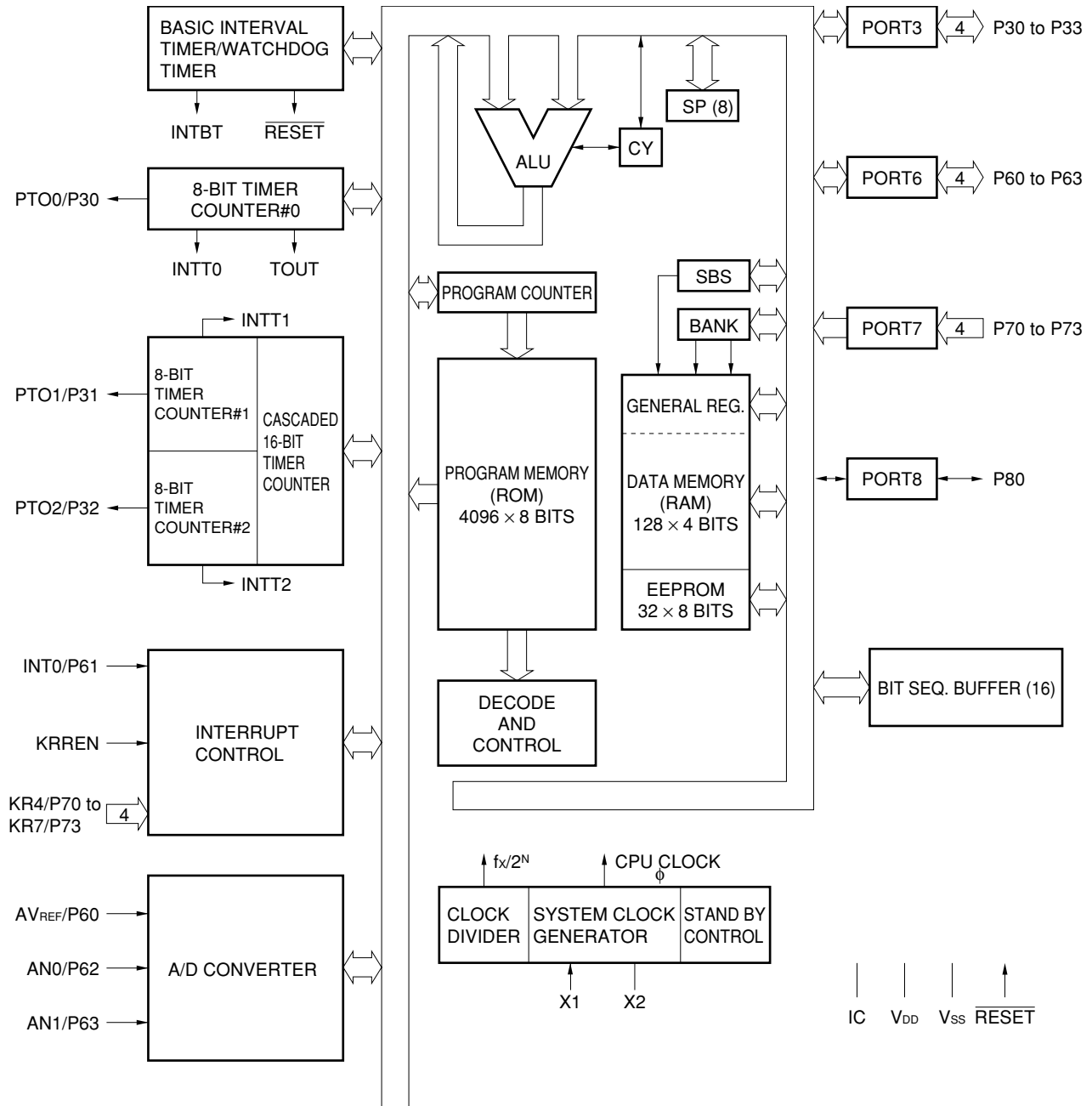


IC: Internally Connected (Connect to V<sub>DD</sub> directly)

Pin Identification

AN0, AN1	: Analog input 0,1	P70 to P73	: Port 7
AVREF	: Analog reference	P80	: Port 8
IC	: Internally connected	PTO0 to PTO2	: Programmable timer outputs 0 to 2
INT0	: External vectored interrupt 0	RESET	: Reset
KR4 to KR7	: Key returns 4 to 7	V <sub>DD</sub>	: Positive power supply
KRREN	: Key return reset enable	V <sub>SS</sub>	: Ground
P30 to P33	: Port 3	X1 and X2	: System clock (crystal/ceramic)
P60 to P63	: Port 6		

2. BLOCK DIAGRAM





### 3. PIN FUNCTION

#### 3.1 Port Pins

Pin Name	Input/Output	Alternate Function	Function	8-bit I/O	After Reset	I/O Circuit TYPE <small>Note 1</small>
P30	Input/Output	PTO0	Programmable 4-bit input/output port (PORT3). This port can be specified input/output bit-wise. On-chip pull-up resistor connection can be specified by software in 4-bit units.	-	Input	E-B
P31		PTO1				
P32		PTO2				
P33		-				
P60	Input/Output	AVREF	Programmable 4-bit input/output port (PORT6). This port can be specified input/output bit-wise. On-chip pull-up resistor can be specified by software in 4-bit units <sup>Note2</sup> .	-	Input	Ⓕ-A
P61		INT0				
P62		AN0				
P63		AN1				
P70	Input	KR4	Noise eliminator can be selected with P61/INT0. 4-bit input port (PORT7). On-chip pull-up resistor can be specified by software bit-wise.	-	Input	Ⓑ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	Input/Output	-	1-bit input/output port (PORT8). On-chip pull-up resistor connection can be specified by software.	-	Input	Ⓕ-A

**Notes** 1. Circled characters indicate the Schmitt-trigger input.

2. Do not specify an on-chip pull-up resistor connection when using the A/D converter.

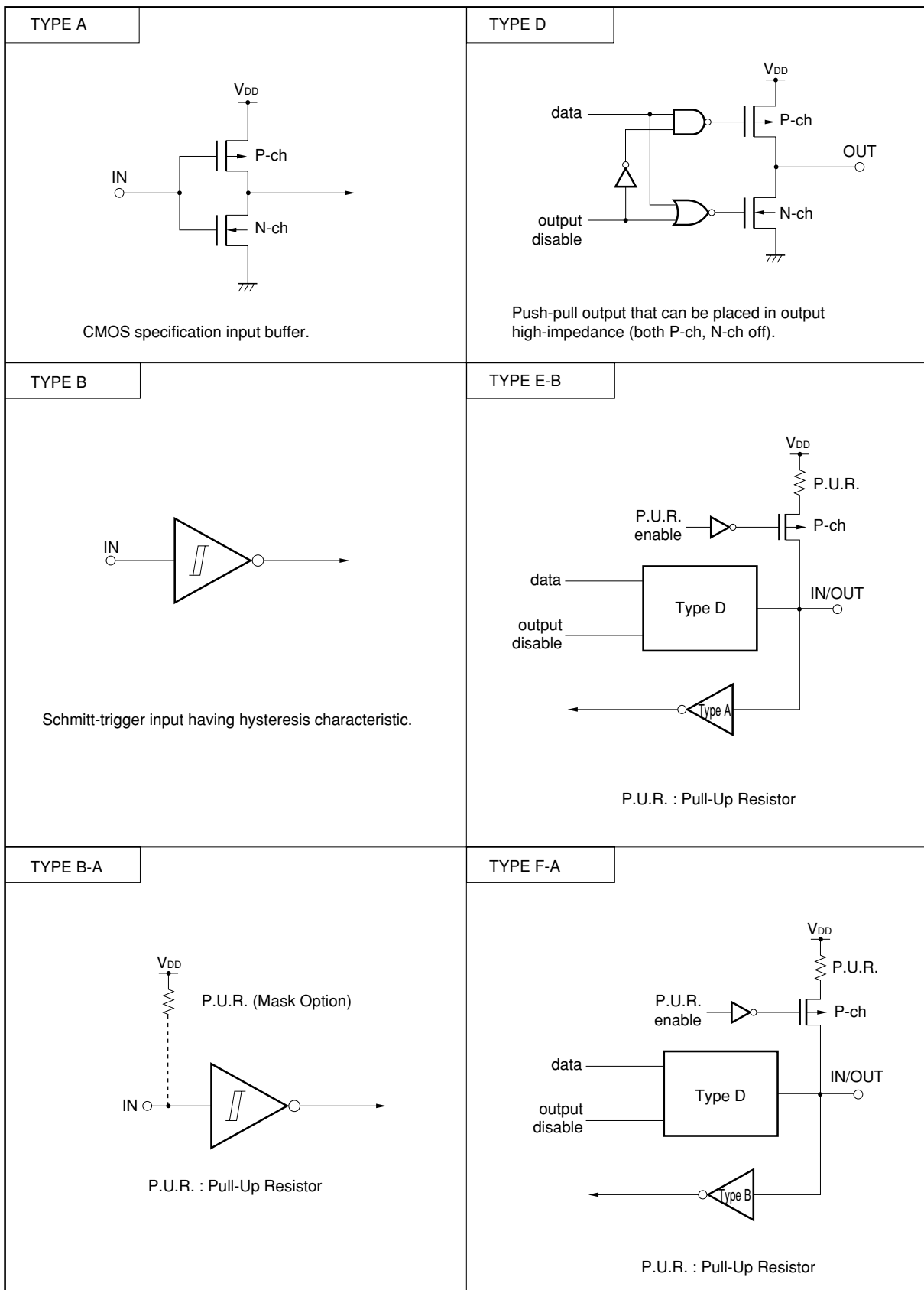
3.2 Non-port Pins

Pin Name	Input/Output	Alternate Function	Function	After Reset	I/O Circuit TYPE <small>Note 1</small>	
PTO0	Output	P30	Timer counter output pins	Input	E-B	
PTO1		P31				
PTO2		P32				
INT0	Input	P61	Edge detection vectored interrupt input pin (detected edge can be selected) Noise elimination circuit can be selected.	Noise elimination circuit can be selected. Asynchronous input	Input	Ⓕ-A
KR4 to KR7	Input	P70 to P73	Falling edge detection testable input pins		Input	Ⓑ-A
AN0	Input	P62	Analog signal input		Input	Ⓕ-A
AN1		P63				
KRREN	Input	–	Key return reset enable pin The reset signal is generated at the falling edge of KRn while KRREN is high in STOP mode.		Input	Ⓑ
AV <sub>REF</sub>	Input	P60	A/D converter reference voltage		Input	Ⓕ-A
X1	Input	–	Crystal/ceramic resonator (for system clock oscillation) connection pin When inputting the external clock, input the external clock to pin X1 and input the inverted phase of the external clock to pin X2.		–	–
X2	–					
RESET	Input	–	System reset input pin (low-level active) Pull-up resistor can be incorporated (mask option).		–	Ⓑ-A
IC	–	–	Internally Connected Connect directly to V <sub>DD</sub> .		–	–
V <sub>DD</sub>	–	–	Positive supply pin		–	–
V <sub>SS</sub>	–	–	Ground potential		–	–

**Note** Circled characters indicate the Schmitt-trigger input.

3.3 Pin Input/Output Circuits

The μPD754264 pin input/output circuits are shown schematically.



## 3.4 Recommended Connection of Unused Pins

Table 3-1. List of Recommended Connection of Unused Pins

Pin	Recommended Connecting Method
P30/PTO0	Input state : Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor. Output state: Leave open.
P31/PTO1	
P32/PTO2	
P33	
P60/AVREF	
P61/INT0	
P62/AN0	
P63/AN1	
P70/KR4	Connect to $V_{DD}$ .
P71/KR5	
P72/KR6	
P73/KR7	
P80	Input state : Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor. Output state: Leave open.
KRREN	When this pin is connected to $V_{DD}$ , internal reset signal is generated at the falling edge of the KRn pin in the STOP mode. When this pin is connected to $V_{SS}$ , internal reset signal is not generated even if the falling edge of KRn pin is detected in the STOP mode.
IC	Connect directly to $V_{DD}$ .

#### 4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

##### 4.1 Difference between Mk I and Mk II Modes

The μPD754264 75XL CPU has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by the bit 3 of the Stack Bank Select register (SBS).

- Mk I mode: Instructions are compatible with the 75X Series. Can be used in the 75XL CPU with a ROM capacity of up to 16 Kbytes.
- Mk II mode: Incompatible with 75X Series. Can be used in all the 75XL CPU's including those products whose ROM capacity is more than 16 Kbytes.

**Table 4-1. Differences between Mk I Mode and Mk II Mode**

	Mk I Mode	Mk II Mode
Number of stack bytes for subroutine instructions	2 bytes	3 bytes
BRA !addr1 instruction CALLA !addr1 instruction	Not available	Available
CALL !addr instruction	3 machine cycles	4 machine cycles
CALLF !faddr instruction	2 machine cycles	3 machine cycles

**Caution** The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL Series. Therefore, this mode is effective for enhancing software compatibility with products that have a program area of more than 16 Kbytes.

With regard to the number of stack bytes during execution of subroutine call instructions, the usable area increases by 1 byte per stack compared to the Mk I mode when the Mk II mode is selected. However, when the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by 1 machine cycle. Therefore, if more emphasis is placed on RAM use efficiency and processing performance than on software compatibility, the Mk I mode should be used.

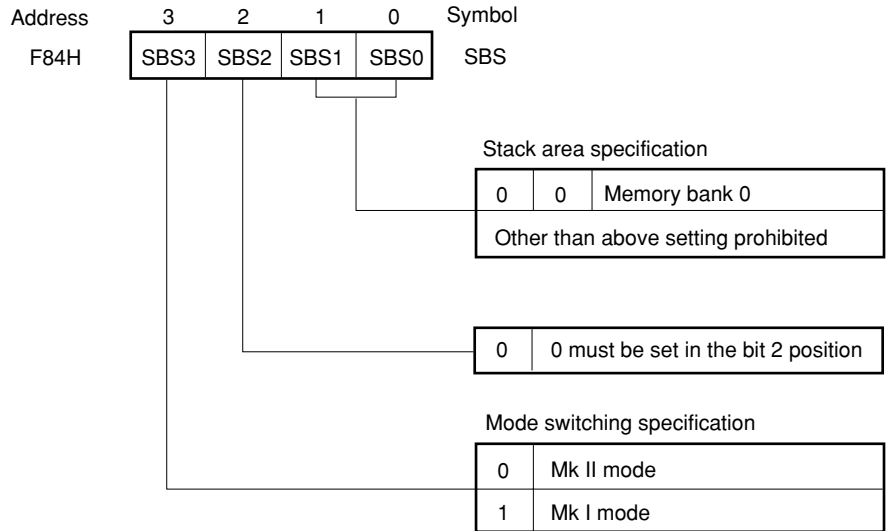
**4.2 Setting Method of Stack Bank Select Register (SBS)**

Switching between the Mk I mode and Mk II mode can be done by the SBS. Figure 4-1 shows the format.

The SBS is set by a 4-bit memory manipulation instruction.

When using the Mk I mode, the SBS must be initialized to 1000B at the beginning of a program. When using the Mk II mode, it must be initialized to 0000B.

**Figure 4-1. Stack Bank Select Register Format**



**Caution** Because SBS. 3 is set to “1” after a  $\overline{\text{RESET}}$  signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to “0” to select the Mk II mode.

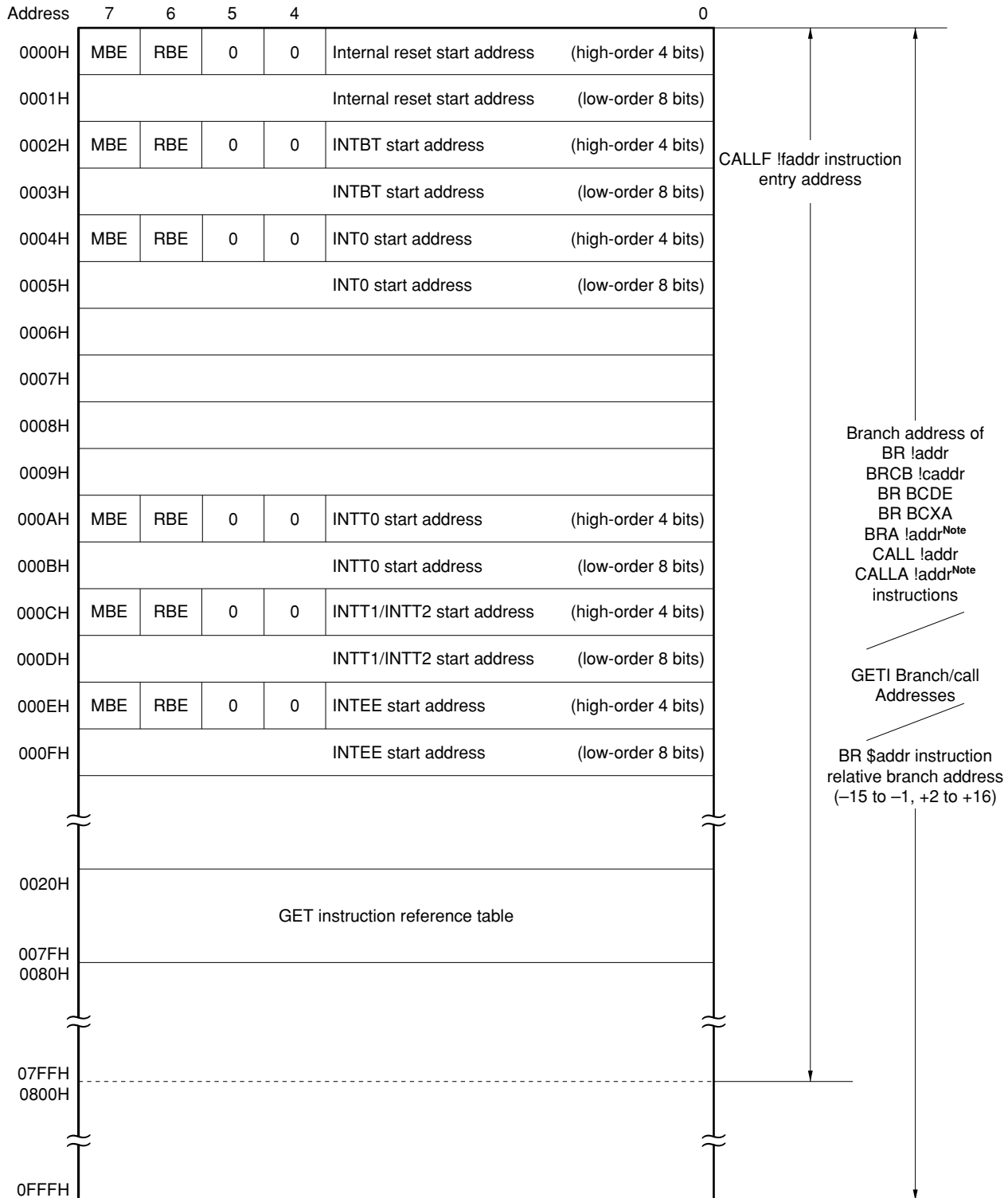
## 5. MEMORY CONFIGURATION

- **Program memory (ROM)** ••• 4096 × 8 bits
  - Addresses 0000H and 0001H  
Vector table wherein the program start address and the values set for the RBE and MBE at the time a  $\overline{\text{RESET}}$  signal is generated are written. Reset and start are possible at an arbitrary address.
  - Addresses 0002H to 000FH  
Vector table wherein the program start address and values set for the RBE and MBE by the vectored interrupts are written. Interrupt service can be started at an arbitrary address.
  - Addresses 0020H to 007FH  
Table area referenced by the GETI instruction<sup>Note</sup>.

**Note** The GETI instruction realizes a 1-byte instruction on behalf of an arbitrary 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the program steps.

- **Data memory**
  - Data area
    - Static RAM ••• 128 words × 4 bits (000H to 07FH)
    - EEPROM ••• 32 words × 8 bits (400H to 43FH)
  - Peripheral hardware area ••• 128 words × 4 bits (F80H to FFFH)

Figure 5-1. Program Memory Map

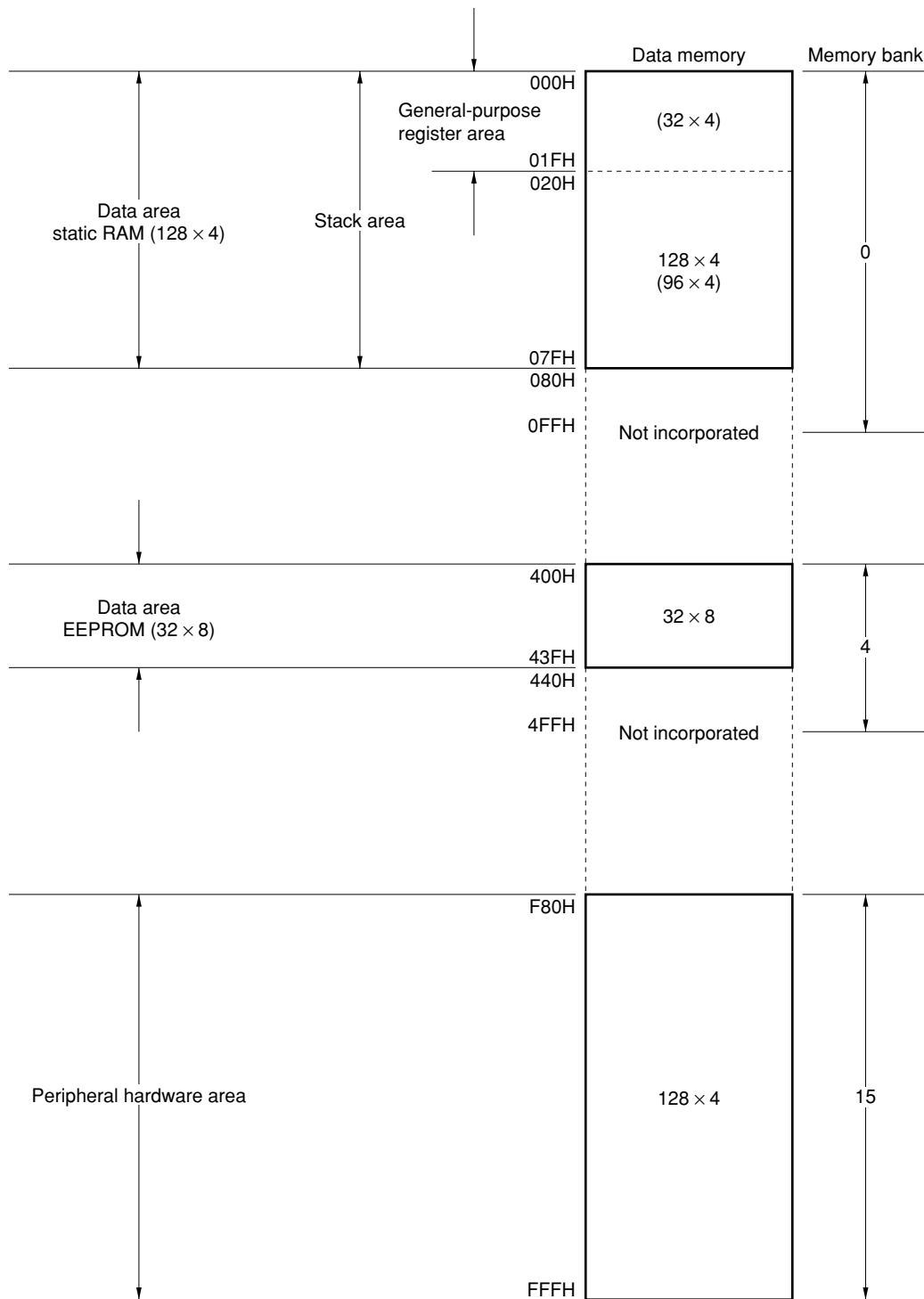


**Note** Can be used in the MkII mode only.

**Remark** In addition to the above, a branch can be made to an address with the low-order 8-bits only of the PC changed by means of a BR PCDE or BR PCXA instruction.



Figure 5-2. Data Memory Map



## 6. EEPROM

The  $\mu$ PD754264 incorporates 32 words  $\times$  8 bit EEPROM (Electrically Erasable PROM) as well as static RAM (128 words  $\times$  4 bit) as a data memory.

The EEPROM incorporated into the  $\mu$ PD754264 has the following features.

- (1) Written data is retained if power is turned off.
- (2) 8-bit data manipulation (auto-erase/auto-write) is available by memory manipulation instruction as well as for static RAM. However available instructions are restricted.
- (3) It can reduce loads of software because the auto-erase and/or auto-write operation is performed by hardware.
- (4) Write operation control using the interrupt request

The interrupt request is generated under following conditions.

- Terminates write operation
- Write status flag

It is possible to check whether enables or disables write operation by bit manipulation instructions.

## 7. PERIPHERAL HARDWARE FUNCTIONS

### 7.1 Digital Input/Output Ports

The following two types of I/O ports are provided.

• CMOS input (Port 7)	:	4
• CMOS I/O (Ports 3, 6, 8)	:	9
<hr/> Total	:	13

**Table 7-1. Types and Features of Digital Ports**

Port Name	Function	Operation and Features	Remarks
PORT3	4-bit I/O	Can be set to input or output mode bit-wise.	Also used as PTO0 to PTO2 pins.
PORT6			Also used as AVREF, INT0, AN0, and AN1 pins.
PORT7	4-bit input	4-bit input only port On-chip pull-up resistor connection can be specified by mask option bit-wise.	Also used as KR4 to KR7 pins.
PORT8	1-bit I/O	Can be set to input or output mode bit wise.	—

### 7.2 Clock Generator

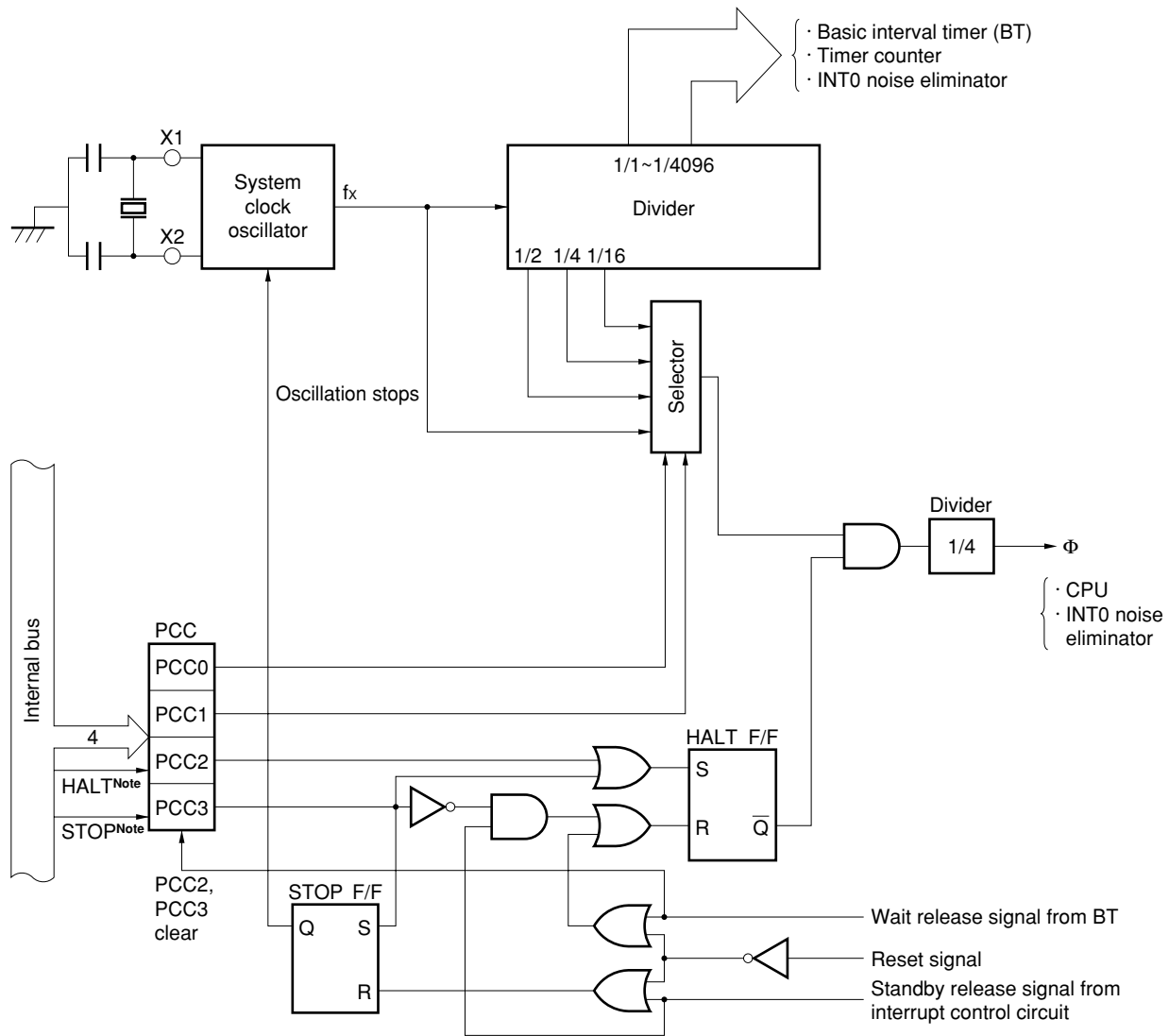
The clock generator provides the clock signals to the CPU and peripheral hardware. Its configuration is shown in Figure 7-1.

The operation of the clock generator is set with the processor clock control register (PCC).

The instruction execution time can be changed.

- 0.95, 1.91, 3.81, 15.3 μs (when the system clock fx operates at 4.19 MHz)
- 0.67, 1.33, 2.67, 10.7 μs (when the system clock fx operates at 6.0 MHz)

Figure 7-1. Clock Generator Block Diagram



**Note** Instruction execution

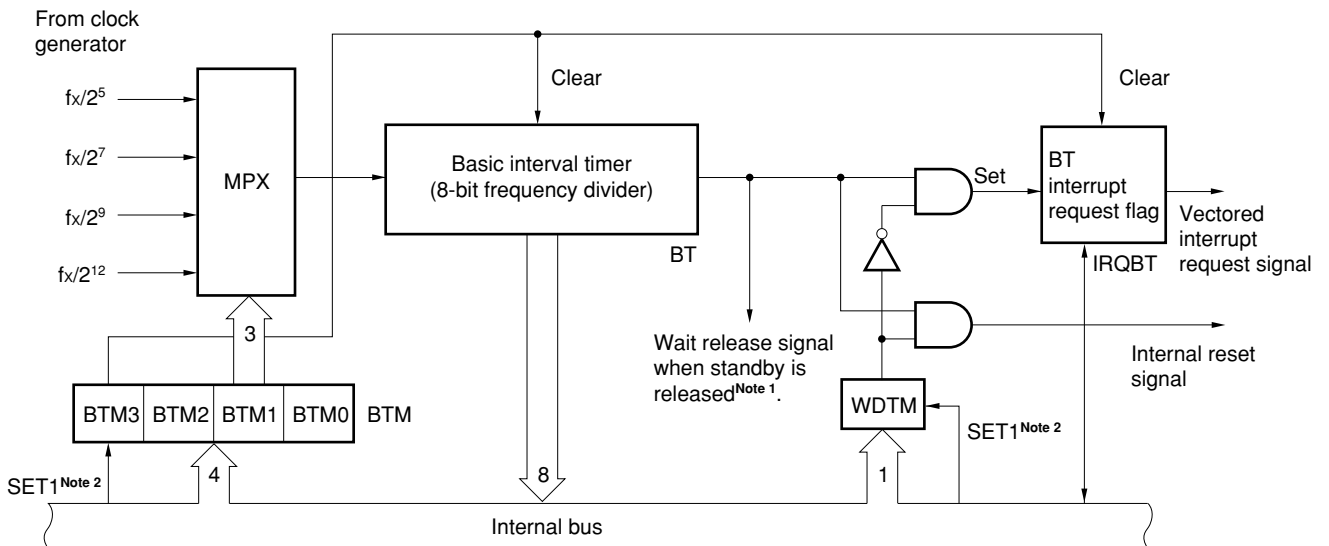
- Remarks**
1.  $f_x$ : System clock frequency
  2. F = CPU clock
  3. PCC: Processor Clock Control Register
  4. One clock cycle ( $t_{CY}$ ) of the CPU clock is equal to one machine cycle of the instruction.

### 7.3 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- (a) Interval timer operation to generate a reference time interrupt
- (b) Watchdog timer operation to detect a runaway of program and reset the CPU
- (c) Selects and counts the wait time when the standby mode is released
- (d) Reads the contents of counting

**Figure 7-2. Basic Interval Timer/Watchdog Timer Block Diagram**



- Notes**
- 1. The wait time can be specified when the standby mode is released.
  - 2. Instruction execution.

**7.4 Timer Counter**

The μPD754264 incorporates three channels of timer counters. Its configuration is shown in Figures 7-3 to 7-5. The timer counter has the following functions.

- (a) Programmable interval timer operation
- (b) Square wave output of any frequency to PTO0-PTO2 pins
- (c) Count value read function

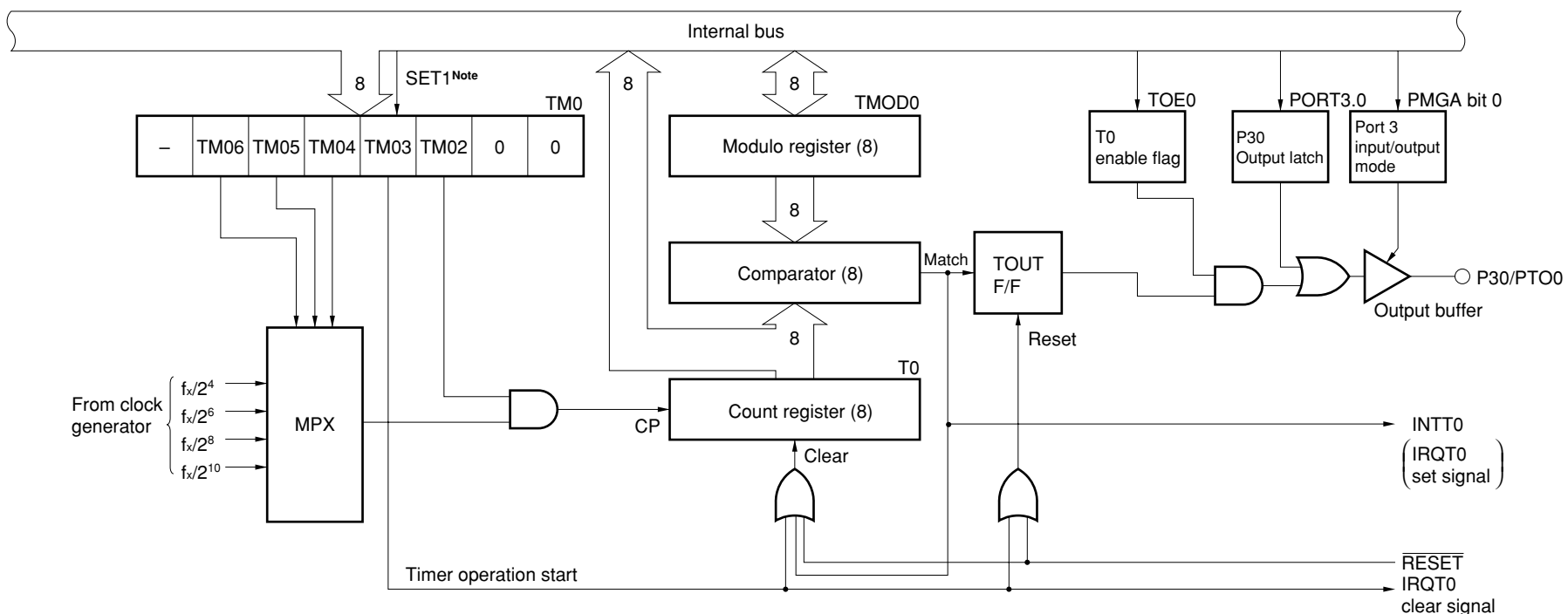
The timer counter can operate in the following four modes as set by the mode register.

**Table 7-2. Mode List**

Mode \ Channel	Channel 0	Channel 1	Channel 2	TM11	TM10	TM21	TM20
8-bit timer counter mode	○	○	○	0	0	0	0
PWM pulse generator mode	×	×	○	0	0	0	1
16-bit timer counter mode	×	○		1	0	1	0
Carrier generator mode	×	○		0	0	1	1

**Remark** ○ : Available  
 × : Not available

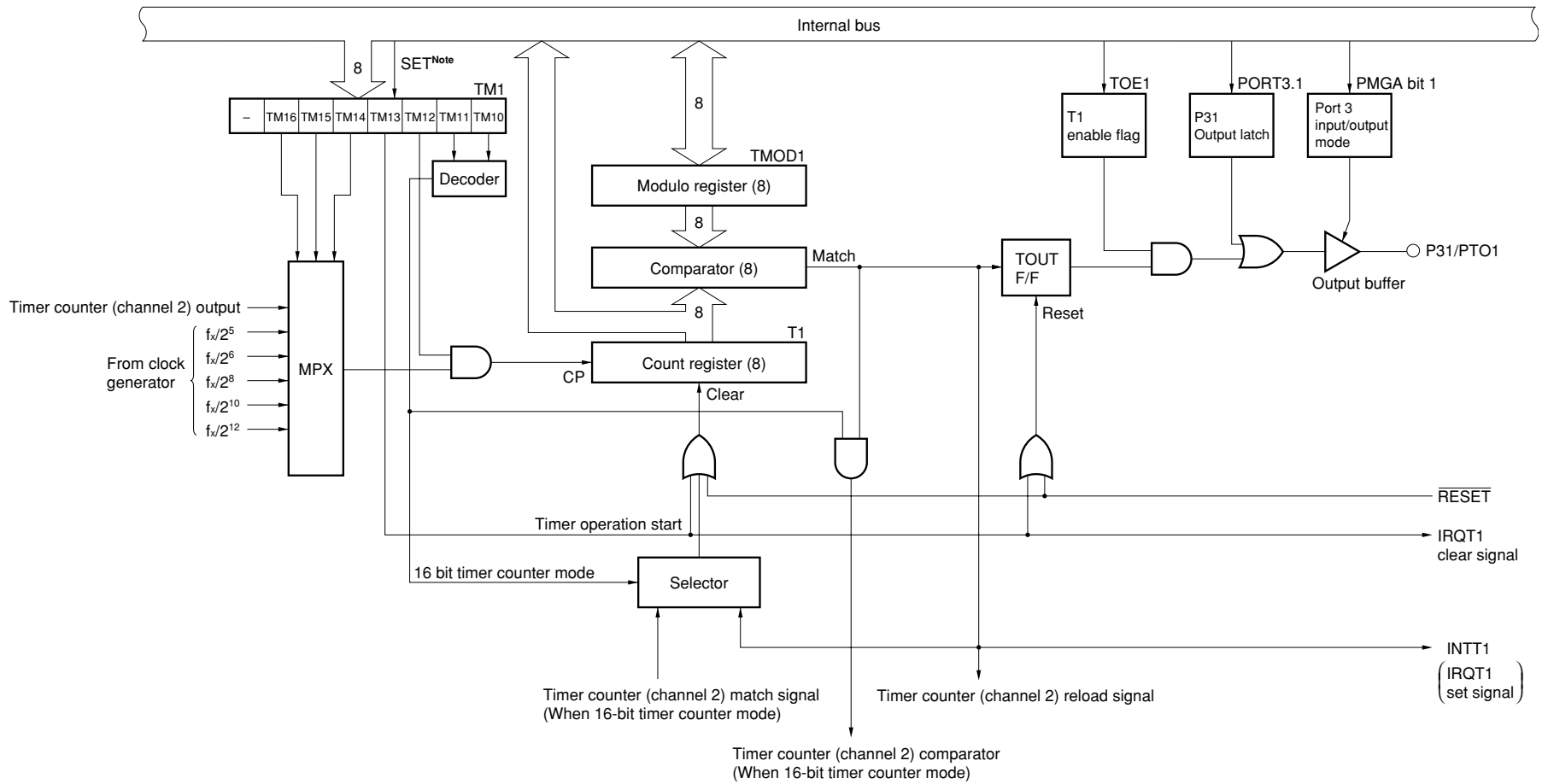
Figure 7-3. Timer Counter (Channel 0) Block Diagram



**Note** Instruction execution

**Caution** When setting data to TM0, be sure to set bits 0 and 1 to 0.

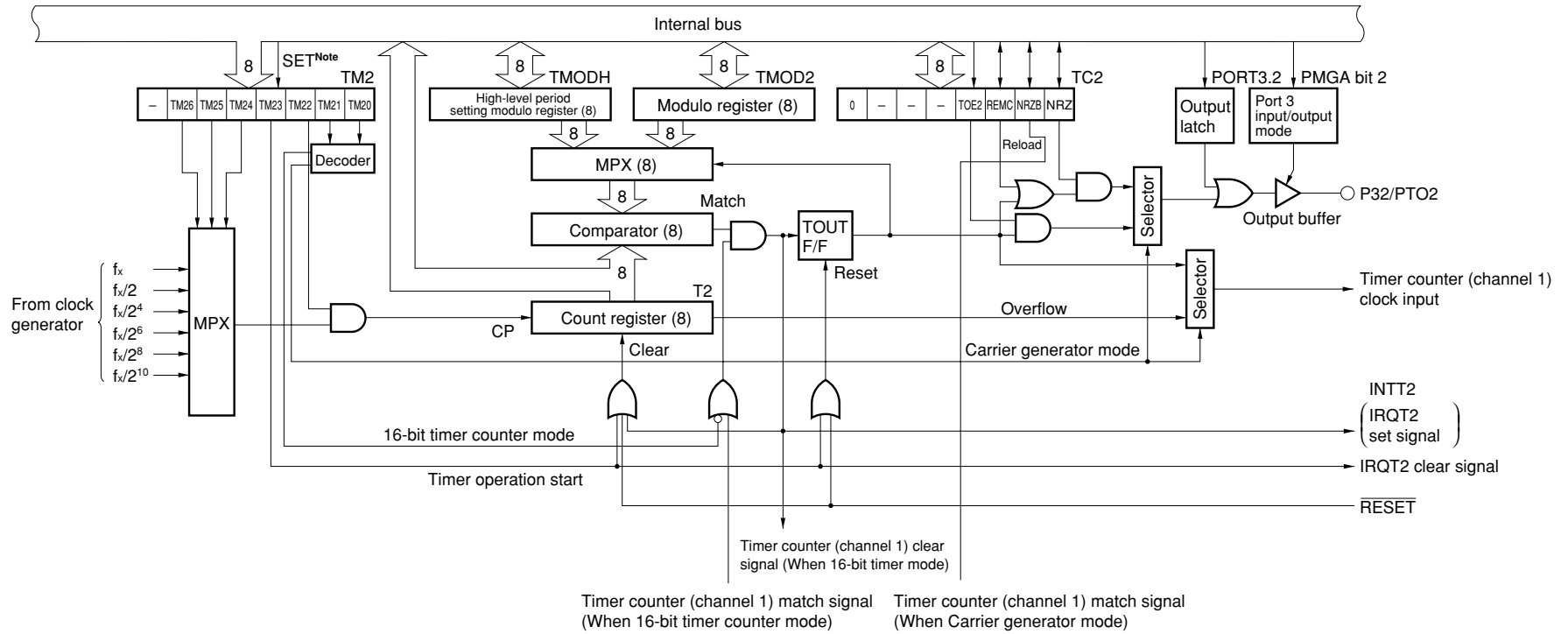
Figure 7-4. Timer Counter (Channel 1) Block Diagram



**Note** Instruction execution



Figure 7-5. Timer Counter (Channel 2) Block Diagram



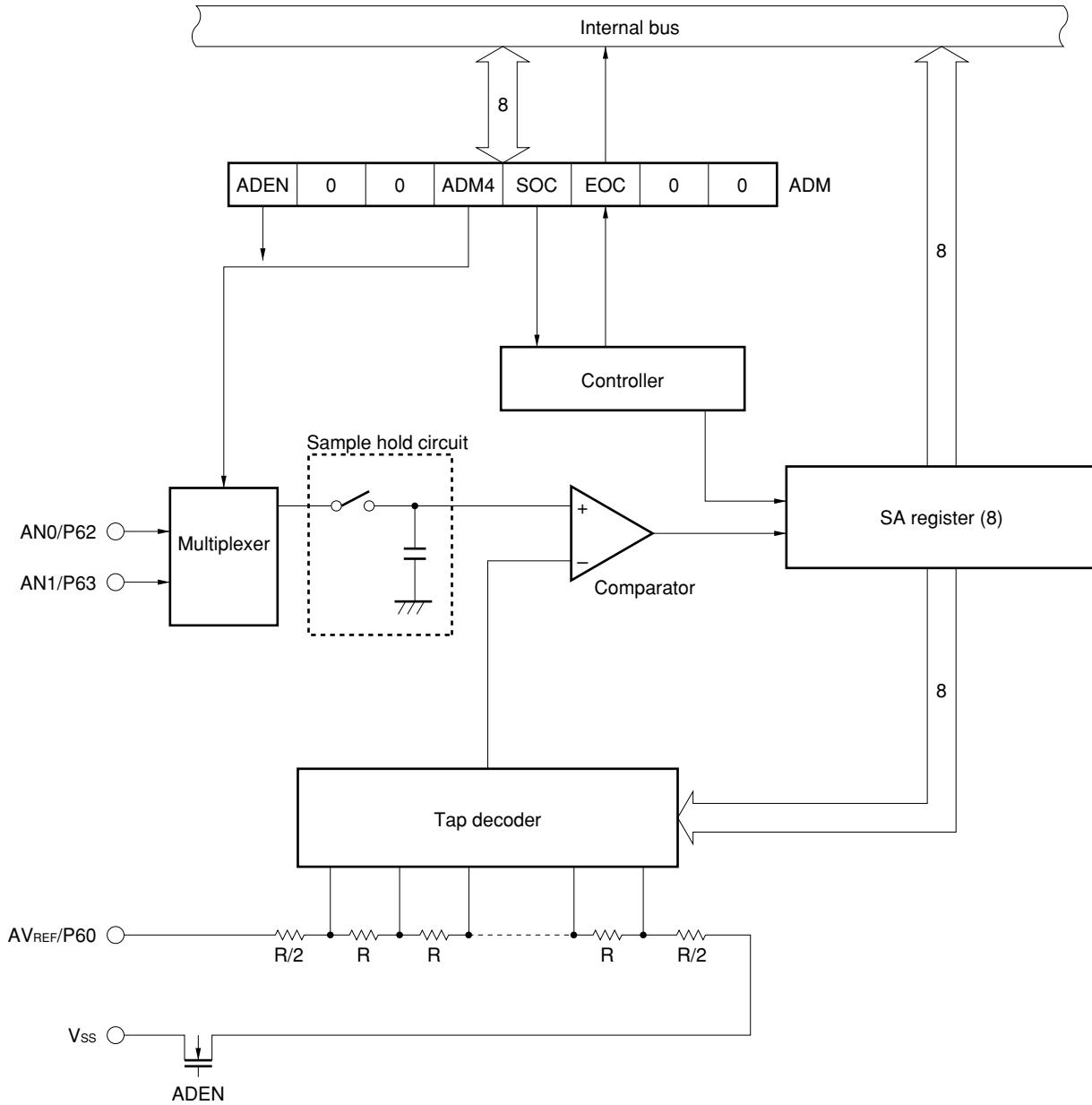
**Note** Instruction execution

**Caution** When setting data to TC2, be sure to set bit 7 to 0.

7.5 A/D Converter

The μPD754264 incorporates an 8-bit resolution A/D converter with 2-channel analog inputs (AN0 and AN1). This A/D converter employs successive approximation.

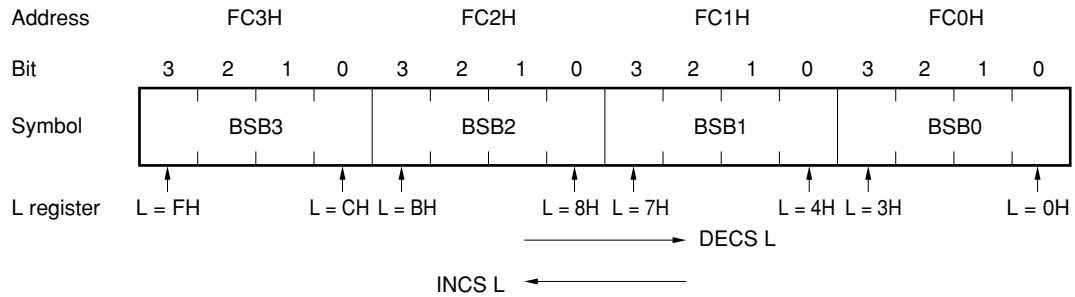
Figure 7-6. A/D Converter Block Diagram



**7.6 Bit Sequential Buffer ..... 16 Bits**

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing large data bit-wise.

**Figure 7-7. Bit Sequential Buffer Format**



- Remarks**
1. In the pmem.@L addressing, the specified bit moves corresponding to the L register.
  2. In the pmem.@L addressing, the BSB can be manipulated regardless of MBE/MSB specification.

## 8. INTERRUPT FUNCTION AND TEST FUNCTION

Figure 8-1 shows the interrupt control circuit. Each hardware device is mapped in the data memory space. The interrupt control circuit of the  $\mu$ PD754264 has the following functions.

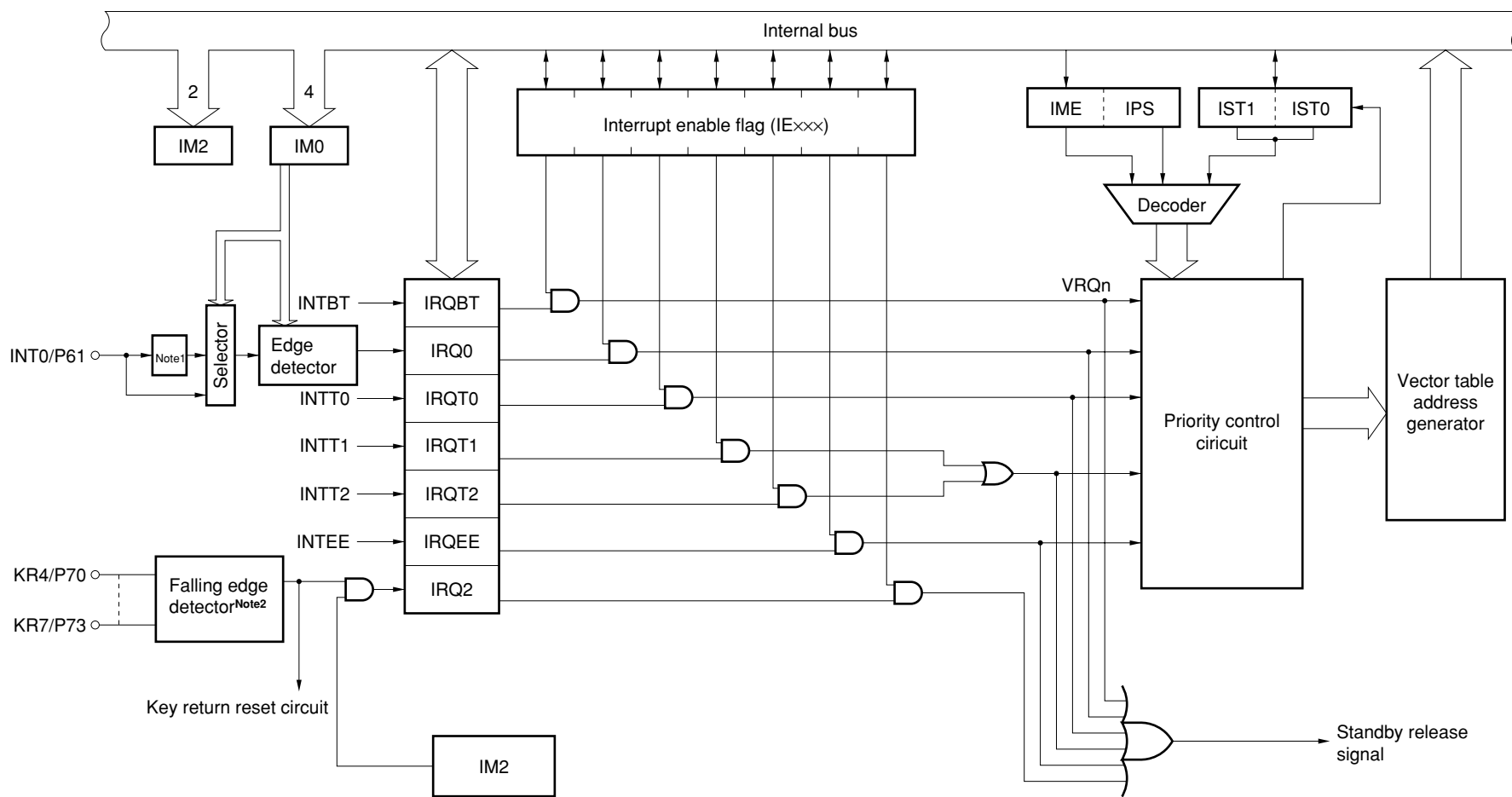
### (1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acknowledgement by the interrupt enable flag (IE $\times\times\times$ ) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQ $\times\times\times$ ). An interrupt generated can be checked by software.
- Release the standby mode. A release interrupt can be selected by the interrupt enable flag.

### (2) Test function

- Test request flag (IRQ2) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

Figure 8-1. Interrupt Control Circuit Block Diagram



**Notes** 1. Noise eliminator (Standby release is disable when noise eliminator is selected.)

2. The INT2 pin is not provided. Interrupt request flag (IRQ2) is set at the KR<sub>n</sub> pin falling edge when IM20 = 1 and IM21 = 0.

9. STANDBY FUNCTION

In order to reduce power dissipation while a program is in a standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD754264.

Table 9-1. Operation Status in Standby Mode

Item \ Mode		STOP Mode	HALT Mode
Set instruction		STOP instruction	HALT instruction
Operation status	Clock generator	Operation stops.	Only the CPU clock $\Phi$ halts (oscillation continues).
	Basic interval timer/ watchdog timer	Operation stops.	Operable BT mode: The IRQBT is set in the basic time interval. WT mode: Reset is generated by the BT overflow.
	Timer counter	Operation stops.	Operable.
	External interrupt	INT0 is not operable. <sup>Note</sup> INT2 is operable during KRn falling period only.	
	CPU	The operation stops.	
Release signal		<ul style="list-style-type: none"> <li>Reset signal</li> <li>Interrupt request signal sent from interrupt enabled peripheral hardware</li> <li>System reset signal (key return reset) generated by KRn falling edge when the KRREN pin = 1</li> </ul>	<ul style="list-style-type: none"> <li>Reset signal</li> <li>Interrupt request signal sent from interrupt enabled peripheral hardware</li> </ul>

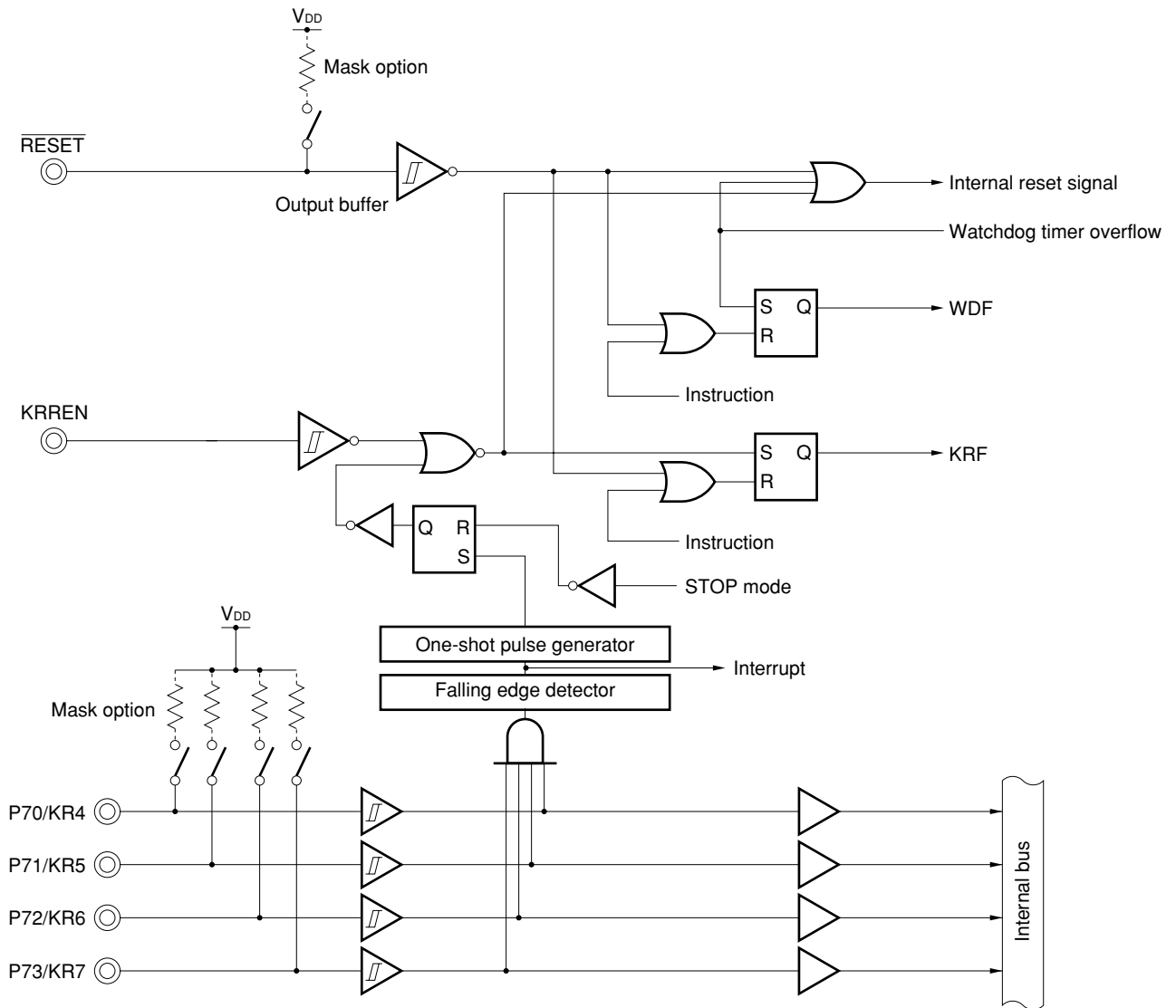
**Note** Can operate only when the noise eliminator is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

## 10. RESET FUNCTION

### 10.1 Configuration and Operation Status of RESET Function

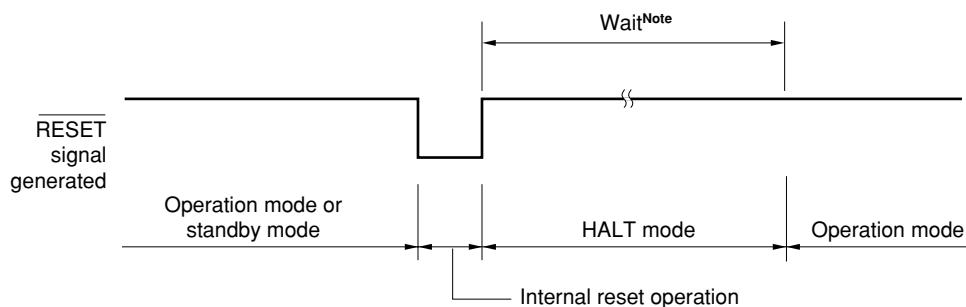
There are three kinds of reset input: the external reset signal ( $\overline{\text{RESET}}$ ), the reset signal sent from the basic interval/watchdog timer, and the reset signal generated by a falling edge signal from KRn in the STOP mode. When any of these reset signals is input, an internal reset signal is generated. The configuration is shown in Figure 10-1.

Figure 10-1. Configuration of Reset Function



Each hardware is initialized by the  $\overline{\text{RESET}}$  signal generation as listed in Table 10-1. Figure 10-2 shows the timing chart of the reset operation.

**Figure 10-2. Reset Operation by  $\overline{\text{RESET}}$  Signal Generation**



**Note** The wait time can be selected from the following three time settings by means of the mask option.

$2^{17}/f_x$  (21.8 ms : @ 6.0-MHz operation, 31.3 ms: @ 4.19-MHz operation)

$2^{15}/f_x$  (5.46 ms : @ 6.0-MHz operation, 7.81 ms: @ 4.19-MHz operation)

$2^{13}/f_x$  (1.37 ms : @ 6.0-MHz operation, 1.95 ms: @ 4.19-MHz operation)



Table 10-1. Hardware Status After Reset (1/3)

Hardware		RESET signal generation in the standby mode	RESET signal generation in operation
Program counter (PC)		Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0.	Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0.
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0, IST1)	0	0
	Bank enable flag (MBE, RBE)	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.
Stack pointer (SP)		Undefined	Undefined
Stack bank select register (SBS)		1000B	1000B
Data memory (RAM)		Held	Undefined
Data memory (EEPROM)		Held <sup>Note 1</sup>	Held <sup>Note 2</sup>
EEPROM write control register (EWC)		0	0
General-purpose register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank select register (MBS, RBS)		0, 0	0, 0
Basic interval timer/watchdog timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
	Watchdog timer enable flag (WDTM)	0	0
Timer counter (channel 0)	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Timer counter (channel 1)	Counter (T1)	0	0
	Modulo register (TMOD1)	FFH	FFH
	Mode register (TM1)	0	0
	TOE1, TOUT F/F	0, 0	0, 0
Timer counter (channel 2)	Counter (T2)	0	0
	Modulo register (TMOD2)	FFH	FFH
	High-level period setting modulo register (TMOD2H)	FFH	FFH
	Mode register (TM2)	0	0
	TOE2, TOUT F/F	0, 0	0, 0
	REMC, NRZ, NRZB	0, 0, 0	0, 0, 0

**Notes** 1. Undefined if STOP mode is entered during an EEPROM write operation. Also undefined if HALT mode is entered during a write operation and a RESET signal is input during a write operation.

2. If a RESET signal is input during an EEPROM write operation, the data at that address is undefined.

**Table 10-1. Hardware Status After Reset (2/3)**

Hardware		RESET signal generation in the standby mode	RESET signal generation in operation
A/D converter	Mode register (ADM)	04H	04H
	SA register (SA)	7FH	7FH
Clock generator	Processor clock control register (PCC)	0	0
Interrupt function	Interrupt request flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt enable flag (IExxx)	0	0
	Interrupt priority selection register (IPS)	0	0
	INT0, 2 mode registers (IM0, IM2)	0, 0	0, 0
Digital port	Output buffer	Off	Off
	Output latch	Cleared (0)	Cleared (0)
	I/O mode registers (PMGA, C)	0	0
	Pull-up resistor setting register (POGA, B)	0	0
Bit sequential buffer (BSB0 to BSB3)		Held	Undefined

**Table 10-1. Hardware Status After Reset (3/3)**

Hardware	RESET signal generation by key return reset	RESET signal generation in the standby mode	RESET signal generation by WDT during operation	RESET signal generation during operation
Watchdog flag (WDF)	Hold the previous status	0	1	0
Key return flag (KRF)	1	0	Hold the previous status	0

**10.2 Watchdog Flag (WDF), Key Return Flag (KRF)**

The WDF is cleared by a watchdog timer overflow signal, and the KRF is set by a reset signal generated by the KRn pins. As a result, by checking the contents of WDF and KRF, it is possible to know what kind of reset signal is generated.

As the WDF and KRF are cleared only by external signal or instruction execution, if once these flags are set, they are not cleared until an external signal is generated or a clear instruction is executed. Check and clear the contents of WDF and KRF after reset start operation by executing SKTCLR instruction and so on.

Table 10-2 lists the contents of WDF and KRF corresponding to each signal. Figure 10-3 shows the WDF operation in generating each signal, and Figure 10-4 shows the KRF operation in generating each signal.

**Table 10-2. WDF and KRF Contents Correspond to Each Signal**

Hardware	External $\overline{\text{RESET}}$ signal generation	Reset signal generation by watchdog timer overflow	Reset signal generation by the KRn input	WDF clear instruction execution	KRF clear instruction execution
Watchdog flag (WDF)	0	1	Hold	0	Hold
Key return flag (KRF)	0	Hold	1	Hold	0

**Figure 10-3. WDF Operation in Generating Each Signal**

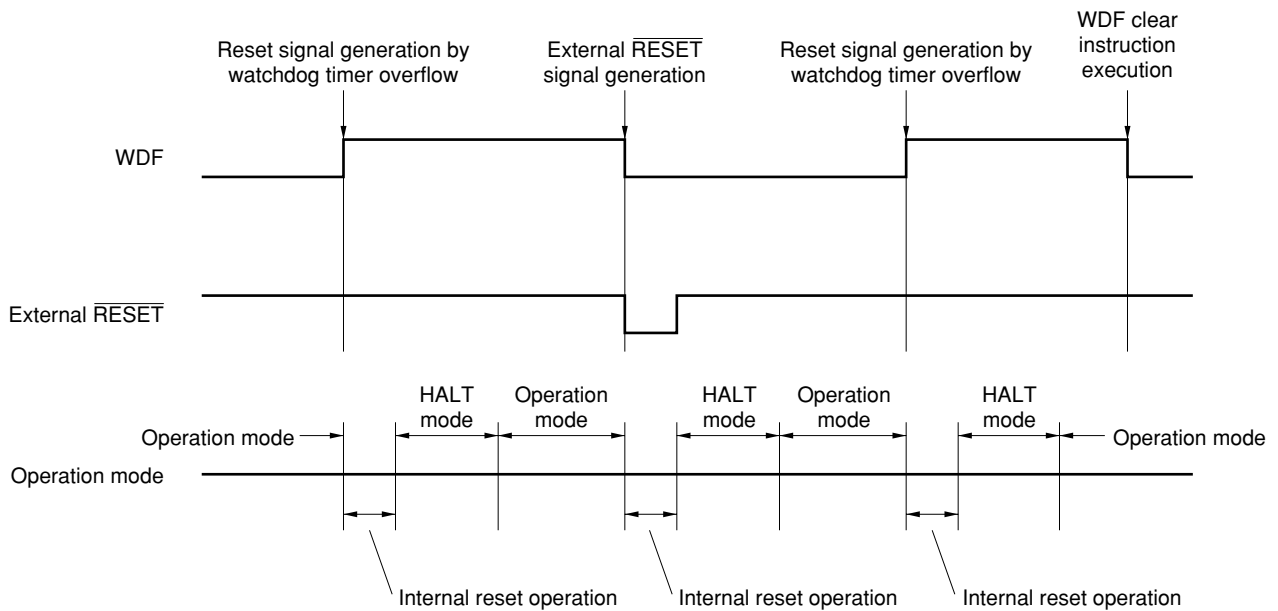
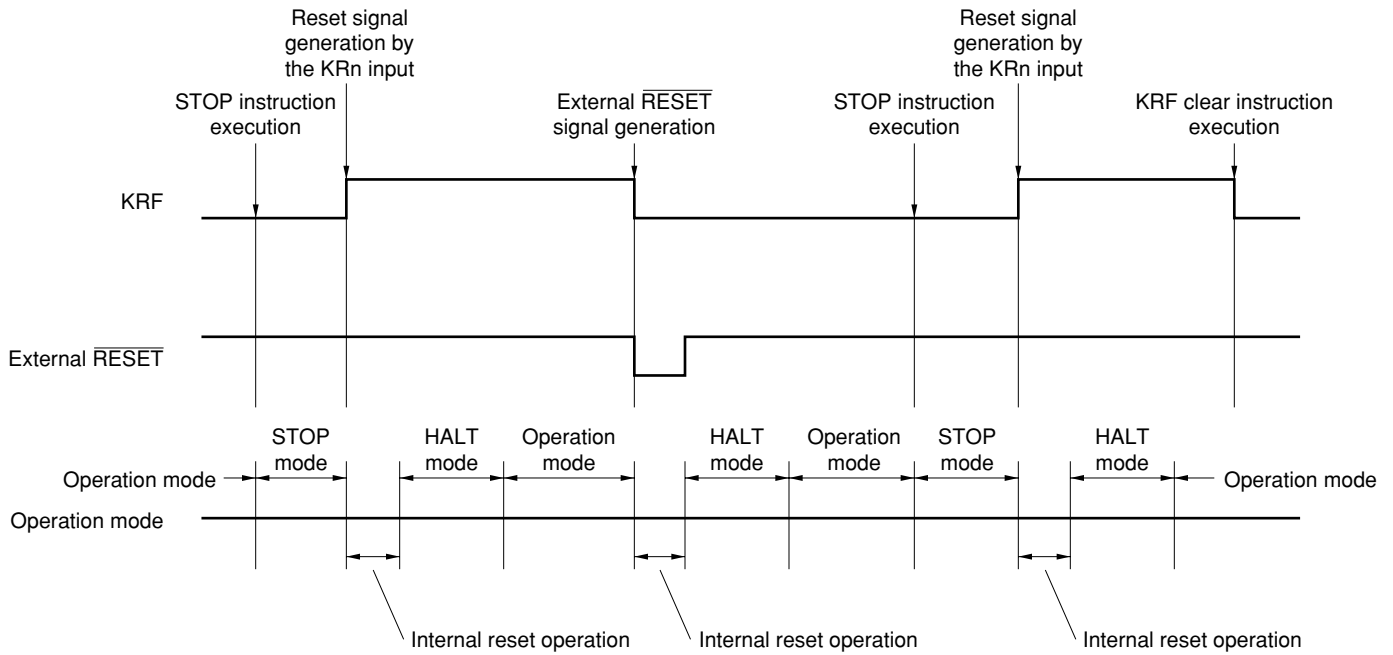


Figure 10-4. KRF Operation in Generating Each Signal



## 11. MASK OPTION

The  $\mu$ PD754264 has the following mask options:

- Mask option of P70/KR4 to P73/KR7  
On-chip pull-up resistor connection can be specified for these pins.  
<1> Do not connect an on-chip pull-up resistor  
<2> Connect the 30-k $\Omega$  (typ.) pull-up resistor bit-wise
- Mask option of  $\overline{\text{RESET}}$  pin  
On-chip pull-up resistor connection can be specified for this pin.  
<1> Do not connect an on-chip pull-up resistor  
<2> Connect the 100-k $\Omega$  (typ.) pull-up resistor
- Standby function mask option  
The wait time when the  $\overline{\text{RESET}}$  signal is input can be selected.  
<1>  $2^{17}/f_x$  (21.8 ms: @  $f_x = 6.0\text{-MHz}$  operation, 31.3 ms: @  $f_x = 4.19\text{-MHz}$  operation)  
<2>  $2^{15}/f_x$  (5.46 ms: @  $f_x = 6.0\text{-MHz}$  operation, 7.81 ms: @  $f_x = 4.19\text{-MHz}$  operation)  
<3>  $2^{13}/f_x$  (1.37 ms: @  $f_x = 6.0\text{-MHz}$  operation, 1.95 ms: @  $f_x = 4.19\text{-MHz}$  operation)

12. INSTRUCTION SETS

(1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to “**RA75X ASSEMBLER PACKAGE USERS’ MANUAL — LANGUAGE (EEU-1367)**”. If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers and labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the registers can be described. However, there are restrictions in the labels that can be described for fmem and pmem. For details, refer to “**μPD754264 user’s manual (U12287E)**”.

Expression format	Description method
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label <sup>Note</sup> 2-bit immediate data or label
fmem pmem	FB0H-FBFH, FF0H-FFFH immediate data or label FC0H-FFFH immediate data or label
addr addr1 caddr faddr	000H-FFFH immediate data or label 000H-FFFH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H-7FH immediate data (where bit 0 = 0) or label
PORTn IExxx RBn MBn	PORT3, 6, 7, 8 IEBT, IET0-IET2, IE0, IE2, IE4E RB0-RB3 MB0, MB4, MB15

**Note** mem can be only used for even address in 8-bit data processing.

**(2) Legend in explanation of operation**

A	: A register, 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: XA register pair; 8-bit accumulator
BC	: BC register pair
DE	: DE register pair
HL	: HL register pair
XA'	: XA' extended register pair
BC'	: BC' extended register pair
DE'	: DE' extended register pair
HL'	: HL' extended register pair
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag, bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORT <sub>n</sub>	: Port n (n = 3, 6, 7, 8)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IE <sub>xxx</sub>	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Separation between address and bit
(xx)	: The contents addressed by xx
xxH	: Hexadecimal data

(3) Explanation of symbols under addressing area column

*1	MB = MBE•MBS (MBS = 0, 4, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS (MBS = 0, 4, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 000H to FFFH	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16 addr1 = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 000H to FFFH	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	
*11	addr1 = 000H to FFFH	

- Remarks**
1. MB indicates memory bank that can be accessed.
  2. In \*2, MB = 0 independently of how MBE and MBS are set.
  3. In \*4 and \*5, MB = 15 independently of how MBE and MBS are set.
  4. \*6 to \*11 indicate the areas that can be addressed.

(4) Explanation of number of machine cycles column

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction<sup>Note</sup>: S = 2

**Note** 3-byt-e instruction: BR !addr, BRA !addr1, CALL !addr, or CALLA !addr1 instruction

**Caution** The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle of CPU clock (= tcy); time can be selected from among four types by setting PCC.



Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Transfer instruction	MOV	A, #n4	1	1	$A \leftarrow n4$		String effect A
		reg1, #n4	2	2	$reg1 \leftarrow n4$		
		XA, #n8	2	2	$XA \leftarrow n8$		String effect A
		HL, #n8	2	2	$HL \leftarrow n8$		String effect B
		rp2, #n8	2	2	$rp2 \leftarrow n8$		
		A, @HL	1	1	$A \leftarrow (HL)$	*1	
		A, @HL+	1	2+S	$A \leftarrow (HL)$ , then $L \leftarrow L+1$	*1	L = 0
		A, @HL-	1	2+S	$A \leftarrow (HL)$ , then $L \leftarrow L-1$	*1	L = FH
		A, @rpa1	1	1	$A \leftarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftarrow (HL)$	*1	
		@HL, A	1	1	$(HL) \leftarrow A$	*1	
		@HL, XA	2	2	$(HL) \leftarrow XA$	*1	
		A, mem	2	2	$A \leftarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftarrow (mem)$	*3	
		mem, A	2	2	$(mem) \leftarrow A$	*3	
		mem, XA	2	2	$(mem) \leftarrow XA$	*3	
		A, reg	2	2	$A \leftarrow reg$		
		XA, rp'	2	2	$XA \leftarrow rp'$		
		reg1, A	2	2	$reg1 \leftarrow A$		
		rp'1, XA	2	2	$rp'1 \leftarrow XA$		
	XCH	A, @HL	1	1	$A \leftrightarrow (HL)$	*1	
		A, @HL+	1	2+S	$A \leftrightarrow (HL)$ , then $L \leftarrow L+1$	*1	L = 0
		A, @HL-	1	2+S	$A \leftrightarrow (HL)$ , then $L \leftarrow L-1$	*1	L = FH
		A, @rpa1	1	1	$A \leftrightarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftrightarrow (HL)$	*1	
		A, mem	2	2	$A \leftrightarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftrightarrow (mem)$	*3	
		A, reg1	1	1	$A \leftrightarrow reg1$		
XA, rp'		2	2	$XA \leftrightarrow rp'$			
Table reference instructions	MOVT	XA, @PCDE	1	3	$XA \leftarrow (PC_{11-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	$XA \leftarrow (PC_{11-8}+XA)_{ROM}$		
		XA, @BCDE	1	3	$XA \leftarrow (BCDE)_{ROM}^{Note}$	*6	
		XA, @BCXA	1	3	$XA \leftarrow (BCXA)_{ROM}^{Note}$	*6	

**Note** Set "0" in register B.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Bit transfer instructions	MOV1	CY, fmem.bit	2	2	$CY \leftarrow (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow (pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow (H+mem_{3-0}.bit)$	*1	
		fmem.bit, CY	2	2	$(fmem.bit) \leftarrow CY$	*4	
		pmem.@L, CY	2	2	$(pmem_{7-2}+L_{3-2}.bit(L_{1-0})) \leftarrow CY$	*5	
		@H+mem.bit, CY	2	2	$(H+mem_{3-0}.bit) \leftarrow CY$	*1	
Operation instructions	ADDS	A, #n4	1	1+S	$A \leftarrow A+n4$		carry
		XA, #n8	2	2+S	$XA \leftarrow XA+n8$		carry
		A, @HL	1	1+S	$A \leftarrow A+(HL)$	*1	carry
		XA, rp'	2	2+S	$XA \leftarrow XA+rp'$		carry
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1+XA$		carry
	ADDC	A, @HL	1	1	$A, CY \leftarrow A+(HL)+CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA+rp'+CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1+XA+CY$		
	SUBS	A, @HL	1	1+S	$A \leftarrow A-(HL)$	*1	borrow
		XA, rp'	2	2+S	$XA \leftarrow XA-rp'$		borrow
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1-XA$		borrow
	SUBC	A, @HL	1	1	$A, CY \leftarrow A-(HL)-CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA-rp'-CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1-XA-CY$		
	AND	A, #n4	2	2	$A \leftarrow A \wedge n4$		
		A, @HL	1	1	$A \leftarrow A \wedge (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \wedge rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \wedge XA$		
	OR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \vee rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$		
	XOR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
XA, rp'		2	2	$XA \leftarrow XA \vee rp'$			
rp'1, XA		2	2	$rp'1 \leftarrow rp'1 \vee XA$			
Accumulator manipulation instructions	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \bar{A}$		

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Increment and Decrement instructions	INCS	reg	1	1+S	reg ← reg+1		reg=0
		rp1	1	1+S	rp1 ← rp1+1		rp1=00H
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL)=0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem)=0
	DECS	reg	1	1+S	reg ← reg-1		reg=FFH
		rp'	2	2+S	rp' ← rp'-1		rp'=FFH
Comparison instruction	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg=n4
		@HL, #n4	1	2+S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	2	1+S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2+S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2+S	Skip if A = reg		A=reg
		XA, rp'	2	2+S	Skip if XA = rp'		XA=rp'
Carry flag manipulation instruction	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY=1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory bit manipulation instructions	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> )) ← 1	*5	
		@H+mem.bit	2	2	(H+mem <sub>3-0</sub> .bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> )) ← 0	*5	
		@H+mem.bit	2	2	(H+mem <sub>3-0</sub> .bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit)=1	*3	(mem.bit)=1
		fmem.bit	2	2+S	Skip if (fmem.bit)=1	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))=1	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if (H+mem <sub>3-0</sub> .bit)=1	*1	(@H+mem.bit)=1
	SKF	mem.bit	2	2+S	Skip if (mem.bit)=0	*3	(mem.bit)=0
		fmem.bit	2	2+S	Skip if (fmem.bit)=0	*4	(fmem.bit)=0
		pmem.@L	2	2+S	Skip if (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))=0	*5	(pmem.@L)=0
		@H+mem.bit	2	2+S	Skip if (H+mem <sub>3-0</sub> .bit)=0	*1	(@H+mem.bit)=0

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition	
Memory bit manipulation instructions	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit)=1 and clear	*4	(fmem.bit)=1	
		pmem.@L	2	2+S	Skip if (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))=1 and clear	*5	(pmem.@L)=1	
		@H+mem.bit	2	2+S	Skip if (H+mem <sub>3-0</sub> .bit)=1 and clear	*1	(@H+mem.bit)=1	
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4		
		CY, pmem.@L	2	2	CY ← CY ∧ (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))	*5		
		CY, @H+mem.bit	2	2	CY ← CY ∧ (H+mem <sub>3-0</sub> .bit)	*1		
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4		
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))	*5		
		CY, @H+mem.bit	2	2	CY ← CY ∨ (H+mem <sub>3-0</sub> .bit)	*1		
	XOR1	CY, fmem.bit	2	2	CY ← CY ⊕ (fmem.bit)	*4		
		CY, pmem.@L	2	2	CY ← CY ⊕ (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))	*5		
		CY, @H+mem.bit	2	2	CY ← CY ⊕ (H+mem <sub>3-0</sub> .bit)	*1		
Branch instructions	BR <sup>Note 1</sup>	addr	–	–	PC <sub>11-0</sub> ← addr ( Select appropriate instruction among BR !addr BRCB !caddr, and BR \$addr according to the assembler being used. )	*6		
		addr1	–	–	PC <sub>11-0</sub> ← addr ( Select appropriate instruction among BR !addr BRA !addr1, BRCB !caddr and BR \$addr1 according to the assembler being used. )	*11		
		! addr	3	3	PC <sub>11-0</sub> ← addr	*6		
		\$addr	1	2	PC <sub>11-0</sub> ← addr	*7		
		\$addr1	1	2	PC <sub>11-0</sub> ← addr1			
		PCDE	2	3	PC <sub>11-0</sub> ← PC <sub>11-8</sub> +DE			
		PCXA	2	3	PC <sub>11-0</sub> ← PC <sub>11-8</sub> +XA			
		BCDE	2	3	PC <sub>11-0</sub> ← BCDE <sup>Note 2</sup>	*6		
		BCXA	2	3	PC <sub>11-0</sub> ← BCXA <sup>Note 2</sup>	*6		
		BRA <sup>Note 1</sup>	!addr1	3	3	PC <sub>11-0</sub> ← addr1	*11	
		BRCB	!caddr	2	2	PC <sub>11-0</sub> ← caddr <sub>11-0</sub>	*8	

- Notes** 1. The above operations in the double boxes can be performed only in the Mk II mode.  
 2. "0" must be set to B register.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Subroutine stack control instructions	CALLA <sup>Note</sup>	!addr1	3	3	(SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC <sub>11-0</sub> (SP-5) ← 0, 0, 0 PC <sub>11-0</sub> ← addr1, SP ← SP-6	*11	
	CALL <sup>Note</sup>	!addr	3	3	(SP-3) ← MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) ← PC <sub>11-0</sub> PC <sub>11-0</sub> ← addr, SP ← SP-4	*6	
				4	(SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC <sub>11-0</sub> (SP-5) ← 0, 0, 0 PC <sub>11-0</sub> ← addr, SP ← SP-6		
	CALLF <sup>Note</sup>	!faddr	2	2	(SP-3) ← MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) ← PC <sub>11-0</sub> PC <sub>11-0</sub> ← 0+faddr, SP ← SP-4	*9	
				3	(SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC <sub>11-0</sub> (SP-5) ← 0, 0, 0 PC <sub>11-0</sub> ← 0+faddr, SP ← SP-6		
	RET <sup>Note</sup>		1	3	PC <sub>11-0</sub> ← (SP) (SP+3) (SP+2) MBE, RBE, 0, 0 ← (SP+1), SP ← SP+4		
					x, x, MBE, RBE ← (SP+4) 0, 0, 0, 0 ← (SP+1) PC <sub>11-0</sub> ← (SP) (SP+3) (SP+2), SP ← SP+6		
	RETS <sup>Note</sup>		1	3+S	MBE, RBE, 0, 0 ← (SP+1) PC <sub>11-0</sub> ← (SP) (SP+3) (SP+2) SP ← SP+4 then skip unconditionally		Unconditional
					0, 0, 0, 0 ← (SP+1) PC <sub>11-0</sub> ← (SP) (SP+3) (SP+2) x, x, MBE, RBE ← (SP+4) SP ← SP+6 then skip unconditionally		
	RETJ <sup>Note</sup>		1	3	MBE, RBE, 0, 0 ← (SP+1) PC <sub>11-0</sub> ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6		
0, 0, 0, 0 ← (SP+1) PC <sub>11-0</sub> ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6							
PUSH	rp		1	1	(SP-1) (SP-2) ← rp, SP ← SP-2		
	BS		2	2	(SP-1) ← MBS, (SP-2) ← RBS, SP ← SP-2		
POP	rp		1	1	rp ← (SP+1) (SP), SP ← SP+2		
	BS		2	2	MBS ← (SP+1), RBS ← (SP), SP ← SP+2		

**Note** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition	
Interrupt control instructions	EI		2	2	IME (IPS.3) ← 1			
		IE <sub>xxx</sub>	2	2	IE <sub>xxx</sub> ← 1			
	DI		2	2	IME (IPS.3) ← 0			
		IE <sub>xxx</sub>	2	2	IE <sub>xxx</sub> ← 0			
Input/output instructions	IN <sup>Note 1</sup>	A, PORT <sub>n</sub>	2	2	A ← PORT <sub>n</sub> (n = 3, 6, 7, 8)			
	OUT <sup>Note 1</sup>	PORT <sub>n</sub> , A	2	2	PORT <sub>n</sub> ← A (n = 3, 6, 8)			
CPU control instructions	HALT		2	2	Set HALT Mode (PCC.2 ← 1)			
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)			
	NOP		1	1	No Operation			
Special instructions	SEL	RB <sub>n</sub>	2	2	RBS ← n (n = 0-3)			
		MB <sub>n</sub>	2	2	MBS ← n (n = 0, 4, 15)			
	GETI <sup>Notes 2, 3</sup>	taddr	1	3	<ul style="list-style-type: none"> <li>When TBR instruction PC<sub>11-0</sub> ← (taddr)<sub>3-0</sub> + (taddr+1)</li> </ul>	*10		
					<ul style="list-style-type: none"> <li>When TCALL instruction (SP-4) (SP-1) (SP-2) ← PC<sub>11-0</sub> (SP-3) ← MBE, RBE, 0, 0 PC<sub>11-0</sub> ← (taddr)<sub>3-0</sub> + (taddr+1) SP ← SP-4</li> </ul>			
					<ul style="list-style-type: none"> <li>When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.</li> </ul>			Depending on the reference instruction
					<ul style="list-style-type: none"> <li>When TBR instruction PC<sub>11-0</sub> ← (taddr)<sub>3-0</sub> + (taddr+1)</li> </ul>			*10
<ul style="list-style-type: none"> <li>When TCALL instruction (SP-6) (SP-3) (SP-4) ← PC<sub>11-0</sub> (SP-5) ← 0, 0, 0, 0 (SP-2) ← x, x, MBE, RBE PC<sub>11-0</sub> ← (taddr)<sub>3-0</sub> + (taddr+1) SP ← SP-6</li> </ul>								
<ul style="list-style-type: none"> <li>When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.</li> </ul>	Depending on the reference instruction							

- Notes**
1. While the IN instruction and OUT instruction are being executed, MBE must be set to 0, or MBE must be set to 1 and MBS must be set to 15.
  2. The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.
  3. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

13. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

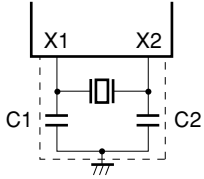
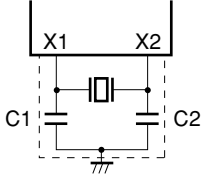
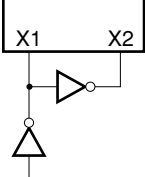
Parameter	Symbol	Test Conditions		Ratings	Unit
Power supply voltage	V <sub>DD</sub>			-0.3 to +7.0	V
Input voltage	V <sub>I</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>O</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
Output current, high	I <sub>OH</sub>	Per pin	P30, P31, P33, P60 to P63, P80	-10	mA
			P32	-20	mA
		For all pins		-30	mA
Output current, low	I <sub>OL</sub> <sup>Note</sup>	Per pin		20	mA
		For all pins		90	mA
Operating ambient temperature	T <sub>A</sub>			-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Caution** If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	f = 1 MHz Unmeasured pins returned to 0 V			15	pF
Output capacitance	C <sub>OUT</sub>				15	pF
I/O capacitance	C <sub>IO</sub>				15	pF

**System Clock Oscillator Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 6.0 V)**

Resonator	Recommended Constant	Parameter	Testing Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note1</sup>		1.0		6.0 <sup>Notes2, 3, 4</sup>	MHz
		Oscillation stabilization time <sup>Note5</sup>	After V <sub>DD</sub> reaches MIN. value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note1</sup>		1.0		6.0 <sup>Notes2, 3, 4</sup>	MHz
		Oscillation stabilization time <sup>Note3</sup>	V <sub>DD</sub> = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f <sub>x</sub> ) <sup>Note1</sup>		1.0		6.0 <sup>Notes2, 3, 4</sup>	MHz
		X1 input high- and low-level widths (t <sub>xH</sub> , t <sub>xL</sub> )		83.3		500	ns

**Notes** 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

- If the oscillation frequency is 2.1 MHz < f<sub>x</sub> ≤ 4.19 MHz at 1.8 V ≤ V<sub>DD</sub> < 2.0 V, set the processor control register (PCC) to a value other than 0011. If the PCC is set to 0011, the rated machine cycle time of 1.9 μs is not satisfied.
- If the oscillation frequency is 4.19 MHz < f<sub>x</sub> ≤ 6.0 MHz at 1.8 V ≤ V<sub>DD</sub> < 2.0 V, set the processor control register (PCC) to a value other than 0011 or 0010. If the PCC is set to 0011 or 0010, the rated machine cycle time of 1.9 μs is not satisfied.
- If the oscillation frequency is 4.19 MHz < f<sub>x</sub> ≤ 6.0 MHz at 2.0 V ≤ V<sub>DD</sub> < 2.7 V, set the processor control register (PCC) to a value other than 0011. If the PCC is set to 0011, the rated machine cycle time of 0.95 μs is not satisfied.
- Oscillation stabilization time is a time required for oscillation to stabilize after application of V<sub>DD</sub>, or after the STOP mode has been released.

**Caution** When using the oscillation circuit of the system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- Keep the wire length as short as possible.
- Do not cross other signal lines.
- Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
- Always keep the ground point of the capacitor of the oscillation circuit as the same potential as V<sub>ss</sub>.
- Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

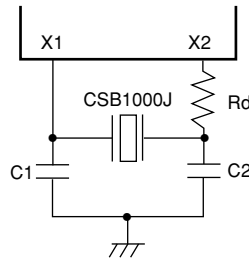


**Recommended Oscillator Constants**

**Ceramic resonator (T<sub>A</sub> = -40 to +85°C)**

Manufacturer	Part Number	Frequency (MHz)	Recommended Oscillator Constant (pF)		Oscillation Voltage Range (V <sub>DD</sub> )		Remark
			C1	C2	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J <sup>Note</sup>	1.0	100	100	1.8	6.0	R <sub>d</sub> = 2.2 kΩ
	CSA2.00MG040	2.0	100	100	1.9		—
	CST2.00MG040		—	—			On-chip capacitor
	CSA4.19MG	4.19	30	30	1.8		—
	CST4.19MGW		—	—			On-chip capacitor
	CSA6.00MG	6.0	30	30	2.0		—
	CST6.00MGW		—	—			On-chip capacitor
	CSA6.00MGU	6.0	30	30	1.8		—
	CST6.00MGWU		—	—			On-chip capacitor

**Note** When using the CSB1000J (1.0 MHz) made by Murata Mfg. Co., Ltd. as a ceramic resonator, a limiting resistor (R<sub>d</sub> = 2.2 kΩ) is necessary (refer to the figure below). This resistor is not necessary when using the other recommended resonators.



**Caution** The oscillator constants and oscillation voltage range indicate conditions for stable oscillation, but do not guarantee oscillation frequency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the oscillator in the actual circuit. Please contact directly the manufacturer of the resonator to be used.

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output current	I <sub>OH</sub>	Per pin	P30, P31, P33, P60 to P63, P80			-5	mA
			P32, V <sub>DD</sub> = 3.0 V, V <sub>OH</sub> = V <sub>DD</sub> - 2.0 V		-7	-15	mA
		Total of all pins				-20	mA
Low-level output current	I <sub>OL</sub>	Per pin				15	mA
		Total of all pins				45	mA
High-level input voltage	V <sub>IH1</sub>	Port 3	2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
			1.8 V ≤ V <sub>DD</sub> < 2.7 V	0.9V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	Ports 6 to 8, KRREN, $\overline{\text{RESET}}$	2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
			1.8 V ≤ V <sub>DD</sub> < 2.7 V	0.9V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IH3</sub>	X1		V <sub>DD</sub> - 0.1		V <sub>DD</sub>	V	
Low-level input voltage	V <sub>IL1</sub>	Port 3	2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V	0		0.3V <sub>DD</sub>	V
			1.8 V ≤ V <sub>DD</sub> < 2.7 V	0		0.1V <sub>DD</sub>	V
	V <sub>IL2</sub>	Ports 6 to 8, KRREN, $\overline{\text{RESET}}$	2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V	0		0.2V <sub>DD</sub>	V
			1.8 V ≤ V <sub>DD</sub> < 2.7 V	0		0.1V <sub>DD</sub>	V
V <sub>IL3</sub>	X1		0		0.1	V	
High-level output voltage	V <sub>OH</sub>	V <sub>DD</sub> = 4.5 to 6.0 V, I <sub>OH</sub> = -1.0 mA		V <sub>DD</sub> - 1.0			V
		V <sub>DD</sub> = 1.8 to 6.0 V, I <sub>OH</sub> = -100 μA		V <sub>DD</sub> - 0.5			V
Low-level output voltage	V <sub>OL</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	Port 3, I <sub>OL</sub> = 15 mA		0.6	2.0	V
			Ports 6, 8, I <sub>OL</sub> = 1.6 mA			0.4	V
		V <sub>DD</sub> = 1.8 to 6.0 V, I <sub>OH</sub> = 400 μA					0.5
High-level input leakage current	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub>	Pins other than X1			3.0	μA
	I <sub>LIH2</sub>		X1			20	μA
Low-level input leakage current	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V	Pins other than X1			-3.0	μA
	I <sub>LIL2</sub>		X1			-20	μA
High-level output leakage current	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub>				3.0	μA
Low-level output leakage current	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V				-3.0	μA
On-chip pull-up resistance	R <sub>L1</sub>	V <sub>IN</sub> = 0 V	Port 3, 6, 8	50	100	200	kΩ
	R <sub>L2</sub>		Port 7 (mask option)	15	30	60	kΩ
			$\overline{\text{RESET}}$ (mask option)	50	100	200	kΩ

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Power supply current <sup>Note 1</sup>	I <sub>DD1</sub>	4.19-MHz crystal oscillation C1 = C2 = 22 pF	V <sub>DD</sub> = 5.0 V ±10% <sup>Note 2</sup>		1.5	5.0	mA	
			V <sub>DD</sub> = 3.0 V ±10% <sup>Note 3</sup>		0.23	1.0	mA	
	I <sub>DD2</sub>	C1 = C2 = 22 pF	HALT mode	V <sub>DD</sub> = 5.0 V ±10%		0.64	3.0	mA
				V <sub>DD</sub> = 3.0 V ±10%		0.20	0.9	mA
	I <sub>DD3</sub>	X1 = 0 V STOP mode	V <sub>DD</sub> = 1.8 to 6.0 V				5	μA
				T <sub>A</sub> = 25°C				1
			V <sub>DD</sub> = 3.0 V ± 10%			0.1	3	μA
T <sub>A</sub> = -40 to +40°C					0.1	1	μA	

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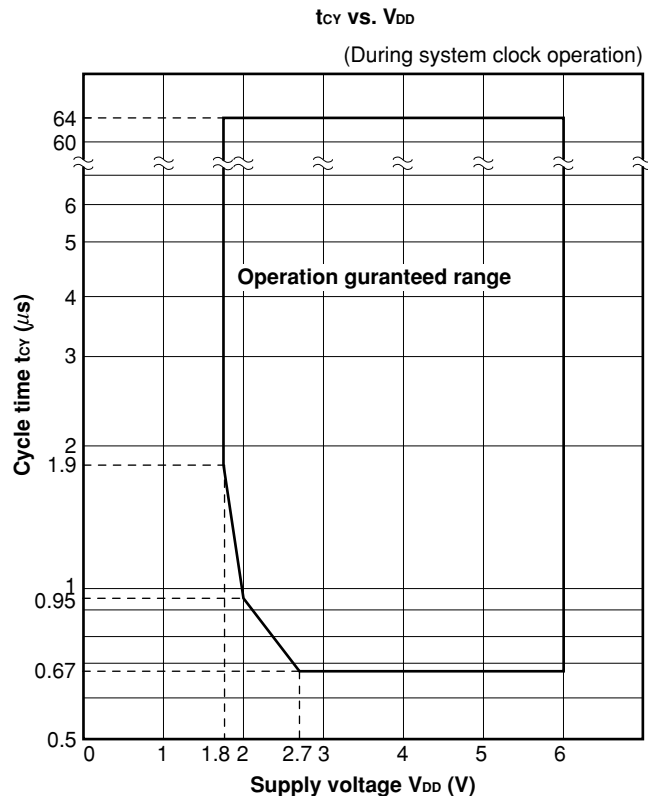
- Notes**
1. The current flowing through the on-chip pull-up resistor, the current during EEPROM writing time, and the current during the A/D converter operation are not included.
  2. When the device is operated in the high-speed mode by setting the processor clock control register (PCC) to 0011H
  3. When the device is operated in the low-speed mode by setting PCC to 0000H

AC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
CPU clock cycle time <sup>Note 1</sup> (Minimum instruction execution time = 1 machine cycle)	t <sub>CY</sub>	V <sub>DD</sub> = 1.8 to 2.0 V	1.9		64.0	μs	
		V <sub>DD</sub> = 2.0 to 2.7 V	0.95		64.0	μs	
		V <sub>DD</sub> = 2.7 to 6.0 V	0.67		64.0	μs	
Interrupt input high- and low-level width	t <sub>INTH</sub> , t <sub>INTL</sub>	INT0		IM02 = 0	Note 2		μs
				IM02 = 1	10		μs
		KR4 to KR7	10				μs
RESET low-level width	t <sub>RSL</sub>		10			μs	

**Notes** 1. The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected resonator (or external clock) and the processor clock control register (PCC). The figure on the right shows the cycle time t<sub>CY</sub> characteristics against the supply voltage V<sub>DD</sub> when the system clock is used.

2. 2t<sub>CY</sub> or 128/f<sub>x</sub> depending on the setting of the interrupt mode register (IM0).



**EEPROM Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 6.0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
EEPROM write current	I <sub>EEW</sub>	4.19 MHz, crystal oscillation	V <sub>DD</sub> = 5.0 V ± 10%		4.5	15	mA
			V <sub>DD</sub> = 3.0 V ± 10%		2.0	6	mA
EEPROM write time	t <sub>EEW</sub>		3.8		10.0	ms	
EEPROM overwrite times	EEWT	T <sub>A</sub> = -40 to +50°C	100000			times/byte	
		T <sub>A</sub> = -40 to +85°C	60000			times/byte	

**A/D Converter Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 6.0 V, 1.8 V ≤ AV<sub>REF</sub> ≤ V<sub>DD</sub>)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution			8	8	8	bit	
Absolute Accuracy <sup>Note 1</sup>		AV <sub>REF</sub> = V <sub>DD</sub>	2.7 ≤ V <sub>DD</sub> ≤ 6.0 V			±1.5	LSB
			1.8 ≤ V <sub>DD</sub> < 2.7 V			±3.0	LSB
		AV <sub>REF</sub> ≠ V <sub>DD</sub>	1.8 ≤ V <sub>DD</sub> ≤ 5.5 V			±3.0	LSB
			1.8 ≤ V <sub>DD</sub> ≤ 6.0 V			±3.5	LSB
Conversion time	t <sub>CONV</sub>	<b>Note 2</b>			168/f <sub>x</sub>	μs	
Sampling time	t <sub>SAMP</sub>	<b>Note 3</b>			44/f <sub>x</sub>	μs	
Analog input voltage	V <sub>IAN</sub>		V <sub>SS</sub>		AV <sub>REF</sub>	V	
Analog input impedance	R <sub>AN</sub>			1000		MΩ	
AV <sub>REF</sub> current	I <sub>REF</sub>			0.25	2.0	mA	

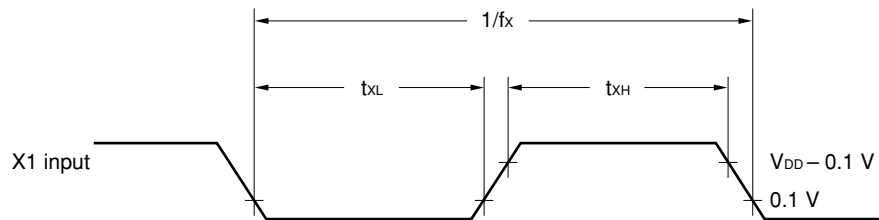
**Notes** 1. Absolute error except quantizing error (±1/2 LSB)

2. The time from conversion start instruction execution to conversion end (ECC = 1) (40.1 μs: @ f<sub>x</sub> = 4.19-MHz operation)
3. The time from conversion start instruction execution to sampling end (10.5 μs: @ f<sub>x</sub> = 4.19-MHz operation)

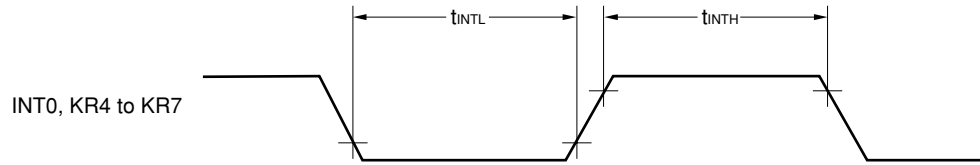
AC Timing Test Points (Excluding X1 Input)



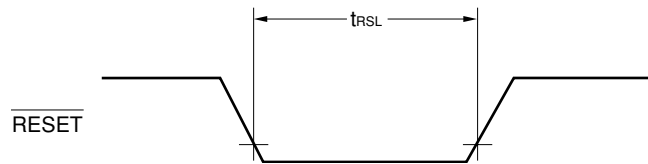
Clock Timing



**Interrupt Input Timing**



**RESET Input Timing**



**Data Memory STOP Mode Low-Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85 °C)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Release signal set time	$t_{SREL}$		0			μs
Oscillation stabilization wait time <sup>Note 1</sup>	$t_{WAIT}$	Release by $\overline{RESET}$		<b>Note 2</b>		ms
		Release by interrupt request		<b>Note 3</b>		ms

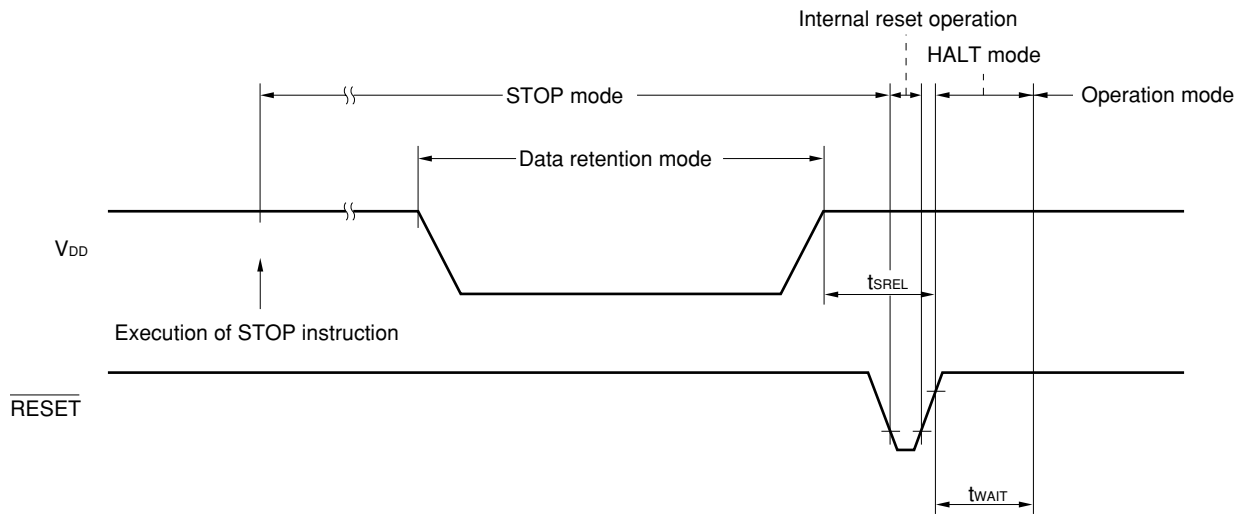
**Notes** 1. The oscillation stabilization wait time is the time during which the CPU operation is stopped to avoid unstable operation at oscillation start.

2. Any of  $2^{17}/f_X$ ,  $2^{15}/f_X$  or  $2^{13}/f_X$  can be selected with mask option.

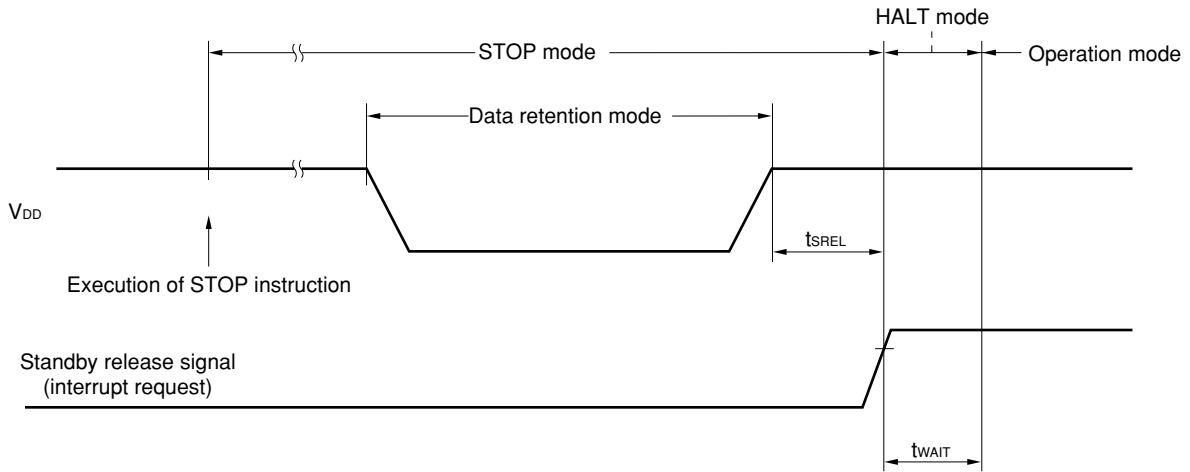
3. Depends on setting of basic interval timer mode register (BTM) (see table below).

BTM3	BTM2	BTM1	BTM0	Wait Time	
				When $f_X = 4.19$ MHz	When $f_X = 6.0$ MHz
-	0	0	0	$2^{20}/f_X$ (Approx. 250 ms)	$2^{20}/f_X$ (Approx. 175 ms)
-	0	1	1	$2^{17}/f_X$ (Approx. 31.3 ms)	$2^{17}/f_X$ (Approx. 21.8 ms)
-	1	0	1	$2^{15}/f_X$ (Approx. 7.81 ms)	$2^{15}/f_X$ (Approx. 5.46 ms)
-	1	1	1	$2^{13}/f_X$ (Approx. 1.95 ms)	$2^{13}/f_X$ (Approx. 1.37 ms)

Data Retention Timing (on releasing STOP mode by  $\overline{\text{RESET}}$ )



Data Retention Timing (Standby release signal: on releasing STOP mode by interrupt signal)

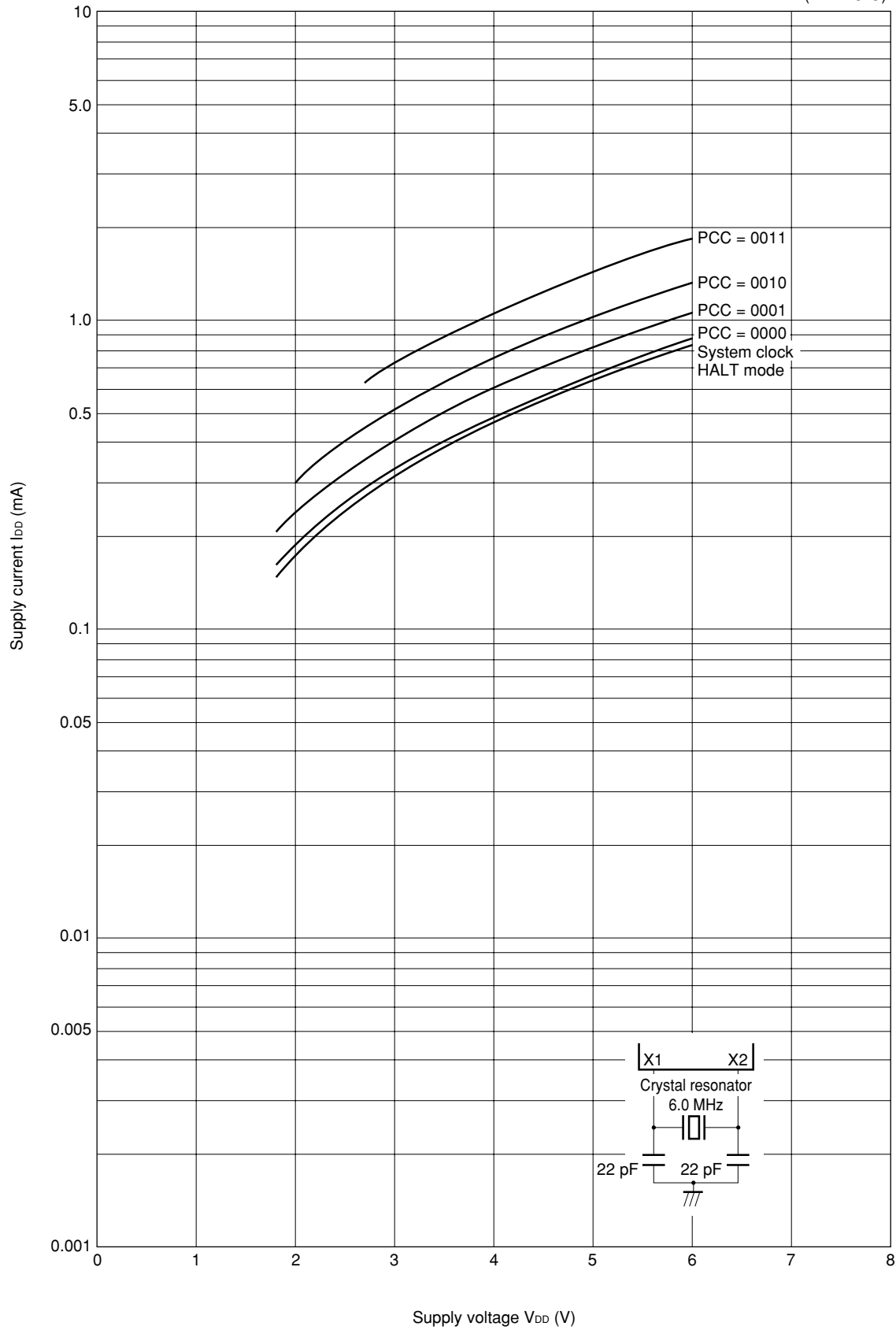




14. CHARACTERISTICS CURVES (REFERENCE VALUES)

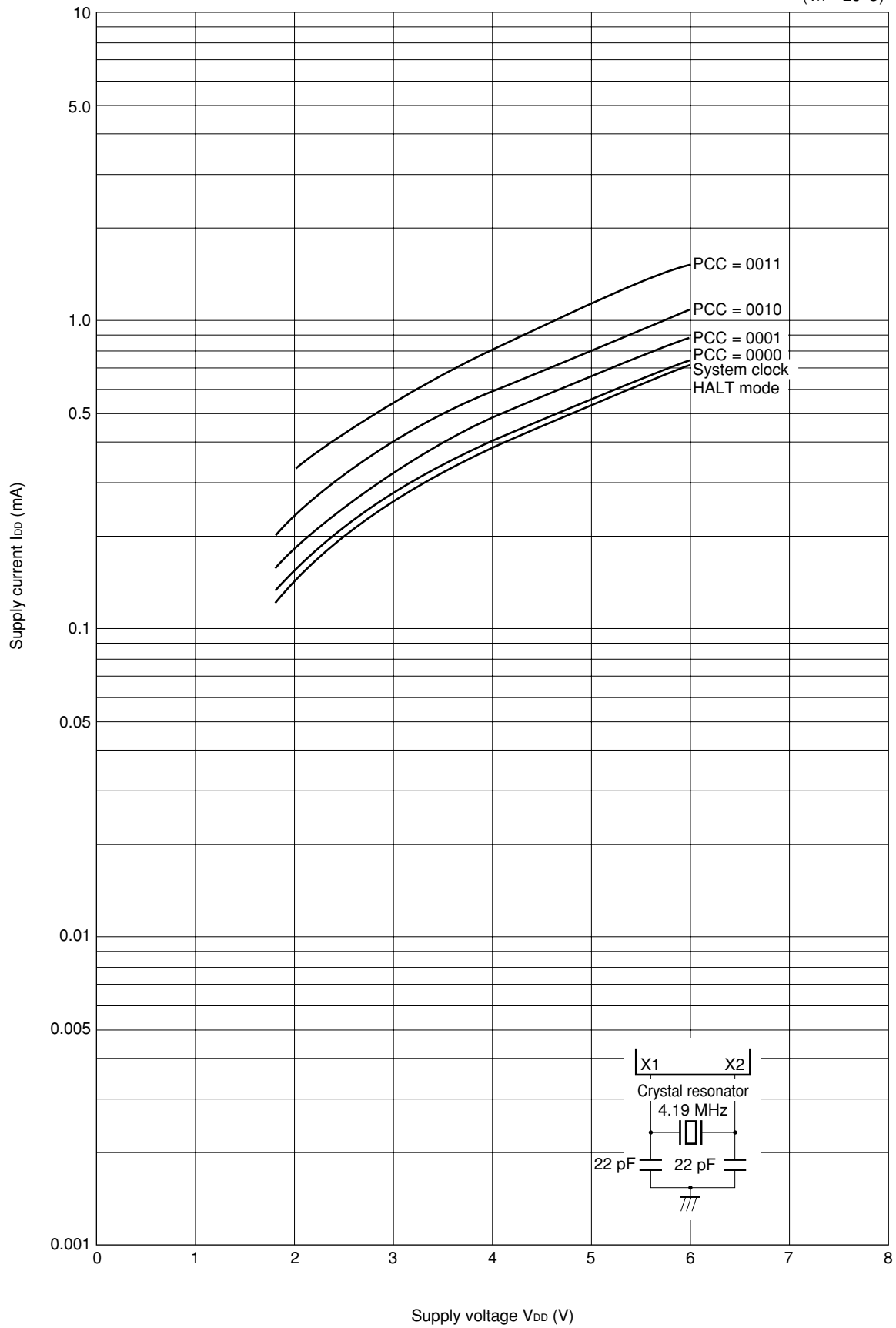
I<sub>DD</sub> vs V<sub>DD</sub> (System Clock: 6.0-MHz Crystal Resonator)

(T<sub>A</sub> = 25°C)



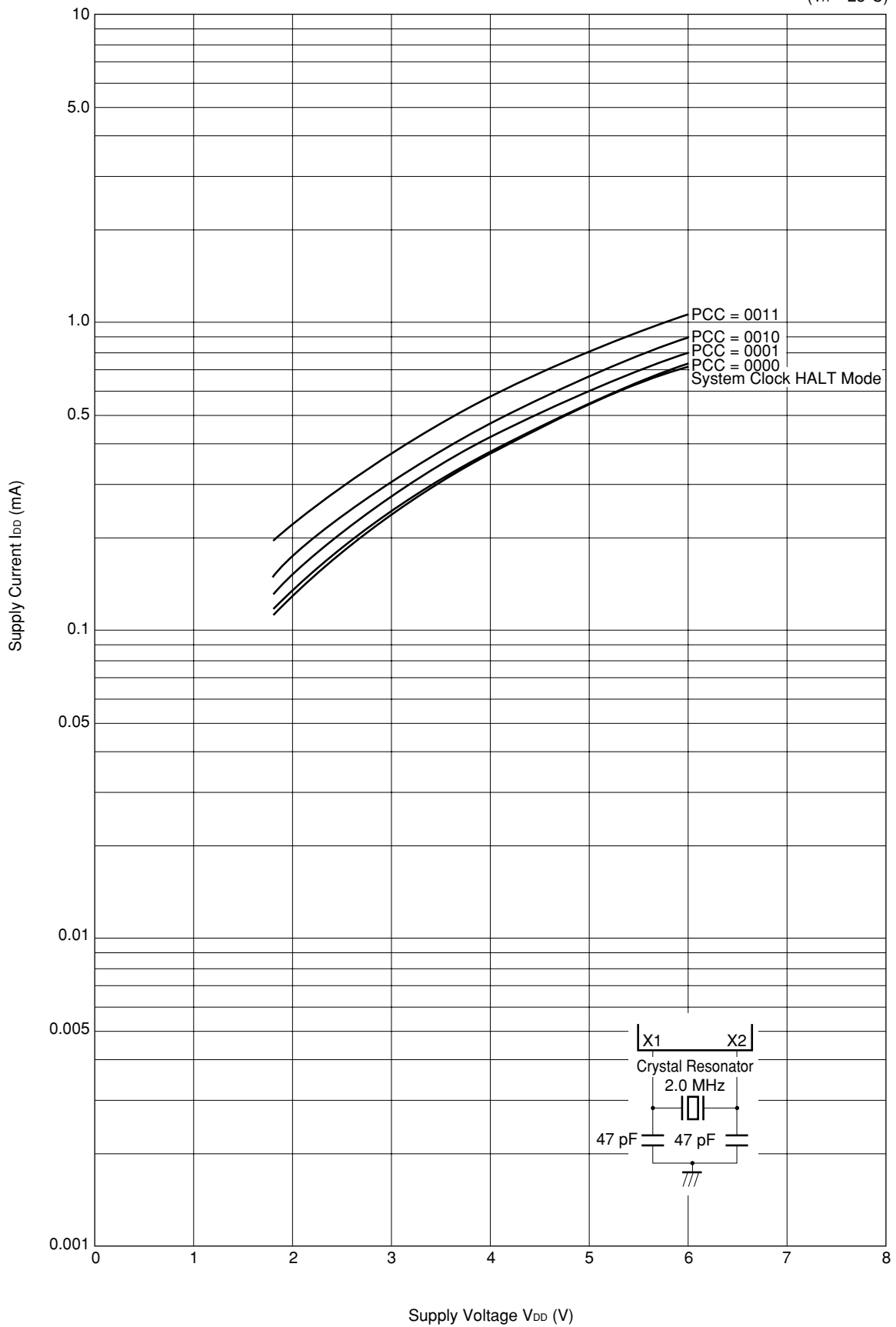
I<sub>DD</sub> vs V<sub>DD</sub> (System Clock: 4.19-MHz Crystal Resonator)

(T<sub>A</sub> = 25°C)



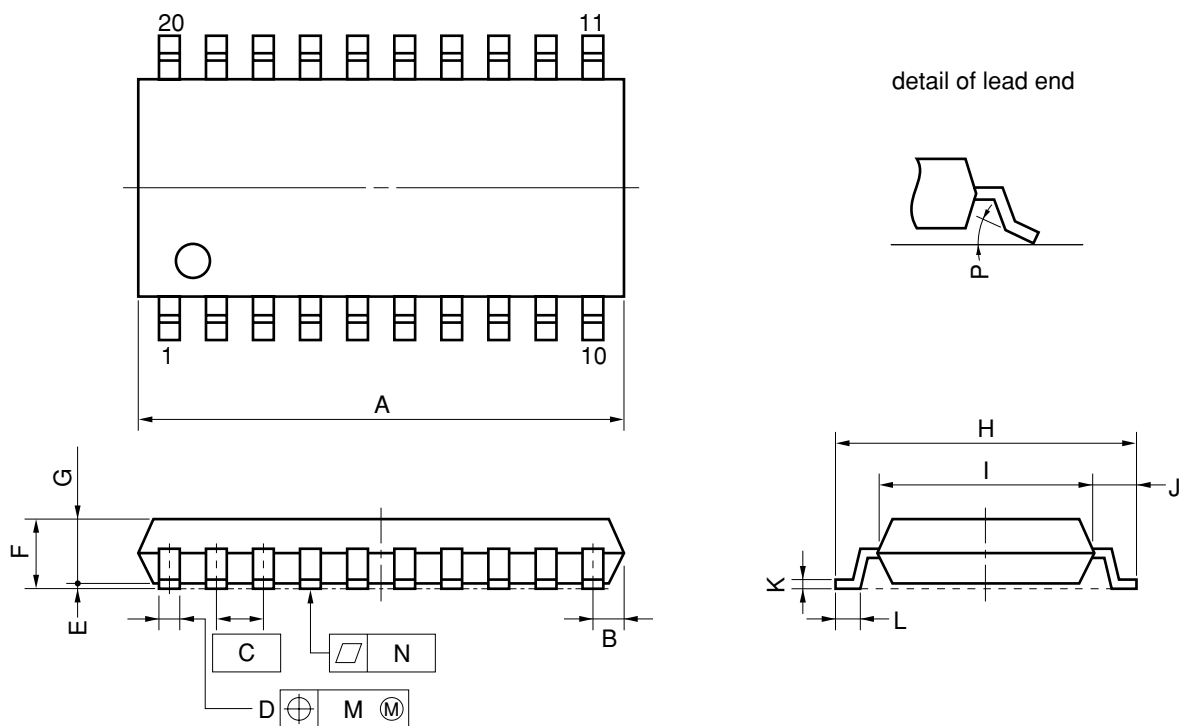
I<sub>DD</sub> vs V<sub>DD</sub> (System Clock: 2.0-MHz Crystal Resonator)

(T<sub>A</sub> = 25°C)



15. PACKAGE DRAWINGS

20 PIN PLASTIC SOP (300 mil)



**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 <sup>+0.10</sup> <sub>-0.05</sub>	0.016 <sup>+0.004</sup> <sub>-0.003</sub>
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	0.20 <sup>+0.10</sup> <sub>-0.05</sub>	0.008 <sup>+0.004</sup> <sub>-0.002</sub>
L	0.6±0.2	0.024 <sup>+0.008</sup> <sub>-0.009</sub>
M	0.12	0.005
N	0.10	0.004
P	3° <sup>+7°</sup> <sub>-3°</sub>	3° <sup>+7°</sup> <sub>-3°</sub>

P20GM-50-300B, C-4

**16. RECOMMENDED SOLDERING CONDITIONS**

The μPD754264 should be soldered and mounted under the following recommended conditions. For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

**Table 16-1. Surface Mounting Type Soldering Conditions**

**(1) μPD754264GS-xxx-BA5: 20-pin plastic SOP (300 mil, 1.27 mm pitch)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once Preheating temperature: 120°C max. (package surface temperature) Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	WS60-107-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	—

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

**Remark** For soldering methods and conditions other than those recommended above, contact an NEC Electronics sales representative.

★ **(2) μPD754264GS-xxx-BA5-A: 20-pin plastic SOP (300 mil, 1.27 mm pitch)**

Undefined

**Remark** Products with “-A” at the end of the part number are lead-free products.

APPENDIX A. COMPARISON OF FUNCTIONS BETWEEN μPD754264 AND 75F4264

Item		μPD754264	μPD75F4264 <sup>Note</sup>
Program memory		Mask ROM 0000H to 0FFFH (4096 × 8 bits)	Flash memory 0000H to 0FFFH (4096 × 8 bits)
Data memory	Static RAM	000H to 07FH (128 × 4 bits)	
	EEPROM	400H to 43FH (32 × 8 bits)	
CPU		75XL CPU	
General-purpose register		(4 bits × 8 or 8 bits × 4) × 4 banks	
Instruction execution time		<ul style="list-style-type: none"> <li>• 0.67, 1.33, 2.67, 10.7 μs (@ f<sub>x</sub> = 6.0-MHz operation)</li> <li>• 0.95, 1.91, 3.81, 15.3 μs (@ f<sub>x</sub> = 4.19-MHz operation)</li> </ul>	
I/O port	CMOS input	4 (on-chip pull-up resistor can be connected by mask option)	
	CMOS I/O	9 (on-chip pull-up resistor connection can be specified by means of software)	
	Total	13	
System clock oscillator		Crystal/ceramic oscillator	
Start-up time after reset		2 <sup>17</sup> /f <sub>x</sub> , 2 <sup>15</sup> /f <sub>x</sub> , 2 <sup>13</sup> /f <sub>x</sub> (can be selected by mask option)	2 <sup>15</sup> /f <sub>x</sub>
Timer		4 channels <ul style="list-style-type: none"> <li>• 8-bit timer counter: 3 channels (can be used as 16-bit timer counter)</li> <li>• Basic interval timer/watchdog timer: 1 channel</li> </ul>	
A/D converter		<ul style="list-style-type: none"> <li>• 8-bit resolution × 2 channels (successive approximation, hardware control)</li> <li>• Can be operated from V<sub>DD</sub> = 1.8 V</li> </ul>	
Programmable threshold port		None	2 channels
Vectored interrupt		External: 1, internal: 5	
Test input		External: 1 (key return reset function available)	
Power supply voltage		V <sub>DD</sub> = 1.8 to 6.0 V	
Operating ambient temperature		T <sub>A</sub> = -40 to +85°C	
Package		• 20-pin plastic SOP (300 mil, 1.27-mm pitch)	

**Note** Under development

**APPENDIX B DEVELOPMENT TOOLS**

The following development tools are provided for system development using the μPD754264.

In the 75XL Series, the relocatable assembler which is common to the series is used in combination with the device file of each product.

**Language processor**

RA75X relocatable assembler	Host machine	OS	Distribution media	Part number (product name)
	PC-9800 Series		MS-DOS™ (Ver. 3.30 to Ver. 6.2 <sup>Note</sup> )	3.5-inch 2HD
5-inch 2HD				μS5A10RA75X
IBM PC/AT™ and compatible machines		Refer to the <b>OS for IBM PC</b>	3.5-inch 2HC	μS7B13RA75X
			5-inch 2HC	μS7B10RA75X

Device file	Host machine	OS	Distribution media	Part number (product name)
	PC-9800 Series		MS-DOS (Ver. 3.30 to Ver. 6.2 <sup>Note</sup> )	3.5-inch 2HD
5-inch 2HD				μS5A10DF754264
IBM PC/AT and compatible machines		Refer to the <b>OS for IBM PC</b>	3.5-inch 2HC	μS7B13DF754264
			5-inch 2HC	μS7B10DF754264

**Note** Ver.5.00 or later have the task swap function, but it cannot be used for this software.

**Remark** Operation of the assembler and device file are guaranteed only on the above host machine and OSs.

**Debugging tool**

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD754264.

The system configurations are described as follows.

Hardware	IE-75000-R <sup>Note 1</sup>	In-circuit emulator for debugging the hardware and software when developing application systems that use the 75X Series and 75XL Series. When developing the μPD754264, the emulation board IE-75300-R-EM and emulation probe EP-754144GS-R that are sold separately must be used with the IE-75000-R. By connecting with the host machine, efficient debugging can be made. It contains the emulation board IE-75000-R-EM which is connected.			
	IE-75001-R	In-circuit emulator for debugging the hardware and software when developing application systems that use the 75X Series and 75XL Series. When developing the μPD754264, the emulation board IE-75300-R-EM and emulation probe EP-754144GS-R which are sold separately must be used with the IE-75001-R. By connecting the host machine, efficient debugging can be made.			
	IE-75300-R-EM	Emulation board for evaluating the application systems that use the μPD754264. It must be used with the IE-75000-R or IE-75001-R.			
	EP-754144GS-R	Emulation probe for the μPD754264GS. It must be connected to IE-75000-R (or IE-75001-R) and IE-75300-R-EM. It is supplied with the flexible boards EV-9500GS-20 (supporting 20-pin plastic shrink SOPs) and EV-9501GS-20 (supporting 20-pin plastic SOPs) which facilitate connection to a target system. The μPD754264GS uses only EV-9501GS-20.			
Software	IE control program	Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronix I/F and controls the above hardware on a host machine.			
		Host machine	OS	Distribution media	Part number (product name)
		PC-9800 Series	MS-DOS (Ver. 3.30 to Ver. 6.2 <sup>Note 2</sup> )	3.5-inch 2HD	μS5A13IE75X
				5-inch 2HD	μS5A10IE75X
		IBM PC/AT and its compatible machine	Refer to the <b>OS for IBM PC</b>	3.5-inch 2HC	μS7B13IE75X
5-inch 2HC	μS7B10IE75X				

**Notes** 1. Maintenance parts

2. Ver.5.00 or later have the task swap function, but it cannot be used for this software.

**Remark** Operation of the IE control program is guaranteed only on the above host machines and OSs.



**OS for IBM PC**

The following IBM PC OSs are supported.

OS	Version
PC DOS™	Ver. 5.02 to Ver. 6.3 J6.1/V <sup>Note</sup> to J6.3/V <sup>Note</sup>
MS-DOS	Ver. 5.0 to Ver. 6.22 5.0/V <sup>Note</sup> to J6.2/V <sup>Note</sup>
IBM DOS™	J5.02/V <sup>Note</sup>

**Note** Supported only English mode.

**Caution** Ver. 5.0 or later have the task swap function, but it cannot be used for operating systems above.

**APPENDIX C. RELATED DOCUMENTS**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Device related documents**

Document Name	Document Number	
	Japanese	English
μPD754264 Data Sheet	U12487J	This document
μPD754264 User's Manual	U12287J	U12287E
75XL Series Selection Guide	U10453J	U10453E

**Development tool related documents**

Document Name		Document Number		
		Japanese	English	
Hardware	IE-75000-R/IE-75001-R User's Manual	EEU-846	EEU-1416	
	IE-75300-R-EM User's Manual	U11354J	U11354E	
	EP-754144GS-R User's Manual	U10695J	U10695E	
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363

**Other related documents**

Document Name		Document Number	
		Japanese	English
IC Package Manual		C10943X	
Semiconductor Device Mounting Technology Manual		C10535J	C10535E
Quality Grades on NEC Semiconductor Devices		C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System		C10983J	C10983E
Static Electricity Discharge (ESD) Test		MEM-539	–
Guide to Quality Assurance for Semiconductor Devices		C11893J	MEI-1202
Microcomputer Related Product Guide - Other Manufacturers		U11416J	–

**Caution** These documents are subject to change without notice. Be sure to read the latest documents.

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Availability of related technical literature
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- Network requirements

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