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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

μ PD75312,75316

4-BIT SINGLE-CHIP MICROCOMPUTER

Phase-out/Discontinued

DESCRIPTION

The μ PD75316 is one of the 75X Series 4-bit single-chip microcomputer having a built-in LCD controller/driver, and has a data processing capability comparable to that of an 8-bit microcomputer.

In addition to high-speed operation with 0.95 μ s minimum instruction execution time for the CPU, the μ PD75316 can also process data in 1-, 4-, and 8-bit units. Therefore, as a 4-bit single-chip microcomputer chip having a built-in LCD panel controller/driver, its data processing capability is the highest in its class in the world.

Detailed functions are described in the following user's manual. Be sure to read it for designing.

μ PD75308 User's Manual: IEM-5016

FEATURES

- Internal memory
 - Program memory (ROM)
 - : 16256 \times 8 bits (μ PD75316)
 - : 12160 \times 8 bits (μ PD75312)
 - Data memory
 - : 512 \times 4 bits
- Capable of high-speed operation and variable instruction execution time to power save
 - 0.95 μ s, 1.91 μ s, 15.3 μ s (operating at 4.19 MHz)
 - 122 μ s (operating at 32.768 kHz)
- 75X architecture comparable to that for an 8-bit microcomputer is employed
- Built-in programmable LCD controller/driver
- Clock operation at reduced power dissipation: 5 μ A TYP. (operating at 3 V)
- Enhanced timer function (3 channels)
- Interrupt functions especially enhanced for applications, such as remote control receiver
- Pull-up resistors can be provided for 31 I/O lines
- Built-in NEC standard serial bus interface (SBI)
- Upgraded model of μ PD7514 (μ PD7500 Series)
- PROM version (μ PD75P316, μ PD75P316A) available

APPLICATIONS

VCRs, CD players, telephones, cameras, blood pressure gauges, etc.

The μ PD75316 is treated as the representative model throughout this document, unless there are differences between μ PD75312 and μ PD75316 functions.

The information in this document is subject to change without notice.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75312GF-xxx-3B9	80-pin plastic QFP (14×20 mm)	Standard
μPD75316GF-xxx-3B9	80-pin plastic QFP (14×20 mm)	Standard

Remarks: xxx is ROM code number.

Please refer to “Quality Grade on NEC Semiconductor Devices” (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

FUNCTIONAL OUTLINE (1/2)

Item	Function			
Number of Basic Instructions	41			
Instruction Cycle	<ul style="list-style-type: none"> • 0.95 μs, 1.91 μs, 15.3 μs (Main system clock: operating at 4.19 MHz) • 122 μs (Subsystem clock: operating at 32.768 kHz) 			
Internal Memory	ROM	16256 × 8-bit (μPD75316), 12160 × 8-bit (μPD75312)		
	RAM	512 × 4-bit		
General-Purpose Registers	<ul style="list-style-type: none"> • 4-bit manipulation: 8 (B, C, D, E, H, L, X, A) • 8-bit manipulation: 4 (BC, DE, HL, XA) 			
Accumulator	<ul style="list-style-type: none"> • Bit accumulator (CY) • 4-bit accumulator (A) • 8-bit accumulator (XA) 			
Instruction Set	<ul style="list-style-type: none"> • Abundant bit manipulation instructions • Efficient 4-bit data manipulation instructions • 8-bit data transfer instructions • GETI instruction executing 2-/3-byte instruction with a single byte 			
I/O Line	40	8	CMOS input pins	Pull-up by software is possible. : 23
		16	CMOS input/output pins	
		8	CMOS output pins	Also serve as segment pins
		8	N-ch open-drain input/output	Withstand voltage: 10 V Pull-up by mask option is possible. : 8
LCD Controller/Driver	<ul style="list-style-type: none"> • Segment number selection: 24/28/32 segments (4/8 pins can also be used as bit ports.) • Display mode selection: Static, 1/2 duty, 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty • Dividing resistor for LCD driving can be built-in by mask option. 			
Supply Voltage Range	V _{DD} = 2.7 to 6.0 V			

FUNCTIONAL OUTLINE (2/2)

Item	Function	
Timer	3 chs	<ul style="list-style-type: none"> • 8-bit timer/event counter <ul style="list-style-type: none"> • Clock source: 4 steps • Event count is possible
		<ul style="list-style-type: none"> • 8-bit basic interval timer <ul style="list-style-type: none"> • Reference time generation: 1.95 ms, 7.82 ms, 31.3 ms, 250 ms (operating at 4.19 MHz) • Can be used as watchdog timer
		<ul style="list-style-type: none"> • Watch timer <ul style="list-style-type: none"> • Generates 0.5-second time intervals • Count clock source: Main system clock or subsystem clock (selectable) • Watch fast forward mode (generates 3.9-ms time intervals) • Buzzer output (2 kHz)
8-bit Serial Interface	<ul style="list-style-type: none"> • Three modes: <ul style="list-style-type: none"> • 3-line serial I/O mode • 2-line serial I/O mode • SBI mode 	
	<ul style="list-style-type: none"> • LSB/MSB first selectable 	
Bit Sequential Buffer	Special bit manipulation memory: 16 bits <ul style="list-style-type: none"> • Ideal for remote controller 	
Clock Output Function	Timer/event counter output (PTO0): Output of square wave at specified frequency	
	Clock output (PCL): Φ, 524, 262, 65.5 kHz (operating at 4.19 MHz)	
	Buzzer output (BUZ): 2 kHz (operating at 4.19 MHz or 32.768 kHz)	
Vector Interrupt	<ul style="list-style-type: none"> • External: 3 • Internal: 3 	
Test Input	<ul style="list-style-type: none"> • External: 1 • Internal: 1 	
System Clock Oscillator Circuit	<ul style="list-style-type: none"> • Ceramic/crystal oscillator circuit for main system clock oscillation: 4.194304 MHz • Crystal oscillator circuit for subsystem clock oscillation: 32.768 kHz 	
Standby Function	STOP/HALT mode	
Package	80-pin plastic QFP (14 × 20 mm)	

CONTENTS

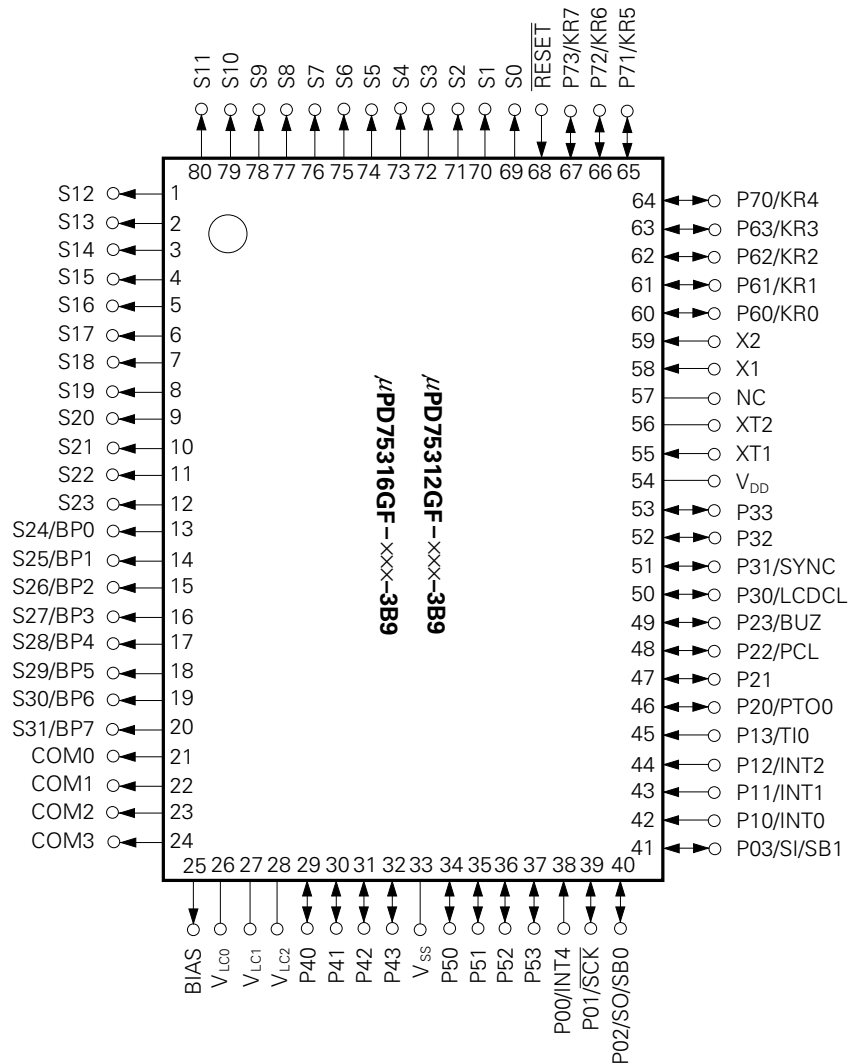
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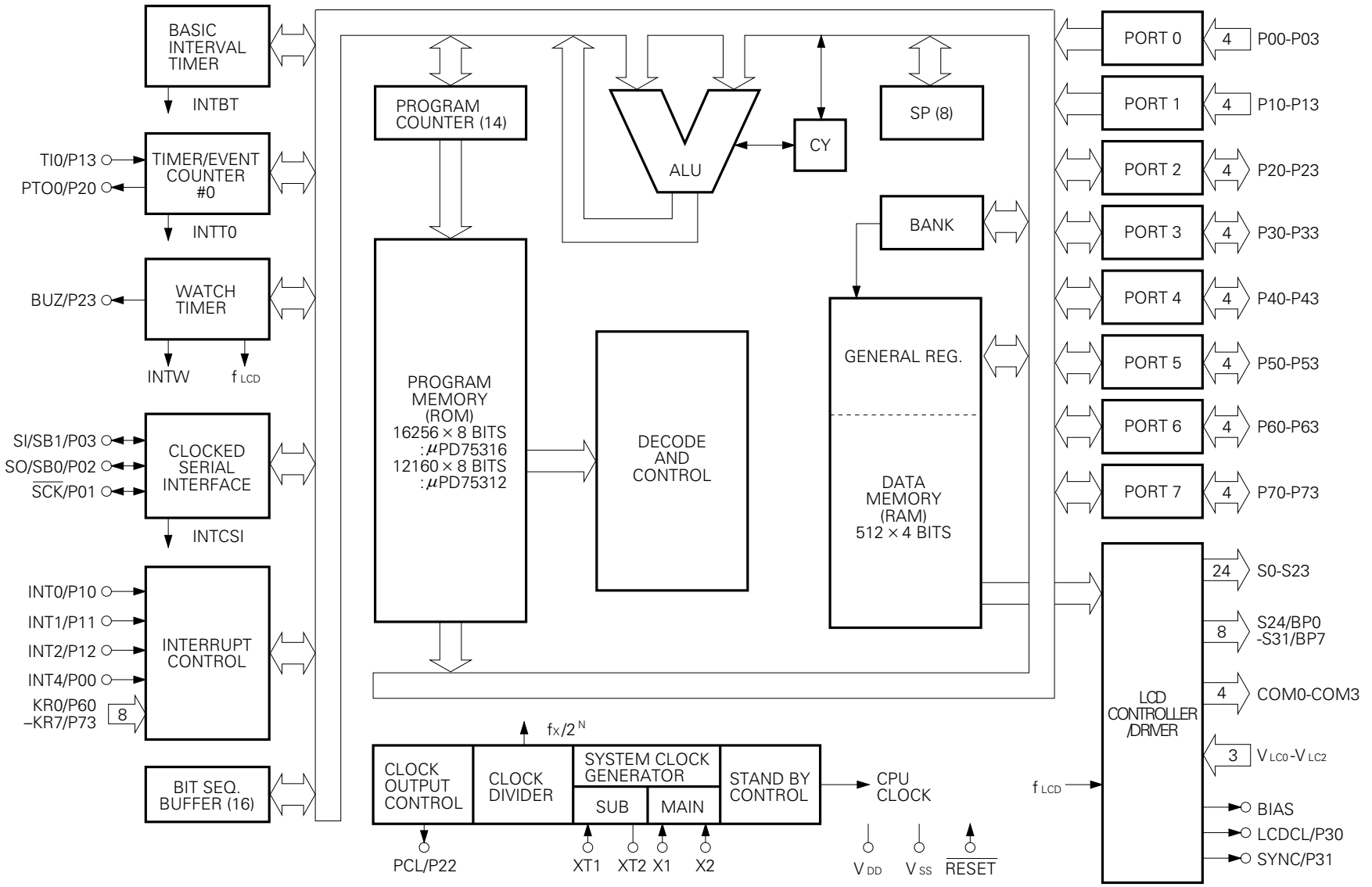
1. PIN CONFIGURATION (Top View)



- | | |
|---------------------------|---|
| P00-P03 : Port 0 | S0-S31 : Segment Output 0-31 |
| P10-P13 : Port 1 | COM0-COM3 : Common Output 0-3 |
| P20-P23 : Port 2 | V _{Lc0} -V _{Lc2} : LCD Power Supply 0-2 |
| P30-P33 : Port 3 | BIAS : LCD Power Supply Bias Control |
| P40-P43 : Port 4 | LCDCL : LCD Clock |
| P50-P53 : Port 5 | SYNC : LCD Synchronization |
| P60-P63 : Port 6 | TI0 : Timer Input 0 |
| P70-P73 : Port 7 | PTO0 : Programmable Timer Output 0 |
| BP0-BP7 : Bit Port | BUZ : Buzzer Clock |
| KR0-KR7 : Key Return | PCL : Programmable Clock |
| SCK : Serial Clock | INT0, INT1, INT4: External Vectored Interrupt 0, 1, 4 |
| SI : Serial Input | INT2 : External Test Input 2 |
| SO : Serial Output | X1, X2 : Main System Clock Oscillation 1, 2 |
| SB0, SB1 : Serial Bus 0,1 | XT1, XT2 : Subsystem Clock Oscillation 1, 2 |
| RESET : Reset Input | NC : No Connection |

Phase-out/Discontinued

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/Output Circuit TYPE*1
P00	Input	INT4	4-bit input port (PORT0) Pull-up resistors can be specified in 3-bit units for the P01 to P03 pins by software.	×	Input	ⓑ
P01	Input/Output	$\overline{\text{SCK}}$				ⓕ-A
P02	Input/Output	SO/SB0				ⓕ-B
P03	Input/Output	SI/SB1				Ⓜ-C
P10	Input	INT0	4-bit input port (PORT1) Internal pull-up resistors can be specified in 4-bit units by software.	×	Input	ⓑ-C
P11		INT1				
P12		INT2				
P13		Ti0				
P20	Input/Output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistors can be specified in 4-bit units by software.	×	Input	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30*2	Input/Output	LCDCL	Programmable 4-bit input/output port (PORT3) This port can be specified for input/output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	×	Input	E-B
P31*2		SYNC				
P32*2		—				
P33*2		—				
P40-43*2	Input/Output	—	N-ch open-drain 4-bit input/output port (PORT4) Internal pull-up resistors can be specified in bit units. (mask option) Withstand voltage is 10 V in the open-drain mode.	○	High level (with internal pull-up resistor) or high impedance	M
P50-53*2	Input/Output	—	N-ch open-drain 4-bit input/output port (PORT5) Internal pull-up resistors can be specified in bit units. (mask option) Withstand voltage is 10 V in the open-drain mode.			M

*1: Circles indicate Schmitt trigger inputs.

2: Can directly drive LED.

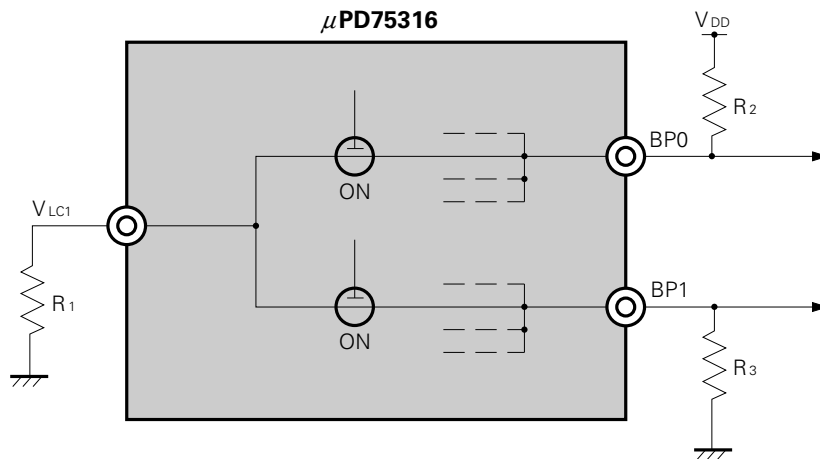
3.1 PORT PINS (2/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/Output Circuit TYPE*1
P60	Input/Output	KR0	Programmable 4-bit input/output port (PORT6) This port can be specified for input/output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	○	Input	⊕-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/Output	KR4	4-bit input/output port (PORT7) Internal pull-up resistors can be specified in 4-bit units by software.		Input	⊕-A
P71		KR5				
P72		KR6				
P73		KR7				
BP0	Output	S24	1-bit output port (BIT PORT) Shared with a segment output pin.	×	*2	G-C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

*1: Circles indicate Schmitt trigger inputs.

2: For BP0-7, V_{LC1} indicated below are selected as the input source. However, the output level is changed depending on BP0-7 and the V_{LC1} external circuits.

Example: Since BP0-7 are connected to each other within the μ PD75316 as shown in the diagram below, the output level of BP0-7 depends on the sizes of R_1 , R_2 and R_3 .



3.2 NONPORT PINS

Pin Name	Input/Output	Also Served As	Function		When Reset	Input/Output Circuit TYPE*1
T10	Input	P13	Timer/event counter external event pulse Input		Input	ⓑ-C
PTO0	Input/Output	P20	Timer/event counter output		Input	E-B
PCL	Input/Output	P22	Clock output		Input	E-B
BUZ	Input/Output	P23	Fixed frequency output (for buzzer or for trimming the system clock)		Input	E-B
$\overline{\text{SCK}}$	Input/Output	P01	Serial clock input/output		Input	ⓕ-A
SO/SB0	Input/Output	P02	Serial data output Serial bus input/output		Input	ⓕ-B
SI/SB1	Input/Output	P03	Serial data input Serial bus input/output		Input	Ⓜ-C
INT4	Input	P00	Edge detection vector interrupt input (both rising and falling edge detection are effective)		Input	ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge can be selected)	Clock synchronous	Input	ⓑ-C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Asynchronous	Input	ⓑ-C
KR0-KR3	Input/Output	P60-P63	Parallel falling edge detection testable input		Input	ⓕ-A
KR4-KR7	Input/Output	P70-P73	Parallel falling edge detection testable input		Input	ⓕ-A
S0-S23	Output	—	Segment signal output		*2	G-A
S24-S31	Output	BP0-7	Segment signal output		*2	G-C
COM0-COM3	Output	—	Common signal output		*2	G-B
V _{LC0} -V _{LC2}	—	—	LCD drive power Internal dividing resistor (mask option)		—	—
BIAS	Output	—	Disconnect output for external expanded driver		*3	—
LCDCL*4	Input/Output	P30	Externally expanded driver clock output		Input	E-B
SYNC*4	Input/Output	P31	Externally expanded driver sync clock output		Input	E-B
X1, X2	Input	—	To connect the crystal/ceramic oscillator to the main system clock generator. When inputting the external clock, input the external clock to pin X1, and the reverse phase of the external clock to pin X2.		—	—
XT1	Input	—	To connect the crystal oscillator to the subsystem clock generator. When the external clock is used, pin XT1 inputs the external clock. In this case, pin XT2 must be left open. Pin XT1 can be used as a 1-bit input (test) pin.		—	—
XT2	—	—				

(to be cont'd)

(cont'd)

Pin Name	Input/Output	Also Served As	Function	When Reset	Input/Output Circuit TYPE*1
RESET	Input	—	System reset input	—	ⓑ
NC *5	—	—	No connection	—	—
V _{DD}	—	—	Positive power supply	—	—
V _{SS}	—	—	GND	—	—

*1: Circles indicate Schmitt trigger inputs.

2: For these display output, V_{LCX} indicated below are selected as the input source.

S0 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}

However, display output level varies depending on the particular display output and V_{LCX} external circuit.

3: Internal dividing resistor provided : Low level

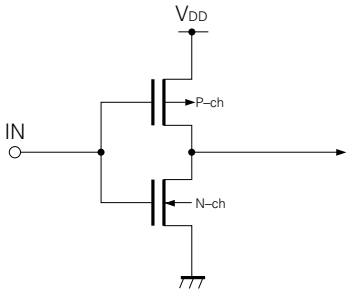
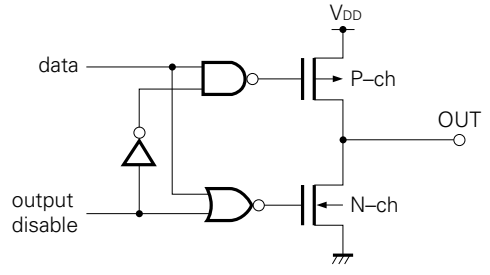
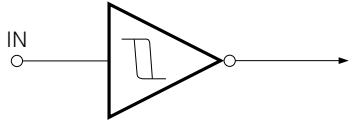
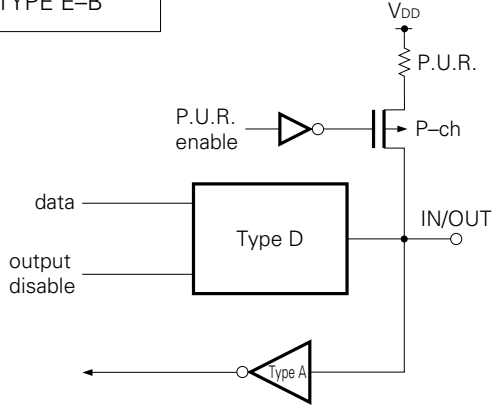
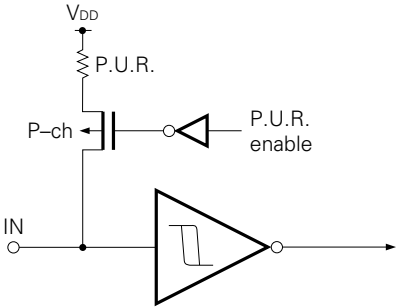
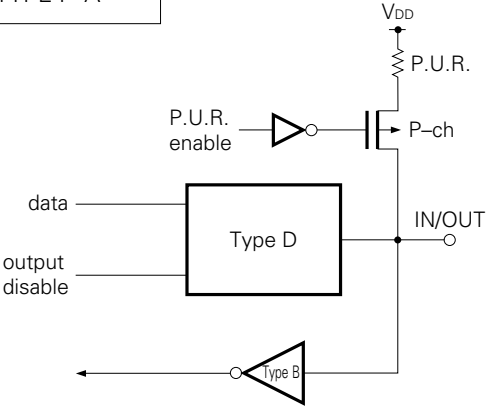
Internal dividing resistor not provided : High impedance

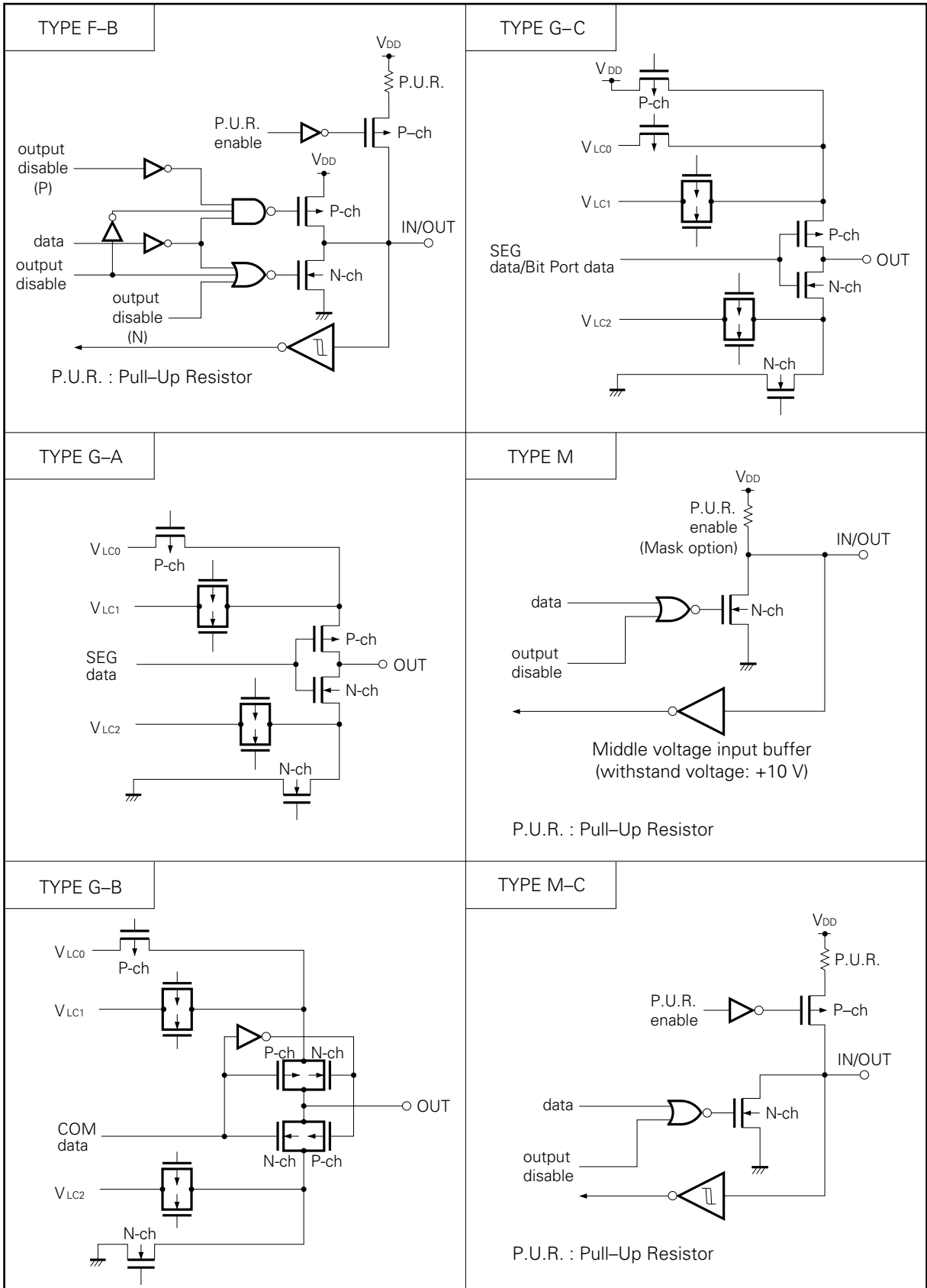
4: These pins are provided for future system expansion. At present, these pins are used only as pins P30 and P31.

5: When sharing the printed circuit board with the μPD75P316, the NC pin must be connected to V_{DD}.

3.3 PIN INPUT/OUTPUT CIRCUITS

The following shows a simplified input/output circuit diagram for each pin of the μ PD75316.

<p>TYPE A (for TYPE E-B)</p>  <p>Input buffer of CMOS standard</p>	<p>TYPE D (for TYPE E-B, F-A)</p>  <p>Push-pull output that can be set in a output high-impedance state (both P-ch and N-ch are off)</p>
<p>TYPE B</p>  <p>Schmitt trigger input with hysteresis characteristics</p>	<p>TYPE E-B</p>  <p>P.U.R. : Pull-Up Resistor</p>
<p>TYPE B-C</p>  <p>P.U.R. : Pull-Up Resistor</p>	<p>TYPE F-A</p>  <p>P.U.R. : Pull-Up Resistor</p>



3.4 RECOMMENDED PROCESSING OF UNUSED PINS

Table 3-1 Unused Pins Processing

Pin	Recommended Connections	
P00/INT4	Connect to V _{SS}	
P01/SCK	Connect to V _{SS} or V _{DD}	
P02/SO/SB0		
P03/SI/SB1		
P10/INT0-P12/INT2	Connect to V _{SS}	
P13/TI0		
P20/PTO0	Input : Connect to V _{SS} or V _{DD} Output: Open	
P21		
P22/PCL		
P23/BUZ		
P30/LCDCL		
P31/SYNC		
P32		
P33		
P40-P43		
P50-P53		
P60/KR0-P63/KR3		
P70/KR4-P73/KR7		
S0-S23		Open
S24/BP0-S31/BP7		
COM0-COM3		
V _{LC0} -V _{LC2}	Connect to V _{SS}	
BIAS	Connect to V _{SS} only when all of the V _{LC0} -V _{LC2} pins are unused, otherwise, open.	
XT1	Connect to V _{SS} or V _{DD}	
XT2	Open	

3.5 NOTES ON USING THE P00/INT4, AND RESET PINS



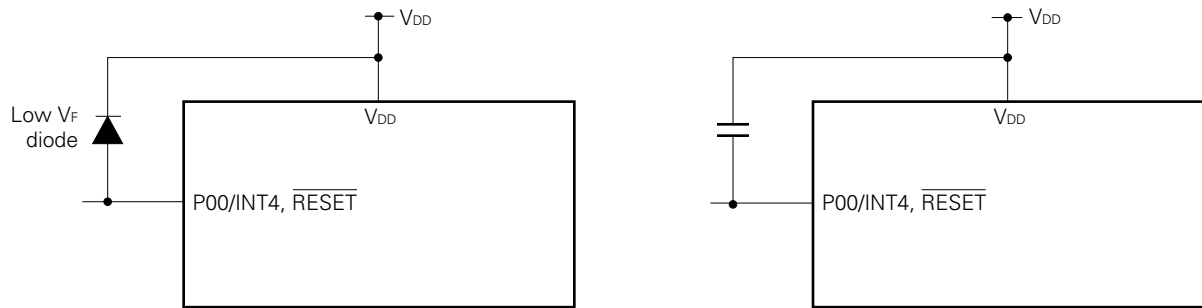
In addition to the functions described in Sections 3.1 and 3.2, an exclusive function for setting the test mode, in which the internal fuctions of the μ PD75316 are tested, is provided to the P00/INT4 and RESET pins.

If a voltage exceeding V_{DD} is applied to either of these pins, the μ PD75316 is put into test mode. Therefore, even when the μ PD75316 is in normal operation, if noise exceeding the V_{DD} is input into any of these pins, the μ PD75316 will enter the test mode, and this will cause problems for normal operation.

As an example, if the wiring to the P00/INT4 pin or the RESET pin is long, stray noise may be picked up and the above montioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- Connect a diode having a low V_F across P00/INT4 and RESET, and V_{DD} .
- Connect a capacitor across P00/INT4 and RESET, and V_{DD} .



4. MEMORY CONFIGURATION

- Program memory (ROM) ...16256 \times 8 bits (0000H-3F7FH): μ PD75316
 ...12160 \times 8 bits (0000H-2F7FH): μ PD75312
 - 0000H, 0001H : Vector table to which address from which program is started is written after reset
 - 0002H-000BH: Vector table to which address from which program is started is written after interrupt
 - 0020H-007FH: Table area referenced by GETI instruction
- Data memory
 - Data area 512 \times 4 bits (000H-1FFH)
 - Peripheral hardware area 128 \times 4 bits (F80H-FFFH)

(a) μPD75316

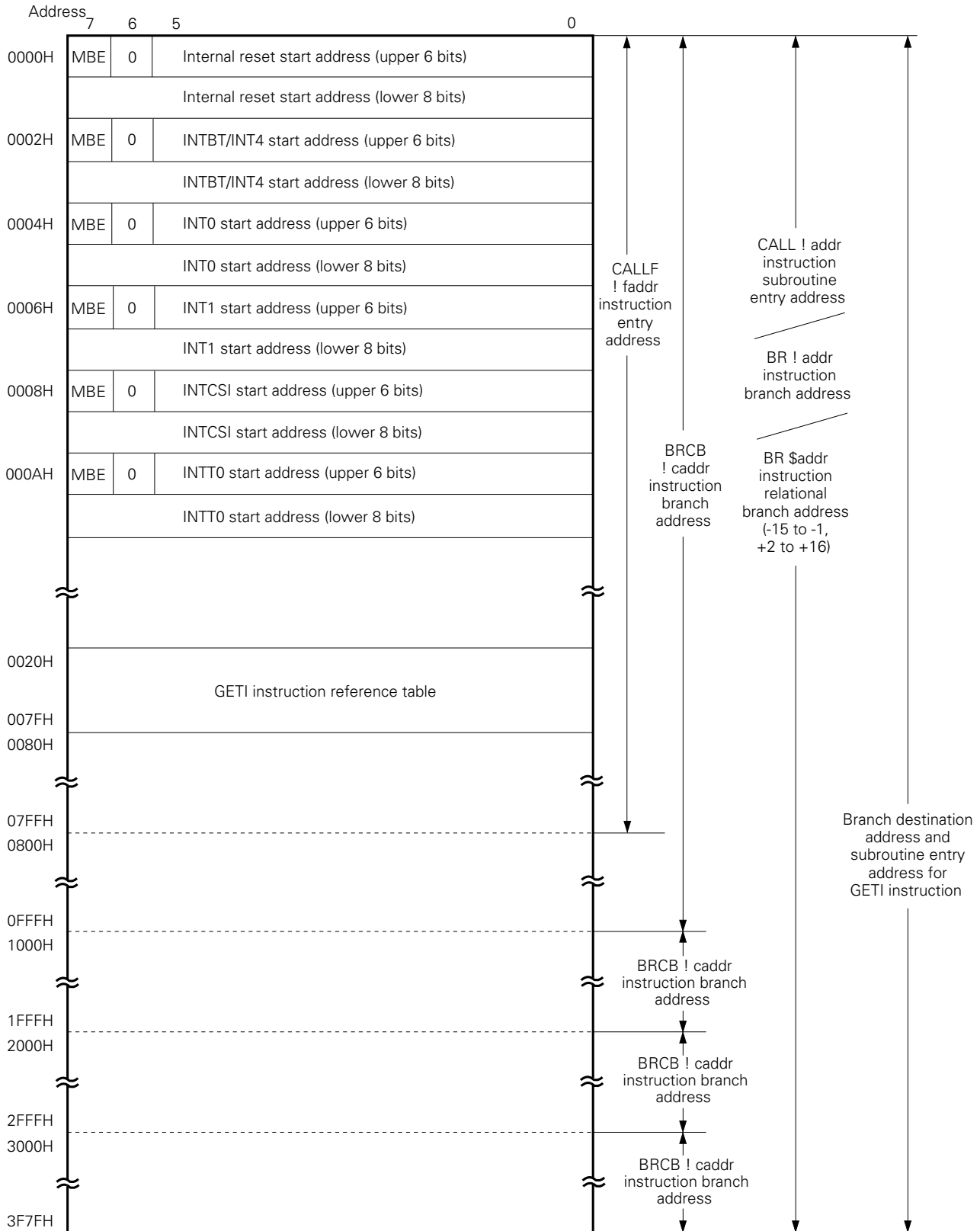


Fig. 4-1 Program Memory Map (1/2)

(b) μPD75312

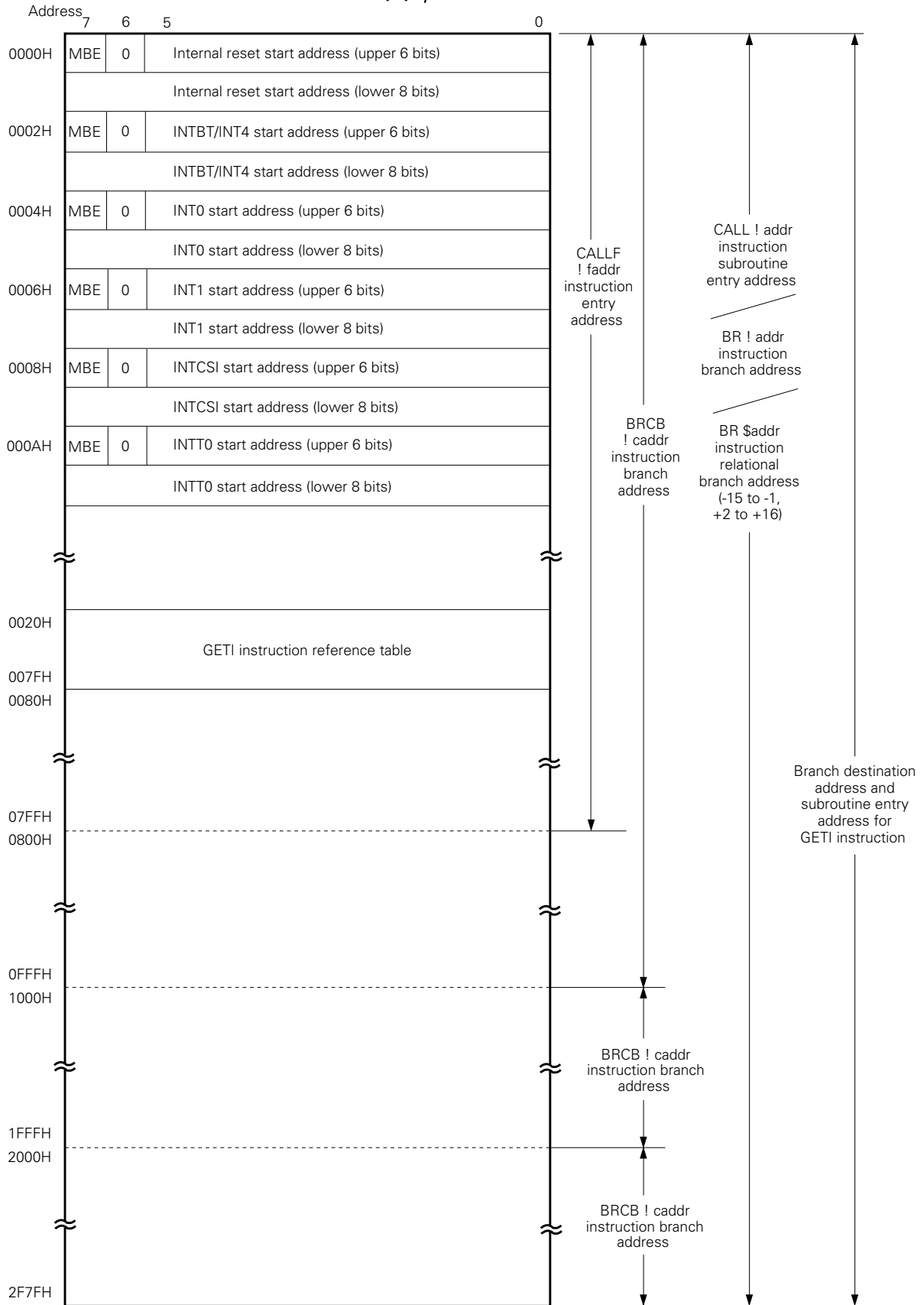


Fig. 4-1 Program Memory Map (2/2)

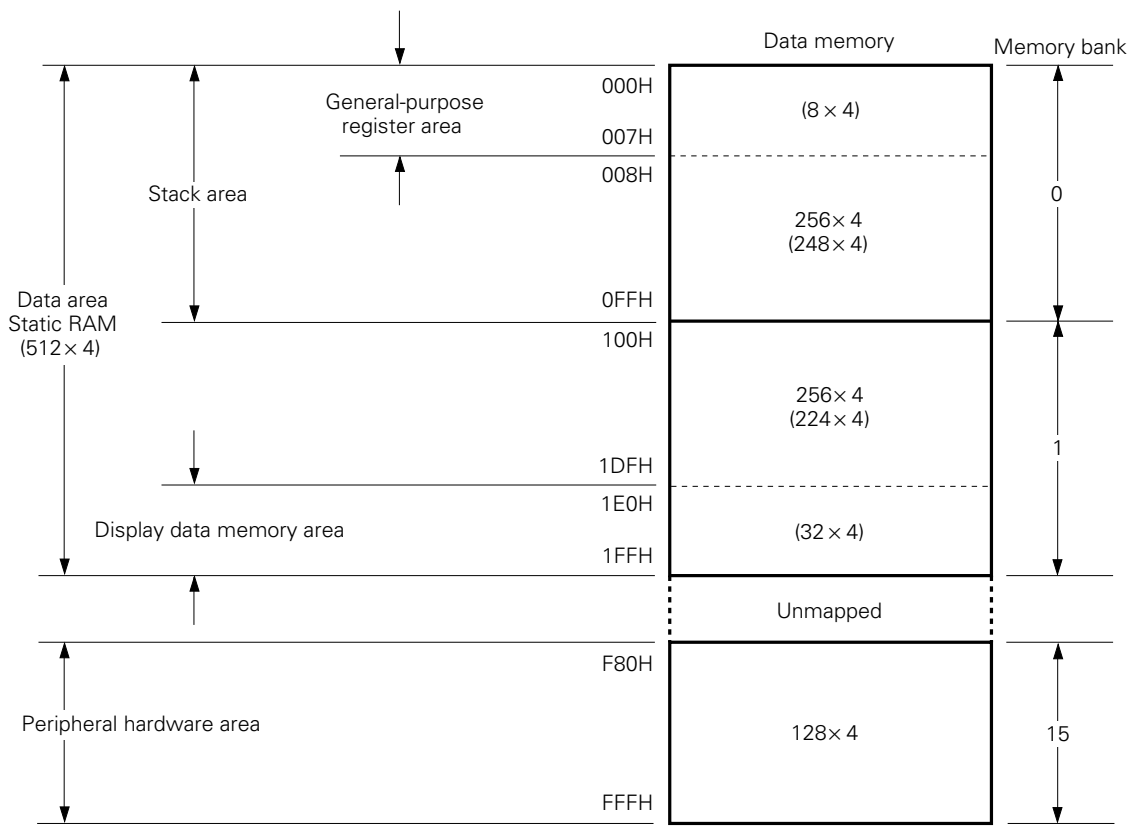


Fig. 4-2 Data Memory Map

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 4 kinds:

- CMOS input (PORT0, 1) : 8
 - CMOS input/output (PORT2, 3, 6, 7) : 16
 - N-ch open-drain (PORT4, 5) : 8
 - CMOS output (BP0-BP7) : 8
-
- Total : 40

Table 5-1 Port Function

Port Name	Function	Operation and Feature	Remarks
PORT0	4-bit input	Can be always read or tested regardless of operation mode of multiplexed pin.	Multiplexed with INT4, SCK, SO/SB0, and SI/SB1
PORT1			Multiplexed with INT0-INT2 and TIO
PORT2	4-bit Input/Output	Can be set in input or output mode in 4-bit units. Ports 6 and 7 are used in pairs to input/output data in 8-bit units.	Multiplexed with PTO0, PCL, and BUZ
PORT7			Multiplexed with KR4-KR7
PORT3 *		Can be set in input or output mode in 1-bit units.	Multiplexed with LCDCL and SYNC
PORT6			Multiplexed with KR0-KR3
PORT4 * PORT5 *	4-bit Input/Output (N-ch open-drain, 10 V)	Can be set in input or output mode in 4-bit units. Ports 4 and 5 are used in pairs to input/output data in 8-bit units.	Can be connected to a pull-up resistor in 1-bit units by using mask option.
BP0-BP7	1-bit output	Output data in 1-bit units. Can be used as LCD drive segment output pins S24-S31 through software.	Low drive capability For driving CMOS load

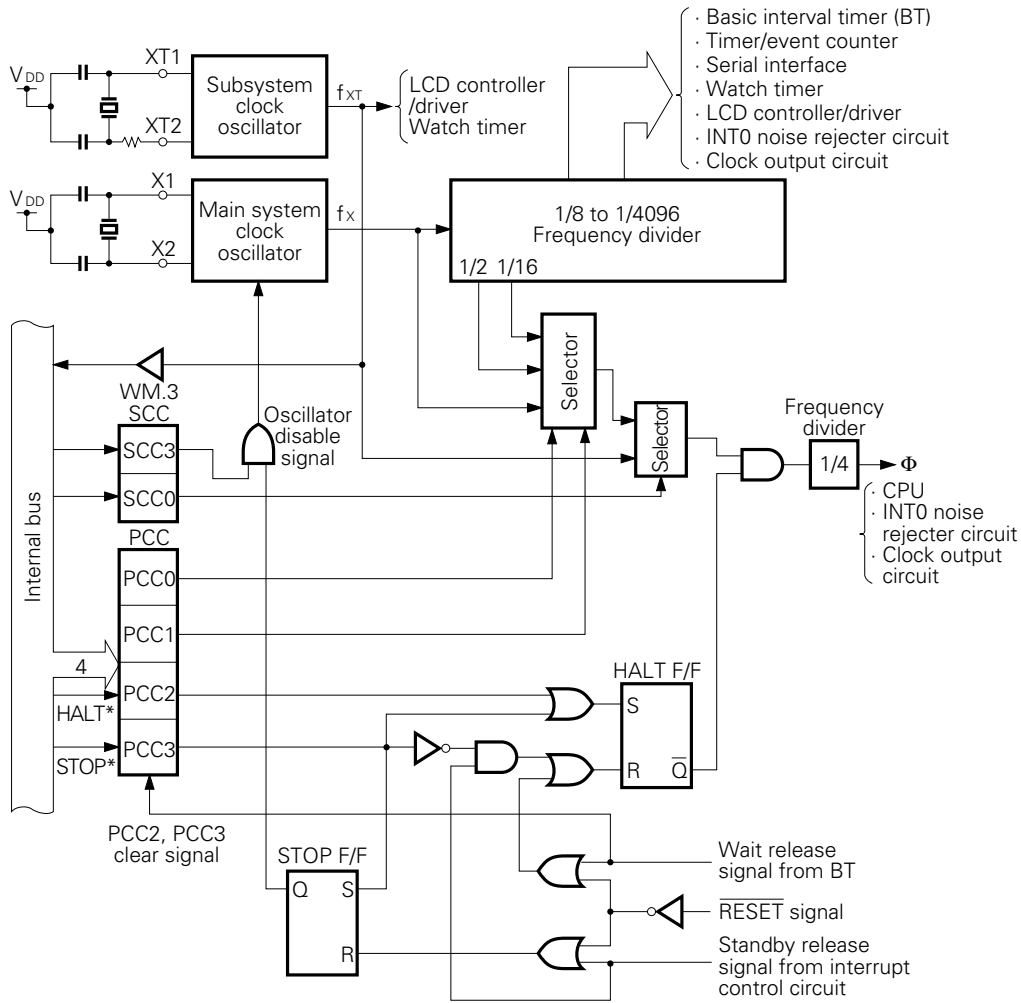
*: Can directly drive LED.

5.2 CLOCK GENERATOR CIRCUIT

The operation of the clock generator circuit is determined by the processor clock control register (PPC) and system clock control register (SCC).

This circuit can generate two types of clocks: main system clock and subsystem clock. In addition, it can also change the instruction execution time.

- 0.95 μ s/1.91 μ s/15.3 μ s (main system clock: 4.19 MHz)
- 122 μ s (subsystem clock: 32.768 kHz)



- Remarks**
- 1: f_X = Main system clock frequency
 - 2: f_{XT} = Subsystem clock frequency
 - 3: PCC: Processor clock control register
 - 4: SCC: System clock control register
 - 5: *: instruction execution.
 - 6: One clock cycle (t_{CY}) of Φ is one machine cycle of an instruction. For t_{CY} , refer to AC characteristics in 11. ELECTRICAL SPECIFICATIONS.

Fig. 5-1 Clock Generator Block Diagram

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock pulse is used for the remote control output, peripheral LSIs, etc.

- Clock output (PCL) : Φ , 524, 262, 65.5 kHz (operating at 4.19 MHz)
- Buzzer output (BUZ) : 2 kHz (operating at 4.19 MHz or 32.768 kHz)

Fig. 5-2 shows the clock output circuit configuration.

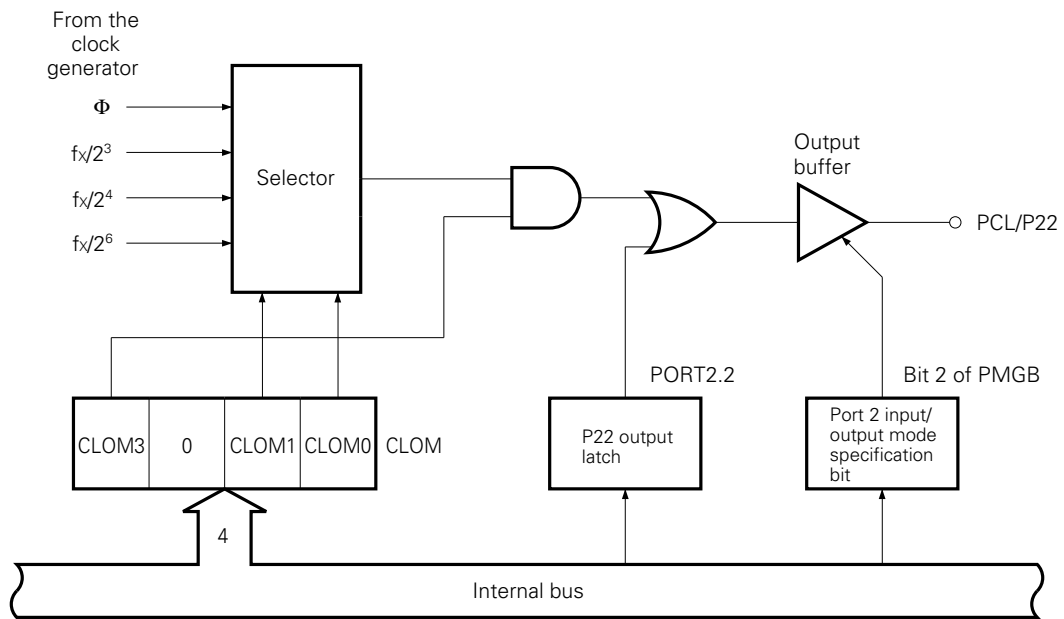


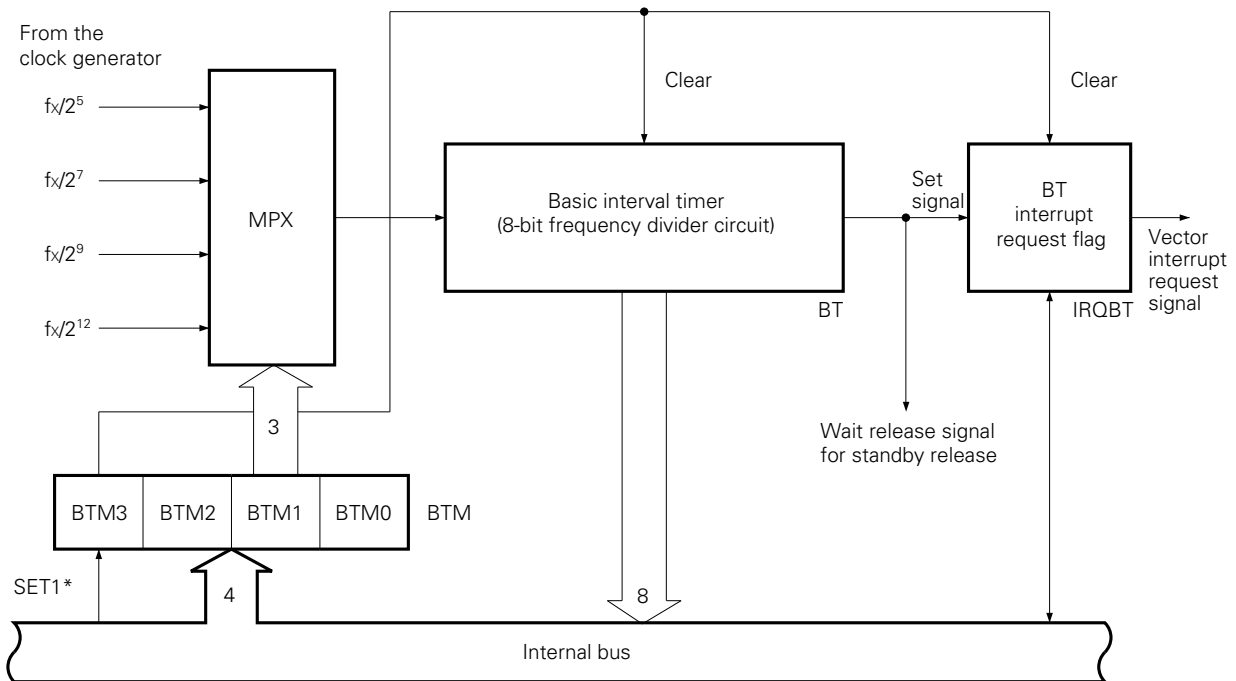
Fig. 5-2 Clock Output Circuit Configuration

Remarks: A measures to prevent outputting narrow width pulse when selecting clock output enable/disable is taken.

5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



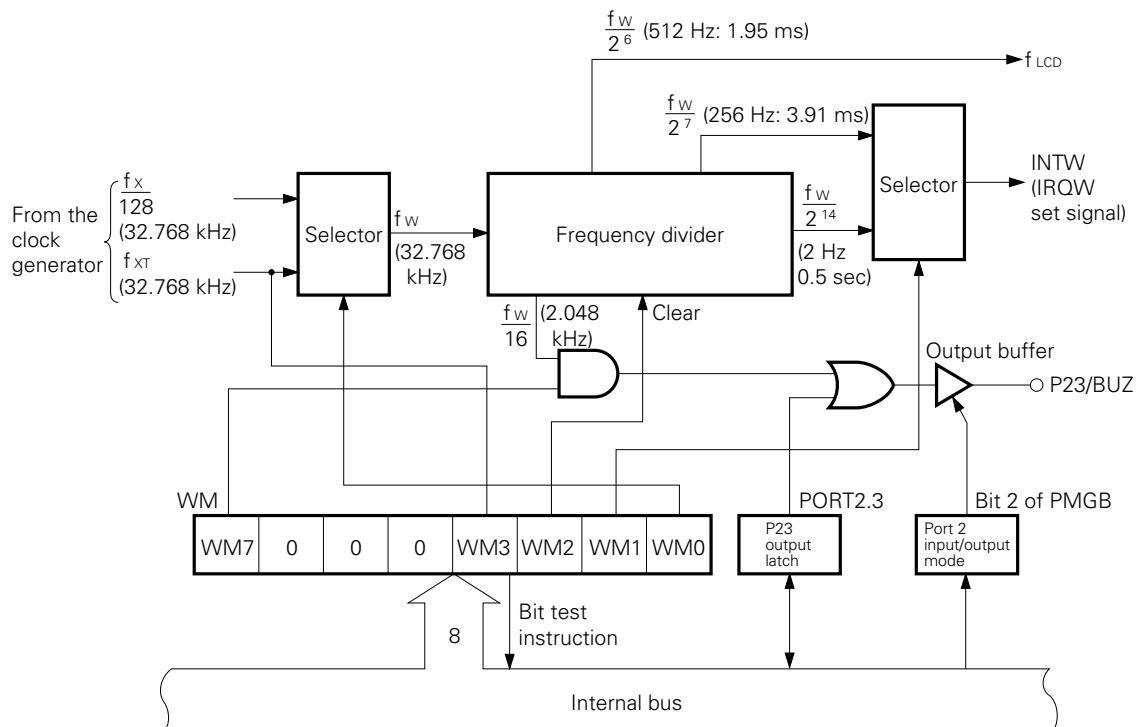
Remarks : *: Instruction execution

Fig. 5-3 Basic Interval Timer Configuration

5.5 WATCH TIMER

The μPD75316 has a built-in 1-ch watch timer. The watch timer is configured as shown in Fig. 5-4.

- Sets the test flag (IRQW) with 0.5 sec interval.
The standby mode can be released by IRQW.
- 0.5 second interval can be generated either from the main system clock or subsystem clock.
- Time interval can be advanced to 128 times faster (3.91 ms) by setting the fast mode. This is convenient for program debugging, test, etc.
- Fixed frequency (2.048 kHz) can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that zero second watch start is possible.



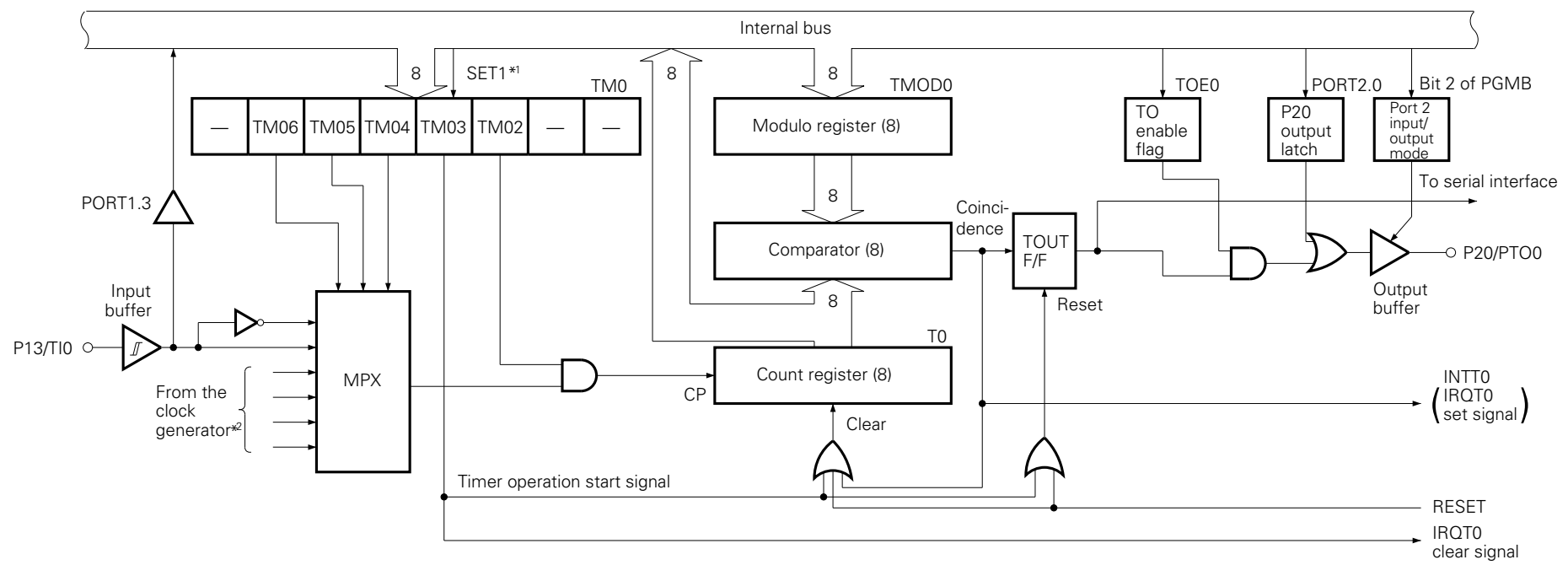
() is for $f_x = 4.194304$ MHz, $f_{xT} = 32.768$ kHz.

Fig. 5-4 Watch Timer Block Diagram

5.6 TIMER/EVENT COUNTER

The μ PD75316 has a built-in 1-ch timer/event counter. The timer/event counter has these functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin.
- Event counter operation
- Divides the T10 pin input in N and outputs to the PTO0 pin (frequency divider operation).
- Supplies serial shift clock to the serial interface circuit.
- Count condition read out function



*1: SET1: Instruction execution
 *2: For details, refer to Fig. 5-1.

Fig. 5-5 Timer/Event Counter Block Diagram

5.7 SERIAL INTERFACE

The μ PD75316 is equipped with an 8-bit clocked serial interface that operates in the following three modes:

- Three-line serial I/O mode
- Two-line serial I/O mode
- SBI mode (serial bus interface mode)

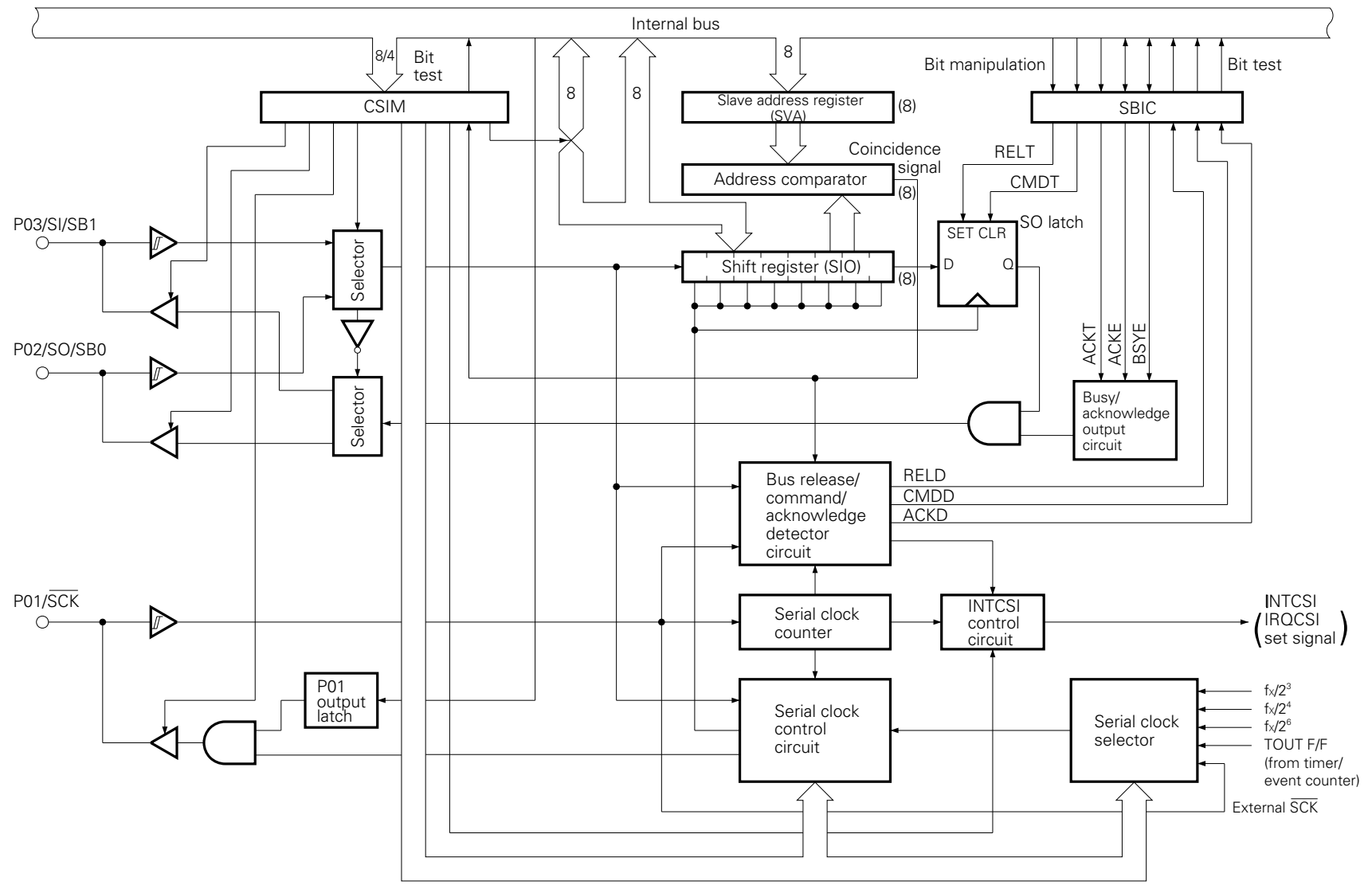


Fig. 5-6 Serial Interface Block Diagram

5.8 LCD CONTROLLER/DRIVER

The μ PD75316 is provided with a display controller that generates segment and common signals and a segment driver and a common driver that can directly drive an LCD panel.

Figure 5-7 shows the LCD controller/driver configuration.

These LCD controller and drivers have the following functions:

- Generate segment and common signals by automatically reading the display data memory by means of DMA
- Five display modes selectable
 - Static
 - 1/2 duty (1/2 bias)
 - 1/3 duty (1/2 bias)
 - 1/3 duty (1/3 bias)
 - 1/4 duty (1/3 bias)
- Four types of frame frequencies selectable in each display mode
- Up to 32 segment signals (S0-S31) and four common signals (COM0-COM3) can be output.
- Four segment signal output pins (S24-S27, S28-S31) can be used as an output port (BP0-BP3, BP4-BP7).
- Dividing resistor for LCD driving power source can be provided (by mask option).
 - All bias modes and LCD drive voltages can be used.
 - Current flowing to dividing resistor can be cut when display is off.
- Display data memory not used for display can be used as ordinary data memory.
- Can also operate on subsystem clock.

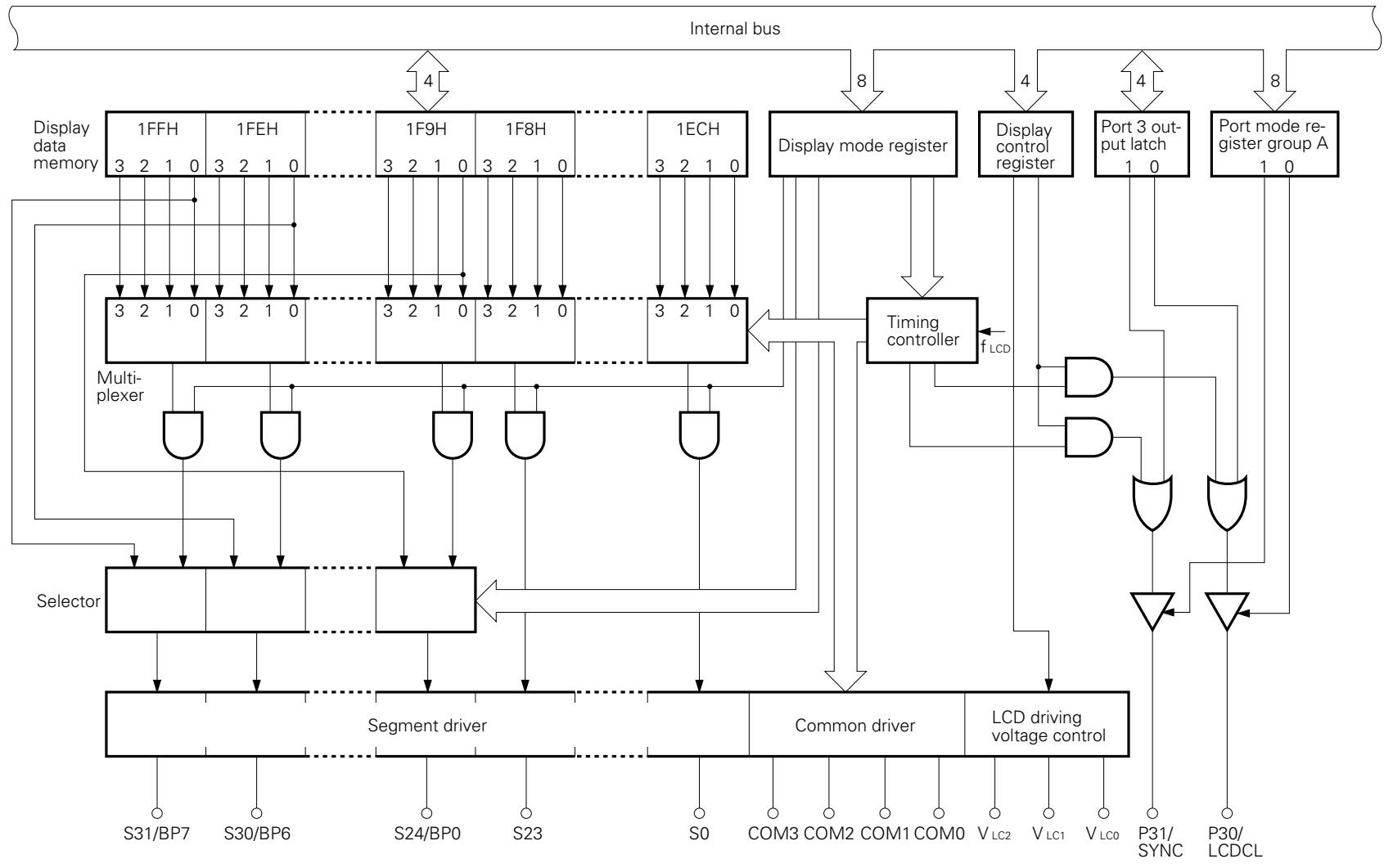
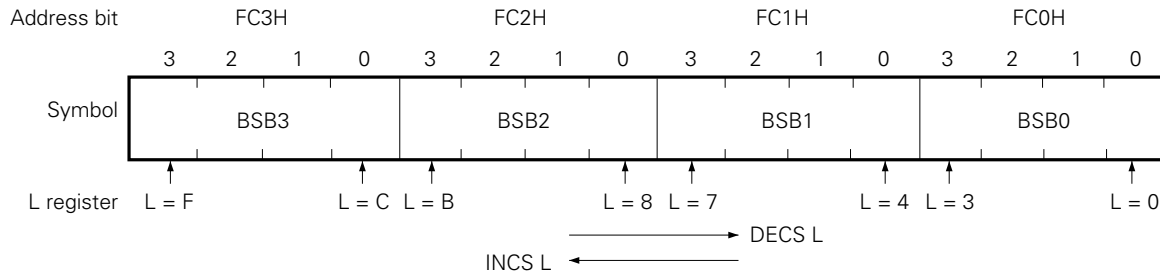


Fig. 5-7 LCD Controller/Driver Block Diagram

5.9 BIT SEQUENTIAL BUFFER 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 5-8 Bit Sequential Buffer Format

6. INTERRUPT FUNCTIONS

The μPD75316 has 6 different interrupt sources. In addition to that, multiple interrupt by software control is also possible. The μPD75316 is also provided with two types of test sources, of which INT2 has two types of edge detection testable inputs.

The interrupt control circuit of the μPD75316 has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

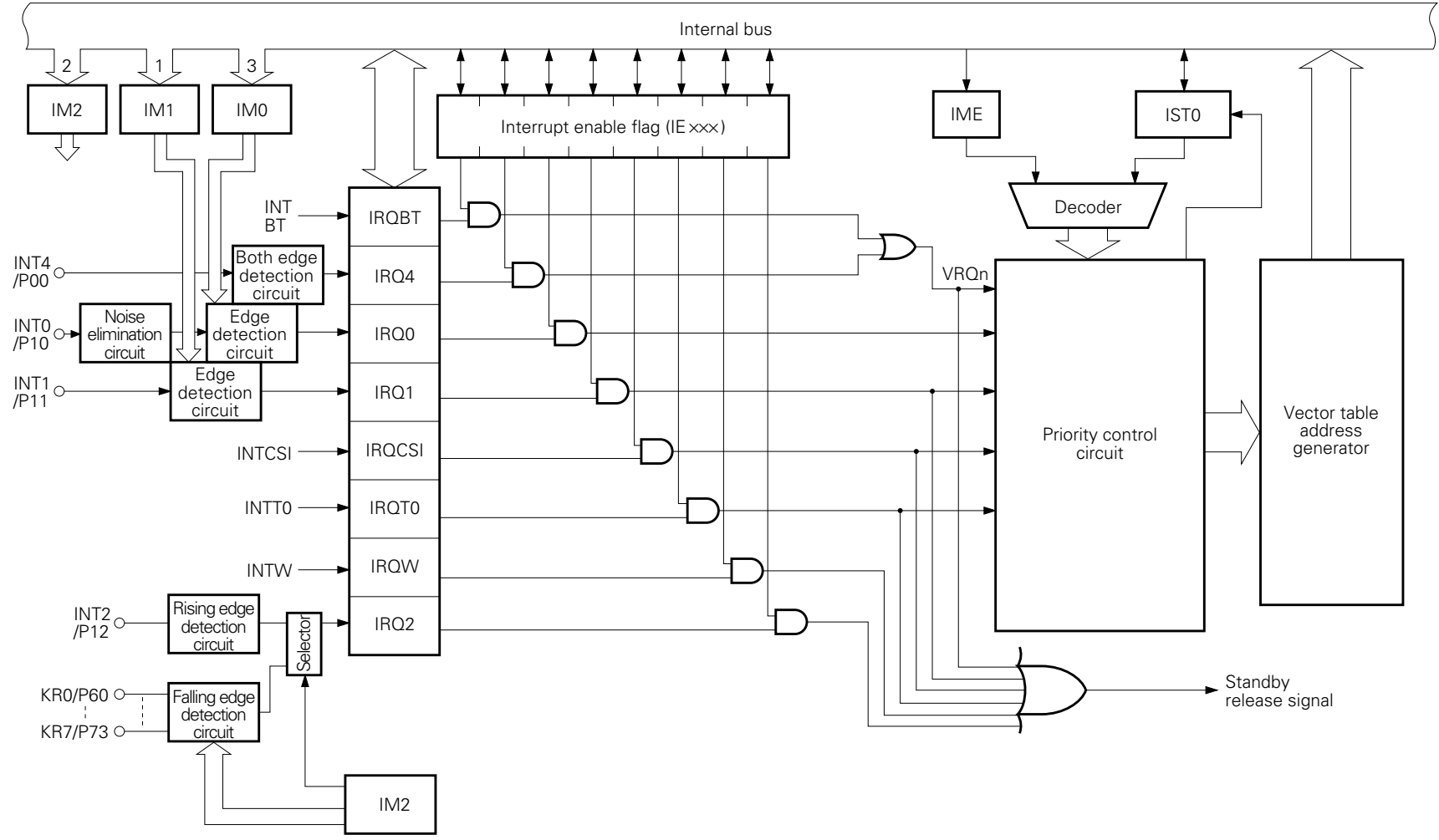


Fig. 6-1 Interrupt Control Block Diagram

7. STANDBY FUNCTIONS

The μPD75316 has two different standby modes (STOP mode and HALT mode) to reduce the power consumption while waiting for program execution.

Table 7-1 Each Status in Standby Mode

		STOP Mode	HALT Mode
Setting Instruction		STOP instruction	HALT instruction
System Clock for Setting		Can be set only when operating on the main system clock	Can be set either with the main system clock or the subsystem clock
Operation Status	Clock Generator	Only the main system clock stops its operation.	Only the CPU clock Φ stops its operation. (oscillation continues)
	Basic Interval Timer	No operation	Operation (Sets IRQBT at reference time interval) *
	Serial Interface	Can operate only when the external SCK input is selected for the serial clock	Can operate *
	Timer/Event Counter	Can operate only when the T10 pin input is selected for the count clock	Can operate *
	Watch Timer	Can operate when f_{XT} is selected for the count clock	Can operate
	LCD Controller	Can operate only when f_{XT} is selected for LCDCL	Can operate
	External Interrupt	INT1, INT2, and INT4 can operate. Only INT0 cannot operate.	
	CPU	No operation	
Release Signal		An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the RESET signal input	An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the RESET signal input

*: Operation is possible only when the main system clock is operating.

8. RESET FUNCTION

When the $\overline{\text{RESET}}$ signal is input, the μPD75316 is reset and each hardware is initialized as indicated in Table 8-1. Fig. 8-1 shows the reset operation timing.

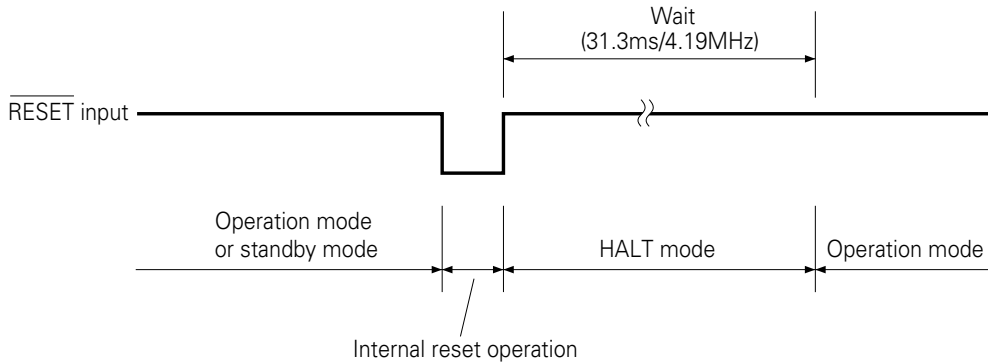


Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

Table 8-1 Status of Each Hardware after Reset (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program Counter (PC)		The contents of the lower 6 bits of address 0000H of the program memory are set to PC13-8, and the contents of address 0001H are set to PC7-0.	The contents of the lower 5 bits of address 0000H of the program memory are set to PC12-8, and the contents of address 0001H are set to PC7-0.
PSW	Carry Flag (CY)	Retained	Undefined
	Skip Flag (SK0-2)	0	0
	Interrupt Status Flag (IST0)	0	0
	Bank Enable Flag (MBE)	The contents of bit 7 of address 0000H of the program memory are set to MBE.	The contents of bit 7 of address 0000H of the program memory are set to MBE.
Stack Pointer (SP)		Undefined	Undefined
Data Memory (RAM)		Retained *	Undefined
General-Purpose Register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank Selection Register (MBS)		0	0
Basic Interval Timer	Counter (BT)	Undefined	Undefined
	Mode Register (BTM)	0	0
Timer/Event Counter	Counter (T0)	0	0
	Module Register (TMOD0)	FFH	FFH
	Mode Register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch Timer	Mode Register (WM)	0	0

*: Data of address 0F8H to 0FDH of the data memory becomes undefined when a $\overline{\text{RESET}}$ signal is input.

Table 8-1 Status of Each Hardware after Reset (2/2)

	Hardware	RESET Input in Standby Mode	RESET Input during Operation
Serial Interface	Shift Register (SIO)	Retained	Undefined
	Operation Mode Register (CSIM)	0	0
	SBI Control Register (SBIC)	0	0
	Slave Address Register (SVA)	Retained	Undefined
Clock Generator, Clock Output Circuit	Processor Clock Control Register (PCC)	0	0
	System Clock Control Register (SCC)	0	0
	Clock Output Mode Register (CLOM)	0	0
LCD Controller	Display Mode Register (LCMD)	0	0
	Display Control Register (LCDC)	0	0
Interrupt Function	Interrupt Request Flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt Enable Flag (IExxx)	0	0
	Interrupt Master Enable Flag (IME)	0	0
	INT0, INT1, INT2 Mode Registers (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital Port	Output Buffer	Off	Off
	Output Latch	Clear (0)	Clear (0)
	Input/Output Mode Register (PMGA, B)	0	0
	Pull-Up Resistor Specification Register (POGA)	0	0
Bit Sequential Buffer (BSB0-3)	Retained	Specified	

9. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and – are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

The symbols in the register and flag symbols can be described as labels in the places of mem, fmem, pmem, and bit (for details, refer to μPD75308 User's Manual (IEM-5016)). However, fmem and pmem restricts the label that can be described.

Representation	Description	
reg	X, A, B, C, D, E, H, L	
reg1	X, B, C, D, E, H, L	
rp	XA, BC, DE, HL	
rp1	BC, DE, HL	
rp2	BC, DE	
rpa	HL, DE, DL	
rpa1	DE, DL	
n4	4-bit immediate data or label	
n8	8-bit immediate data or label	
mem *	8-bit immediate data or label	
bit	2-bit immediate data or label	
fmem	FB0H to FBFH, FF0H to FFFH immediate data or label	
pmem	FC0H to FFFH immediate data or label	
addr	μPD75312	0000H-2F7FH immediate data or label
	μPD75316	0000H-3F7FH immediate data or label
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (where bit0 = 0) or label	
PORTn	PORT0 to PORT7	
IExxx	IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW	
MBn	MB0, MB1, MB15	

*: Only even addresses can be described as mem for 8-bit data processing.

(2) Legend of operation field

A	: A register; 4-bit accumulator
B	: B register; 4-bit accumulator
C	: C register; 4-bit accumulator
D	: D register; 4-bit accumulator
E	: E register; 4-bit accumulator
H	: H register; 4-bit accumulator
L	: L register; 4-bit accumulator
X	: X register; 4-bit accumulator
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC); 8-bit accumulator
DE	: Register pair (DE); 8-bit accumulator
HL	: Register pair (HL); 8-bit accumulator
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; or bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
PORT _n	: Port n (n = 0 to 7)
IME	: Interrupt mask enable flag
IE _{xxx}	: Interrupt enable flag
MBS	: Memory bank selector register
PCC	: Processor clock control register
·	: Delimiter of address and bit
(xx)	: Contents addressed by xx
xxH	: Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)		Data memory addressing
*2	MB = 0		
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)		
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH		
*5	MB = 15, pmem = FC0H-FFFH		
*6	μPD75312	addr = 0000H-2F7FH	Program memory addressing
	μPD75316	addr = 0000H-3F7FH	
*7	addr = (Current PC) - 15 to (Current PC) - 1 (Current PC) + 2 to (Current PC) + 16		
*8	μPD75312	caddr = 0000H-0FFFH (PC ₁₃ = 0, PC ₁₂ = 0) or 1000H-1FFFH (PC ₁₃ = 0, PC ₁₂ = 1) or 2000H-2F7FH (PC ₁₃ = 1, PC ₁₂ = 0)	
	μPD75316	caddr = 0000H-0FFFH (PC ₁₃ = 0, PC ₁₂ = 0) or 1000H-1FFFH (PC ₁₃ = 0, PC ₁₂ = 1) or 2000H-2FFFH (PC ₁₃ = 1, PC ₁₂ = 0) or 3000H-3F7FH (PC ₁₃ = 1, PC ₁₂ = 1)	
*9	faddr = 0000H-07FFH		
*10	taddr = 0020H-007FH		

- Remarks**
- 1: MB indicates memory bank that can be accessed.
 - 2: In *2, MB = 0 regardless of MBE and MBS.
 - 3: In *4 and *5, MB = 15 regardless of MBE and MBS.
 - 4: *6 to *10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped S = 0
- When 1-byte or 2-byte instruction is skipped S = 1
- When 3-byte instruction (BR ! addr or CALL ! addr) is skipped S = 2

Note : The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ , (=t_{CV}), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instruc-tions	Mne-monics	Operand	Bytes	Ma-chine Cyc-les	Operation	Ad-dress-ing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	$A \leftarrow n4$		String effect A
		reg1, #n4	2	2	$reg1 \leftarrow n4$		
		XA, #n8	2	2	$XA \leftarrow n8$		String effect A
		HL, #n8	2	2	$HL \leftarrow n8$		String effect B
		rp2, #n8	2	2	$rp2 \leftarrow n8$		
		A, @HL	1	1	$A \leftarrow (HL)$	*1	
		A, @rpa1	1	1	$A \leftarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftarrow (HL)$	*1	
		@HL, A	1	1	$(HL) \leftarrow A$	*1	
		@HL, XA	2	2	$(HL) \leftarrow XA$	*1	
		A, mem	2	2	$A \leftarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftarrow (mem)$	*3	
		mem, A	2	2	$(mem) \leftarrow A$	*3	
		mem, XA	2	2	$(mem) \leftarrow XA$	*3	
		A, reg	2	2	$A \leftarrow reg$		
		XA, rp	2	2	$XA \leftarrow rp$		
		reg1, A	2	2	$reg1 \leftarrow A$		
		rp1, XA	2	2	$rp1 \leftarrow XA$		
	XCH	A, @HL	1	1	$A \leftrightarrow (HL)$	*1	
		A, @rpa1	1	1	$A \leftrightarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftrightarrow (HL)$	*1	
		A, mem	2	2	$A \leftrightarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftrightarrow (mem)$	*3	
		A, reg1	1	1	$A \leftrightarrow reg1$		
Table Reference	MOVT	XA, @PCDE	1	3	$XA \leftarrow (PC_{13-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	$XA \leftarrow (PC_{13-8}+XA)_{ROM}$		
Arith-metic Opera-tion	ADDS	A, #n4	1	1+S	$A \leftarrow A+n4$		carry
		A, @HL	1	1+S	$A \leftarrow A+(HL)$	*1	carry
	ADDC	A, @HL	1	1	$A, CY \leftarrow A+(HL)+CY$	*1	
		SUBS	A, @HL	1	1+S	$A \leftarrow A-(HL)$	*1
	SUBC	A, @HL	1	1	$A, CY \leftarrow A-(HL)-CY$	*1	
		AND	A, #n4	2	2	$A \leftarrow A \wedge n4$	
	A, @HL		1	1	$A \leftarrow A \wedge (HL)$	*1	
	OR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
	XOR	A, #n4	2	2	$A \leftarrow A \vee n4$		
A, @HL		1	1	$A \leftarrow A \vee (HL)$	*1		
Accum-ulator Manipu-lation	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \bar{A}$		

Instructions	Mne-monics	Operand	Bytes	Ma-chine Cyc-les	Operation	Ad-dress-ing Area	Skip Conditions
Incre-ment/ Decre-ment	INCS	reg	1	1+S	reg ← reg+1		reg = 0
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL) = 0
	mem	2	2+S	(mem) ← (mem)+1	*3	(mem) = 0	
	DECS	reg	1	1+S	reg ← reg-1		reg = FH
Compare	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4		*1 (HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
Carry flag	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
Manipu-lation	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← \overline{CY}		
Memory/ Bit Manipu-lation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem ₇₋₂ + L ₃₋₂ .bit(L ₁₋₀)) ← 1	*5	
		@H+mem.bit	2	2	(H + mem ₃₋₀ .bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem ₇₋₂ + L ₃₋₂ .bit(L ₁₋₀)) ← 0	*5	
		@H+mem.bit	2	2	(H+mem ₃₋₀ .bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem ₇₋₂ +L ₃₋₂ .bit(L ₁₋₀)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H + mem ₃₋₀ .bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if (pmem ₇₋₂ +L ₃₋₂ .bit(L ₁₋₀)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem ₃₋₀ .bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem ₇₋₂ +L ₃₋₂ .bit(L ₁₋₀)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem ₃₋₀ .bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ (pmem ₇₋₂ +L ₃₋₂ .bit(L ₁₋₀))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem ₃₋₀ .bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ (pmem ₇₋₂ +L ₃₋₂ .bit(L ₁₋₀))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem ₃₋₀ .bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY ⊕ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ⊕ (pmem ₇₋₂ +L ₃₋₂ .bit(L ₁₋₀))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ⊕ (H+mem ₃₋₀ .bit)	*1	

Instruc-tions	Mne-monics	Operand	Bytes	Ma-chine Cycles	Operation	Ad-dress-ing Area	Skip Conditions
Branch	BR	addr	—	—	PC ₁₃₋₀ ← addr (The most suitable instruction is selectable from among BR !addr, BRCB !caddr, and BR \$addr depending on the assembler.)	*6	
		!addr	3	3	PC ₁₃₋₀ ← addr	*6	
		\$addr	1	2	PC ₁₃₋₀ ← addr	*7	
	BRCB	!caddr	2	2	PC ₁₃₋₀ ← PC _{13,12} + caddr ₁₁₋₀	*8	
Subrou-tine/ Stack Control	CALL	!addr	3	3	(SP-4)(SP-1)(SP-2) ← PC ₁₁₋₀ (SP-3) ← MBE, 0, PC ₁₃ , PC ₁₂ PC ₁₃₋₀ ← addr, SP ← SP-4	*6	
	CALLF	!faddr	2	2	(SP-4)(SP-1)(SP-2) ← PC ₁₁₋₀ (SP-3) ← MBE, 0, PC ₁₃ , PC ₁₂ PC ₁₃₋₀ ← 00, faddr, SP ← SP-4	*9	
	RET		1	3	MBE, PC ₁₃ , PC ₁₂ ← (SP+1) _{3,1,0} PC ₁₁₋₀ ← (SP)(SP+3)(SP+2) SP ← SP+4		
	RETS		1	3+S	MBE, PC ₁₃ , PC ₁₂ ← (SP+1) _{3,1,0} PC ₁₁₋₀ ← (SP)(SP+3)(SP+2) SP ← SP+4, then skip unconditionally		Undefined
	RETI		1	3	PC ₁₃ , PC ₁₂ ← (SP+1) _{1,0} PC ₁₁₋₀ ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
		PUSH	rp	1	1	(SP-1)(SP-2) ← rp, SP ← SP-2	
		BS	2	2	(SP-1) ← MBS, (SP-2) ← 0, SP ← SP-2		
		POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP+2	
	BS		2	2	MBS ← (SP+1), SP ← SP+2		
Inter-rupt Control	EI		2	2	IME ← 1		
		!Exxx	2	2	!Exxx ← 1		
	DI		2	2	IME ← 0		
		!Exxx	2	2	!Exxx ← 0		
I/O	IN	A,PORT _n	2	2	A ← PORT _n (n = 0-7)		
		XA,PORT _n	2	2	XA ← PORT _{n+1} ,PORT _n (n = 4, 6)		
	OUT	PORT _n ,A	2	2	PORT _n ← A (n = 2-7)		
		PORT _n ,XA	2	2	PORT _{n+1} ,PORT _n ← XA (n = 4, 6)		
CPU Control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	MB _n	2	2	MBS ← n (n = 0-3, 15)		
	GETI	taddr	1	3	· Where TBR instruction, PC ₁₃₋₀ ← (taddr) ₅₋₀ +(taddr+1) · Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC ₁₁₋₀ (SP-3) ← MBE, 0, PC ₁₃ , PC ₁₂ PC ₁₃₋₀ ← (taddr) ₅₋₀ +(taddr+1) SP ← SP-4 · Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)	*10	Depends on referenced instruction

Note: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

Remarks: The TBR and TCALL instructions are the assembler pseudo-instructions for the table definition of GETI instruction.

10. SELECTION OF MASK OPTION

The following mask operations are available and can be specified for each pin.

Pin	Mask Option
P40-P43, P50-P53	<ul style="list-style-type: none"> • With pull-up resistor (Specification in bit units) • Without pull-up resistor (Specification in bit units)
V _{LC0} -V _{LC2} , BIAS	<ul style="list-style-type: none"> • With dividing resistor for LCD drive power source (Specification in 4-bit units) • Without dividing resistor for LCD drive power source (Specification in 4-bit units)

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V _{DD}			-0.3 to +7.0	V
Input Voltage	V _{I1}	Other than ports 4, 5		-0.3 to V _{DD} +0.3	V
	V _{I2}	Ports 4, 5	w/pull-up resistor	-0.3 to V _{DD} +0.3	V
			Open drain	-0.3 to +11	V
Output Voltage	V _O			-0.3 to V _{DD} +0.3	V
High-Level Output Current	I _{OH}	1 pin		-15	mA
		All pins		-30	mA
Low-Level Output Current	I _{OL} *	1 pin	Peak	30	mA
			rms	15	mA
		Other than ports 0, 2, 3, 5	Peak	100	mA
			rms	60	mA
		Total of ports 4, 6, 7	Peak	100	mA
			rms	60	mA
Operating Temperature	T _{opt}			-40 to +85	°C
Storage Temperature	T _{stg}			-65 to +150	°C

*: rms = Peak value x √Duty

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C _{IN}	f = 1 MHz			15	pF
Output Capacitance	C _{OUT}	Pins other than those measured are at 0 V			15	pF
Input/Output Capacitance	C _{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic *3		Oscillation frequency(f _x)*1	V _{DD} = oscillation voltage range	1.0		5.0 ^{*3}	MHz
		Oscillation stabilization time*2	After V _{DD} came to MIN. of oscillation voltage range			4	ms
Crystal *3		Oscillation frequency (f _x)*1		1.0	4.19	5.0 ^{*3}	MHz
		Oscillation stabilization time*2	V _{DD} = 4.5 to 6.0 V			10	ms
External Clock		X1 input frequency (f _x)*1		1.0		5.0 ^{*3}	MHz
		X1 input high-, low-level widths (t _{xH} , t _{xL})		100		500	ns

*1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit.

For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range or the STOP mode has been released.

3: When the oscillation frequency is 4.19 MHz < f_x ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs. ★

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f _{xT})		32	32.768	35	kHz
		Oscillation stabilization time*	V _{DD} = 4.5 to 6.0 V			1.0	2
External Clock		XT1 input frequency (f _{xT})*		32		100	kHz
		XT1 input high-, low-level widths (t _{xTH} , t _{xTL})		5		15	μs

*: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

★ **Note:** When using the oscillation circuit of the main system clock and subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD} . Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

RECOMMENDED OSCILLATION CIRCUIT CONSTANTS

MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR ($T_a = -40$ to $+85^\circ\text{C}$)

Manufacturer	Product Name	External Capacitance (pF)		Operating Voltage Range (V)		Remarks
		C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSA 2.00MG093	15	15	2.5	3.5	*
	CSB 1000D20	220	220	2.7	6.0	
	CSA 2.00MG093 CSA 4.19MGU CSA 4.91MGU	30	30			
	CST 2.00MG093 CST 4.19MGU CST 4.91MGU	Unnecessary	Unnecessary			
Kyoto Ceramic Co., Ltd.	KBR-1000H	100	100	3.0	6.0	
	KBR-2.0MS	68	68			
	KBR-4.0MS KBR-4.19MS KBR-4.91MS	33	33			

*: When CSA2.00MG093 is used, the supply voltage is $V_{DD} = 2.5$ to 3.5 [V].

MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR ($T_a = -20$ to $+70^\circ\text{C}$)

Manufacturer	Frequency (MHz)	Retainer	External Capacitance (pF)		Operating Voltage Range		Remarks
			C1	C2	MIN. (V)	MAX. (V)	
Kinseki	1.00 2.00 4.19 4.91	HC-18/U HC-49/U HC-43/U	22	22	2.7	6.0	

SUBSYSTEM CLOCK: 32.768 kHz CRYSTAL OSCILLATOR ($T_a = -10$ to $+60^\circ\text{C}$)

Manufacturer	Product Name	External Circuit Constants			Operating Voltage Range		Remarks
		C3 (pF)	C4 (pF)	R (kΩ)	MIN. (V)	MAX. (V)	
Kinseki	P-3	22	22	330	2.7	6.0	

Note: Fine-tune the oscillation frequency of the crystal oscillator at the external capacitance C1 side.

DC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
High-Level Input Voltage	V _{IH1}	Ports 2, 3	0.7V _{DD}		V _{DD}	V	
	V _{IH2}	Ports 0, 1, 6, 7, RESET	0.8V _{DD}		V _{DD}	V	
	V _{IH3}	Ports 4, 5	w/pull-up resistor	0.7V _{DD}		V _{DD}	V
			Open-drain	0.7V _{DD}		10	V
V _{IH4}	X1, X2, XT1	V _{DD} -0.5		V _{DD}	V		
Low-level Input Voltage	V _{IL1}	Ports 2, 3, 4, 5	0		0.3V _{DD}	V	
	V _{IL2}	Ports 0, 1, 6, 7, RESET	0		0.2V _{DD}	V	
	V _{IL3}	X1, X2, XT1	0		0.4	V	
High-Level Output Voltage	V _{OH1}	Ports 0, 2, 3, 6, 7 and BIAS	V _{DD} = 4.5 to 6.0 V I _{OH} = -1 mA	V _{DD} -1.0		V	
			I _{OH} = -100 μA	V _{DD} -0.5		V	
	V _{OH2}	BP0-7 (with two I _{OH} outputs)	V _{DD} = 4.5 to 6.0 V I _{OH} = -100 μA	V _{DD} -2.0		V	
			I _{OH} = -30 μA	V _{DD} -1.0		V	
Low-Level Output Voltage	V _{OL1}	Ports 0, 2, 3, 4, 5, 6, 7, and 8	Ports 3, 4, and 5 V _{DD} = 4.5 to 6.0 V I _{OL} = -15 mA		0.4	2.0	V
			V _{DD} = 4.5 to 6.0 V I _{OL} = 1.6 mA			0.4	V
			I _{OL} = 400 μA			0.5	V
		SB0, 1	Open-drain Pull-up resistor ≥ 1 kΩ			0.2V _{DD}	V
	V _{OL2}	BP0-7 (with two I _{OL} outputs)	V _{DD} = 4.5 to 6.0 V I _{OL} = 100 μA			1.0	V
			I _{OL} = 50 μA			1.0	V
High-Level Input Leakage Current	I _{LIH1}	V _{IN} = V _{DD}	Other than below			3	μA
			X1, X2, XT1			20	μA
	I _{LIH3}	V _{IN} = 10 V	Ports 4, 5 (open-drain)			20	μA
Low-Level Input Leakage Current	I _{LIL1}	V _{IN} = 0 V	Other than below			-3	μA
			X1, X2, XT1			-20	μA
High-Level Output Leakage Current	I _{LOH1}	V _{OUT} = V _{DD}	Other than below			3	μA
			V _{OUT} = 10 V	Ports 4, 5 (open-drain)			20
Low-Level Output Leakage Current	I _{LOL}	V _{OUT} = 0 V				-3	μA
Internal Pull-Up Resistor	R _{L1}	Ports 0, 1, 2, 3, 6, 7 (except P00) V _{IN} = 0V	V _{DD} = 5.0 V±10%	15	40	80	kΩ
			V _{DD} = 3.0 V±10%	30		300	kΩ
	R _{L2}	Ports 4, 5 V _{OUT} = V _{DD} -2.0 V	V _{DD} = 5.0 V±10%	15	40	70	kΩ
			V _{DD} = 3.0 V±10%	10		60	kΩ
LCD Drive Voltage	V _{LCD}		2.5		V _{DD}	V	
LCD Step-down Resistor	R _{LCD}		60	100	150	kΩ	
LCD Output Voltage Deviation (Common) *1	V _{ODC}	I _o = ±5 μA	V _{LCD0} = V _{LCD} V _{LCD1} = V _{LCD} ×2/3	0		±0.2	V
LCD Output Voltage Deviation (Segment)	V _{ODS}	I _o = ±1 μA	V _{LCD2} = V _{LCD} ×1/3 2.7 V ≤ V _{LCD} ≤ V _{DD}	0		±0.2	V

(to be cont'd)

(cont'd)

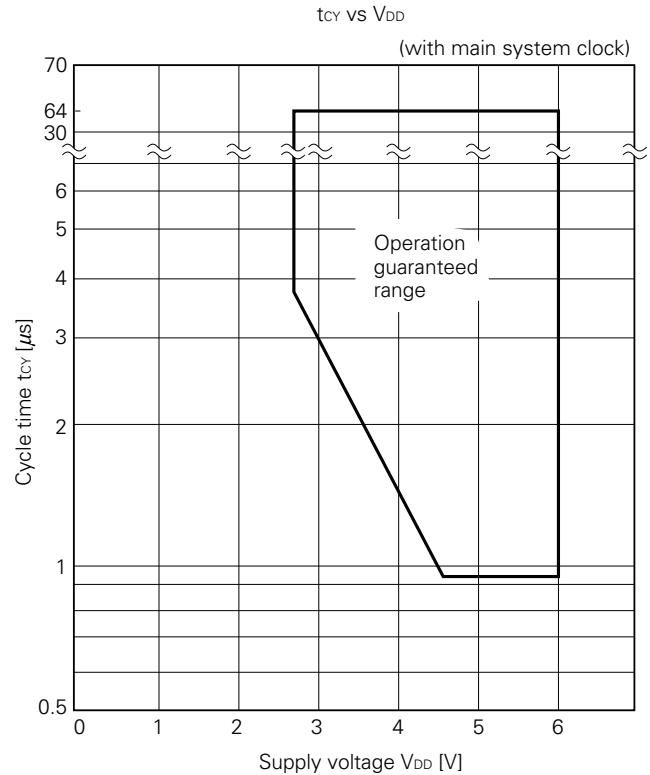
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Supply Current *2	IDD1	4.19 MHz*3 crystal oscillator C1 = C2 = 22pF	V _{DD} = 5 V±10%*4		2.5	8	mA
			V _{DD} = 3 V±10%*5		0.35	1.2	mA
	IDD2	HALT mode	V _{DD} = 5 V±10%		500	1500	μA
			V _{DD} = 3 V±10%		150	450	μA
	IDD3	32 kHz*6 crystal oscillator	V _{DD} = 3 V±10%		30	90	μA
	IDD4		HALT mode V _{DD} = 3 V±10%		5	15	μA
	IDD5	XT1 = 0 V STOP mode	V _{DD} = 5 V±10%		0.5	20	μA
			V _{DD} = 3 V±10%		0.1	10	μA
T _a = 25°C				0.1	5	μA	

- *1: "Voltage deviation" means the difference between the ideal segment or common output value (V_{LCDn}: n = 0, 1, 2) and output voltage.
- 2: Currents for the built-in pull-up resistor and the LCD step-down resistor are not included.
- 3: Including when the subsystem clock is operated.
- 4: When operand in the high-speed mode with the processor clock control register (PCC) set to 0011.
- 5: When operated in the low-speed mode with the PCC set to 0000.
- 6: When operated with the subsystem clock by setting the system clock control register (SCC) to 1001 to stop the main system clock operation.

AC CHARACTERISTICS ($T_a = -40$ to $+85^\circ\text{C}$, $V_{DD} = 2.7$ to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
CPU Clock Cycle Time (Minimum Instruction Execution Time = 1 Machine Cycle)*1	t_{CY}	w/main system clock	$V_{DD} = 4.5$ to 6.0 V	0.95		64	μs
				3.8		64	μs
		w/sub-system clock		114	122	125	μs
TIO Input Frequency	f_{TI}	$V_{DD} = 4.5$ to 6.0 V		0	1	MHz	
				0	275	kHz	
TIO Input High-, Low-Level Widths	t_{TIH} , t_{TIL}	$V_{DD} = 4.5$ to 6.0 V		0.48		μs	
				1.8		μs	
Interrupt Input High-, Low-Level Widths	t_{INTH} , t_{INTL}	INT0	*2			μs	
		INT1, 2, 4	10			μs	
		KR0-7	10			μs	
RESET Low-Level Width	t_{RSL}		10			μs	

- *1: The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC). The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.
- 2: $2t_{CY}$ or $128/f_x$ depending on the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

Two-Line and Three-Line Serial I/O Modes (SCK: internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK Cycle Time	t _{KCY1}	V _{DD} = 4.5 to 6.0 V	1600			ns
			3800			ns
SCK High-, Low-Level Widths	t _{KL1}	V _{DD} = 4.5 to 6.0 V	t _{KCY1} /2-50			ns
	t _{KH1}		t _{KCY1} /2-150			ns
SI Set-Up Time (vs. SCK ↑)	t _{SIK1}		150			ns
SI Hold Time (vs. SCK ↑)	t _{SI1}		400			ns
SCK ↓→ SO Output Delay Time	t _{KSO1}	R _L = 1 kΩ, C _L = 100 pF*	V _{DD} = 4.5 to 6.0 V		250	ns
					1000	ns

TWO-LINE AND THREE-LINE SERIAL I/O MODES (SCK: external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK Cycle Time	t _{KCY2}	V _{DD} = 4.5 to 6.0 V	800			ns
			3200			ns
SCK High-, Low-Level Widths	t _{KL2}	V _{DD} = 4.5 to 6.0 V	400			ns
	t _{KH2}		1600			ns
SI Set-Up Time (vs. SCK ↑)	t _{SIK2}		100			ns
SI Hold Time (vs. SCK ↑)	t _{SI2}		400			ns
SCK ↓→ SO Output Delay Time	t _{KSO2}	R _L = 1 kΩ, C _L = 100 pF*	V _{DD} = 4.5 to 6.0 V		300	ns
					1000	ns

*: R_L and C_L are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{\text{SCK}}$: internal clock output (master))

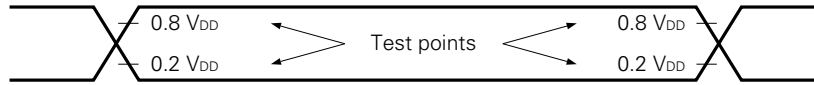
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK Cycle Time	t _{KCY3}	V _{DD} = 4.5 to 6.0 V	1600			ns
			3800			ns
SCK High-, Low-Level Widths	t _{KL3} t _{KH3}	V _{DD} = 4.5 to 6.0 V	t _{KCY3} /2-50			ns
			t _{KCY3} /2-150			ns
SB0, 1 Set-Up Time (vs. SCK ↑)	t _{SIK3}		150			ns
SB0, 1 Hold Time (vs. SCK ↑)	t _{KSI3}		t _{KCY3} /2			ns
SCK ↓← SB0, 1 Output Delay Time	t _{KSO3}	R _L = 1 kΩ, C _L = 100 pF*	V _{DD} = 4.5 to 6.0 V	0	250	ns
				0	1000	ns
$\overline{\text{SCK}}$ ↑→ SB0, 1 ↓	t _{KSB}		t _{KCY3}			ns
SB0,1 ↓→ $\overline{\text{SCK}}$	t _{SBK}		t _{KCY3}			ns
SB0, 1 Low-Level Width	t _{SBL}		t _{KCY3}			ns
SB0, 1 High-Level Width	t _{SBH}		t _{KCY3}			ns

SBI MODE ($\overline{\text{SCK}}$: external clock input (slave))

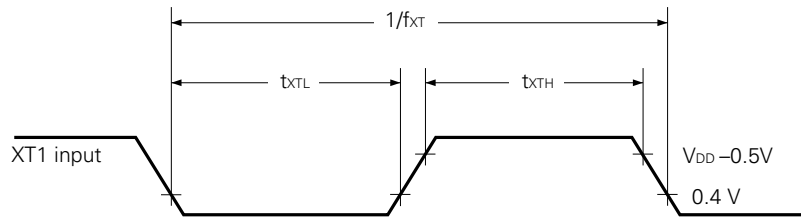
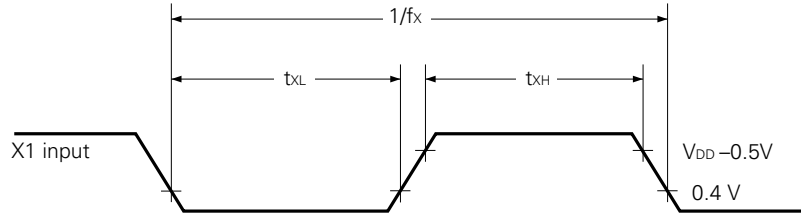
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK Cycle Time	t _{KCY4}	V _{DD} = 4.5 to 6.0 V	800			ns
			3200			ns
SCK High-, Low-Level Widths	t _{KL4} t _{KH4}	V _{DD} = 4.5 to 6.0 V	400			ns
			1600			ns
SB0, 1 Set-Up Time (vs. $\overline{\text{SCK}}$ ↑)	t _{SIK4}		100			ns
SB0, 1 Hold Time (vs. $\overline{\text{SCK}}$ ↑)	t _{KSI4}		t _{KCY4} /2			ns
$\overline{\text{SCK}}$ ↓→ SB0, 1 Output Delay Time	t _{KSO4}	R _L = 1 kΩ, C _L = 100 pF*	V _{DD} = 4.5 to 6.0 V	0	300	ns
				0	1000	ns
$\overline{\text{SCK}}$ ↑→ SB0, 1 ↓	t _{KSB}		t _{KCY4}			ns
SB0,1 ↓→ $\overline{\text{SCK}}$ ↓	t _{SBK}		t _{KCY4}			ns
SB0, 1 Low-Level Width	t _{SBL}		t _{KCY4}			ns
SB0, 1 High-Level Width	t _{SBH}		t _{KCY4}			ns

*: R_L and C_L are load resistance and load capacitance of the SB0 and SB1 output lines.

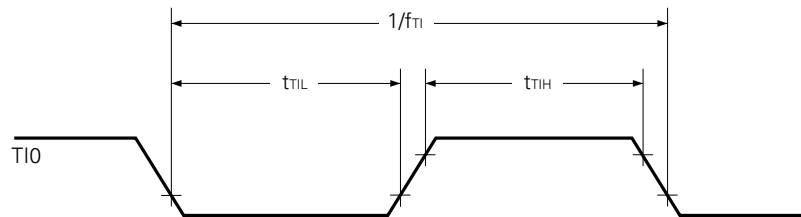
AC TIMING TEST POINT (excluding X1 and XT1 inputs)



CLOCK TIMING

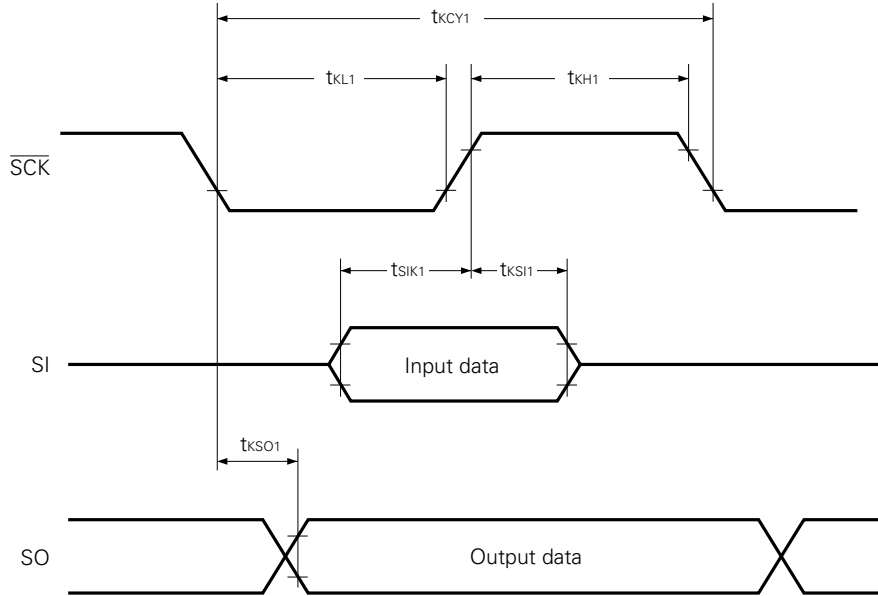


T10 TIMING

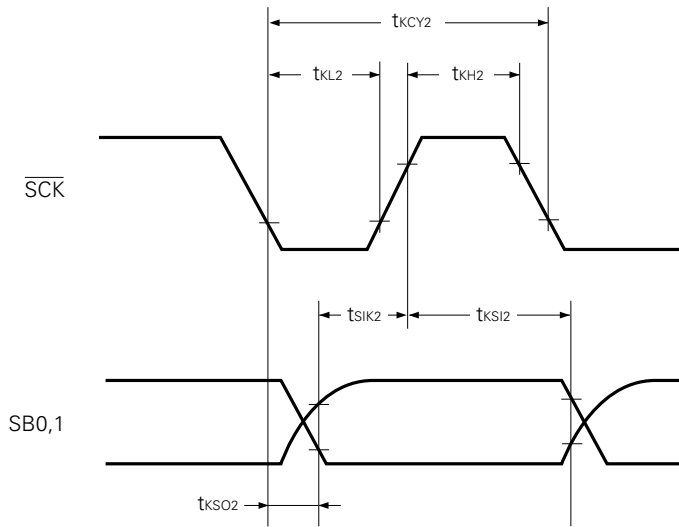


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

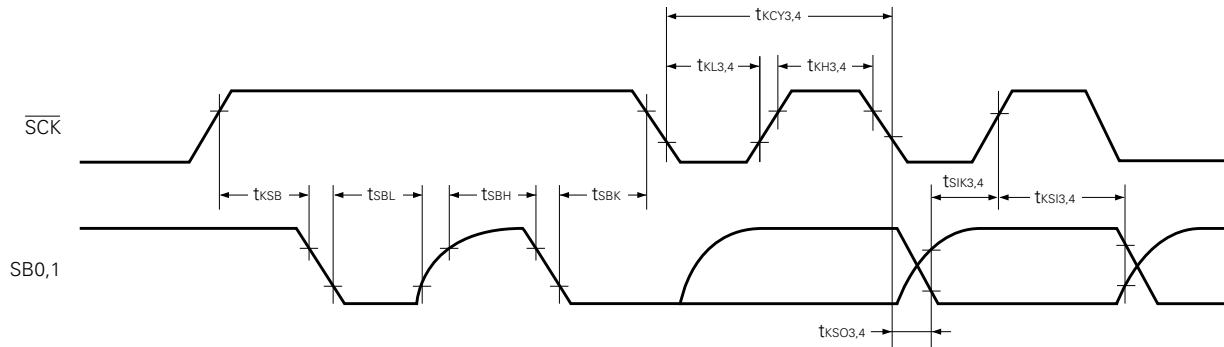


TWO-LINE SERIAL I/O MODE:

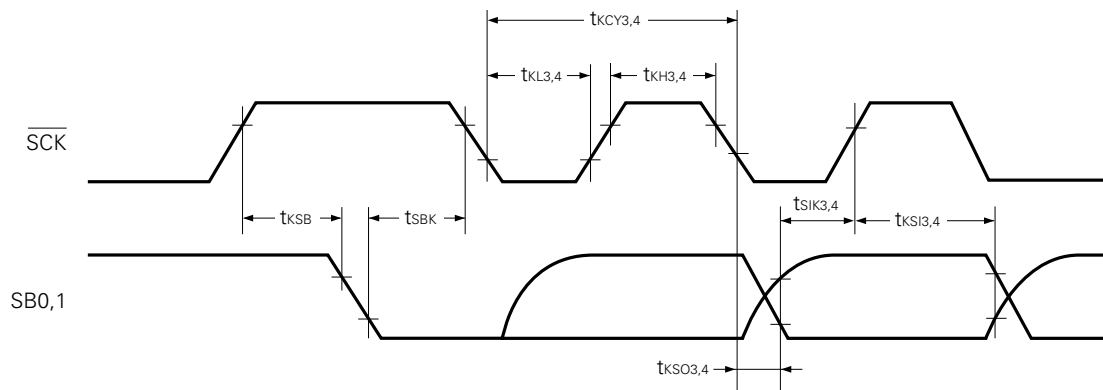


SERIAL TRANSFER TIMING

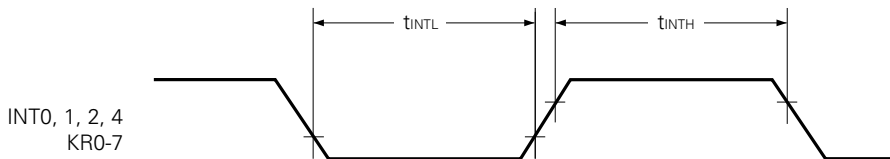
BUS RELEASE SIGNAL TRANSFER:



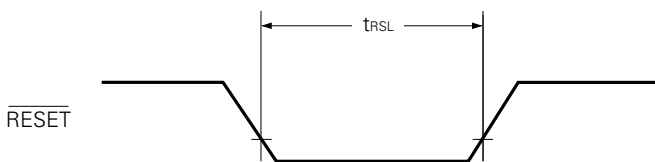
COMMAND SIGNAL TRANSFER:



INTERRUPT INPUT TIMING:



RESET INPUT TIMING:



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

($T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	$V_{DDDR} = 2.0\text{ V}$		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{\text{RESET}}$		$2^{17}/f_x$		ms
		Released by interrupt		*3		ms

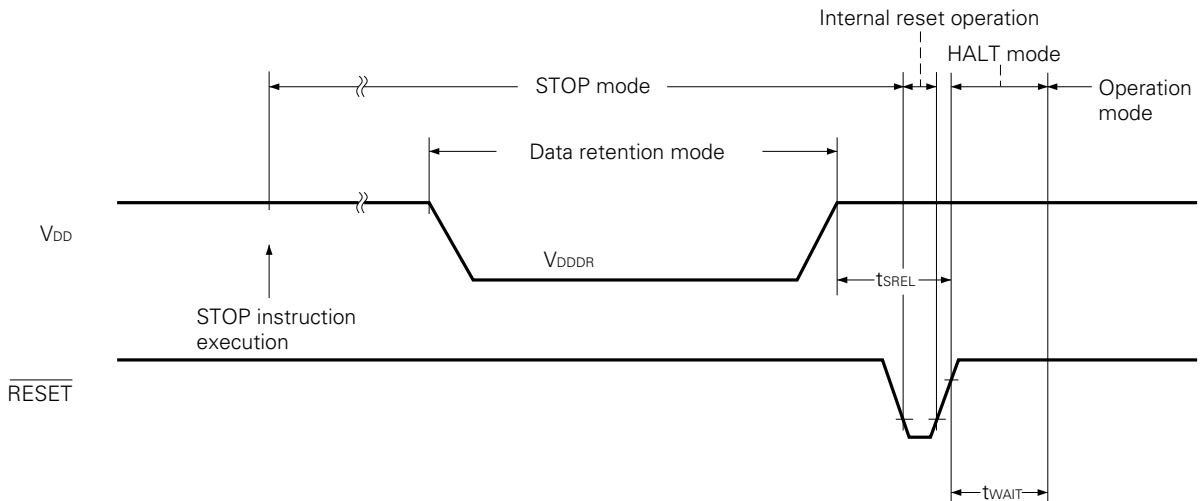
*1: Does not include current flowing through internal pull-up resistor

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

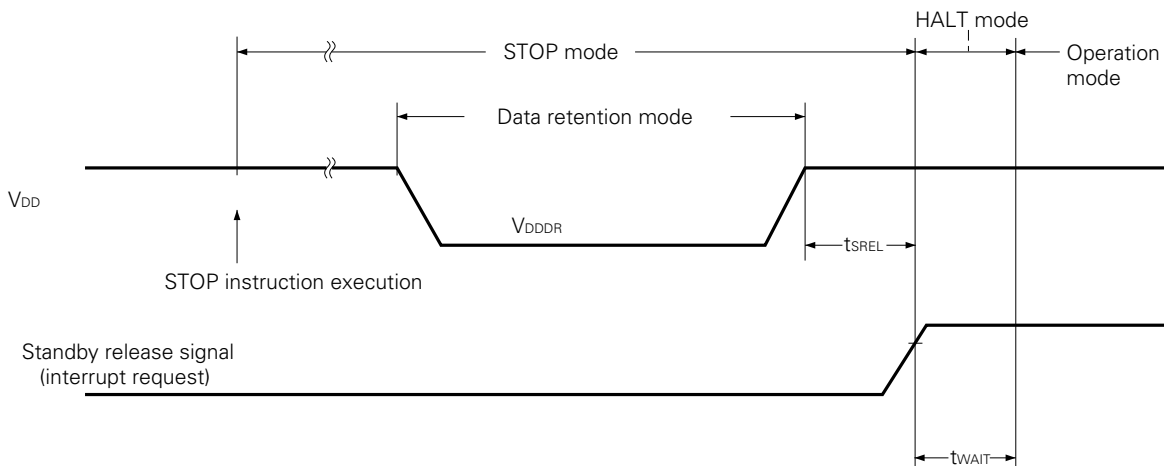
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time (): $f_x = 4.19\text{ MHz}$
-	0	0	0	$2^{20}/f_x$ (approx. 250 ms)
-	0	1	1	$2^{17}/f_x$ (approx. 31.3 ms)
-	1	0	1	$2^{15}/f_x$ (approx. 7.82 ms)
-	1	1	1	$2^{13}/f_x$ (approx. 1.95 ms)

DATA RETENTION TIMING (releasing STOP mode by $\overline{\text{RESET}}$)



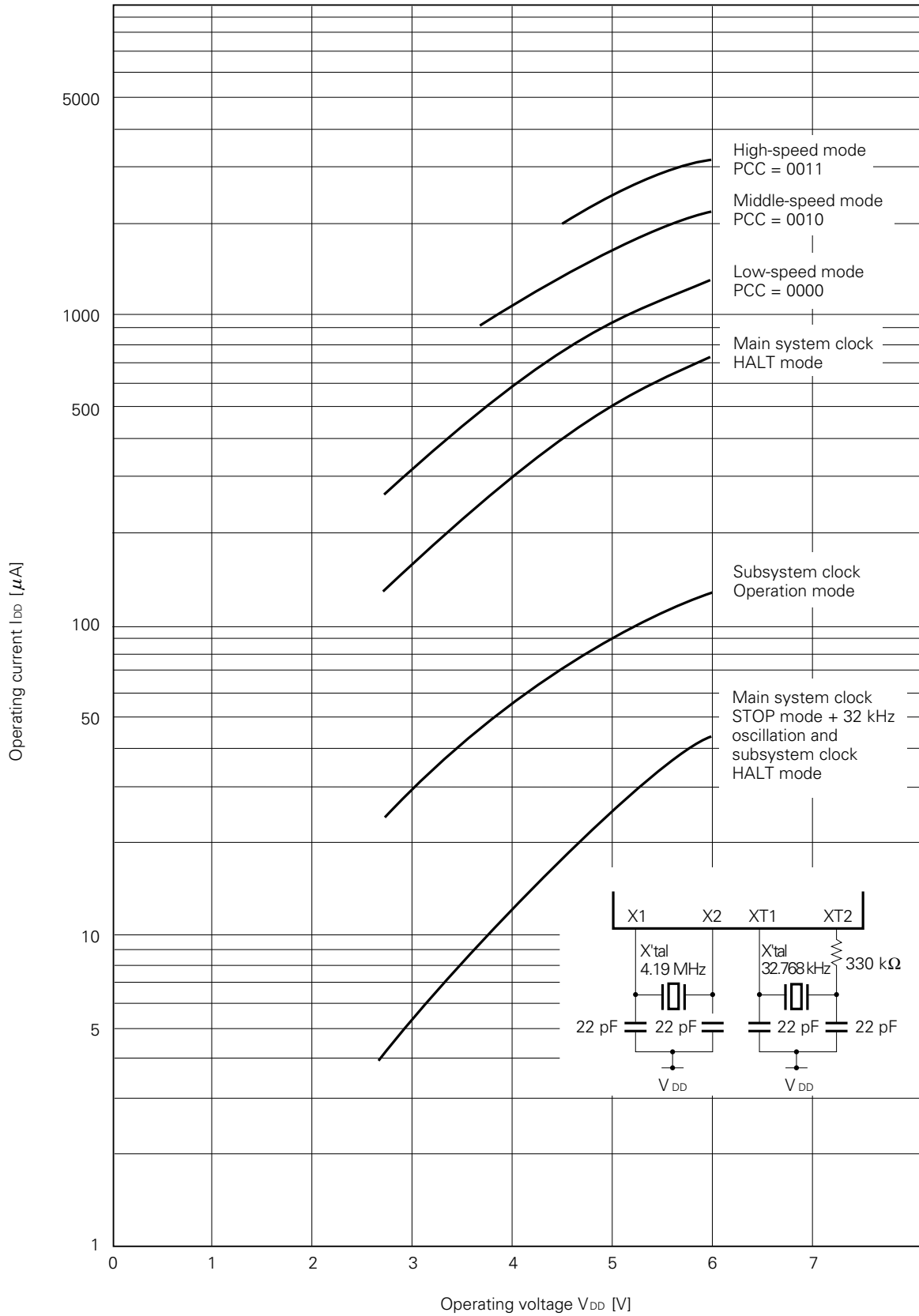
DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



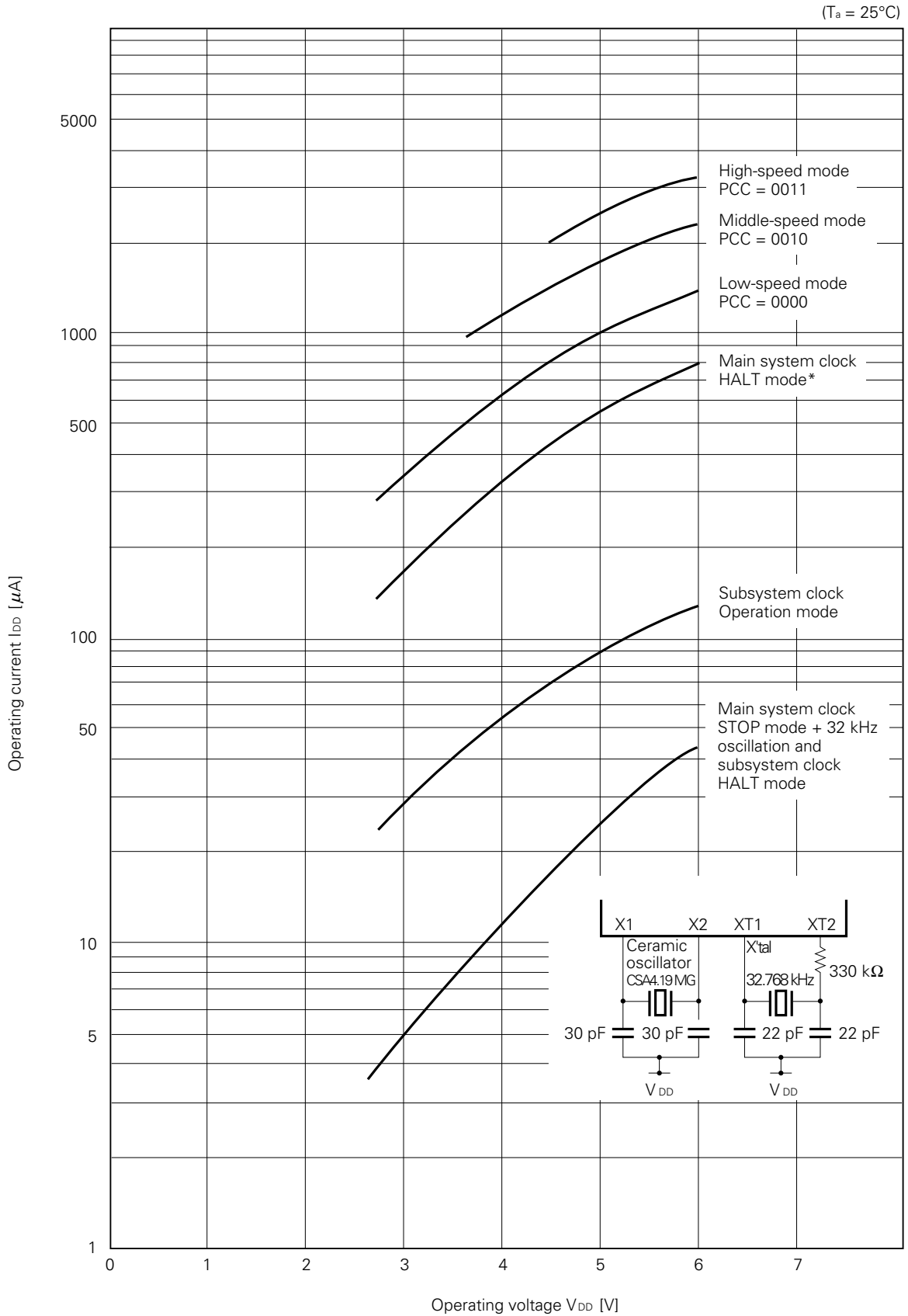
12. CHARACTERISTIC CURVES (REFERENCE VALUE)

I_{DD} vs V_{DD} (Crystal oscillation: 4.19 MHz)

(T_a = 25°C)



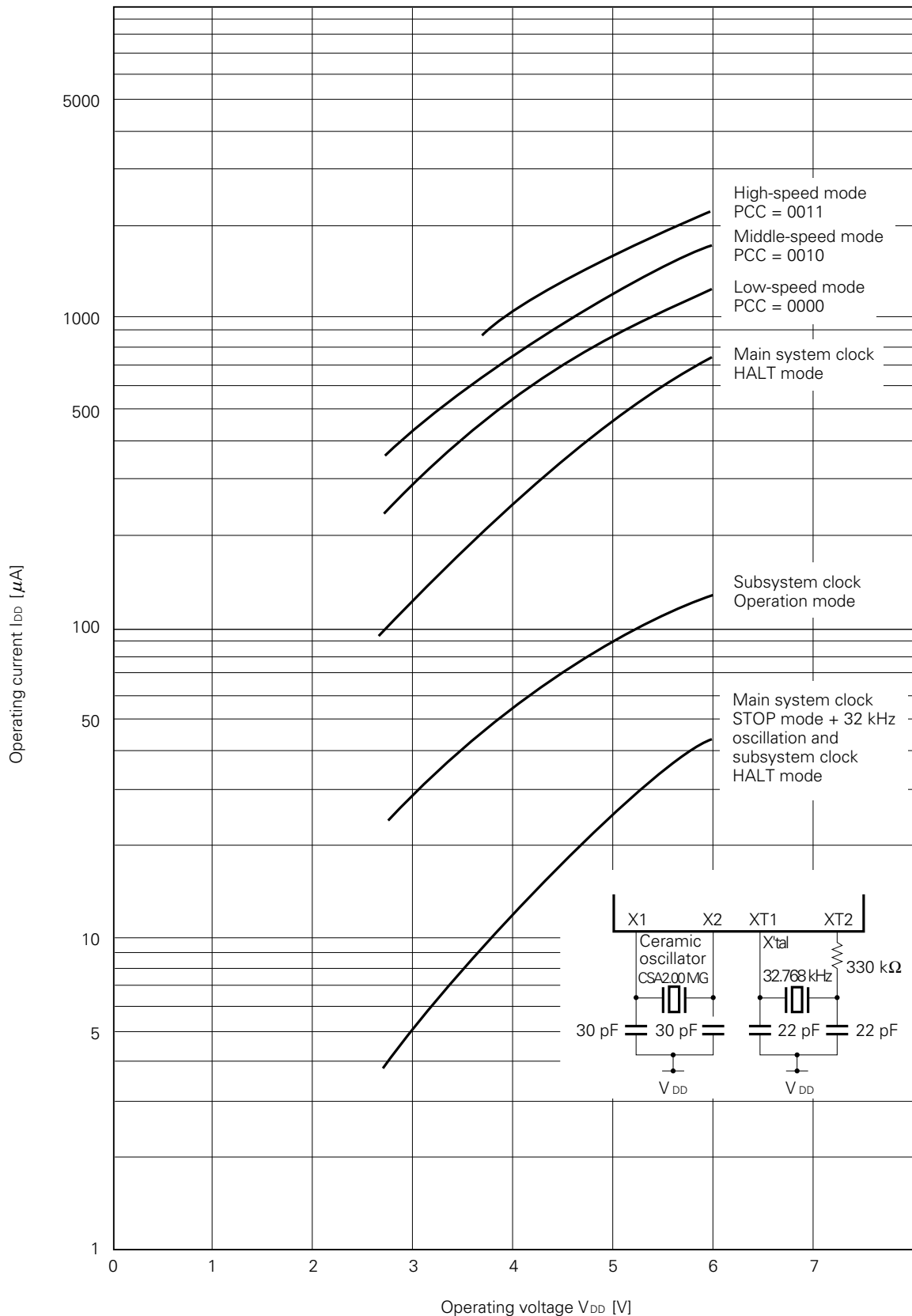
I_{DD} vs V_{DD} (Ceramic oscillation: 4.19 MHz)



*: When compared to crystal oscillation, increased by approximately 10%.

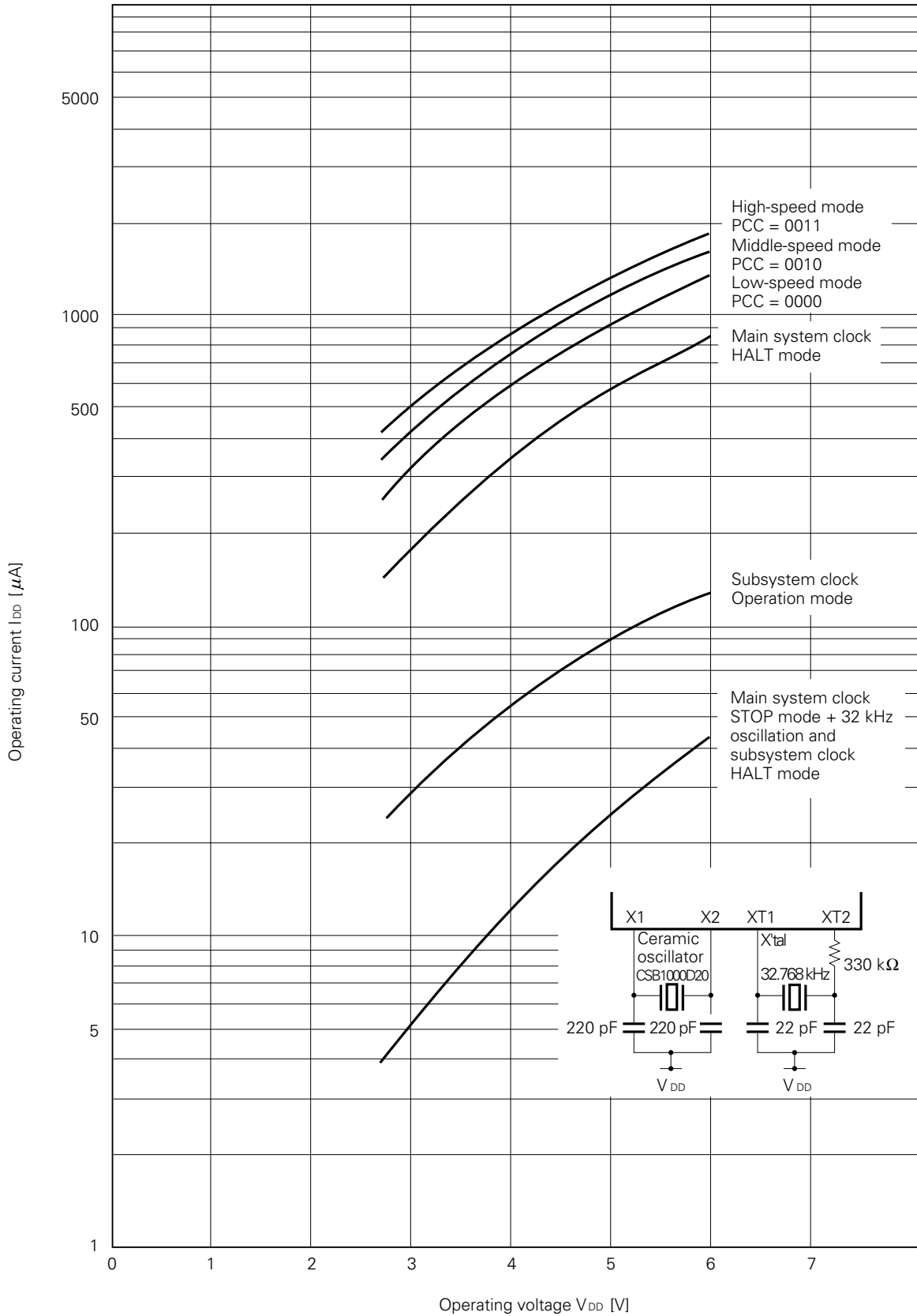
I_{DD} vs V_{DD} (Ceramic oscillation: 2.00 MHz)

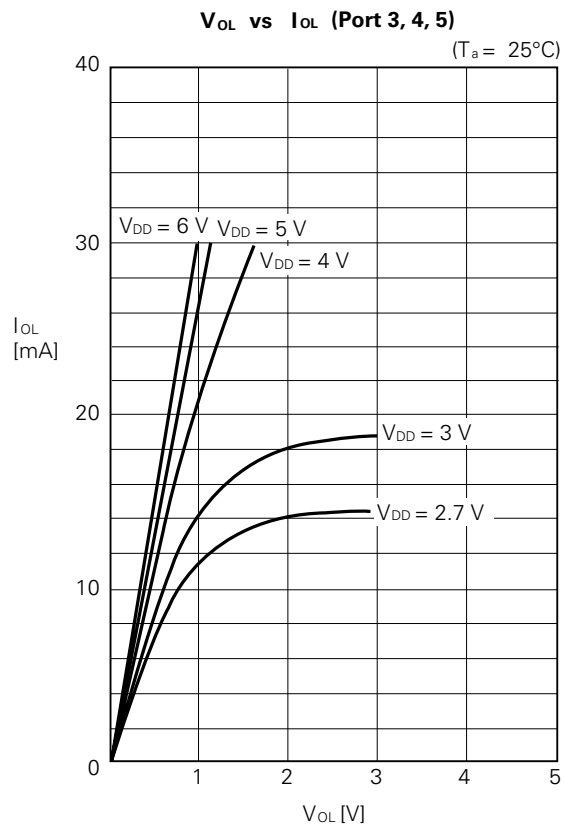
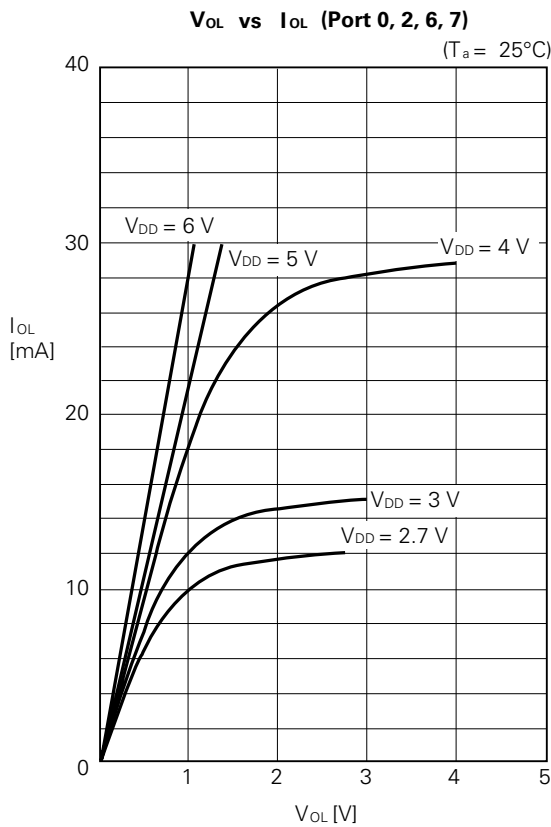
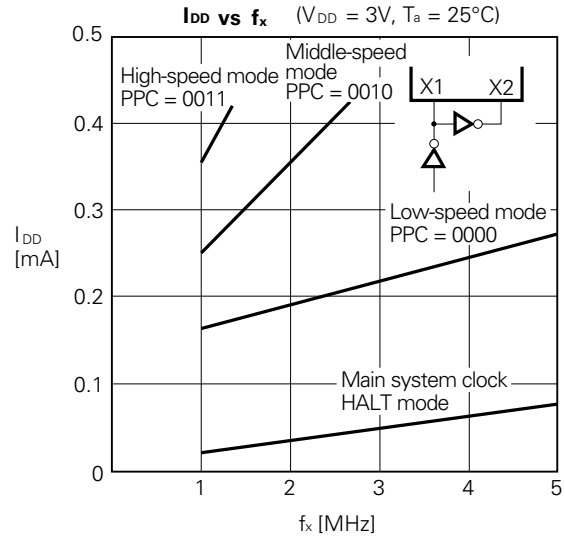
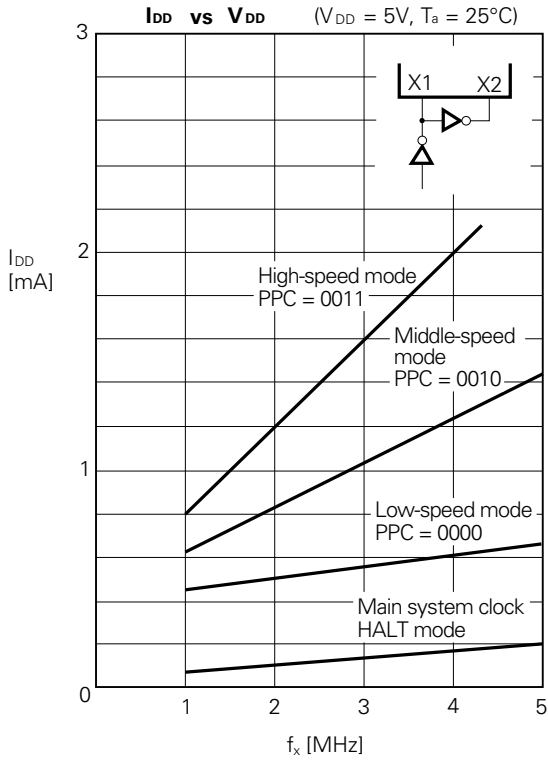
($T_a = 25^\circ\text{C}$)

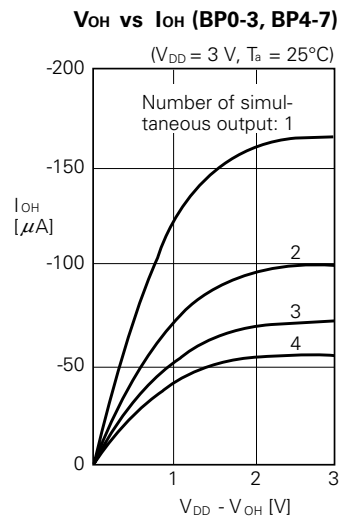
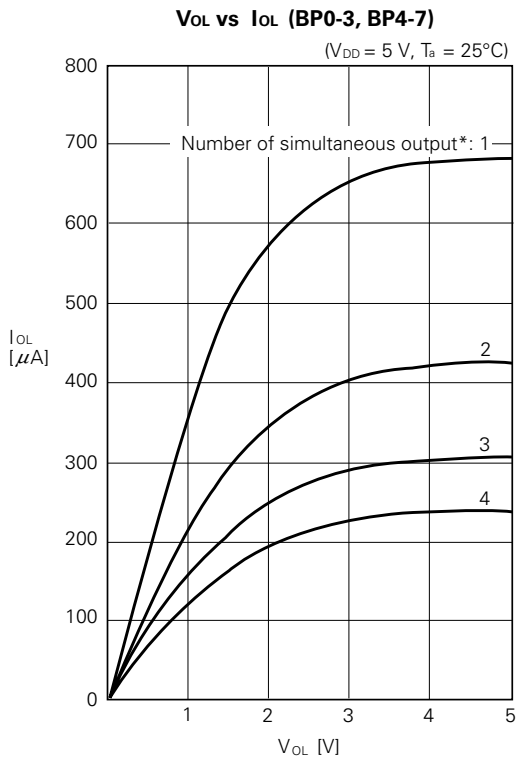
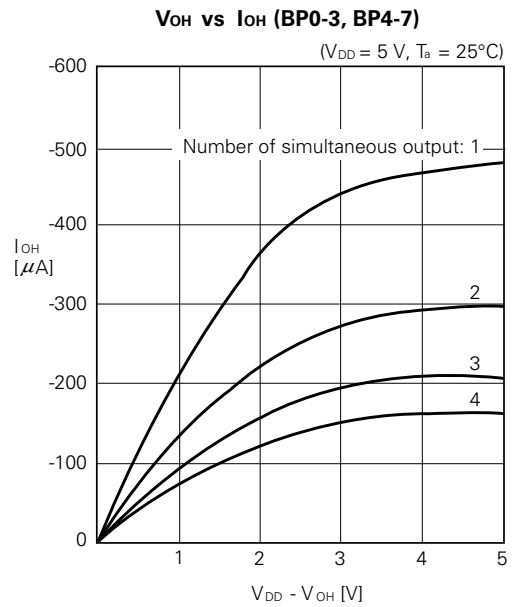
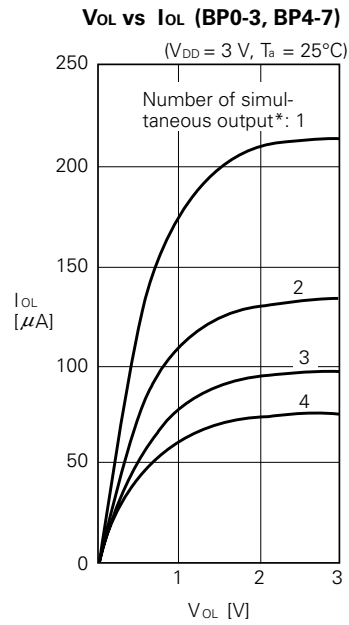
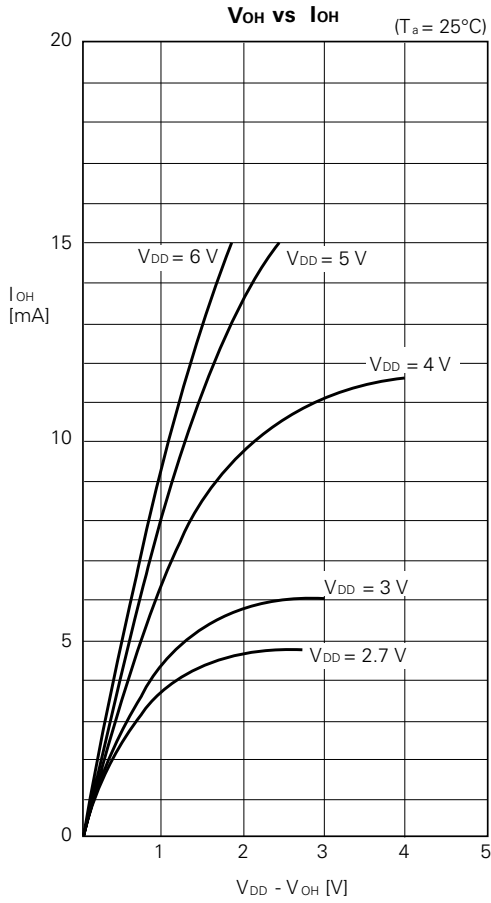


I_{DD} vs V_{DD} (Ceramic oscillation:1 MHz)

($T_a = 25^\circ\text{C}$)



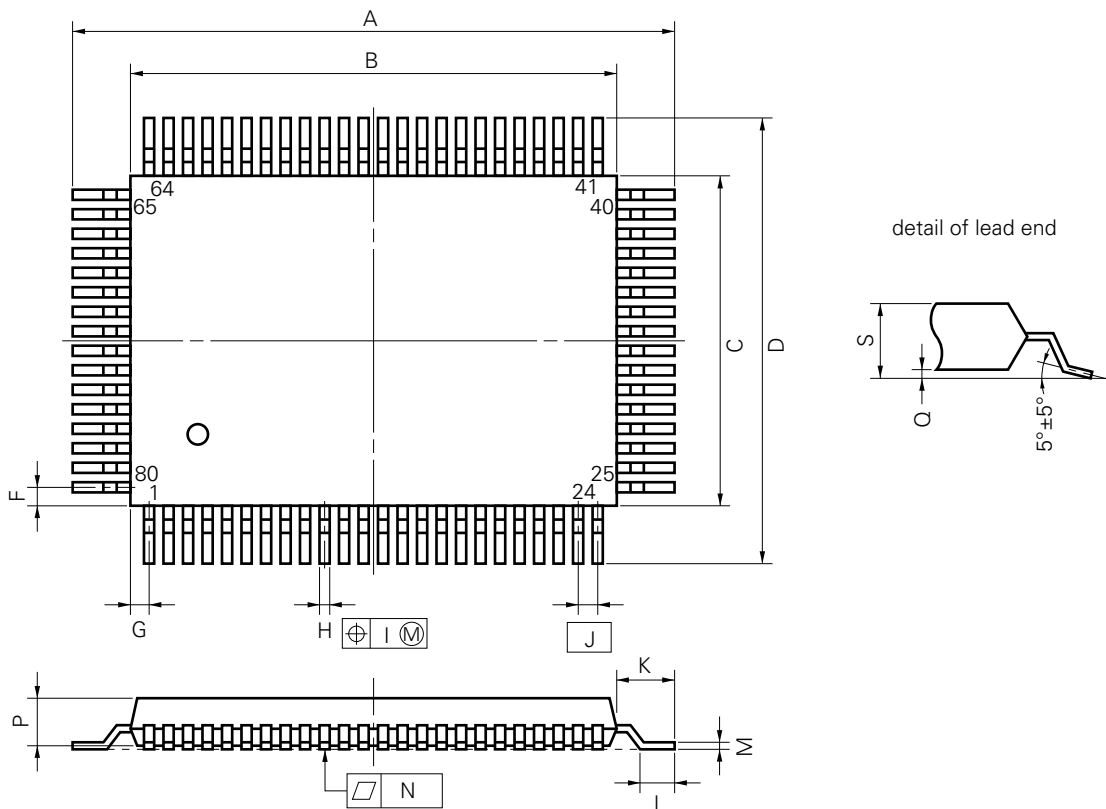




*: Of pins BP0-BP3 and BP4-BP7, for each, the number of pins simultaneously outputting the same level.

13. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)

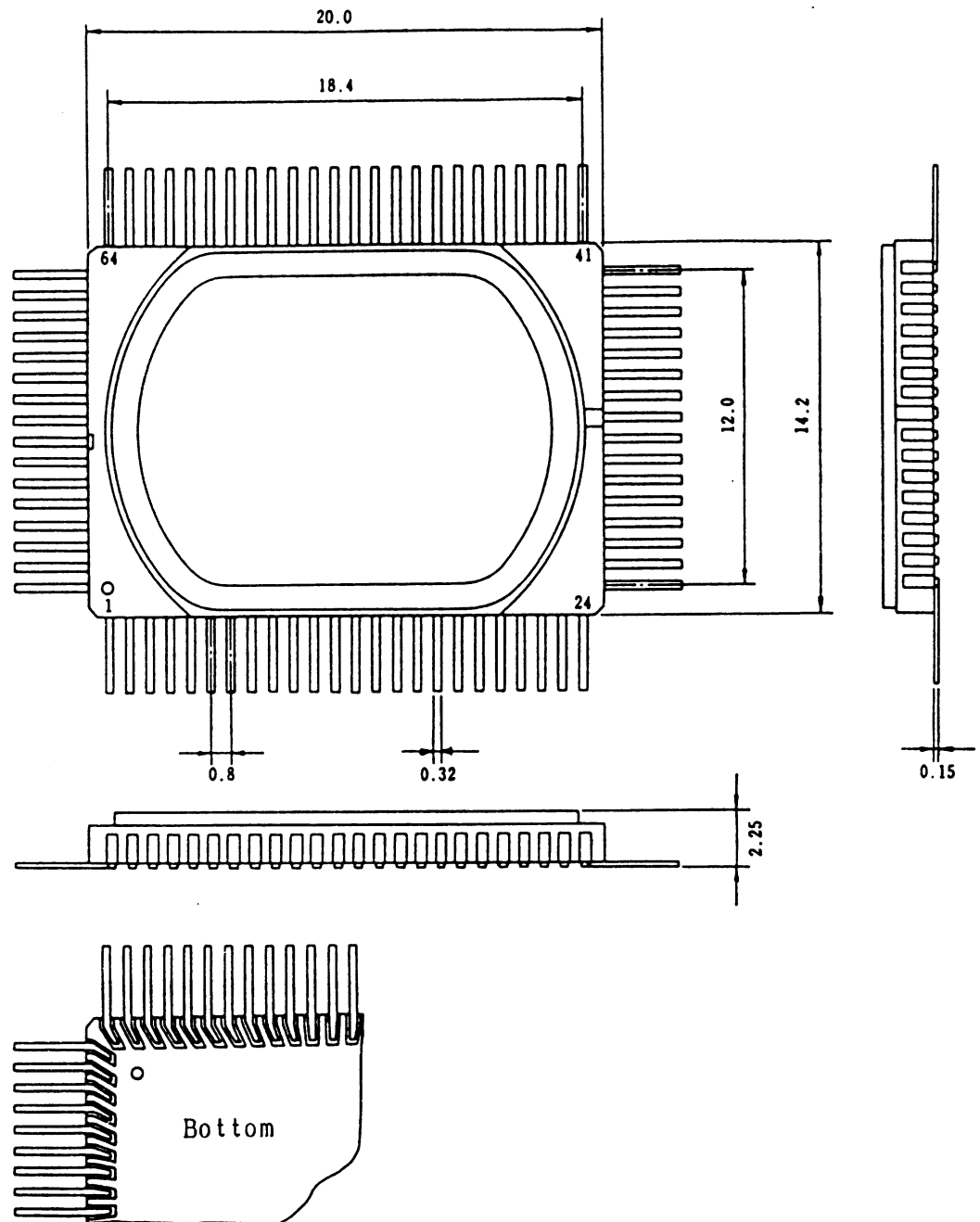


P80GF-80-3B9-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Phase-out/Discontinued**80-PIN CERAMIC QFP FOR ES (REFERENCE) (UNITS IN mm)****Warnings:**

1. The metal cap; connected with pin 33, changes to level V_{SS} .
2. The leads on the bottom surface are formed obliquely.
3. The length of the leads is not specified as the cutting of the lead tips is not controlled during the manufacturing process.

★ **14. RECOMMENDED SOLDERING CONDITIONS**

It is recommended that μPD75316 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

The soldering methods and conditions are not listed here, consult NEC.

Table 14-1 Soldering Conditions

μPD75312GF - xxx - 3B9: 80-pin plastic QFP (14×20 mm)

μPD75316GF - xxx - 3B9: 80-pin plastic QFP (14×20 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1	IR30-00-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1	VP15-00-1
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available. For details, consult NEC.

APPENDIX A. COMPARISON OF FEATURES AMONG THIS SERIES PRODUCTS

Product Name		μPD75304/75306/75308	μPD75312/75316	μPD75P308	μPD75P316
Item					
Supply Voltage Range		2.7 to 6.0 V		5 V±5%	
ROM Configuration		Mask ROM		EPROM/ one-time PROM	One-time PROM
Program Memory (byte)		4096/6016/8064	12160/16256	8064	16256
Data Memory (×4 bits)		512			
Instruction Cycle		0.95 μs, 1.91 μs, 15.3 μs (Main system clock: operating at 4.19 MHz) 122 μs (Subsystem clock: operating at 32.768 kHz)			
I/O Port	CMOS Input	40	8	Internal pull-up resistor possible through software: 23	
	CMOS I/O		16		
	CMOS Output		8	Also used as segment pins	
	N-ch Open-Drain I/O		8	10 V withstand, Internal pull-up resistor possible by mask option	10 V withstand, Internal pull-up resistor possible by mask option (However, w/o pull-up resistor)
LCD Controller/Driver		<ul style="list-style-type: none"> Common output: Static to 1/4 duty are selected. Segment output: Can be output up to 32. 			
		With dividing resistor for LCD drive by mask option		Without dividing resistor for LCD drive option	
LCD Drive Voltage		2.5 to V _{DD}			
Timer/Counter		<ul style="list-style-type: none"> 8-bit timer/event counter 8-bit basic interval timer Watch timer 			
Serial Interface		<ul style="list-style-type: none"> NEC standard serial bus interface (SBI) Clock serial interface 			
Vector Interrupt		External: 3, Internal: 3			
Test Input		External: 1, Internal: 1			
Clock Output (PCL)		Φ, 524 kHz, 262 kHz, 65.5 kHz (Main system clock: operating at 4.19 MHz)			
Buzzer Output (BUZ)		2 kHz (Main system clock: operating at 4.19 MHz, or subsystem clock: operating at 32.768 kHz)			
Package		80-pin plastic QFP (14×20 mm)		<ul style="list-style-type: none"> 80-pin plastic QFP (14×20 mm) 80-pin ceramic WQFN (w/LCC) 	80-pin plastic QFP (14×20 mm)
PROM Model		μPD75P308	μPD75P316 μPD75P316A	—	—

Product Name		μPD75304B/75306B/75308B	μPD75312B	μPD75316B	μPD75P316B*	μPD75P316A
Item						
Supply Voltage Range		2.0 to 6.0 V				
ROM Configuration		Mask ROM			One-time PROM	EPROM/ one-time PROM
Program Memory (byte)		4096/6016/8064	12160	16256		
Data Memory (×4 bits)		512	1024			
Instruction Cycle		0.95 μs, 1.91 μs, 15.3 μs (Main system clock: operating at 4.19 MHz) 122 μs (Subsystem clock: operating at 32.768 kHz)				
I/O Port	CMOS Input	40	8	Internal pull-up resistor possible through software: 23		
	CMOS I/O		16			
	CMOS Output		8	Also used as segment pins		
	N-ch Open-Drain I/O		8	10 V withstand, Internal pull-up resistor possible by mask option	10 V withstand, Internal pull-up resistor possible by mask option (However, w/o pull-up resistor)	
LCD Controller/Driver		<ul style="list-style-type: none"> • Common output: Static to 1/4 duty are selected. • Segment output: Can be output up to 32. 				
		With dividing resistor for LCD drive by mask option			Without dividing resistor for LCD drive option	
LCD Drive Voltage		2.0 to V _{DD}				
Timer/Counter		<ul style="list-style-type: none"> • 8-bit timer/event counter • 8-bit basic interval timer • Watch timer 				
Serial Interface		<ul style="list-style-type: none"> • NEC standard serial bus interface (SBI) • Clock serial interface 				
Vector Interrupt		External: 3, Internal: 3				
Test Input		External: 1, Internal: 1				
Clock Output (PCL)		Φ, 524 kHz, 262 kHz, 65.5 kHz (Main system clock: operating at 4.19 MHz)				
Buzzer Output (BUZ)		2 kHz (Main system clock: operating at 4.19 MHz, or subsystem clock: operating at 32.768 kHz)				
Package		80-pin plastic QFP • (14×20 mm) • (□14 mm) 80-pin plastic TQFP (□12 mm)	80-pin plastic QFP (□14 mm) 80-pin plastic TQFP (□12 mm)		80-pin ceramic WQFN 80-pin plastic QFP • (14×20 mm)	
PROM Model		GF package : μPD75P316A GC/GK package: μPD75P316B	μPD75P316B		—	—

*: Under development

APPENDIX B. DEVELOPMENT TOOLS



The following development support tools are readily available to support development of systems using μPD75312 and 75316:

PROM writing tools

Hardware	IE-75000-R * ¹ IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM * ²	Emulation board for IE-75000-R and IE-75001-R
	EP-75308GF-R EV-9200G-80	Emulation prove for μPD75312GF and 75316GF, provided with 80-pin conversion socket EV-9200G-80.
	PG-1500	PROM programmer
	PA-75P308GF	PROM programmer adapter solely used for μPD75P316GF and 75P316AGF. It is connected to PG-1500.
Software	IE Control Program	Host machine <ul style="list-style-type: none"> • PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A*³) • IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

*1: Maintenance product

2: Not provided with IE-75001-R.

3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this function.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

★ **APPENDIX C. RELATED DOCUMENTS**

GENERAL NOTES ON CMOS DEVICES**① STATIC ELECTRICITY (ALL MOS DEVICES)**

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to "Processing of Unused Pins" in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

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