To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD75218

4-BIT SINGLE-CHIP MICROCOMPUTER

The μPD75218 is a microcomputer with a CPU capable of 1-, 4-, and 8-bit-wise data processing, ROM, RAM, I/O ports, an FIP controller/driver, a watch timer, a timer/pulse generator capable of outputting 14-bit PWM pulses, a serial interface and a vectored interrupt function integrated on a single chip.

It is most suitable for applications which use fluorescent display tubes as display devices and require the timer/watch function and high-speed interrupt servicing, such as VCR, CD and ECR. It can help to provide the unit with many functions and to decrease performance costs.

The μPD75218 has larger ROM and RAM capacity than its predecessor, μPD75217. So several codes required before have been reduced to only one code in the μPD75218 specifications.

The one-time PROM product, μPD75P218 and various development tools (IE-75001-R, assembler, etc.) are available for system development evaluation or small production.

The following manual provides detailed description of the functions of the μPD75218. Be sure to read this manual when you design an application system.

μPD75218 User's Manual: IEU-692

FEATURES

- On-chip large-capacity ROM and RAM
  - Program memory (ROM): 32K × 8 bits
  - Data memory (RAM) : 1K × 4 bits
- Architecture equal to that of an 8-bit microcomputer
- High-speed operation: Minimum instruction execution time : 0.67 μs (when the microcomputer operates at 6.0 MHz)
- Instruction execution time variable function realizing a wide range of operating voltages
- On-chip programmable fluorescent indication panel (FIP) controller/driver
- Timer function : 4 ch
  - 14-bit PWM output capability with the voltage synthesizer type electronic tuner
  - Buzzer output capability
- Interrupt function with importance attached to applications
  - For power-off detection
  - For reception of remote-controller signal
- Product with an on-chip PROM : μPD75P218 (on-chip EPROM : WQFN package)

The information in this document is subject to change without notice.

Document No. IC-3035
(O. D. No. IP-8484)
Date Published November 1993 P
Printed in Japan

Major changes in this version are indicated by stars (★) in the margins.

ORDERING INFORMATION

Part number	Package	Quality grade
μPD75218CW-×××	64-pin plastic shrink DIP (750 mil)	Standard
μPD75218GF-×××-3BE	64-pin plastic QFP (14 × 20 mm)	Standard

Remark ××× is a ROM code.

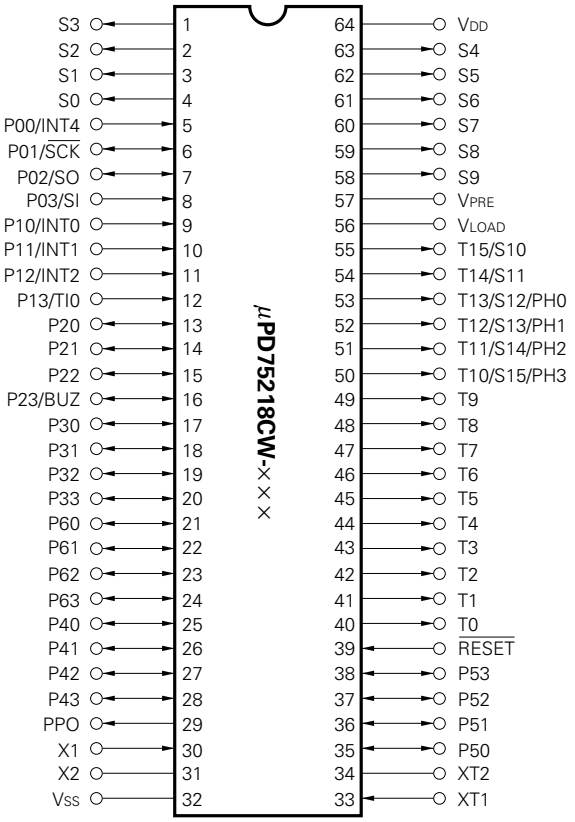
Please refer to "Quality Grades on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications

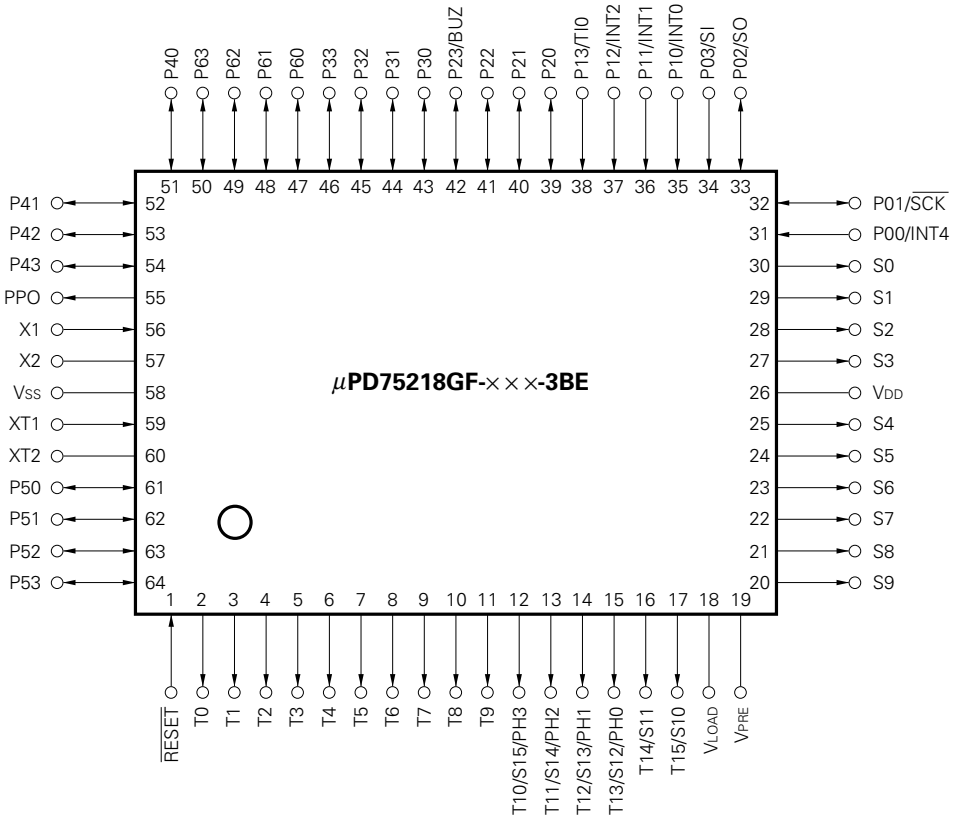
LIST OF FUNCTIONS

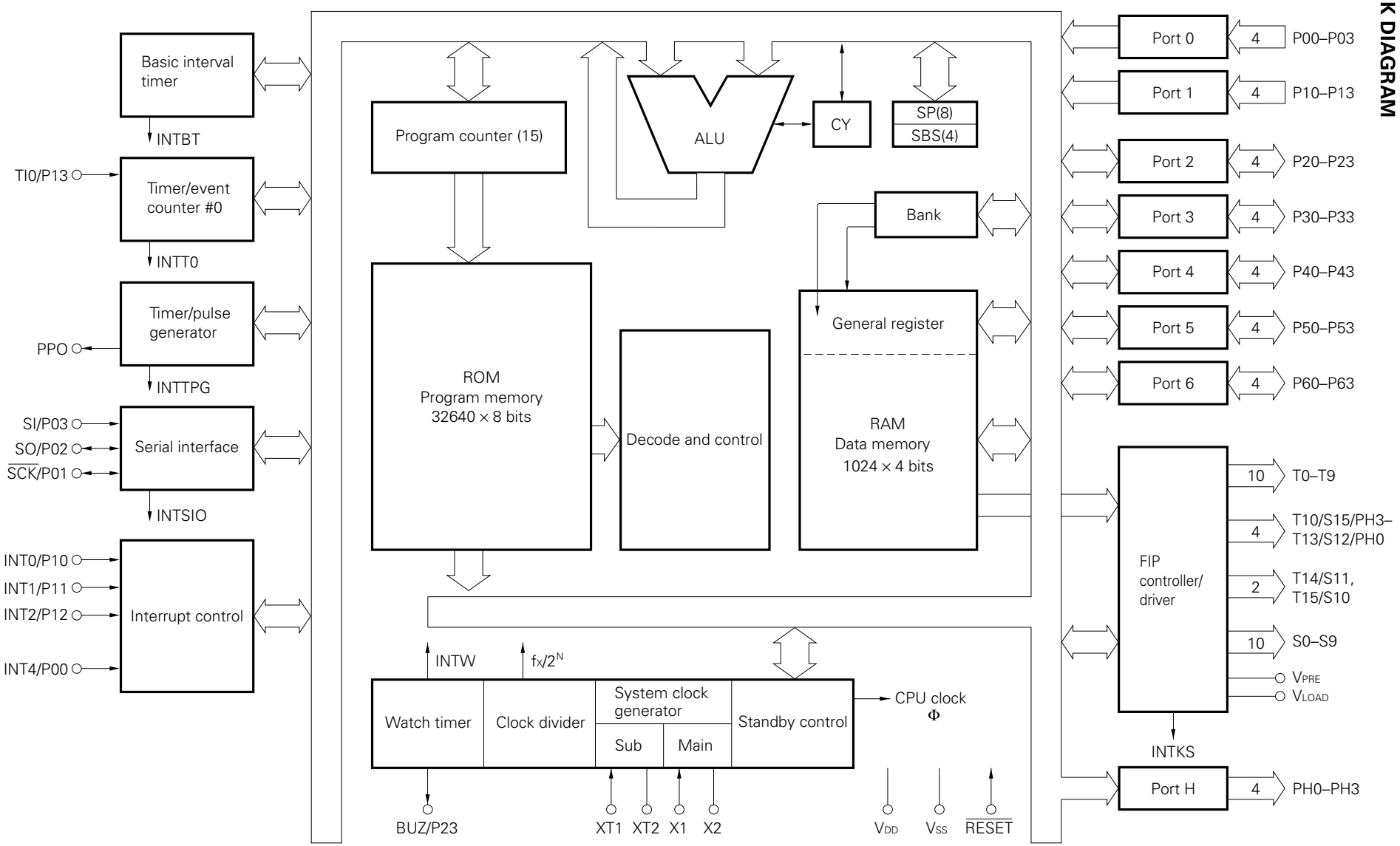
Item	Function
Built-in memory	ROM: 32640 × 8 bits, RAM: 1024 × 4 bits
I/O line (including FIP® dual-function pins and excluding FIP dedicated pins)	33 lines • CMOS input : 8 lines • CMOS I/O : 20 lines (LED drive: 8 lines) • CMOS output : 1 line (PWM/pulse output) • P-ch open-drain output with high withstand voltage and high current: 4 lines (LED drive)
Instruction cycle	• 0.67 μs, 1.33 μs, 10.7 μs (with main system clock operating at 6.0 MHz) • 0.95 μs, 1.91 μs, 15.3 μs (with main system clock operating at 4.19 MHz) • 122 μs (with subsystem clock operating at 32.768 kHz)
FIP controller/driver	• Number of segments: 9 to 16 segments • Number of digits : 9 to 16 digits • Dimmer function : 8 levels • Mask option for pull-down resistors • Key scan interrupt generation
Timer	4 channels • Timer/pulse generator : 14-bit PWM output enabled • Watch timer : Buzzer output enabled • Timer/event counter • Basic interval timer : Watchdog timer application capability
Serial interface	• MSB start/LSB start switchable • Serial bus configuration capability
Vectored interrupt	External : 3, Internal : 5
Test input	External : 1, Internal : 1
System clock oscillator	• Ceramic/crystal oscillator for main system clock oscillation: 6.0 MHz standard • Ceramic/crystal oscillator for main system clock oscillation: 4.19 MHz standard • Crystal oscillator for subsystem clock oscillation : 32.768 kHz standard
Mask option	• High withstand-voltage port (pull-down resistor) • Port 6 (pull-down resistor)
Operating temperature range	–40 to +85 °C
Operating supply voltage	2.7 to 6.0 V (standby data hold : 2.0 to 6.0 V)
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)







3. PIN FUNCTIONS

3.1 PORT PINS

Pin	I/O	Dual-function pin	Function	8-bit I/O	After reset	Input / output circuit type[Note]
P00	Input	INT4	4-bit input port (PORT0)	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ
P02	Input/output	SO				Ⓖ
P03	Input	SI				Ⓑ
P10	Input	INT0	Noise elimination function available		Input	Ⓑ
P11		INT1	Noise elimination function available			
P12		INT2	4-bit input port (PORT1)			
P13		TI0				
P20	Input/output	——	4-bit input/output port (PORT2)	×	Input	E
P21		——				
P22		——				
P23		BUZ				
P30 to P33	Input/output	——	Programmable 4-bit input/ output port (PORT3). Input/output specifiable in 1-bit units.		Input	E
P40 to P43	Input/output	——	4-bit input/output port (PORT4). LED direct drive capability.	○	Input	E
P50 to P53	Input/output	——	4-bit input/output port (PORT5). LED direct drive capability.		Input	E
P60 to P63	Input/output	——	Programmable 4-bit input/output port (PORT6). Input/output specifiable in 1-bit units. On-chip pull-down resistor available (mask option). Suitable for key input.	×	Input	V
PH0	Output	T13/S12	4-bit P-ch open-drain output port with high withstand voltage and high current (PORTH). LED direct drive capability. On-chip pull-down resistor available (mask option).	×	Low level (with an on-chip pull-down resistor) or high impedance.	I
PH1		T12/S13				
PH2		T11/S14				
PH3		T10/S15				

Note The circuit-type codes enclosed in circles indicate that the corresponding circuits have a Schmitt-triggered input.

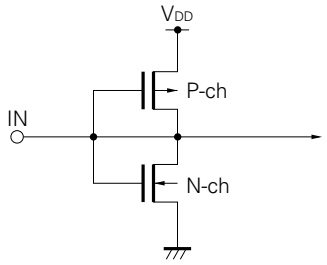
3.2 NON-PORT PINS

Pin	I/O	Dual-function pin	Function		After reset	Input / output circuit type[Note]
T0 to T9	Output	—	FIP controller/driver output pins. Pull-down resistor can be incorporated in bit units (mask option).	Output pins with high withstand voltage and high current for digit output	Low level (with an on-chip pull-down resistor) or high impedance (without a pull-down resistor)	I
T10/S15 to T13/S12		PH3 to PH0		Output pins with high withstand voltage and high current also used for digit/segment output. Extra pins can be used as PORTH.		
T14/S11, T15/S10		—		Output pins with high withstand voltage and high current also used for digit/segment output. Static output also possible.		
S9				High withstand-voltage output for segment output. Static output also possible.		
S0 to S8				High withstand-voltage output for segment output		
PPO	Output	—	Timer/pulse generator pulse output		High impedance	D
TI0	Input	P13	External event pulse input for timer/event counter		—	Ⓑ
$\overline{SCK}$	Input/output	P01	Serial clock input/output		Input	Ⓕ
SO	Input/output	P02	Serial data output or serial data input/output		Input	Ⓖ
SI	Input	P03	Serial data input or normal input		Input	Ⓑ
INT4	Input	P00	Edge-detected vectored interrupt input (rising and falling edge detection).		—	Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input with noise elimination function (detection edge selection possible).		—	Ⓑ
INT1		P11				
INT2	Input	P12	Edge-detected testable input (rising edge detection).		—	Ⓑ
BUZ	Input/output	P23	Fixed frequency output (for buzzer or system clock trimming).		Input	E
X1	Input	—	Crystal/ceramic connection pin for main system clock oscillation. External clock input to X1 and its inverted clock input to X2.		—	—
X2	—					
XT1	Input	—	Crystal connection pin for subsystem clock oscillation. External clock input to XT1. Leave XT2 open.		—	—
XT2	—					
$\overline{RESET}$	Input	—	System reset input (low level active).		—	Ⓑ
★ V_{PRE}	—	—	FIP controller/driver output buffer power supply.		—	I
V_{LOAD}	—	—	FIP controller/driver pull-down resistor connection pin.		—	I
V_{DD}	—	—	Positive power supply.		—	—
V_{SS}	—	—	GND potential.		—	—

Note The circuit-type codes enclosed in circles indicate that the corresponding circuits have a Schmitt-triggered input.

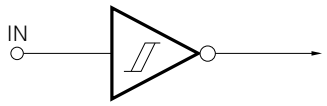
3.3 PIN INPUT/OUTPUT CIRCUIT LIST

Type A



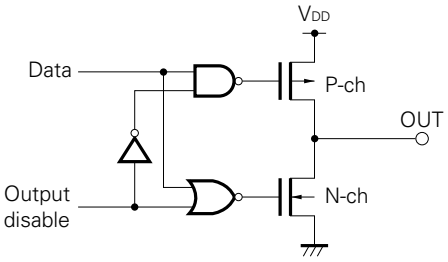
CMOS-specified input buffer

Type B



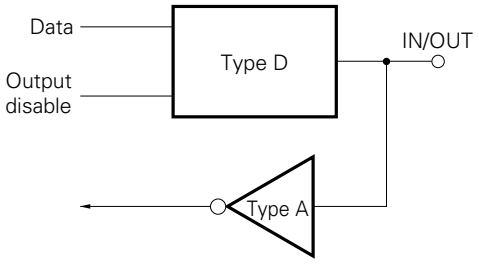
Schmitt trigger input having hysteresis characteristics

Type D



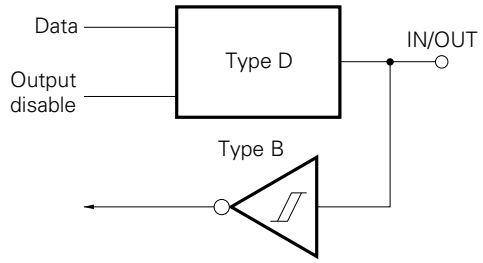
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type E



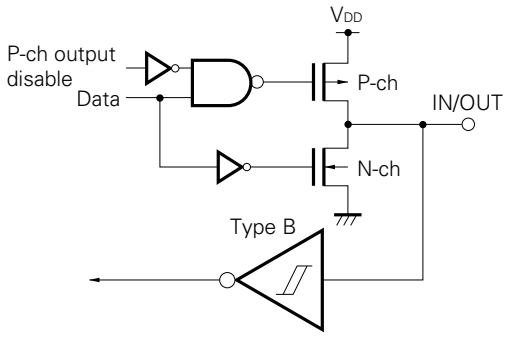
Input/output circuit consisting of type D push-pull output and type A input buffer

Type F



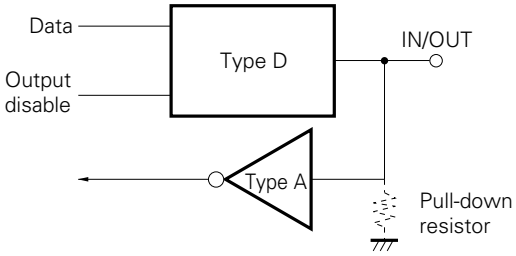
Input/output circuit consisting of type D push-pull output and type B schmitt trigger input

Type G



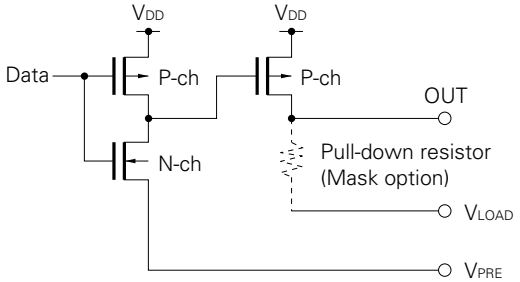
Input/output circuit capable of switching between push-pull output and N-ch open-drain output (with P-ch off).

Type V



(Mask option)

Type I



3.4 HANDLING UNUSED PINS

Pin	Recommended connection
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO	
P03/SI	
P10/INT0 to P12/INT2	Connect to V_{SS}
P13/TI0	
P20 to P22	Input state : Connect to V_{SS} or V_{DD} Output state : Leave open
P23/BUZ	
P30 to P33	
P40 to P43	
P50 to P53	
P60 to P63	
PPO	Leave open
S0 to S9	
T15/S10 to T14/S11	
T0 to T9	
T10/S15/PH3 to T13/S12/PH0	
XT1	Connect to V_{SS} or V_{DD}
XT2	Leave open
V_{LOAD} when there is no on-chip load resistor	Connect to V_{SS} or V_{DD}

3.5 NOTES ON USE OF THE P00/INT4 PIN AND $\overline{\text{RESET}}$ PIN

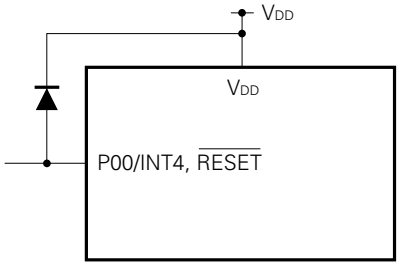
P00/INT4 and $\overline{\text{RESET}}$ pins have the function (especially for IC test) to test μPD75218 internal operations in addition to the functions described in **sections 3.1** and **3.2**.

The test mode is set when a voltage larger than V_{DD} is applied to one of these pins. If noise larger than V_{DD} is applied in normal operation, the test mode may be set thereby adversely affecting normal operation.

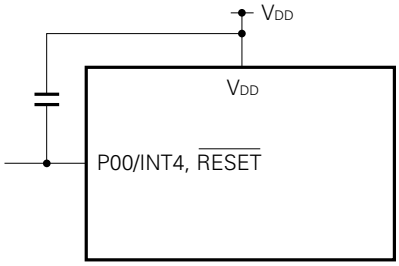
Since there is a display output pin having a high-voltage amplitude (35 V) next to the P00/INT4 and $\overline{\text{RESET}}$ pins, if cables for the related signals are routed in parallel, wiring noise larger than V_{DD} may be applied to the P00/INT4 and $\overline{\text{RESET}}$ pins causing errors.

Thus, carry out wiring so that wiring noise can be minimized, If noise still cannot be suppressed, take the measure against noise using the following external components.

- **Connecting a diode between the pins and V_{DD}**



- **Connecting a capacitor between the pins and V_{DD}**

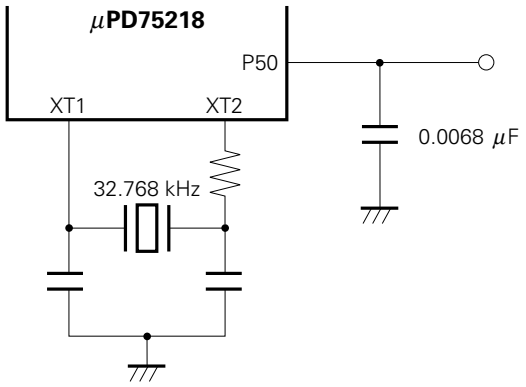


3.6 NOTES ON USE OF THE XT1, XT2 AND P50 PIN

When selecting the 32.768 kHz subsystem clock connected to the XT1 and XT2 pins as the watch timer source clock, the signal to be input or output to the P50 pin next to the XT2 pin must be a signal required to be switched between high and low the minimum number of times (once/second or less).

If the P50 pin signal is switched frequently between high and low, a spike is generated in the XT2 pin because of capacitance coupling of the P50 and XT2 pins and the correct watch functions cannot be achieved (the watch becomes fast).

If it is necessary to allow the P50 pin signal to switch between high and low, mount an external capacitor to the P50 pin as shown below.

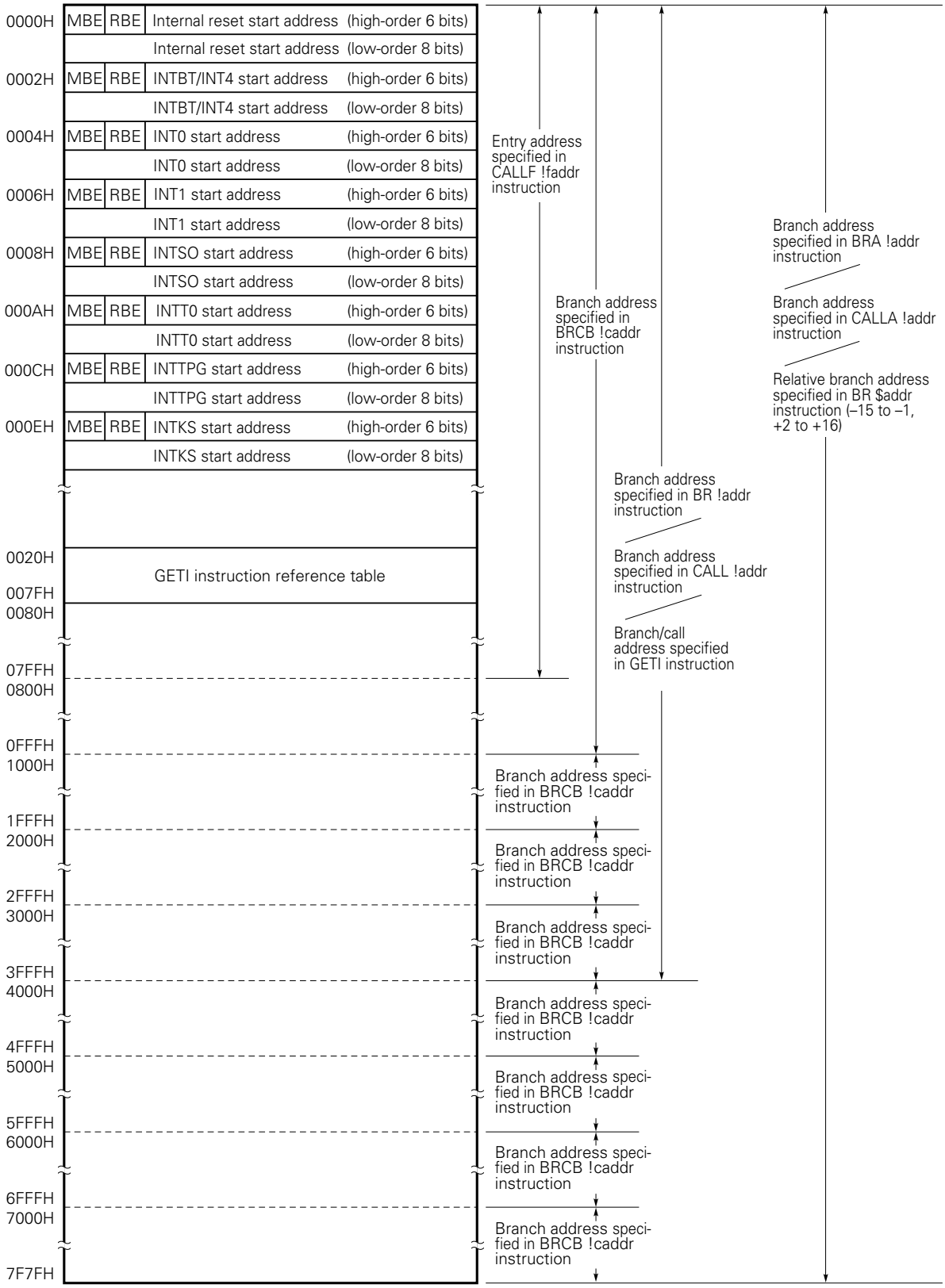


4. MEMORY CONFIGURATION

- Program memory (ROM): 32640 words × 8 bits
  - 0000H and 0001H: Vector table which contains the program start address after reset
  - 0002H to 000FH : Vector table which contains the program start addresses when interrupts occur
  - 0020H to 007FH : Table area referenced by a GETI instruction

- Data memory
  - Data area : 1024 words × 4 bits (000H to 3FFH)
  - Peripheral hardware area : 128 words × 4 bits (F80H to FFFH)

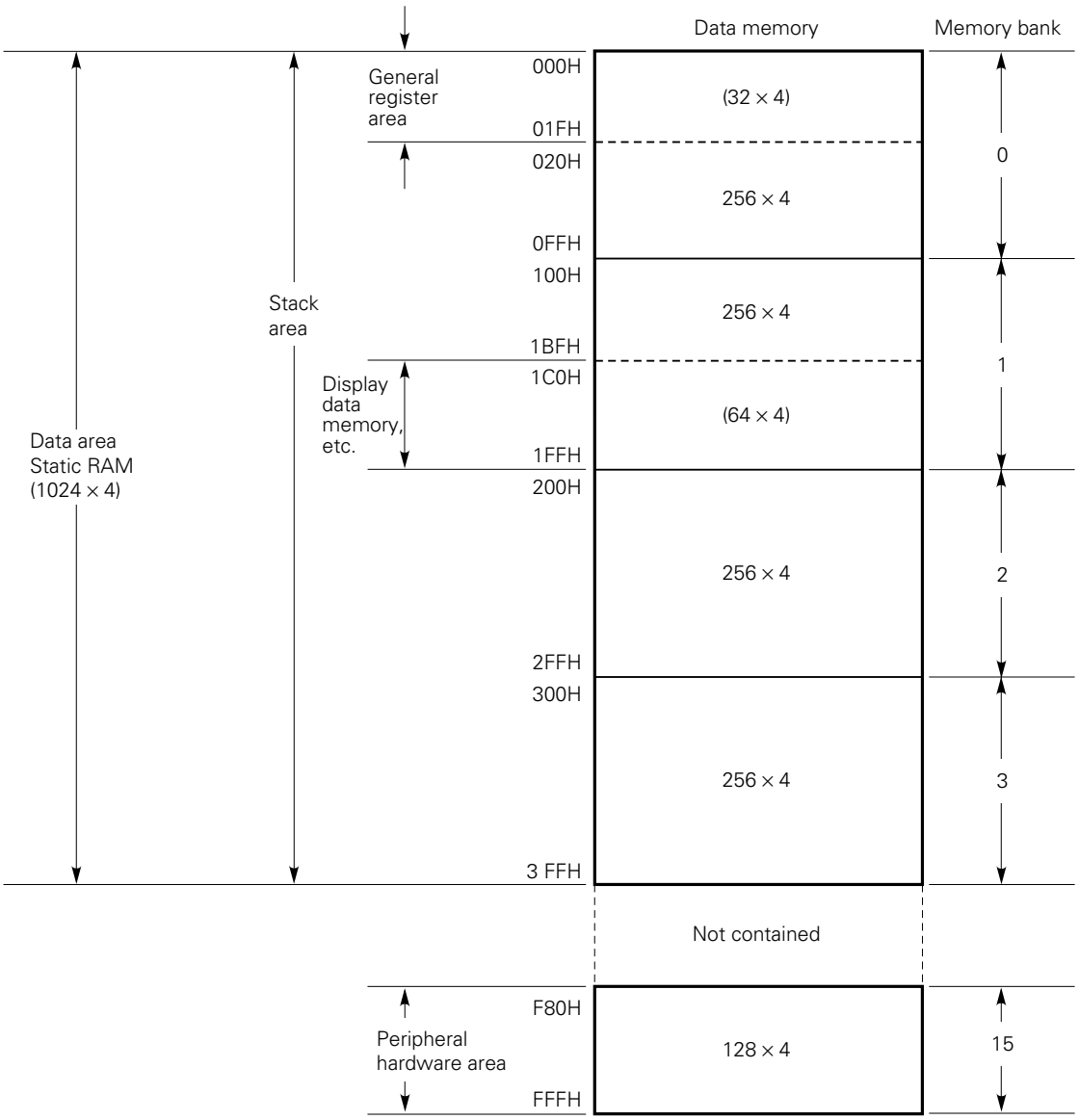
Fig. 4-1 Program Memory Map



Caution The start address of an interrupt vector shown above consists of 14 bits. So the start address must be set within a 16K-byte space (0000H to 3FFFH).

Remark In all cases other than those listed above, branch to the address with only the lower 8 bits of the PC changed is enabled by BR PCDE and BR PCXA instructions.

Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

The μPD75218 has the following three types of I/O port:

- 8 CMOS input pins (PORT0 and PORT1)
- 20 CMOS I/O pins (PORT2, PORT3, PORT4, PORT5, and PORT6)
- 4 P-ch open-drain output pins with high withstand voltage and high current (PORTH)

Total: 32 pins

Table 5-1 Functions of Ports

Port	Function	Operation and feature	Remarks
PORT0	4-bit input	Always read or test possible irrespective of the dual-function pin operating mode.	Shares the pins with SI, SO, $\overline{SCK}$ and INT4.
PORT1		Always read or test possible, P10 and P11 are inputs with the noise elimination function.	Shares the pins with INT0 to INT2 and TI0.
PORT2 PORT4 PORT5	4-bit input/output	Can be set to the input or output mode in 4-bit units. Ports 4 and 5 can input/output data in pairs in 8-bit units. Ports 4 and 5 can directly drive LEDs.	P23 shares the pin with BUZ.
PORT3 PORT6		Can be set bit-wise to the input or output mode. Port 6 can incorporate a pull-down resistor by mask option.	
PORTH	4-bit output	P-ch open-drain output port with high withstand voltage and high current. Can drive an FIP and LED directly. Can incorporate a pull-down resistor in bit units by mask option.	Shares the pins with T10/S15 to T13/S12.

5.2 CLOCK GENERATOR

Operation of the clock generator is specified by the processor clock control register (PCC) and system clock control register (SCC).

The main system clock or subsystem clock can be selected.

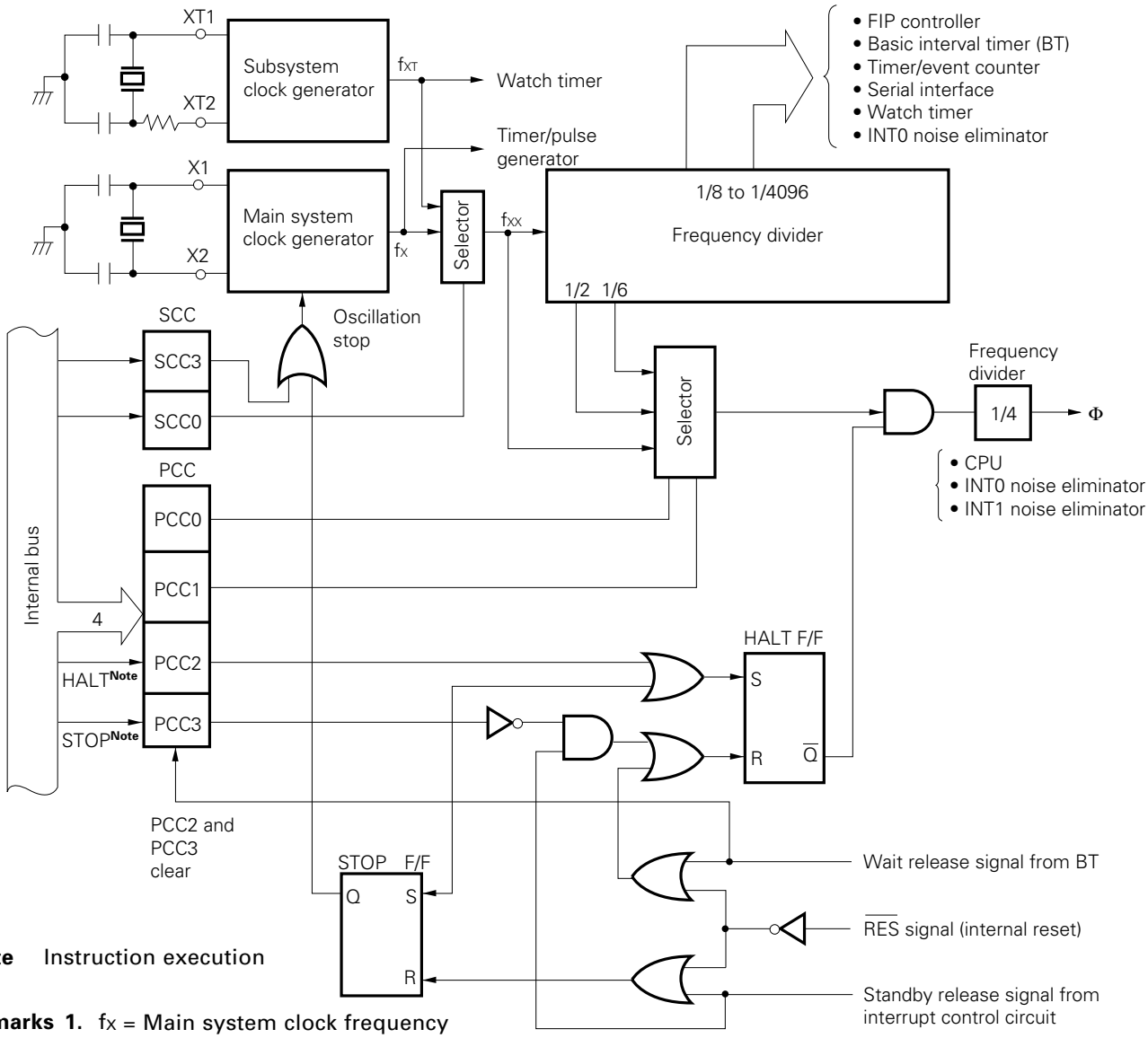
The instruction execution time is variable.

0.67 μs, 1.33 μs, 10.7 μs (main system clock: 6.0 MHz)

0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)

122 μs (subsystem clock: 32.768 kHz)

Fig. 5-1 Clock Generator Block Diagram



Note Instruction execution

Remarks 1. f_X = Main system clock frequency

2. f_{XT} = Subsystem clock frequency

3. f_{XX} = System clock frequency

4. Φ = CPU clock

5. PCC: Processor clock control register

6. SCC: System clock control register

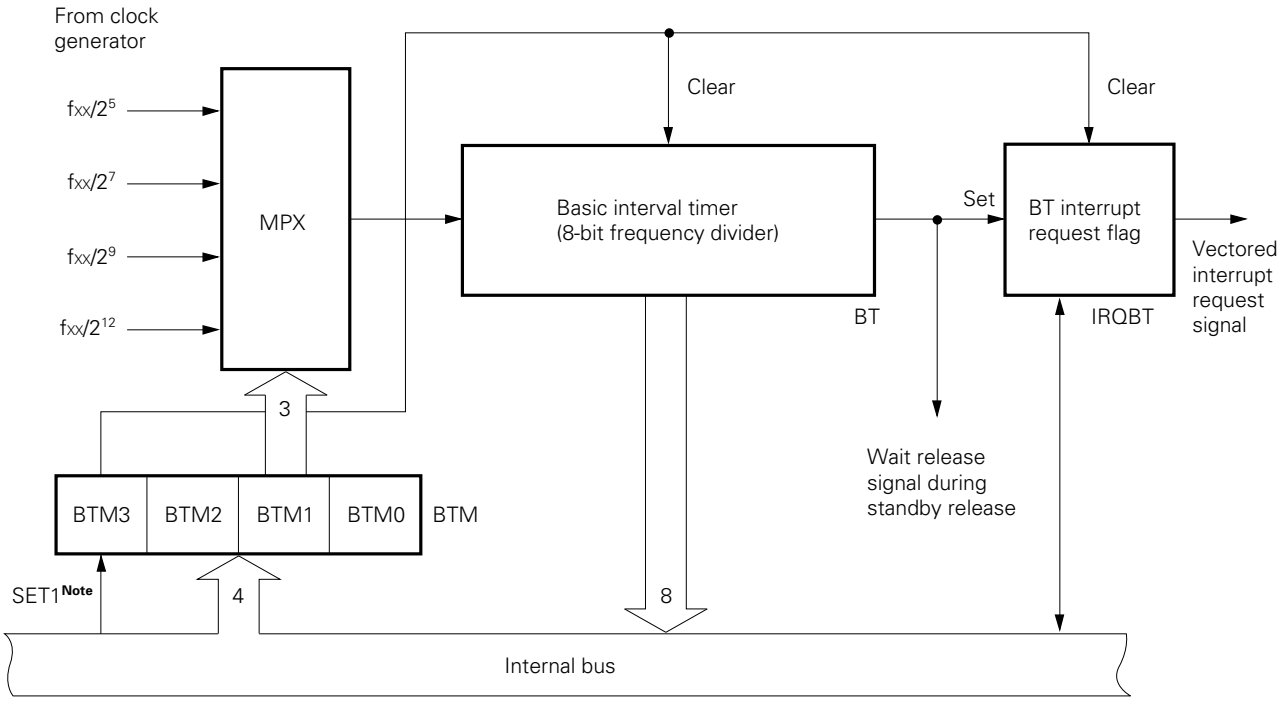
★ **7.** 1 clock cycle (t_{CY}) of Φ is 1 machine cycle of an instruction. For t_{CY}, see "AC Characteristics" in **Chapter 12**.

5.3 BASIC INTERVAL TIMER

The basic interval timer has the following functions:

- Interval timer operation to generate reference time
- Watchdog timer application to detect inadvertent program loop
- Wait time select and count upon standby mode release
- Count contents read

Fig. 5-2 Basic Interval Timer Configuration



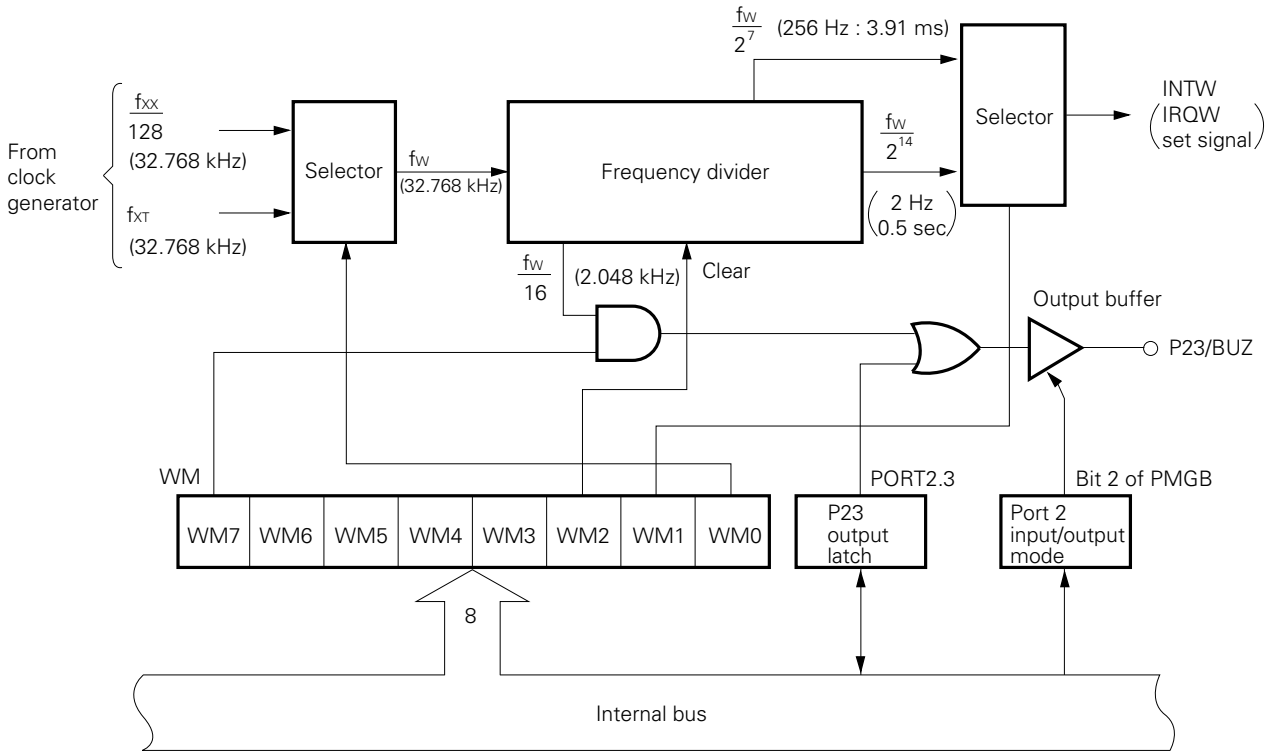
Note Instruction execution

5.4 WATCH TIMER

The μPD75218 incorporates one channel of watch timer. The watch timer has the following functions:

- Sets the test flag (IRQW) at 0.5 sec intervals.
  The standby mode can be released by IRQW.
- 0.5 second interval can be set with the main system clock and subsystem clock.
- The fast mode enables to set 128-time (3.91 ms) interval useful to program debugging and inspection.
- The fixed frequencies (2.048 kHz) can be output to the P23/BUZ pin for use to generate buzzer sound and trim the system clock oscillator frequency.
- Since the frequency divider can be cleared, the watch can be started from zero second.

Fig. 5-3 Watch Timer Block Diagram



Remark Values when fXX is 4.194304 MHz and fXT is 32.768 kHz are indicated in parentheses.

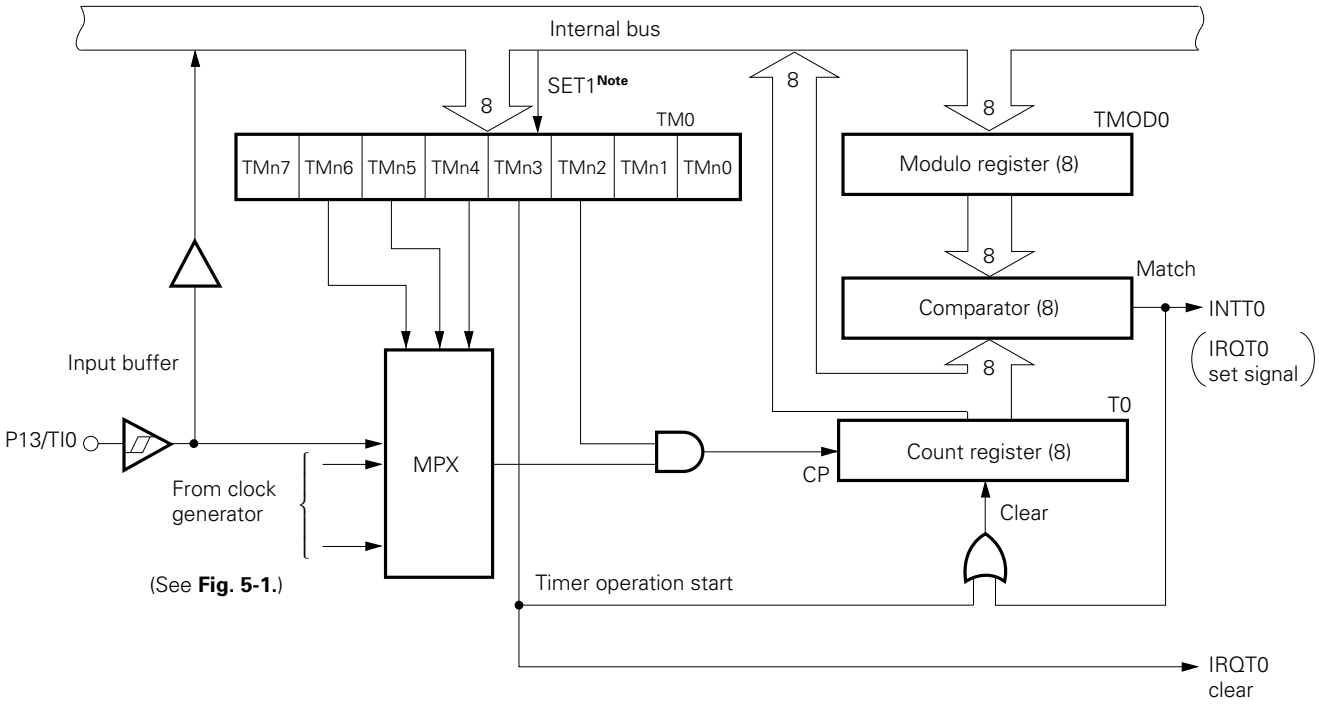
Caution When the main system clock operates at 6.0 MHz, a time interval of 0.5 second cannot be produced. Before producing this time interval, the main system clock must be changed to the subsystem clock.

5.5 TIMER/EVENT COUNTER

The μPD75218 incorporates one channel of timer/event counter. The timer/event counter has the following functions:

- Program interval timer operation
- Event counter operation
- Count state read function

Fig. 5-4 Timer/Event Counter Block Diagram



Note Instruction execution

5.6 TIMER/PULSE GENERATOR

The μPD75218 incorporates one channel of timer/pulse generator which can be used as a timer or a pulse generator. The timer/pulse generator has the following functions:

(a) Functions available in the timer mode

- 8-bit interval timer operation (IRQTPG generation) enabling the clock source to be varied at 5 levels
- Square wave output to PPO pin

(b) Functions available in the PWM pulse generation mode

- 14-bit accuracy PWM pulse output to the PPO pin (Used as a digital-to-analog converter and applicable to tuning)
- Fixed time interval ($\frac{2^{15}}{fx}$ = 5.46 ms when the microcomputer operates at 6.0 MHz)**Note** interrupt generation

If pulse output is not necessary, the PPO pin can be used as a 1-bit output port.

Note 7.81 ms when the microcomputer operates at 4.19 MHz

Caution If the STOP mode is set while the timer/pulse generator is in operation, erroneous operation may result. To prevent that from occurring, preset the timer/pulse generator to the stop state using its mode register.

Fig. 5-5 Block Diagram of Timer/Pulse Generator (Timer Mode)

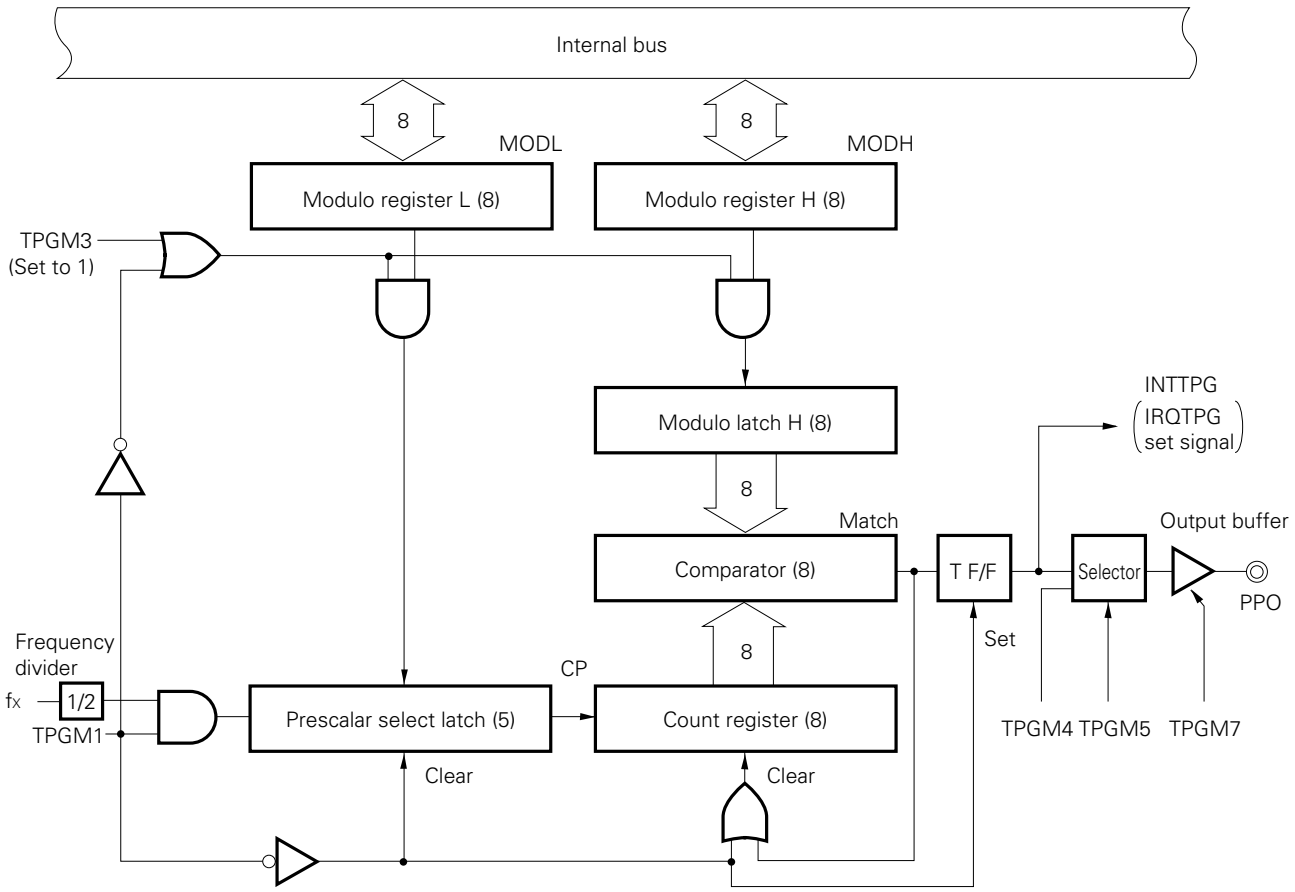
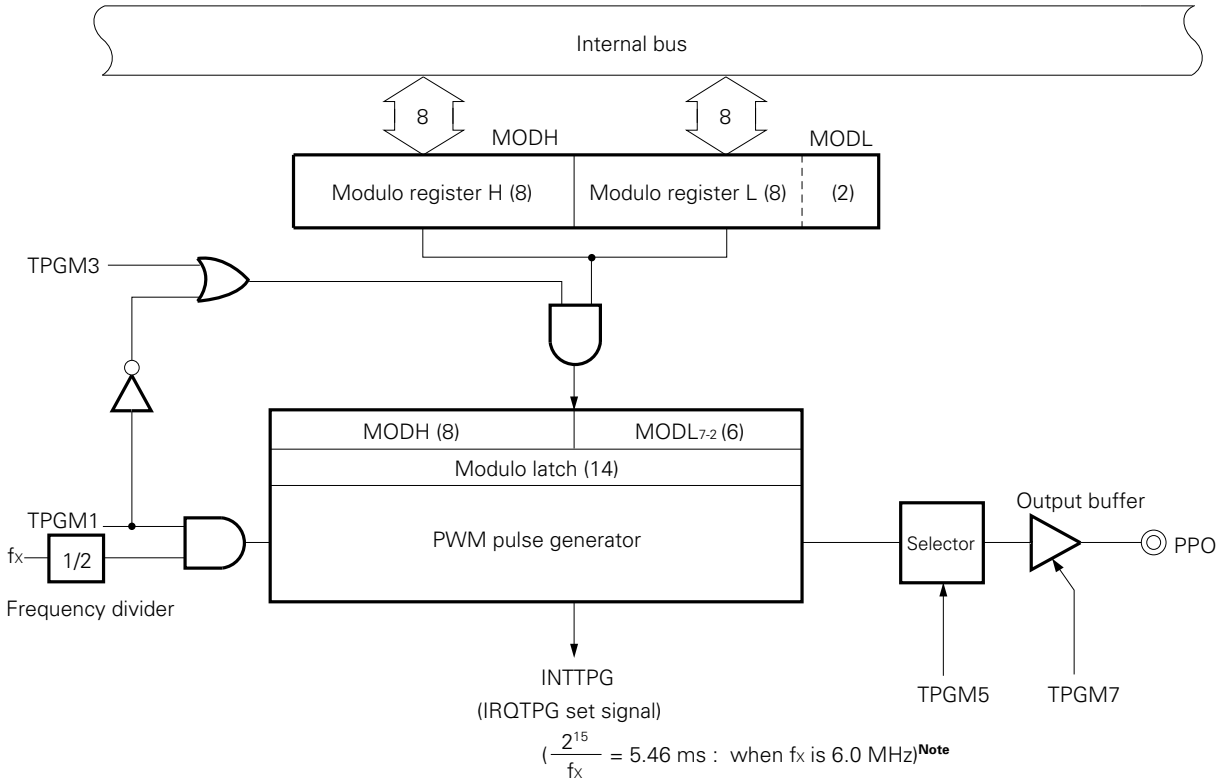


Fig. 5-6 Timer/Pulse Generator Block Diagram (PWM Pulse Generation Mode)



Note 7.81 ms when the microcomputer operates at 4.19 MHz.

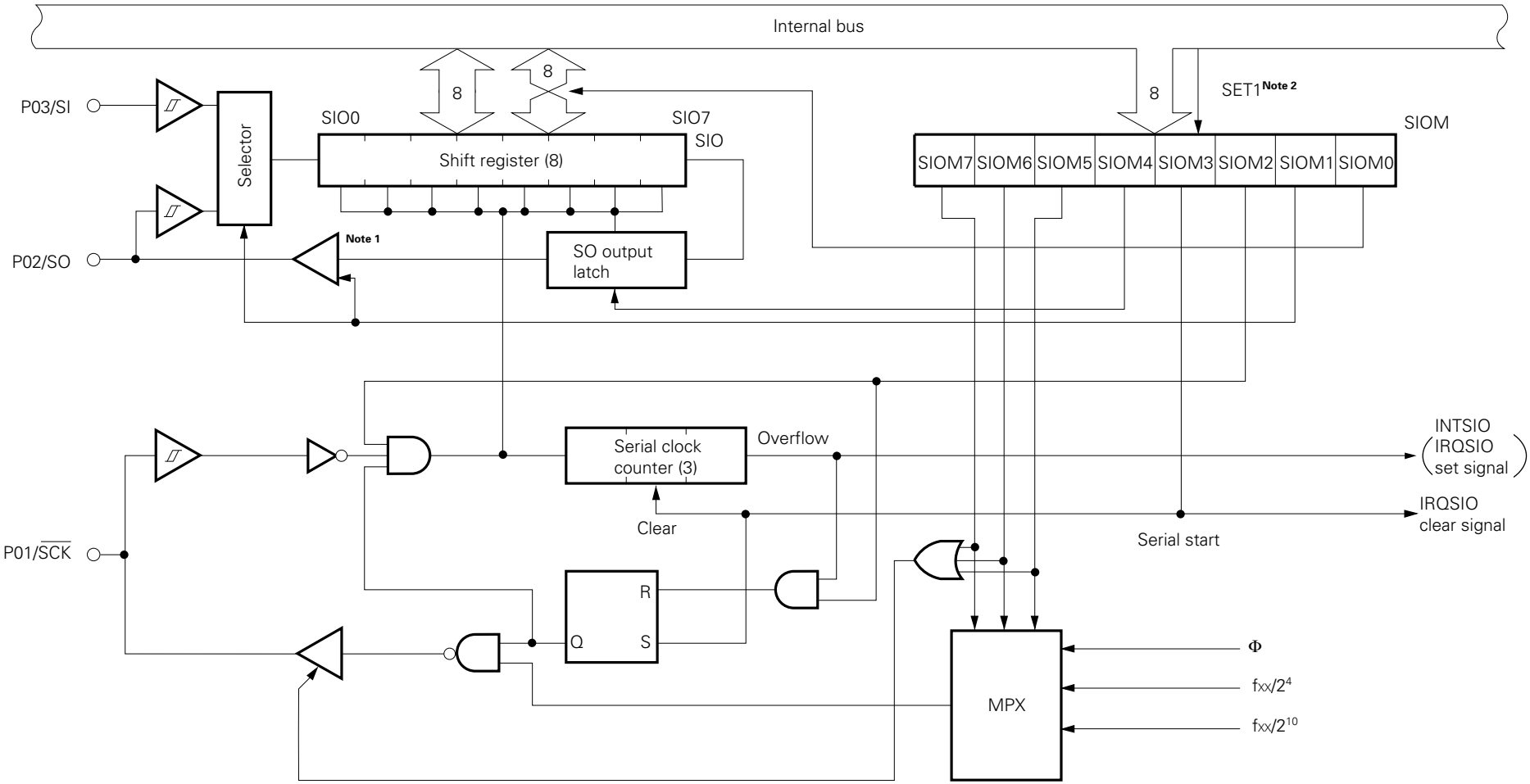
5.7 SERIAL INTERFACE

The serial interface has the following functions:

- Clock synchronous 8-bit send/receive operation (simultaneous send/receive)
- Clock synchronous 8-bit serial bus operation (data input/output from the SO pin. N-ch open-drain SO output)
- Start LSB/MSB switching

These functions facilitate data communication with another microcomputer of μPD7500 series or 78K series via a serial bus and coupling with peripheral devices.

Fig 5-7 Serial Interface Block Diagram



Notes 1. CMOS output and N-ch open-drain output switchable output buffer.

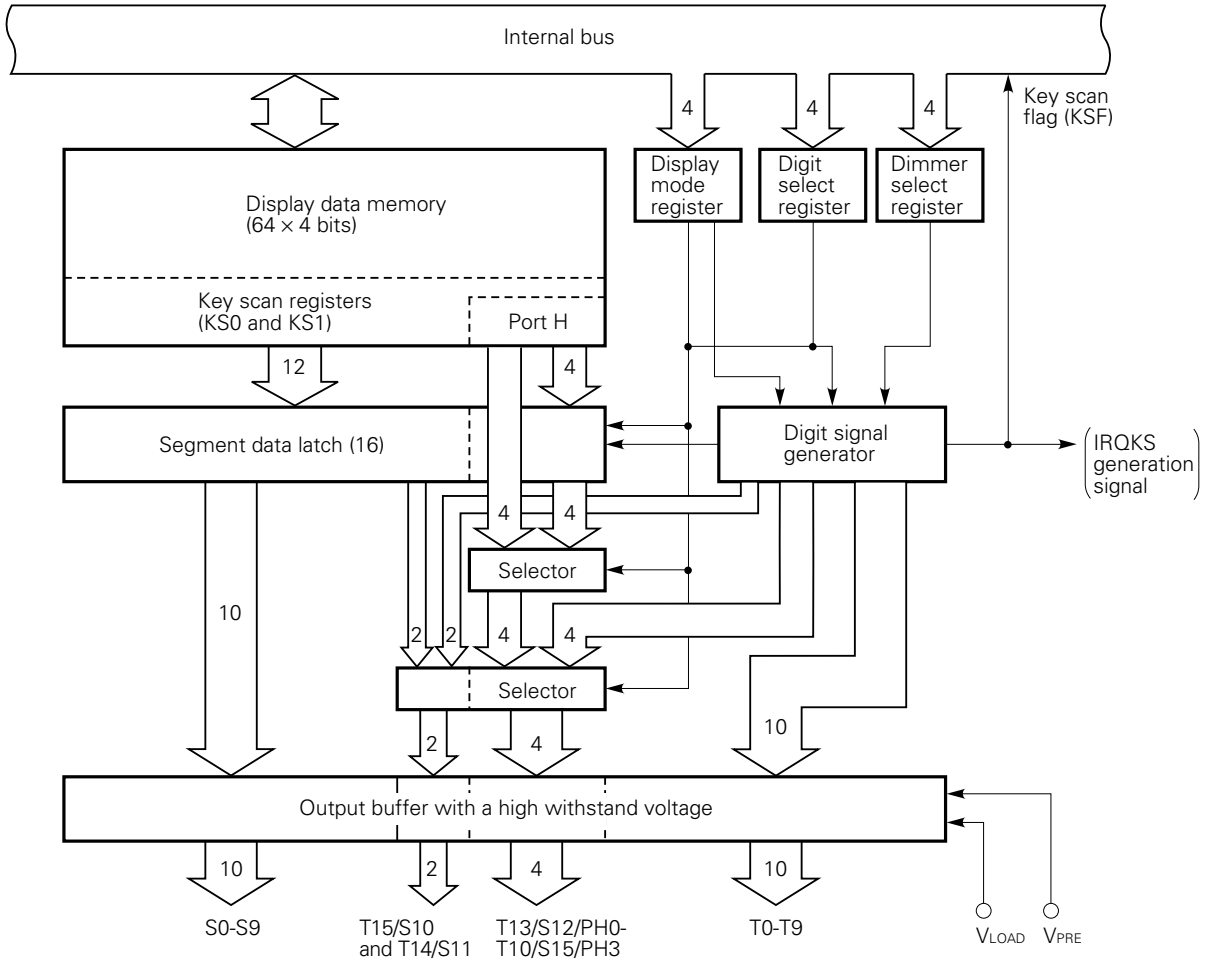
2. Instruction execution

5.8 FIP CONTROLLER/DRIVER

The FIP controller/driver in the μPD75218 has the same functions as that in its predecessor, μPD75216A:

- The FIP controller/driver outputs the segment signal by automatically reading display data (DMA operation) and automatically generates the digit signal.
- The FIP controller/driver can control the FIP of 9 to 16 segments and 9 to 16 digits with the display mode register (DSPM) and the digit select register (DIGS) (within the range of up to 26 display outputs).
- The display outputs unused for dynamic display can be used as static outputs.
- The dimmer function provides eight levels of intensity.
- Such hardware is contained that a key scan application is possible.
  - A key scan interrupt (IRQKS) is caused. (A key scan timing is detected.)
  - Key scan data can be output from key scan registers (KS0 and KS1) onto a segment output pin.
- A high-voltage output pin (40 V) is provided which can directly drive the FIP.
  - Pins dedicated to segments (S0 to S9): V_{OD} = 40 V, I_{OD} = 3 mA
  - Digit output pins (T0 to T15): V_{OD} = 40 V, I_{OD} = 15 mA
- A mask option enables a pull-down resistor to be incorporated for each bit.

Fig. 5-8 FIP Controller/Driver Block Diagram



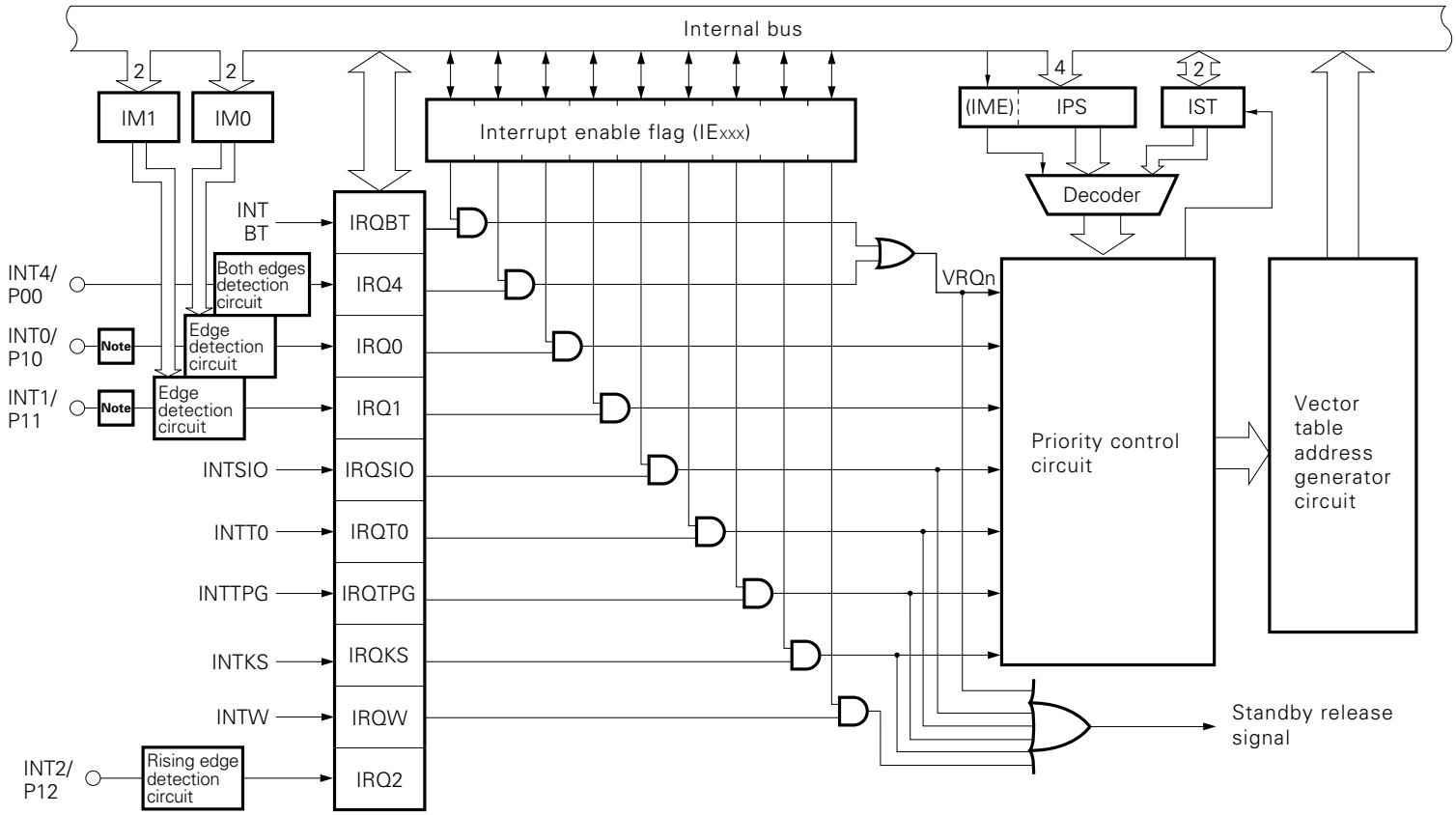
Caution The FIP controller/driver can only operate at the high and intermediate speeds (PCC = 0011B or 0010B) of the main system clock (SCC.0 = 0). It may cause errors with any other clock or in the standby mode. Thus, be sure to stop FIP controller operation (DSPM.3 = 0) and then shift the unit to any other clock mode or the standby mode.

6. INTERRUPT FUNCTIONS

The μPD75218 has eight types of interrupt sources and can generate multiple interrupts with priority order. It is also equipped with two types of test sources. INT2 is an edge detected testable input.
The μPD75218 interrupt control circuit has the following functions:

- Hardware-controlled vectored interrupt function which can control interrupt acknowledge with the interrupt enable flag (IE×××) and the interrupt master enable flag (IME).
- Function of setting any interrupt start address.
- Multiple interrupt function which can specify priority order with the interrupt priority select register (IPS).
- Interrupt request flag (IRQ×××) test function. (Interrupt generation can be checked by software.)
- Standby mode release function (Interrupts to be released can be selected by interrupt enable flags.)

Fig. 6-1 Interrupt Control Circuit Block Diagram



Note Noise eliminator

7. STANDBY FUNCTIONS

Two standby modes (STOP mode and HALT mode) are available for the μPD75218 to decrease power consumption in the program standby mode.

Table 7-1 Operation Status in Standby Mode

		STOP mode	HALT mode
Set instruction		STOP instruction	HALT instruction
System clock when set		Setting enabled only for main system clock	Setting enabled for either main system clock or subsystem clock
Operating State	Clock oscillator	Oscillator stops only for main system clock	Stops only for CPU clock Φ (oscillation continued)
	Basic interval timer	Operation stopped	Operation continued (IRQBT set at reference time intervals)
	Serial interface	Operation enabled only when external $\overline{SCK}$ input is selected for serial clock	Operation enabled when serial clock other than Φ is specified
	Timer/event counter	Operation enabled only when TI0 pin input is specified for count clock	Operation enabled
	Timer/pulse generator	Operation stopped	Operation enabled
	Watch timer	Operation enabled only f_{XT} is selected for count clock	Operation enabled
	FIP controller/driver	Operation disabled (display off mode set before disabling)	
	CPU	Operation stopped	
Release signal		Interrupt request signals (except INT0, INT1, and INT2) from operable hardware enabled by interrupt enable flags, or $\overline{RESET}$ input.	

8. RESET FUNCTIONS

The reset signal ($\overline{RES}$) generator has a configuration shown in Fig. 8-1.

Fig. 8-1 Reset Signal Generator

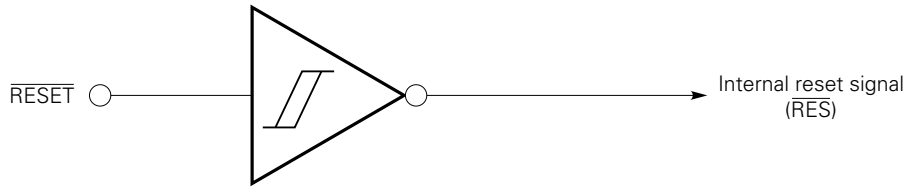
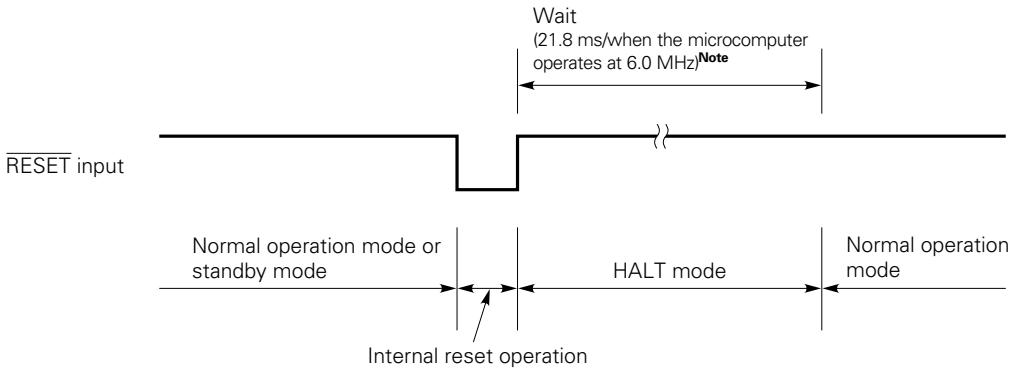


Fig. 8-2 shows the reset operation.

Fig. 8-2 Reset Operation by $\overline{RESET}$ Input



Note 31.3 ms when the microcomputer operates at 4.19 MHz

Table 8-1 lists the hardware statuses after reset operation.

Table 8-1 Hardware Statuses after Reset Operation

Hardware		$\overline{\text{RESET}}$ input in standby mode	$\overline{\text{RESET}}$ input during operation
Program counter (PC)		Set the low-order six bits at address 0000H in program memory to PC_{13-8}, set the contents of address 0001H to PC_{7-0}, and set PC_{14} to zero.	Set the low-order six bits at address 0000H in program memory to PC_{13-8}, set the contents of address 0001H to PC_{7-0}, and set PC_{14} to zero.
PSW	Carry flag (CY)	Retained	Undefined
	Skip flag (SK0-SK2)	0	0
	Interrupt status flag (IST0, IST1)	0	0
	Bank enable flag (MBE, RBE)	Set bit 6 of address 0000H in program memory to RBE and set bit 7 to MBE.	Set bit 6 of address 0000H in program memory to RBE and set bit 7 to MBE.
Stack pointer (SP)		Undefined	Undefined
Stack bank selection register (SBS)		Undefined	Undefined
Data memory (RAM)		Retained[Note]	Undefined
General register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank selection register (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
Timer/pulse generator	Modulo register (MODH, MODL)	Retained	Undefined
	Mode register (TPGM)	0	0
Clock timer	Mode register (WM)	0	0
Serial interface	Shift register (SIO)	Retained	Undefined
	Mode register (SIOM)	Set bit 4 to 1 and other bits to 0.	Set bit 4 to 1 and other bits to 0.
Clock generator	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
Interrupt	Interrupt request flag (IRQ××)	Reset (0)	Reset (0)
	Interrupt enable flag (IE××)	0	0
	Priority specification flag (IPS)	0	0
	INT0/INT1 mode register (IM0, IM1)	0, 0	0, 0
Digital port	Output buffer	Off	Off
	Output latch	Cleared (0)	Cleared (0)
	I/O mode register (PMGA, PMGB)	0	0
PORT H	Output latch	Retained	Undefined
FIP controller/driver	Display mode register (DSPM)	0	0
	Digit selection register (DIGS)	1000B	1000B
	Dimmer selection register (DIMS)	0	0
	Display data memory	Retained	Undefined
	Output buffer	Off	Off

Note Data from address 0F8H to address 0FDH in the data memory becomes undefined by $\overline{\text{RESET}}$ input.

9. INSTRUCTION SET

(1) Representation format and description method of operands

An operand is described in the operand field of each instruction according to the description method corresponding to the operand representation format of the instruction (refer to "RA75X Assembler Package User's Manual, Language" (EEU-1363) for details). When two or more elements are described in the description method field, select one of them. Uppercase letters, a plus sign (+), and a minus sign (-) are keywords, so they can be used without alteration.

Specify an appropriate numeric value or label for immediate data.

Representation format	Description method
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL-, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label[Note]
bit	2-bit immediate data or label
fmem	FB0H-FBFH/FF0H-FFFH immediate data or label
pmem	FC0H-FFFH immediate data or label
addr1	0000H-7F7FH immediate data or label
addr	0000H-3F7FH immediate data or label
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H-7FH immediate data (bit 0 = 0) or label
PORTn	PORT0-PORT6
IE×××	IEBT, IESIO, IET0, IETPG, IE0, IE1, IEKS, IEW, IE4
RBn	RB0-RB3
MBn	MB0, MB1, MB2, MB3, MB15

Note Only even addresses can be specified for 8-bit data processing.

(2) Legend

A	:	A register, 4-bit accumulator
B	:	B register, 4-bit accumulator
C	:	C register, 4-bit accumulator
D	:	D register, 4-bit accumulator
E	:	E register, 4-bit accumulator
H	:	H register, 4-bit accumulator
L	:	L register, 4-bit accumulator
X	:	X register, 4-bit accumulator
XA	:	Register pair (XA), 8-bit accumulator
BC	:	Register pair (BC), 8-bit accumulator
DE	:	Register pair (DE), 8-bit accumulator
HL	:	Register pair (HL), 8-bit accumulator
XA′	:	Extended register pair (XA′)
BC′	:	Extended register pair (BC′)
DE′	:	Extended register pair (DE′)
HL′	:	Extended register pair (HL′)
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag, bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 to 6)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority specification register
IE×××	:	Interrupt enable flag
RBS	:	Register bank select register
MBS	:	Memory bank select register
PCC	:	Processor clock control register
.	:	Address/bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Explanation of the symbols in the addressing area field

*1	MB = MBE•MBS (MBS = 0, 1, 2, 3, or 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0: MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1: MB = MBS (MBS = 0, 1, 2, 3, or 15)	
*4	MB = 15, fmem = FB0H-FBFH or FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-3F7FH	Program memory addressing
*7	addr = (Current PC) - 15 to (Current PC) - 1 or (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H-0FFFH ($PC_{14,13,12}$ = 000B) or 1000H-1FFFH ($PC_{14,13,12}$ = 001B) or 2000H-2FFFH ($PC_{14,13,12}$ = 010B) or 3000H-3FFFH ($PC_{14,13,12}$ = 011B) or 4000H-4FFFH ($PC_{14,13,12}$ = 100B) or 5000H-5FFFH ($PC_{14,13,12}$ = 101B) or 6000H-6FFFH ($PC_{14,13,12}$ = 110B) or 7000H-7F7FH ($PC_{14,13,12}$ = 111B)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	
*11	addr1 = 0000H-7F7FH	

Remarks 1. MB indicates an accessible memory bank.

2. For *2, MB is always 0 irrespective of MBE and MBS.

3. For *4 and *5, MB is always 15 irrespective of MBE and MBS.

4. *6 to *11 indicate each addressable area.

(4) Explanation of the machine cycle column

S represents the number of machine cycles required when a skip instruction with the skip function performs a skip operation. S assumes one of the following values:

- When no skip operation is performed : S = 0
- When a 1-byte instruction or 2-byte instruction is skipped : S = 1
- When a 3-byte instruction is skipped : S = 2

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle of the CPU clock Φ (= t_{CY}), and three types of times are available for selection according to the PCC setting.

Instruction	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A,#n4	1	1	A ← n4		String effect A
		reg1,#n4	2	2	reg1 ← n4		
		XA,#n8	2	2	XA ← n8		String effect A
		HL,#n8	2	2	HL ← n8		String effect B
		rp2,#n8	2	2	rp2 ← n8		
		A,@HL	1	1	A ← (HL)	*1	
		A,@HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A,@HL-	1	2 + S	A ← (HL), then L ← L - 1	*1	L = FH
		A,@rpa1	1	1	A ← (rpa1)	*2	
		XA,@HL	2	2	XA ← (HL)	*1	
		@HL,A	1	1	(HL) ← A	*1	
		@HL,XA	2	2	(HL) ← XA	*1	
		A,mem	2	2	A ← (mem)	*3	
		XA,mem	2	2	XA ← (mem)	*3	
		mem,A	2	2	(mem) ← A	*3	
		mem,XA	2	2	(mem) ← XA	*3	
		A,reg	2	2	A ← reg		
		XA,rp'	2	2	XA ← rp'		
		reg1,A	2	2	reg1 ← A		
		rp'1,XA	2	2	rp'1 ← XA		
	XCH	A,@HL	1	1	A ↔ (HL)	*1	
		A,@HL+	1	2 + S	A ↔ (HL), then L ← L + 1	*1	L = 0
		A,@HL-	1	2 + S	A ↔ (HL), then L ← L - 1	*1	L = FH
		A,@rpa1	1	1	A ↔ (rpa1)	*2	
		XA,@HL	2	2	XA ↔ (HL)	*1	
		A,mem	2	2	A ↔ (mem)	*3	
		XA,mem	2	2	XA ↔ (mem)	*3	
		A,reg1	1	1	A ↔ reg1		
		XA,rp'	2	2	XA ↔ rp'		
Table reference	MOVT	XA,@PCDE	1	3	XA ← $(PC_{14-8}+DE)_{ROM}$		
		XA,@PCXA	1	3	XA ← $(PC_{14-8}+XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$	*11	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$	*11	

Instruction	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY,fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← (H+mem_{3-0}.bit)	*1	
		fmem.bit,CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L,CY	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H+mem.bit,CY	2	2	(H+mem_{3-0}.bit) ← CY	*1	
Arithmetic/logical	ADDS	A,#n4	1	1 + S	A ← A + n4		carry
		XA,#n8	2	2 + S	XA ← XA + n8		carry
		A,@HL	1	1 + S	A ← A + (HL)	*1	carry
		XA,rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1,XA	2	2 + S	rp'1 ← rp'1 + XA		carry
	ADDC	A,@HL	1	1	A,CY ← A + (HL) + CY	*1	
		XA,rp'	2	2	XA,CY ← XA + rp' + CY		
		rp'1,XA	2	2	rp'1,CY ← rp'1 + XA + CY		
	SUBS	A,@HL	1	1 + S	A ← A - (HL)	*1	borrow
		XA,rp'	2	2 + S	XA ← XA - rp'		borrow
		rp'1,XA	2	2 + S	rp'1 ← rp'1 - XA		borrow
	SUBC	A,@HL	1	1	A,CY ← A - (HL) - CY	*1	
		XA,rp'	2	2	XA,CY ← XA - rp' - CY		
		rp'1,XA	2	2	rp'1,CY ← rp'1 - XA - CY		
	AND	A,#n4	2	2	A ← A ∧ n4		
		A,@HL	1	1	A ← A ∧ (HL)	*1	
		XA,rp'	2	2	XA ← XA ∧ rp'		
		rp'1,XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A,#n4	2	2	A ← A ∨ n4		
		A,@HL	1	1	A ← A ∨ (HL)	*1	
		XA,rp'	2	2	XA ← XA ∨ rp'		
		rp'1,XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A,#n4	2	2	A ← A ∀ n4		
		A,@HL	1	1	A ← A ∀ (HL)	*1	
		XA,rp'	2	2	XA ← XA ∀ rp'		
		rp'1,XA	2	2	rp'1 ← rp'1 ∀ XA		
Accumulator manipulation	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		

Instruction	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg - 1		reg = FH
		rp′	2	2 + S	rp′ ← rp′ - 1		rp′ = FFH
Comparison	SKE	reg,#n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL,#n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A,@HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA,@HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A,reg	2	2 + S	Skip if A = reg		A = reg
		XA,rp′	2	2 + S	Skip if XA = rp′		XA = rp′
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		

Instruction	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem$_{3-0}$.bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem$_{3-0}$.bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∀ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∀ (H+mem$_{3-0}$.bit)	*1	
Branch	BR	addr1	—	—	PC$_{14-0}$ ← addr1 (The assembler selects an appropriate instruction from the BR !addr, BRA !addr1, BRCB !caddr, and BR $addr instructions.)	*11	
		$addr	1	2	PC$_{14-0}$ ← addr	*7	
		!addr	3	3	PC$_{14}$ ← 0, PC$_{13-0}$ ← !addr	*6	
		PCDE	2	3	PC$_{14-0}$ ← PC$_{14-8}$ + DE		
		PCXA	2	3	PC$_{14-0}$ ← PC$_{14-8}$ + XA		
		BCDE	2	3	PC$_{14-0}$ ← BCDE		
		BCXA	2	3	PC$_{14-0}$ ← BCXA		
	BRA	!addr1	3	3	PC$_{14-0}$ ← !addr1	*11	
	BRCB	!caddr	2	2	PC$_{14-0}$ ← PC$_{14,13,12}$ + caddr$_{11-0}$	*8	

Instruction	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALL	!addr	3	4	(SP-6)(SP-3)(SP-4) ← PC_{11-0} (SP-5) ← 0,PC_{14},PC_{13}, PC_{12} (SP-2) ← ×,×,MBE,RBE PC_{14} ← 0, PC_{13-0} ← addr, SP ← SP - 6	*6	
	CALLA	!addr1	3	3	(SP-6)(SP-3)(SP-4) ← PC_{11-0} (SP-5) ← 0,PC_{14},PC_{13}, PC_{12} (SP-2) ← ×,×,MBE,RBE PC_{14-0} ← addr1, SP ← SP - 6	*11	
	CALLF	!faddr	2	3	(SP-6)(SP-3)(SP-4) ← PC_{11-0} (SP-5) ← 0,PC_{14},PC_{13}, PC_{12} (SP-2) ← ×,×,MBE,RBE PC_{14-0} ← 0000, faddr, SP ← SP - 6	*9	
	RET		1	3	×,×,MBE,RBE ← (SP+4) PC_{11-0} ← (SP)(SP+3)(SP+2) ×,PC_{14},PC_{13},PC_{12} ← (SP+1) SP ← SP + 6		
	RETS		1	3 + S	×,×,MBE,RBE ← (SP+4) PC_{11-0} ← (SP)(SP+3)(SP+2) ×,PC_{14},PC_{13},PC_{12} ← (SP+1) SP ← SP + 6 then skip unconditionally		Unconditionally
	RETI		1	3	×,PC_{14},PC_{13},PC_{12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP + 6		
	PUSH	rp	1	1	(SP-1)(SP-2) ← rp, SP ← SP - 2		
		BS	2	2	(SP-1) ← MBS, (SP-2) ← RBS, SP ← SP - 2		
	POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP+1), RBS ← (SP), SP ← SP + 2		
Interrupt control	EI		2	2	IME(IPS.3) ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME(IPS.3) ← 0		
		IE×××	2	2	IE××× ← 0		
I/O	IN[Note]	A,PORTn	2	2	A ← PORTn (n=0 to 6)		
		XA,PORTn	2	2	XA ← $PORTn_{+1}$,PORTn (n=4)		
	OUT[Note]	PORTn,A	2	2	PORTn ← A (n=2 to 6)		
		PORTn,XA	2	2	$PORTn_{+1}$,PORTn ← XA (n=4)		

Note MBE = 0, or MBE = 1 and MBS = 15 must be set when an IN/OUT instruction is executed.

Instruction	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
CPU control	HALT		2	2	Set HALT mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP mode (PCC.3 ← 1)		
	NOP		1	1	No operation		
Special	SEL	RBn	2	2	RBS ← n (n=0-3)		
		MBn	2	2	MBS ← n (n=0,1,2,3,15)		
	GETI[Note]	taddr	1	3	• For a TBR instruction $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr+1)$ $PC_{14} \leftarrow 0$	*10	
				4	• For a TCALL instruction $(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$ $(SP-5) \leftarrow 0, PC_{14}, PC_{13}, PC_{12}$ $(SP-2) \leftarrow \times,\times$,MBE,RBE $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr+1)$ $SP \leftarrow SP-6 \quad PC_{14} \leftarrow 0$		
				3	• For an instruction other than TBR and TCALL Executes the instruction in (taddr)(taddr+1).		Depends upon the referenced instruction.

Note The TBR and TCALL instructions are table definition assembler pseudo instructions of the GETI instructions.

10. MASK OPTION SELECTION

The μPD75218 has the following mask options enabling or disabling on-chip components.

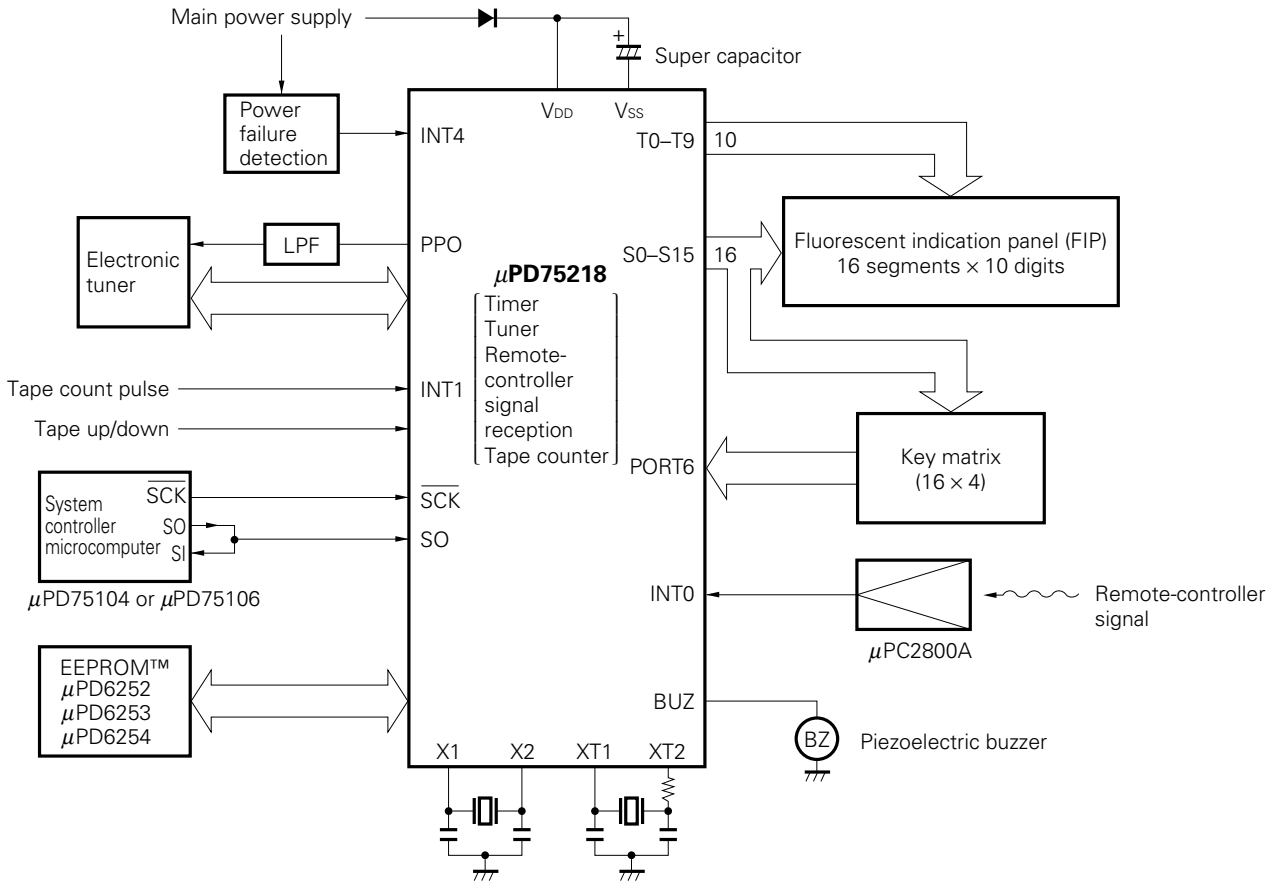
Pin	Mask option
P60 to P63	Pull-up resistor incorporation enabled in bit units
T0/T9	
T10/S15/PH3 to T13/S12/PH0	
T14/S11, T15/S10	
S0 to S9	
XT1, XT2	The feedback resistor for the subsystem clock oscillator can be removed

Cautions 1. In a system not using subsystem clocks, power consumption in the STOP mode can be decreased by removing the feedback resistor from the oscillator.

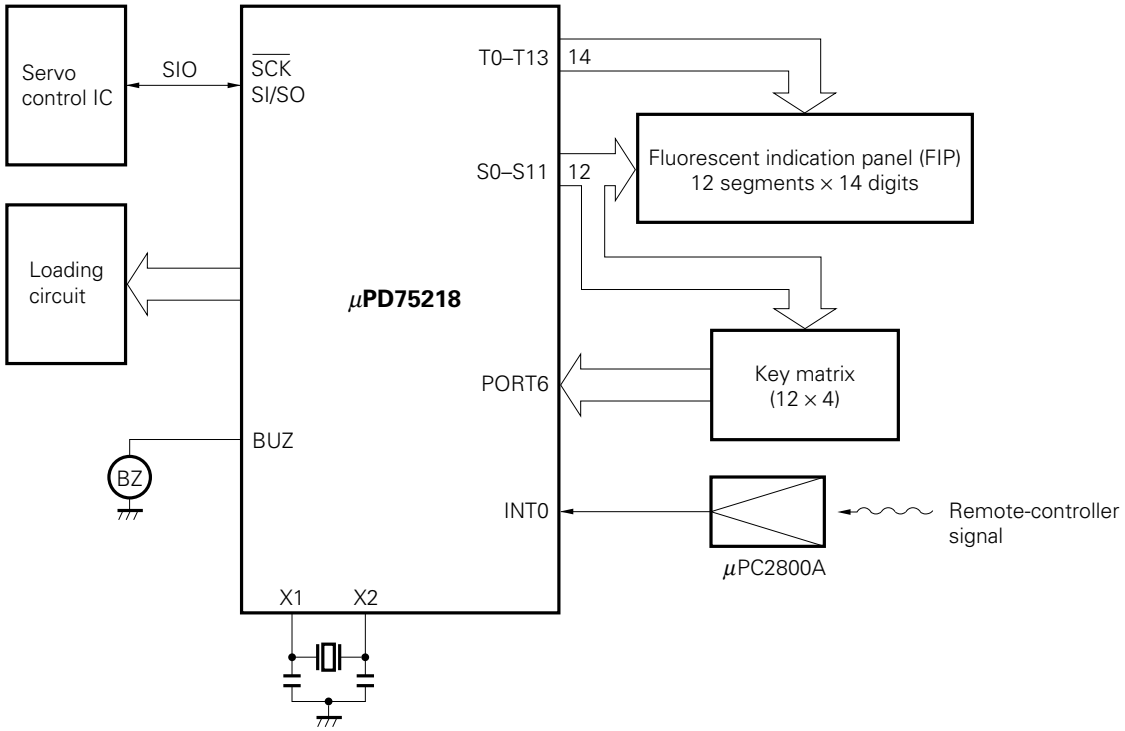
2. The feedback resistor must be incorporated when the subsystem clock is used.

11. APPLICATION BLOCK DIAGRAM

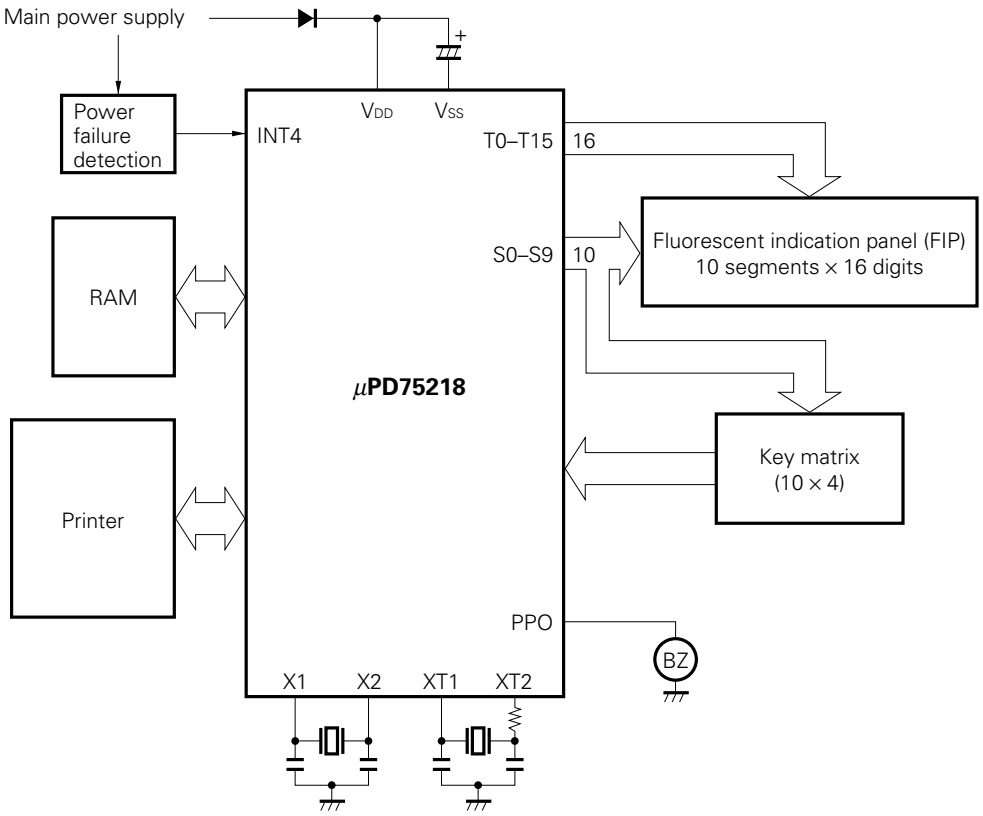
11.1 VCR TIMER TUNER



11.2 COMPACT DISK PLAYER



11.3 ECR



★ 12. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}		–0.3 to +7.0	V
	V_{LOAD}		V_{DD} – 40 to V_{DD} + 0.3	V
	V_{PRE}		V_{DD} – 11 to V_{DD} + 0.3	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Pins except display output pins	–0.3 to V_{DD} + 0.3	V
	V_{OD}	Display output pins	V_{DD} – 40 to V_{DD} + 0.3	V
Output high current	I_{OH}	Per pin except display output pins	–15	mA
		Per pin for S0 to S9	–15	mA
		Per pin for T0 to T15	–30	mA
		Total of pins except display output pins	–20	mA
		Total of display output pins	–120	mA
Output low current	I_{OL}	Per pin	17	mA
		Total of pins	60	mA
Total loss[Note 1]	P_T	Plastic QFP	450	mW
		Plastic shrink DIP	600	mW
Operating temperature	T_{opt}		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

OPERATING SUPPLY VOLTAGE (Ta = –40 to +85 °C)

Parameter	Conditions	Min.	Max.	Unit
CPU[Note 2]		[Note 3]	6.0	V
Display controller		4.5	6.0	V
Timer/pulse generator		4.5	6.0	V
Other hardware[Note 2]		2.7	6.0	V

Notes 1. Calculation of total loss

Design so that the sum of the following three power consumption values for the μPD75218CW/GF will be less than the total loss P_T (It is recommended to use the system with 80 % or less of the rating).

① CPU loss : Given as V_{DD} (Max.) × I_{DD1} (Max.)

② Output pin loss : There are normal output pin loss and display output pin loss. It is necessary to add a loss derived from the flow of maximum current to each output pin.

③ Pull-down register loss: Power loss due to a pull-down resistor incorporated in the display output pin by mask option.

Example Suppose 4-LED output with 9 segments and 11 digits, V_{DD} = 5 V + 10 % and 4.19 MHz oscillation and let a maximum of 3 mA, 15 mA and, 10 mA flow to a segment pin, timing pin and LED output pin, respectively. Further, let the voltage of fluorescent display tube (V_{LOAD} voltage) be –30 V and normal voltage be small.

① CPU loss : 5.5 V × 9.0 mA = 49.5 mW

② Pin loss : Segment pin ..... 2 V × 3 mA × 9 = 54 mW

Timing pin ..... 2 V × 15 mA = 30 mW

$$\text{LED output} \ldots\ldots \left(\frac{10}{15} \times 2\ \text{V}\right) \times 10\ \text{mA} \times 4 = 53\ \text{mW}$$

③ Pull-down resistor loss ..... $\dfrac{(30 + 5.5\ \text{V})^2}{25\ \text{k}\Omega} \times 10 = 504.1\ \text{mW}$

P_T = ① + ② + ③ = 690.6 mW

In this example, the power consumption of 690.6 mW is higher than the allowable total loss for the shrink DIP package (600 mW). It is necessary to decrease power consumption by decreasing the number of on-chip pull-down resistors. In this example, power consumption can be adjusted to 577.8 mW by incorporating pull-down resistors in only 11 digit outputs and 7 segment outputs and externally mounting pull-down resistors to the 2 remaining segment outputs.

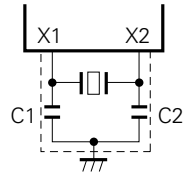
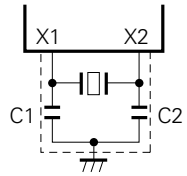
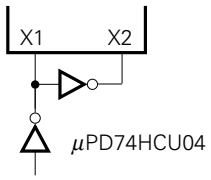
2. Except the system clock oscillator, display controller and timer/pulse generator.

3. The operating voltage range varies depending on the cycle time. Refer to the AC characteristics.

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance		C_{IN}				15	pF
Output capacitance	Except display output	C_{OUT}	f = 1 MHz 0 V for pins other than pins to be measured			15	pF
	Display output					35	pF
Input /output capacitance		C_{IO}				15	pF

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATOR (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constants	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator **Note 3**		Oscillator frequency (f_{XX}) **Note 1**	V_{DD} = Oscillation voltage range	2.0		6.2	MHz
		Oscillation settling time **Note 2**	After V_{DD} reaches Min. of the oscillation voltage range			4	ms
Crystal resonator **Note 3**		Oscillator frequency (f_{XX}) **Note 1**		2.0	4.19	6.2	MHz
		Oscillation settling time **Note 2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) **Note 1**		2.0		6.2	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		250	ns

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

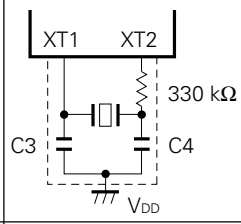
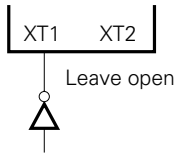
2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} reaches Min. of the oscillation voltage range or after the STOP mode is released.

3. See "Recommended Parameters for the Oscillation Circuit" for the resonators.

Caution When the main system clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas. Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{DD}. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

CHARACTERISTICS OF THE SUBSYSTEM CLOCK OSCILLATOR (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constants	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal resonator **Note 3**		Oscillator frequency (f_{XT}) **Note 1**		32	32.768	35	kHz
		Oscillation settling time **Note 2**	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		10		32	μs

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} reaches Min. of the oscillation voltage range.

3. Recommended resonators are listed on the next page.

Caution When the subsystem clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas. Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{DD}. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

When the subsystem clock is used, pay special attention to its wiring; the subsystem clock oscillator has low amplification to minimize current consumption and is more likely to malfunction due to noise than the main system clock oscillator.

RECOMMENDED PARAMETERS FOR THE OSCILLATION CIRCUIT

When a ceramic resonator is used for the main system clock (T_a = -40 to +70 °C)

Manufacturer	Product name	Oscillation frequency (MHz)	External capacitance (pF)		Oscillation voltage range (V)	
			C1	C2	Min.	Max.
Murata Mfg.	CSA×××MG	2.00 to 2.44	30	30	2.7	6.0
	CST×××MG		Built-in	Built-in		
	CSA×××MG093	2.45 to 3.50	30	30		
	CST×××MGW093		Built-in	Built-in		
	CSA×××MGU	2.51 to 6.00	30	30		
	CST×××MGWU		Built-in	Built-in		
	CSA×××MG	2.45 to 3.50	30	30	3.0	
	CST×××MGW		Built-in	Built-in		
	CSA×××MG	2.51 to 6.00	30	30	3.3	
	CST×××MGW		Built-in	Built-in		

When a ceramic resonator is used for the main system clock (T_a = -20 to +80 °C)

Manufacturer	Product name	Oscillation frequency (MHz)	External capacitance (pF)		Oscillation voltage range (V)	
			C1	C2	Min.	Max.
Kyocera	KBR-2.0MS	2.0	47	47	2.7	6.0
	KBR-4.0MWS	4.0	33	33		
	KBR-4.19MWS	4.19	Built-in	Built-in		
	KBR-4.19MSA		33	33		
	KBR-4.19MKS		Built-in	Built-in		
	PBRC 4.19A		33	33		
	KBR-6.0MWS	6.0	Built-in	Built-in		
	KBR-6.0MSA		33	33		
	KBR-6.0MKS		Built-in	Built-in		
	PBRC 6.00A		33	33		

When a crystal resonator is used for the main system clock (T_a = -20 to +70 °C)

Manufacturer	Product name	Oscillation frequency (MHz)	External capacitance (pF)		Oscillation voltage range (V)	
			C1	C2	Min.	Max.
Kinseki	HC-49/U-S	3.072 to 6.000	18	18	2.7	6.0

When a crystal resonator is used for the subsystem clock (T_a = -15 to +60 °C)

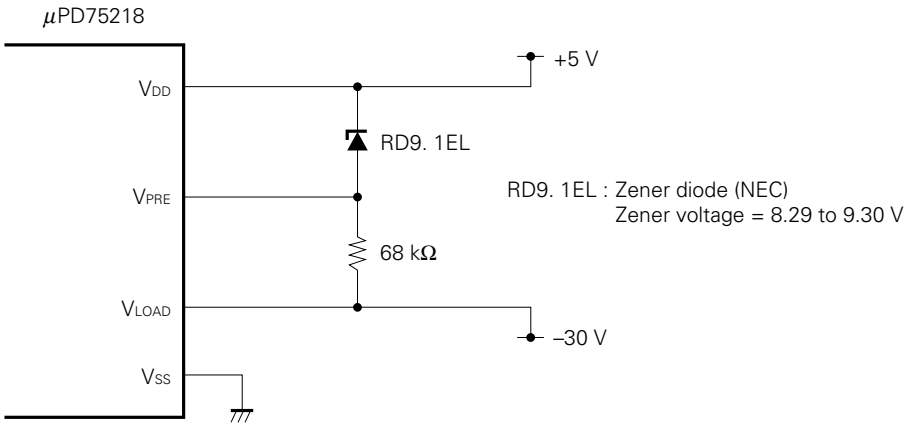
Manufacturer	Product name	Oscillation frequency (MHz)	External capacitance and resistance			Oscillation voltage range (V)	
			C1 (pF)	C2 (pF)	R (kΩ)	Min.	Max.
Kyocera	KF-38G	32.768	18	18	220	4.0	6.0

Caution When finely adjusting the oscillation frequency of a crystal resonator, adjust external capacitance C1 or C3.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
Input high voltage	V_{IH1}	Except below			0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, $\overline{RESET}$			0.75V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2, XT1			V_{DD}–0.4		V_{DD}	V
	V_{IH4}	Port 6	V_{DD} = 4.5 to 6.0 V		0.65V_{DD}		V_{DD}	V
					0.7V_{DD}		V_{DD}	V
Input low voltage	V_{IL1}	Except below			0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, $\overline{RESET}$			0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1			0		0.4	V
Output high voltage	V_{OH}	All output pins	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD}–1.0			V
			I_{OH} = –100 μA		V_{DD}–0.5			V
Output low voltage	V_{OL}	Ports 4, 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA			0.5	2.0	V
		All output pins	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
			I_{OL} = 400 μA				0.5	V
Input high leakage current	I_{LIH1}	Except X1,X2,XT1	V_{IN} = V_{DD}				3	μA
	I_{LIH2}	X1, X2, XT1					20	μA
Input low leakage current	I_{LIL1}	Except X1,X2,XT1	V_{IN} = 0 V				–3	μA
	I_{LIL2}	X1, X2, XT1					–20	μA
Output high leakage current	I_{LOH}	All output pins	V_{OUT} = V_{DD}				3	μA
Output low leakage current	I_{LOL1}	Except display output	V_{OUT} = 0 V				–3	μA
	I_{LOL2}	Display output	V_{OUT} = V_{LOAD} = V_{DD} – 35 V				–10	μA
Display output current	I_{OD}	S0 to S9	V_{DD} = 4.5 to 6.0 V, V_{OD} = V_{DD} – 2 V	V_{PRE} = V_{DD} – 9 ±1 V[Note 1]	–3	–5.5		mA
				V_{PRE} = 0 V	–1.5	–3.5		mA
		T0 to T15		V_{PRE} = V_{DD} – 9 ±1 V[Note 1]	–15	–22		mA
				V_{PRE} = 0 V	–7	–15		mA
Built-in pull-down resistor (mask option)	R_{P6}	Port 6 V_{IN} = V_{DD}	V_{DD} = 4.5 to 6.0 V		20	80	200	kΩ
					20		1000	kΩ
	R_L	Display output	V_{OD} – V_{LOAD} = 35 V		25	70	135	kΩ
Supply current[Note 2]	I_{DD1}	6.0 MHz crystal oscillation C1 = C2 = 15pF	V_{DD} = 5 V ±10 %[Note 3]			4.0	13.5	mA
			V_{DD} = 3 V ±10 %[Note 4]			0.55	1.8	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10 %		600	1800	μA
				V_{DD} = 3 V ±10 %		200	600	μA
	I_{DD1}	4.19 MHz crystal oscillation C1 = C2 = 15pF	V_{DD} = 5 V ±10 %[Note 3]			3.0	9.0	mA
			V_{DD} = 4 V ±10 %[Note 4]			0.45	1.5	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10 %		550	1800	μA
				V_{DD} = 3 V ±10 %		180	600	μA
	I_{DD3}	32 kHz crystal oscillation[Note 5]	V_{DD} = 3 V ±10 %			40	120	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10 %		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10 %			0.5	20	μA
			V_{DD} = 3 V ±10 %			0.1	10	μA

Notes 1. The following external circuit is recommended.



2. Current to the on-chip pull-down resistor (mask option) is not included.

3. When the processor clock control register (PCC) is set to 0011 and is operated in the high-speed mode.

4. When the PCC register is set to 0000 and is operated in the low-speed mode.

5. When the system clock control register (SCC) is set to 1001 and is operated with the subsystem clock with main system clock oscillation stopped.

AC CHARACTERISTICS (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

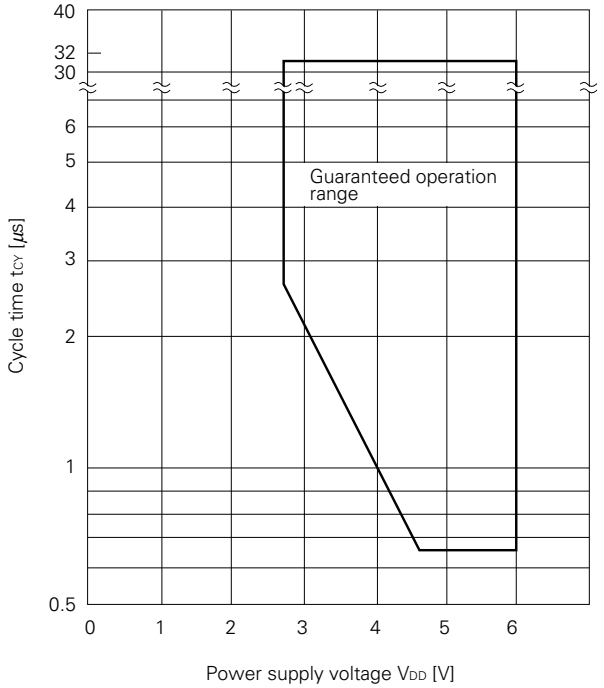
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CPU clock cycle time (minimum instruction execution time = 1 machine cycle)**Note 1**	t_{CY}	Operation with main system clock	V_{DD} = 4.5 to 6.0 V	0.67		32	μs
				2.6		32	μs
		Operation with sub-system clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		0.6	MHz
				0		165	kHz
TI0 input high and low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.83			μs
				3			μs
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 to 6.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
$\overline{SCK}$ high and low-level widths	t_{KH}, t_{KL}	V_{DD} = 4.5 to 6.0 V	Input	0.4			μs
			Output	t_{KCY}/2–50			ns
			Input	1.6			μs
			Output	t_{KCY}/2–150			ns
SI setup time (referred to $\overline{SCK}$↑)	t_{SIK}			100			ns
SI hold time (referred to $\overline{SCK}$↑)	t_{KSI}			400			ns
Delay from $\overline{SCK}$↓ to SO output	t_{KSO}	V_{DD} = 4.5 to 6.0 V				300	ns
						1000	ns
Interrupt input high and low-level widths	t_{INTH}, t_{INTL}		INT0	**Note 2**			μs
			INT1	2t_{CY}			μs
			INT2, INT4	10			μs
$\overline{RESET}$ low-level width	t_{RSL}			10			μs

Notes 1. CPU clock (Φ) cycle time is determined by the oscillator frequency of the connected resonator, the system clock control register (SCC) and the processor clock control register (PCC). The cycle time t_{CY} characteristics for power supply voltage V_{DD} when the main system clock is in operation is shown on the right.

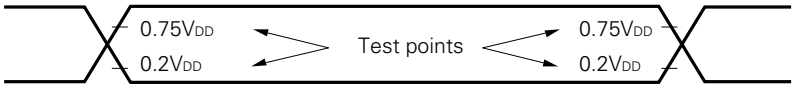
2. 2t_{CY} or 128/f_{XX} is set by interrupt mode register (IM0) setting.

t_{CY} vs V_{DD}

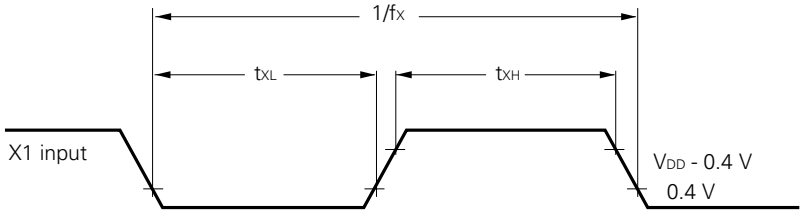
(Operation with main system clock)

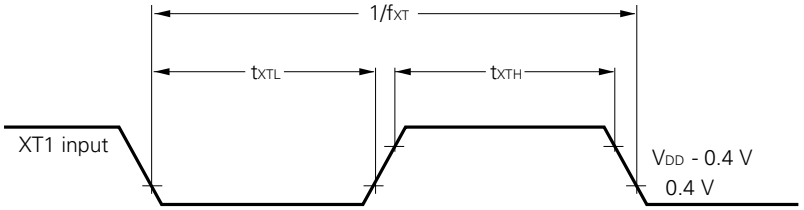


AC Timing Measurement Values (Except X1 and XT1 Inputs)

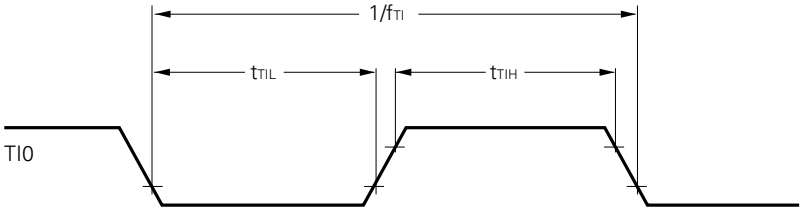


Clock Timing

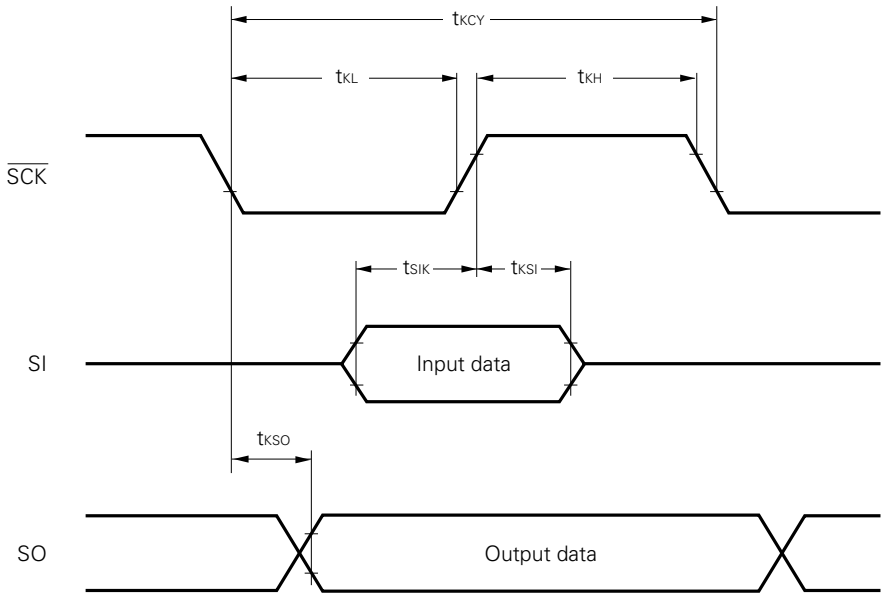




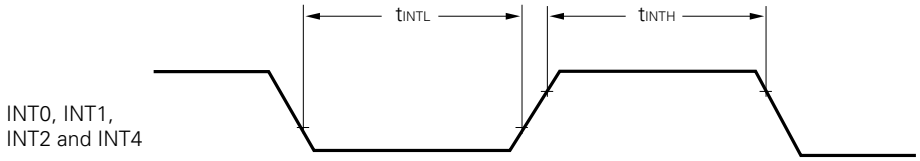
TI0 Timing



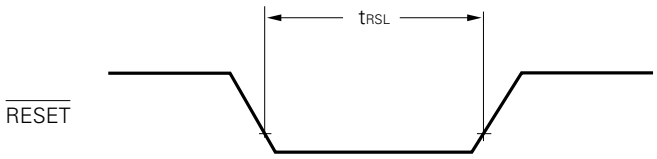
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA RETENTION CHARACTERISTICS FOR DATA MEMORY AT LOW SUPPLY VOLTAGE IN STOP MODE
(Ta = –40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current Note 1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation settling time Note 2	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		Note 3		ms

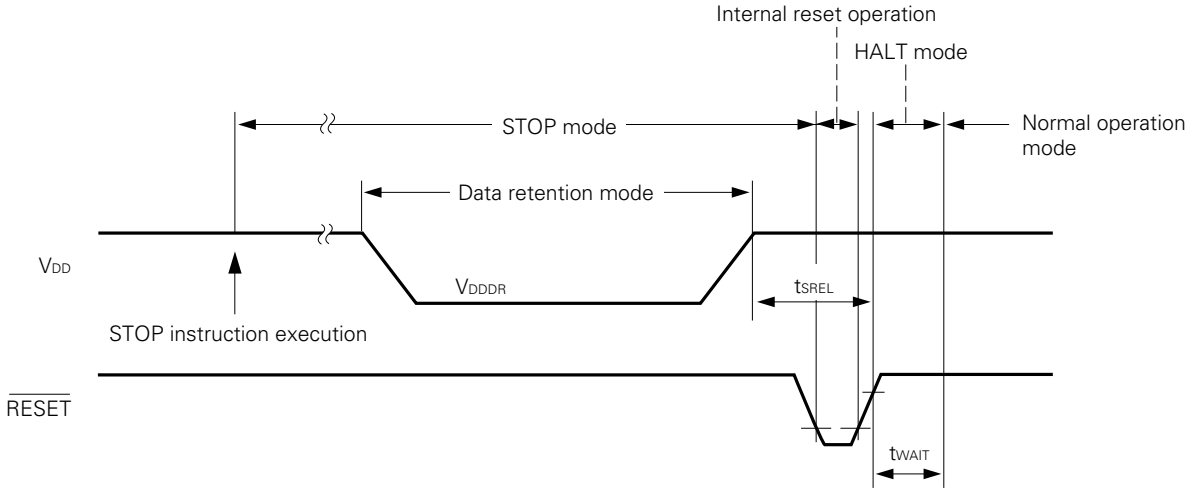
Notes 1. Current to the on-chip pull-down resistor (mask option) is not included.

2. Oscillation settling time is time to stop CPU operation to prevent unstable operation upon oscillation start.

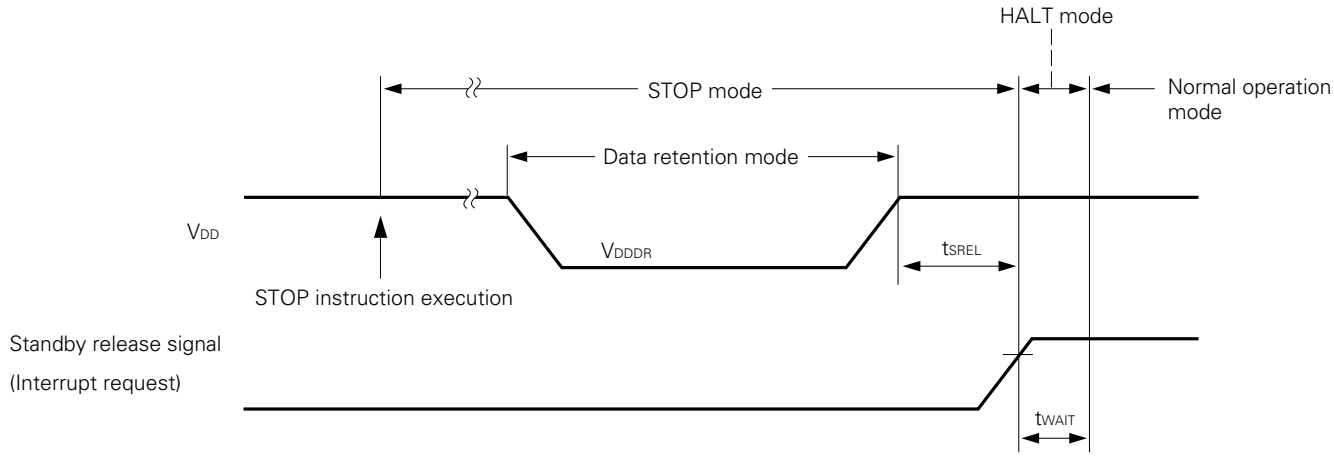
3. According to the setting of the basic interval timer mode register (BTM) (See below.)

BTM3	BTM2	BTM1	BTM0	Settling time (values at f_{XX} = 6.0 MHz in parentheses)
—	0	0	0	$2^{20}/f_{XX}$ (approx. 175 ms)
—	0	1	1	$2^{17}/f_{XX}$ (approx. 21.8 ms)
—	1	0	1	$2^{15}/f_{XX}$ (approx. 5.46 ms)
—	1	1	1	$2^{13}/f_{XX}$ (approx. 1.37 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

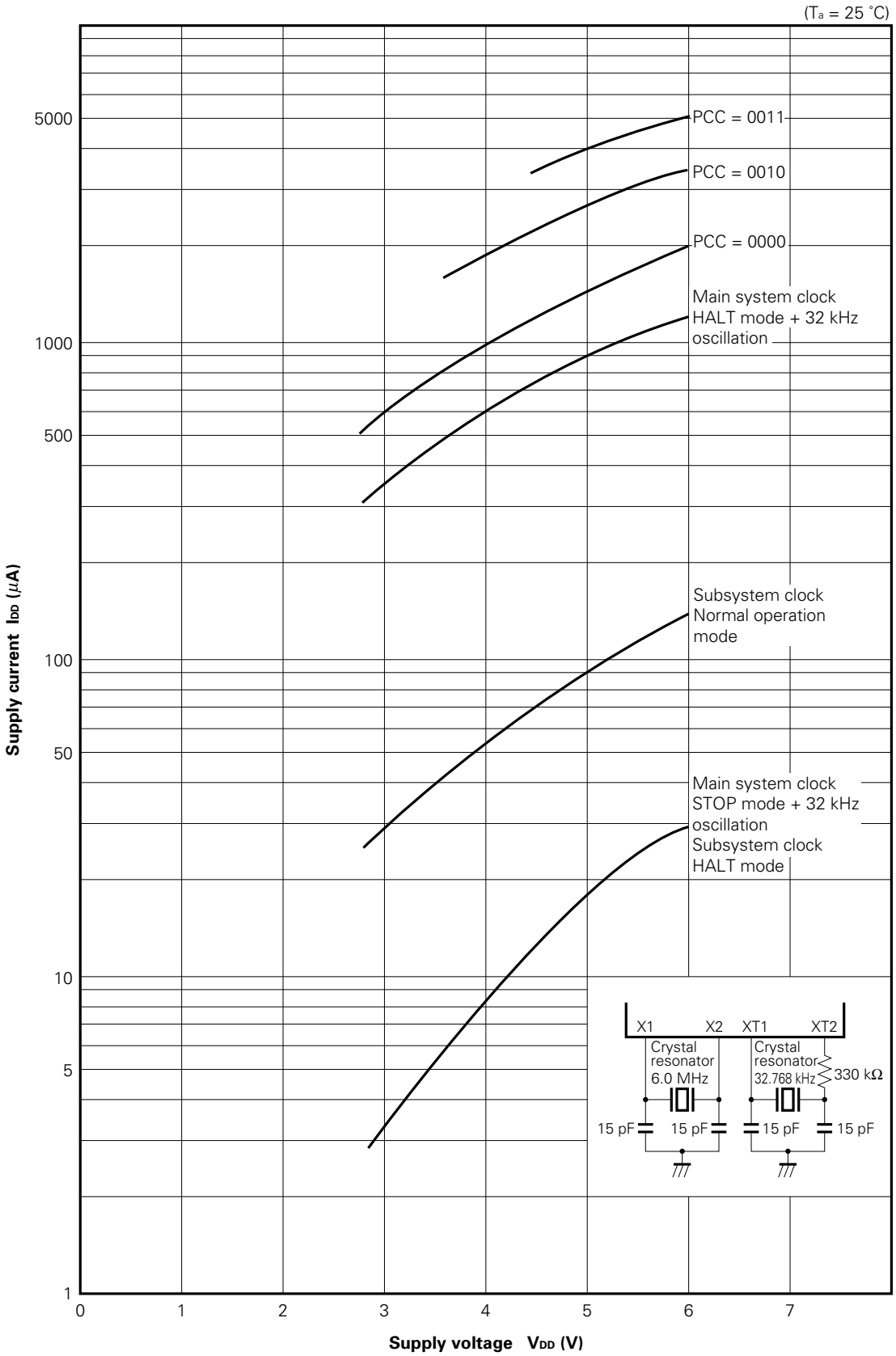


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

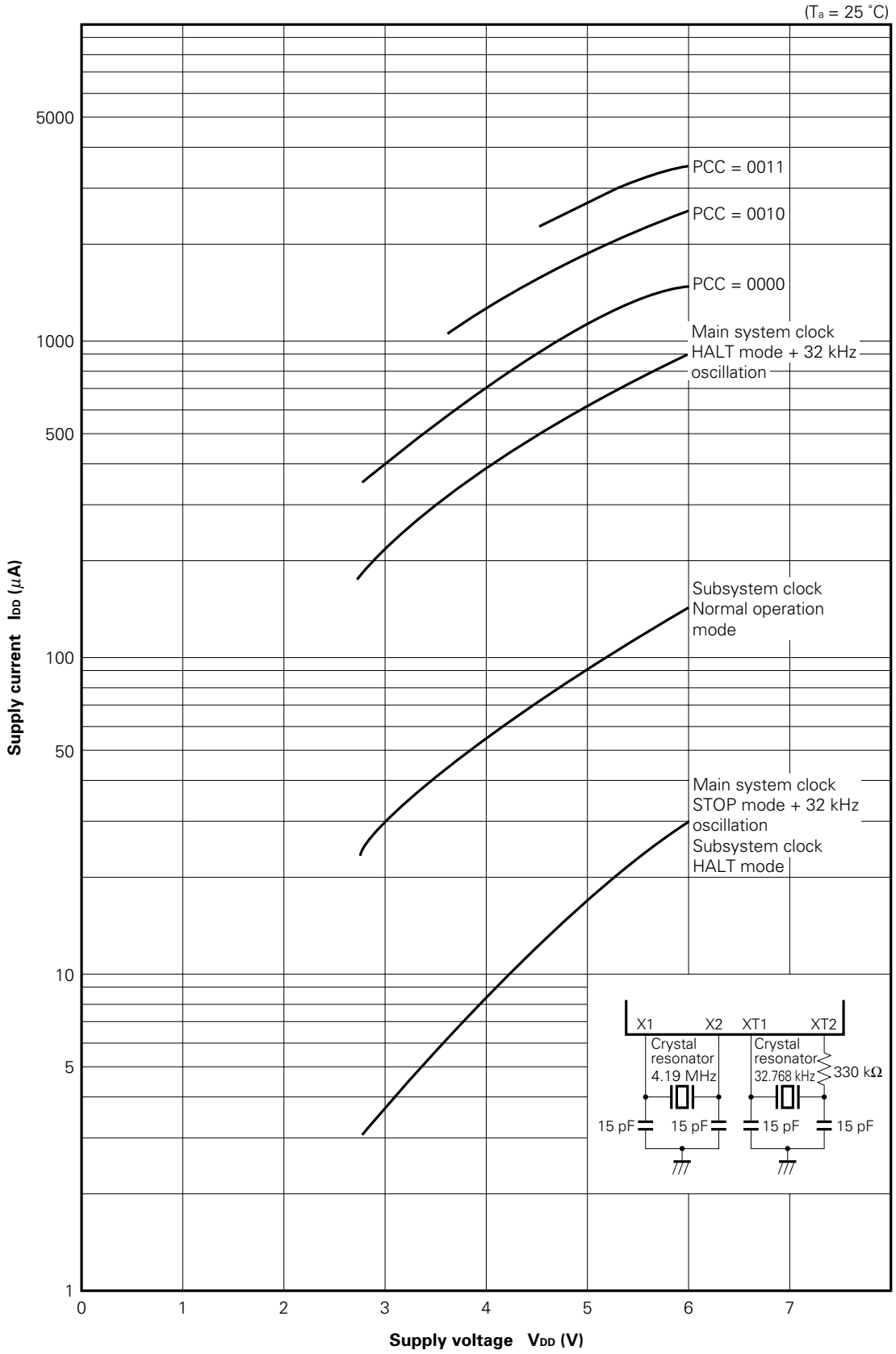


13. CHARACTERISTIC CURVES (FOR REFERENCE) ★

I_{DD} vs V_{DD} (Main system clock: 6.0 MHz)

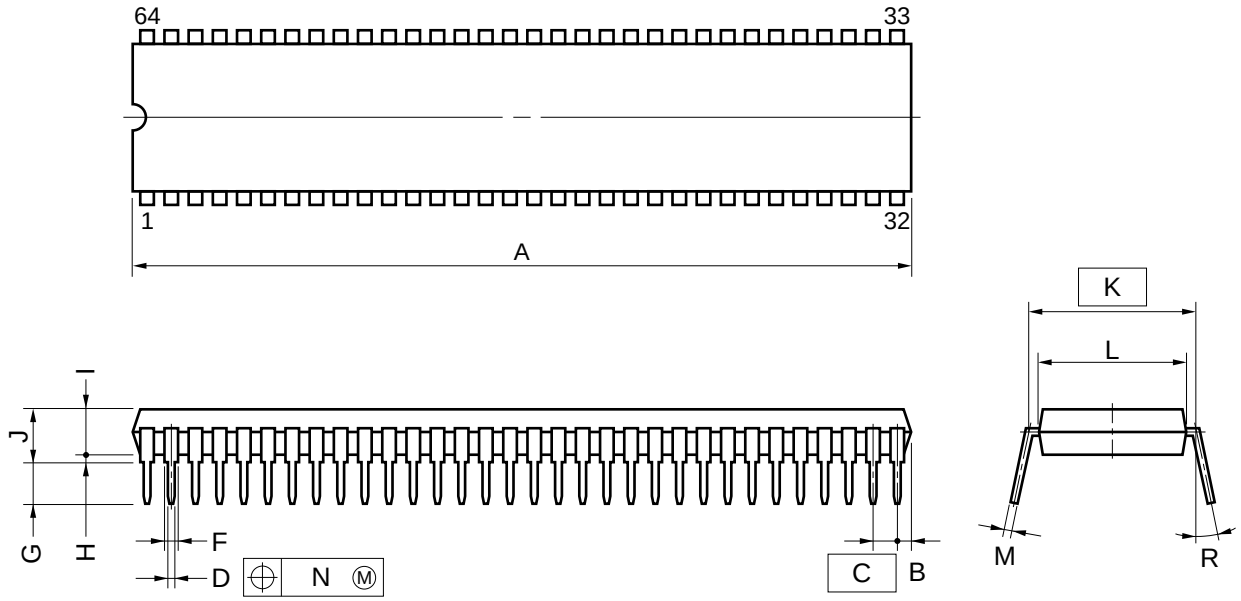


I_{DD} vs V_{DD} (Main system clock: 4.19 MHz)



14. PACKAGE DIMENSIONS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

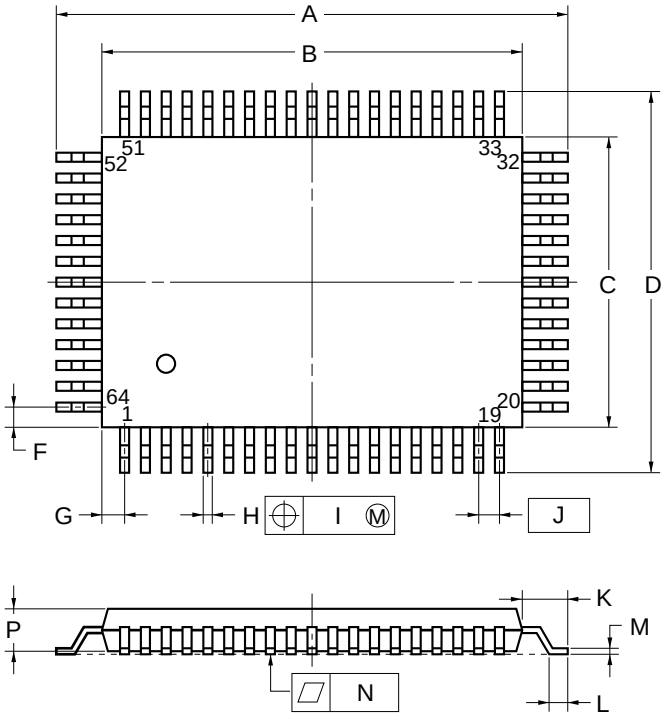
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

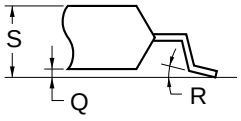
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.008}_{-0.009}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P64GF-100-3B8,3BE,3BR-2

15. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For the details of the recommended soldering conditions refer to our document **SMD Surface Mount Technology Manual**(IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 15-1 Soldering Conditions for Surface-Mount Devices

μPD75218GF-×××-3BE: 64-pin plastic QFP (14 × 20 mm)

Soldering process	Soldering conditions	Symbol
Wave soldering	Temperature in the soldering vessel: 260 ˚C or less Soldering time: 10 seconds or less Number of soldering processes: 1 Pre-heating temperature: 120 ˚C max. (package surface temperature) Exposure limit[Note]: 2 days (20 hours of pre-baking is required at 125 ˚C afterward.)	WS60-202-1
Infrared ray reflow	Peak package's surface temperature: 230 ˚C Reflow time: 30 seconds or less (at 210 ˚C or more) Number of reflow processes: 1 Exposure limit[Note]: 2 days (20 hours of pre-baking is required at 125 ˚C afterward.)	IR30-202-1
VPS	Peak package's surface temperature: 215 ˚C Reflow time: 40 seconds or less (at 200 ˚C or more) Number of reflow processes: 1 Exposure limit[Note]: 2 days (20 hours of pre-baking is required at 125 ˚C afterward.)	VP15-202-1
Partial heating method	Terminal temperature: 300 ˚C or less Flow time: 3 seconds or less (one side per device)	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 ˚C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

Table 15-2 Soldering Conditions for Inserted Devices

μPD75218CW-×××: 64-pin plastic shrink DIP (750 mil)

Soldering process	Soldering conditions
Wave soldering (only for leads)	Temperature in the soldering vessel: 260 °C or less Soldering time: 10 seconds or less
Partial heating method	Terminal temperature: 260 °C or less Flow time: 10 seconds or less

Caution In wave soldering, apply solder only to the lead section. Care must be taken that jet solder does not contact the main body of the package.

Notice

Other versions of the products are available. For these versions, the recommended reflow soldering conditions have been mitigated as follows:
Higher peak temperature (235 °C), two-stage, and longer exposure limit.
Contact an NEC representative for details.

APPENDIX A FUNCTIONS OF μPD752×× SERIES PRODUCTS

Item		μPD75216A	μPD75217	μPD75218	μPD75P218
ROM		16256 × 8	24448 × 8	32640 × 8	
RAM		512 × 4	768 × 4	1024 × 4	
Instruction cycle	When main system clock is selected	0.95 μs/1.91 μs/15.3 μs (When the microcomputer operates at 4.19 MHz)		0.67 μs/1.33 μs/10.7 μs (When the microcomputer operates at 6.0 MHz) 0.95 μs/1.91 μs/15.3 μs (When the microcomputer operates at 4.19 MHz)	
	When sub-system clock is selected	122 μs (When the microcomputer operates at 32.768 kHz)			
I/O lines including FIP dual-function pins and excluding FIP dedicated pins	Total number of I/O lines	33			
	CMOS input lines	8			
	CMOS I/O lines	20: 8 lines for driving LED			
		Port 6: Pull-down resistors contained (mask option)			Port 6: No pull-down resistors contained
	CMOS output lines	1: Timer/pulse generator output			
	P-ch open-drain output with high withstand voltage and high current	4 lines for driving LED: Pull-down resistors contained (mask option)			No pull-down resistors contained
FIP controller/driver	Output with high withstand voltage	26 lines: 40 V max.			
		Whether built-in pull-down resistors are used or the pins are used as open-drain output is selected bit by bit (mask option).			S0-S8,T0-T9: Built-in pull-down resistors used S9,T10-T15: Open-drain output
	Number of segments	9 to 16			
	Number of digits	9 to 16			
Timer		4 channels • Timer/event counter • Basic interval timer : Watchdog timer operation is possible. • Timer/pulse generator : 14-bit PWM output is possible. • Watch timer : Buzzer output is possible.			
Serial interface		MSB or LSB first can be selected. Serial bus can be configured.			
Vectored interrupt		External: 3, internal: 5			
Test input		External: 1, internal: 1			
System clock oscillator		2 built-in circuits • When main system clock is selected: 6.0 MHz (the μPD75218 and μPD75P218 only) 4.19 MHz • When subsystem clock is selected: 32.768 kHz			
Power-on reset circuit		Incorporated (mask option)	None		
Data retention at low supply voltage		Possible (2 V)			
★ Operating temperature range		-40 to +85 °C			-40 to +70 °C
Operating supply voltage		2.7 to 6.0 V			
Package		64-pin plastic shrink DIP (750 mil) 64-pin plastic QFP (14 × 20 mm) 64-pin ceramic WQFN (the μPD75P218 only)			

APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided for developing systems including the μPD75218:

Hardware	IE-75000-R[Note 1] IE-75001-R	In-circuit emulator for the 75X series
	IE-75000-R-EM[Note 2]	Emulation board for the IE-75000-R and IE-75001-R
	EP-75216ACW-R	Emulation probe for the μPD75218CW
	EP-75216AGF-R EV-9200G-64	Emulation probe for the μPD75218GF. A 64-pin conversion socket, the EV-9200G-64, is attached to the probe.
	PG-1500	PROM programmer
	PA-75P216ACW	PROM programmer adapter for the μPD75P218CW. Connected to the PG-1500.
	PA-75P218GF	PROM programmer adapter for the μPD75P218GF. Connected to the PG-1500.
	PA-75P218KB	PROM programmer adapter for the μPD75P218KB. Connected to the PG-1500.
Software	IE control program	Host machine • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A[Note 3]) • IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

Notes 1. Maintenance service only

2. Not contained in the IE-75001-R

3. These software cannot use the task swap function, which is available in MS-DOS Ver. 5.00 and Ver. 5.00A.

Remark Refer to "75X Series Selection Guide" (IF-1027) for development tools manufactured by third parties.

APPENDIX C RELATED DOCUMENTS

Documents related to the device

Document name	Document No.
User's manual	IEU-692
75X series selection guide	IF-1027

Documents related to development tools

	Document name		Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1416
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75216ACW-R User's Manual		EEU-1321
	EP-75216AGF-R User's Manual		EEU-1309
	PG-1500 User's Manual		EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-1346
		Language	EEU-1363
	PG-1500 Controller User's Manual		EEU-1291

Other related documents

Document name	Document No.
Package Manual	IEI-1213
SMD Surface Mount Technology Manual	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEI-1203
Electrostatic Discharge (ESD) Test	IEI-1201
Guide to Quality Assurance for Semiconductor Devices	MEI-1202

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

[MEMO]

M4 92.6