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April 1st, 2010
Renesas Electronics Corporation

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Data Sheet

4-Bit Single-Chip Microcomputer

Description

The μPD75116 is one of the 4-bit single-chip microcomputer 75X series.

The μPD75116 is a product with the extended ROM capacity of the μPD75108. In addition of high-speed operations, it can manipulate data in units of 1, 4 and 8 bits. In particular, the I/O operation of the μPD75116 have been improved by a wide variety of bit control instructions. The μPD75116 is provided with interface inputs/outputs with peripheral circuits having different power vltages, LED direct drive outputs and analog inputs.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μPD751xx Series User's Manual: IEM-922

Features

- Architecture "75X" equivalent to 8-bit microcomputer
- Minimum instruction execution time (high-speed operation): 0.95 μs (when operated at 4.19 MHz and 5 V)
- Instruction execution variable function: 0.95μs/1.91μs/15.3 μs (when operated at 4.19 MHz)
- Many input/output ports: 58
- 3-channel on-chip 8-bit timers
- 8-bit on-chip serial interface
- Multi-interruptible vector interrupt function
- On-chip PROM product available: μPD75P116 (one-time) PROM

Ordering Information

Ordering Code	Package	Quality Grade
μPD75112CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75112GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard
μPD75116CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75116GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard

Remarks: xxx is a ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Applications

Control of VCRs, audio products, push-button telephones, wireless machines, printers, etc.

Unless there are any particular functional differences, the μPD75116 is described in this document as a representative product.

The information in this document is subject to change without notice.
The mark ★ shows major revised points.

Outline of Functions

Item	Description	
No. of basic instruction	43	
Min. instruction execution time	0.95 μ s/1.91 μ s/15.3 μ s (when operated at 4.19 MHz), switchable at 3 levels	
On-chip memory	ROM	12160 \times 8 (μ PD75112), 16256 \times 8 (μ PD75116)
	RAM	512 \times 4
General register	4 bits \times 8 \times 4 banks (memory mapping)	
Accumulator	Three accumulated in compliance with controlled date lengths <ul style="list-style-type: none"> • 1-bit accumulator (CY), 4-bit accumulator (A), 8-bit accumulator (XA) 	
Input/output port	58 in total <ul style="list-style-type: none"> • CMOS input pin : 10 • CMOS input/output pin (LED direct drive enable) : 32 • Intermediate withstand voltage N-ch open drain : 12 input/output pin (LED direct drive enable, bitwise pull-up resistor incorporation enable) • Comparator input pin (4-bit accuracy) : 4 	
Timer/counter	<ul style="list-style-type: none"> • 8-bit timer/event counter \times 2 • 8-bit basic interval timer (applicable to watchdog timer) 	
Serial interface	<ul style="list-style-type: none"> • 8-bits • First LSB/first MSB switchable • Two transfer modes (transmit and receiver/receive dedicated mode) 	
Vector interrupt	External : 3, Internal : 4	
Test input	External : 2	
Standby	<ul style="list-style-type: none"> • STOP/HALT mode 	
Operating temperature range	-40 to +85°C	
Operating voltage	2.7 to 6.0 V	
Others	<ul style="list-style-type: none"> • On-chip power-on reset circuit (mask option) • On-chip bit control memory (bit sequential buffer) 	
Package	<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 \times 20 mm) 	

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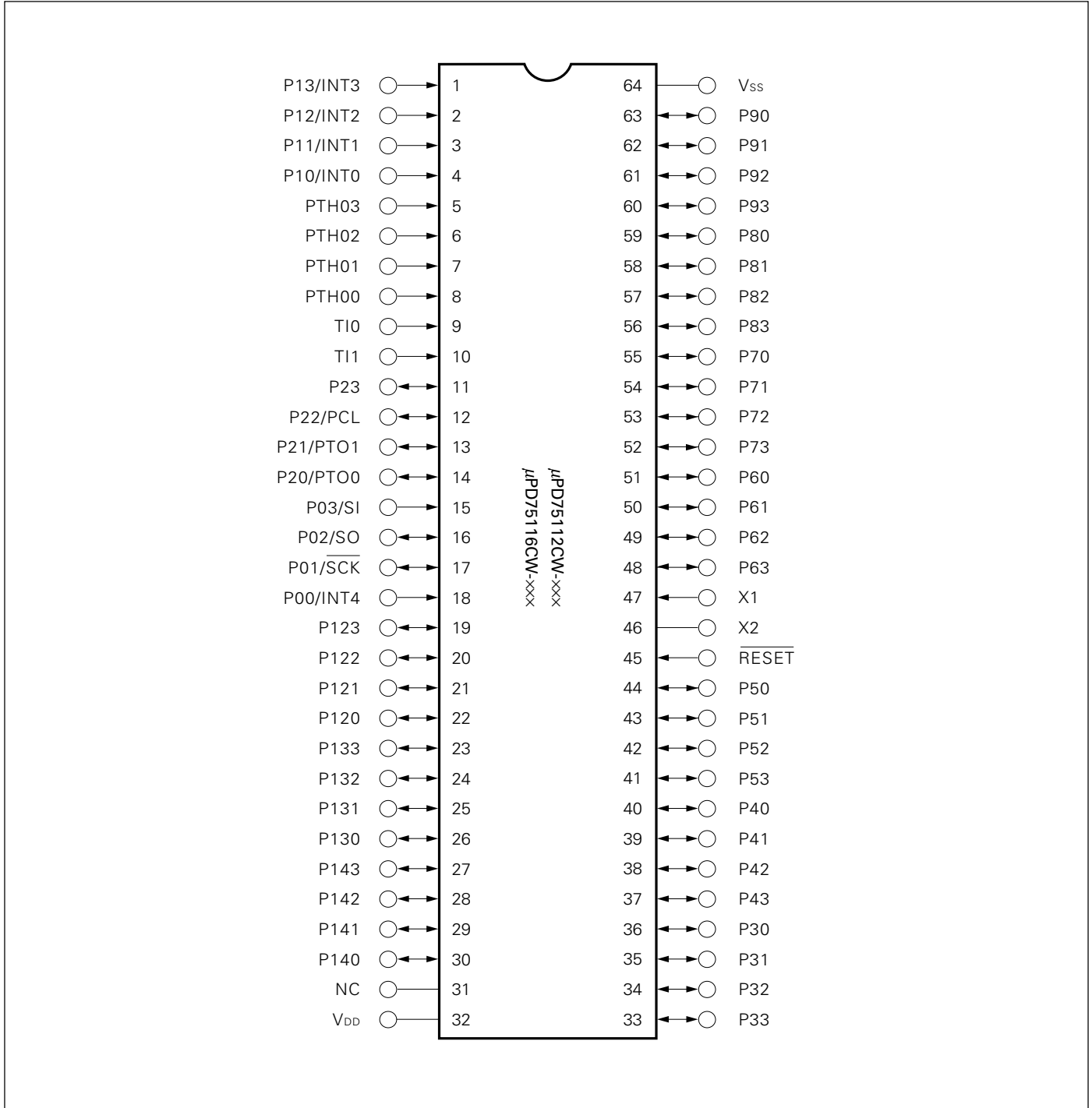
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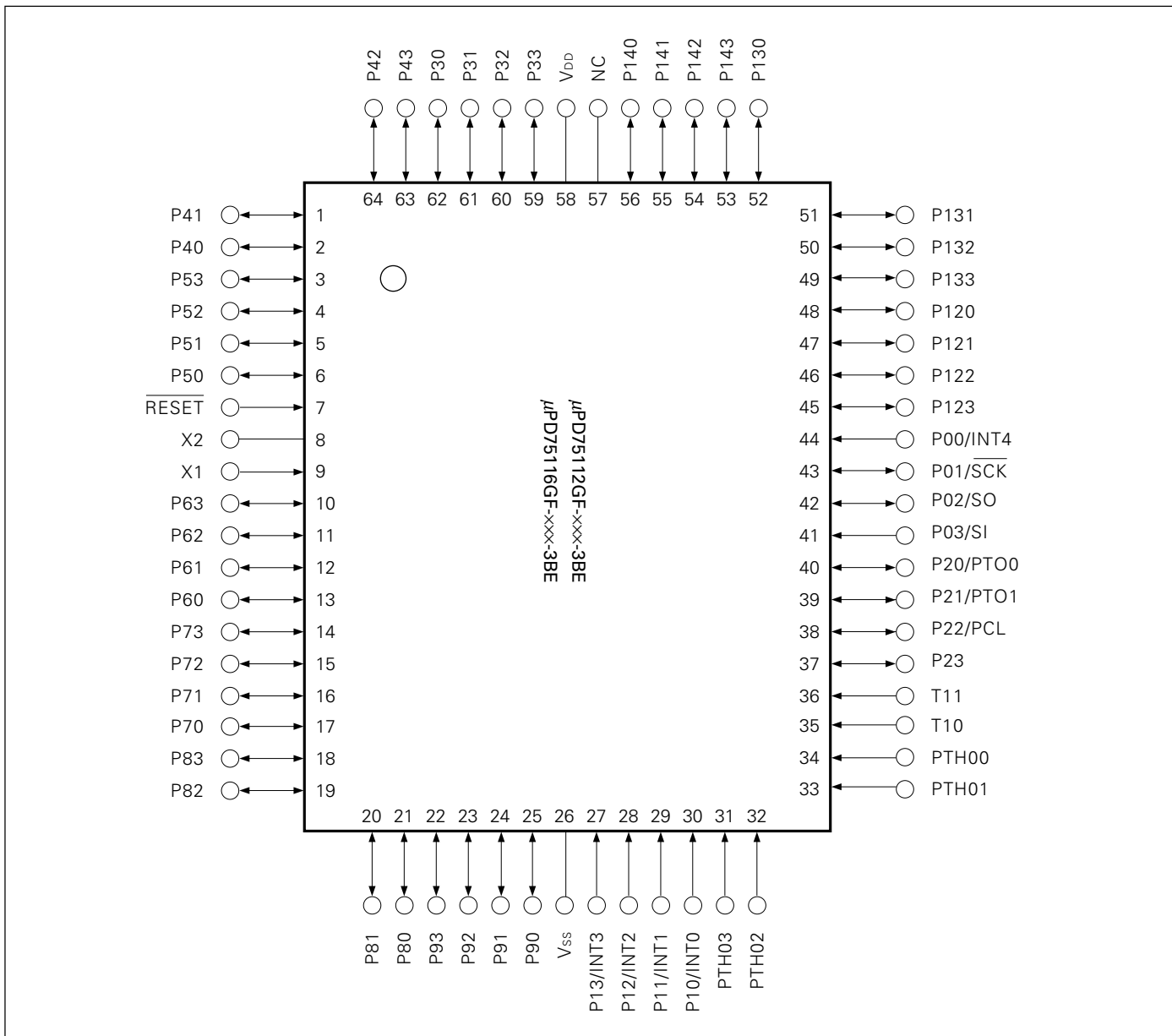
1. Pin Configuration (Top View)

64-Pin Plastic Shrink DIP (750 mil)



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64-Pin Plastic QFP (14 × 20 mm)



★

Pin Name

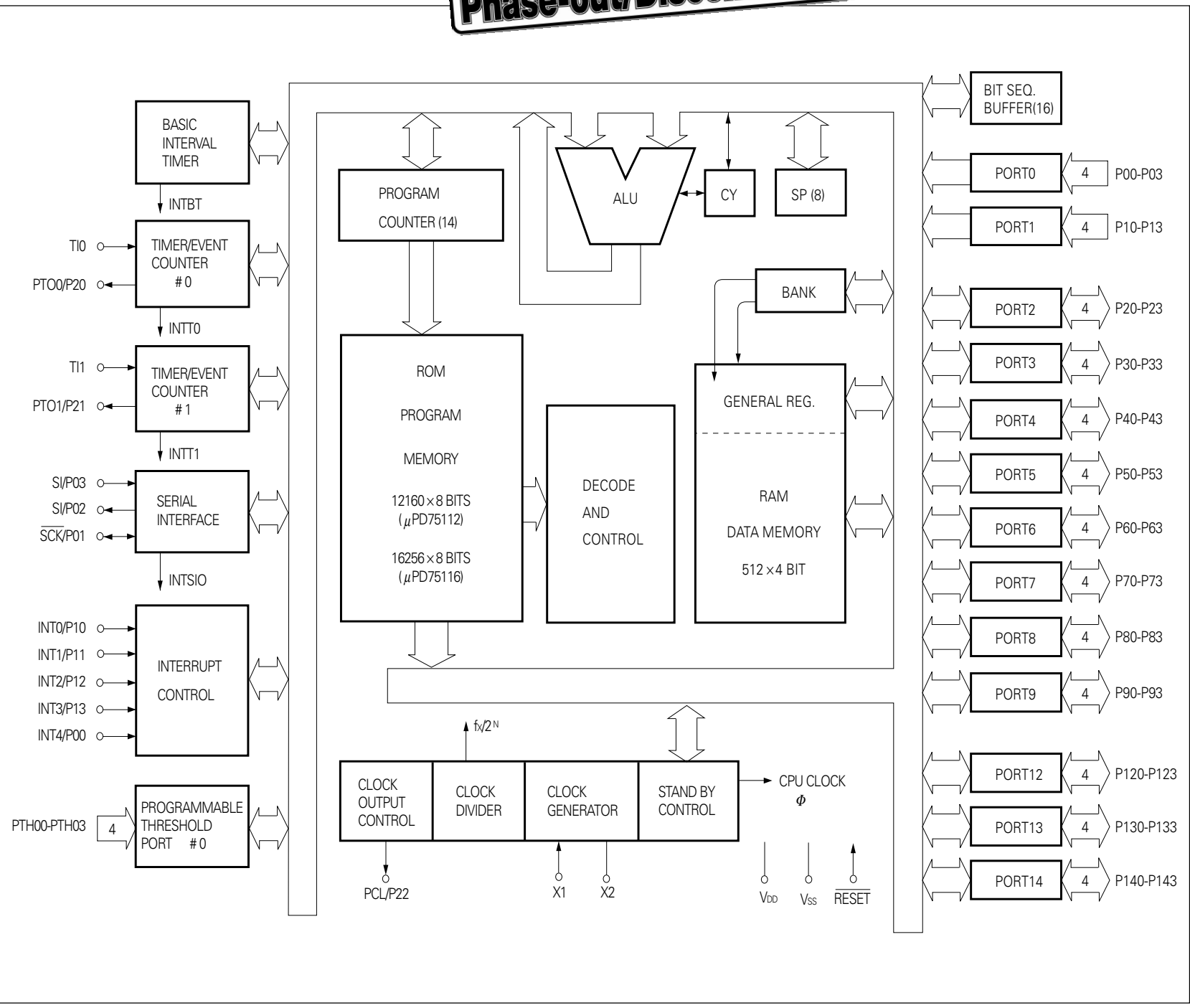
P00-P03	: Port0	SCK	: Serial Clock
P10-P13	: Port1	SO	: Serial Output
P20-P23	: Port2	SI	: Serial Input
P30-P33	: Port3	PTO0, PTO1	: Programmable Timer Output 0.1
P40-P43	: Port4	PCL	: Programmable Clock
P50-P53	: Port5	PTH00-PTH03	: Programmable Threshold Input
P60-P63	: Port6	INT0, INT1, INT4	: External Vectored Interrupt Input
P70-P73	: Port7	INT2, INT3	: External Test Input
P80-P83	: Port8	T10, T11	: Timer Input
P90-P93	: Port9	X1, X2	: Clock Oscillation
P120-P123	: Port12	RESET	: Reset
P130-P133	: Port13	NC	: No Connection
P140-P143	: Port14	V _{DD}	: Positive Power Supply
		V _{SS}	: Ground

Phase-out/Discontinued

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2. Block Diagram



3. Pin Functions

3.1 Port Pins

Pin Name	Input/ Output	Dual Function Pin	Function	8-Bit I/O	At Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT0)	×	Input	ⓑ
P01	Input/output	$\overline{\text{SCK}}$				ⓕ
P02	Input/output	SO				E
P03	Input	SI				ⓑ
P10	Input	INT0	4-bit input port (PORT1)		Input	ⓑ
P11		INT1				
P12		INT2				
P13		INT3				
P20 *3	Input/output	PTO0	4-bit input/output port (PORT2)	×	Input	E
P21 *3		PTO1				
P22 *3		PCL				
P23 *3		—				
P30 to P33 *3	Input/output	—	Programmable 4-bit input/output port (PORT3) Bit-wise input/output setting enable		Input	E
P40 to P43 *3	Input/output	—	4-bit input/output port (PORT4)	○	Input	E
P50 to P53 *3	Input/output	—	4-bit input/output port (PORT5)		Input	E
P60 to P63 *3	Input/output	—	Programmable 4-bit input/output port (PORT6) Bit-wise input/output setting enable	○	Input	E
P70 to P73 *3	Input/output	—	4-bit input/output port (PORT7)		Input	E
P80 to P83 *3	Input/output	—	4-bit input/output port (PORT8)	○	Input	E
P90 to P93 *3	Input/output	—	4-bit input/output port (PORT9)		Input	E
P120 to P123 *3	Input/output	—	N-ch open drain 4-bit input/ output port (PORT12) Bit-wise pull-up resistor incorporation enable (mask option) 2 V withstand for open drain	○	Input*2	M
P130 to P133 *3	Input/output	—	N-ch open drain 4-bit input/ output port (PORT13) Bit-wise pull-up resistor incorporation enable (mask option) 12 V withstand for open drain		Input*2	M
P140 to P143 *3	Input/output	—	N-ch open drain 4-bit input/output port (PORT14) Bit-wise pull-up resistor incorporation enable (mask option) 12 V withstand for open drain	—	Input*2	M

* 1: Circles indicate Schmitt trigger inputs.
2: High impedance for open drain

High level for on-chip pull-up resistors
3: LED direct drive is possible

3.2 Non-Port Pins

Pin Name	Input/Output	Dual Function Pin	Function	At Reset	I/O Circuit Type*1
PTH00 to PTH03	Input	——	Threshold voltage ariable 4-bit analogy input port.		N
TI0	Input	——	External event pulse input for the timer/event counter or edge detect vector interrupt input. 1-bit input enable.		Ⓑ
TI1					
PTO0	Input/output	P20	Timer/event counter output.	Input	E
PTO1		P21			
$\overline{\text{SCK}}$	Input/output	P01	Serial clock input/output.	Input	Ⓕ
SO	Input/output	P02	Serial data output.	Input	E
SI	Input	P03	Serial data input.	Input	Ⓑ
INT4	Input	P00	Edge detect vector interrupt input (for detecting both rising and falling edges).	Input	Ⓑ
INT0	Input	P10	Edge detect vector interrupt input (detected edge selectable).	Input	Ⓑ
INT1		P11			
INT2	Input	P12	Edge detect testable input (for rising edge detection).	Input	Ⓑ
INT3		P13			
PCL	Input/output	P22	Clock output.	Input	E
X1, X2		——	Crystal/ceramic connect pin (system clock oscillation). In case with the external clock, input a signal to X1 and the antiphase to X2.		
$\overline{\text{RESET}}$	Input	——	System reset input (low level active).		Ⓑ
NC*2	——	——	No Connection		
V _{DD}		——	Positive power supply.		
V _{SS}		——	GND potential.		

* 1: Circles indicate Schmitt trigger inputs.

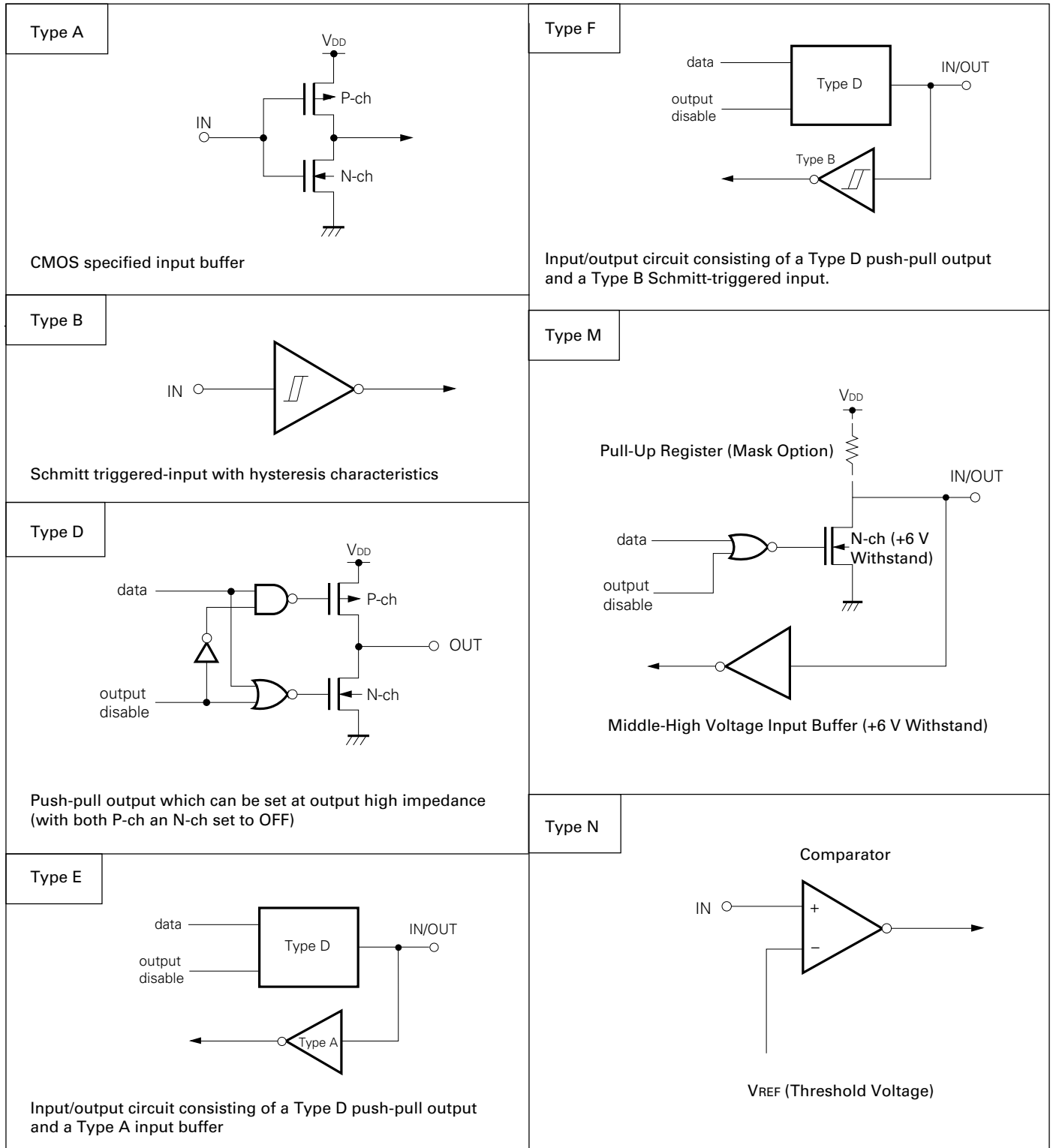
2: When the PWB is shared with the μPD75P116, connect the NC pin to V_{DD} directly.

μ PD75112, 75116

3.3 Pin Input/Output Circuits

μ PD75116 pin input/output circuit are shown in schematic form.

Figure 3-1 Pin Input/Output Circuits



3.4 Recommended Connection of Unused Pins

Pin	Recommended Connecting Method	
PTH00 to PTH03	Connect to Vss or VDD	
T10		
T11		
P00	Connect to Vss	
P01 to P03	Connect to Vss or VDD	
P10 to P13	Connect to Vss	
P20 to P23	Input state : Connect to Vss or VDD Output state : Leave open	
P30 to P33		
P40 to P43		
P50 to P53		
P60 to P63		
P70 to P73		
P80 to P83		
P90 to P93		
P120 to P123		
P130 to P133		
P140 to P143		
RESET		Connect to VDD*1
NC		Leave open or connect to VDD*2

*1: Only when a power-on reset generator is built in by mask option, connect to VDD.

*2: When the PWB is shared with the μPD75P116, connect the NC pin to VDD directly.

3.5 Caution Relating to Use of P00/INT4 Pin and RESET Pin

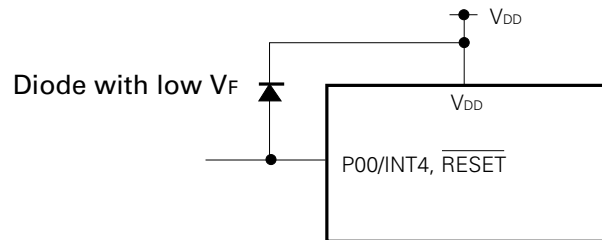
In addition to the functions described in sections 3.1 and 3.2, the P00/INT4 pin and the RESET pin have the function to set the IC test mode for testing the μPD75116 internal operations.

When a voltage larger than VDD is applied to one of these two pins, the test mode is set. Thus, if noise exceeding VDD is applied even during normal operations, the test mode is set and normal operations may be discontinued.

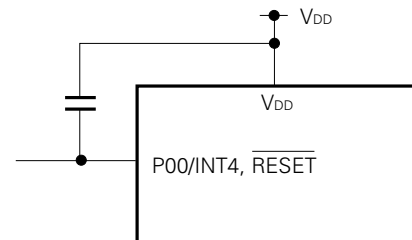
For example, if a cable from the P00/INT4 or RESET pin is too long, inter-wiring noise may be applied to the pin, the pin voltage may become larger than VDD, causing malfunctioning.

Thus, carry out wiring to minimize inter-wiring noise. If the noise cannot be suppressed completely, carry out the following countermeasure against noise using an externally mounted component.

- o Connect a diode with low V_F (max 0.3 V) between V_{DD}S



- o Connect a capacitor between V_{DD}S

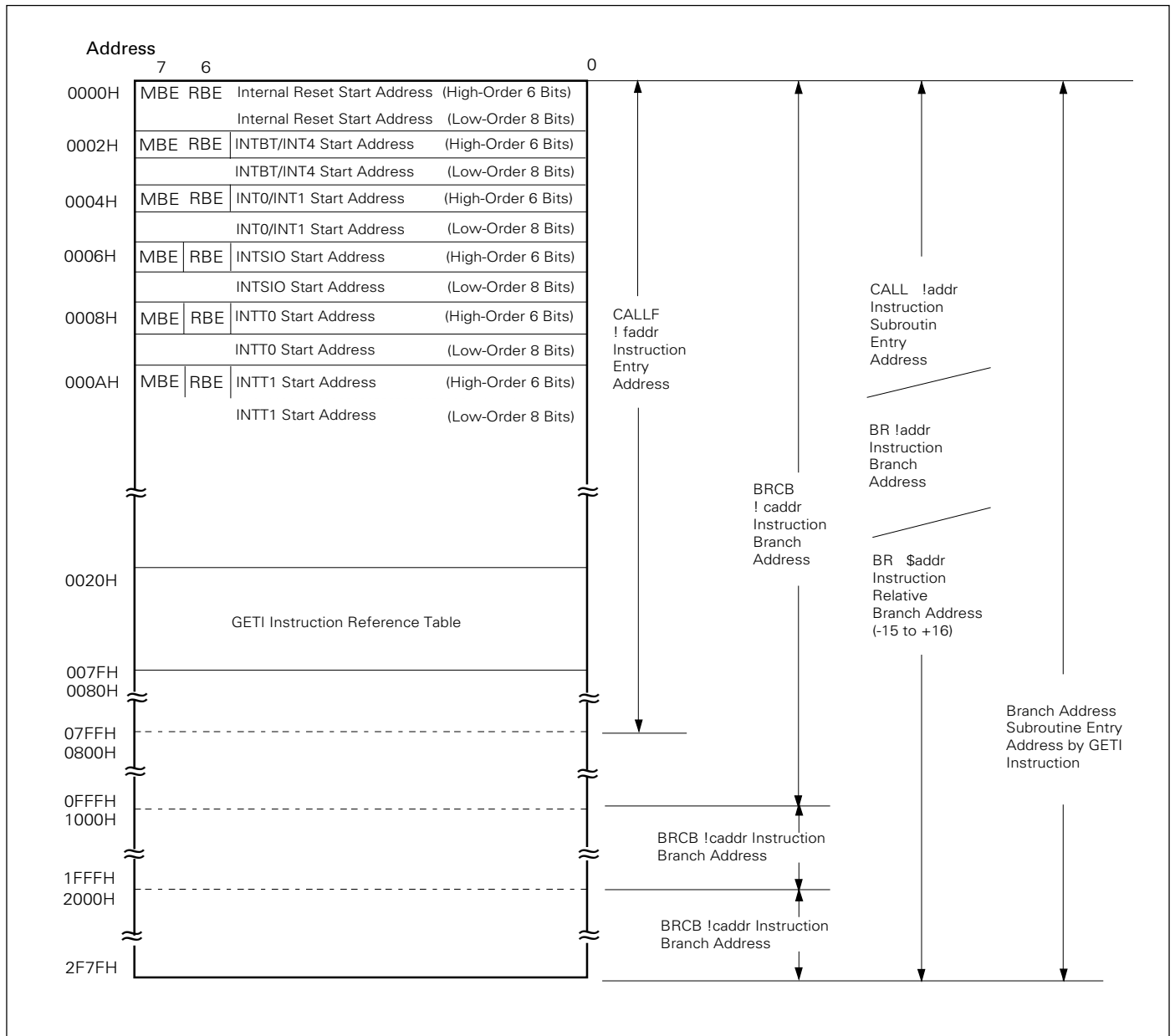


μPD75112, 75116

4. Memory Configuration

- Program Memory (ROM)
 - 12160 × 8 bits (0000H to 2F7FH): μPD75112
 - 16256 × 8 bits (0000H to 3F7FH): μPD75116
 - 0000H to 0001H: Vector table for writing the program start address by reset
 - 0002H to 000BH: Vector table for writing the program start address by interrupt
- 0020H to 007FH: Table area to be referred to by the GETI instruction
- Data Memory
 - Data area
512 × 4 bits (000H to 1FFH)
 - Peripheral hardware area
128 × 4 bits (F80H to FFFH)

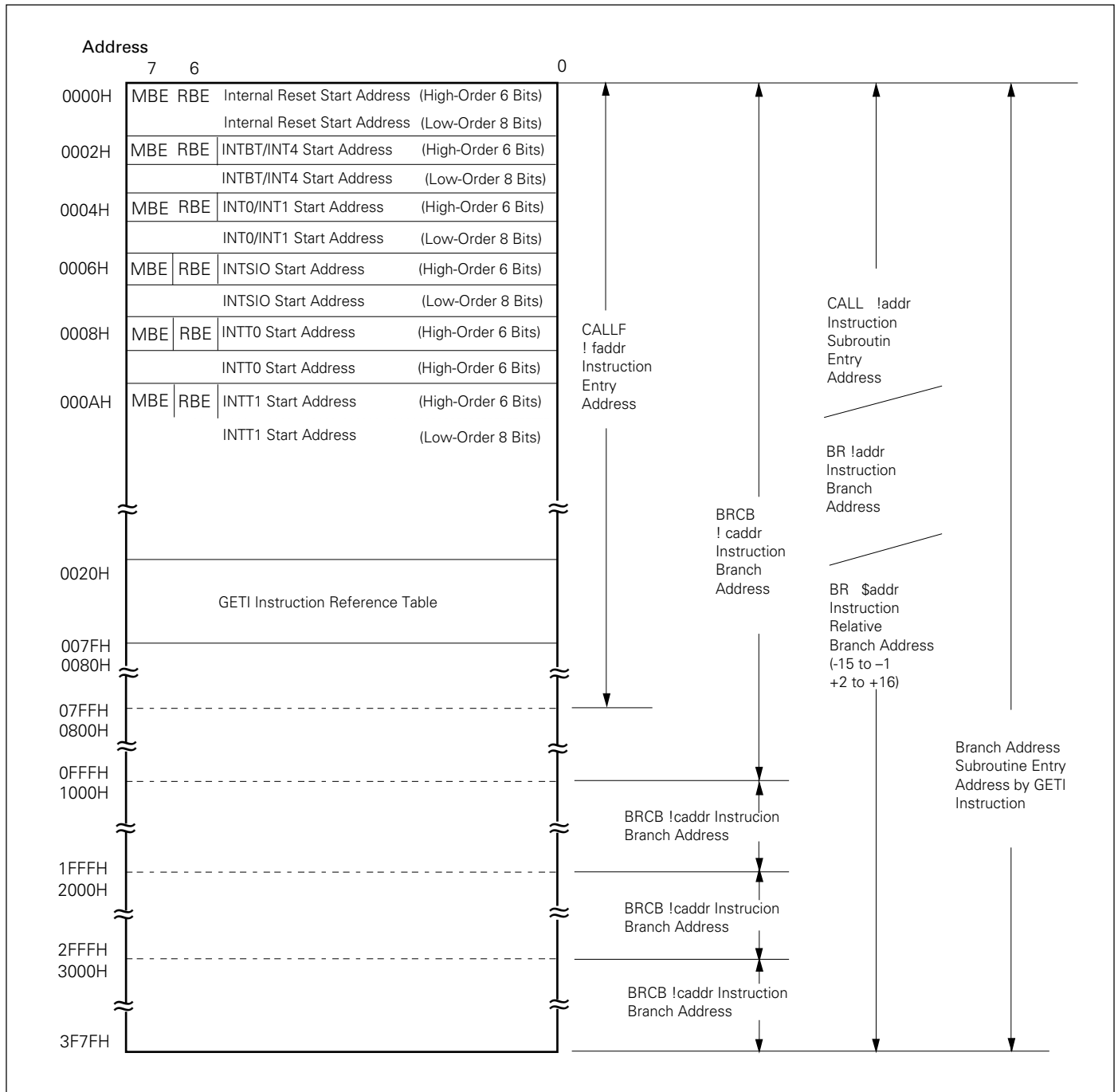
Figure 4-1 Program Memory Map (μPD75112)



Remarks: In all other cases, the program can be branched by the BR PCDE and BR PCXA

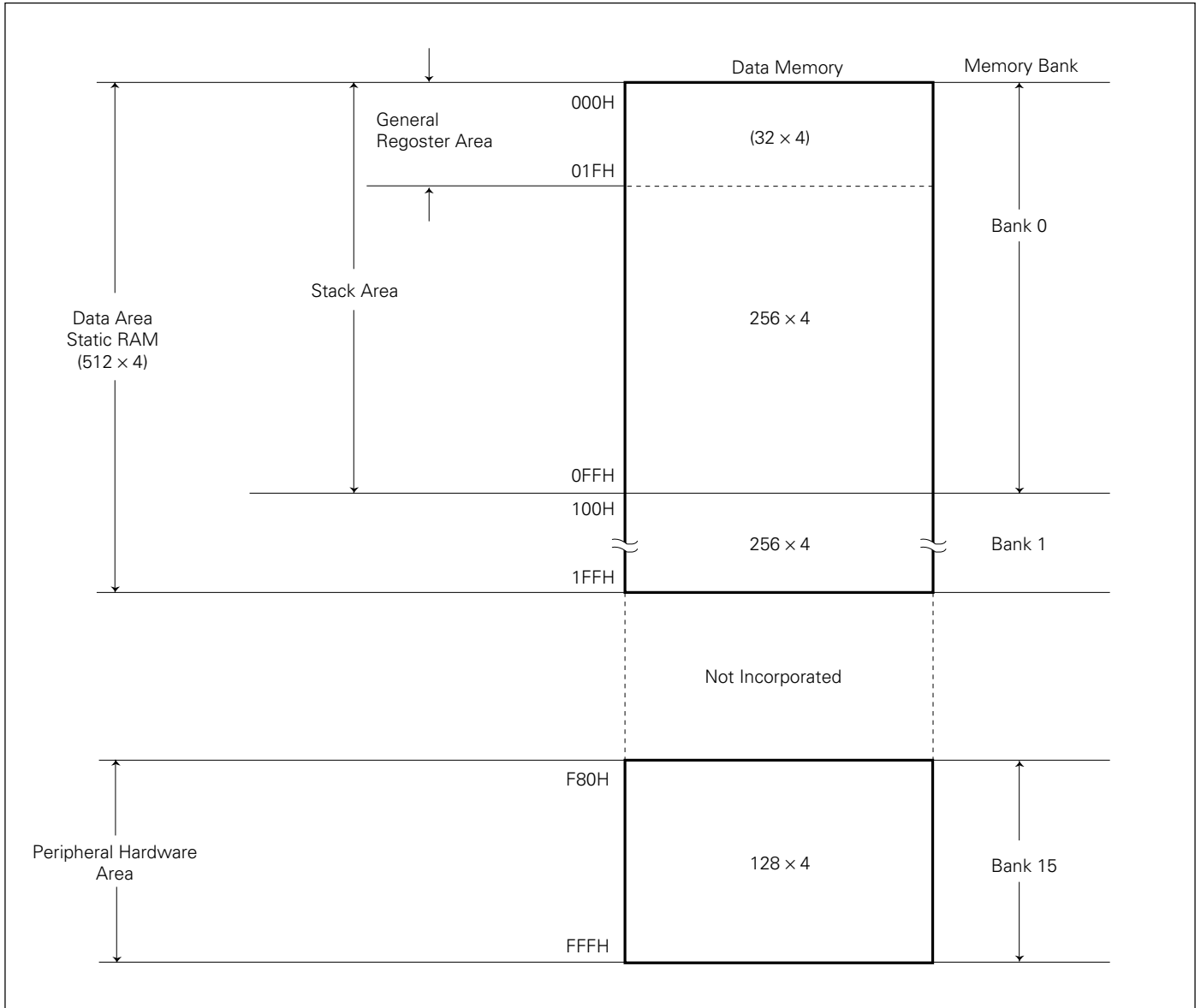
instructions to an address with only the lower 8 bits of PC changed.

Figure 4-2 Program Memory Map (μPD75116)



Remarks: In all other cases, the program can be branched by the BR PCDE and BR PCXA instructions to an address with only the lower 8 bits of PC changed.

Figure 4-3 Data Memory Map



5. Peripheral Hardware Functions

5.1 Digital Input/Output Port

The digital input/output port has the following tree types.

- CMOS input (PORT0, 1) : 8
 - CMOS input/output (PORT 2 to PORT 9) : 32
 - N-ch open-drain input/output (PORT 12 to PORT 14): 12
-
- Total 52

Table 5-1 Functions of Digital Ports

Port (Code)	Functions	Operations and Features	Remarks
PORT0 PORT1	4-bit input	Read or test always enable irrespectively of the operating mode of dual-function pins.	Share the pins with SI, SO, $\overline{\text{SCK}}$ and INT0 to 4.
PORT3 PORT6	4-bit input/ output*	Can be set bit-wise to the input or output mode.	
PORT2 PORT4 PORT5 PORT7 PORT8 PORT9		Can be set in 4-bit units to the input or output mode. Ports 4 and 5, 6 and 7, 8 and 9 can form pairs and data can be input/output in 8-bit units.	Port 2 shares the pin with PTO0, PTO1 and PCL.
PORT12 PORT13 PORT14	4-bit input/ output* (N-ch open-drain, 12 V withstand voltage)	Can be set in 4-bit units the input or output mode. Ports 12 and 13 can form a pair and data can be input/output in 8-bit units.	On-chip pull-up registers can be specified bit-wise by mask option.

*: Can directly drive LEDs.

5.2 Clock Generator

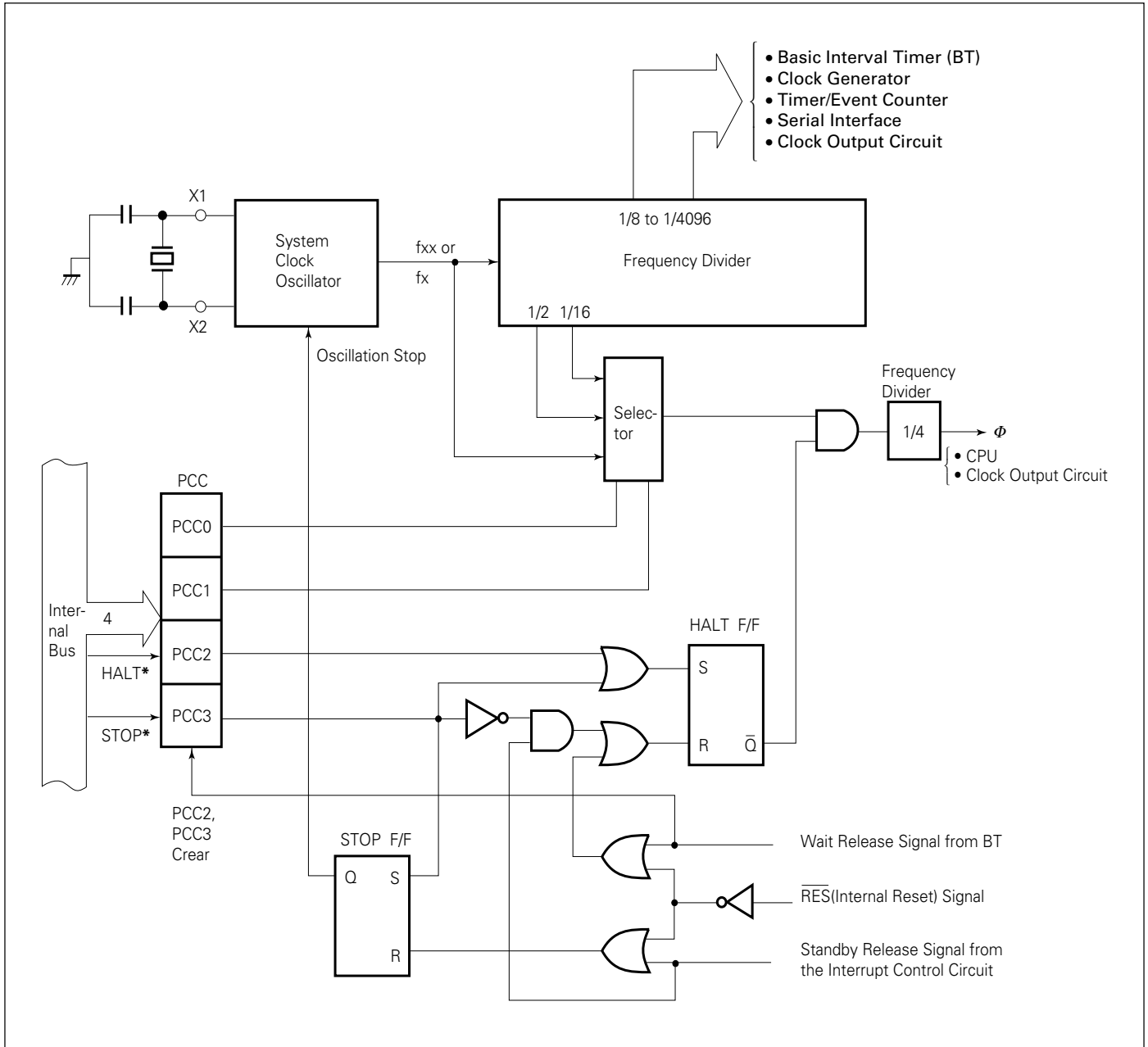
The clock generator is a circuit which supplies the CPU and peripheral hardware with various clocks and controls the CPU operating mode.

The instruction execution time can be changed.

- 0.95 μs/1.91 μs/15.3 μs (at 4.19 MHz operation)

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★ **Figure 5-1 Block Diagram of Clock Generator**



- Remarks 1:** fxx=crystal/ceramic oscillator frequency.
2: fx=external clock frequency.
3: Φ =CPU clock
4: *indicates instruction execution.
5: PCC (processor clock control register)
6: 1 clock cycle (tc_Y) of Φ is 1 machine cycle of the instruction. For tc_Y, see the AC characteristics in the 12. "Electrical Specifications".

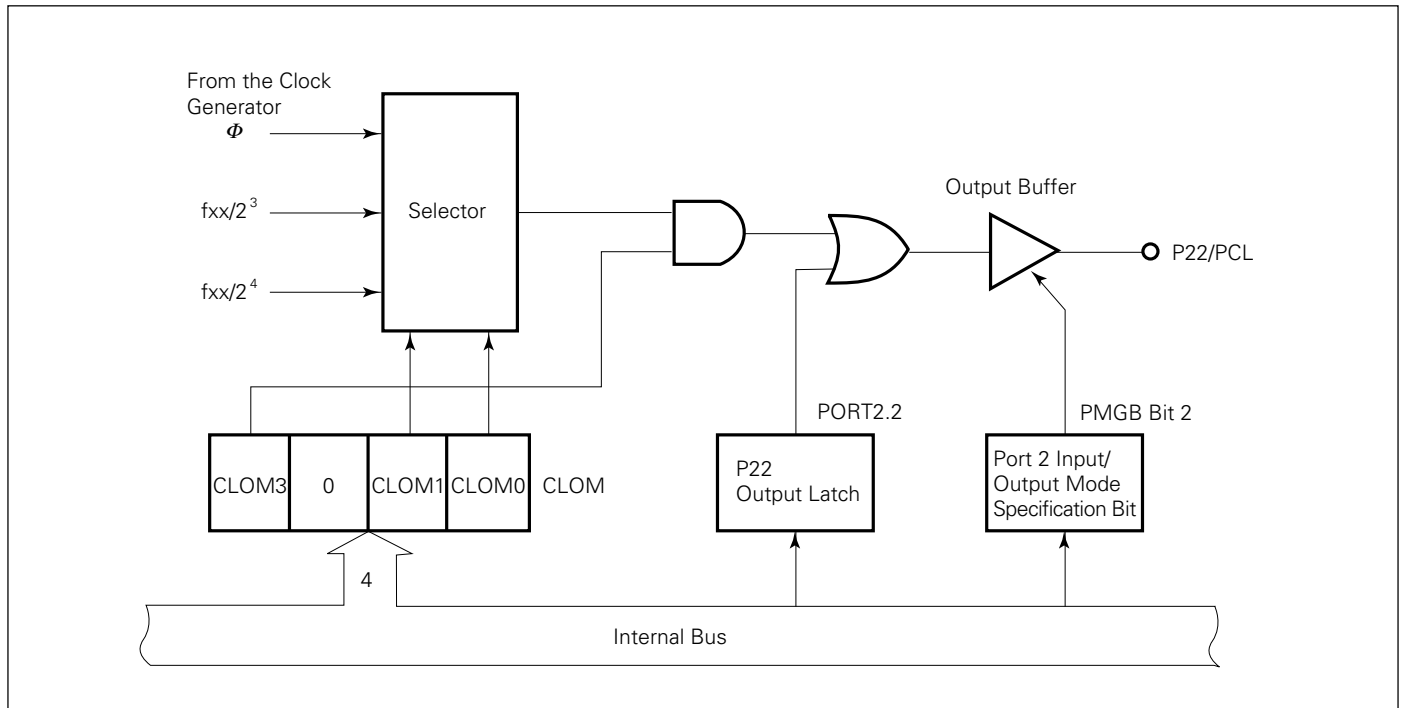
5.3 Clock Output Circuit

The clock output circuit is a circuit to generate clock pulses from the P22/PCL pin. It is used to supply the peripheral LSIs with clock pulses.

- Clock output (PCL): Φ , 524 kHz, 262 kHz (at 4.19 MHz operation)

The clock output circuit configuration is shown as the following.

Figure 5-2 Clock Output Circuit Configuration

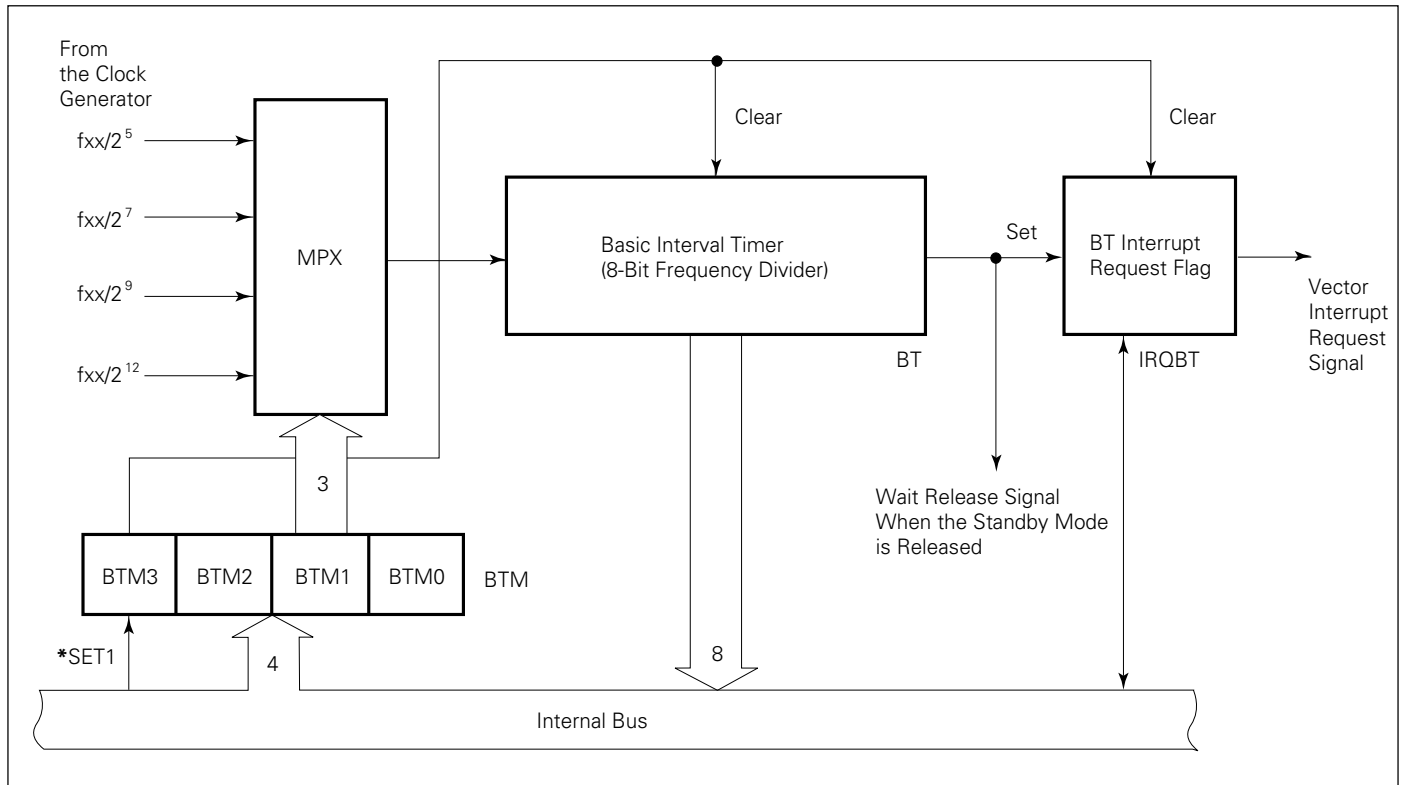


5.4 Basic Interval Timer

The basic interval timer has the following functions;

- Interval timer operation to generate reference time interrupts
- Watchdog timer application to detect program overrun
- Wait time selection and count when the standby mode is released
- Count content read

Figure 5-3 Basic Interval Timer Configuration



Remark: * indicates instruction execution.

5.5 Timer/Event Counter

The μ PD75116 has a two-channel on-chip timer/event counters.

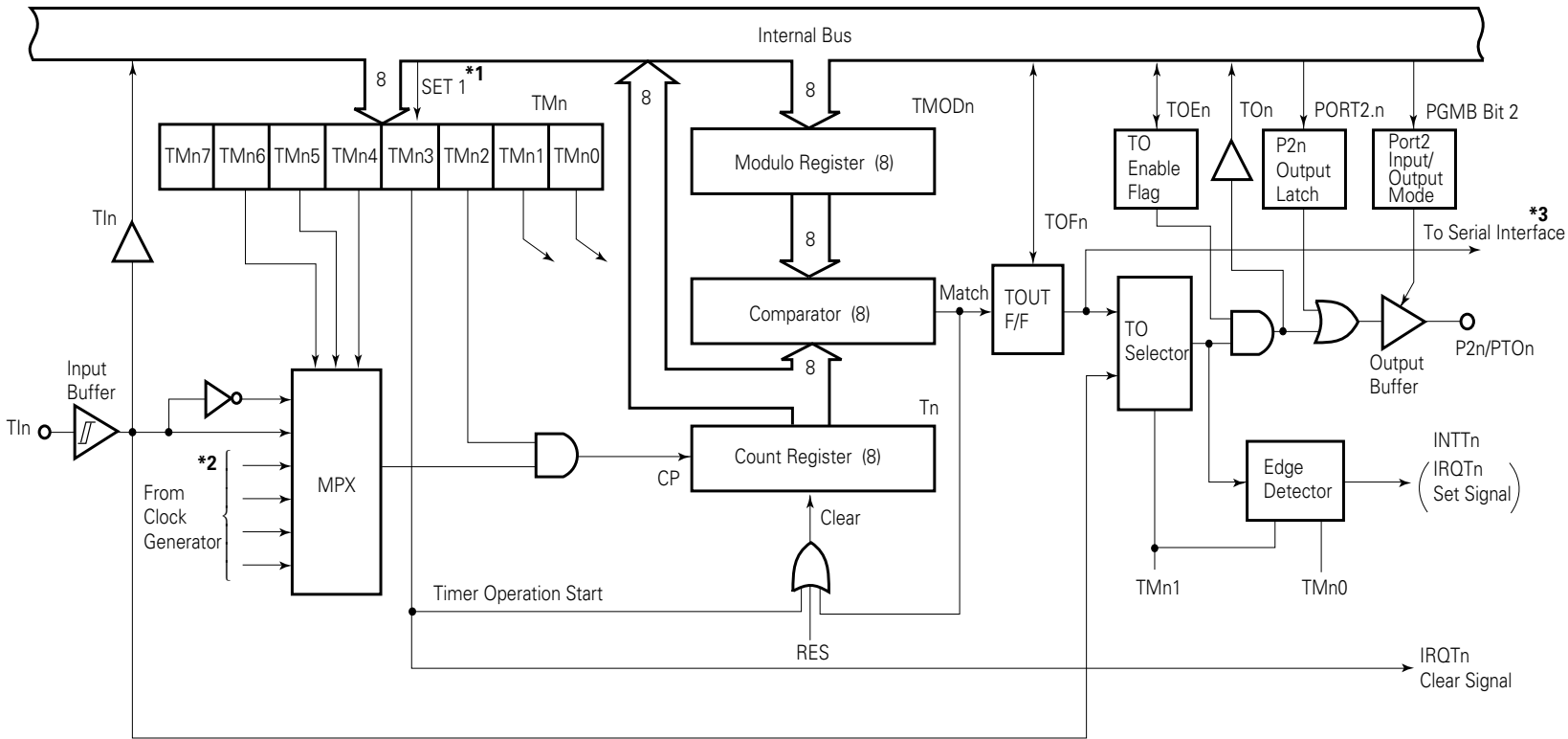
Channels 0 and 1 of the timer/event counter have the same configuration and functions. They differ only in the selectable count pulse (CP) and the function of supplying clocks to the serial interface.

The timer/event counter has the following functions:

- Programmable interval timer operation
- Output of square wave having any selected frequency to PTO_n pin
- Event counter operation
- Use of TIn pin as an external interrupt input pin
- Output of TIn pin input divided by N to PTO_n pin (frequency divider operation)
- Serial shift clock supply to the serial interface circuit (channel 0 only)
- Count status read function

Phase-out/Discontinued

Figure 5-4 Block Diagram of Timer/Event Counter (n=0, 1)



- * 1: SET1: Instruction execution
- * 2: Refer to Figure 5-1
- * 3: Only channel 0 of the time/event counter can output a signal to the serial interface

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5.6 Serial Interface

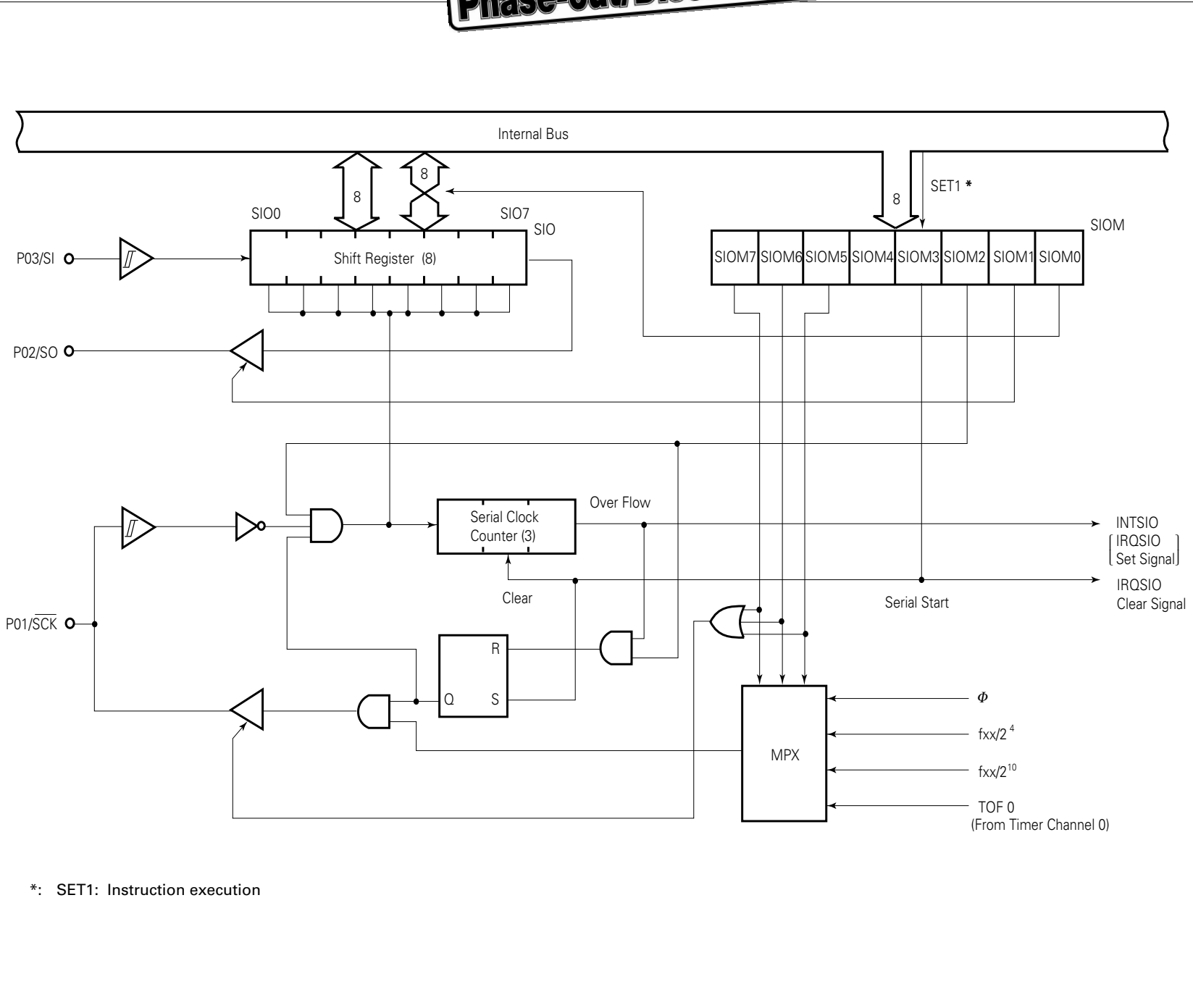
The μ PD75116 incorporates the clock synchronous 8-bit serial interface. The serial interface has the following two modes.

- Operation stop mode
- 3-wire serial I/O mode (MSB/LSB top switching possible)

Connection with the μ PD75116 and the 75X series, 78K series and various I/O devices is possible in the 3-wire serial I/O mode.

Phase-out/Discontinued

Figure 5-5 Block Diagram of Serial Interface



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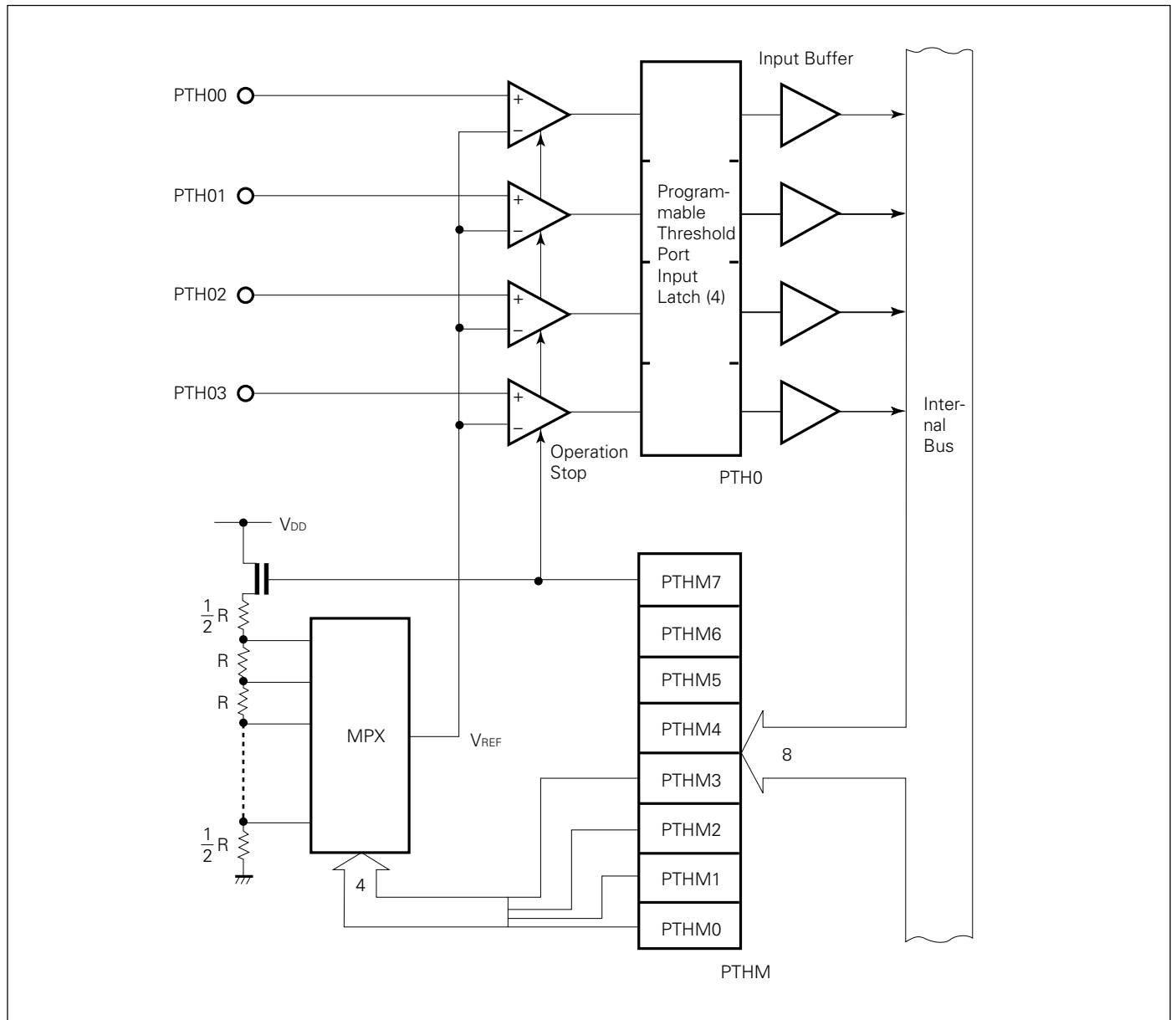
5.7 Programmable Threshold Port (Analog Input Port)

The μ PD75116 is equipped with 4-bit analog input pins (PTH00 to PTH03) capable of changing the threshold voltage. These pins are configured as shown in Figure 5-6.

Sixteen threshold voltage (V_{REF}) values ($V_{DD} \times \frac{0.5}{16} - V_{DD} \times \frac{15.5}{16}$) are available and analog signals can be directly input.

The analog input port can also be used as a digital signal input port by selecting $V_{DD} \times \frac{7.5}{16}$ for V_{REF} .

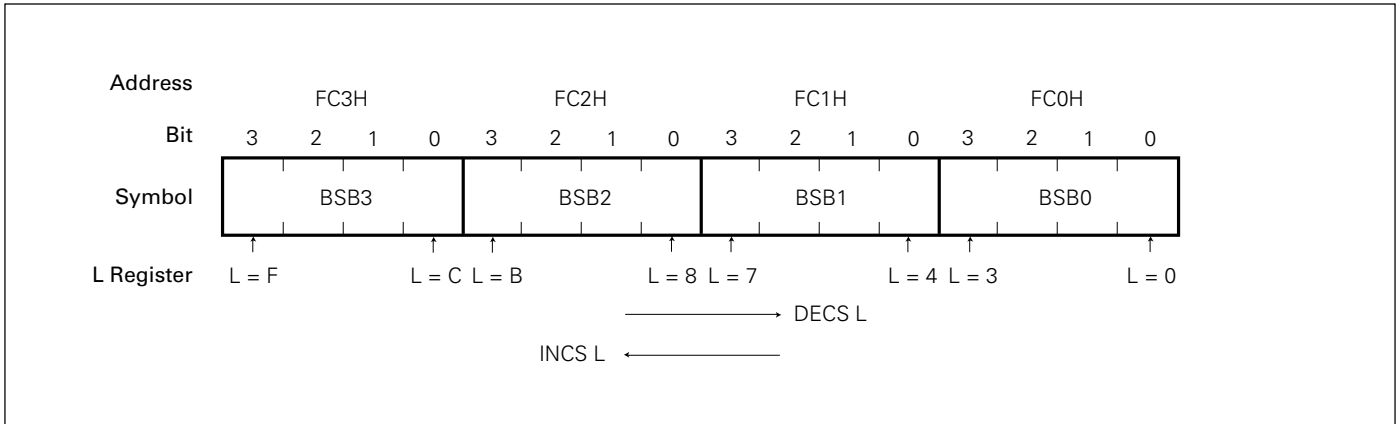
Figure 5-6 Block Diagram of Programmable Threshold Port



5.8 Bit Sequential Buffer ... 16 bit

The bit sequential buffer is a special data memory for bit control. Since this buffer can easily operate bits by sequentially changing address and bit specifications, it can be conveniently be used for bit-wise processing of data having long bit lengths.

Figure 5-7 Bit Sequential Buffer Format



Remarks: In pmen. @L addressing, the specified bit moves in accordance with the L register.

5.9 Power-On Flag (Mask Option)

The power-on flag (PONF) is only set (1) when the power-on reset circuit is activated and the power-on reset signal is generated (see **Figure 8-1**).

PONF is mapped on bit 0 at address FD1H of the data memory space and is manipulated by a bit manipulation instruction.

However, it cannot be set (1) by the SET1 instruction.

6. Interrupt Functions

There are seven types of interrupt sources for the μ PD75116 to allow multi-interruption with priority.

The μ PD75116 is also provided with two types of edge detection testable inputs.

The μ PD75116 interrupt control circuit has the following functions;

- Hardware controlled vector interrupt function which enables to control by the interrupt enable flag (IE_{xxx}) and the interrupt master enable flag (IME) whether an interrupt should be enabled.
- Interrupt start address can be set freely.
- Multiple interrupt function which enables to specify priority by the interrupt priority select register (IPS).
- Interrupt request flag (IRQ_{xxx}) test function (interrupt generation can be checked by the software).
- Standby mode release (the interrupt to be released can be selected by the interrupt enable flag).

Phase-out/Discontinued

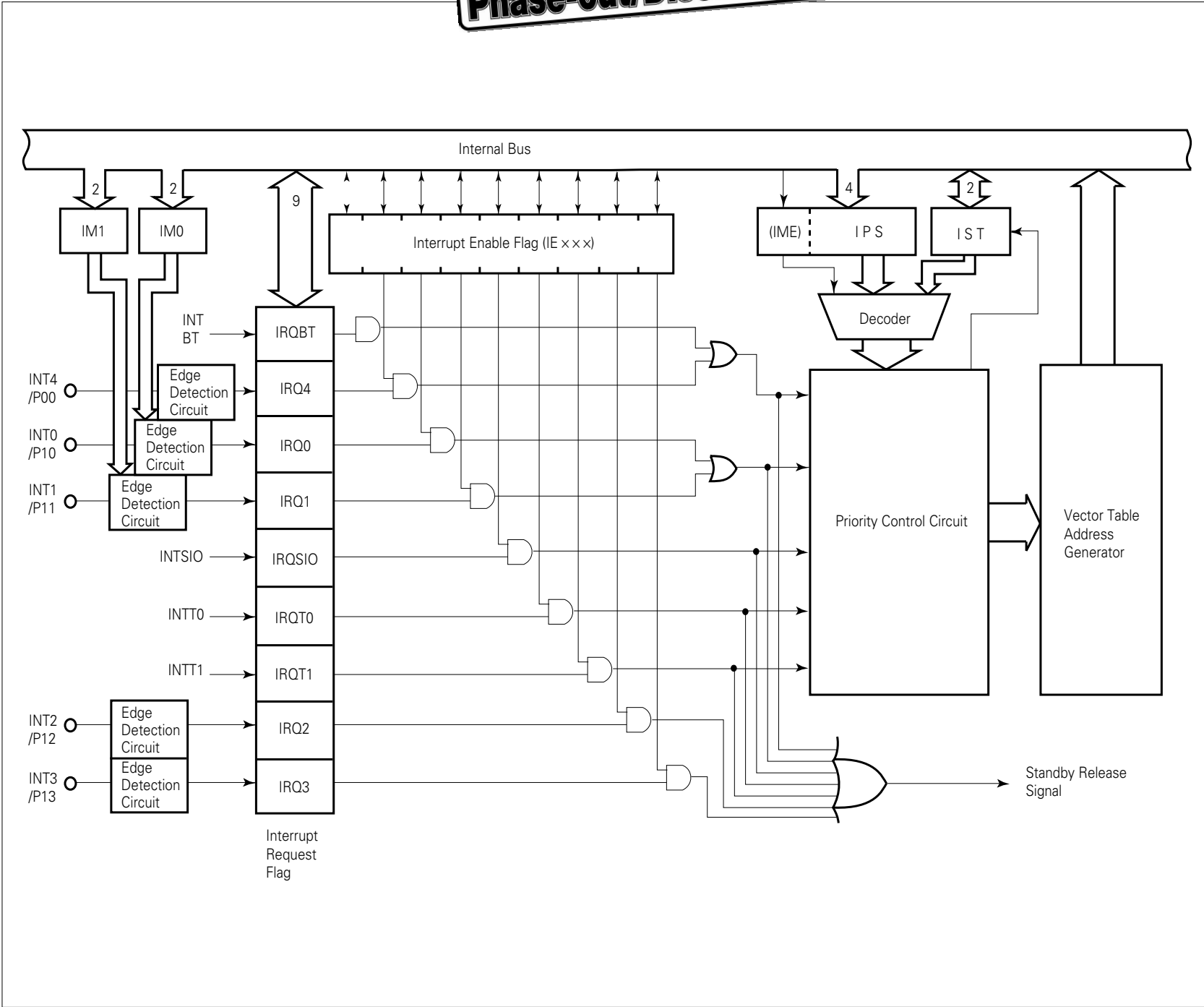


Figure 6-1 Block Diagram of Interrupt Control Circuit

7. Standby Functions

Two types of standby modes (STOP and HALT modes) are available for the μ PD75116 to decrease power consumption during standby for program.

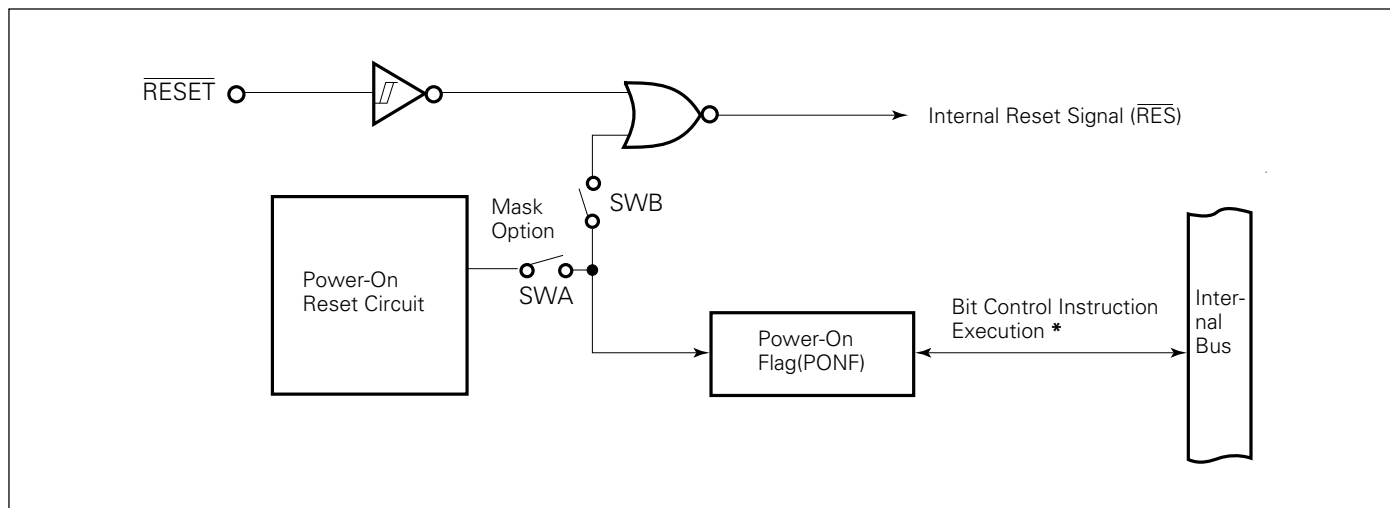
Table 7-1 Operation Statuses in Standby Mode

		STOP Mode	HALT Mode
Set instruction		STOP instruction	HALT instruction
Operation status	Clock generator	Clock oscillation stop	Only CPU clock ϕ stop
	Basic interval timer	Operation stop	Operation (IRQBT set at reference time intervals)
	Serial interface	Operation enabled only when external \overline{SCK} input and TO0 clock are set for serial clocks (when timer/event counter 0 is set to external TIO input) is selected	Operation enabled when a clock other than ϕ is specified for the serial clock
	Timer/event counter	Operation enabled only when TIn pin input is specified for the count clock	Operation enabled
	Clock output circuit	Operation stop	Clock other than CPU clock ϕ enabled for output
	CPU	Operation stop	Operation stop
Release signal		Interrupt request signal enabled by interrupt enable flag or \overline{RESET} input	

8. Reset Functions

The reset signal ($\overline{\text{RES}}$) generator is configured as shown in Figure 8-1.

Figure 8-1 Reset Signal Generator



* PONF setting (1) by SET1 instruction is not possible.

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The power-on reset circuit generates the internal reset signal by rising of supply voltage. This pulse is used in the three ways according to the specification of mask option of SWA and SWB shown in Figure 8-1 (refer to "11. Mask Option Selection").

Reset operations are shown in Figures 8-2 and 8-3.

Figure 8-2 Reset Operation by Power-on Reset

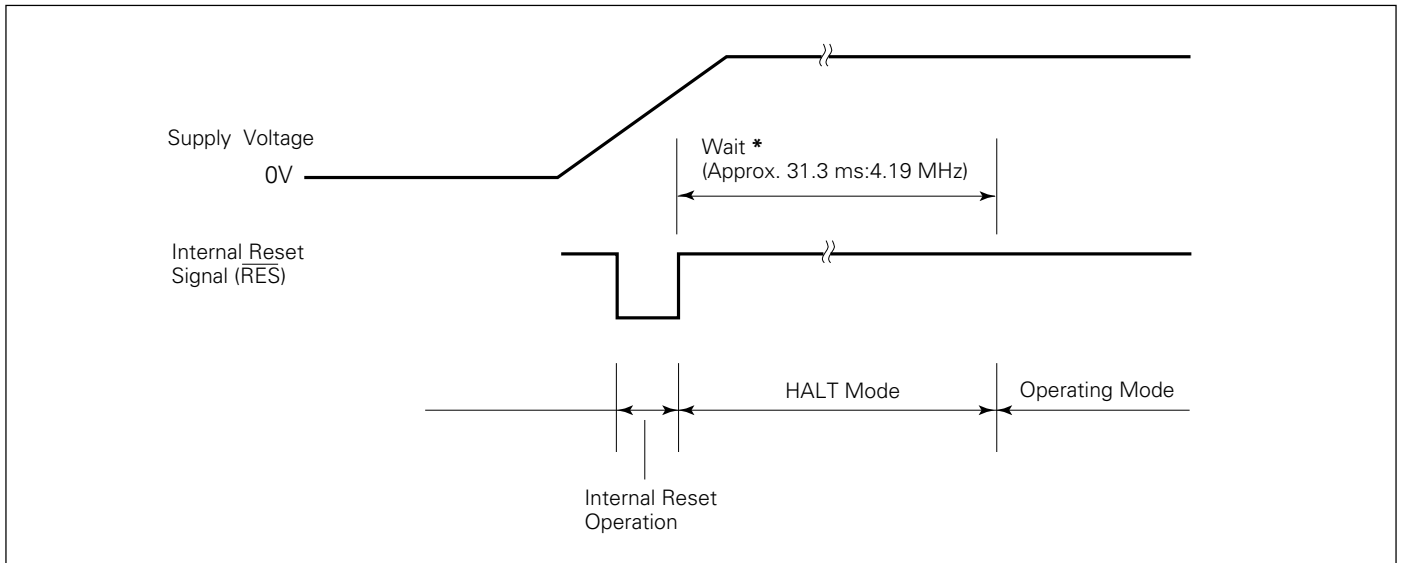
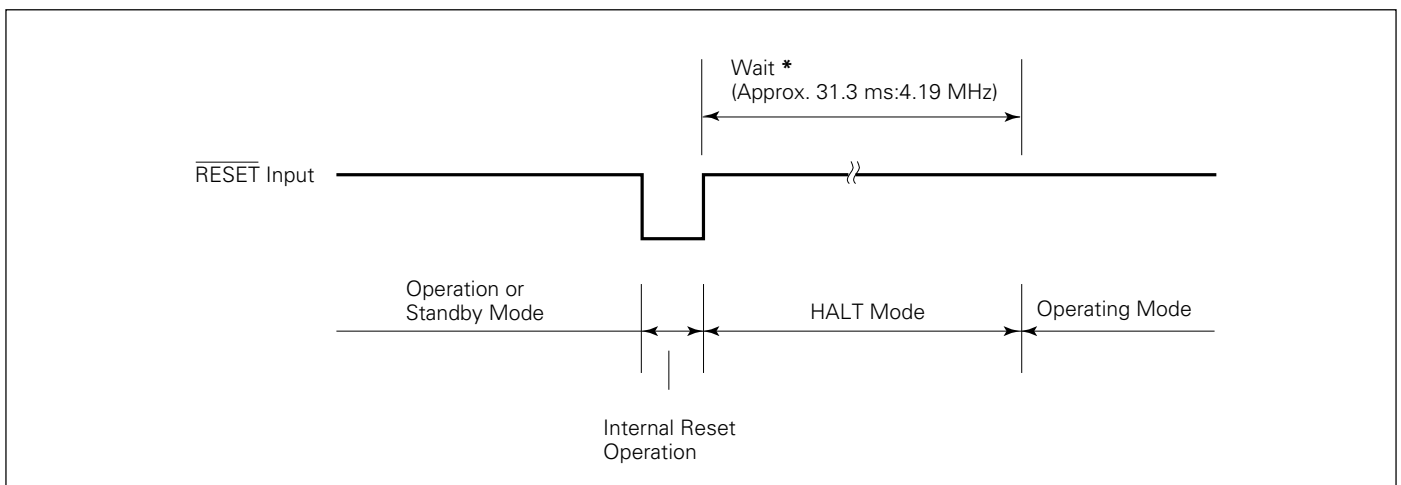


Figure 8-3 Reset Operation by $\overline{\text{Reset}}$ Input



* The wait time does not include a time from the generation of $\overline{\text{RES}}$ signal to the start of oscillation.

Each hardware status after reset operation is shown in Table 8-1.

Table 8-1 Hardware Statuses after Reset

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input in Power-On Reset or Operation
Program counter (PC)		Lower 6 bits of address 0000H of the program memory are set to PC13 to PC8 and the content of address 0001H is set to PC7 to PC0.	same as left
PWS	Carry flag (CY)	Hold	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0, 1)	0	0
	Bank enable flags (MBE, RBE)	Bits 6 and 7 of address 0000H of the program memory are set to RBE and MBE, respectively.	same as left
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Hold *1	Undefined
General registers (X, A, H, L, D, E, B, C)		Hold	Undefined
Bank select registers (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/ event counter (n = 0, 1)	Counter (Tn)	0	0
	Modulo register (TMODn)	FFH	FFH
	Mode register (TMn)	0	0
	TOEn, TOFn	0, 0	0, 0
Serial interface	Shift register (SIO)	Hold	Undefined
	Mode register (SIOM)	0	0
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	Clock output mode register (CLOM)	0	0
Interrupt	Interrupt request flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt enable flag (IExxx)	0	0
	Priority select register (IPS)	0	0
	INT0, 1 mode registers (IM0, IM1)	0, 0	0, 0
Digital port	Output buffer	Off	Off
	Output latch	Clear (0)	Clear (0)
	Input/output mode registers (PMGA, PMGB, PMGC)	0	0
Analog port	PTH00 to PTH03 input latches	Undefined	Undefined
	Mode register (PTHM)	0	0
Power-on flag (PONF)		Hold	1 or undefined *2
Bit sequential buffers (BSB0 to BSB3)		0	0

* 1: Power-on reset 1
 $\overline{\text{RESET}}$ input in operation ... Undefined

2: Data at addresses 0F8H to 0FDH of the data memory becomes undefined due to $\overline{\text{RESET}}$ input.

9. Instruction Set

(1) Operand identifier and description method

In the operand column of each instruction, describe the corresponding operand in accordance with the description method for the operand identifier of the instruction (refer to the "**RA75X Assembler Package User's Manual Language Volume**" (EEU-730) for details). If more than one description method is available, select one of them. Capital alphabetic letters, plus and minus signs are key words. Describe them as they are.

In the case of immediate data, describe appropriate numeric values or labels.

Symbols of various registers and flags can be described as labels instead of mem, fmem, pmem, bit, etc. (Refer to the "**μPD751xx Series User's Manual (IEM-922)**" for details). Labels which can be described are limited for fmem and pmem.

Identifier	Description Method	
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'	
rpa rpa1	HL, HL+, HL-, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem bit	8-bit immediate data or label* 2-bit immediate data or label	
fmem pmem	FB0H to FBFH and FF0H to FFFH immediate data or labels FC0H to FFFH immediate data or labels	
addr	μPD75112	0000H to 2F7FH immediate data or labels
	μPD75116	0000H to 3F7FH immediate data or labels
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (bit = 0) or labels	
PORTn IExxx RBn MBn	PORT0 to PORT9, PORT12 to PORT14 IEBT, IESIO, IET0, IET1, IE0 to IE4 RB0 to RB3 MB0, MB1, MB15	

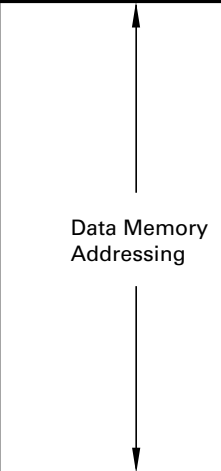
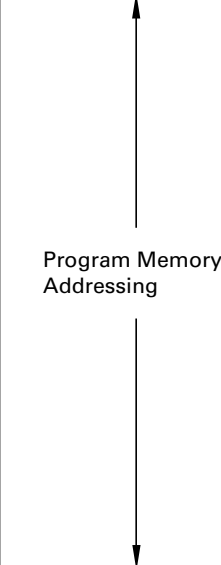
*: In the case of 8-bit data processing, only even address can be described for "mem".

(2) Legend in the description of operations

A	:	A register; 4-bit accumulator
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
X	:	X register
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
XA'	:	Extended register pair (XA')
BC'	:	Extended register pair (BC')
DE'	:	Extended register pair (DE')
HL'	:	Extended register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORT _n	:	Port n (n = 0 to 9, 12 to 14)
IME	:	Interrupt mask enable flag
IPS	:	Interrupt priority select register
IE _{xxx}	:	Interrupt enable flag
RBS	:	Register bank select register
MBS	:	Memory bank select register
PCC	:	Processor clock control register
.	:	Address and bit division
(xx)	:	Content addressed by xx
xxH	:	Hexadecimal data

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(3) Description of symbols in the addressing area column

*1	MB=MBE•MBS (MBS=0, 1, 15)	
*2	MB=0	
*3	MBE=0 : MB=0 (00H-7FH) MB=15 (80H-FFH) MBE=1 : MB=MBS (MBS=0, 1, 15)	
*4	MB=15, fmem=FB0H-FBFH, FF0H-FFFH	
*5	MB=15, pmem=FC0H-FFFH	
*6	addr=0000H-2F7FH (μ PD75112) =0000H-3F7FH (μ PD75116)	
*7	addr=(Current PC) -15 to (Current PC) +16	
*8	caddr=0000H-0FFFH (PC ₁₃ , PC ₁₂ =00B : μ PD75112, 116) or =1000H-1FFFH (PC ₁₃ , PC ₁₂ =01B : μ PD75112, 116) or =2000H-2F7FH (PC ₁₃ , PC ₁₂ =10B : μ PD75112) or =2000H-2FFFH (PC ₁₃ , PC ₁₂ =10B : μ PD75116) or =3000H-3F7FH (PC ₁₃ , PC ₁₂ =11B : μ PD75116)	
*9	faddr=0000H-07FFH	
*10	taddr=0020H-007FH	

- Remarks**
- 1: MB indicates an accessible memory bank.
 - 2: In *2, MB = 0 irrespectively of MBE and MBS.
 - 3: In *4 and *5, MB = 15 irrespectively of MBE and MBS.
 - 4: *6 to *10 indicate addressable areas.

One machine cycle is equal to one cycle (=tcy)of CPU clock. Three values are available for the one machine cycle by PCC setting.

(4) Description of machine cycle column

S indicates the number of machine cycles required for the instruction having skip function to execute skip operation. The value of S varies as follows:

- When no skip S = 0
- When 1-byte or 2-byte instruction is skipped S = 1
- When 3-byte instruction (BR !addr, CALL !addr instructions) is skipped S = 2

Note: GETI instruction is skipped in one-machine cycle.

Instruction	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A←n4		Stack A
		reg1, #n4	2	2	reg1←n4		
		XA, #n8	2	2	XA←n8		Stack A
		HL, #n8	2	2	HL←n8		Stack B
		rp2, #n8	2	2	rp2←n8		
		A, @HL	1	1	A←(HL)	*1	
		A, @HL+	1	2+S	A←(HL), then L←L+1	*1	L=0
		A, @HL-	1	2+S	A←(HL), then L←L-1	*1	L=FH
		A, @rpa1	1	1	A←(rpa1)	*2	
		XA, @HL	2	2	XA←(HL)	*1	
		@HL, A	1	1	(HL)←A	*1	
		@HL, XA	2	2	(HL)←XA	*1	
		A, mem	2	2	A←(mem)	*3	
		XA, mem	2	2	XA←(mem)	*3	
		mem, A	2	2	(mem)←A	*3	
		mem, XA	2	2	(mem)←XA	*3	
		A, reg	2	2	A←reg		
		XA, rp'	2	2	XA←rp'		
		reg1, A	2	2	reg1←A		
		rp'1 XA	2	2	rp'1←XA		
	XCH	A, @HL	1	1	A↔(HL)	*1	
		A, @HL+	1	2+S	A↔(HL), then L←L+1	*1	L=0
		A, @HL-	1	2+S	A↔(HL), then L←L-1	*1	L=FH
		A, @rpa1	1	1	A↔(rpa1)	*2	
		XA, @HL	2	2	XA↔(HL)	*1	
		A, mem	2	2	A↔(mem)	*3	
		XA, mem	2	2	XA↔(mem)	*3	
		A, reg1	1	1	A↔reg1		
		XA, rp'	2	2	XA↔rp'		
	Table Reference	MOVT	XA, @PCDE	1	3	XA←(PC13-8+DE) _{ROM}	
XA, @PCXA			1	3	XA←(PC13-8+XA) _{ROM}		
Bit Transfer	MOV1	CY, fmem. bit	2	2	CY←(fmem.bit)	*4	
		CY, pmem. @L	2	2	CY←(pmem7-2+L3-2.bit(L1-0))	*5	
		CY, @H+mem. bit	2	2	CY←(H+mem3-0.bit)	*1	
		fmem. bit, CY	2	2	(fmem.bit)←CY	*4	
		pmem. @L, CY	2	2	(pmem7-2+L3-2.bit(L1-0))←CY	*5	
		@H+mem. bit, CY	2	2	(H+mem3-0.bit)←CY	*1	

Instruction	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Arithmetic	ADDS	A, #n4	1	1+S	$A \leftarrow A+n4$		Carry
		XA, #n8	2	2+S	$XA \leftarrow XA+n8$		Carry
		A, @HL	1	1+S	$A \leftarrow A+(HL)$	*1	Carry
		XA, rp'	2	2+S	$XA \leftarrow XA+rp'$		Carry
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1+XA$		Carry
	ADDC	A, @HL	1	1	$A, CY \leftarrow A+(HL)+CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA+rp'+CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1+XA+CY$		
	SUBS	A, @HL	1	1+S	$A \leftarrow A-(HL)$	*1	borrow
		XA, rp'	2	2+S	$XA \leftarrow XA-rp'$		borrow
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1-XA$		borrow
	SUBC	A, @HL	1	1	$A, CY \leftarrow A-(HL)-CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA-rp'-CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1-XA-CY$		
	AND	A, #n4	2	2	$A \leftarrow A \wedge n4$		
		A, @HL	1	1	$A \leftarrow A \wedge (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \wedge rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \wedge XA$		
	OR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \vee rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$		
	XOR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
XA, rp'		2	2	$XA \leftarrow XA \vee rp'$			
rp'1, XA		2	2	$rp'1 \leftarrow rp'1 \vee XA$			
Accumulator Operation	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \bar{A}$		
Increase/Decrease	INCS	reg	1	1+S	$reg \leftarrow reg+1$		reg=0
		rp1	1	1+S	$rp1 \leftarrow rp1+1$		rp1=00H
		@HL	2	2+S	$(HL) \leftarrow (HL)+1$	*1	(HL)=0
		mem	2	2+S	$(mem) \leftarrow (mem)+1$	*3	(mem)=0
	DECS	reg	1	1+S	$reg \leftarrow reg-1$		reg=FFH
		rp'	2	2+S	$rp' \leftarrow rp'-1$		rp'=FFH
Compare	SKE	reg, #n4	2	2+S	Skip if reg=n4		reg=n4
		@HL, #n4	2	2+S	Skip if (HL)=n4	*1	(HL)=n4
		A, @HL	1	1+S	Skip if A=(HL)	*1	A=(HL)

Instruction	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Compare	SKE	XA, @HL	2	2+S	Skip if XA=(HL)	*1	XA=(HL)
		A, reg	2	2+S	Skip if A=reg		A=reg
		XA, rp'	2	2+S	Skip if XA=rp'		XA=rp'
Carry Flag Operation	SET1	CY	1	1	$CY \leftarrow 1$		
	CLR1	CY	1	1	$CY \leftarrow 0$		
	SKT	CY	1	1+S	Skip if CY=1		CY=1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Instruction	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Memory Bit Manipulation	SET1	mem. bit	2	2	(mem.bit) \leftarrow 1	*3	
		fmem. bit	2	2	(fmem.bit) \leftarrow 1	*4	
		pmem. @L	2	2	(pmem7-2+L3-2.bit(L1-0)) \leftarrow 1	*5	
		@H+mem. bit	2	2	(H+mem3-0.bit) \leftarrow 1	*1	
	CLR1	mem. bit	2	2	(mem.bit) \leftarrow 0	*3	
		fmem. bit	2	2	(fmem.bit) \leftarrow 0	*4	
		pmem. @L	2	2	(pmem7-2+L3-2.bit(L1-0)) \leftarrow 0	*5	
		@H+mem. bit	2	2	(H+mem3-0.bit) \leftarrow 0	*1	
	SKT	mem. bit	2	2+S	Skip if (mem.bit)=1	*3	(mem.bit)=1
		fmem. bit	2	2+S	Skip if (fmem.bit)=1	*4	(fmem.bit)=1
		pmem. @L	2	2+S	Skip if (pmem7-2+L3-2.bit(L1-0))=1	*5	(pmem.@L)=1
		@H+mem. bit	2	2+S	Skip if (H+mem3-0.bit)=1	*1	(@H+mem.bit)=1
	SKF	mem. bit	2	2+S	Skip if (mem.bit)=0	*3	(mem.bit)=0
		fmem. bit	2	2+S	Skip if (fmem.bit)=0	*4	(fmem.bit)=0
		pmem. @L	2	2+S	Skip if (pmem7-2+L3-2.bit(L1-0))=0	*5	(pmem.@L)=0
		@H+mem. bit	2	2+S	Skip if (H+mem3-0.bit)=0	*1	(@H+mem.bit)=0
	SKTCLR	fmem. bit	2	2+S	Skip if (fmem.bit)=1 and clear	*4	(fmem.bit)=1
		pmem. @L	2	2+S	Skip if (pmem7-2+L3-2.bit(L1-0))=1 and clear	*5	(pmem.@L)=1
		@H+mem. bit	2	2+S	Skip if (H+mem3-0.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem. bit	2	2	CY \leftarrow CY \wedge (fmem.bit)	*4	
		CY, pmem. @L	2	2	CY \leftarrow CY \wedge (pmem7-2+L3-2.bit(L1-0))	*5	
		CY, @H+mem. bit	2	2	CY \leftarrow CY \wedge (H+mem3-0.bit)	*1	
	OR1	CY, fmem. bit	2	2	CY \leftarrow CY \vee (fmem.bit)	*4	
		CY, pmem. @L	2	2	CY \leftarrow CY \vee (pmem7-2+L3-2.bit(L1-0))	*5	
CY, @H+mem. bit		2	2	CY \leftarrow CY \vee (H+mem3-0.bit)	*1		
XOR1	CY, fmem. bit	2	2	CY \leftarrow CY \vee (fmem.bit)	*4		
	CY, pmem. @L	2	2	CY \leftarrow CY \vee (pmem7-2+L3-2.bit(L1-0))	*5		
	CY, @H+mem. bit	2	2	CY \leftarrow CY \vee (H+mem3-0.bit)	*1		
Branch	BR	addr	—	—	PC ₁₃₋₀ \leftarrow addr (Most appropriate instruction is selected by assembler from among BR !addr, BRCB !caddr and BR \$addr)	*6	
		!addr	3	3	PC ₁₃₋₀ \leftarrow addr	*6	
		\$addr	1	2	PC ₁₃₋₀ \leftarrow addr	*7	
	BRCB	!caddr	2	2	PC ₁₃₋₀ \leftarrow PC ₁₃ , 12+caddr11-0	*8	
	BR	PCDE	2	3	PC ₁₃₋₀ \leftarrow PC ₁₃₋₈ +DE		
		PCXA	2	3	PC ₁₃₋₀ \leftarrow PC ₁₃₋₈ +XA		

Instruction	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition	
Subroutine Stack Control	CALL	laddr	3	3	(SP-4)(SP-1)(SP-2)←PC11-0 (SP-3)←MBE, RBE, PC13, 12 PC13-0←addr, SP←SP-4	*6		
	CALLF	lfaddr	2	2	(SP-4)(SP-1)(SP-2)←PC11-0 (SP-3)←MBE, RBE, PC13, 12 PC13-0←00, faddr, SP←SP-4	*9		
	RET		1	3	MBE, RBE, PC13, 12←(SP+1) PC11-0←(SP)(SP+3)(SP+2) SP←SP+4			
	RETS		1	3+S	MBE, RBE, PC13, 12←(SP+1) PC11-0←(SP)(SP+3)(SP+2) SP←SP+4, then skip unconditionally		Unconditional	
	RETI		1	3	PC13, 12←(SP+1) PC11-0←(SP)(SP+3)(SP+2) PSW←(SP+4)(SP+5), SP←SP+6			
	PUSH	rp		1	1	(SP-1)(SP-2)←rp, SP←SP-2		
		BS		2	2	(SP-1)←MBS, (SP-2)←RBS, SP←SP-2		
	POP	rp		1	1	rp←(SP-1)(SP), SP←SP-2		
BS			2	2	MBS←(SP+1), RBS←(SP), SP←SP+2			
Interrupt Control	EI		2	2	IME (IPS.3)←1			
		IExxx	2	2	IExxx←1			
	DI		2	2	IME (IPS.3)←0			
		IExxx	2	2	IExxx←0			
Input/Output	IN*1	A, PORTn	2	2	A←PORTn (n=0-9, 12-14)			
		XA, PORTn	2	2	XA←PORTn+1, PORTn (n=4, 6, 8, 12)			
	OUT*1	PORTn, A	2	2	PORTn←A (n=2-9, 12-14)			
		PORTn, XA	2	2	PORTn+1, PORTn←XA (n=4, 6, 8, 12)			
CPU Control	HALT		2	2	Set HALT Mode (PCC.2←1)			
	STOP		2	2	Set STOP Mode (PCC.3←1)			
	NOP		1	1	No Operation			
Special	SEL	RBn	2	2	RBS←n (n=0-3)			
		MBn	2	2	MBS←n (n=0, 1, 15)			
	GETI*2	taddr	1	3	<ul style="list-style-type: none"> TBR Instruction PC13-0←(taddr)4-0+(taddr+1) TCALL Instruction (SP-4)(SP-1)(SP-2)←PC11-0 (SP-3)←MBE, RBE, PC13, 12 PC13-0←(taddr)5-0+(taddr+1) SP←SP-4 When not TBR and TCALL instructions, (taddr) and (taddr+1) instructions are executed. 	*10	Depends on the instruction referred to.	

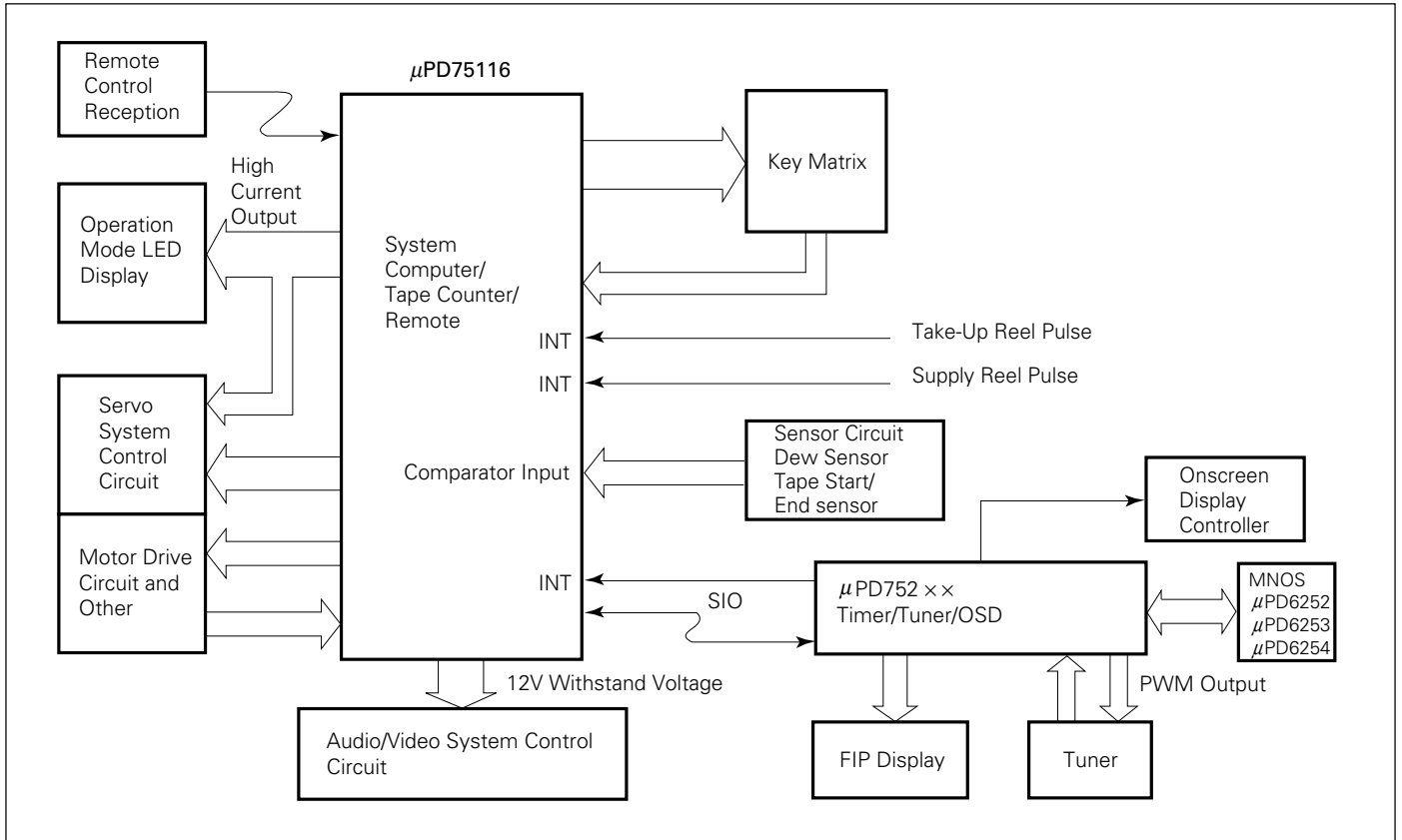
* 1: MBE=0 or 1 and MBS=15 must be set for execution of IN/OUT instruction.

* 2: TBR and TCALL instructions are assembler pseudo-instructions for GETI instruction table definition.

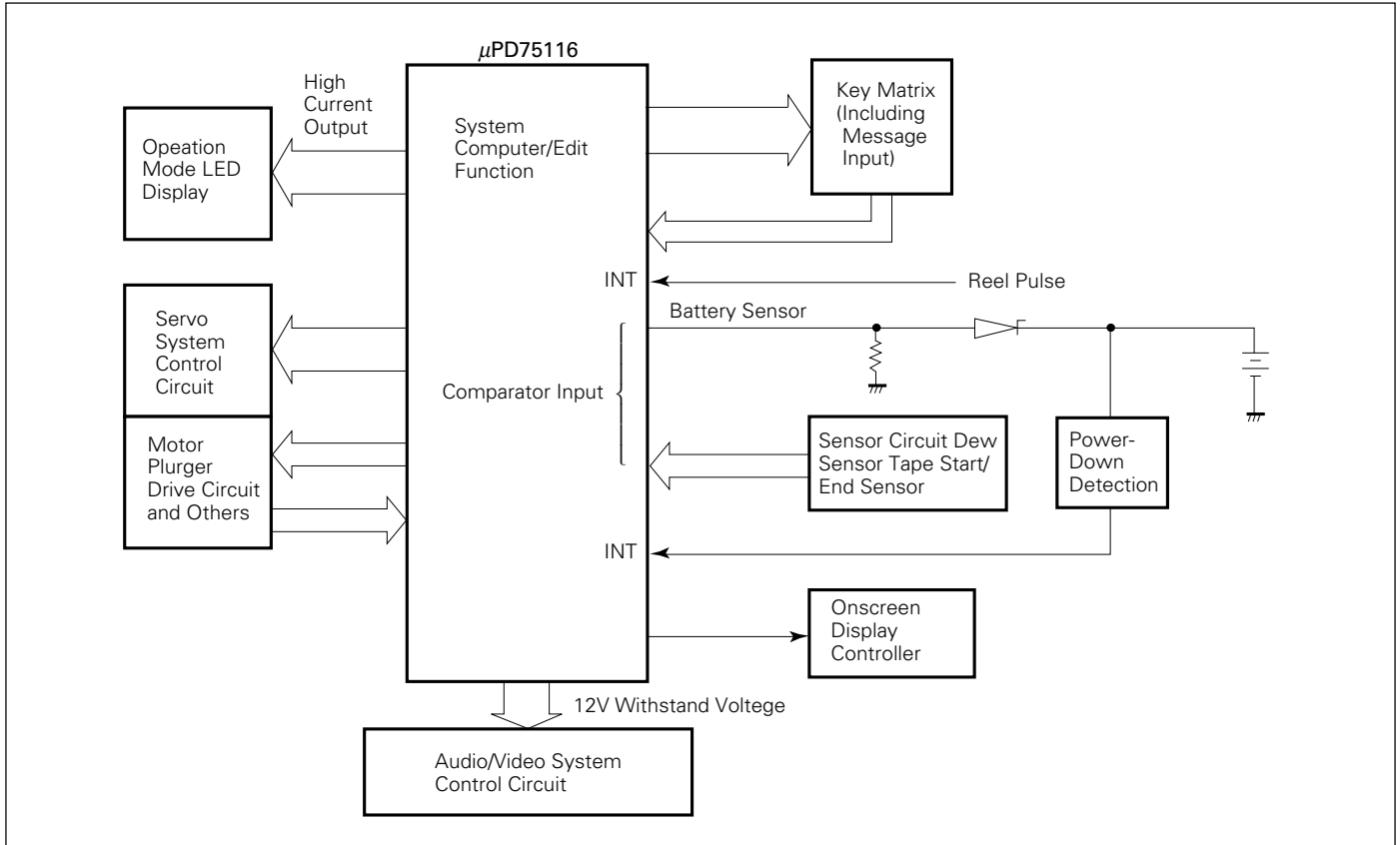
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10. Application Block Diagrams

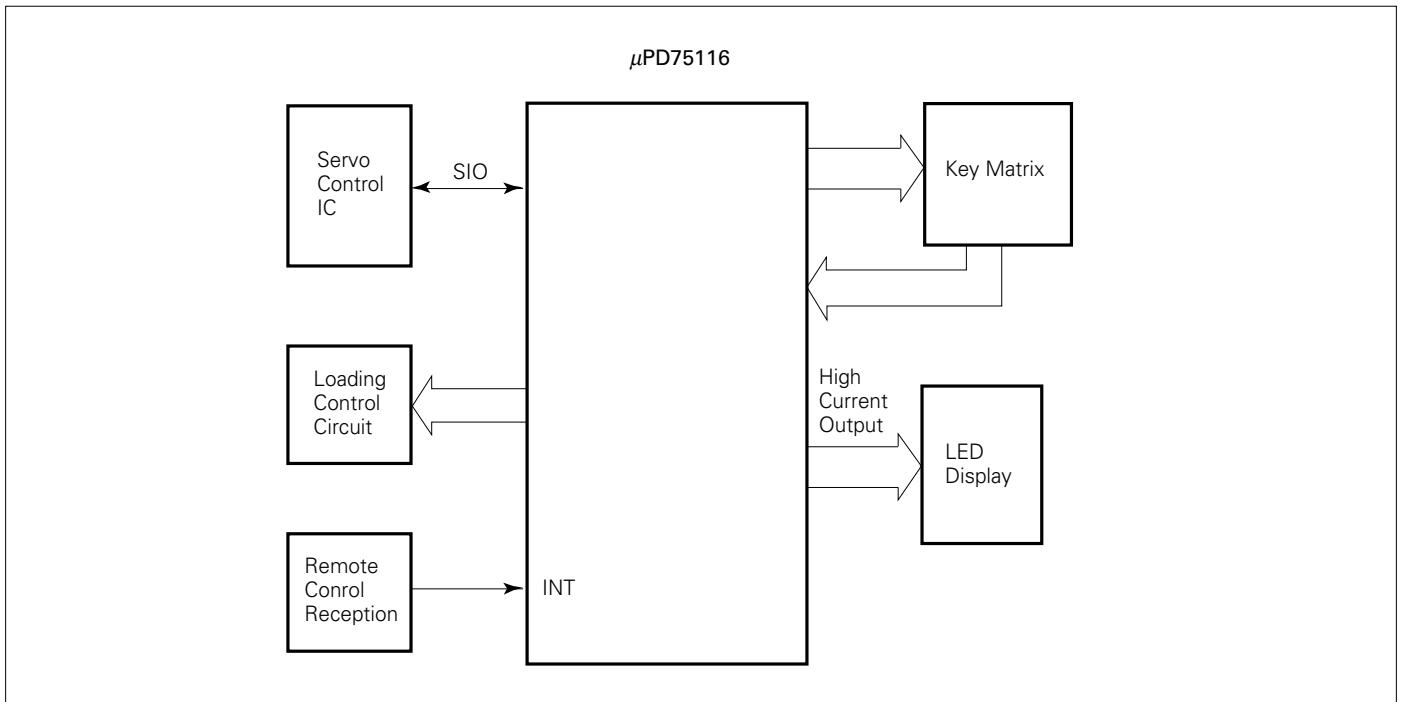
10.1 VCR System Coputer Applications



10.2 VCR Camera Applications

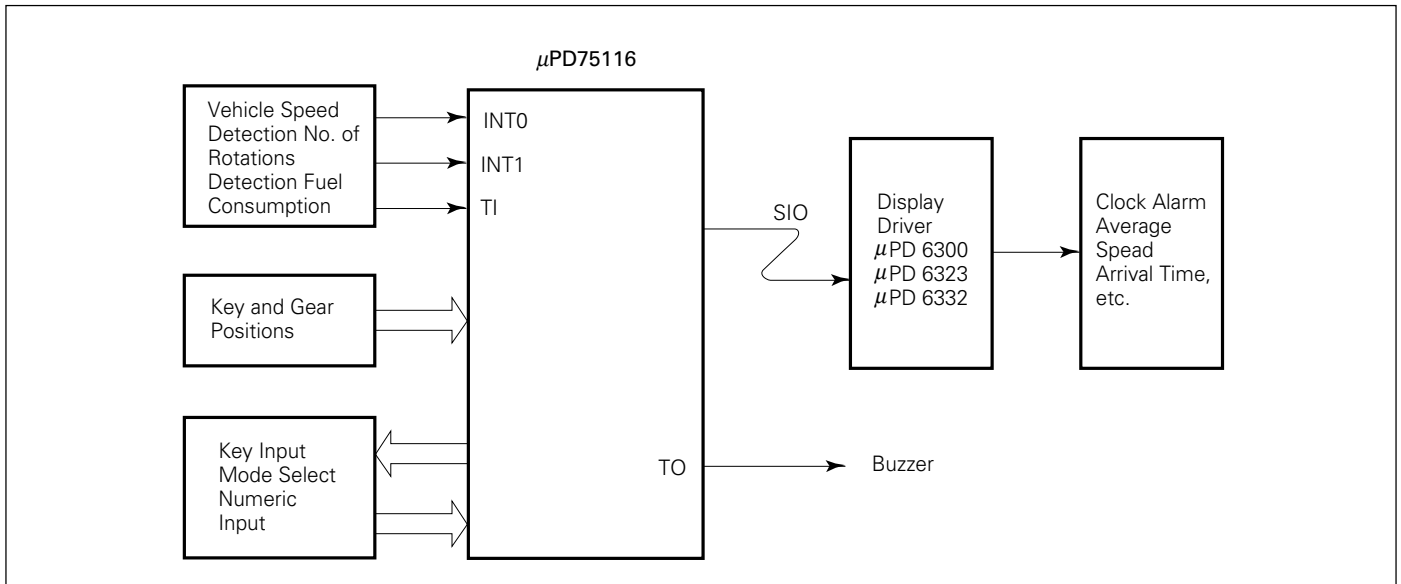


10.3 Compact Disk Player

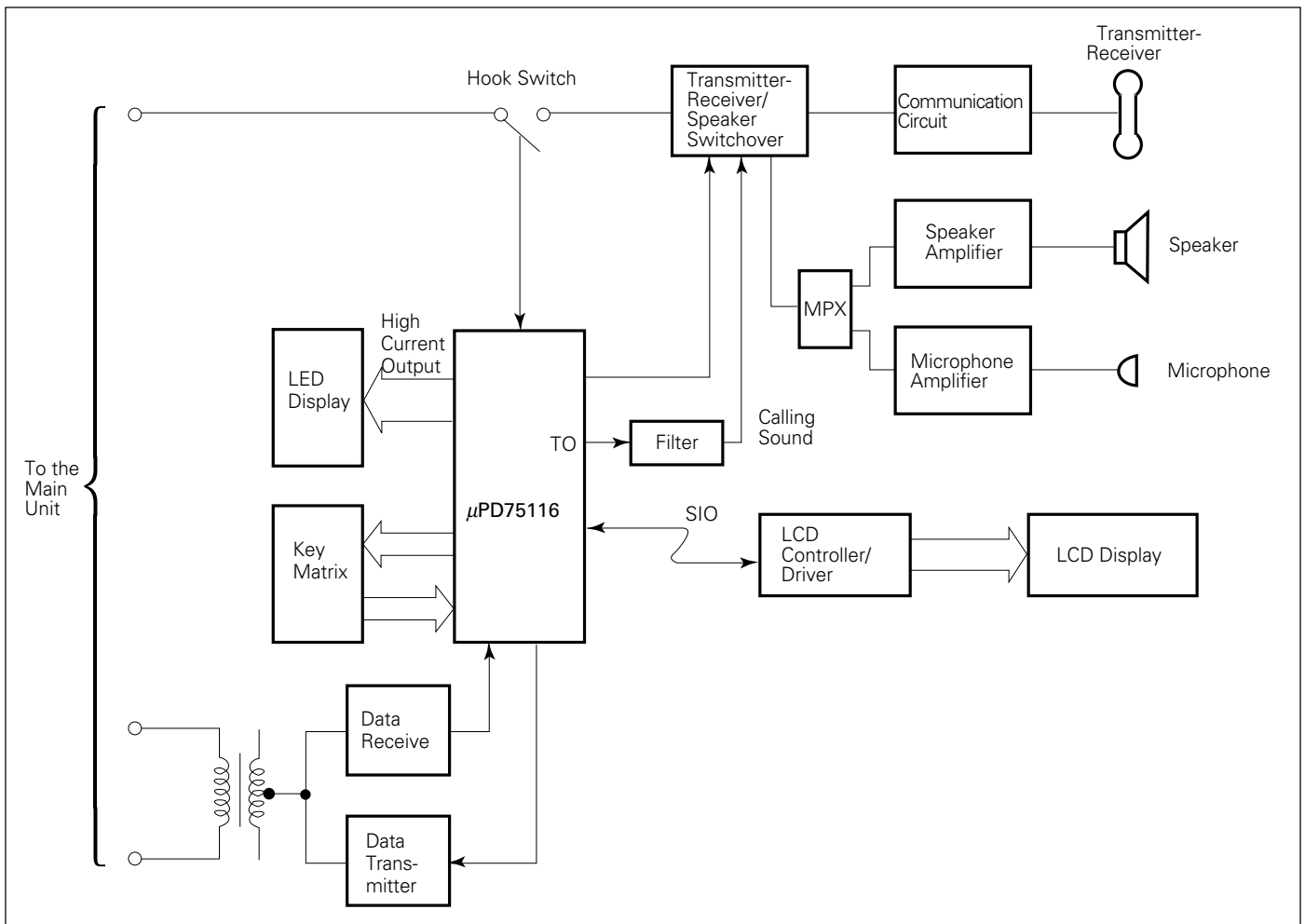


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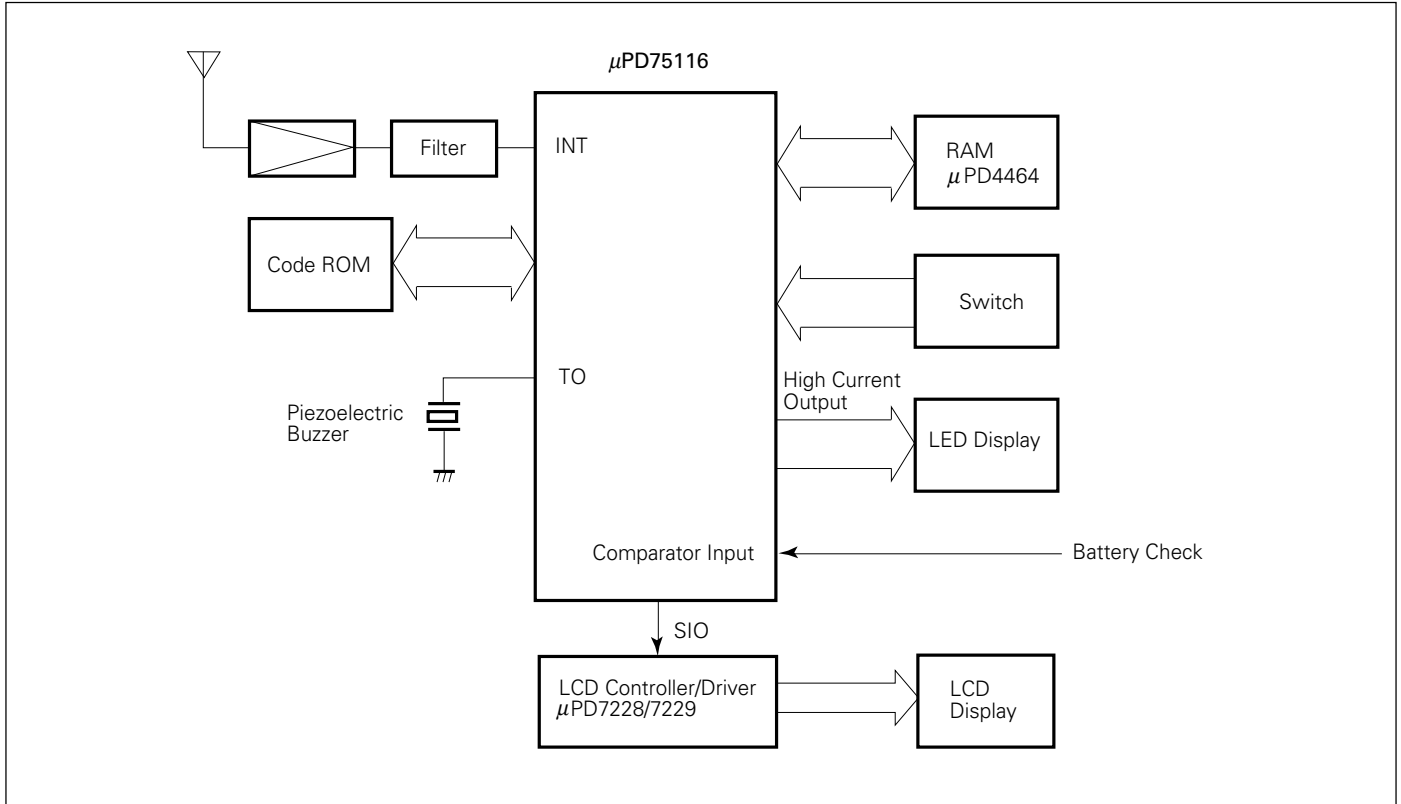
10.4 Vehicle-Mounted Applications (Trip Computer)



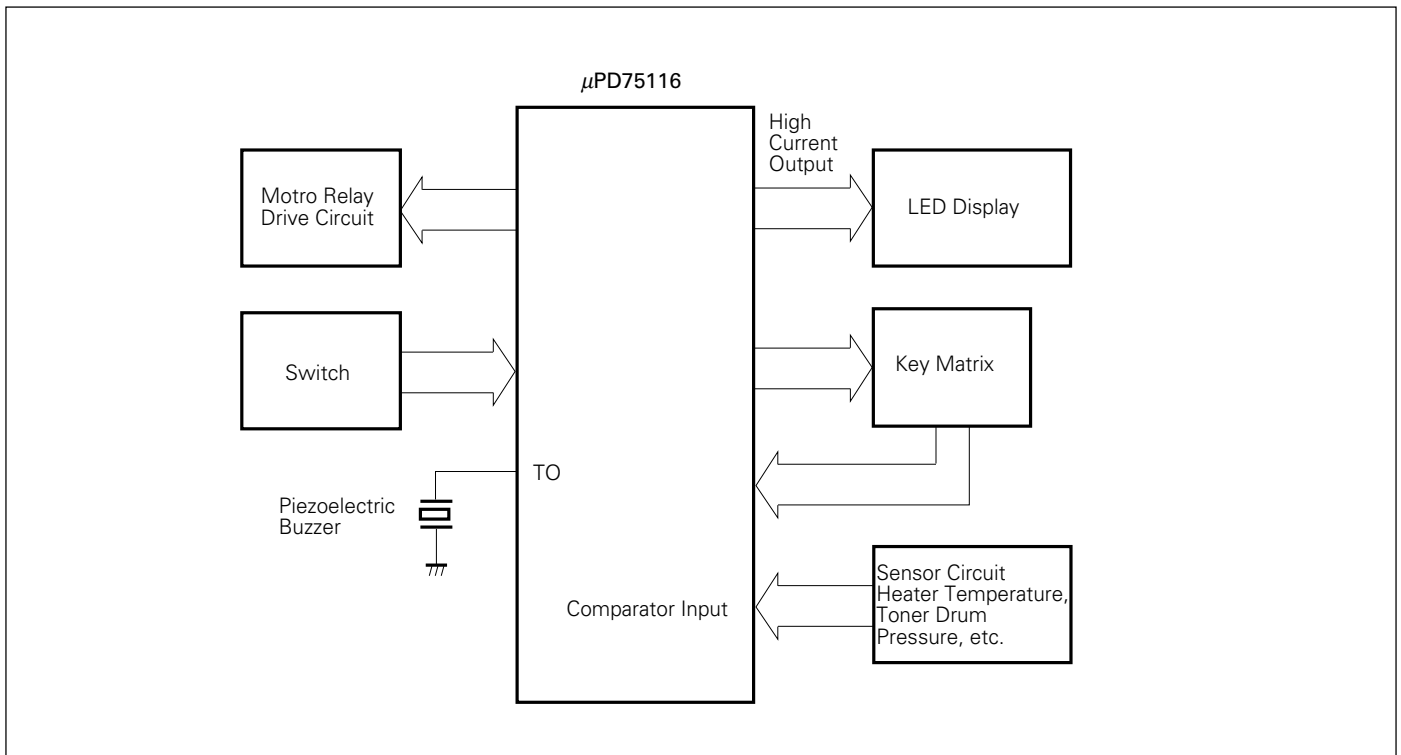
10.5 Push-Button Telephone



10.6 Display Pager

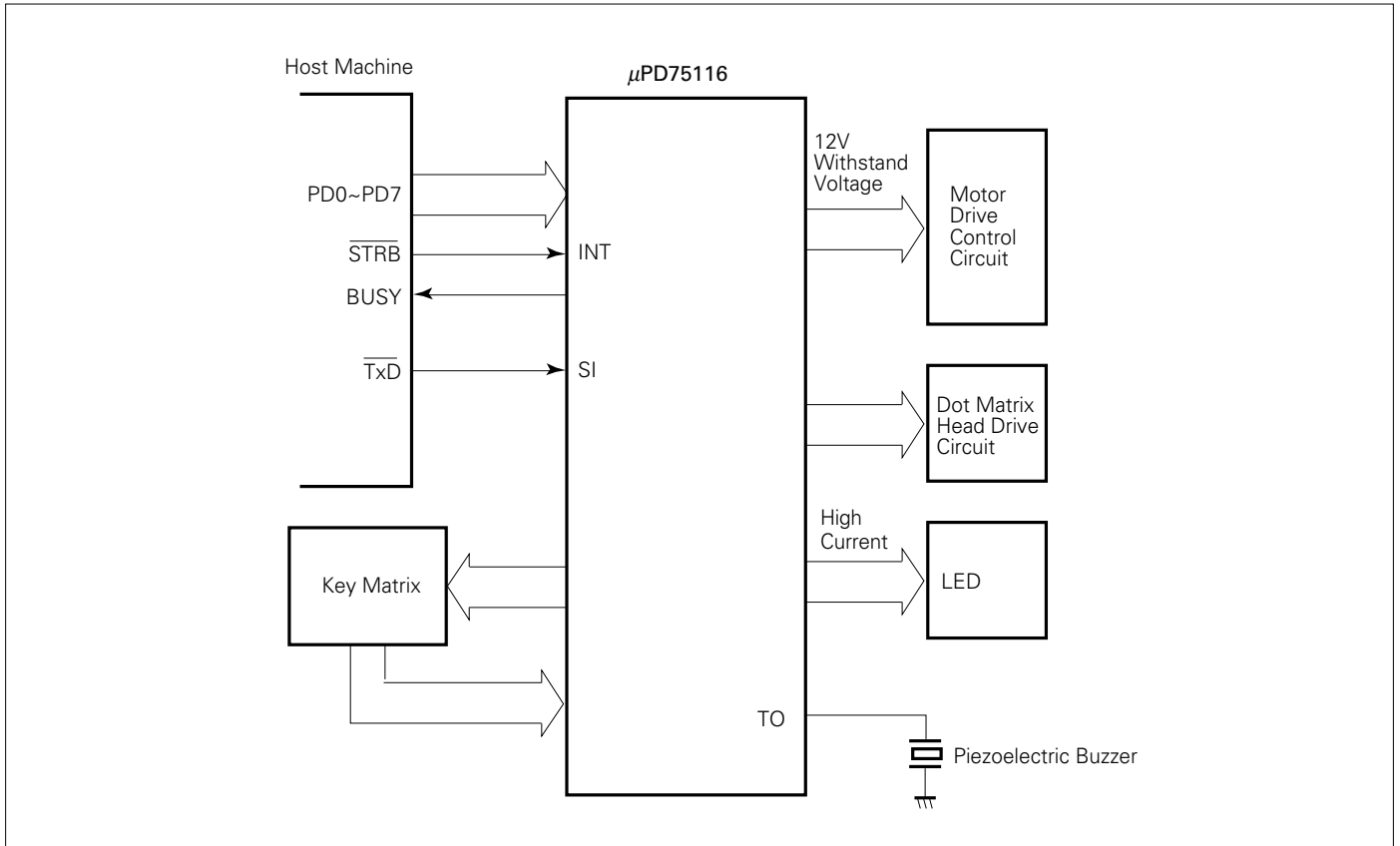


10.7 PPC



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10.8 Printer Controller



11. Mask Option Selection

The following mask options are available for the ★ μPD75116.

Whether or not they should be incorporated can be selected.

(1) Pins

Pin	Mask Option
P120 to P123	Bit-wise pull-up resistor incorporation enable
P130 to P133	
P140 to P143	

(2) Power-on reset circuit and power-on flag (PONF)

One of the following three settings can be selected.

Mask Option Specification		Switch Selection (See Figure 8-1)		Internal Reset Signal (RES)
Power-on Reset Circuit	Power-on Flag (PONF)	SWA	SWB	
Incorporated	Incorporated	ON	ON	Generated automatically
Not incorporated	Incorporated	ON	OFF	Not generated automatically
Not incorporated	Not incorporated	OFF	OFF	————

12. Electrical Specifications

Absolute Maximum Ratings

(Ta = 25 °C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Power supply voltage	V _{DD}			-0.3 to +7.0	V
Input voltage	V _{I1}	Except for ports 12 to 14		-0.3 to V _{DD} +0.3	V
		V _{I2} *1	Ports 12 to 14	On-chip pull-up resistor	-0.3 to V _{DD} +0.3
	Open drain			-0.3 to +13	V
Output voltage	V _O			-0.3 to V _{DD} +0.3	V
Output current high	I _{OH}	1 pin		-15	mA
		All pins		-30	mA
Output current low	I _{OL} *2	1 pin	Peak value	30	mA
			Effective value	15	mA
		Total current of ports 0, 2 to 4, 12 to 14	Peak value	100	mA
			Effective value	60	mA
		Total current of ports 5 to 9	Peak value	100	mA
			Effective value	60	mA
Operation temperature	T _{opt}			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C

* 1: When applying a voltage larger than 10V to ports 12, 13 and 14 each, set the power impedance (pull-up resistor) to 50 kΩ or more.

2: Calculate each effective value using the following expression:

$$[\text{Effective value}] = [\text{Peak value}] \times \sqrt{\text{duty}}$$

Note: Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Operating Voltage ★
(Ta = -40 to +85 °C)

Parameter	Test Conditions	MIN.	MAX.	Unit
CPU*1		*2	6.0	V
Programmable threshold port (comparator input)		4.5	6.0	V
Power-on reset circuit*3		4.5	6.0	V
Other hardware*1		2.7	6.0	V

*1: Except system clock oscillator, programmable threshold port and power-on reset circuit

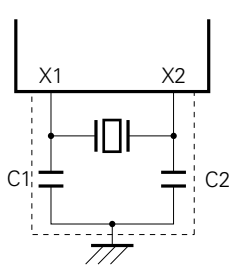
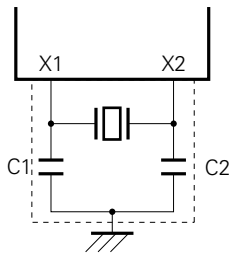
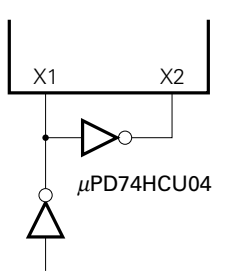
*2: Operating voltage range depends on the cycle time.
See the **AC Characteristics**.

*3: Whether or not it should be incorporated can be selected by mask options.
See the **Power-On Reset Circuit Characteristics (Mask Option)**.

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Oscillate Characteristics

($T_a = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 6.0 V)

Oscillator	Recommended Constant	Parameter	Test Condition	MIN.	TYP.	MAX.	Unit
Ceramic oscillation		Oscillator frequency (f_{xx})*1	V_{DD} = oscillation voltage range	2.0		5.0*3	MHz
		Oscillation stabilizing time*2	Oscillation voltage range MIN.	4			ms
Crystal oscillator		Oscillator frequency (f_{xx})*1		2.0	4.19	5.0*3	MHz
		Oscillation stabilizing time*2	$V_{DD} = 4.5$ to 6.0 V	10			ms
				30			ms
External clock		X1 input frequency (f_x)*1		2.0		5.0*3	MHz
		X1 input high and low level widths (t_{XH} , t_{XL})		100		250	ns

- * 1: Oscillator frequency and X1 input frequency indicate only characteristics of the oscillator. Refer to AC characteristics for the instruction execution time.
- 2: The oscillation stabilizing time is necessary for oscillation to stabilize after V_{DD} reaches oscillation voltage range MIN. or the STOP mode is released.
- ★ 3: When the oscillator frequency is $4.19 \text{ MHz} < f_{xx} \leq 5.0 \text{ MHz}$, PCC=0011 should not be selected as instruction execution time. If PCC=0011 is selected, 1 machine cycle becomes less than $0.95 \mu\text{s}$, with the result that the specified MIN. value of $0.95 \mu\text{s}$ cannot be observed.

Note: When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance. ★

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V_{SS} . Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

Recommended Oscillator Constant

Ceramic Oscillators

(Ta = -40 to +85 °C)

Manufacturer	Product Name	Capacity of Externally-Mounted Product [pF]		Oscillation Voltage range [V]	
		C1	C2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSA 2.00MG	30	30	2.7	6.0
	CSA 4.19MG	30	30	3.0	6.0
	CSA 4.19MGU	30	30	2.7	6.0
	CST 4.19T	Built-in	Built-in	3.0	6.0
Kyocera Corp.	KBR-2.0MS	100	100	3.0	6.0
	KBR-4.0MS	33	33	3.0	6.0
	KBR-4.19MS	33	33	3.0	6.0
	KBR-4.9152M	33	33	3.0	6.0

Crystal Resonator

(Ta = -20 to +70 °C)

Manufacturer	Product Name	Capacity of Externally-Mounted Product [pF]		Oscillation Voltage range [V]	
		C1	C2	MIN.	MAX.
Kinseki Co., Ltd.	HC-49/U	22	22	2.7	6.0

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DC Characteristics

(Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V _{IH1}	Except for ports listed below		0.7V _{DD}		V _{DD}	V
	V _{IH2}	Ports 0, 1, T10, 1, RESET		0.8V _{DD}		V _{DD}	V
	V _{IH3}	Ports 12 to 14	On-chip pull-upresistor	0.7V _{DD}		V _{DD}	V
			Open drain	0.7V _{DD}		12	V
V _{IH4}	X1, X2		V _{DD} -0.5		V _{DD}	V	
Input vltage low	V _{IL1}	Except for ports listed below		0		0.3V _{DD}	V
	V _{IL2}	Ports 0, 1, T10, 1, RESET		0		0.2V _{DD}	V
	V _{IL3}	X1, X2		0		0.4	V
Output voltage high	V _{OH}	V _{DD} = 4.5 to 6.0 V, I _{OH} = -1 mA		V _{DD} -1.0			V
		I _{OH} = -100μA		V _{DD} -0.5			V
Output voltage low	V _{OL}	V _{DD} = 4.5 to 6.0 V	Ports 0, 2 to 9, I _{OL} = 15 mA		0.35	2.0	V
			Ports 12 to 14, I _{OL} = 10 mA		0.35	2.0	V
	V _{DD} = 4.5 to 6.0V, I _{OL} = 1.6 mA					0.4	V
	I _{OL} = 400μA					0.5	V
Input leakage current high	I _{LIH1}	V _{IN} = V _{DD}	Except for ports listed below			3	μA
			X1, X2			20	μA
	I _{LIH3}	V _{IN} = 12 V	Ports 12 to 14 (for open drain)			20	μA
Input leakage current low	I _{LIL1}	V _{IN} = 0 V	Except for X1, X2			-3	μA
			X1, X2			-20	μA
Output leakage current high	I _{LOH1}	V _{OUT} = V _{DD}	Except for ports listed below			3	μA
			I _{LOH2}	V _{OUT} = 12 V	Ports 12 to 14 (for open drain)		
Output leakage current low	I _{LOL}	V _{OUT} = 0 V				-3	μA
On-chip pull-up resistor	R _L	Ports 12 to 14	V _{DD} =5 V ±10%	15	40	70	kΩ
				10		80	kΩ
Supply current*1	I _{DD1}	4.19 MHz crystal oscillation C1 = C2 = 22 pF	V _{DD} =5 V ±10%*2		3	9	mA
			V _{DD} =3 V ±10%*3		0.55	1.5	mA
	I _{DD2}		HALT mode	V _{DD} =5 V ±10%	600	1800	μA
				V _{DD} =3 V ±10%	200	600	μA
I _{DD3}	STOP mode, V _{DD} = 3 V ±10%			0.1	10	μA	

* 1: Current for the on-chip pull-up resistor, power-on reset circuit (mask option) and comparator circuit is not included.
 2: When operated in the high-speed mode with the processor clock

control resistor (PCC) set tp 0011.
 3: When operated in the low-speed mode with the PCC set to 0000.

Capacitance

($T_a = 25\text{ }^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz 0 V for pins except the measured pins			15	pF
Output capacitance	C_{OUT}				15	pF
Input/output capacitance	C_{IO}				15	pF

Comparator Characteristics

($T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $V_{DD} = 4.5\text{ to }6.0\text{ V}$)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD}	V
PTH input voltage	V_{IPTH}		0		V_{DD}	V
Comparator circuit consumption		Set PTHM7 to "1".		1		mA

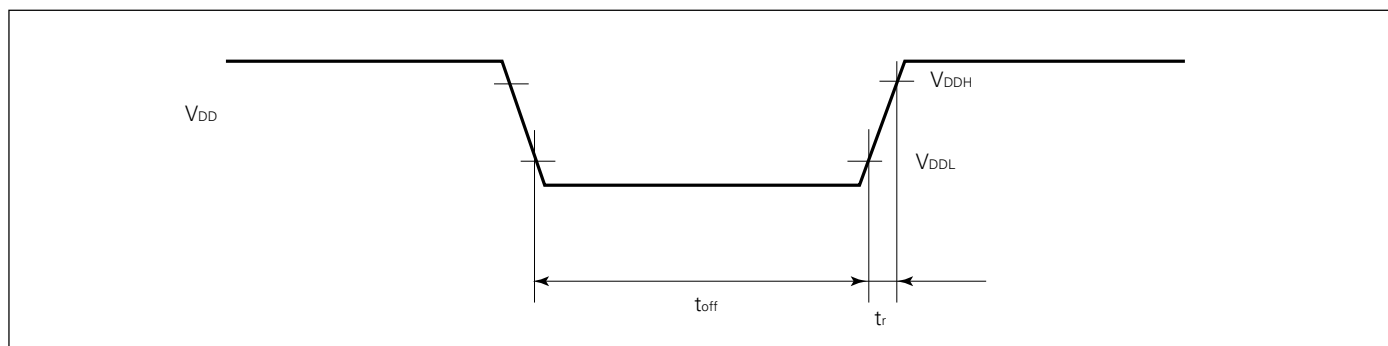
Power-On Reset Circuit Characteristics (Mask Option)

($T_a = -40\text{ to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power-on reset operating voltage high	V_{DDH}		4.5		6.0	V
Power-on reset operating voltage low	V_{DDL}		0		0.2	V
Supply voltage rise time	t_r		10		*1	μs
Supply voltage off time	t_{off}		1			s
Power-on reset circuit current consumption*2	I_{DDPR}	$V_{DD} = 5\text{ V} \pm 10\%$		10	100	μA
		$V_{DD} = 2.5\text{ V}$		2	20	μA

*1: $2^{17}/f_{XX}$ (31.3 ms when $f_{XX} = 4.19\text{ MHz}$)

*2: Current flow upon power-on reset or with an on-chip power-on flag



Note: Start the power supply smoothly.

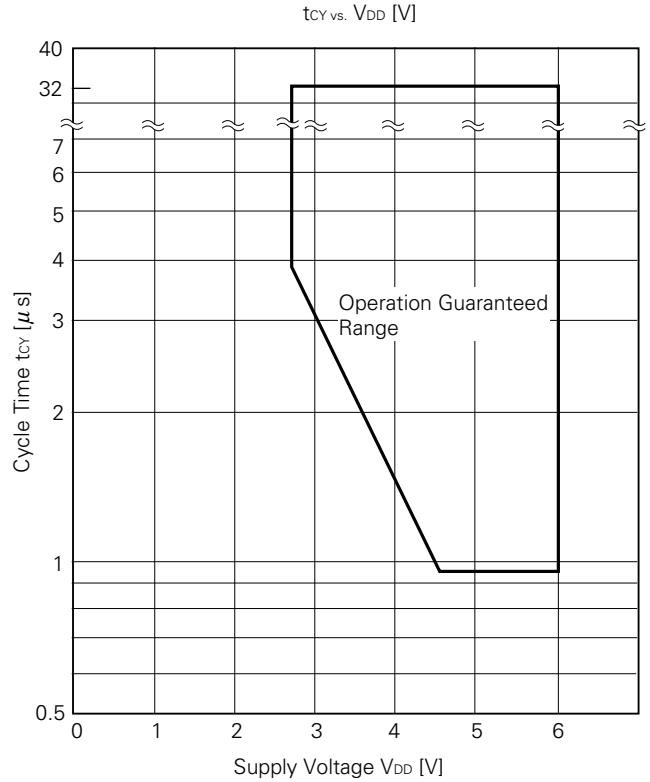
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AC Characteristics

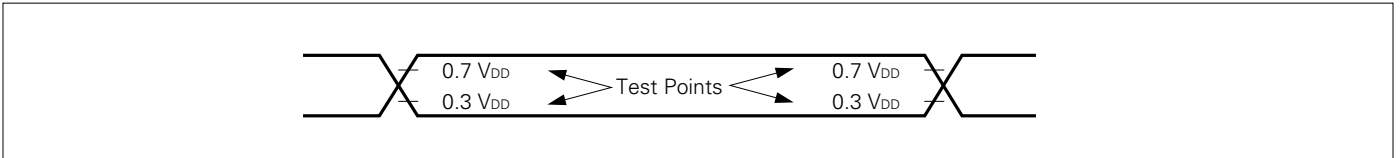
(Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
CPU clock cycle time* (min. instruction execution time = 1 machine cycle)	tcy	VDD = 4.5 to 6.0 V	0.95		32	μs
			3.8		32	μs
TI0, TI1 input frequency	fTI	VDD = 4.5 to 6.0 V	0		1	MHz
			0		275	kHz
TI0, TI1 input high and low-level widths	tTIH, tTIL	VDD = 4.5 to 6.0 V	0.48			μs
			1.8			μs
SCK cycle time	tkcy	VDD = 4.5 to 6.0 V	Input	0.8		μs
			Output	0.95		μs
			Input	3.2		μs
			Output	3.8		μs
SCK high and low-level widths	tkH, tkL	VDD = 4.5 to 6.0 V	Input	0.4		μs
			Output	tkcy/2-50		ns
			Input	1.6		μs
			Output	tkcy/2-50		ns
SI setup time (to SCK↑)	tsik		100			ns
SI hold time (from SCK↑)	tkSI		400			ns
S0 output delay time from SCK↓	tkSO	VDD = 4.5 to 6.0 V			300	ns
					1000	ns
INT0 to INT4 High and low-level widths	tINTH, tINTL		5			μs
RESET low-level width	trSL		5			μs

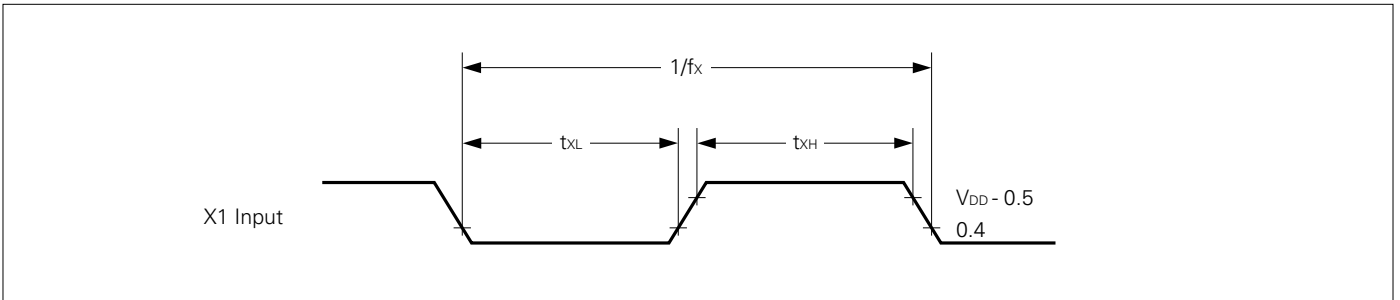
*: The cycle time of the CPU clock (ϕ) is determined by the input frequency of the ceramic crystal oscillator and the setting of the processor clock control register (PCC). The cycle time (t_{CY}) for V_{DD} is shown below.



AC Timing Test Point (Except for Ports 0, 1, TI0, TI1, X1, X2 and RESET)

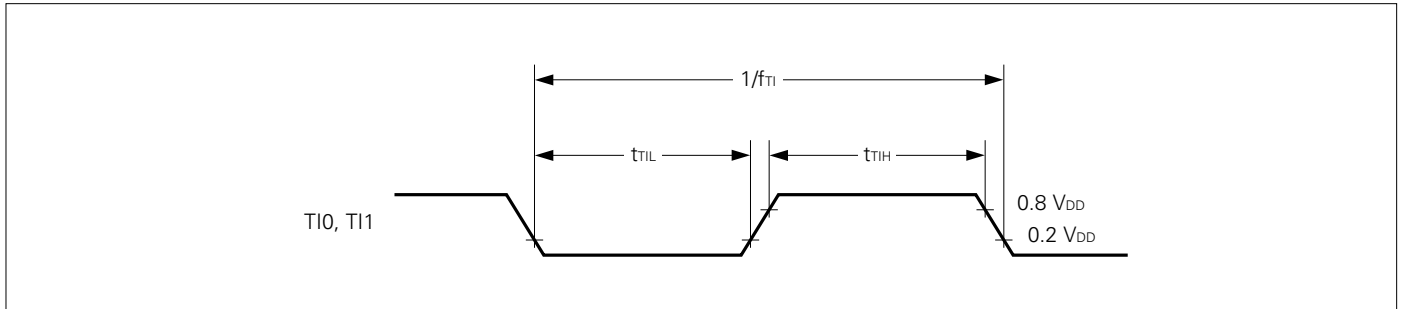


Clock Timing

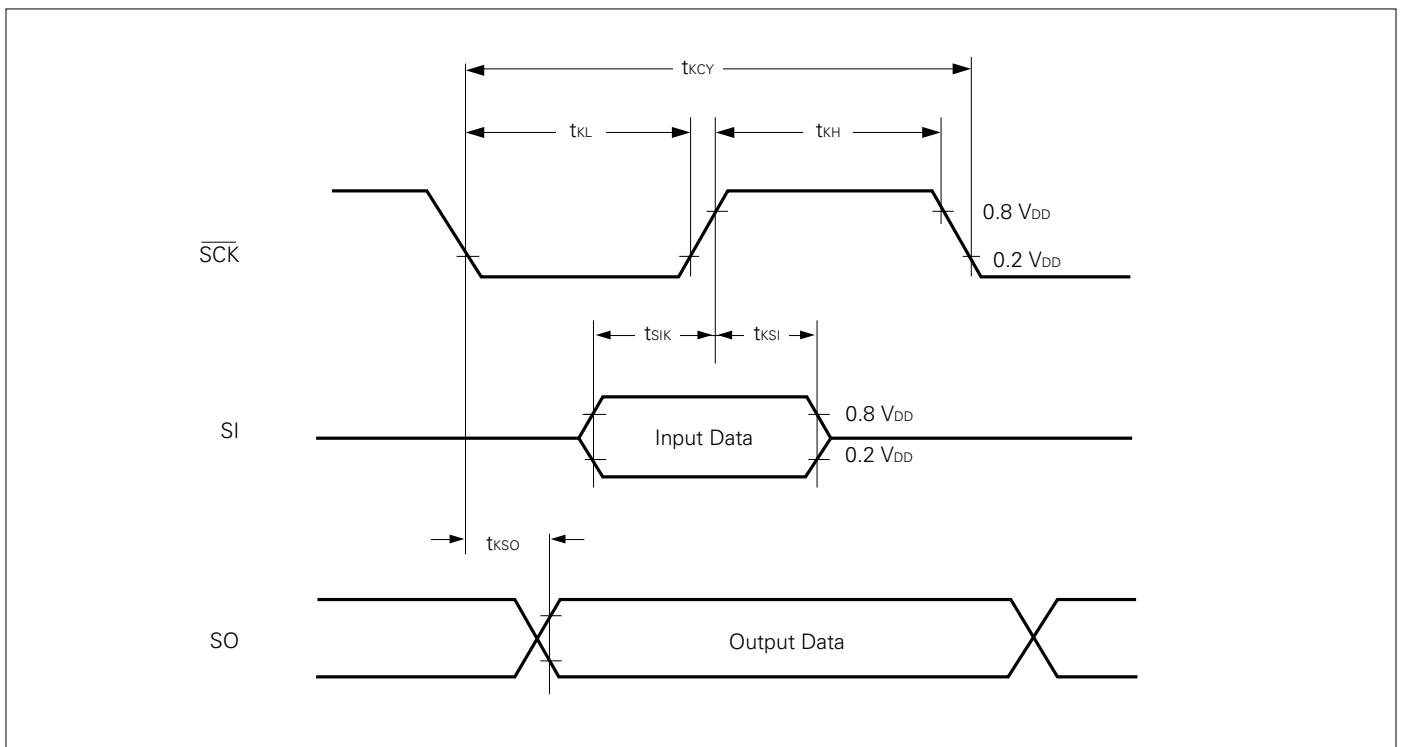


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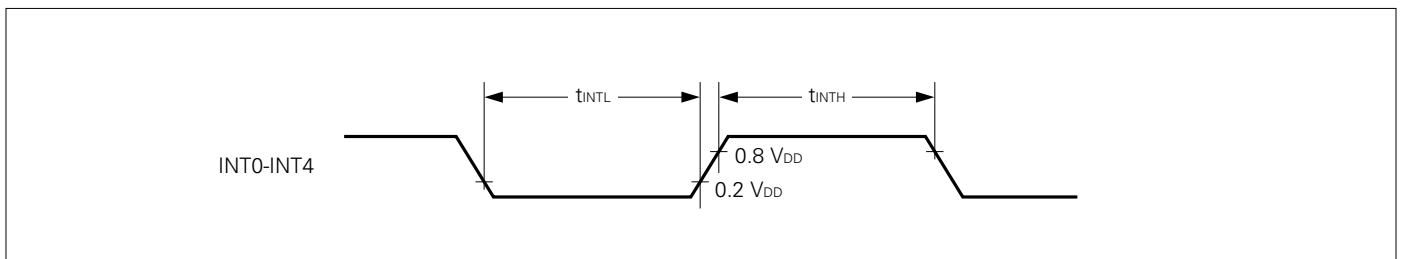
T10 and T11 Input Timing



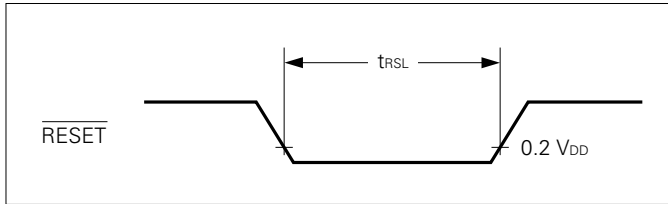
Serial Transfer Timing



Interrupt Input Timing



RESET Input Timing



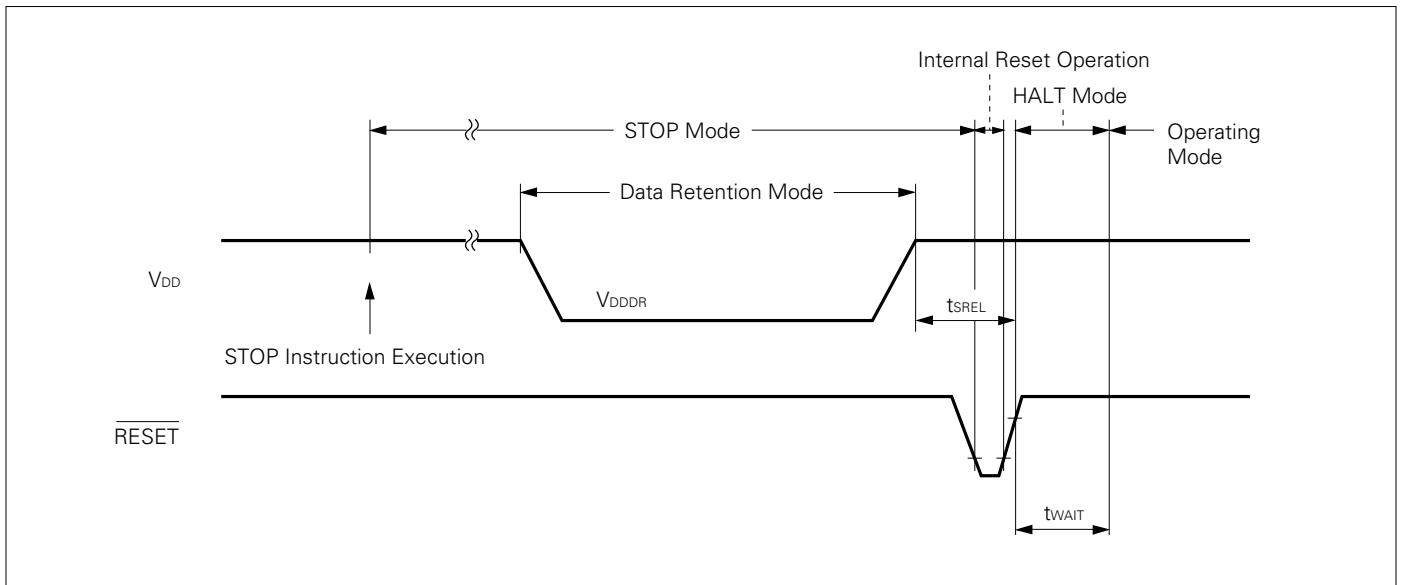
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Ta = -40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		2.0		6.0	V
Data retention supply current *1	VDDDR	VDDDR = 2.0 V		0.1	10	μA
Release signal set time	tsREL		0			μs
Oscillation stabilization wait time *2	tWAIT	Release by $\overline{\text{RESET}}$		$2^{17}/f_x$		ms
		Release by interrupt request		*3		ms

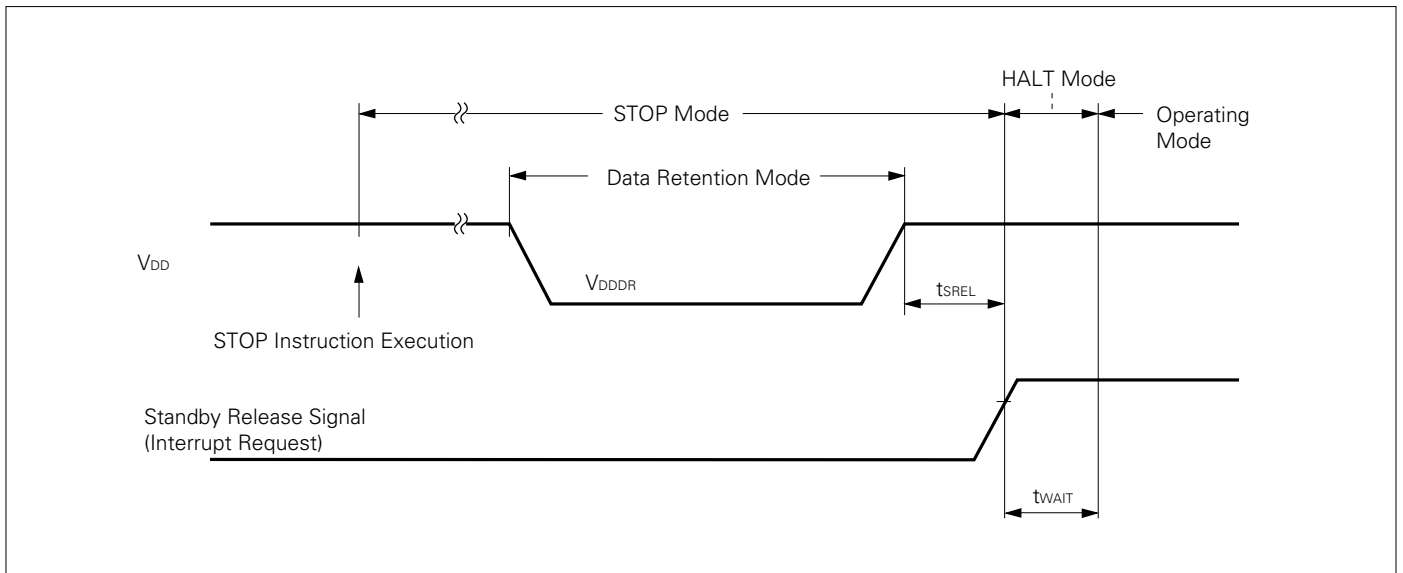
- * 1: Current for the on-chip pull-up resistor, power-on circuit (mask option) and comparator circuit is not included.
- 2: The oscillation stabilizing time is intended to stop the CPU to prevent any unstable operation at the start of oscillation.
- 3: Depends on the following setting of the basic interval timer mode register (BTM).

BTM3	BTM2	BTM1	BTM0	Wait Time (fxx=4.19 MHz Valu's in Parentheses)
—	0	0	0	$2^{20}/f_{xx}$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_{xx}$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_{xx}$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_{xx}$ (approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)

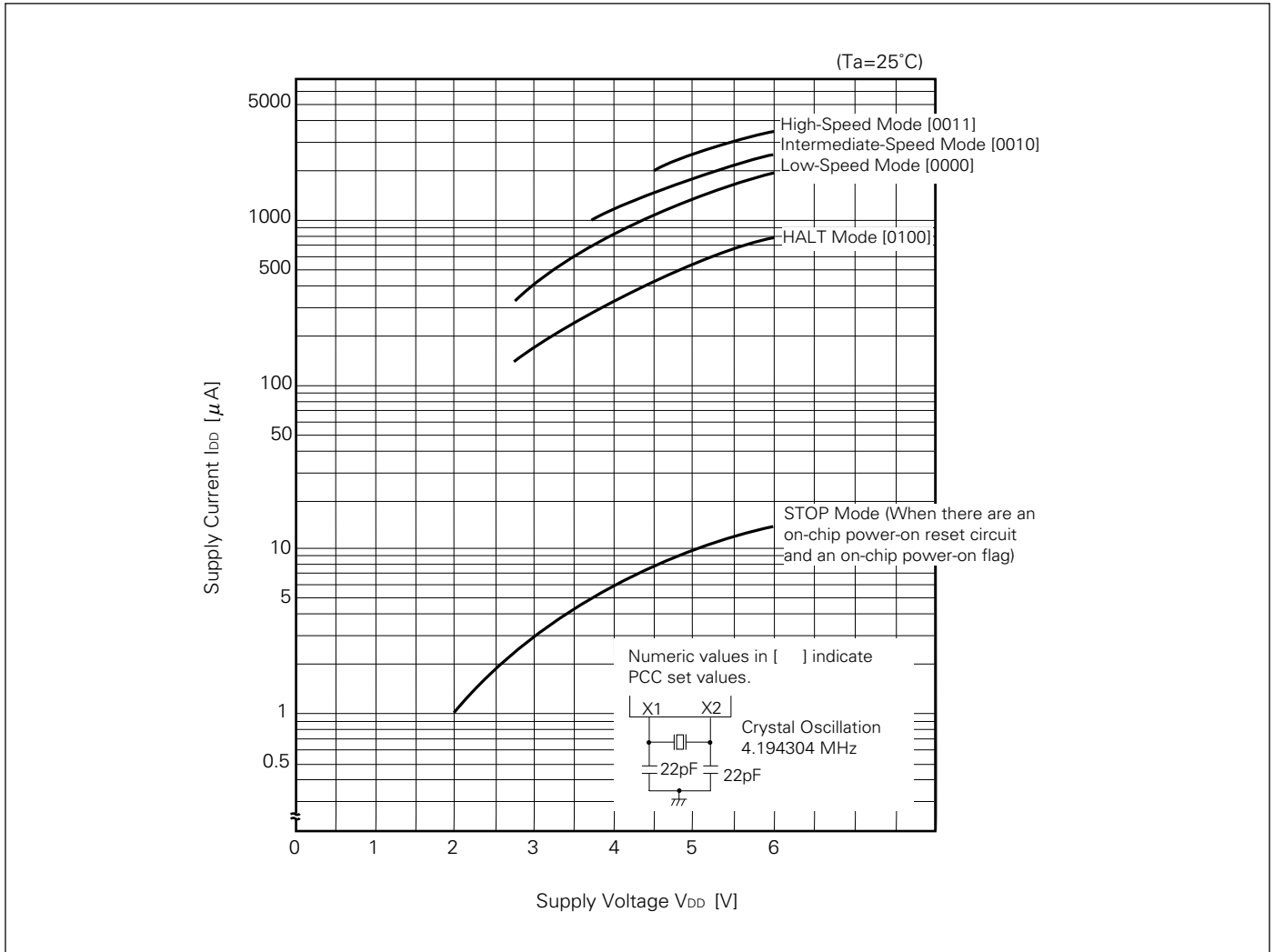


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



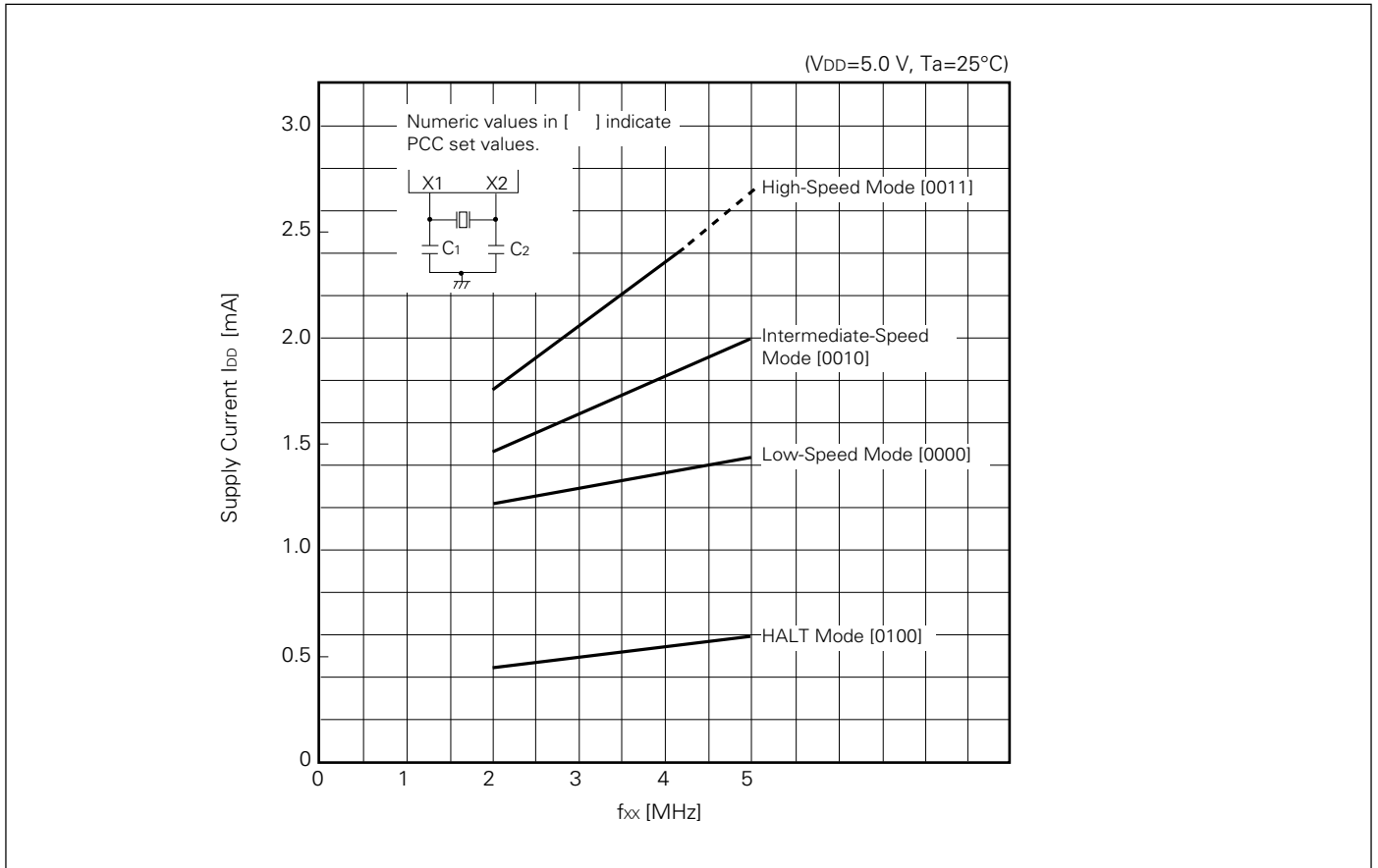
13. Characteristic Curves

I_{DD} vs. V_{DD} Characteristics Example (Crystal Oscillation)

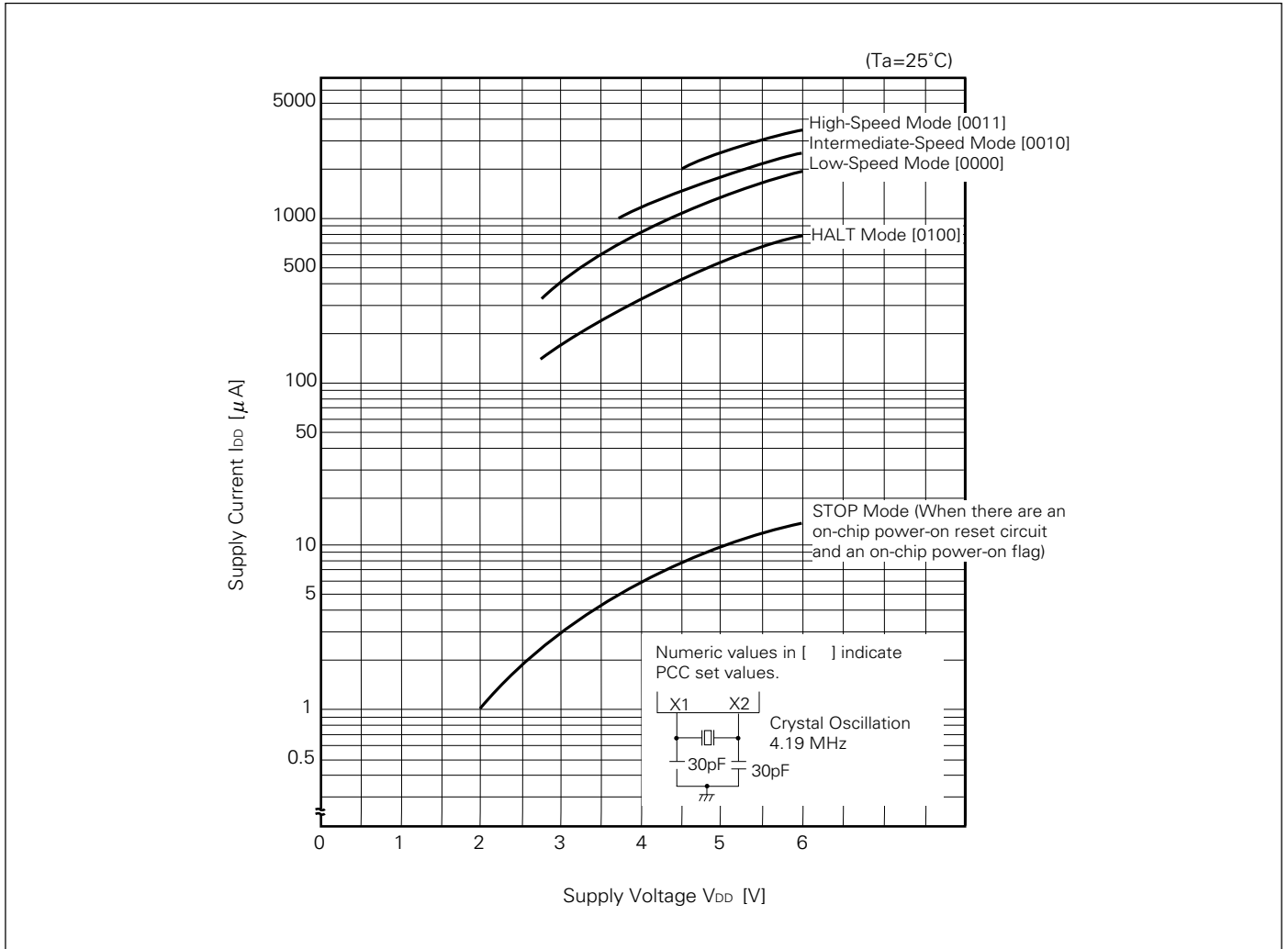


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I_{DD} vs. f_{XX} Characteristics Example (Crystal Oscillation)

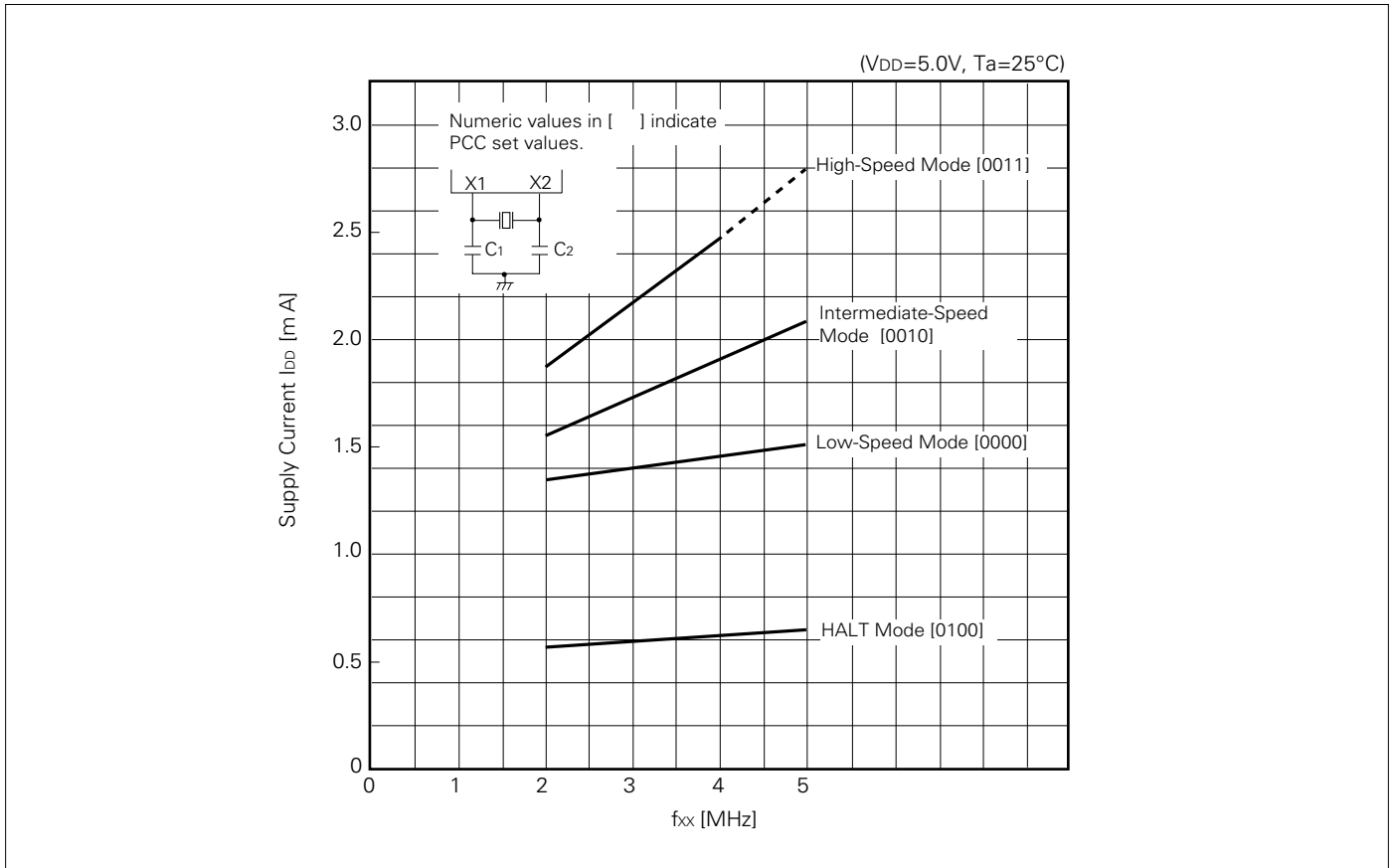


I_{DD} vs. V_{DD} Characteristics Example (Ceramic Oscillation)

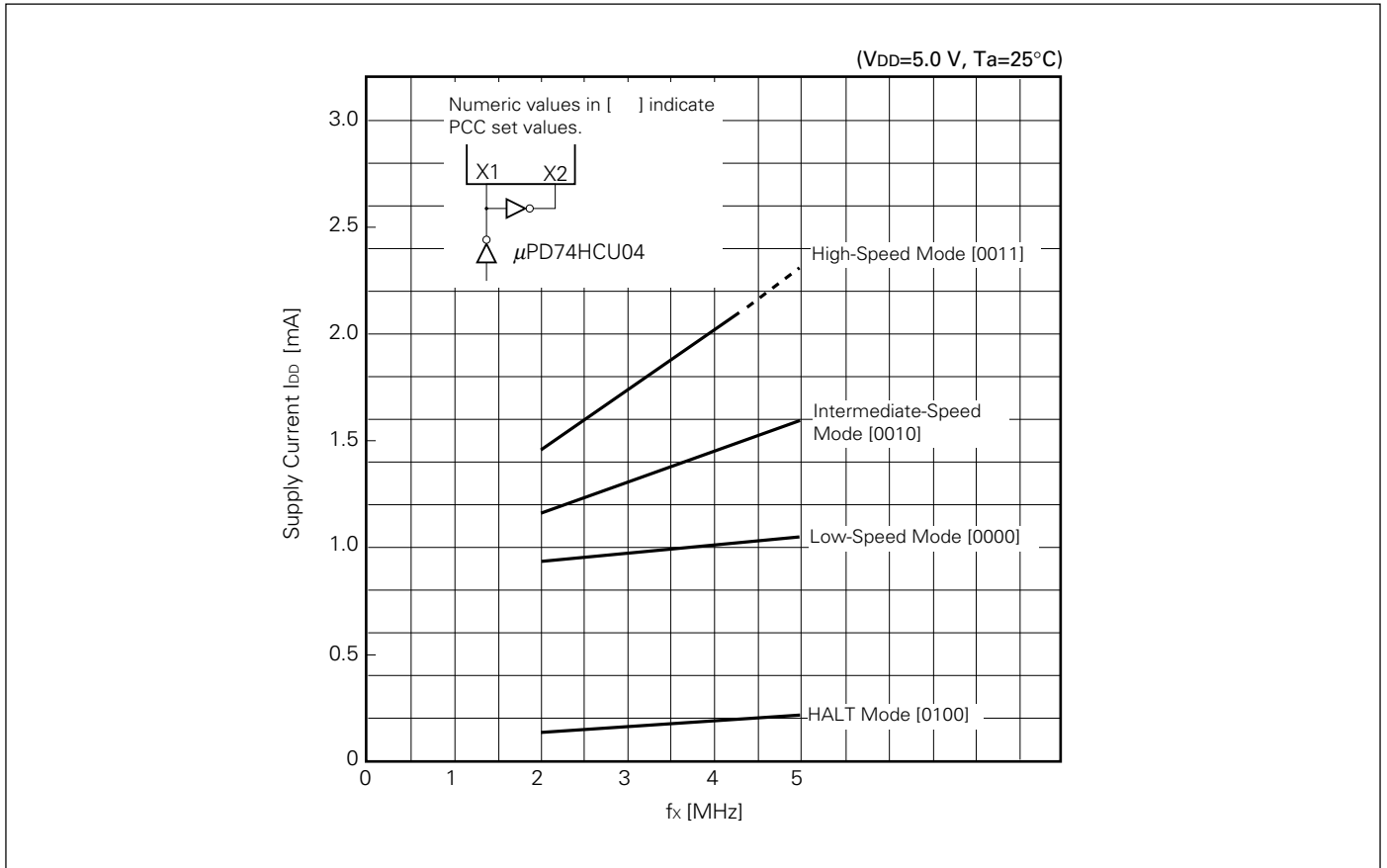


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I_{DD} vs. f_{XX} Characteristics Example (Ceramic Oscillation)

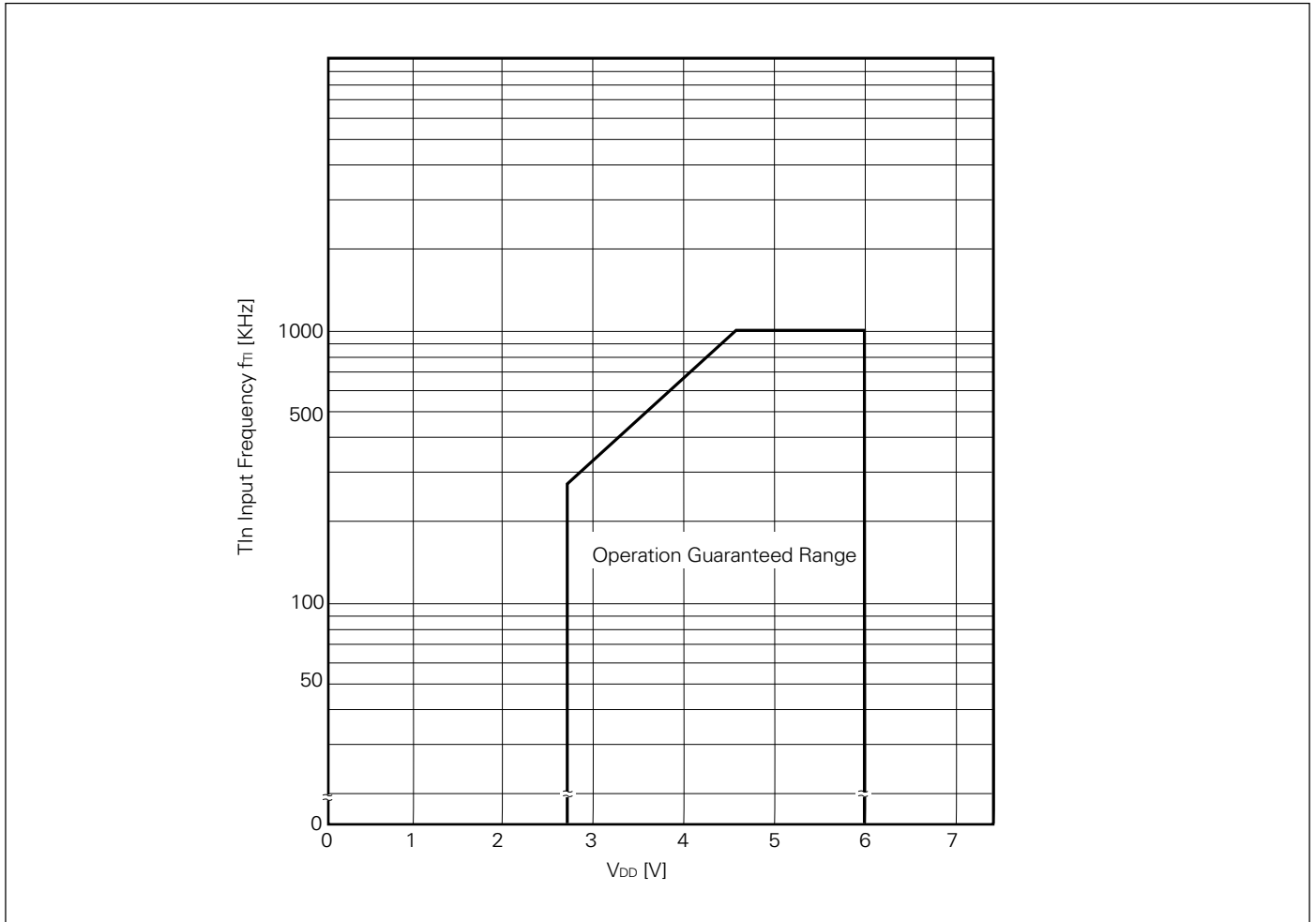


I_{DD} vs. f_x Characteristics Example (External Clock)

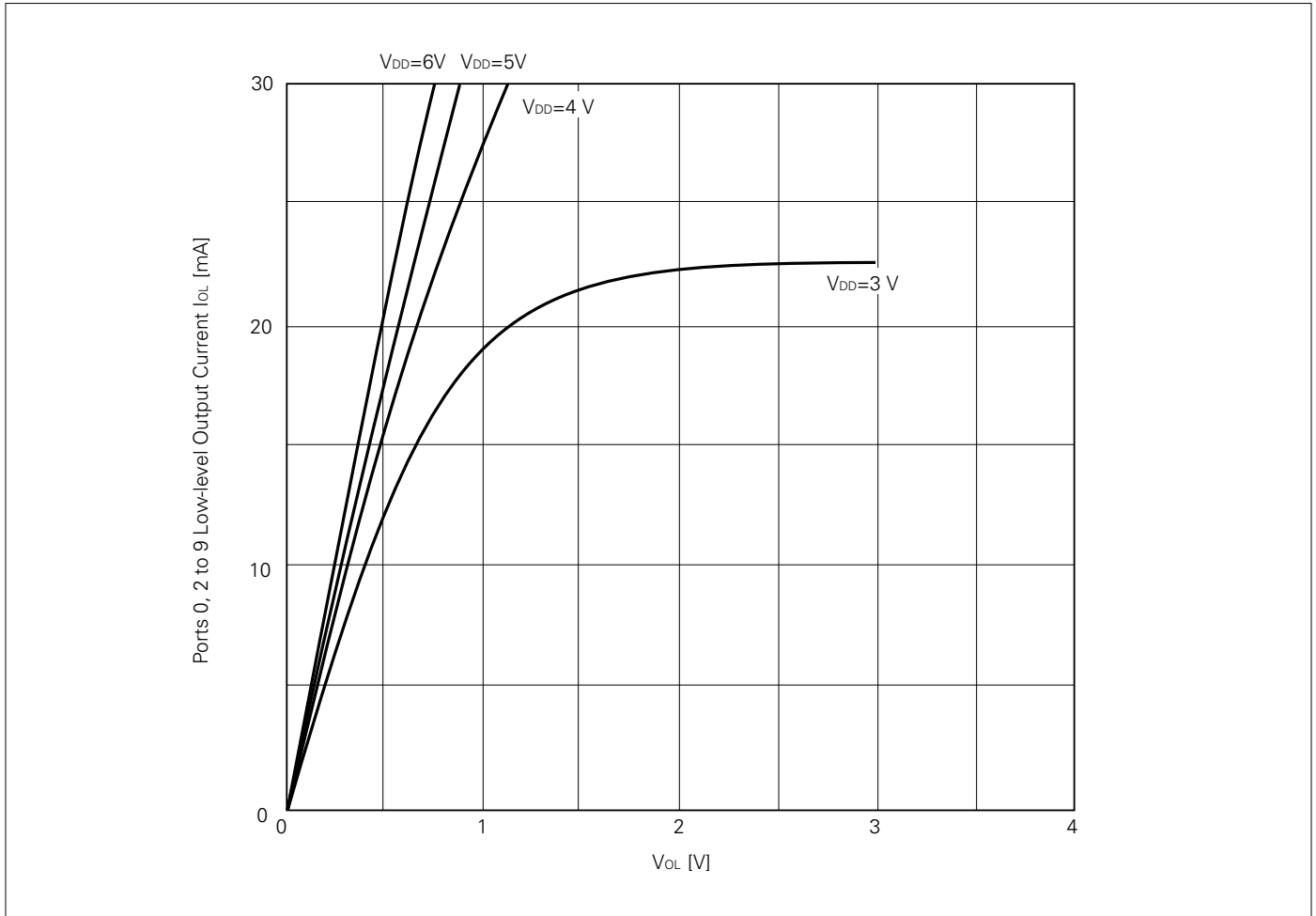


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f_{TI} vs. V_{DD} Characteristic

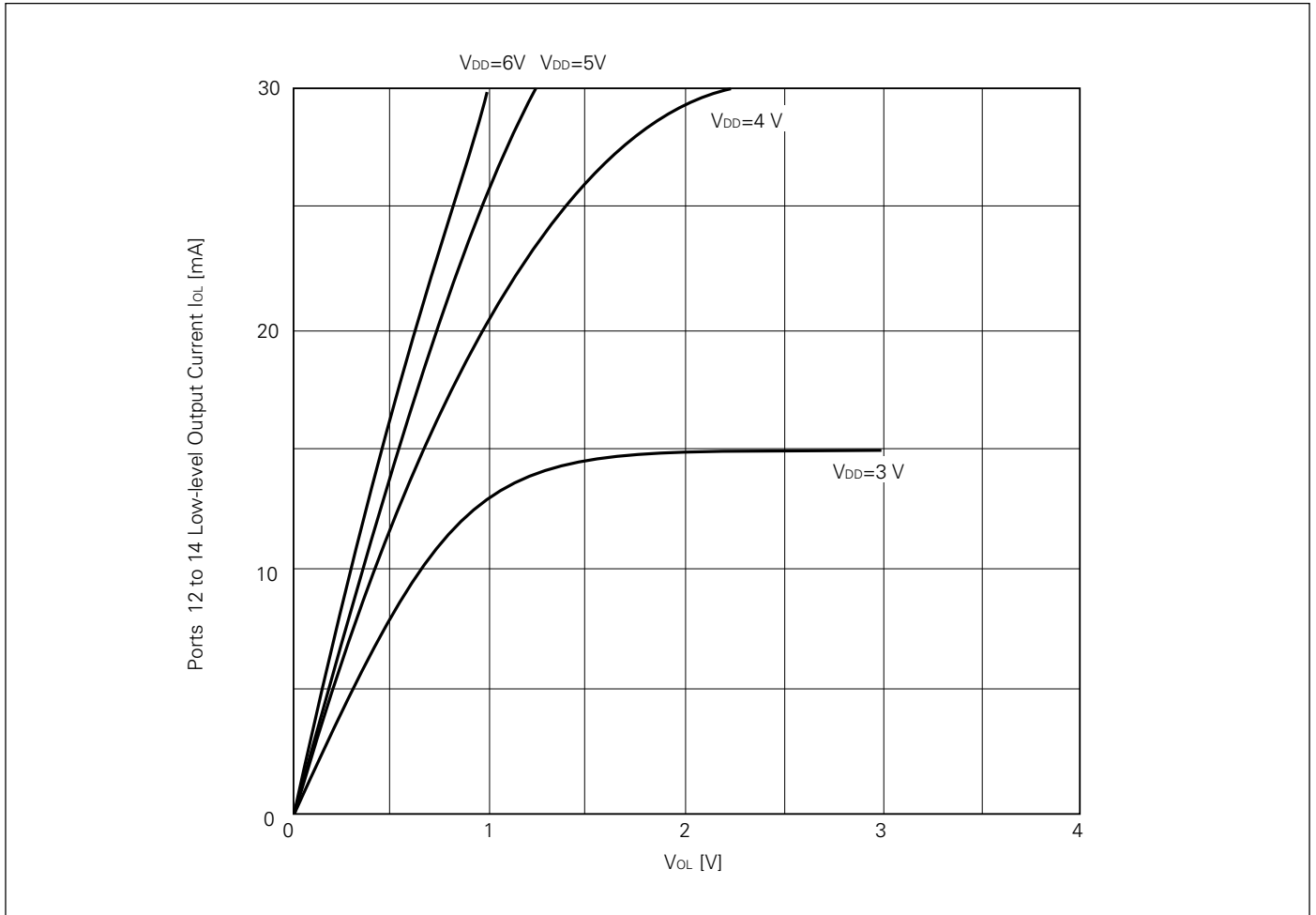


V_{OL} vs. I_{OL} (Ports 0, 2 to 9) Characteristics Example

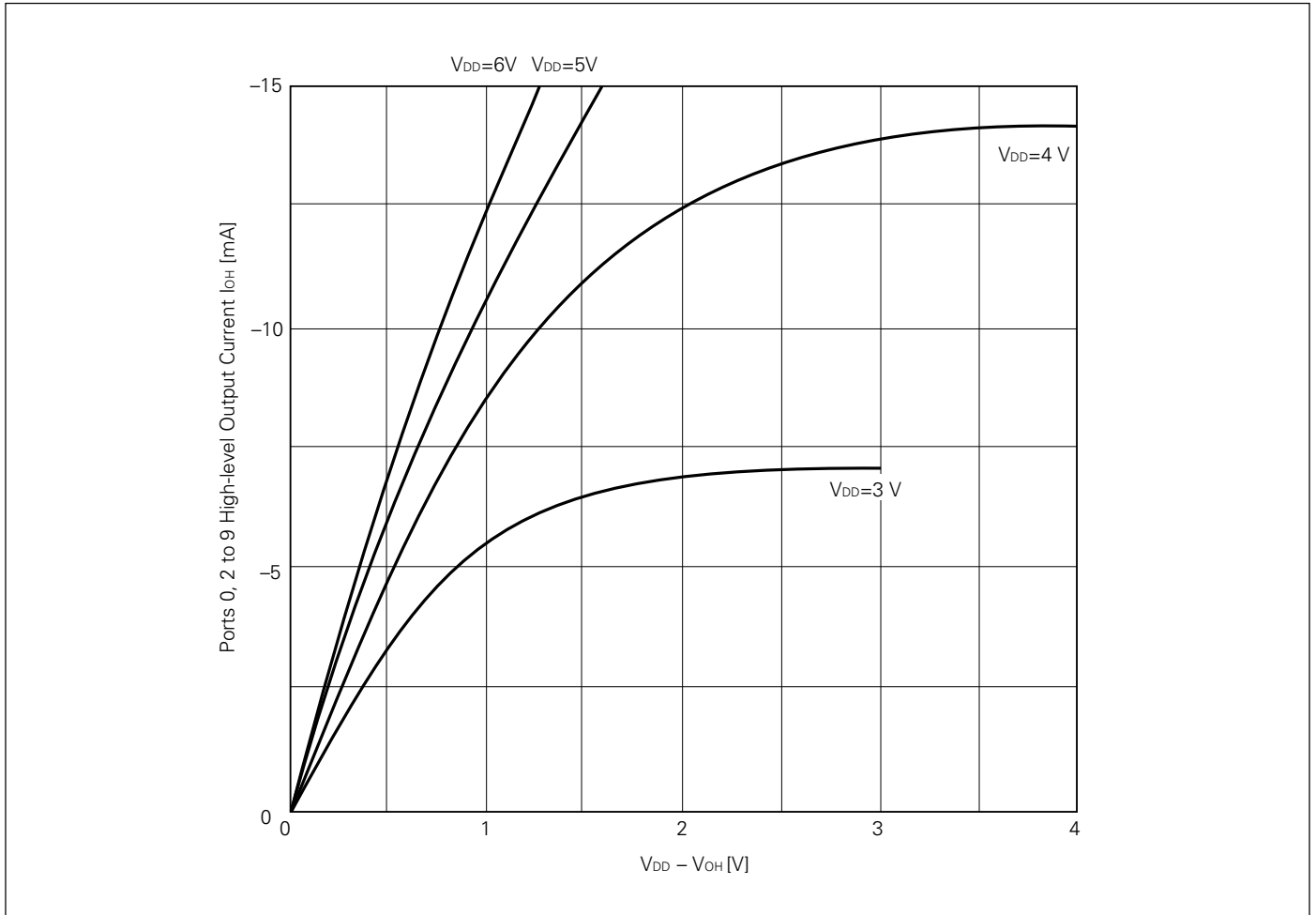


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V_{OL} vs. I_{OL} (Ports 12 to 14) Characteristics Example



V_{OH} vs. I_{OH} (Ports 0, 2 to 9) Characteristics Example

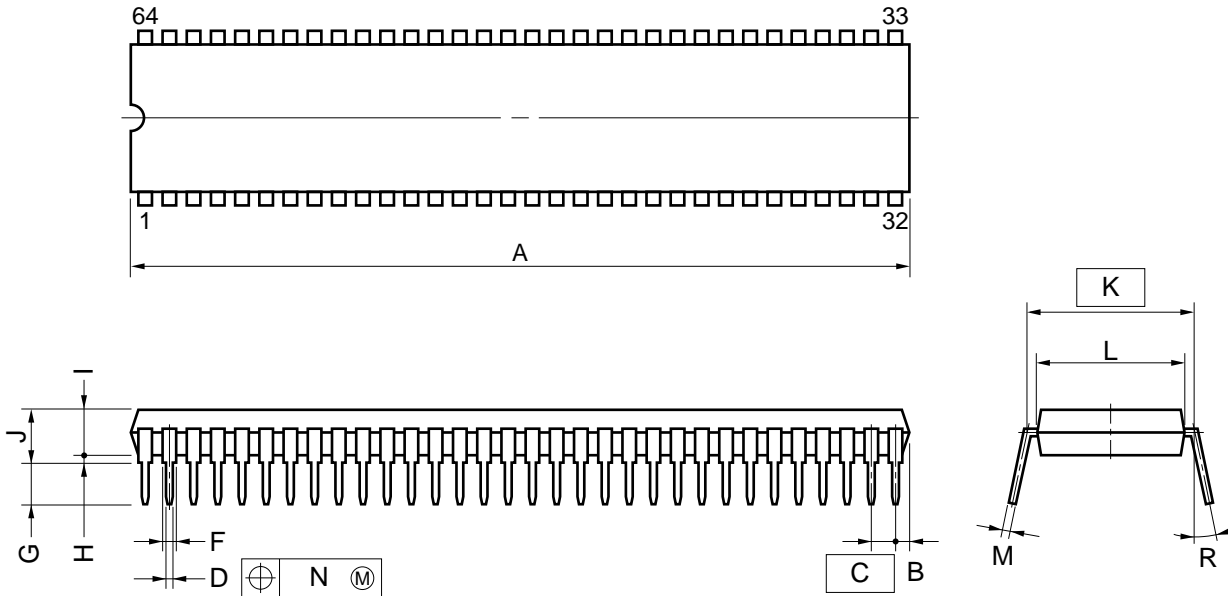


Remarks: Values for the above characteristic curves are reference values unless the guaranteed ranges are indicated.

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14. Packing Information

64 PIN PLASTIC SHRINK DIP (750 mil)



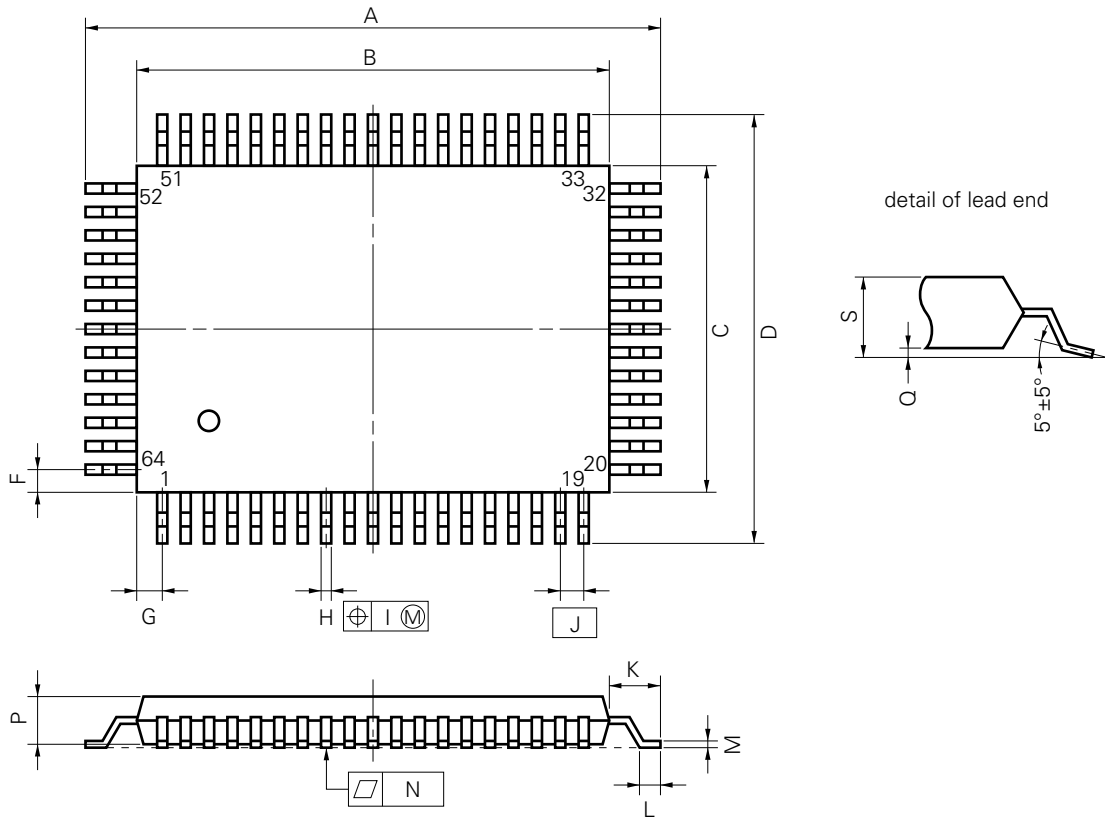
NOTE

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20) (14 × 20) (Unit: mm) ★



P64GF-100-3B8,3BE,3BR-1

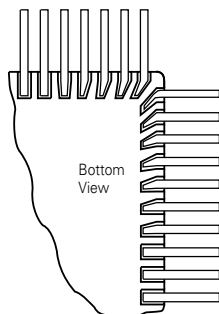
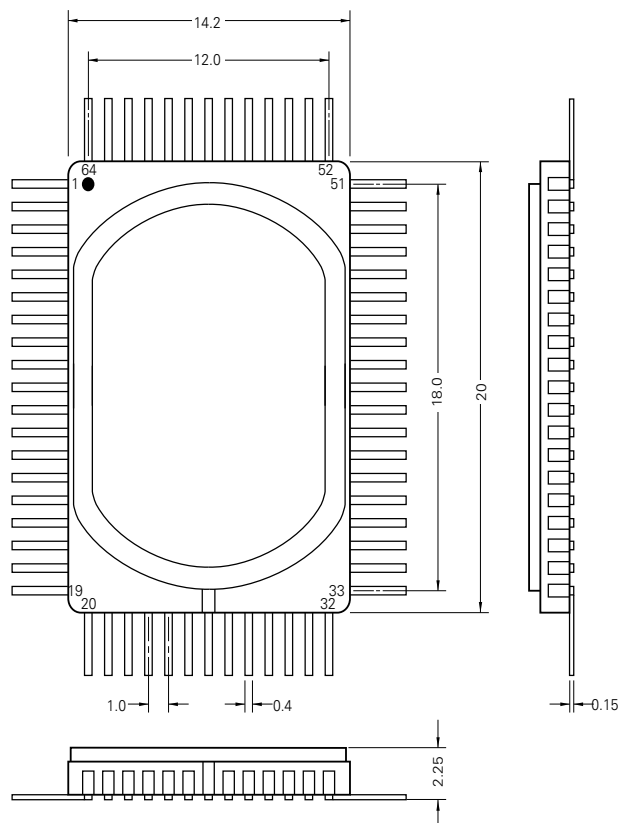
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	0.016 ^{+0.004} _{-0.005}
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

μ PD75112, 75116

64-Pin Ceramic QFP for ES (Reference Drawing) (Unit: mm)



Cautions

- 1: The metal cap is connected to pin 26 and is set to Vss (GND) level.**
- 2: The lead wire at the bottom is formed diagonally.**
- 3: Since the cutting treatment of the lead wire edge is not under process control, the lead lengths are not specified.**

15. Recommended Soldering Conditions ★

The μPD75112 and 75116 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document “**Surface Mount Technology Manual**” (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 15-1 Surface Mounting Type Soldering Conditions

μPD75112GF-xxx-3BE : 64-pin plastic QFP (14 × 20mm)

μPD75116GF-xxx-3BE : 64-pin plastic QFP (14 × 20mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 °C Duration: 30 sec. max. (at 210°C above) Number of times: Once	IR30-00-1
VPS	Package peak temperature: 215 °C Duration: 40 sec. max. (at 200°C above) Number of times: Once	VP15-00-1
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Pin part heating	Pin part temperature: 300 °C max. Duration: 3 sec. max. (per device side)	—

Note: Use more than one soldering method should be avoided (except in the case of pin part).

Table 15-2 Insertion Type Soldering Conditions

μPD75112CW-xxx: 64-pin plastic shrink DIP (750 mil)

μPD75116CW-xxx: 64-pin plastic shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (lead part only)	Solder bath temperature: 260 °C max. Duration: 10 sec. max.
Pin part heating	Pin part temperature: 260 °C max. Duration: 10 sec. max.

Note: Wave soldering is only for the lead part in order that jet solder can not contact with the chip.

Notice

A version of this product with improved recommended soldering conditions is available. For details (improvements such as infrared reflow peak temperature extension (235 °C, number of times: twice, relaxation of time limit), contact NEC sales

μPD75112, 75116

★ **APPENDIX A. Differences between μPD751×× Series Products and Related Prom Products**

Product Name		μPD75104	μPD75106	μPD75108	μPD75112	μPD75116	μPD75P108B	μPD75P116	
Item									
ROM Configuration		Mask ROM					PROM		
ROM (bit)		0000H to 0FFFH 4096 × 8	0000H to 177FH 6016 × 8	0000H to 1F7FH 8064 × 8	0000H to 2F7FH 12160 × 8	0000H to 3F7FH 16256 × 8	0000H to 1F7FH 8064 × 8	0000H to 3F7FH 16256 × 8	
RAM (bit)		320 × 4 (Bank 0: 256 × 4 Bank 1: 64 × 4)			512 × 4 (Bank 0: 256 × 4 Bank 1: 256 × 4)				
Instruction set		High end (Only μPD75104 does not incorporate BR !addr instruction).							
I/O line	Total	58							
	Input/output	<ul style="list-style-type: none"> • CMOS input/output: 32 • +12 V withstand N-ch voltage open-drain input/output: 12 (Pull-up resistor can be on-chip by mask option.) Each pin can directly drive LED: 44 					<ul style="list-style-type: none"> • CMOS input/output: 32 • +12 V withstand N-ch open-drain input/output: 12 Each pin can directly drive LED: 44 		
	Input	<ul style="list-style-type: none"> • CMOS input/output: 10 • Comparator: 4 							
Power-on reset circuit		Can be on-chip by mask option					None		
Power-on flag									
Supply voltage range		2.7 to 6.0 V					2.7 to 6.0 V	5 V±10%	
Pin functions	31 Pin (SDIP)	NC					V _{PP}		
	57 Pin (QFP)								
	33 to 36 Pins (SDIP)	P33 to P30					P33/MD3 to P30/MD0		
	59 to 62 Pins (QFP)								
Package		<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm) 					<ul style="list-style-type: none"> • 64-pin ceramic shrink DIP (with window) 		

APPENDIX B. Development Tools

The following tools are available for the development of systems for which the μPD75116 is used.

Hardware	IE-75000-R*1 IE-75001-R	75X series in-circuit emulator
	IE-75000-R-EM*2	Emulation board for IE-75000R and IE-75001-R.
	EP-75108CW-R	Emulation probe for μPD75112CW and 75116CW.
	EP-75108GF-R	Emulation probe for μPD75112GF and 75116GF. 64-pin conversion socket EV-9200G64 added.
	EV-9200G64	
	PG-1500	PROM programmer
	PA-75P108CW	μPD75P116CW PROM programmer adapter connected to PG-1500
PA-75P116GF	μPD75P116GF PROM programmer adapter connected to PG-1500	
Software	IE control program	Host machine <ul style="list-style-type: none"> • PC-9800 series (MS-DOS™ Ver. 3.30 to 5.00A*3) • IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

* 1: Maintenance product

2: Not incorporated in the IE-75001-R.

3: The task swap function, which is provided with Ver. 5.00/5.00A, is not available with this software.

Remarks: For development tools manufactured by a third party, see the "75X Series Selection Guide" (IF-151)".

★ **APPENDIX C. Related Documentations**

List of Device Related Documentations

Document Name		Document Number
User's Manual		IEM-1260
Instruction Application Table		—
Application Note	(I) Introductory Volume	IEM-1139
	(II) Remote Control Reception Volume	IEM-1281
	(III) Bar-Code Reader Volume	IEM-1265
	(IV) IC Control for MSK Transmission/Reception Volume	IEA-1278
75X Series Selection Guide		IF-1027

List of Development Tools Related Documentations

Document Name		Document Number	
Hardware	IE-75000-R/IE-75001-R User's Manual	EEU-1416	
	IE-75000-R-EM User's Manual	EEU-1294	
	EP-75108CW-R User's Manual	EEU-1308	
	EP-75108GF-R User's Manual	EEU-1318	
	PG-1500 User's Manual	EEU-1335	
Software	RA75X Assembler Package User's Manual	Operation Volume	EEU-1346
		Language Volume	EEU-1343
	PG-1500 Controller User's Manual		EEU-1291

List of Other Related Documentations

Document Name	Document Number
Package Manual	IEI-1213
Surface Mount Technology Manual	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	—
Electrostatic Discharge (ESD) Test	—
Semiconductor Devices Quality Guarantee Guide	MEI-1202
Microcomputer Related Products Guide Other Manufactures Volume	—

Note: The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Phase-out/Discontinued

NEC

μPD75112, 75116

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Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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