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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD75028

4-BIT SINGLE-CHIP MICROCOMPUTER

The μPD75028 is a 75X series 4-bit single-chip microcomputer.

The minimum instruction execution time of the μPD75028's CPU is 0.95 μs. In addition to this high-speed capability, the chip contains an A/D converter and furnishes high-performance functions such as the serial bus interface (SBI) function that follows the NEC standard format, providing powerful features and high cost performance.

A PROM version, μPD75P036, is also available. The μPD75P036 is suitable for small-scale production or experimental production in system development.

Detailed functional description for the μPD75028 is shown in the following user's manual. Be sure to read it when starting design.

μPD75028 User's Manual: IEU-

FEATURES

- Fast execution time (@4.19 MHz)
  - High speed cycle: 0.95 μs
  - Low-voltage cycles: 1.91 μs and 15.3 μs
- Power-reducing operation
  - With system clock operating at 32.768 kHz (execution time: 122 μs)
- A/D converter
  - 8-channel, 8-bit
- Low-voltage operation possible (V_{DD} = 2.7 to 6.0 V)
- Four timers
  - One of them can be used as PWM output, 16-bit counter for an integrating A/D converter, etc.
- NEC standard serial bus interface
  - SBI mode
- Very low-power clock operation: 5 μA TYP. (at 3 V in HALT mode)

APPLICATIONS

Electric home appliances, air conditioners, cameras, and electronic measuring instruments

ORDERING INFORMATION

Part number	Package	Quality grade
μPD75028CW-×××	64-pin plastic shrink DIP (750 mil)	Standard
μPD75028GC-×××-AB8	64-pin plastic QFP (□ 14 mm)	Standard

Remark ××× is a mask ROM code number.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

Document No. IC-2514B
(O.D. No. IC-7913B)
Date Published January 1994 P
Printed in Japan

The mark ★ shows major revised points.

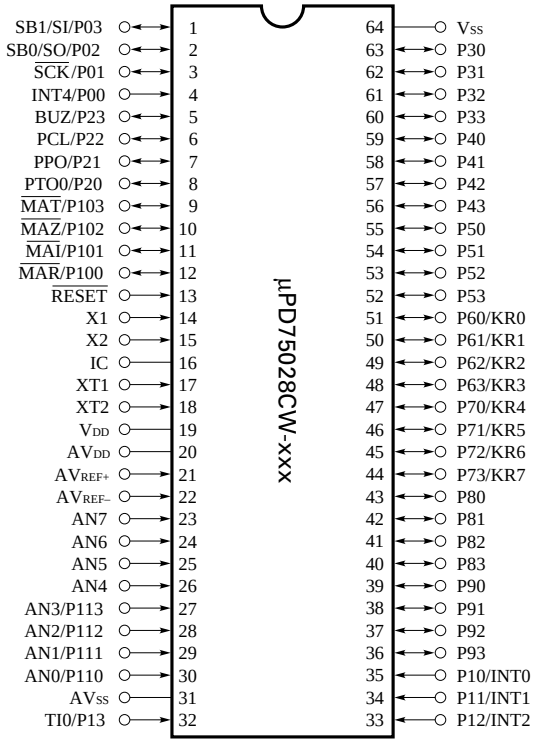
FUNCTION TABLE

Item		Function			
Instruction execution time		• 0.95, 1.91, 15.3 μs (at main system clock of 4.19 MHz) • 122 μs (at subsystem clock of 32.768 kHz)			
Internal memory	ROM	8064 × 8 bits			
	RAM	512 × 4 bits			
General registers		• 8: in 4-bit mode • 4: in 8-bit mode			
I/O ports		48	12	CMOS input pins	Selectable by software Of these, 27 can have pull-up resistors, and 4 can have pull-down resistors.
			24	CMOS I/O pins (Of these, four can directly drive LEDs.)	
			12	N-ch open-drain I/O pins (Of these, eight can directly drive LEDs.)	Break-down voltage: 10 V Mask-option pull-up resistors are available.
Timer		4 channels	• Timer/event counter • Basic interval timer : applicable to Watchdog timer • Clock timer : Capable of buzzer output • Multi-function timer		
Serial interface		• 3-wire serial I/O mode • 2-wire serial I/O mode • SBI mode			
A/D converter		8 bits (resolution) × 8 channels (successive approximation) Operable at low voltage: V_{DD} = 2.7 to 6.0 V			
Bit sequential buffer		16 bits			
Clock output function		Φ, $f_X/2^3$, $f_X/2^4$, $f_X/2^6$			
Vectored interrupts		External: 3, Internal: 4			
Test input		External: 1, Internal: 1			
System clock oscillator		• Ceramic/crystal oscillator for main system clock • Crystal oscillator for subsystem clock			
Standby function		STOP/HALT mode			
Operating ambient temperature		–40 °C +70 °C			
Operating power supply voltage		2.7 to 6.0 V			
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (□ 14 mm)			

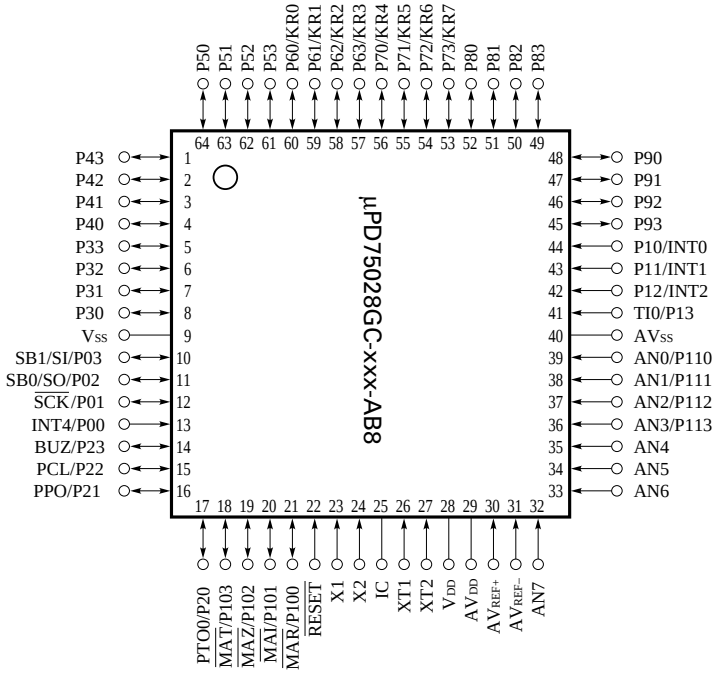
CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **64-pin plastic shrink DIP (750 mil)**



- **64-pin plastic QFP (□ 14 mm)**



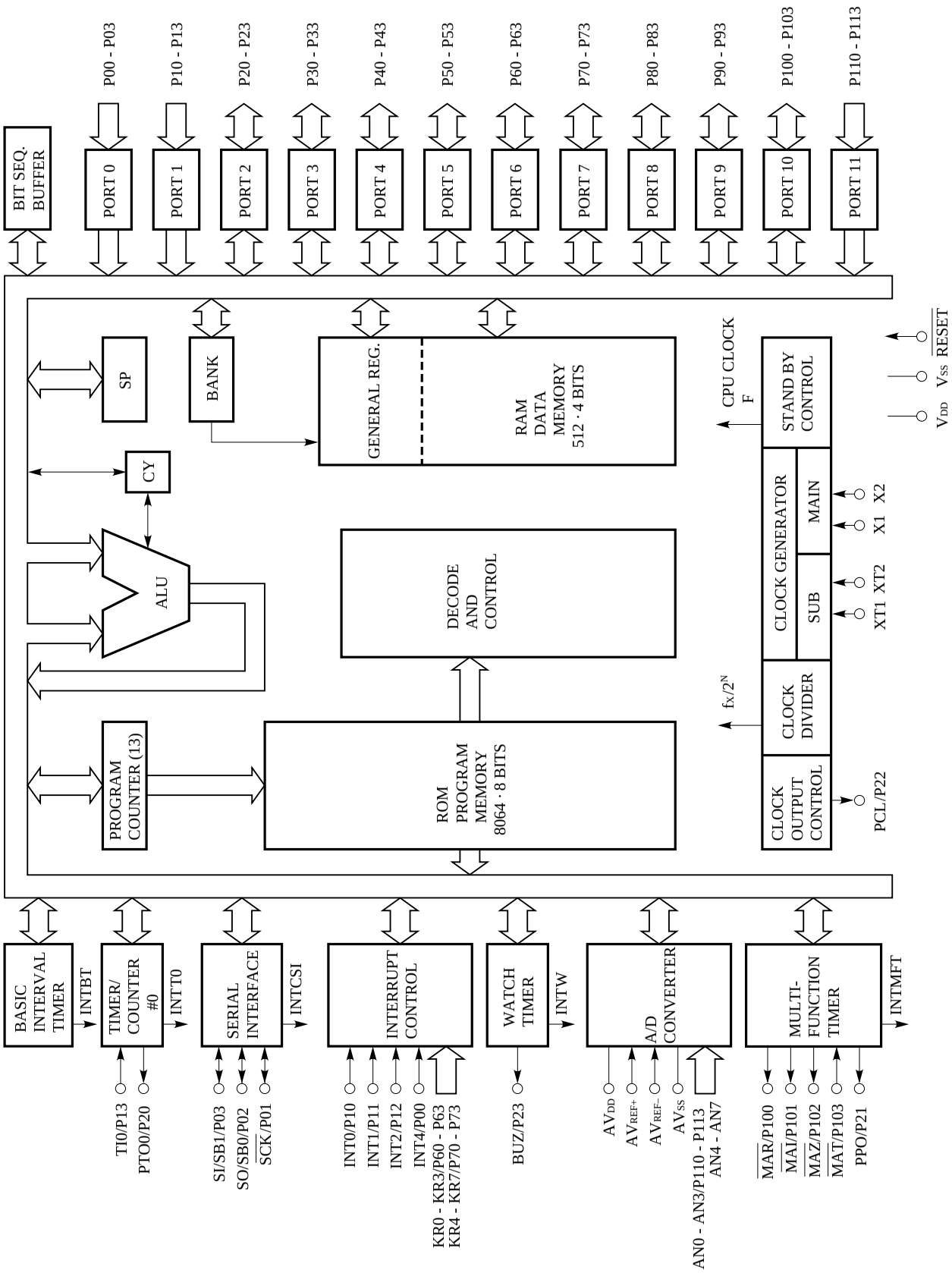
IC: Internally Connected (should be connected directly to V_{DD})

PIN NAMES

P00 - 03 : Port 0
P10 - 13 : Port 1
P20 - 23 : Port 2
P30 - 33 : Port 3
P40 - 43 : Port 4
P50 - 53 : Port 5
P60 - 63 : Port 6
P70 - 73 : Port 7
P80 - 83 : Port 8
P90 - 93 : Port 9
P100 - 103 : Port 10
P110 - 113 : Port 11
KR0 - 7 : Key Return
$\overline{SCK}$: Serial Clock
SI : Serial Input
SO : Serial Output
SB0, 1 : Serial Bus 0, 1
$\overline{RESET}$: Reset Input
TI0 : Timer Input 0
PTO0 : Programmable Timer Output 0
BUZ : Buzzer Clock
PCL : Programmable Clock
INT0, 1, 4 : External Vectored Interrupt 0, 1, 4
INT2 : External Test Input 2
X1, 2 : Main System Clock Oscillation 1, 2
XT1, 2 : Subsystem Clock Oscillation 1, 2
$\overline{MAR}$: Reference Integration Control
$\overline{MAI}$: Integration Control
$\overline{MAZ}$: Autozero Control
$\overline{MAT}$: External Comparate Timing Input
} MFT A/D mode
PPO : Programmable Pulse Output ··· MFT timer mode
AN0 - 7 : Analog Input 0 - 7
AV_{REF+} : Analog Reference (+)
AV_{REF-} : Analog Reference (–)
AV_{DD} : Analog V_{DD}
AV_{SS} : Analog V_{SS}
V_{DD} : Positive Power Supply
V_{SS} : Ground

Remark MFT: Multi-Function Timer

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin name	Input/ output	Shared pin	Function	8-bit I/O	When reset	I/O circuit type Note 1
P00	Input	INT4	4-bit input port (PORT0). For P01 - P03, pull-up resistors can be provided by software in units of 3 bits.	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ-A
P02	I/O	SO/SB0				Ⓕ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ-C
P11		INT1	4-bit input port (PORT1). Pull-up resistors can be provided by software in units of 4 bits.			
P12		INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P21		PPO				
P22		PCL				
P23		BUZ				
P30 Note 2	I/O	–	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P31 Note 2		–				
P32 Note 2		–				
P33 Note 2		–				
P40 - P43 Note 2	I/O	–	N-ch open-drain 4-bit I/O port (PORT4). A pull-up resistor can be provided for each bit (mask option). Withstand voltage is 10 V in open-drain mode.	○	High level (when pull-up resistors are provided) or high impedance	M
P50 - P53 Note 2	I/O	–	N-ch open-drain 4-bit I/O port (PORT5). A pull-up resistor can be provided for each bit (mask option). Withstand voltage is 10 V in open-drain mode.		High level (when pull-up resistors are provided) or high impedance	M

Note 1. The circle (◯) indicates the Schmitt trigger input.

2. Can directly drive LEDs.

3.1 PORT PINS (2/2)

Pin name	Input/ output	Shared pin	Function	8-bit I/O	When reset	I/O circuit type Note
P60	I/O	KR0	Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	○	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	4-bit I/O port (PORT 7). A pull-up resistor can be provided by software in units of 4 bits		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80 - P83	I/O	–	4-bit I/O port (PORT 8). A pull-up resistor can be provided by software in units of 4 bits.	×	Input	E-B
P90 - P93	I/O	–	4-bit I/O port (PORT 9). A pull-up resistor can be provided by software in units of 4 bits.		Input	E-D
P100	I/O	$\overline{MAR}$	N-ch open drain 4-bit I/O port (PORT 10). A pull-up resistor can be provided for each bit (mask option). Withstand voltage is 10 V in open-drain mode.	×	High level (when pull-up resistors are provided) or high impedance	M
P101		$\overline{MAI}$				
P102		$\overline{MAZ}$				
P103		$\overline{MAT}$				
P110	Input	AN0	4-bit input port (PORT11).		Input	Y-A
P111		AN1				
P112		AN2				
P113		AN3				

Note The circle (○) indicates the Schmitt trigger input.

3.2 NON-PORT PINS (1/2)

Pin name	Input/ output	Shared pin	Function		When reset	I/O circuit type Note 1
TI0	Input	P13	Input for receiving external event pulse signal for timer/event counter		–	Ⓑ-C
PTO0	I/O	P20	Timer/event counter output		Input	E-B
PCL	I/O	P22	Clock output		Input	E-B
BUZ	I/O	P23	Output for arbitrary frequency output (for buzzer output or system clock trimming)		Input	E-B
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	Ⓕ-A
SO/SB0	I/O	P02	Serial data output Serial bus I/O		Input	Ⓕ-B
SI/SB1	I/O	P03	Serial data input Serial bus I/O		Input	Ⓜ-C
INT4	Input	P00	Edge detection vectored interrupt input (either rising edge or falling edge detection)		–	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input (detection edge selectable)	Clock synchro-nous	–	Ⓑ-C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Asynchronous	–	Ⓑ-C
KR0 - KR3	I/O	P60 - P63	Parallel falling edge detection testable input		Input	Ⓕ-A
KR4 - KR7	I/O	P70 - P73	Parallel falling edge detection testable input		Input	Ⓕ-A
$\overline{MAR}$	I/O	P100	In MFT integrat-ing A/D converter mode	Reverse integration signal output	Note 2	M
$\overline{MAI}$	I/O	P101		Integration signal output	Note 2	M
$\overline{MAZ}$	I/O	P102		Auto-zero signal output	Note 2	M
$\overline{MAT}$	I/O	P103		Comparator input	Note 2	M
PPO	I/O	P21	In MFT timer mode	Timer pulse output	Input	E-B
AN0 - AN3	Input	P110 - P113	For A/D converter only	8-bit analog input	Input	Y-A
AN4 - AN7		–				Y
AV_{REF+}	Input	–		Reference voltage input (AV_{DD} side)	–	Z-A
AV_{REF-}	Input	–		Reference voltage input (AV_{SS} side)	–	Z-A
AV_{DD}	–	–		Positive power supply	–	–
AV_{SS}	–	–		Ground	–	–

Note 1. The circle (◯) indicates the Schmitt trigger input.

2. High level (in use of on-chip pull-up resistor) or high impedance

Remark MFT: Multi-Function Timer

3.2 NON-PORT PINS (2/2)

Pin name	Input/ output	Shared pin	Function	When reset	I/O circuit type Note
X1, X2	Input	–	Crystal/ceramic connection for main system clock generation. When external clock signal is used, it is applied to X1, and its reverse phase signal is applied to X2.	–	–
XT1, XT2	Input	–	Crystal connection for subsystem clock generation. When external clock signal is used, it is applied to XT1, and its reverse phase signal is applied to XT2, XT1 can be used as a 1-bit input (test).	–	–
$\overline{\text{RESET}}$	Input	–	System reset input	–	Ⓑ
IC	–	–	Internally connected. (To be connected to V_{DD})	–	–
V_{DD}	–	–	Positive power supply	–	–
V_{SS}	–	–	GND potential	–	–

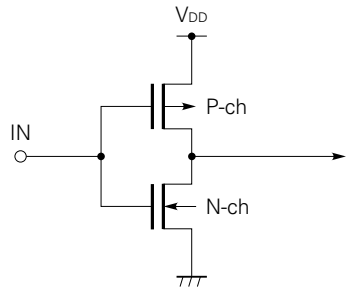
Note The circle (◯) indicates the Schmitt trigger input.

3.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuit of each μPD75028 pin is shown below in a simplified manner.

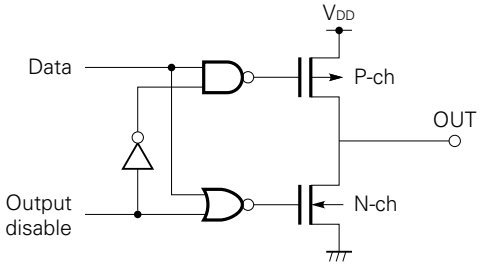
(1/3)

Type A (For type E-B)



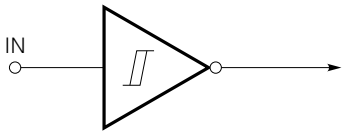
CMOS input buffer

Type D (For type E-B, F-A)



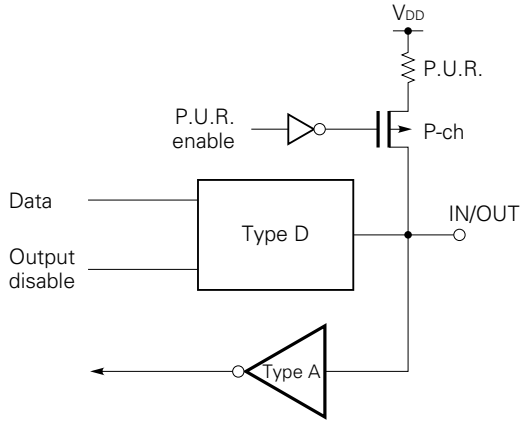
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type B



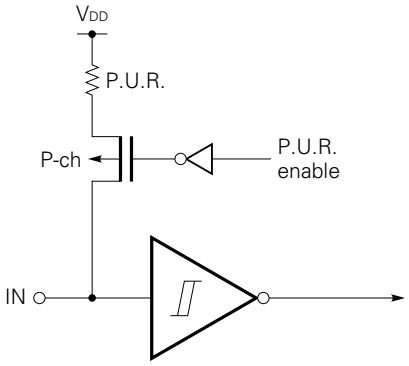
Schmitt trigger input with hysteresis

Type E-B



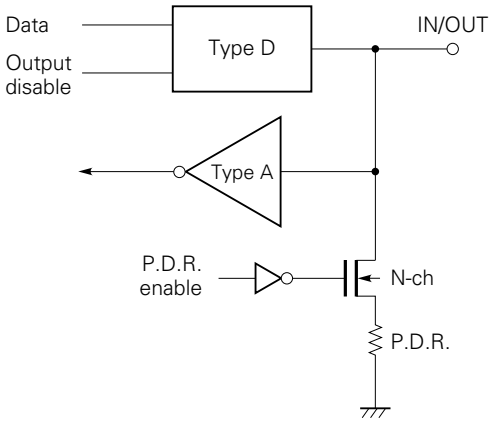
P.U.R.: Pull-Up Resistor

Type B-C



P.U.R.: Pull-Up Resistor

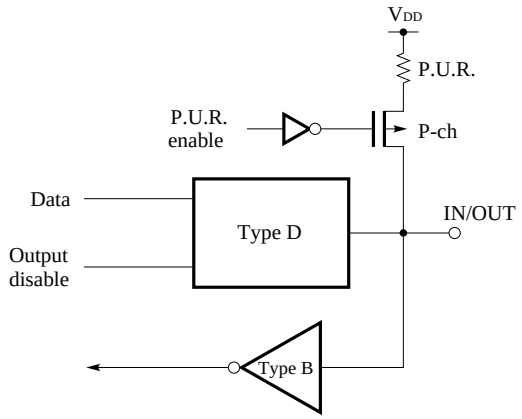
Type E-D



P.D.R.: Pull-Down Resistor

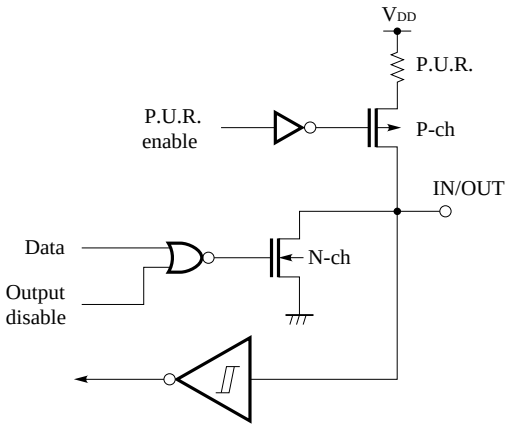
(2/3)

Type F-A



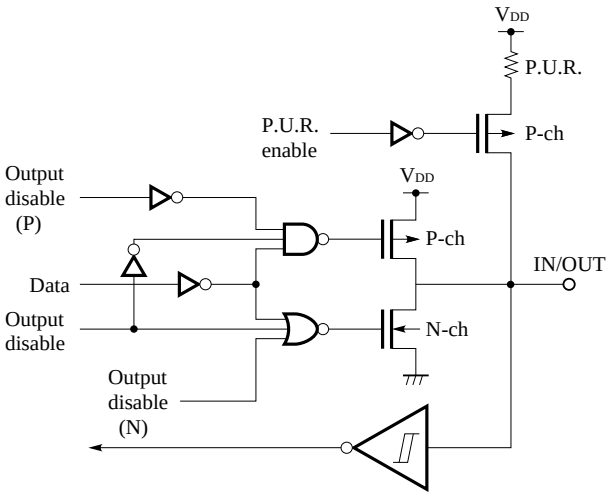
P.U.R.: Pull-Up Resistor

Type M-C



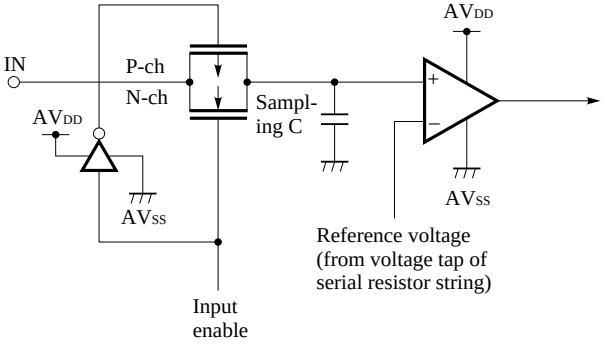
P.U.R.: Pull-Up Resistor

Type F-B

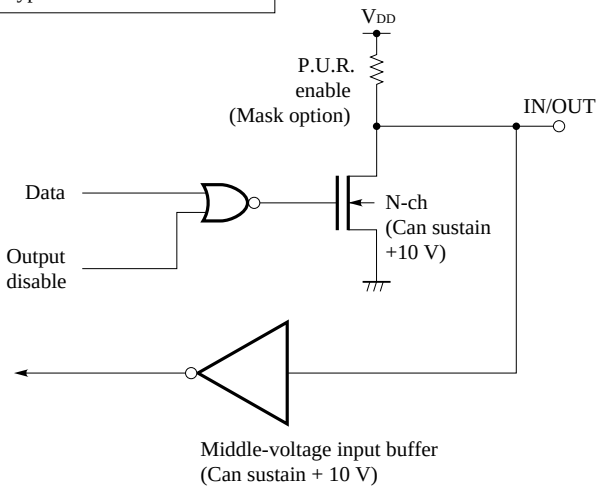


P.U.R.: Pull-Up Resistor

Type Y

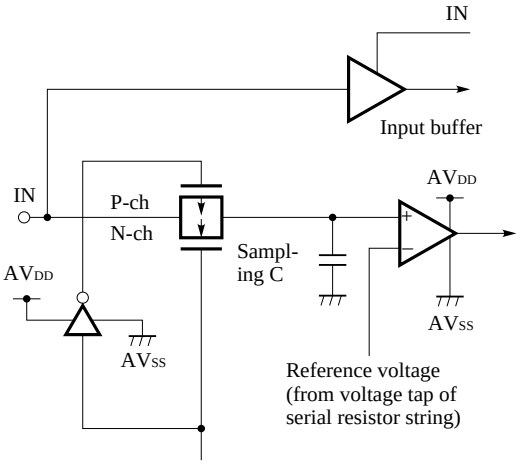


Type M

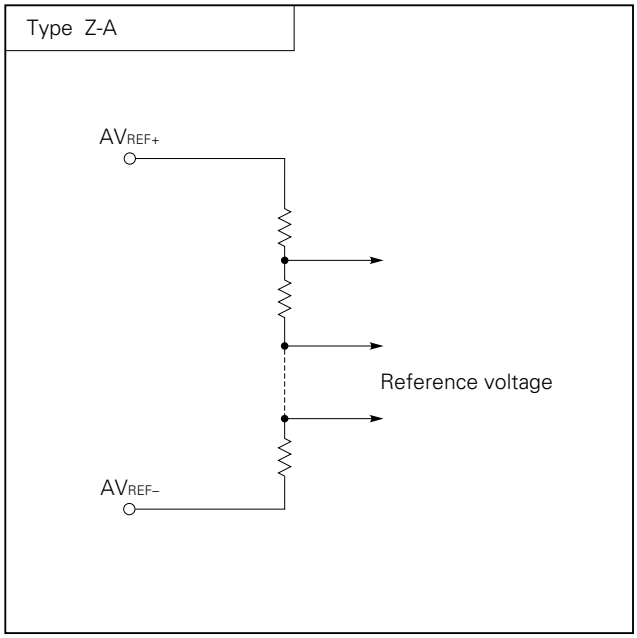


P.U.R.: Pull-Up Resistor

Type Y-A



(3/3)



3.4 MASK OPTION SELECTION

The following mask options are available for selection for each pin.

Pin name	Mask option	
P40 - P43, P50 - P53, P100 - P103	① Pull-up resistor provided (specificable bit by bit)	② Pull-up resistor not provided (specifiable bit by bit)
XT1, XT2	① Feedback resistor provided (if a subsystem clock is used)	② Feedback resistor not provided (if a subsysem clock is not used)

★ 3.5 HANDLING UNUSED PINS

Table 3-1 Handling Unused Pins

Pin name	Recommended connection
P00/INT4	Connected to V_{SS}
P01/$\overline{SCK}$	Connected to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connected to V_{SS}
P13/TI0	
P20/PTO0	Input mode : Connected to V_{SS} or V_{DD} Output mode : Left unconnected
P21	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-P53	
P60-P63	
P70-P73	
P80-P83	
P90-P93	
P100-P103	
P110/AN0-P113/AN3	Connected to V_{SS} or V_{DD}
AN4-AN7	
AV_{REF+}	Connected to V_{SS}
AV_{REF-}	
AV_{SS}	
AV_{DD}	Connected to V_{DD}
XT1	Connected to V_{SS} or V_{DD}
XT2	Left unconnected
IC	Directly connected to V_{DD}

4. MEMORY MAPPING

- Program memory (ROM) : 8064 × 8 bits (0000H-1F7FH)
  - 0000H-0001H : A vector table where a program start address is written upon resetting.
  - 0002H-000DH : A vector table where a program start address is written upon interruption.
  - 0020H-007FH : A table area referenced by GETI instruction.
- Data memory
  - Data area : 512 × 4 bits (000H-1FFH)
  - Peripheral hardware area : 128 × 4 bits (F80H-FFFH)

Fig. 4-1 Program Memory Map

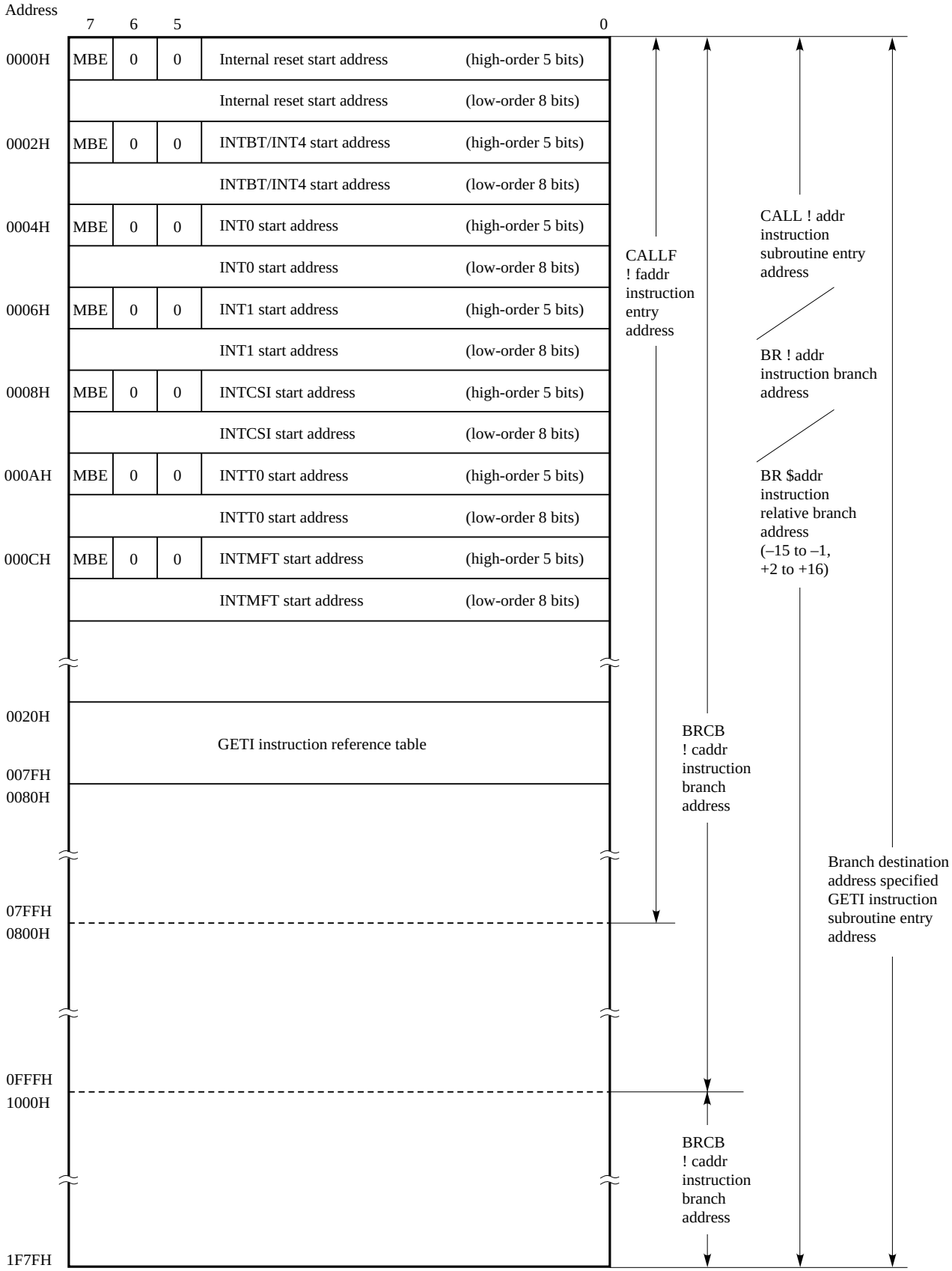
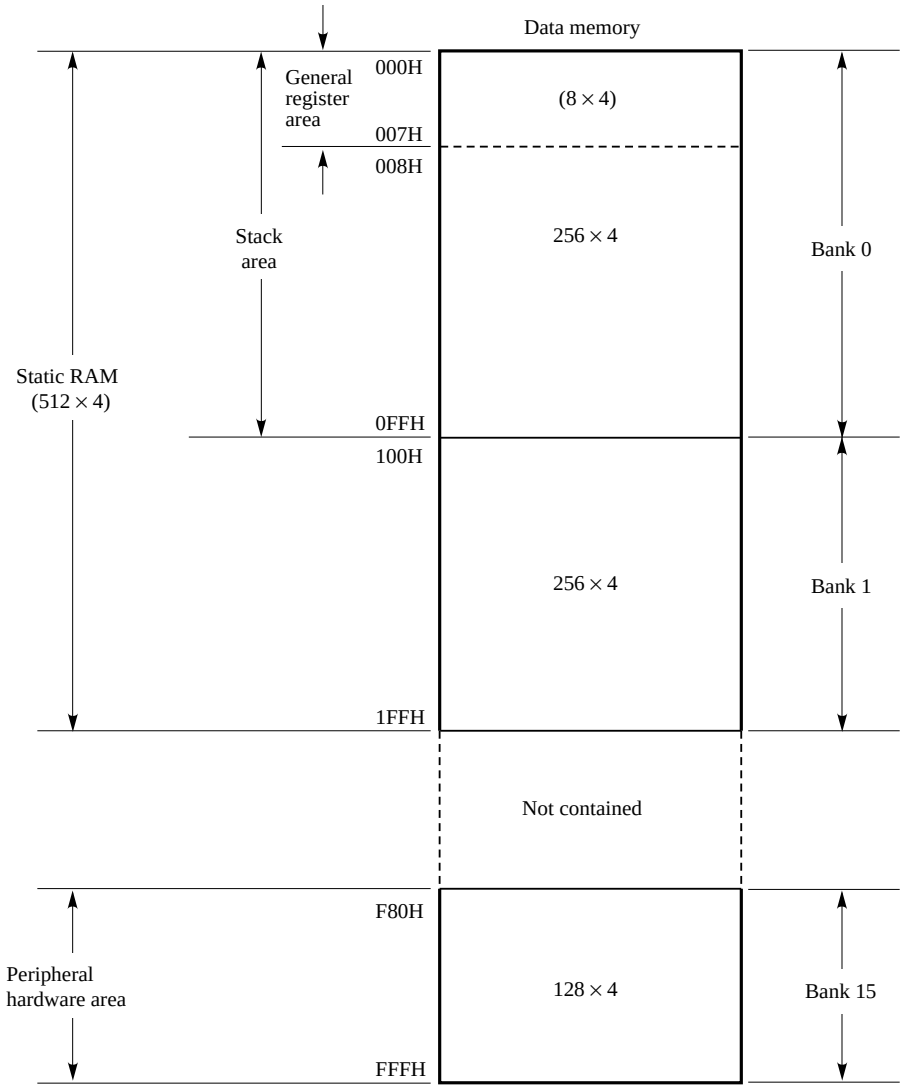


Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

There are the following three types of ports:

- CMOS input ports (port 0, 1, 11) : 12
- CMOS I/O ports (port 2, 3, 6, 7, 8, 9) : 24
- N-ch open-drain I/O ports (port 4, 5, 10) : 12

Total 48

Table 5-1 Port Functions

Port name	Function	Operation/features	Remarks
PORT0 PORT1	4-bit Input	Can be read or tested regardless of the operation mode of the shared pin.	Shared with the SO/SB0, SI/SB1, $\overline{SCK}$, INT0-2, 4, and TI0 pins.
PORT2 PORT7	4-bit I/O	Can be specified for input/output in 4-bit units. Port 6 and 7 can be paired to input/output data in 8-bit units.	Port 2 pins are also used as PTO0, PPO, PCL, and BUZ.
			Port 7 pins are also used as KR4-7.
PORT3 **Note** PORT6		Can be specified for input/output in bit units.	Port 6 pins are also used as KR0 - 3.
★ PORT4 **Note** PORT5 **Note** PORT10	4-bit I/O (N-ch open drain, can sustain 10 V)	Can be specified for input/output in 4-bit units. Port 4 and 5 can be paired to input/output data in 8-bit units.	Pull-up resistor mask-option is available for each bit.
			Port 10 pins are also used as $\overline{MAR}$, $\overline{MAI}$, $\overline{MAZ}$, and $\overline{MAT}$.
PORT8 PORT9	4-bit I/O	Can be specified for input/output in 4-bit units.	—
PORT11	4-bit Input	4-bit port dedicated to input	Port 11 is shared with pins AN0 to AN3.

Note Can directly drive LEDs.

5.2 CLOCK GENERATOR CIRCUIT

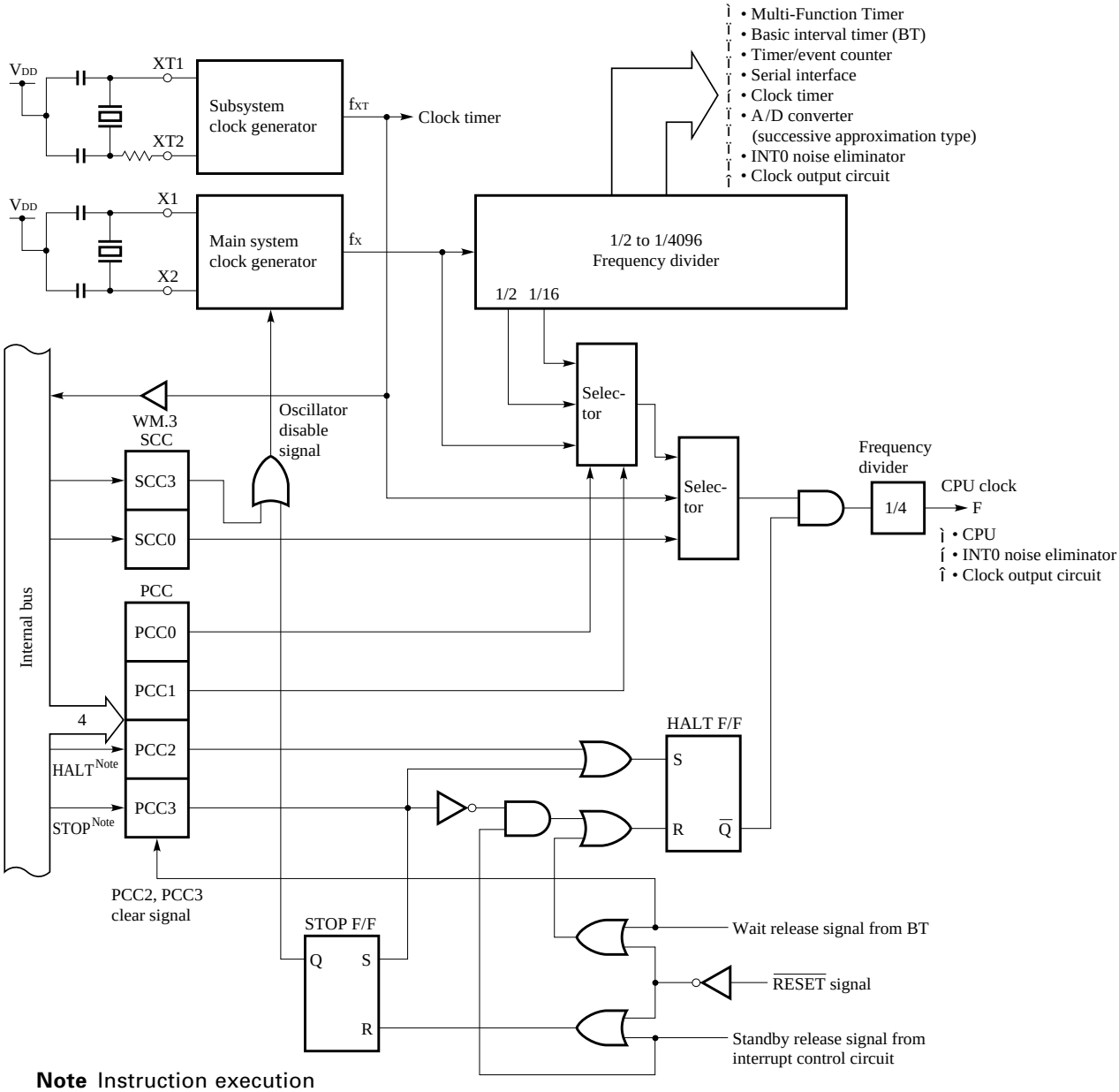
The operation of the clock generator is determined by the processor clock control register (PCC) and the system clock control register (SCC).

Two types of clock frequencies are available: main system clock and subsystem clock frequencies.

It is possible to vary the instruction execution time.

- 0.95 μs, 1.91 μs, 15.3 μs (at main system clock of 4.19 MHz)
- 122 μs (at subsystem clock of 32.768 kHz)

Fig. 5-1 Clock Generator Block Diagram



Note Instruction execution

Remarks 1. fX = Main system clock frequency

2. fXT = Subsystem clock frequency

3. PCC: Processor clock control register

4. SCC: System clock control register

5. One clock cycle of Φ (tCY) is equal to 1 machine cycle of an instruction. For the tCY, refer to **10. ELECTRICAL SPECIFICATIONS AC characteristics**.

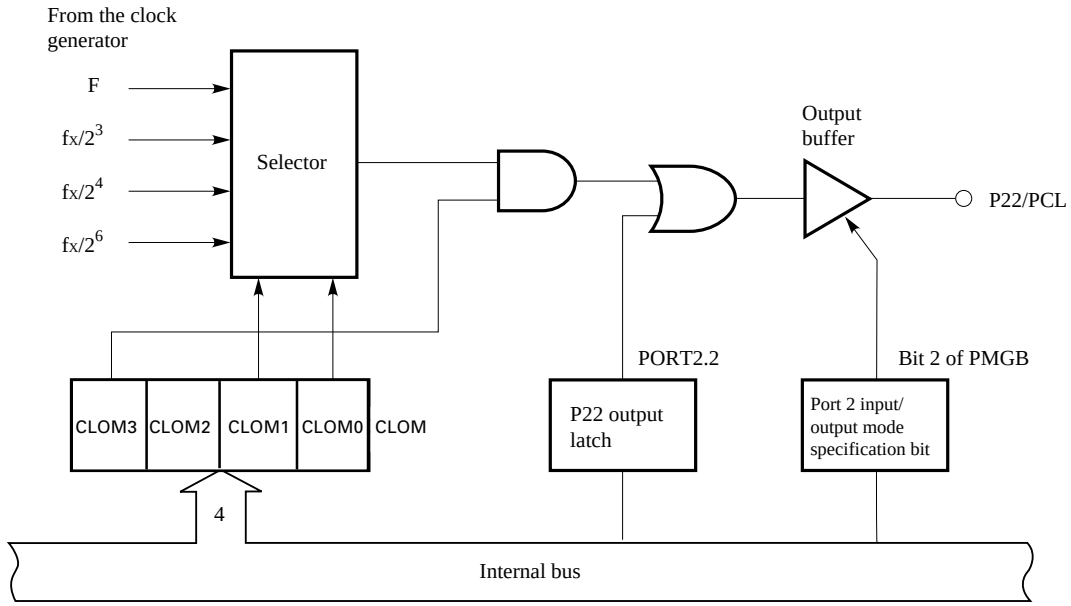
5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulses through the P22/PCL pin. It is used to output clock pulses to a remote control output or peripheral LSI.

- Clock output (PCL): Φ, 524 kHz, 262 kHz, 65.5 kHz (at fx = 4.19 MHz)

The configuration of the clock output circuit is shown below.

Fig. 5-2 Clock Output Circuit Configuration



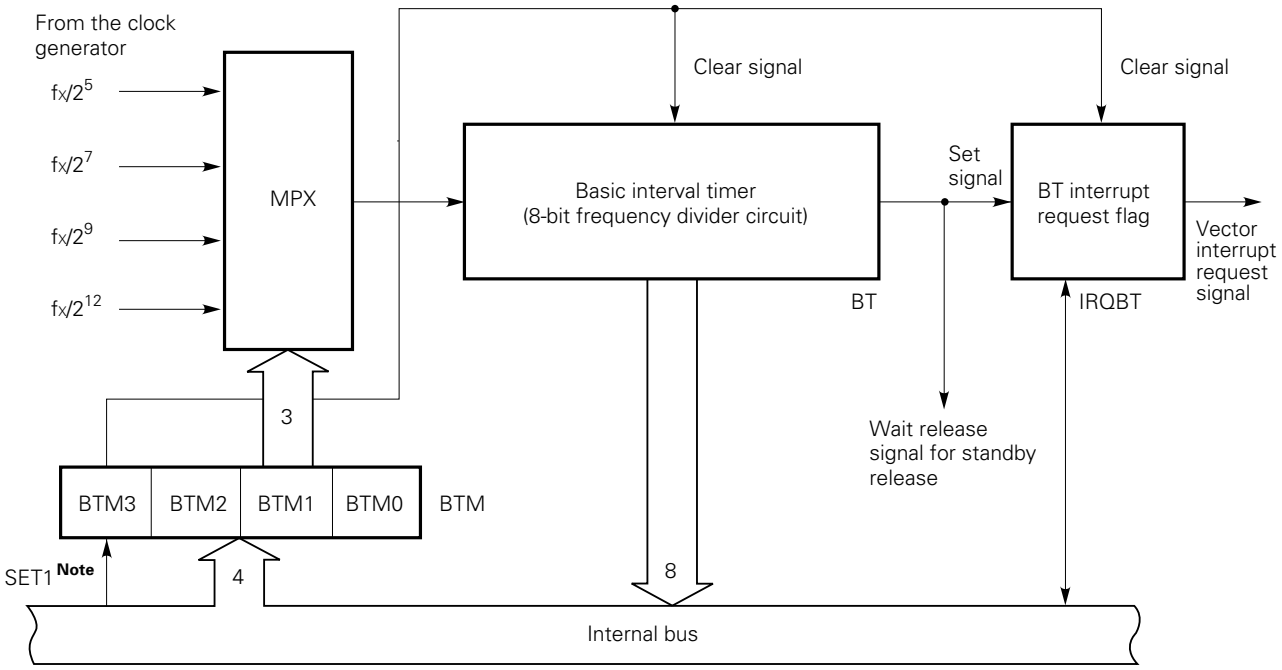
Remark Measures are taken to prevent outputting a narrow pulse when selecting clock output enable/disable.

5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference timer interrupt
- Watchdog timer application which detects a program runaway
- Selection of wait time for releasing the standby mode and counting the wait time
- Reading out the count value

Fig. 5-3 Basic Interval Timer Configuration



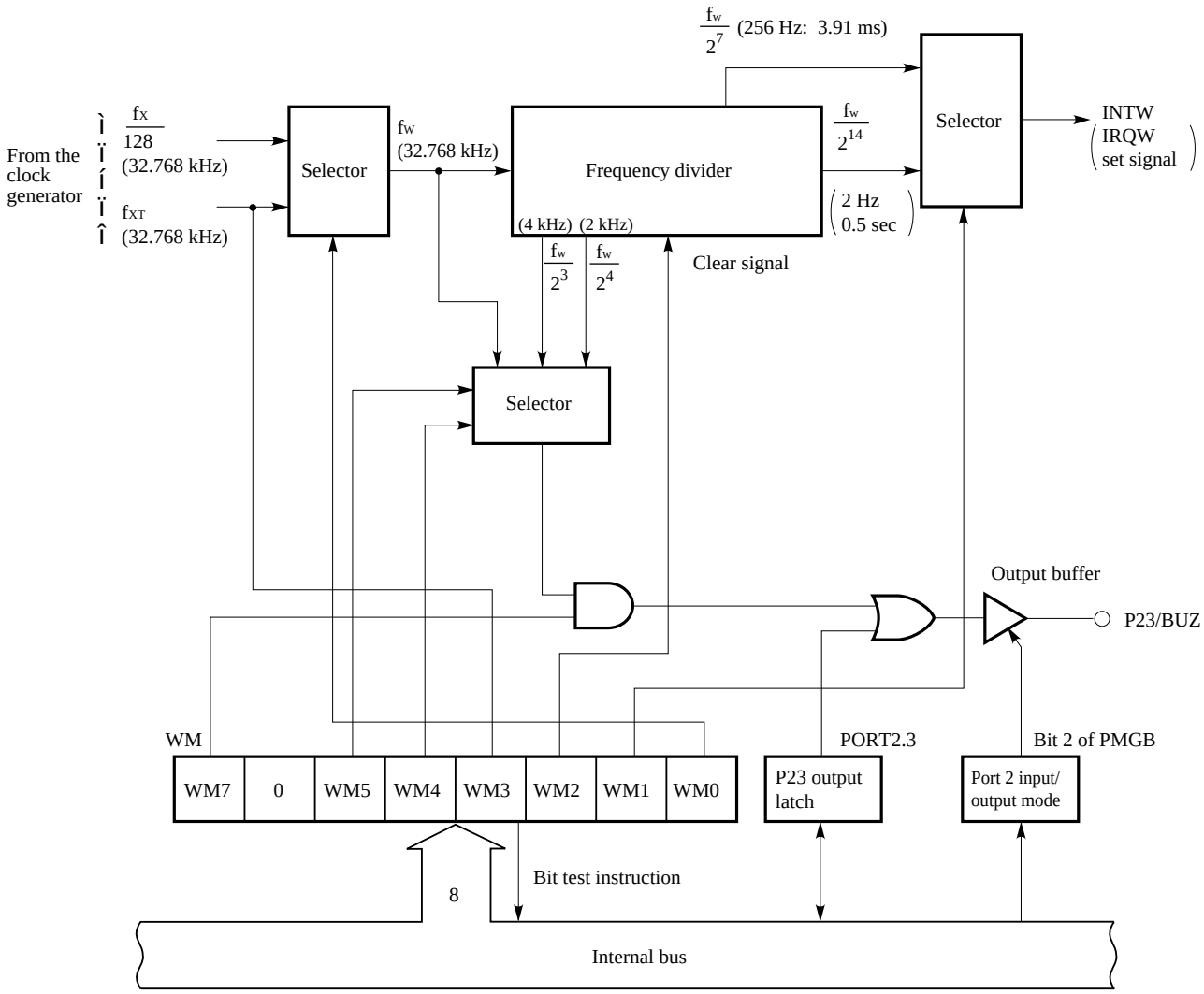
Note Instruction execution

5.5 CLOCK TIMER

The μPD75028 has a built-in 1-ch clock timer. The clock timer has the following functions:

- Sets the test flag (IRQW) with a 0.5-sec interval. The standby mode can be released by IRQW.
- The 0.5-second interval can be generated from either the main system clock or subsystem clock.
- The time interval can be made 128 times faster (3.91 ms) by selecting the fast mode. This is convenient for program debugging, testing, etc.
- Any of the frequencies 2.048 kHz, 4.096 kHz, and 32.768 kHz can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that a zero-second start of the clock can be made.

Fig. 5-4 Clock Timer Block Diagram



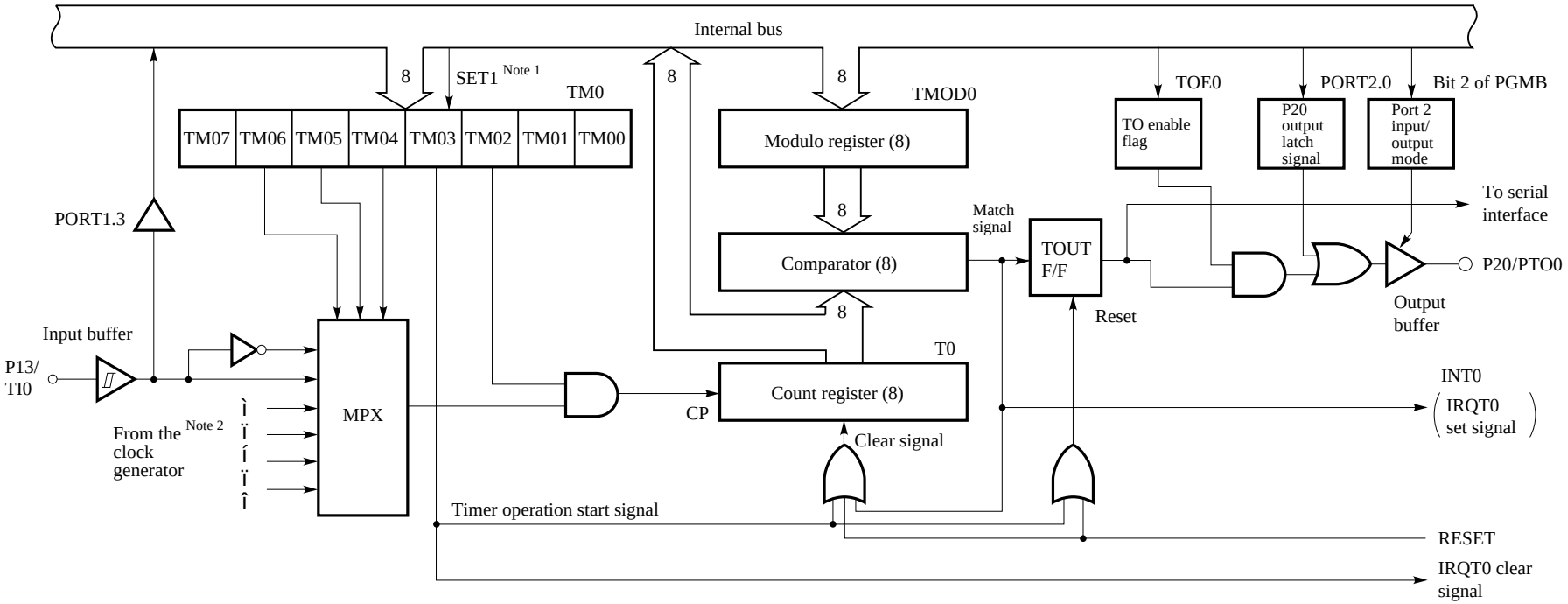
( ) is for fx = 4.194304 MHz, fXT = 32.768 kHz.

5.6 TIMER/EVENT COUNTER

The μPD75028 has a built-in 1-ch timer/event counter. The timer/event counter has the following functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin
- Event counter operation
- Divides the TI0 pin input by N and outputs to the PTO0 pin (frequency divider operation)
- Supplies serial shift clock to the serial interface circuit
- Count condition read out function

Fig. 5-5 Timer/Event Counter Block Diagram



Note 1. Instruction execution
2. For details, see Fig. 5-1.

5.7 SERIAL INTERFACE

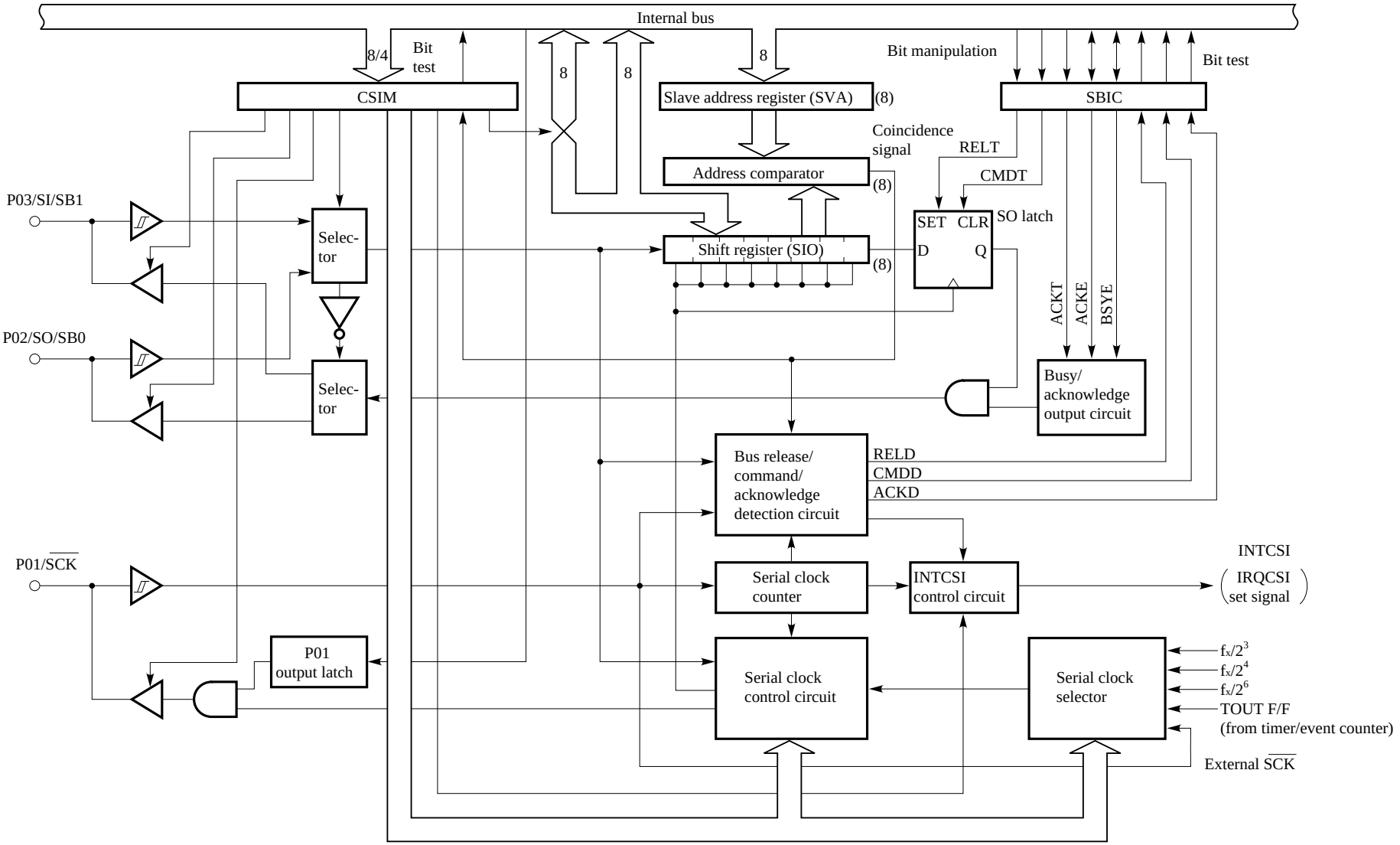
The serial interface has the following modes:

- 3-wire serial I/O mode (Start bit (MSB or LSB) switchable)
- 2-wire serial I/O mode (MSB-first)
- SBI mode (MSB-first)

In 3-wire serial I/O mode, the serial interface allows connection to 75X series, 78K series, and various I/O devices.

In 2-wire serial I/O mode and SBI mode, it allows connection to two or more devices.

Fig. 5-6 Serial Interface Block Diagram

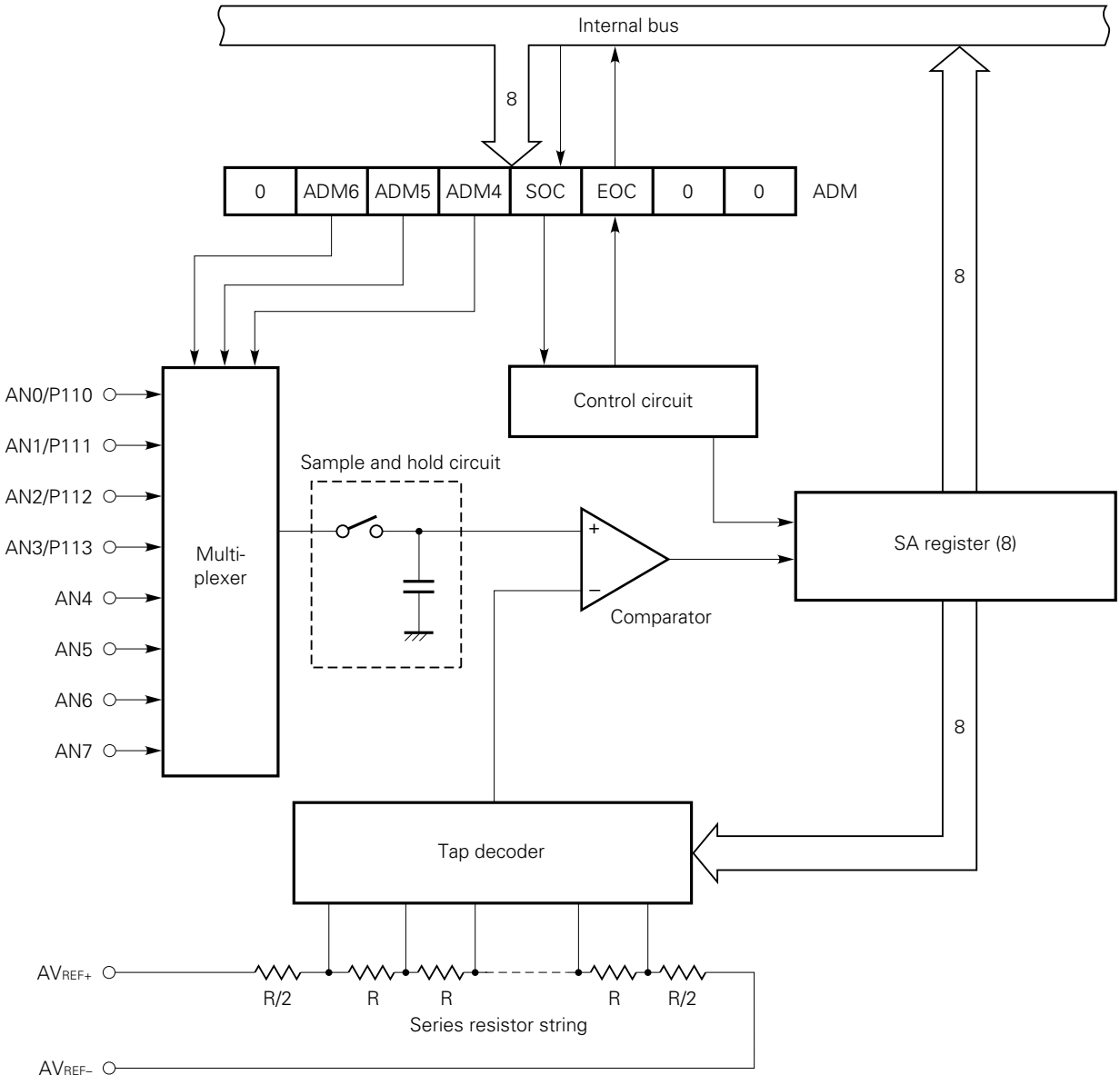


5.8 A/D CONVERTER

The μPD75028 contains an 8-bit analog/digital (A/D) converter that has eight analog input channels (AN0 - AN7).

The A/D converter employs the successive-approximation method.

Fig. 5-7 Configuration of the A/D Converter



5.9 MULTI-FUNCTION TIMER (MFT)

The μPD75028 contains one channel of the multi-function timer (MFT). MFT has the following functions:

(1) 8-bit timer mode

- Programmable interval timer operation
- Square wave output of any frequency to PPO pin

(2) PWM output mode

- Output of 6-, 7-, or 8-bit precision PWM signal to PPO pin

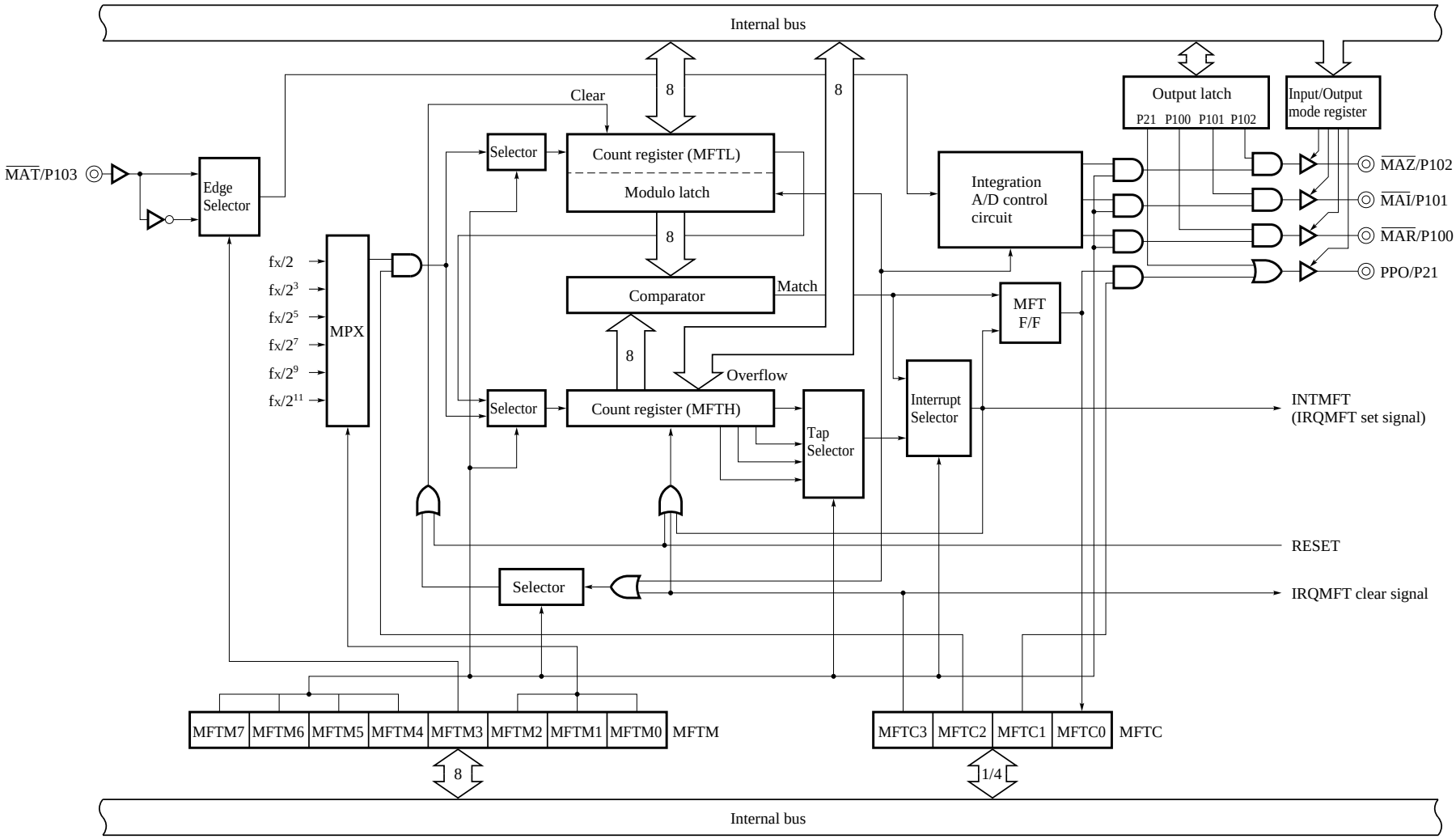
(3) 16-bit free-running timer mode

- Interval timer operation to cause an interrupt to occur at given time intervals
- Applicable as a one-shot timer

(4) Integration A/D converter mode

- Output of 16-bit integration A/D converter control signal
- 13-, 14-, 15-, or 16-bit resolution can be selected

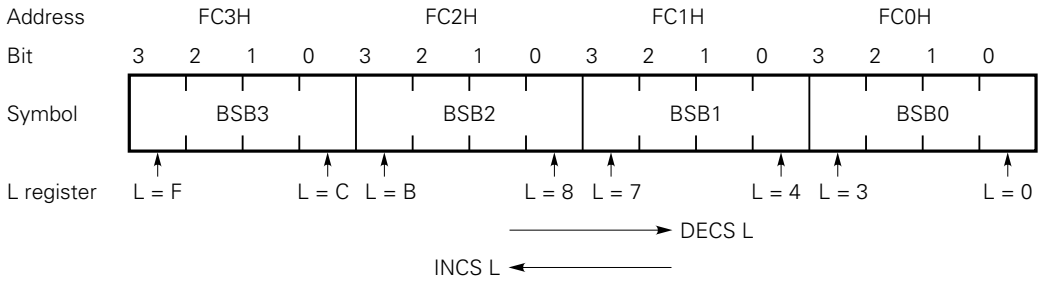
Fig. 5-8 Multi-function Timer Block Diagram



5.10 BIT SEQUENTIAL BUFFER: 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially updated by bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.

Fig. 5-9 Bit Sequential Buffer Format



Remark For pmem.@L addressing, the specification bit is shifted according to the L register.

6. INTERRUPT FUNCTIONS

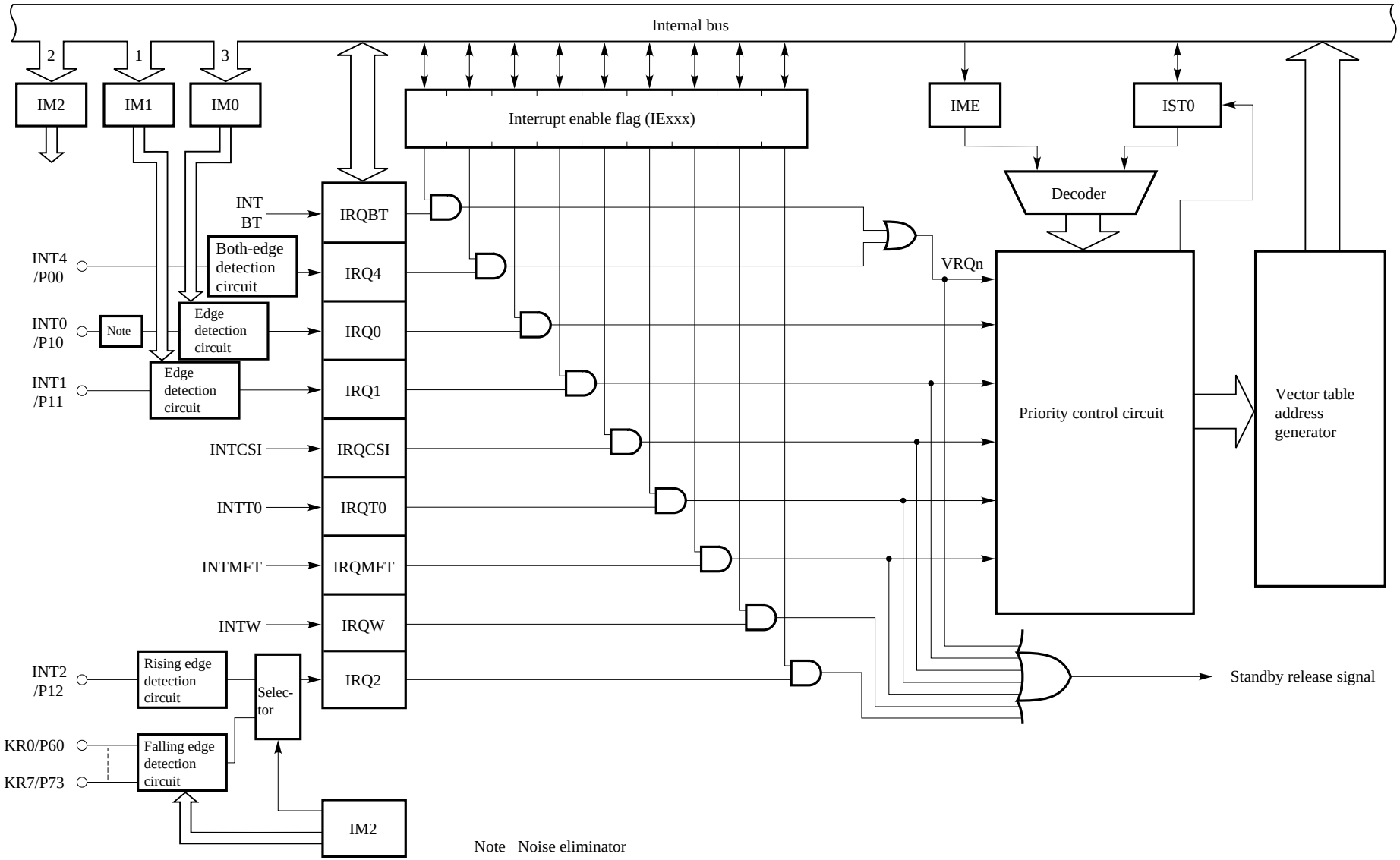
The μPD75028 has 7 different interrupt sources. In addition, multiple interrupts are possible by software control. Two types of test source are also provided. Of these, INT2 has two edge detection testable inputs.

The interrupt control circuit of the μPD75028 has the following functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt using the interrupt flag (IE×××) and interrupt master enable flag (IME).
- The interrupt start address can be set arbitrarily.
- Interrupt request flag (IRQ×××) test function (an interrupt generation can be confirmed by software).
- Standby mode release (interrupts to be released can be selected by the interrupt enable flag).

Phase-out/Discontinued

Fig. 6-1 Interrupt Control Circuit Block Diagram



Note Noise eliminator

7. STANDBY FUNCTION

The μPD75028 has two different standby modes (STOP mode and HALT mode) to reduce power dissipation while waiting for program execution.

Table 7-1 Standby Mode Statuses

		STOP mode	HALT mode
Instruction for setting		STOP instruction	HALT instruction
System clock for setting		Can be set only when operating on the main system clock	Can be set either with the main system clock or the subsystem clock
Operation status	Clock generator	Only the main system clock stops its operation	Only the CPU clock Φ stops its operation (oscillation continues)
	Basic interval timer	Does not operate	Can operate only at main system clock Φ oscillation. (IRQBT is set at reference time intervals.)
	Serial interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock	Can operate only when external $\overline{SCK}$ input is selected as the serial clock or at main system clock oscillation.
	Timer/event counter	Can operate only when the TI0 pin input is selected for the count clock	Can operate only when TI0 pin input is specified as the count clock or at main system clock oscillation.
	Clock timer	Can operate when f_{XT} is selected as the count clock	Can operate
	A/D converter	Does not operate	Can operate **Note**
	Multi-function timer	Does not operate	Can operate **Note**
	External interrupt	INT1, INT2, and INT4 can operate. Only INT0 cannot operate.	
	CPU	Does not operate	
Release signal		An interrupt request signal from hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input	An interrupt request signal from hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input

Note Operation is possible only when the main system clock operates.

8. RESET OPERATION

When the $\overline{\text{RESET}}$ signal is input, the μPD75028 is reset and all hardware is initialized as indicated in Table 8-1. Fig. 8-1 shows the reset operation timing.

Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

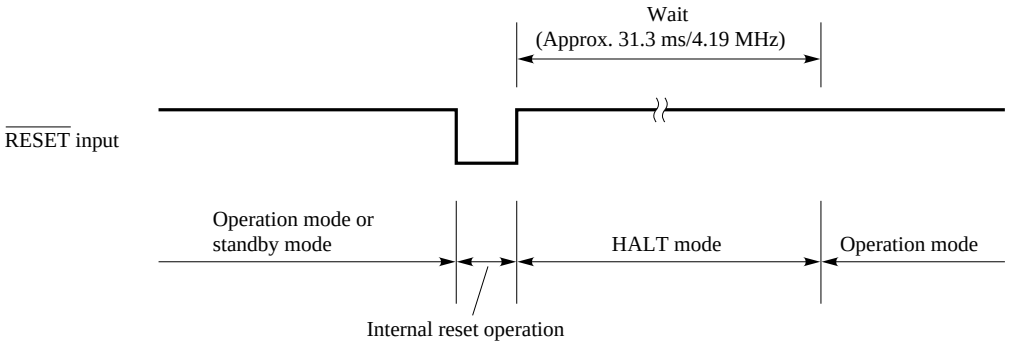


Table 8-1 Status of All Hardware after Reset (1/2)

Hardware		$\overline{\text{RESET}}$ input in standby mode	$\overline{\text{RESET}}$ input during operation
Program counter (PC)		The contents of the lower 5 bits of address 0000H of the program memory are set to PC12 - 8, and the contents of address 0001H are set to PC7 - 0.	
PSW	Carry flag (CY)	Retained	Undefined
	Skip flag (SK0-2)	0	0
	Interrupt status flag (IST0)	0	0
	Bank enable flag (MBE)	The contents of bit 7 of address 0000H of the program memory is set to MBE.	
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Retained **Note**	Undefined
General purpose register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank selection register (MBS)		0	0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Clock timer	Mode register (WM)	0	0

Note Data of address 0F8H to 0FDH of the data memory becomes undefined when the $\overline{\text{RESET}}$ signal is input.

Table 8-1 Status of All Hardware after Reset (2/2)

Hardware		$\overline{\text{RESET}}$ input in standby mode	$\overline{\text{RESET}}$ input during operation
Serial interface	Shift register (SIO)	Retained	Undefined
	Operation mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Retained	Undefined
Clock generator, Clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Interrupt function	Interrupt enable flag (IE×××)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0, 1, 2, mode register (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital port	Output buffer	Off	Off
	Output latch	Clear (0)	Clear (0)
	Input/output mode register (PMGA, B, C)	0	0
	Pull-up resistor specification register (POGA, POGB)	0	0
	Pull-down resistor specification register (PDGB)	0	0
Multi-function timer	Counter (MFTL)	FFH	FFH
	Counter (MFTH)	0	0
	Mode register (MFTM)	0	0
	Control register (MFTC)	0	0
A/D converter	Mode register (ADM)	04H	04H
	SA register (SA)	Undefined	Undefined
Bit sequential buffer (BSB0-3)		Retained	Undefined

9. INSTRUCTION SET

(1) Operand identifier and its descriptive method

The operands are described in the operand column of each instruction according to the descriptive method for the operand format of the appropriate instructions. (For details, refer to the **"RA75X Assembler Package User's Manual, Language" (EEU-xxx)**.) For descriptions in which alternatives exist, one element should be selected. Uppercase alphabetic characters and plus and minus signs are keywords; therefore, they should be described as they are.

For immediate data, the appropriate numerical values or labels should be described.

Symbols of various registers and flags can be described as labels instead of mem, fmem, pmem, and bit (For details, see "**μPD75028 User's Manual (IEU-xxxx).**").

There are restrictions to labels that can be described instead of fmem and pmem.

Identifier	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE
rpa rpa1	HL, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem[Note] bit	8-bit immediate data or label 2-bit immediate data or label
fmem pmem	FB0H - FBFH, FF0H - FFFH immediate data or label FC0H - FFFH immediate data or label
addr caddr faddr	0000H - 1F7FH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H - 7FH immediate data (however, bit 0 = 0) or label
PORTn IE××× MBn	PORT0 - PORT11 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW, IEMFT MB0, MB1, MB15

Note Only even address can be specified for mem when processing 8-bit data.

(2) Symbol definitions in operation description

A : A register; 4-bit accumulator
B : B register
C : C register
D : D register
E : E register
H : H register
L : L register
X : X register
XA : Pair register (XA); 8-bit accumulator
BC : Pair register (BC)

DE : Pair register (DE)
HL : Pair register (HL)
PC : Program counter
SP : Stack pointer
CY : Carry flag; Bit accumulator
PSW : Program status word
MBE : Memory bank enable flag
PORTn : Port n (n = 0 to 11)
IME : Interrupt master enable flag
IE××× : Interrupt enable flag
MBS : Memory bank selection register
PCC : Processor clock control register
. : Address, bit delimiter
(××) : Contents addressed by ××
××H : Hexadecimal data

(3) Symbols used for the addressing area column

*1	MB = MBE · MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0: MB = 0 (00H - 7FH) MB = 15 (80H - FFH) MBE = 1: MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H - FBFH, FF0H - FFFH	
*5	MB = 15, pmem = FC0H - FFFH	
*6	addr = 0000H - 1F7FH	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H - 0FFFH (PC_{12} = 0) or 1000H - 1F7FH (PC_{12} = 1)	
*9	faddr = 0000H - 07FFH	
*10	taddr = 0020H - 007FH	

Remarks 1. MB indicates the memory bank that can be accessed.
2. For *2, MB = 0 regardless of MBE and MBS settings.
3. For *4 and *5, MB = 15 regardless of MBE and MBS.
4. For *6 to *10, each addressable area is indicated.

(4) Description of machine cycle column

S indicates the number of machine cycles necessary for skipping any skip instruction. The value of S changes as follows:

- When no skip is performed ..... S = 0
- When a 1-byte or 2-byte instruction is skipped ..... S = 1
- When a 3-byte instruction (BR !addr, CALL !addr instruction) is skipped ..... S = 2

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle (= t_{CY}) is equivalent to one CPU clock Φ cycle. Therefore, the length of the machine cycle can be selected from three different lengths by the PCC setting.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A ← n4		String A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String A
		HL, #n8	2	2	HL ← n8		String B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
	MOVT	XA, @PCDE	1	3	XA ← $(PC_{12\text{-}8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{12\text{-}8} + XA)_{ROM}$		
Arithmetic	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Accumulator manipulation	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 1$	*5	
		@H+mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 1$	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 0$	*5	
		@H+mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 0$	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 0$	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 0$	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$ and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$ and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	$CY \leftarrow CY \wedge (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \wedge (pmem_{7-2} + L_{3-2}.bit(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow CY \wedge (H + mem_{3-0}.bit)$	*1	
	OR1	CY, fmem.bit	2	2	$CY \leftarrow CY \vee (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \vee (pmem_{7-2} + L_{3-2}.bit(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow CY \vee (H + mem_{3-0}.bit)$	*1	

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Memory bit manipulation	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∀ (H + mem_{3-0}.bit)	*1	
Branch	BR	addr	–	–	PC_{12-0} ← addr (Appropriate instructions are selected from BR !addr, BRCB !caddr, and BR $addr by the assembler.)	*6	
		!addr	3	3	PC_{12-0} ← addr	*6	
		$addr	1	2	PC_{12-0} ← addr	*7	
	BRCB	!caddr	2	2	PC_{12-0} ← PC_{12} + $caddr_{11-0}$	*8	
Subroutine stack control	CALL	!addr	3	3	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← addr, SP ← SP – 4	*6	
	CALLF	!faddr	2	2	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP–3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← 00, faddr, SP ← SP – 4	*9	
	RET		1	3	MBE, ×, ×, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4		
	RETS		1	3 + S	MBE, ×, ×, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4, then skip unconditionally		Unconditional
	RETI		1	3	MBE, ×, ×, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1)(SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← 0, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), SP ← SP + 2		
Interrupt control	EI		2	2	IME ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME ← 0		
		IE×××	2	2	IExxx ← 0		
Input/output	IN	A, PORTn	2	2	A ← PORTn (n = 0 - 11)		
		XA, PORTn	2	2	XA ← PORTn+1,PORTn (n = 4, 6)		
	OUT	PORTn, A	2	2	PORTn ← A (n = 2 - 10)		
		PORTn, XA	2	2	PORTn+1,PORTn ← XA (n = 4, 6)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		

Caution When executing the IN/OUT instruction, MBE must be set to 0 or MBE and MBS must be set to 1 and 15, respectively.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Special	SEL	MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI	taddr	1	3	• For the TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$	*10	
					• For the TCALL instruction (SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$ SP ← SP – 4		
					• For other than the TBR and TCALL instruction (taddr) (taddr + 1) is executed.		Depends on the reference instruction

10. ELECTRICAL SPECIFICATIONS

Absolute maximum ratings (T_a = 25 °C)

Parameter	Symbol	Test conditions			Ratings	Unit
Power supply voltage	V_{DD}				–0.3 to +7.0	V
Input voltage	V_{I1}	Except for port 4, 5, 10			–0.3 to V_{DD} +0.3	V
	V_{I2}	Port 4, 5, 10	Pull-up resistor is contained		–0.3 to V_{DD} +0.3	V
			Open drain		–0.3 to +11	V
Output voltage	V_O				–0.3 to V_{DD} +0.3	V
Output high current	I_{OH}	Each output pin			–10	mA
		Total			–30	mA
Output low current	I_{OL} **Note**	Port 0, 3, 4, 5 Each output pin		Peak value	30	mA
				rms value	15	mA
		Except for port 0, 3, 4, 5 Each output pin		Peak value	20	mA
				rms value	5	mA
		Port 0, 3 to 9, 11 total		Peak value	170	mA
				rms value	120	mA
		Port 0, 2, 10 total		Peak value	30	mA
				rms value	20	mA
Operation temperature	T_{opt}				–40 to +70	°C
Storage temperature	T_{stg}				–65 to +150	°C

Note To obtain the rms value, calculate

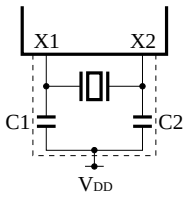
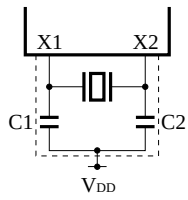
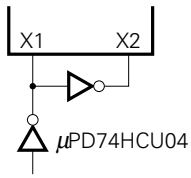
[rms value] = [peak value] × $\sqrt{\text{duty}}$

Caution If any of the ratings described above should exceed the specified absolute maximum rating even for a moment, the quality of the product would be impaired. An absolute maximum rating is a critical value that can physically damage the product. Be sure to use the product under conditions within the absolute maximum ratings.

Capacitance (T_a = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1MHz Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_O				15	pF
Input/Output capacitance	C_{IO}				15	pF

Main system clock oscillator characteristics (T_a = −40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constants	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = oscillator operating voltage range	2.0		5.0 Note 3	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches the minimum oscillator operating voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		2.0	4.19	5.0 Note 3	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) Note 1		2.0		5.0 Note 3	MHz
		X1 input high- and low-level width (t_{XH}, t_{XL})		100		250	ns

Note 1. Indicates only the characteristics of the oscillator. For instruction execution time, see "AC Characteristics."

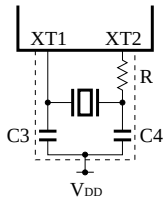
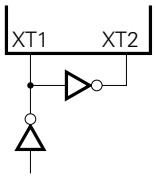
2. Time required for stabilization of oscillation after application of V_{DD} or after cancellation of STOP mode.

★ **3.** If the oscillation frequency is 4.19 MHz < f_X ≤ 5.0 MHz, do not select PCC = 0011 as instruction execution time. If it is selected, one machine cycle would become shorter than 0.95 μs, and the minimum limit of 0.95 μs could not be secured.

★ **Caution In use of the main system clock oscillator, follow the following guidlines for wiring on the portion indicated by " " in the figure to avoid influence due to line capacitance:**

- **Route as short as possible.**
- **Do not let the wiring cross another signal line.**
- **Do not place the wiring near a line in which a variable high current flows.**
- **Be sure that the potential on the connection point for the oscillator capacitor is always equal to V_{DD}. Do not connect the wire in question to a power supply pattern in which a high current flows.**
- **Do not take off signal from the oscillator.**

Subsystem clock oscillator characteristics (T_a = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constants	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high- and low-level width (t_{XTH}, t_{XTL})		5		15	μs

Note 1. Indicates only the characteristics of the oscillator. For instruction execution time, see "AC Characteristics."

2. Time required for stabilization of oscillation after application of V_{DD}.

Caution In use of the subsystem clock oscillator, follow the following guidlines for wiring on the portion indicated by " " in the figure to avoid influence due to line capacitance: ★

- **Route as short as possible wire.**
- **Do not let the wiring cross another signal line.**
- **Do not place the wiring near a line in which a variable high current flows.**
- **Be sure that the potential on the connection point for the oscillator capacitor is always equal to V_{DD}. Do not connect the wire in question to a power supply pattern in which a high current flows.**
- **Do not take off signal from the oscillator.**

For reduction of current consumption, the subsystem clock oscillator has a low amplification factor. It is more likely to have a malfunction due to noise than the main system clock oscillator. When the subsystem clock is to be used, pay special attention in selecting the method of wiring.

★ **Recommended oscillator constants**

Main system clock: Ceramic (T_a = –40 to +85 °C)

Manufacturer	Product	Frequency (MHz)	Recommended circuit constant		Oscillation voltage range	
			C1 (pF)	C2 (PF)	MIN. (V)	MAX. (V)
Murata	CSA X.XXMG Note	2.00 to 2.44	30	30	3.0	6.0
	CST X.XXMG Note		—	—		
	CSA X.XXMG Note	2.45 to 4.49	30	30	3.5	
	CST X.XXMGW Note		—	—		
	CSA X.XXMG Note	4.50 to 5.00	30	30	4.0	
	CST X.XXMGW Note		—	—		
Kyocera	KBR-1000H	1.00	100	100	2.7	6.0
	KBR-2.0MS	2.00	47	47		
	KBR-4.0MSA	4.00	33	33		
	KBR-5.0MSA	5.00	33	33		

Note X.XX indicates a frequency.

Subsystem clock: Crystal (T_a = –15 to +60 °C)

Manufacturer	Product	Frequency (kHz)	Recommended circuit constant			Oscillation voltage range	
			C3 (pF)	C4 (pF)	R (kΩ)	MIN. (V)	MAX. (V)
Kyocera	KF-38G	32.768	18	33	150	2.7	6.0

DC characteristics (T_a = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH1}	Port 2, 3, 8, 9, 11		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Port 0, 1, 6, 7, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Port 4, 5, 10	Pull-up resistor is contained	0.7 V_{DD}		V_{DD}	V
			Open drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD} – 0.5		V_{DD}	V
Input low voltage	V_{IL1}	Port 2 to 5, 8 to 11		0		0.3 V_{DD}	V
	V_{IL2}	Port 0, 1, 6, 7, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1, XT2		0		0.4	V
Output high voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output low voltage	V_{OL}	Port 3, 4, 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0, 1	Open drain Pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
Input high leakage current	I_{LIH1}	V_I = V_{DD}	Except for below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_I = 9 V	Port 4, 5, 10 (when open drain is selected)			20	μA
Input low leakage current	I_{LIL1}	V_I = 0 V	Except for below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output high leakage current	I_{LOH1}	V_O = V_{DD}	Except for below			3	μA
	I_{LOH2}	V_O = 9 V	Port 4, 5, 10 (when open drain is selected)			20	μA
Output low leakage current	I_{LOL}	V_O = 0 V				–3	μA
Internal pull-up resistor	R_{U1}	Port 0, 1, 2, 3, 6, 7, 8 (except P00) V_I = 0 V	V_{DD} = 5.0 V ±10 %	15	40	80	kΩ
			V_{DD} = 3.0 V ±10 %	30		300	kΩ
	R_{U2}	Port 4, 5, 10 V_O = V_{DD} –2.0 V	V_{DD} = 5.0 V ±10 %	15	40	70	kΩ
			V_{DD} = 3.0 V ±10 %	10		60	kΩ
Internal pull-down resistor	R_D	Port 9 V_{IN} = V_{DD}	V_{DD} = 5.0 V ±10 %	10	40	70	kΩ
			V_{DD} = 3.0 V ±10 %	10		60	kΩ

Parameter	Symbol	Test conditions			MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	4.19 MHz Note 2 crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10 % Note 3			2.5	8	mA
			V_{DD} = 3 V ± 10 % Note 4			0.35	1.2	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10 %		500	1500	μA
				V_{DD} = 3 V ±10 %		150	450	μA
	I_{DD3}	32.768 Note 5 kHz crystal oscillation		V_{DD} = 3 V ±10 %		30	90	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10 %		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode		V_{DD} = 5 V ±10 %		0.5	20	μA
			V_{DD} = 3 V ±10 %			0.1	10	μA
				T_a = 25 °C		0.1	5	μA

Note 1. Current flowing into internal pull-up resistor is not contained.

2. Case where subsystem clock is oscillated is also contained.

3. When the processor clock control register (PCC) is set to 0011 and the μPD75028 is operated in high speed mode.

4. When PCC is set to 0000 and the μPD75028 is operated in low speed mode.

5. When the system clock control register (SCC) is set to 1001, main system clock oscillation is stopped and the μPD75028 is operated with subsystem clock.

AC characteristics (T_a = –40 to +70 ˚C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time (minimum instruction execution time = 1 machine cycle) **Note 1**	t_{CY}	Operation with main system clock	V_{DD} = 4.5 to 6.0 V	0.95		32	μs
				3.8		32	μs
		Operation with subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input high, low level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high, low level width	t_{INTH}, t_{INTL}	INT0		**Note 2**			μs
		INT1, 2, 4		10			μs
		KR0 to 7		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

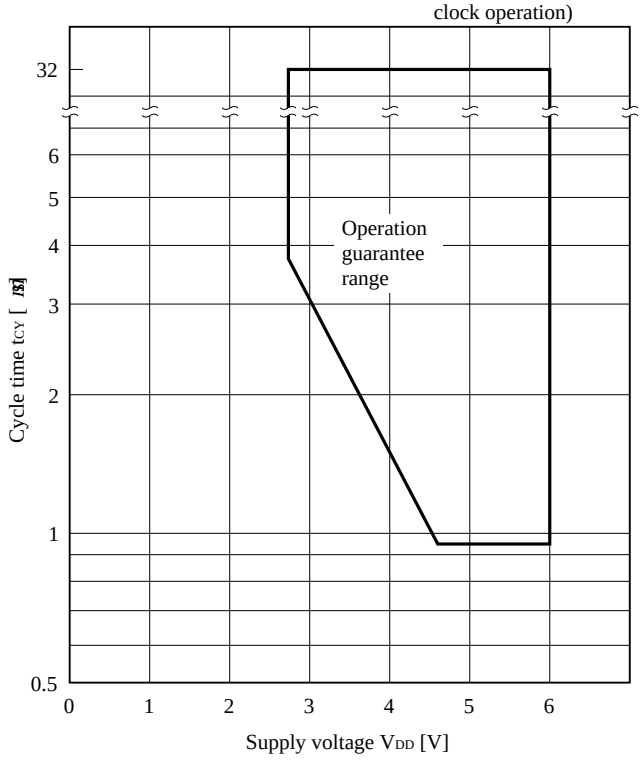
Note 1. The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected resonator, the system clock control register (SCC), and the processor clock control register (PCC).

The right chart shows the cycle time t_{CY} characteristics for power supply voltage V_{DD} during main system clock operation.

2. $2t_{CY}$ or $128/f_X$ depending on how the interrupt mode register (IM0) is set.

t_{CY} vs V_{DD}

(During main system clock operation)



Serial transfer operation

2-wire, 3-wire serial I/O mode ($\overline{SCK}$ - internal clock output)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high, low level width	t_{KL1}, t_{KH1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2-50$			ns
				$t_{KCY1}/2-150$			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓ → SO output delay time	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

2-wire, 3-wire serial I/O mode ($\overline{SCK}$ - external clock input)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low level width	t_{KL2}, t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓ → SO output delay time	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns

Note R_L and C_L are output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$ - internal clock output (master))

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high, low level width	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2-50$			ns
				$t_{KCY3}/2-150$			ns
SB0, SB1 setup time (to $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, SB1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			$t_{KCY3}/2$			ns
$\overline{SCK}$ ↓ → SB0, SB1 output delay time	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0, 1 ↓ → $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0, SB1 low level width	t_{SBL}			t_{KCY3}			ns
SB0, SB1 high level width	t_{SBH}			t_{KCY3}			ns

SBI mode ($\overline{SCK}$ - external clock input (slave))

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low level width	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
$\overline{SB0}$, SB1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, SB1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			$t_{KCY4}/2$			ns
$\overline{SCK}$ ↓ → SB0, SB1 output delay time	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0, 1 ↓ → $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 low level width	t_{SBL}			t_{KCY4}			ns
SB0, SB1 high level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L are SB0, SB1 output line load resistance and load capacitance, respectively.

A/D converter (T_a = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Absolute accuracy Note 1		2.5 V ≤ AV_{REF+} ≤ AV_{DD}	–10 ≤ T_a ≤ +70 °C			±1.5	LSB
			–40 ≤ T_a < –10 °C			±2.0	
Conversion time Note 2	t_{CONV}					168/f_X	μs
Sampling time Note 3	t_{SAMP}					44/f_X	μs
Analog input voltage	V_{IAN}			AV_{REF-}		AV_{REF+}	V
Analog supply voltage	AV_{DD}			2.5		V_{DD}	V
Reference input voltage Note 4	AV_{REF+}	2.5 V ≤ (AV_{REF+}) – (AV_{REF-})		2.5		AV_{DD}	V
Reference input voltage Note 4	AV_{REF-}	2.5 V ≤ (AV_{REF+}) – (AV_{REF-})		0		1.0	V
Analog input impedance	R_{AN}				1000		MΩ
AV_{REF} current	I_{REF}				0.25	2.0	mA

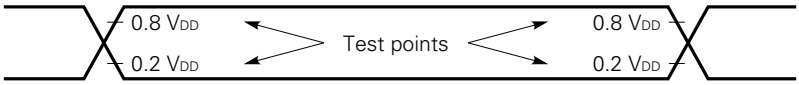
Note 1. Absolute accuracy from which quantization error (±1/2 LSB) is removed.

2. Time until conversion end (EOC = 1) after conversion start instruction execution (40.1 μs: During f_X = 4.19 MHz operation).

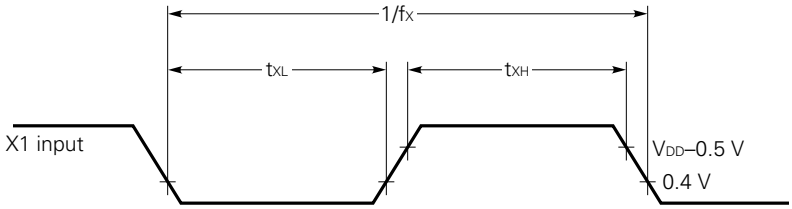
3. Time until sampling end after conversion start instruction execution (10.5 μs: During f_X = 4.19 MHz operation).

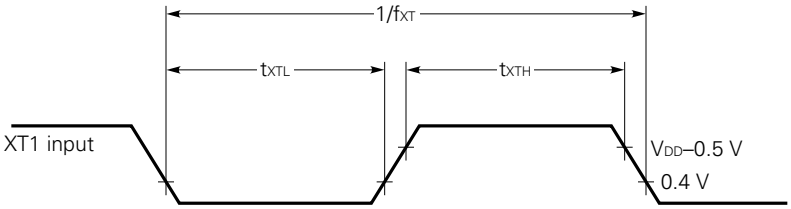
4. (AV_{REF+}) – (AV_{REF-}) must be more than 2.5 V.

AC timing test points (Except X1, XT1)

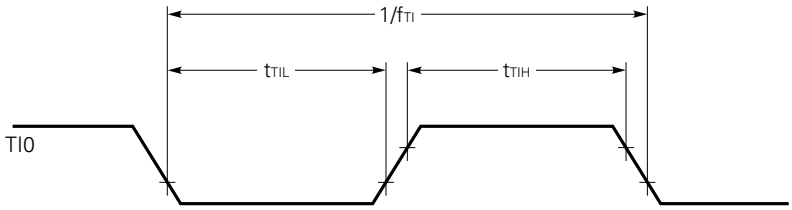


Clock timing



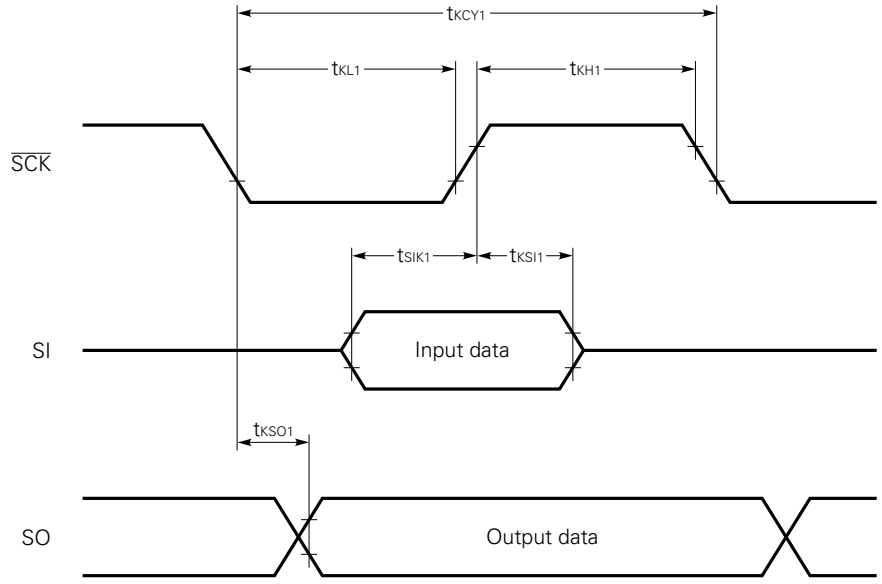


TI0 timing

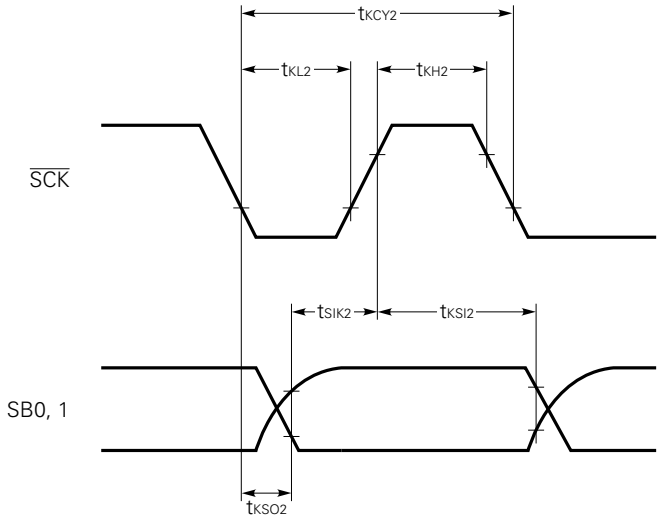


Serial transfer timing

Serial I/O made (3-wire)

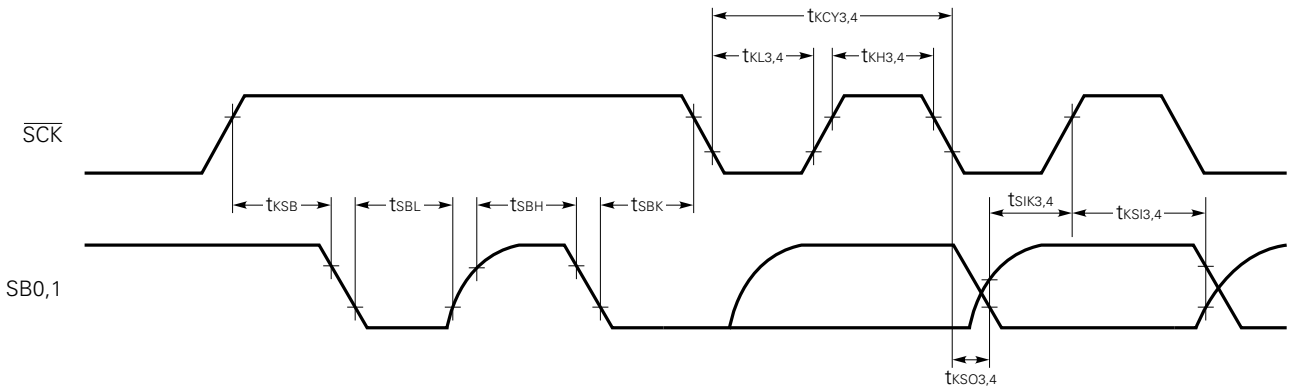


Serial I/O mode (2-wire)

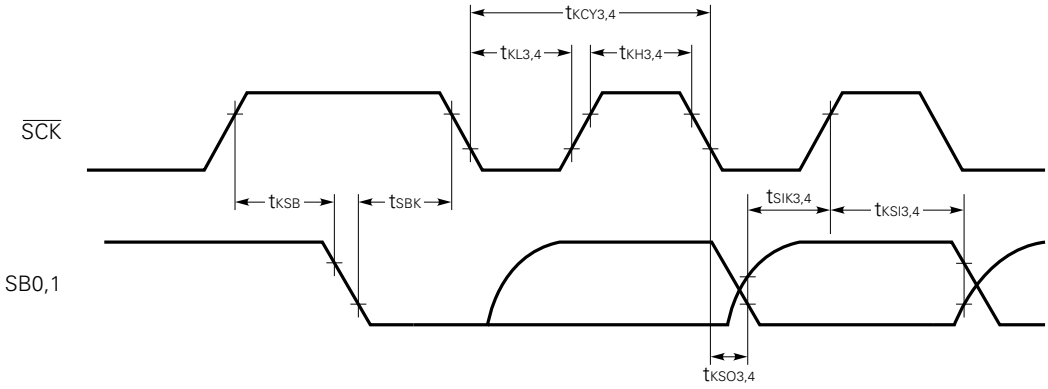


Serial transfer timing

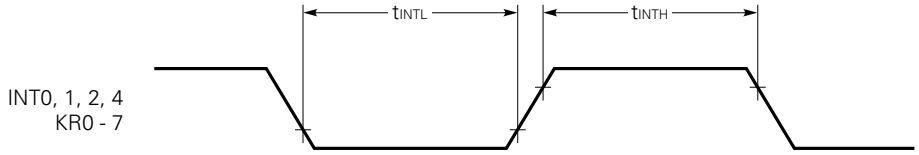
SBI mode bus release signal transfer timing



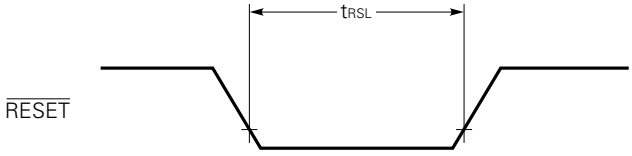
SBI mode command signal transfer timing



Interrupt input timing



RESET input timing



Data memory STOP mode low voltage data retention characteristics (T_a = –40 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		2.0		6.0	V
Data retention current **Note 1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal SET time	t_{SREL}		0			μs
Oscillation stabilization time **Note 2**	t_{WAIT}	Release by $\overline{\text{RESET}}$ input		$2^{17}/f_X$		ms
		Release by interrupt request		**Note 3**		ms

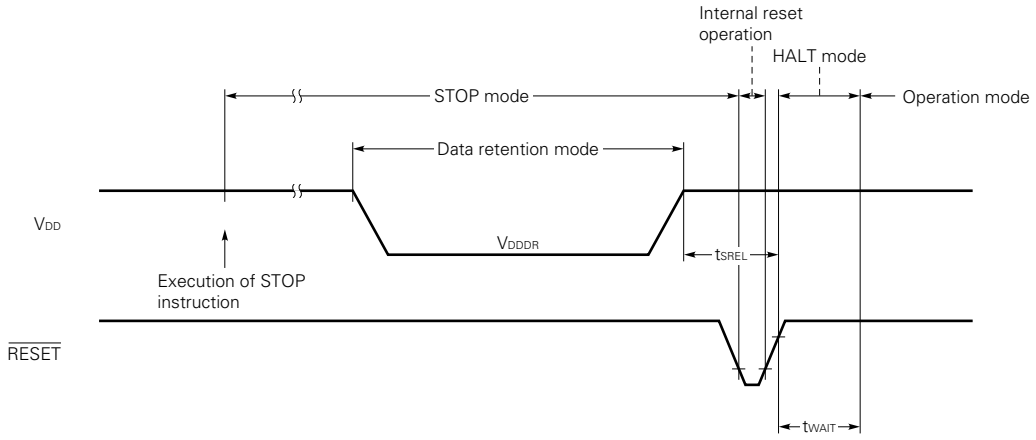
Note 1. On-chip pull-up resistor current is not included in this table.

2. The oscillation stabilization WAIT time is the time during which the CPU operation is stopped to prevent unstable operation when oscillation is started.

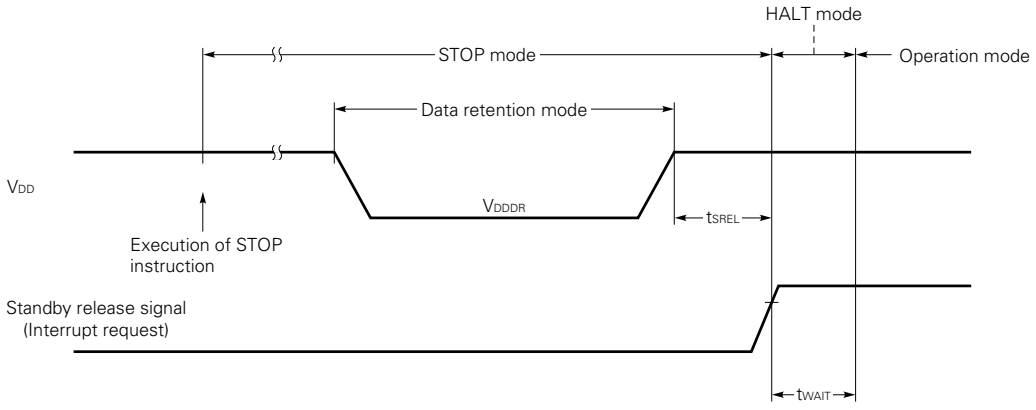
3. The WAIT time depends on the setting of the basic interval timer mode register (BTM) according to the following table.

BTM3	BTM2	BTM1	BTM0	WAIT time (f_X = 4.19 MHz)
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

Data retention timing (STOP mode is released by $\overline{\text{RESET}}$ input)

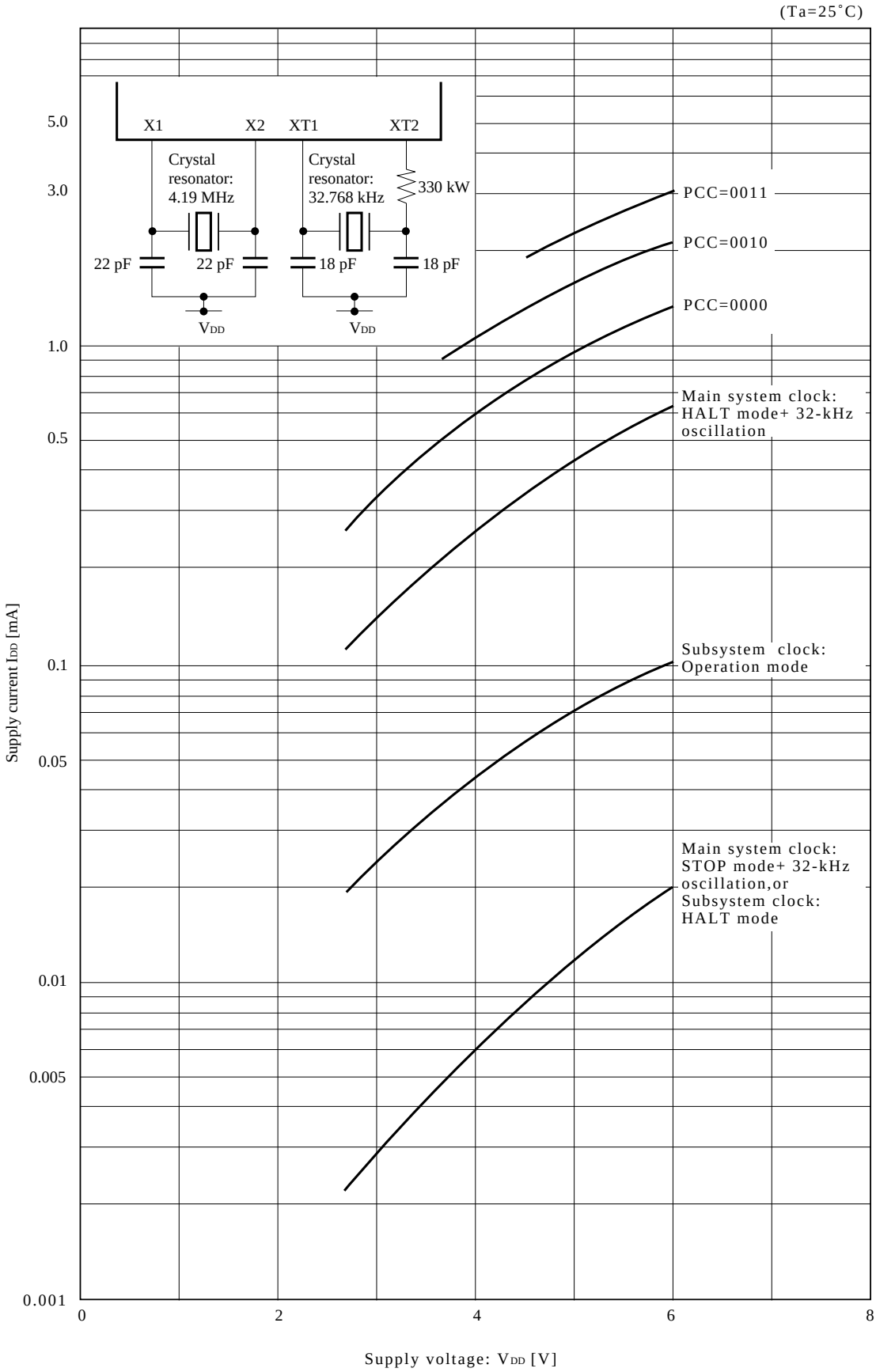


Data retention timing (Standby release signal: STOP mode is released by interrupt signal)

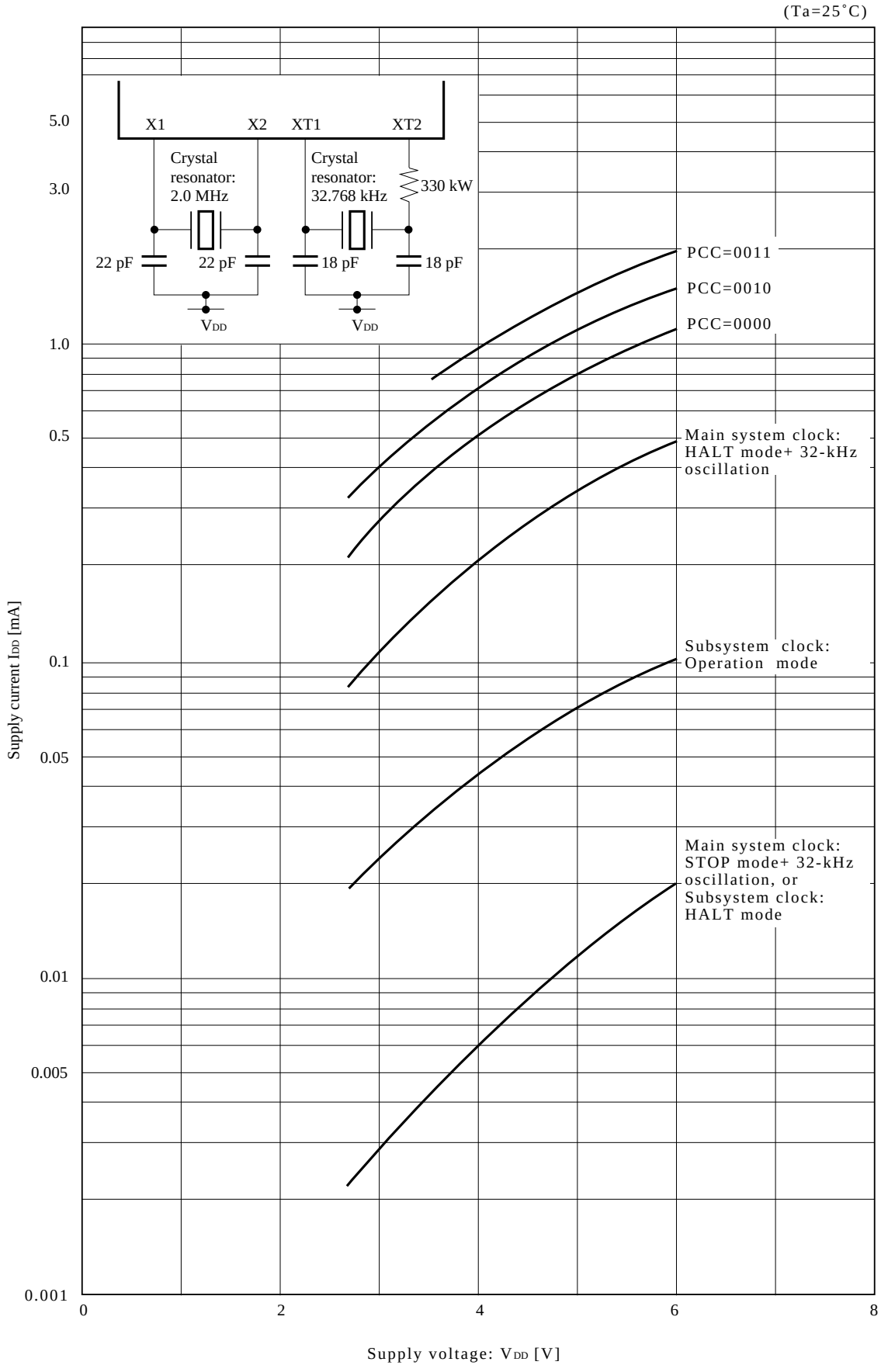


11. CHARACTERISTIC CURVES (FOR REFERENCE ONLY) ★

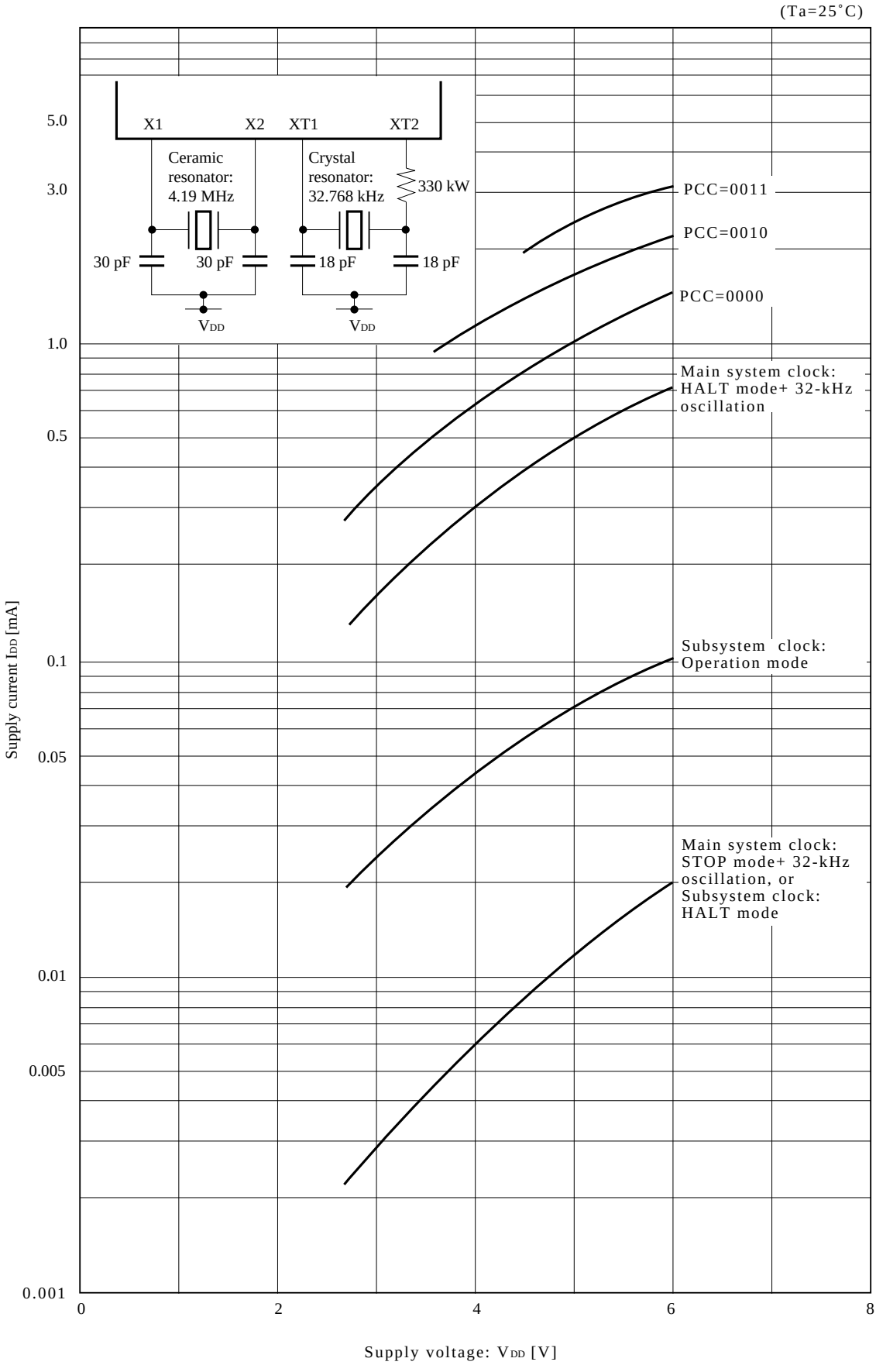
I_{DD} vs. V_{DD} (Main system clock: 4.19 MHz, crystal resonator)



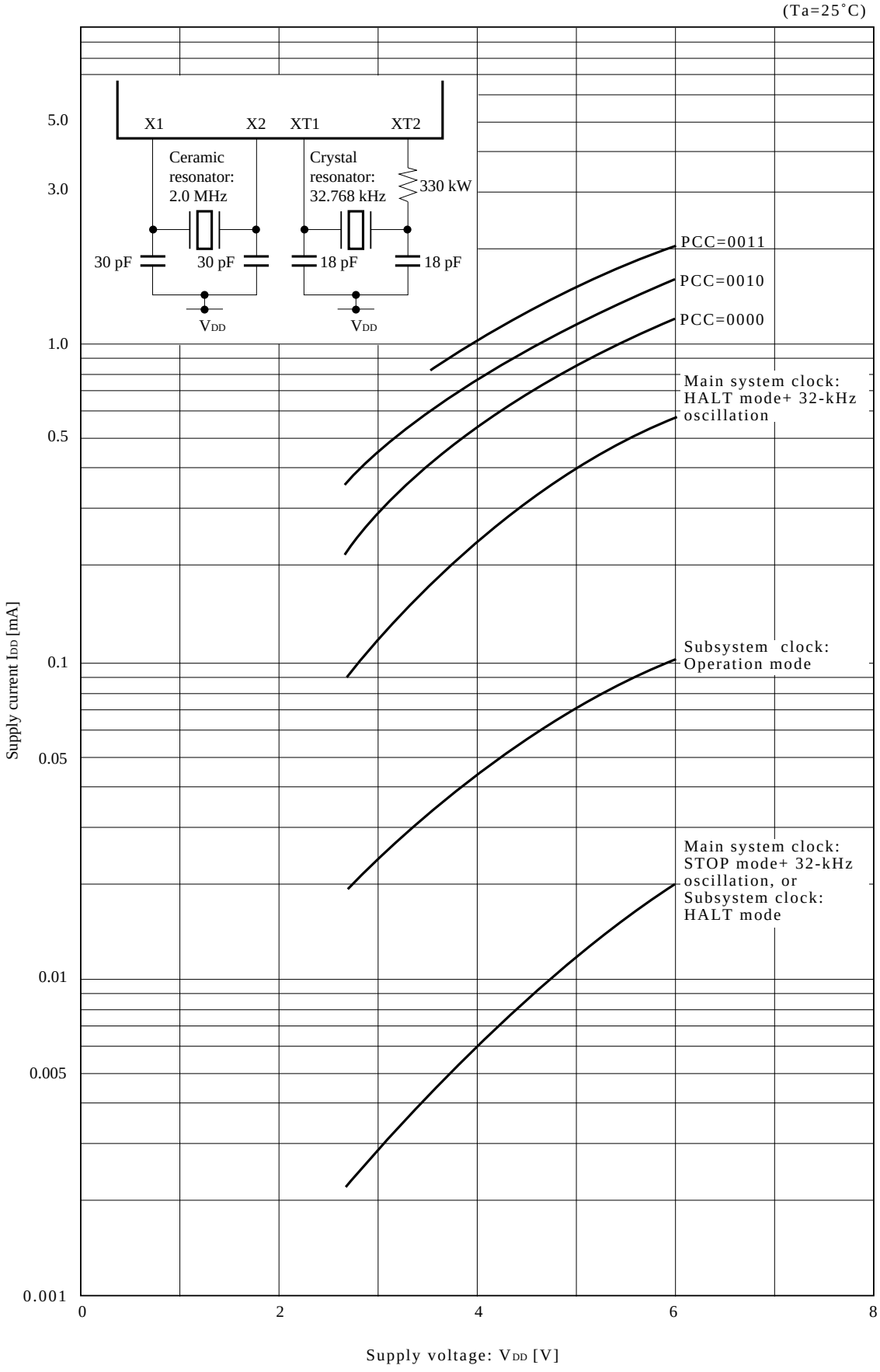
I_{DD} vs. V_{DD} (Main system clock: 2.0 MHz, crystal resonator)



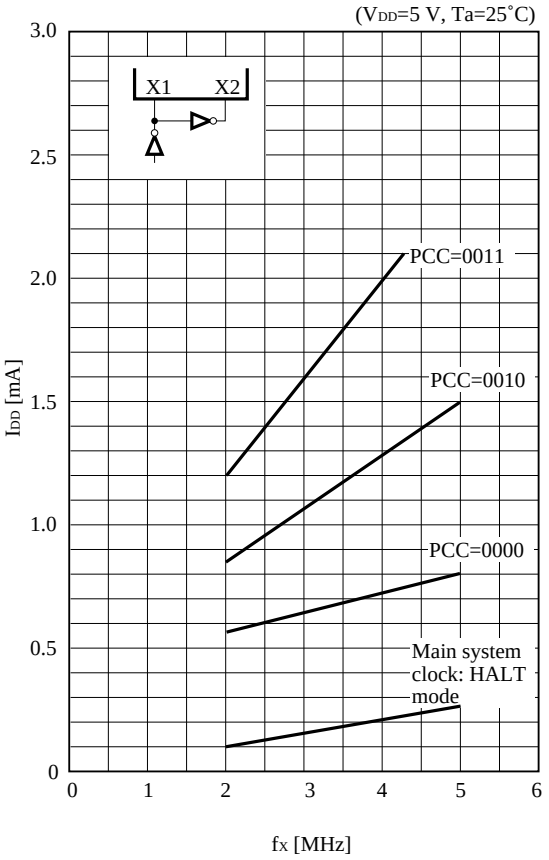
I_{DD} vs. V_{DD} (Main system clock: 4.19 MHz, ceramic resonator)



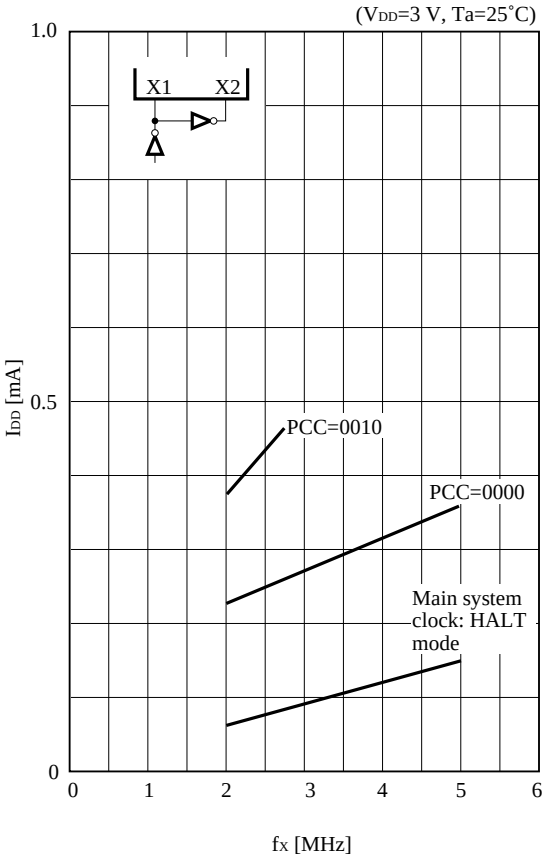
I_{DD} vs. V_{DD} (Main system clock: 2.0 MHz, ceramic resonator)



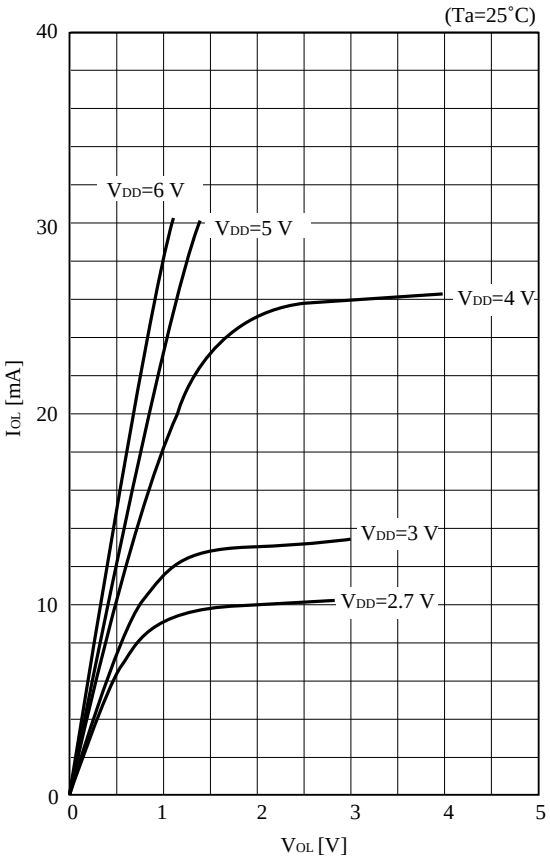
IDD vs. fX



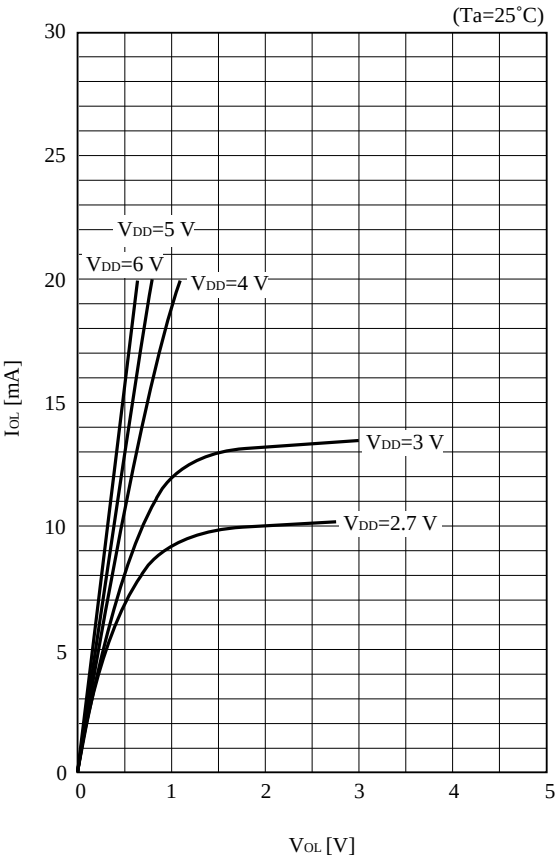
IDD vs. fX



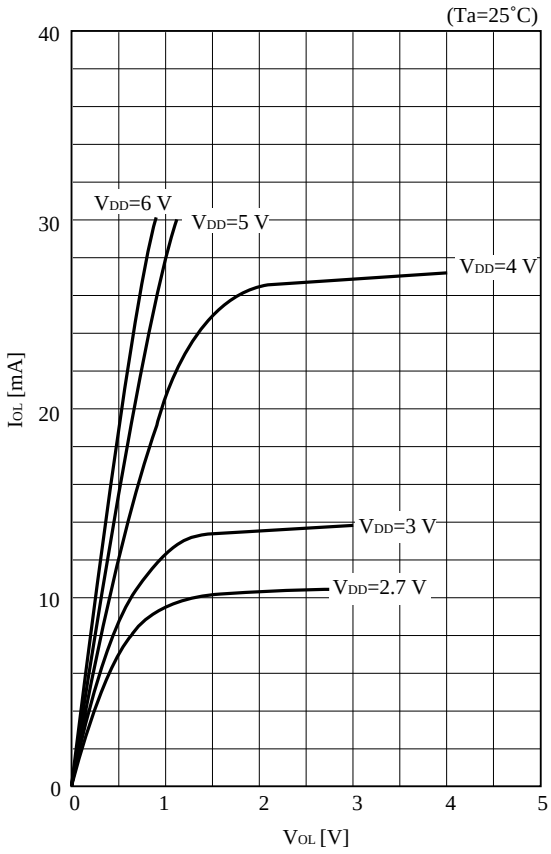
IOL vs. VOL (Port 0)



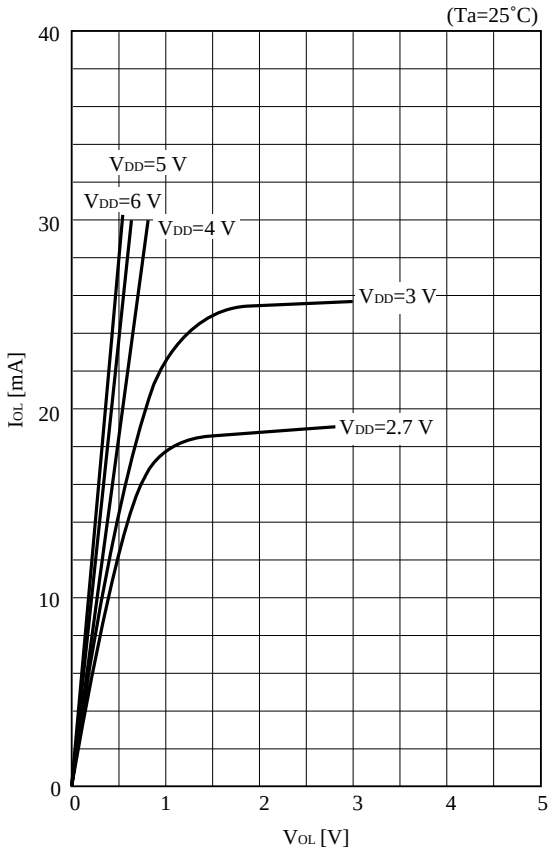
IOL vs. VOL (Port 2, 6 through 10)



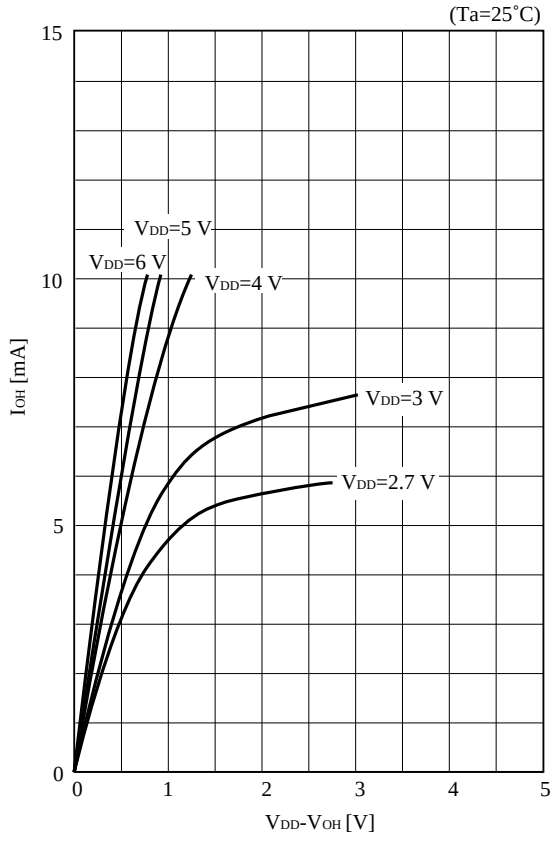
IOL vs. VOL (Port 3)



IOL vs. VOL (Port 4, 5)

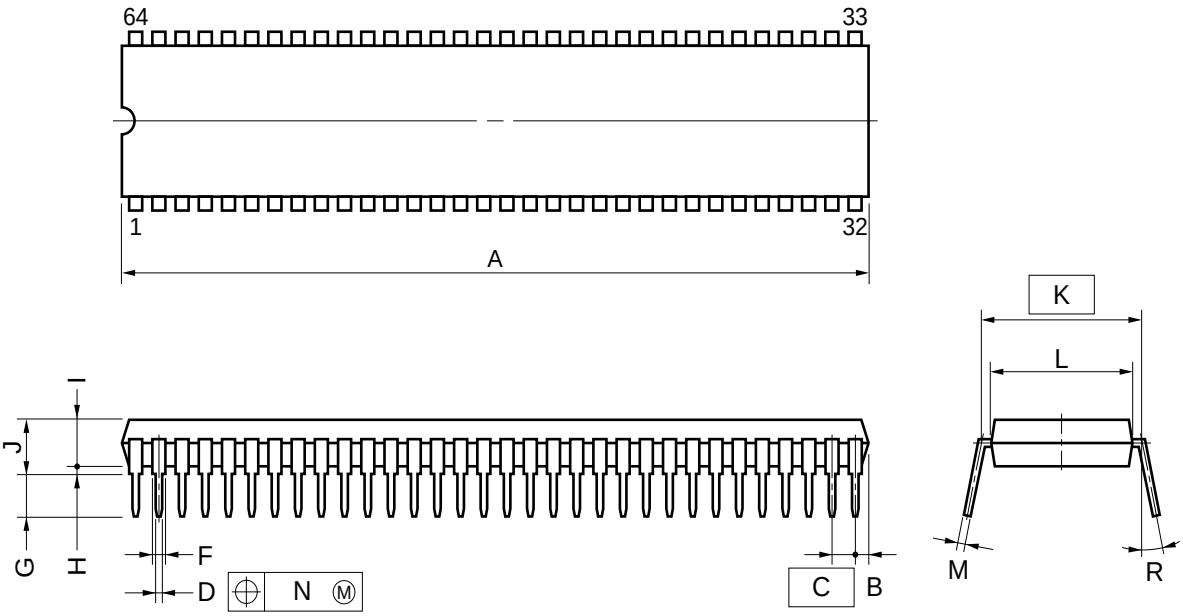


IOH vs. VOH



12. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

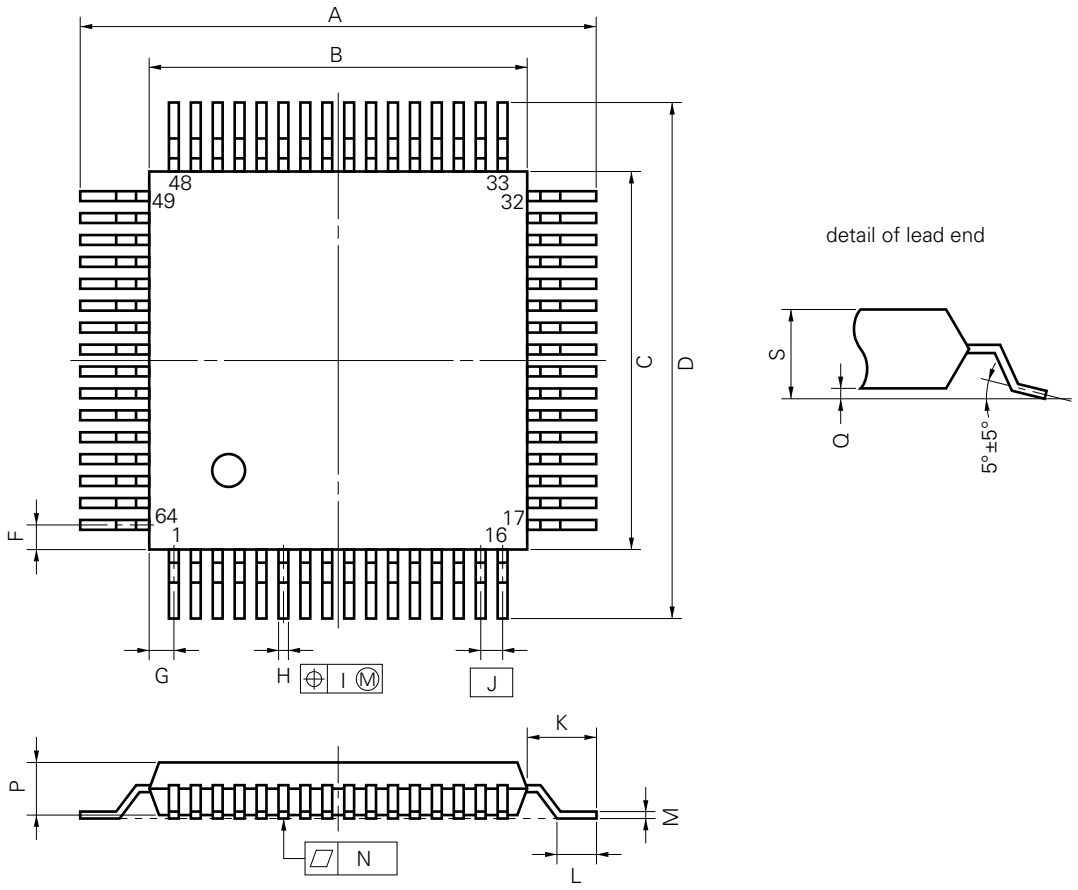
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)



P64GC-80-AB8-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	$0.35^{+0.10}_{-0.05}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

13. RECOMMENDED SOLDERING CONDITIONS

The following conditions (See table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

For more details, refer to our document "**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL**" (IEI-1207).

Table 13-1 Type of Surface Mount Device

μPD75028GC-×××-AB8: 64-pin plastic QFP (□ 14 mm)

Soldering Process	Soldering Conditions	Symbol
Wave Soldering	Solder temperature: 260 °C or lower, Flow time: 10 seconds or less, Exposure limit [Note]: 7 days (10 hours pre-baking is required at 125 °C afterwards) Temperature of pre-heat: 120 °C or lower (Package surface temperature) Number of flow process: 1	WS60-107-1
Infrared Ray Reflow	Peak temperature of package surface: 230 °C or lower Reflow time: 30 seconds or less (210 °C or higher), Number or reflow process: 1 Exposure limit [Note]: 7 days (10 hours pre-baking is required at 125 °C afterwards)	IR30-107-1
VPS	Peak temperature of package surface: 215 °C or lower Reflow time: 40 seconds or less (200 °C or higher), Number of reflow process: 1 Exposure limit [Note]: 7 days (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-1
Partial Heating Method	Pin temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package)	—

Note Exposure limit before soldering after dry-pack package is opened. Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

Table 13-2 Type of Through Hole Device

μPD75028CW-×××: 64-pin plastic shrink DIP (750 mil)

Soldering Process	Soldering Conditions
Wave Soldering	Solder temperature: 260 °C or lower, Flow time: 10 seconds or less
Partial Heating Method	Pin temperature: 260 °C or lower, Time: 10 seconds or less

Caution Do not jet molten solder on the surface of package.

PRODUCT NEWS

A product whose recommended soldering conditions have been improved is available.
(Improvements: Expansion of infrared ray reflow soldering peak temperature (235 °C), two sessions of soldering, extended term of storage, etc.)
For details, contact our sales staff.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are provided for the development of a system which employs the μPD75028.

Hardware	IE-75000-R [Note 1] IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM [Note 2]	Emulation board for IE-75000-R and IE-75001-R
	EP-75028CW-R	Emulation probe for μPD75028CW
	EP-75028GC-R EV-9200GC-64	Emulation probe for μPD75028GC with the 64-pin conversion socket EV-9200GC-64
	PG-1500	PROM programmer
	PA-75P036CW	PROM programmer adapter for μPD75P036CW. Connected to PG-1500.
	PA-75P036GC	PROM programmer adapter for μPD75P036GC. Connected to PG-1500.
Software	IE control program	Host machine • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A [Note 3]) • IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

Note 1. Available for maintenance purpose only.

2. Not included with IE-75001-R.

3. Ver. 5.00/5.00A has a task swap function. However, it cannot be used for these software programs.

Remark For development tools available from third parties, please refer to **"75X Series Selection Guide (IF-xxx)."**

APPENDIX B. RELATED DOCUMENTS ★

List of documents related to devices

Document	Document No.
User's Manual	IEU-694
Instruction Table	IEM-5511
Application Note	IEA-689
75X Series Selection Guide	IF-151

List of documents related to development tools

Document			Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846
	IE-75000-R-EM User's Manual		EEU-673
	EP-75028CW-R User's Manual		EEU-697
	EP-75028GC-R User's Manual		EEU-692
	PG-1500 User's Manual		EEU-651
Software	RA75X Assembler Package User's Manual	Operation	EEU-731
		Language	EEU-730
	PG-1500 Controller User's Manual		EEU-704

Other documents

Document	Document No.
Package Manual	IEI-635
Semiconductor Device Mounting Technology Manual	IEI-616
NEC Semiconductor Device Quality Grades	IEI-620
NEC Semiconductor Device Reliability and Quality Control	IEM-5068
About Electrostatic Discharge (ESD) Test	MEM-539
Semiconductor Device Quality Assurance Guide	MEI-603
Microcomputer-Related Product Guide: Third Parties' Products	MEI-604

Remark The document numbers are those of Japanese-version documents.

Caution The above documents are subject to change without notice. Be sure to use the latest documents for design or for any other similar purpose.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

M4 92.6