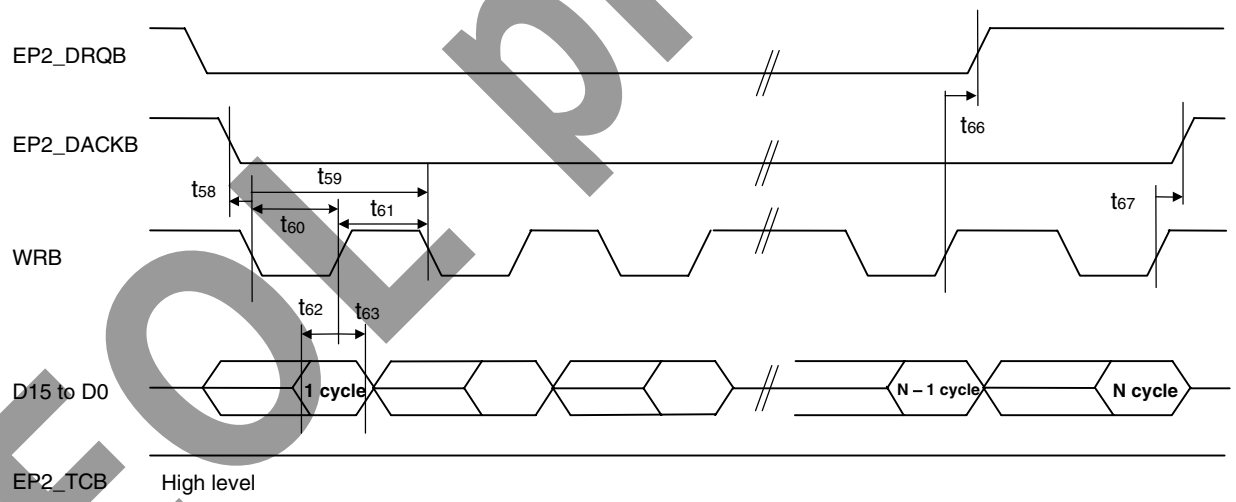
(d) CPU bus DMA demand write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T58	DMA request acknowledge setup time (WRB↓)	0		∞	ns
T59	DMA demand mode write transfer cycle time	72		∞	ns
T60	Write command width	38		∞	ns
T61	Write command inactive time	34		∞	ns
T62	Write data setup time (WRB↑)	10		∞	ns
T63	Write data hold time (WRB↑)	0		∞	ns
T64	EP2_TCB setup time (WRB↓)	0		**Note**	ns
T65	EP2_TCB hold time (WRB↓)	17		∞	ns
T66	DMA request off time (WRB↑)	–		60	ns
T67	DMA request acknowledge hold time (WRB↑)	0		∞	ns
T70	DMA request off time (EP2_DACKB↓)	–		38	ns
T73	DMA request on time (EP2_DACKB↑)	–		88	ns
T75	DMA request off time (WRB↓)	–		60	ns

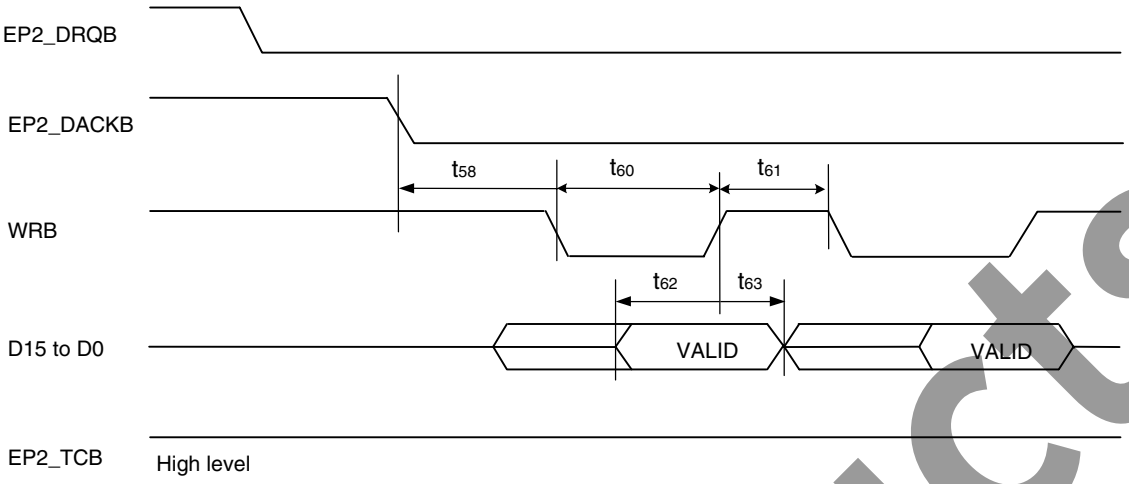
Note Can be input after immediately previous WRB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

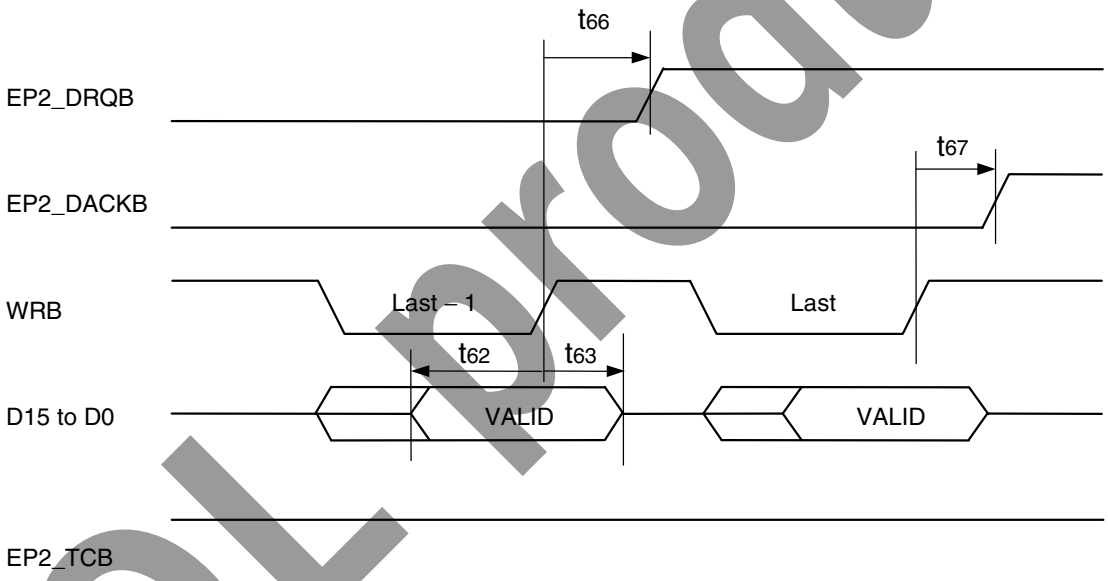
(Overall)



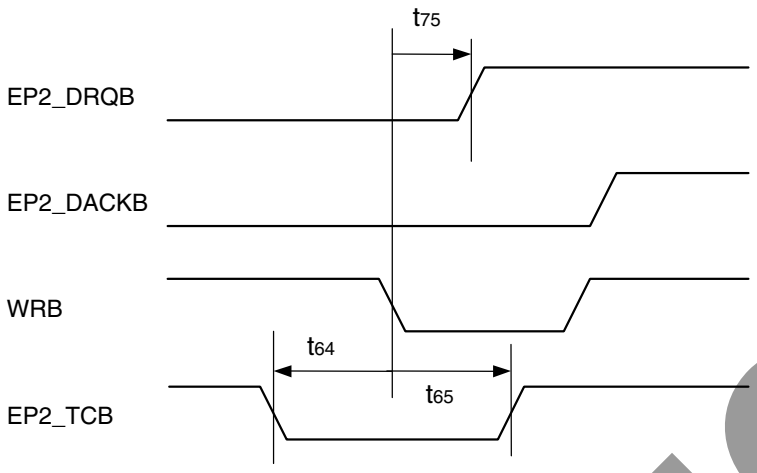
(Start timing)



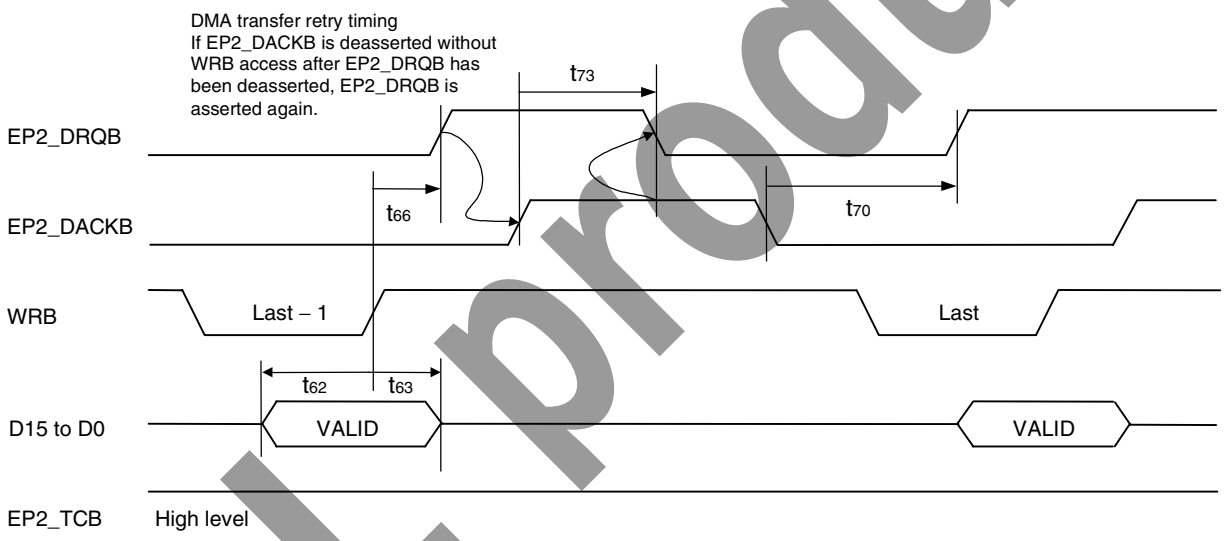
(End timing)



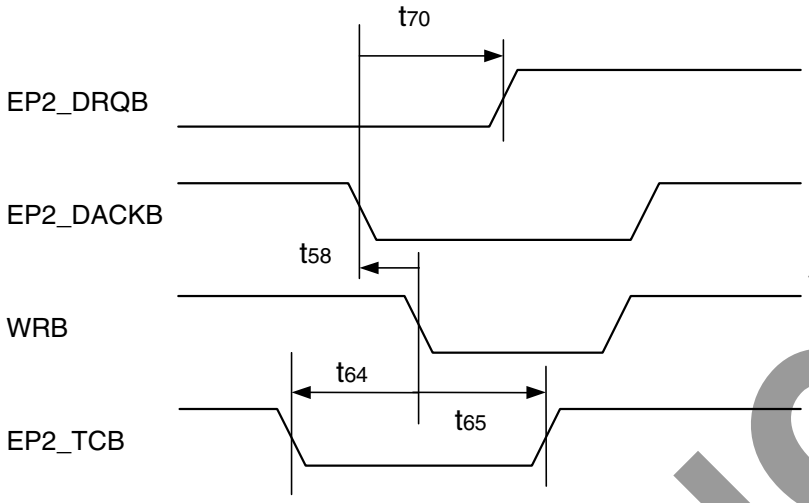
(TCB timing)



(Retransmission timing)



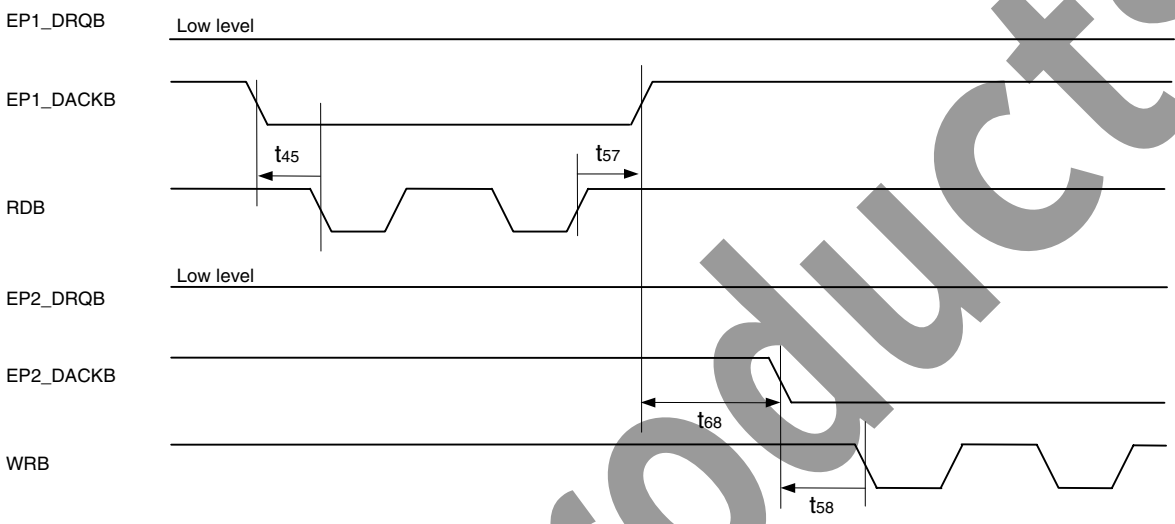
(If EP1_TCB is input when retransmission is executed)



(a) CPU bus DMA read transfer vs. write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T68	RDB vs. WRB command inactive time	34		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).



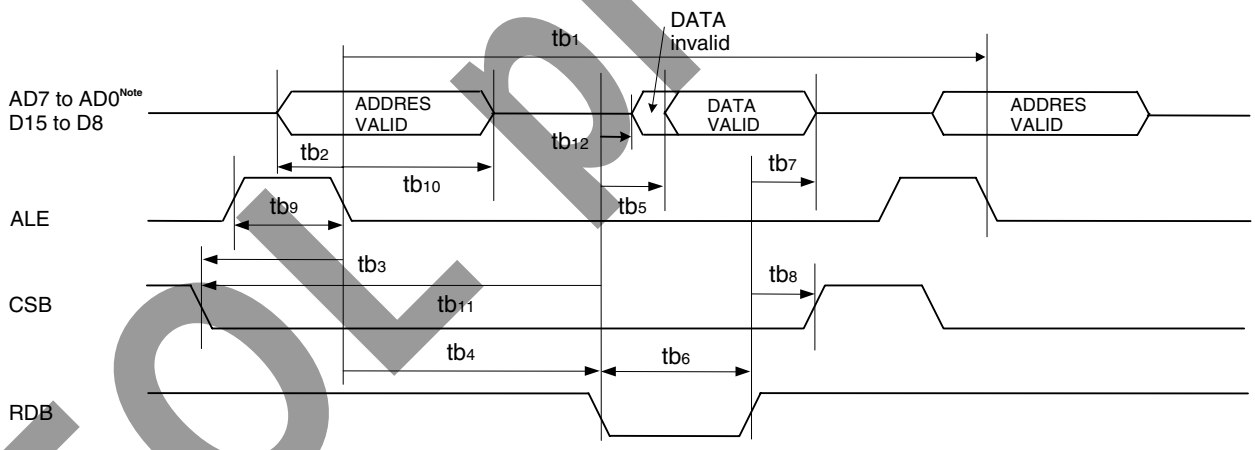
2.6.3 AC characteristics of BIU block with function 2 or 3 selected

(1) CPU bus read operation

Symbol	Parameter	Min.	Typ.	Max.	Unit
TB1	Read cycle time	86		∞	ns
TB2	Address setup time (ALE↓)	10		∞	ns
TB3	Chip select setup time (ALE↓)	17		∞	ns
TB4	Read command delay time (ALE↓)	7		∞	ns
TB5	Output data delay time (RDB↓)	–		57	ns
TB6	Read command width	57		∞	ns
TB7	Output data hold time (RDB↑)	4		–	ns
TB8	Chip select hold time (RDB↑)	5		∞	ns
TB9	ALE width	10		∞	ns
TB10	Address hold time (ALE↓)	0		∞	ns
TB11	Chip select setup time (RDB↓)	5		∞	ns
TB12	Buffer direction change time (RDB↓)	–		14	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

CPU bus read timing



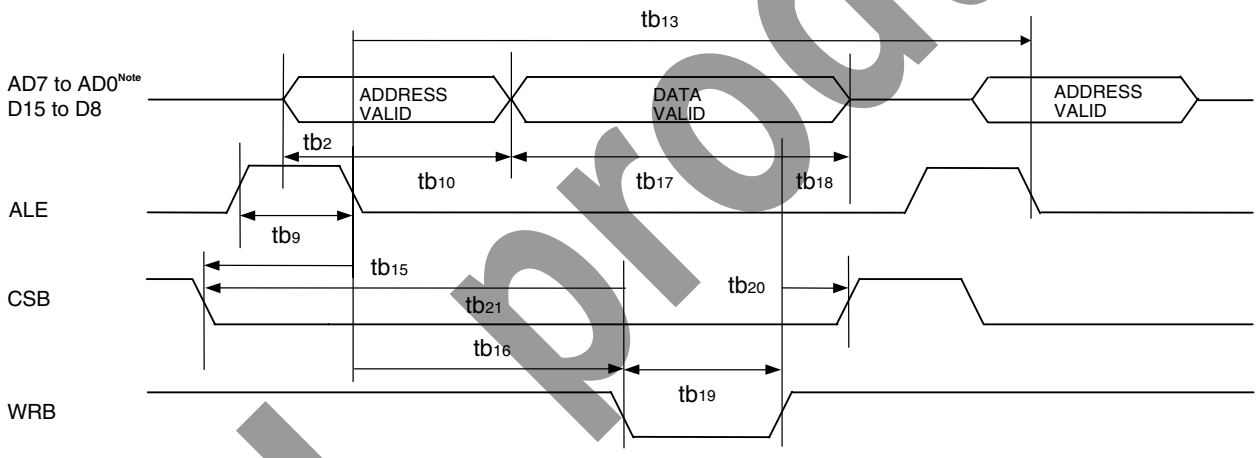
Note D7 to D0 for Function 2

(2) CPU bus write operation

Symbol	Parameter	Min.	Typ.	Max.	Unit
TB13	Write cycle time	58		∞	ns
TB14	Address setup time (ALE↓)	17		∞	ns
TB15	Chip select setup time (ALE↓)	17		∞	ns
TB16	Write command delay time (ALE↓)	7		∞	ns
TB17	Input data setup time (WRB↑)	10		∞	ns
TB18	Input data hold time (WRB↑)	0		∞	ns
TB19	Write command width	34		∞	ns
TB20	Chip select hold time (WRB↑)	0		∞	ns
TB21	Chip select setup time (WRB↓)	5		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

CPU bus write timing



Note D7 to D0 for Function 2

2.6.4 External local bus

(1) External local bus 16-bit mode

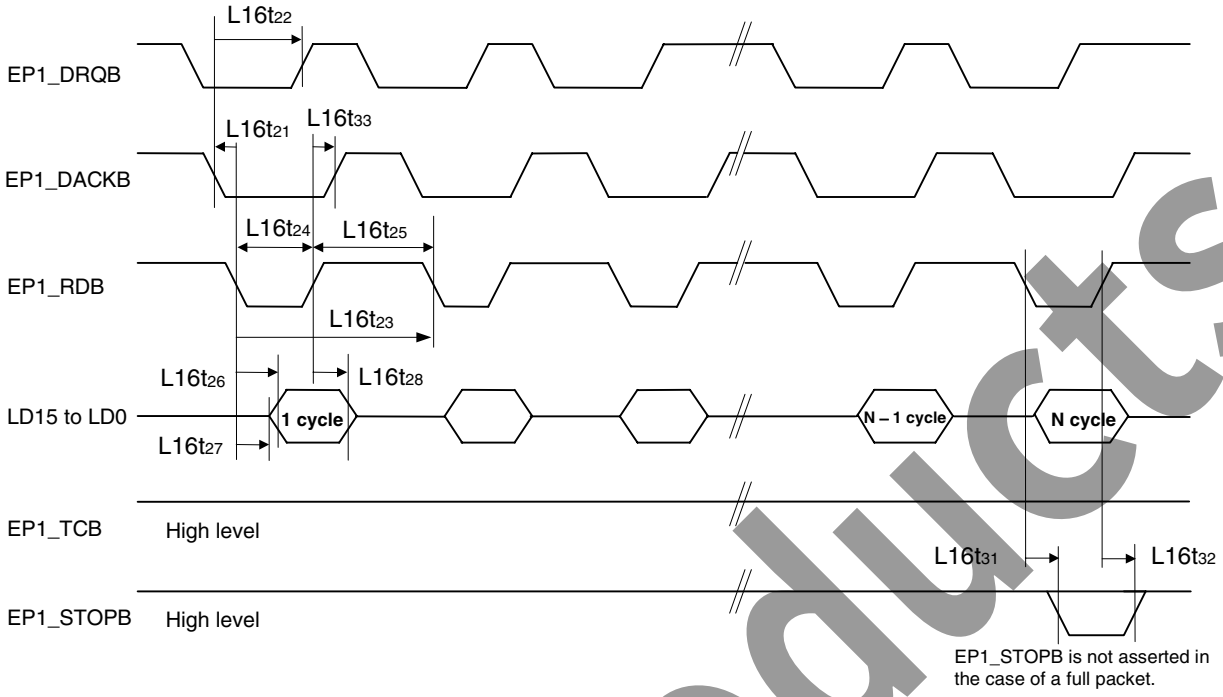
(a) External local bus 16-bit mode DMA single mode read transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T21	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L16T22	DMA request off time 1 (EP1_DACKB↓)	–		54	ns
L16T23	DMA single mode read transfer cycle time	91		∞	ns
L16T24	Read command width	57		∞	ns
L16T25	Read command inactive time	34		∞	ns
L16T26	Read data delay time (EP1_RDB↓)	–		57	ns
L16T27	Buffer direction change time (EP1_RDB↓)	–		14	ns
L16T28	Read data hold time (EP1_RDB↑)	4		–	ns
L16T29	EP1_TCB setup time (EP1_RDB↓)	0		**Note**	ns
L16T30	EP1_TCB hold time (EP1_RDB↓)	17		∞	ns
L16T31	EP1_STOPB delay time (EP1_RDB↓)	–		15	ns
L16T32	EP1_STOPB delay time (EP1_RDB↑)	3		–	ns
L16T33	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns
L16T34	Undefined	–		–	ns

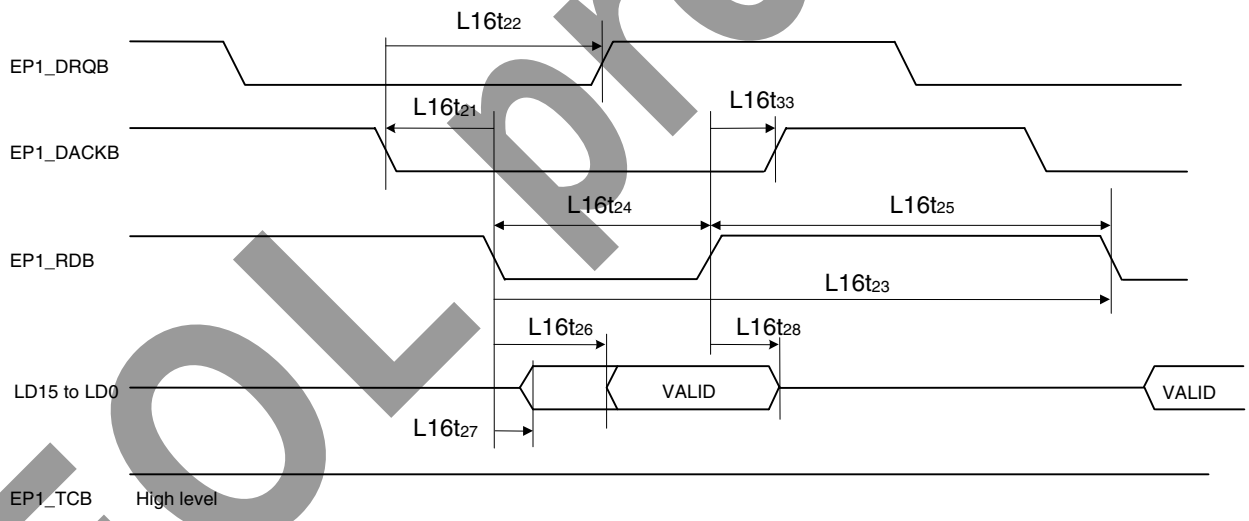
Note Can be input after previous EP1_RDB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

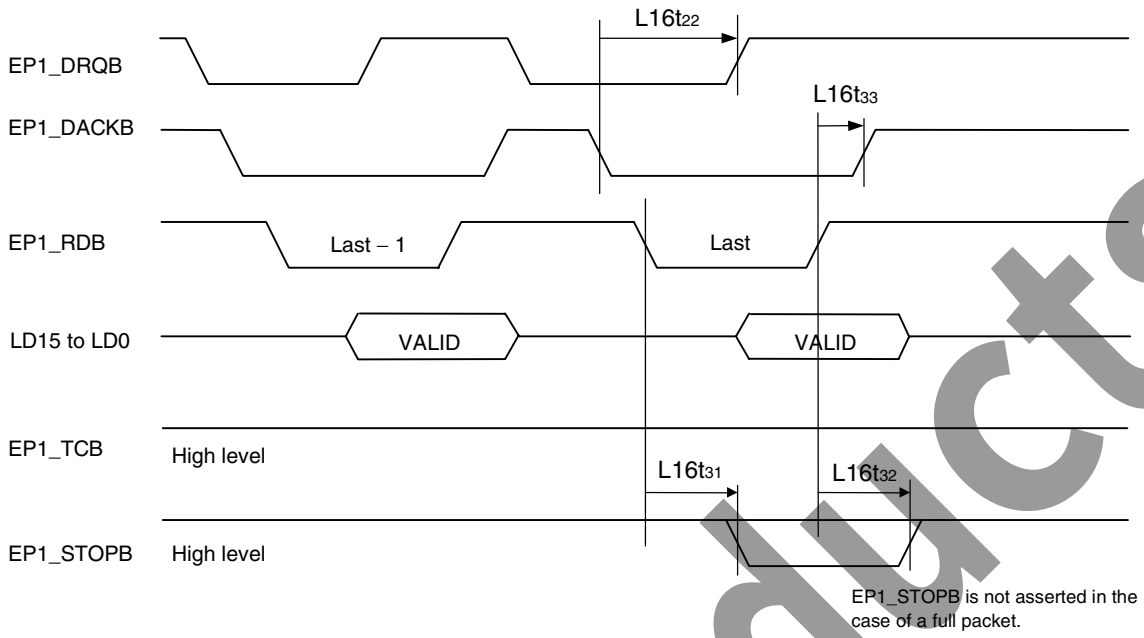
(Overall)



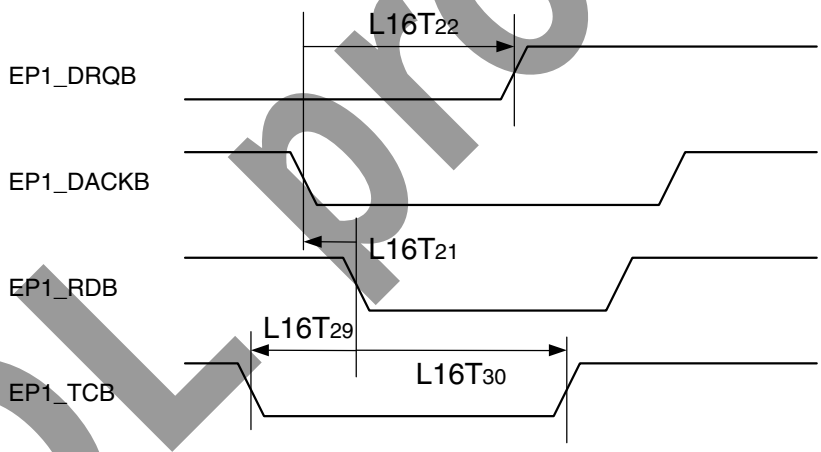
(Start timing)



(End timing)



(TCB timing)



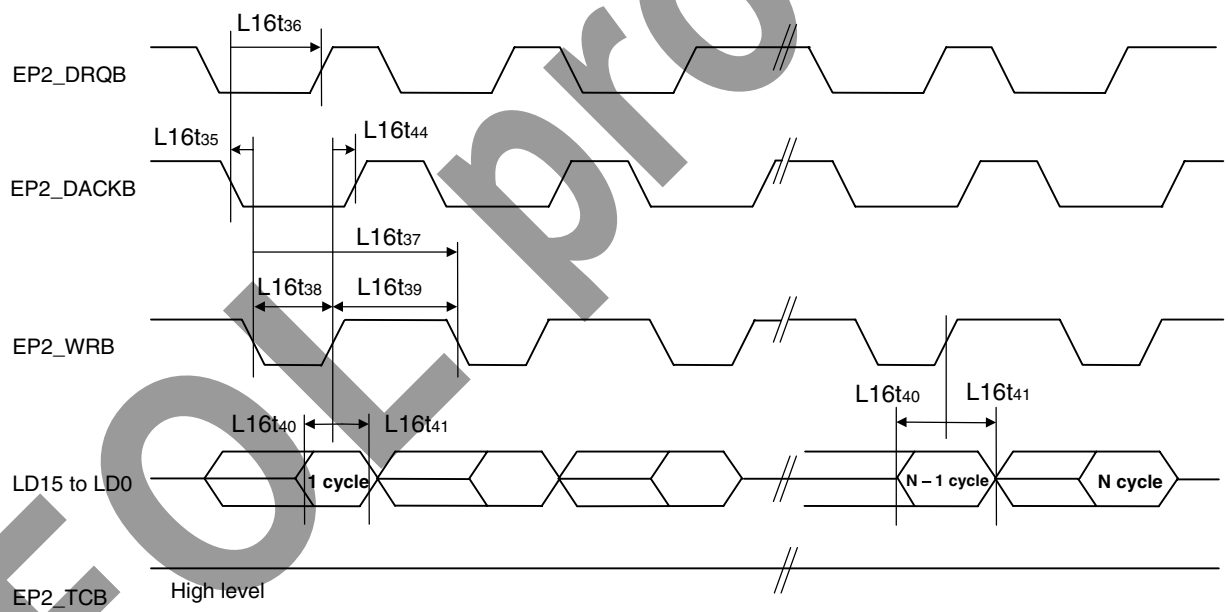
(a) External local bus 16-bit mode DMA single mode write transfer

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T35	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L16T36	DMA request off time 1 (EP2_DACKB↓)	–		54	ns
L16T37	DMA single mode write transfer cycle time	88		∞	ns
L16T38	Write command width	54		∞	ns
L16T39	Write command inactive time	34		∞	ns
L16T40	Write data setup time (EP2_WRB↑)	10		∞	ns
L16T41	Write data hold time (EP2_WRB↑)	0		∞	ns
L16T42	EP2_TCB setup time (EP2_WRB↓)	0		**Note**	ns
L16T43	EP2_TCB hold time (EP2_WRB↓)	17		∞	ns
L16T44	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns

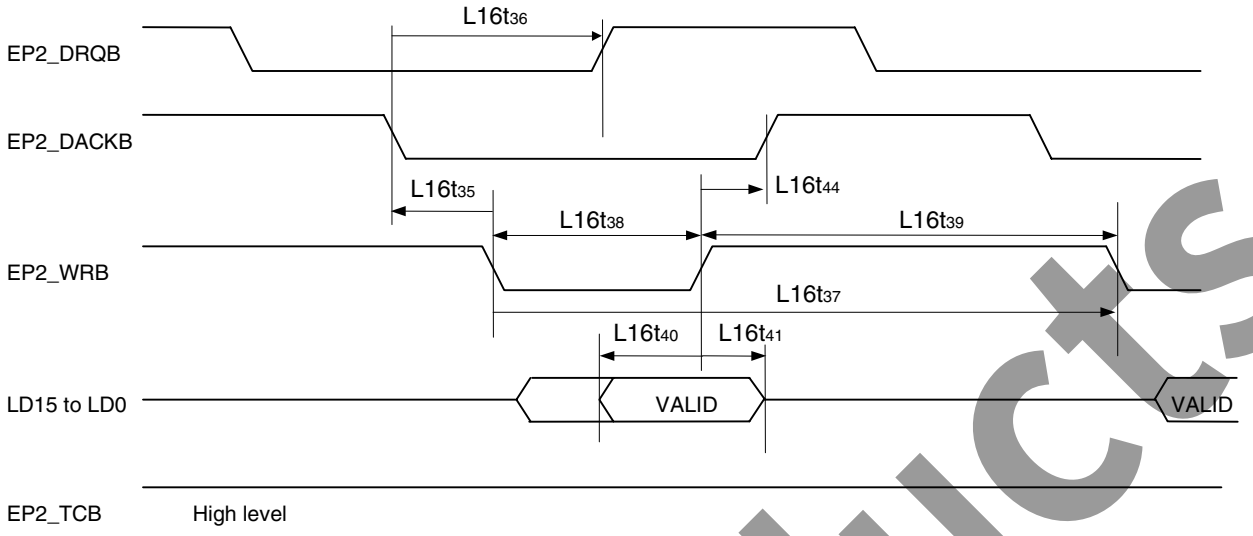
Note Can be input after previous EP2_WRB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

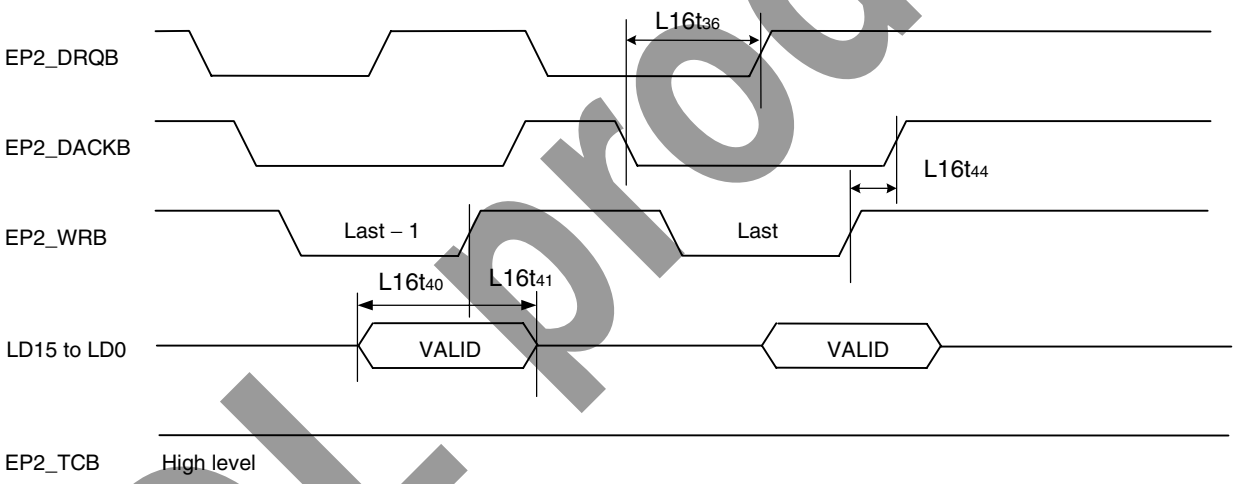
(Overall)



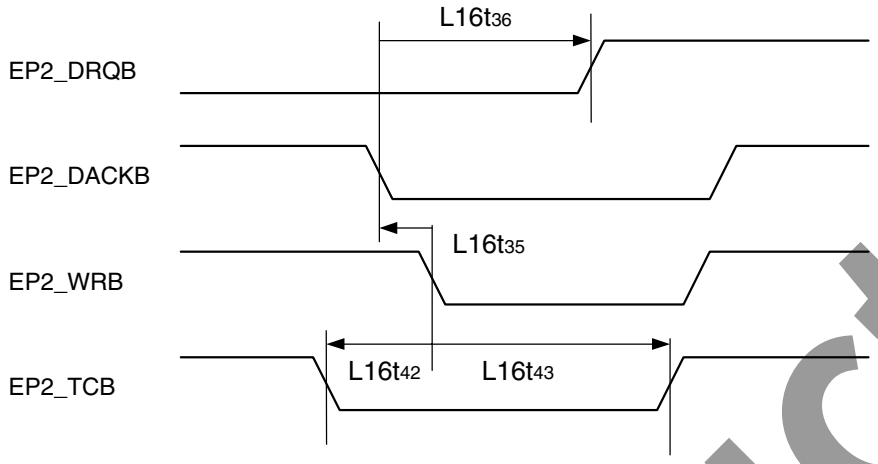
(Start timing)



(End timing)



(TCB timing)



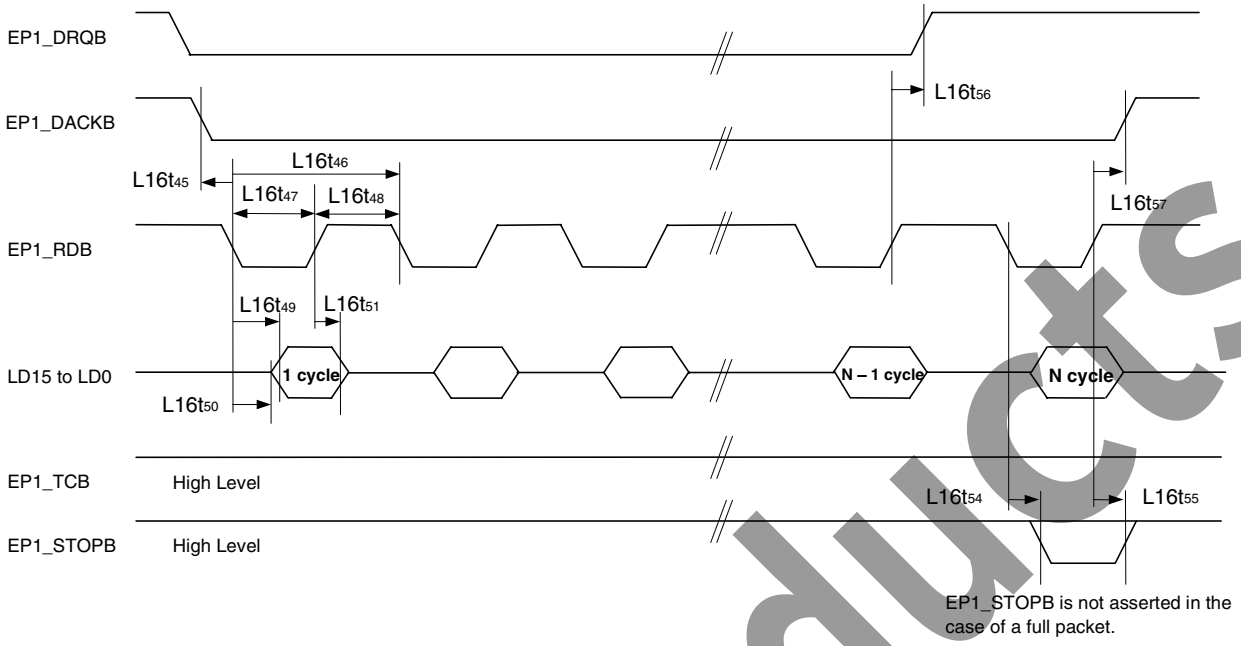
(c) External local bus 16-bit mode DMA demand read transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T45	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L16T46	DMA demand mode read transfer cycle time	91		∞	ns
L16T47	Read command width	57		∞	ns
L16T48	Read command inactive time	34		∞	ns
L16T49	Read data delay time (EP1_RDB↓)	–		57	ns
L16T50	Buffer direction change time (EP1_RDB↓)	–		14	ns
L16T51	Read data hold time (EP1_RDB↑)	4		–	ns
L16T52	EP1_TCB setup time (EP1_RDB↓)	0		**Note**	ns
L16T53	EP1_TCB hold time (EP1_RDB↓)	17		∞	ns
L16T54	EP1_STOPB delay time (EP1_RDB↓)	–		15	ns
L16T55	EP1_STOPB delay time (EP1_RDB↑)	3		–	ns
L16T56	DMA request off time (EP1_RDB↑)	–		59	ns
L16T57	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns
L16T69	DMA request off time (EP1_DACKB↓)	–		38	ns
L16T71	DMA request off time (EP1_DACKB↓) 1 cycle transfer	–		38	ns
L16T72	DMA request on time (EP1_DACKB↑)	–		88	ns
L16T74	DMA request off time (EP1_RDB↓)	–		60	ns

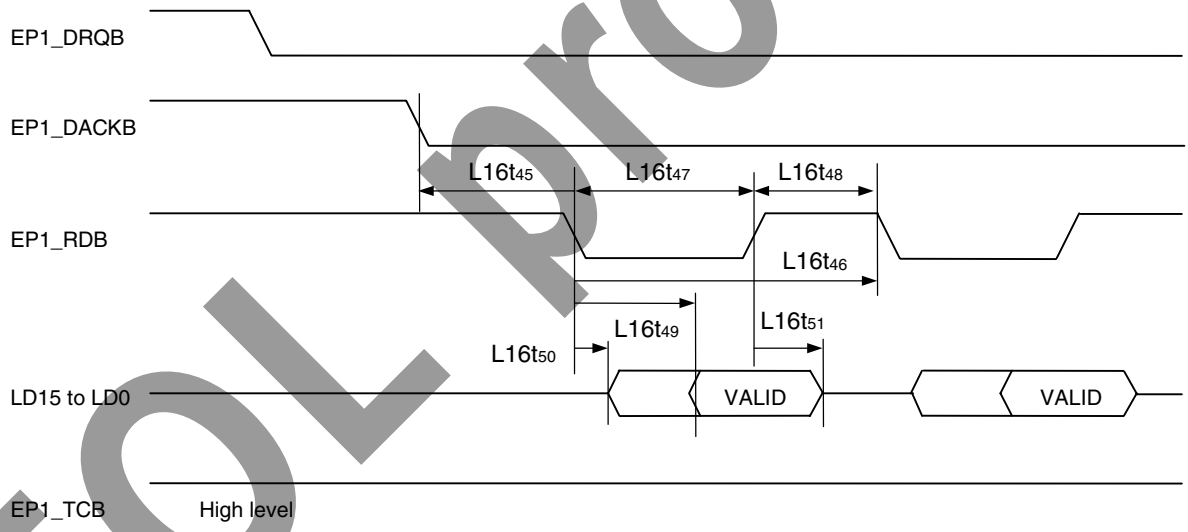
Note Can be input after immediately previous EP1_RDB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

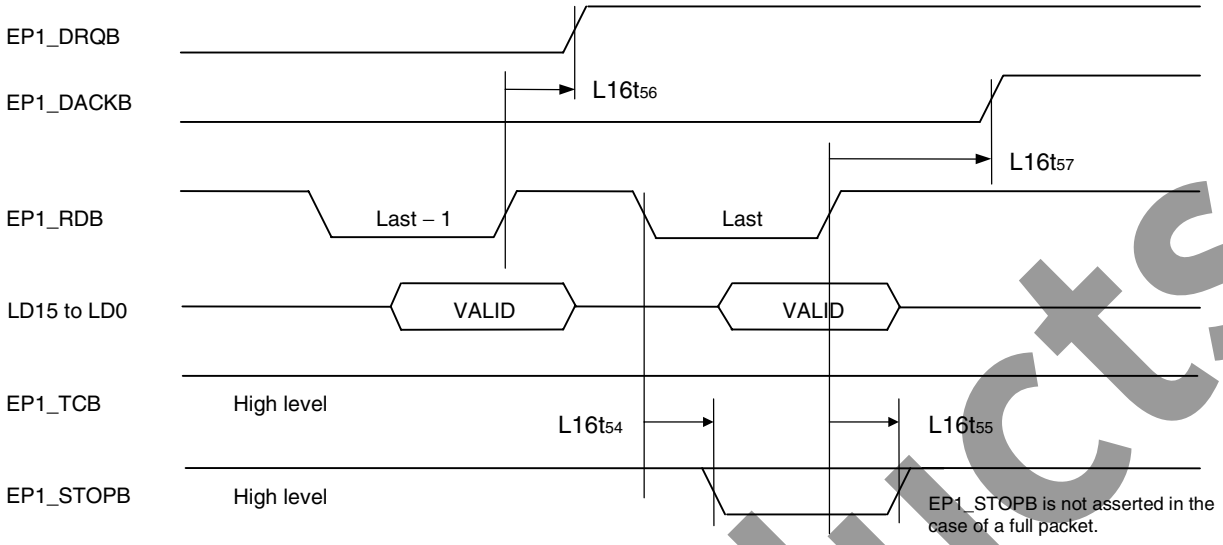
(Overall)



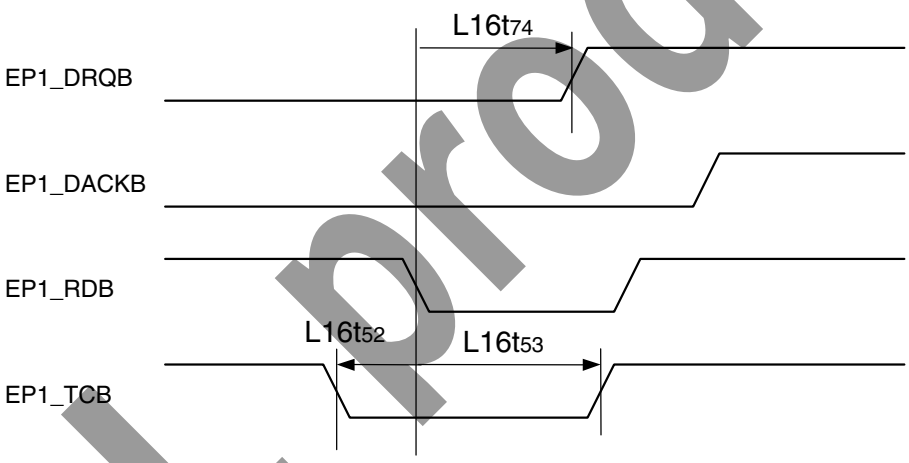
(Start timing)



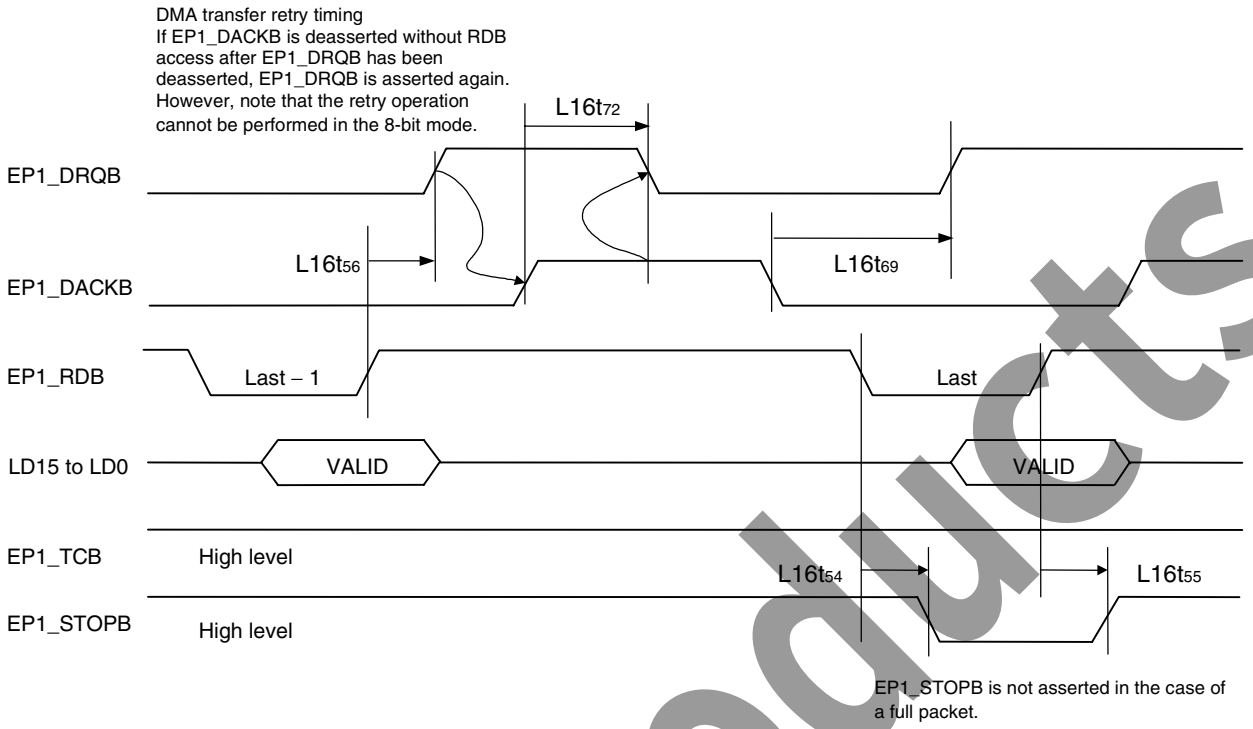
(End timing)



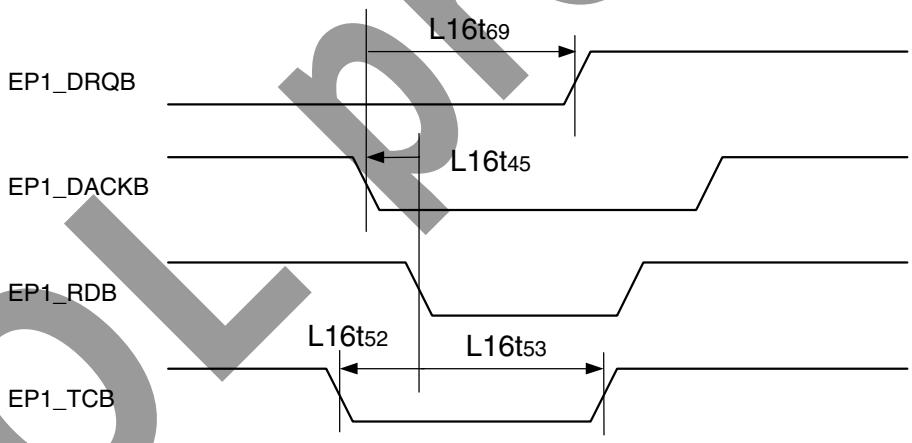
(TCB timing)



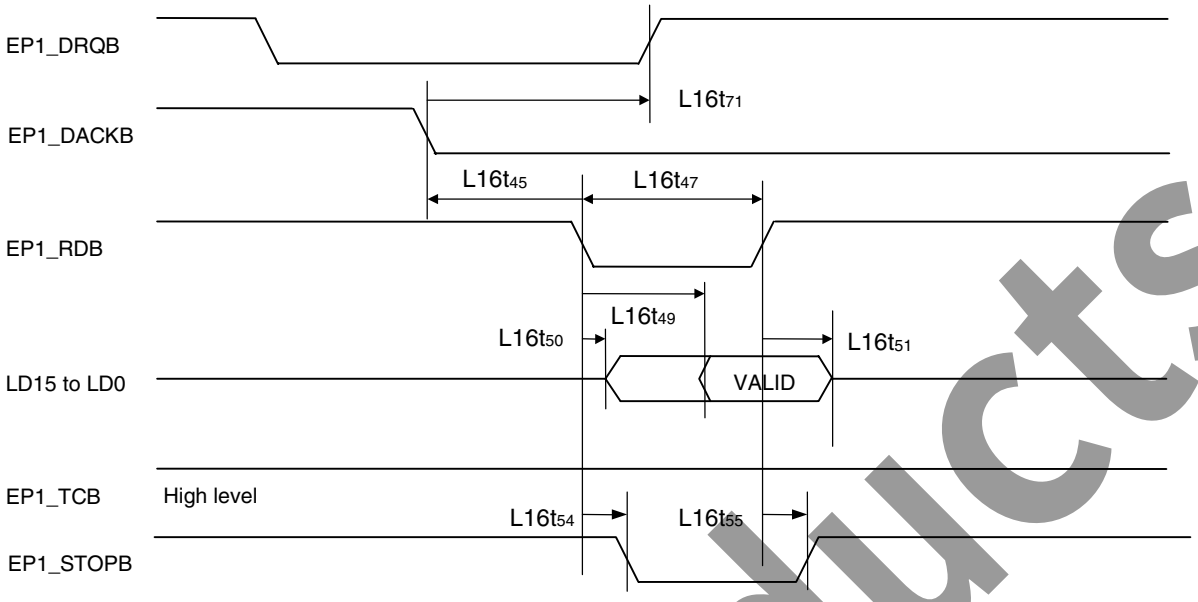
(Retransmission timing)



(If EP1_TCB is input when retransmission is executed)



(One-cycle transfer)



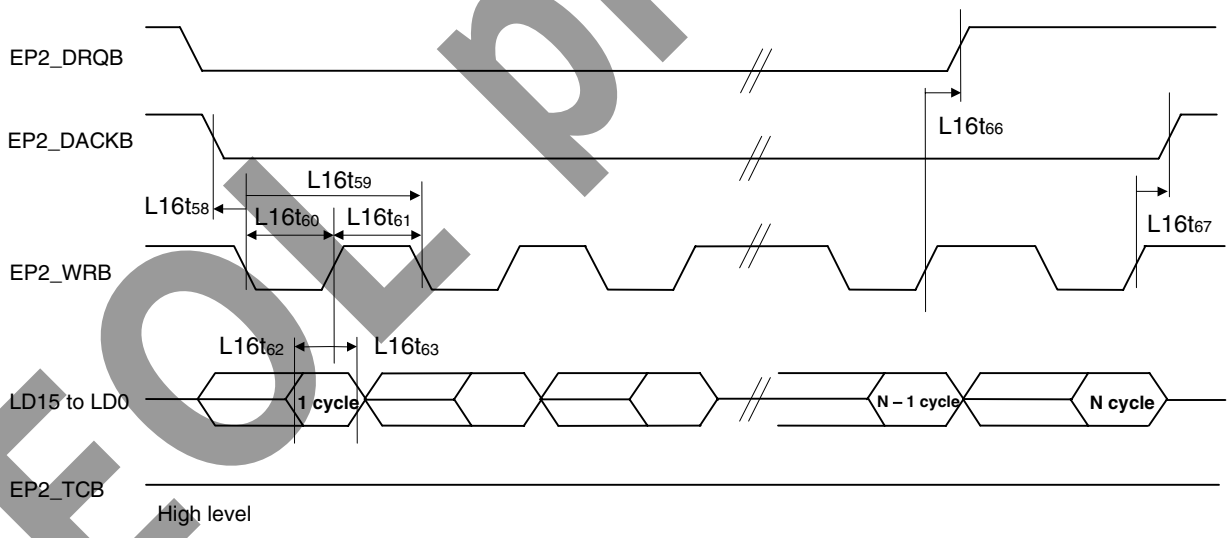
(d) External local bus 16-bit mode DMA demand write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T58	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L16T59	DMA demand mode write transfer cycle time	72		∞	ns
L16T60	Write command width	38		∞	ns
L16T61	Write command inactive time	34		∞	ns
L16T62	Write data setup time (EP2_WRB↑)	10		∞	ns
L16T63	Write data hold time (EP2_WRB↑)	0		∞	ns
L16T64	EP2_TCB setup time (EP2_WRB↓)	0		**Note**	ns
L16T65	EP2_TCB hold time (EP2_WRB↓)	17		∞	ns
L16T66	DMA request off time (EP2_WRB↑)	–		60	ns
L16T67	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns
L16T70	DMA request off time (EP2_DACKB↓)	–		38	ns
L16T73	DMA request on time (EP2_DACKB↑)	–		88	ns
L16T75	DMA request off time (EP2_WRB↓)	–		60	ns

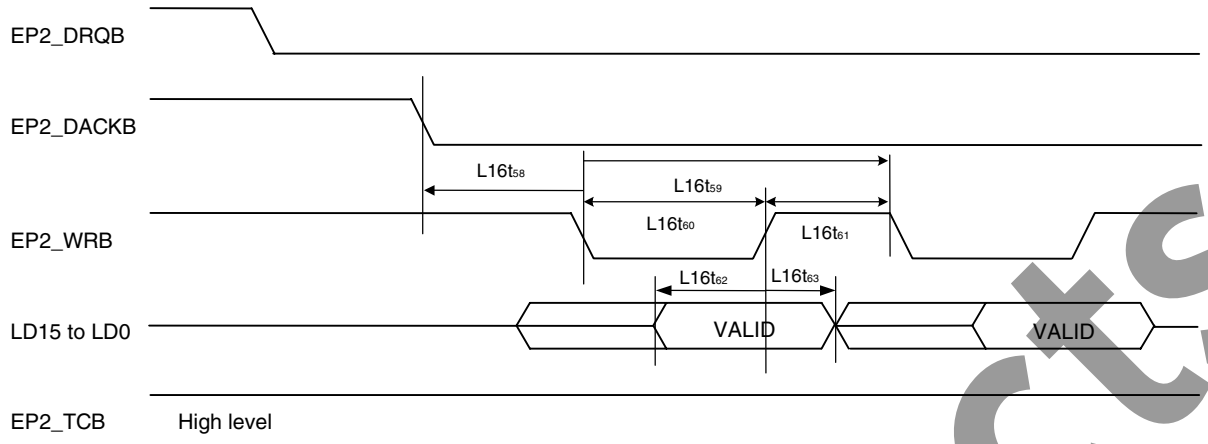
Note Can be input after previous EP2_WRB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

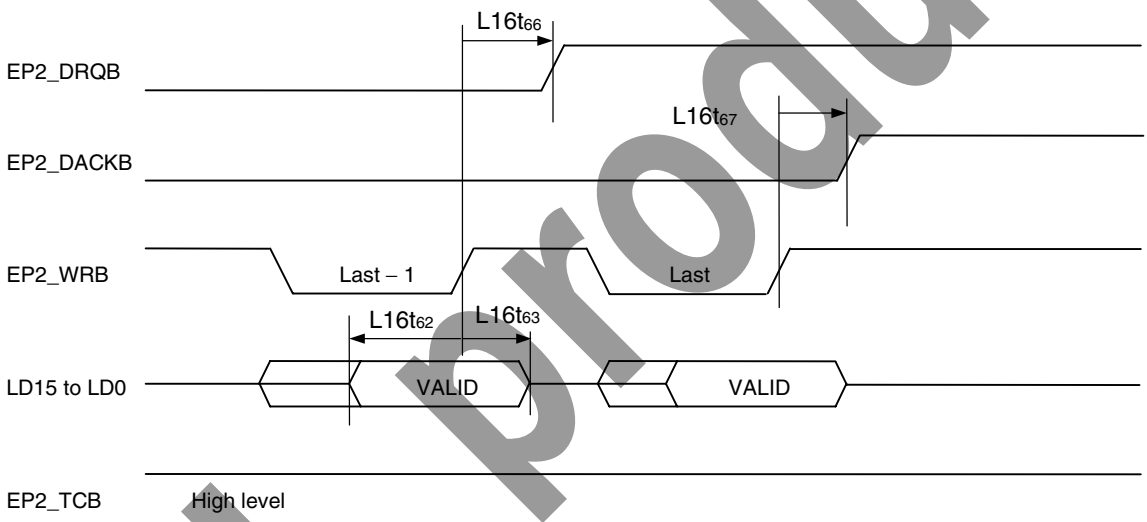
(Overall)



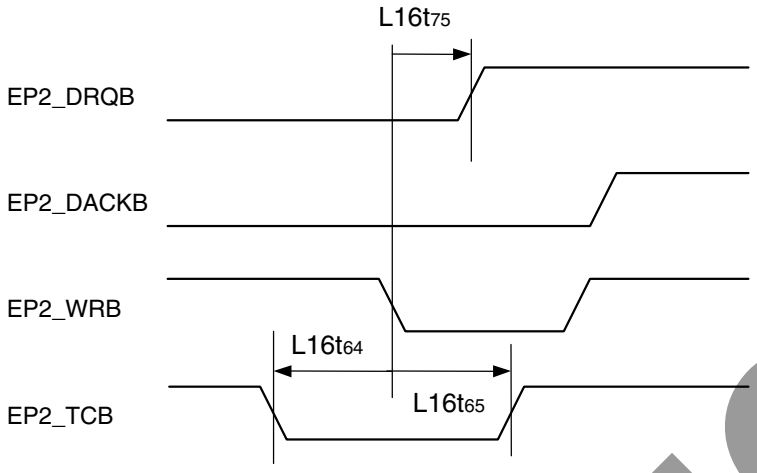
(Start timing)



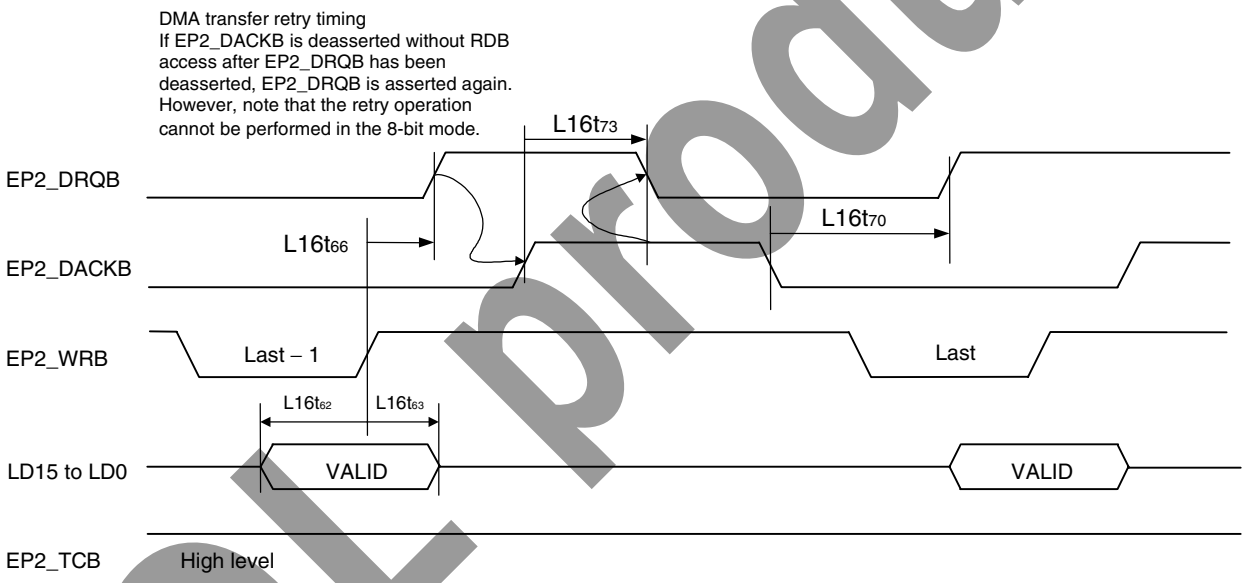
(End timing)



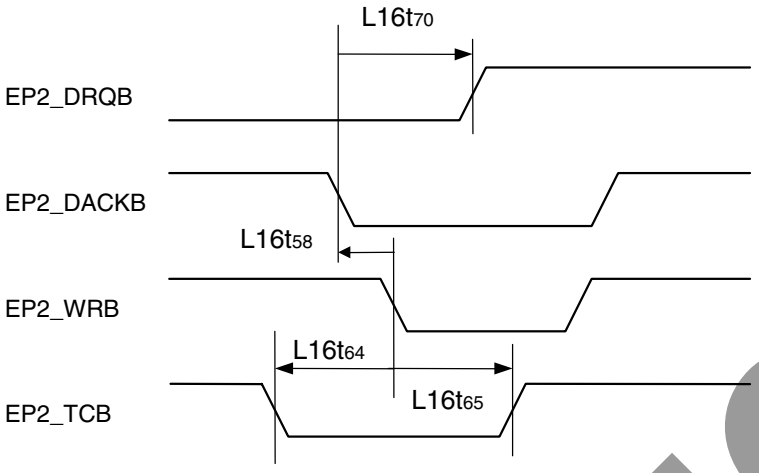
(TCB timing)



(Retransmission timing)



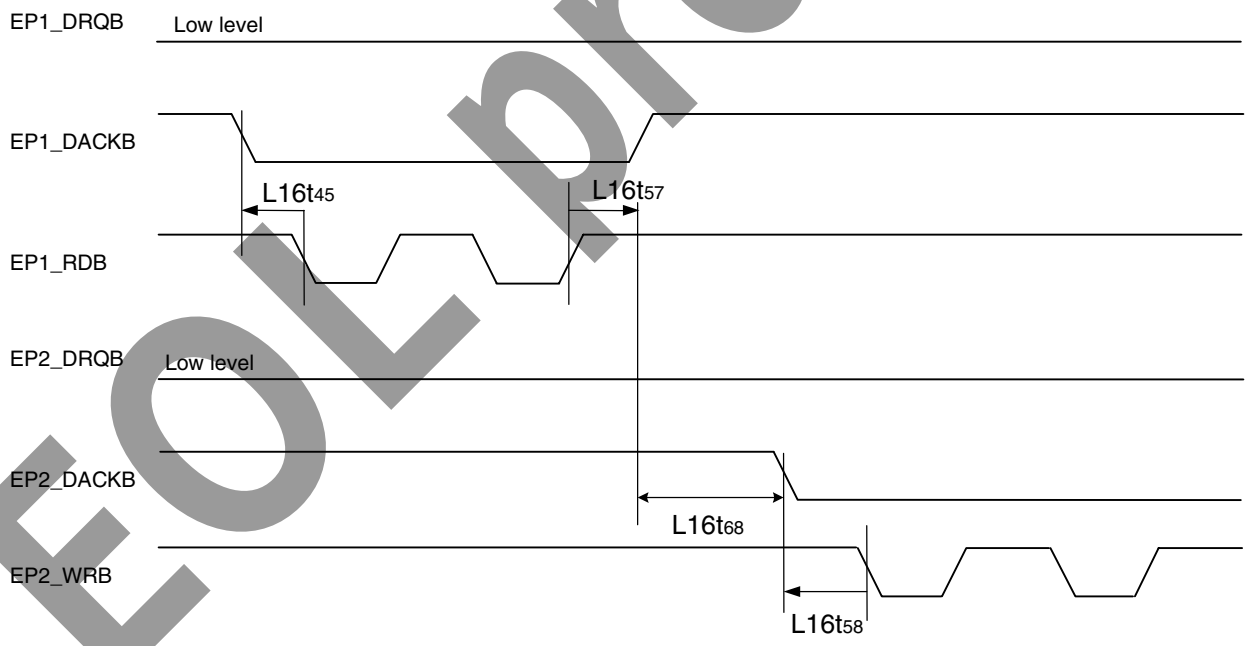
(If EP1_TCB is input when retransmission is executed)



(e) External local bus 16-bit mode DMA EP1_Read transfer vs. EP2_Write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T68	EP1_RDB vs. EP2_WRB command inactive time	34		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).



(2) External local bus 8-bit mode

(a) External local bus 8-bit mode DMA single mode read transfer timing

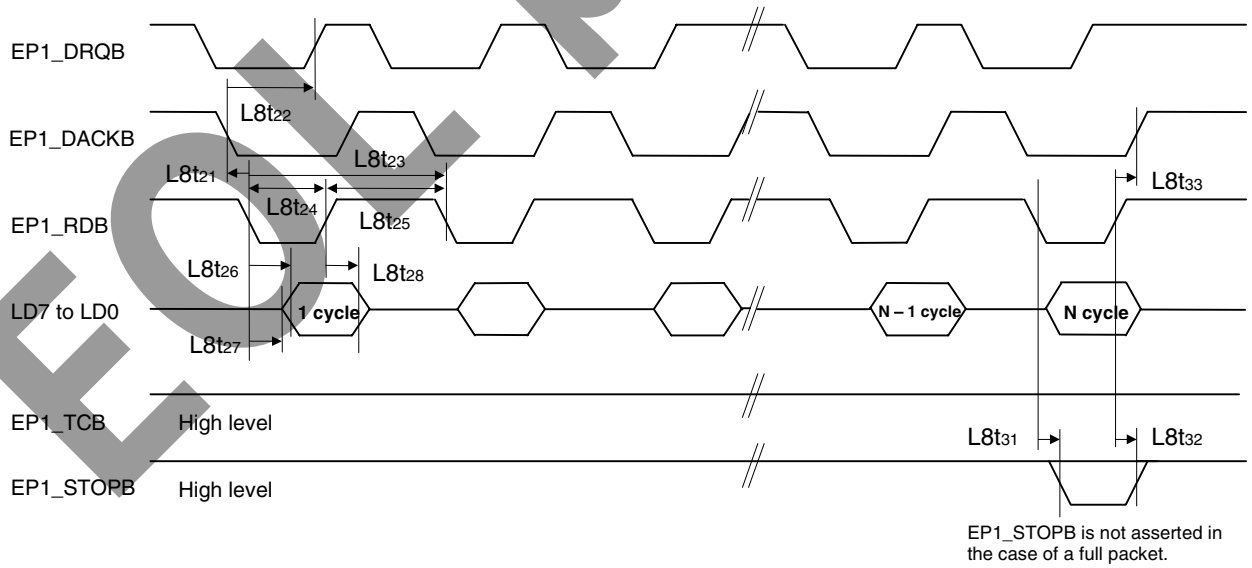
Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T21	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L8T22	DMA request off time 1 (EP1_DACKB↓)	–		10	ns
L8T23	DMA single mode read transfer cycle time	91		∞	ns
L8T24	Read command width	57		∞	ns
L8T25	Read command inactive time	34		∞	ns
L8T26	Read data delay time (EP1_RDB↓)	–		57	ns
L8T27	Buffer direction change time (EP1_RDB↓)	–		14	ns
L8T28	Read data hold time (EP1_RDB↑)	4		–	ns
L8T31	EP1_STOPB delay time (EP1_RDB↓)	–		15	ns
L8T32	EP1_STOPB delay time (EP1_RDB↑)	3		–	ns
L8T33	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns
L8T34	Undefined	–		–	ns

Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

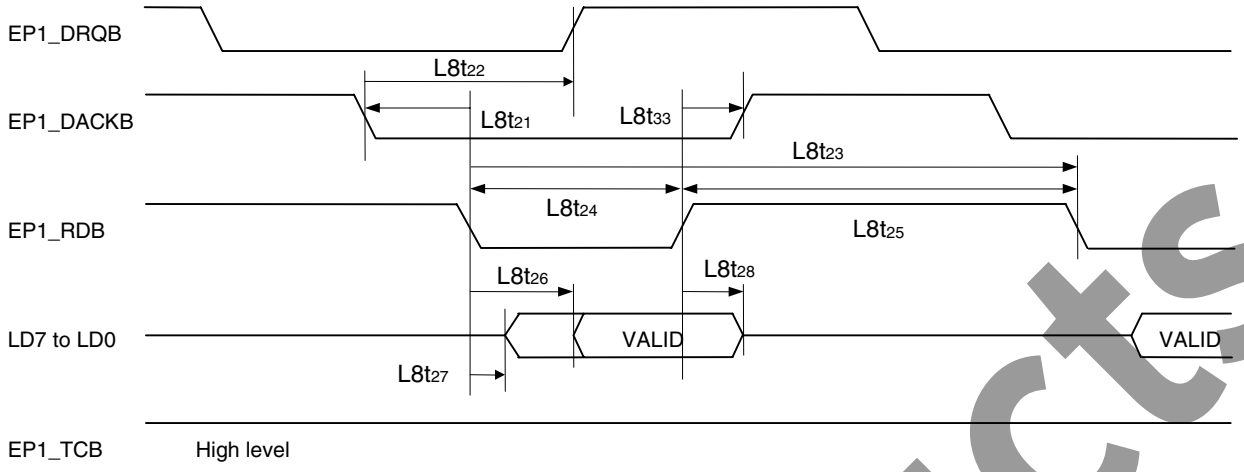
2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

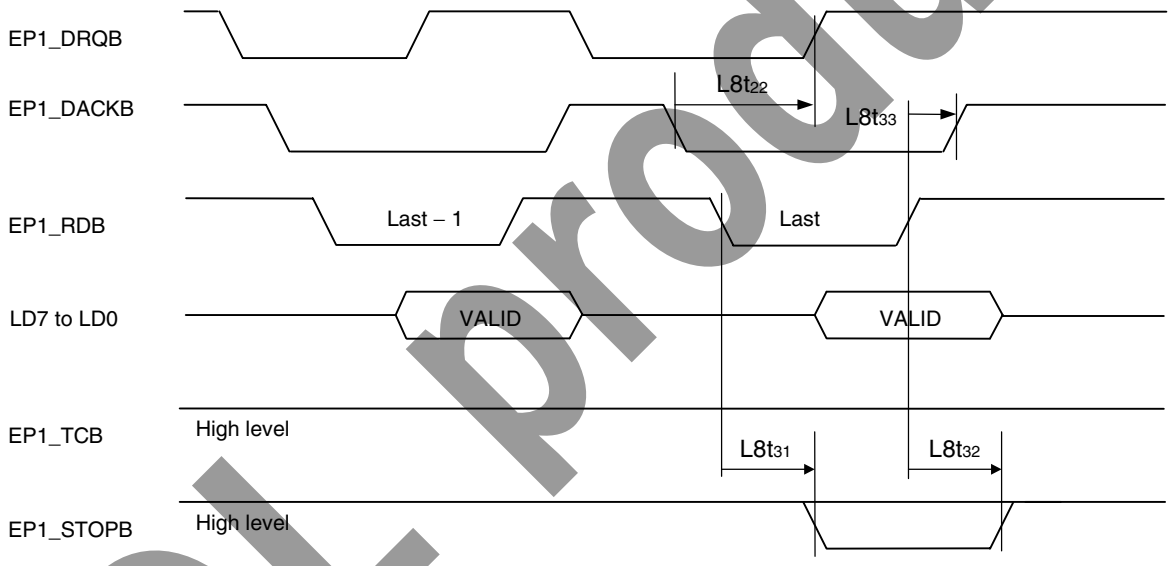
(Overall)



(Start timing)



(End timing)



EP1_STOPB is not asserted in the case of a full packet.

(b) External local bus 8-bit mode DMA single mode write transfer

Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T35	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L8T36	DMA request off time 1 (EP2_DACKB↓)	–		54[Note]	ns
L8T37	DMA single mode write transfer cycle time	88		∞	ns
L8T38	Write command width	54		∞	ns
L8T39	Write command inactive time	34		∞	ns
L8T40	Write data setup time (EP2_WRB↑)	10		∞	ns
L8T41	Write data hold time (EP2_WRB↑)	0		∞	ns
L8T44	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns

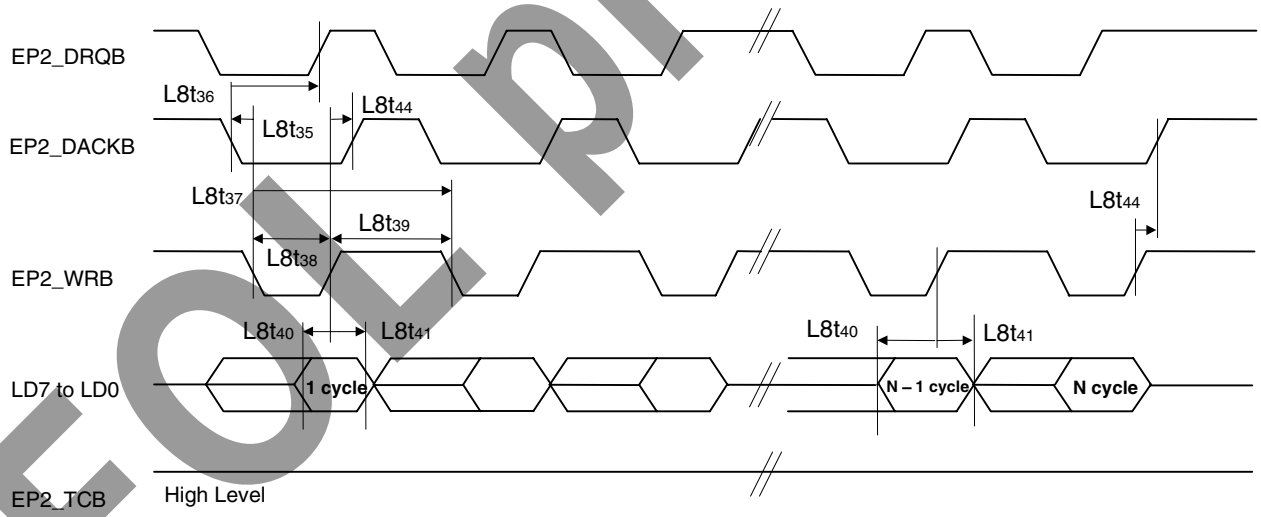
Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

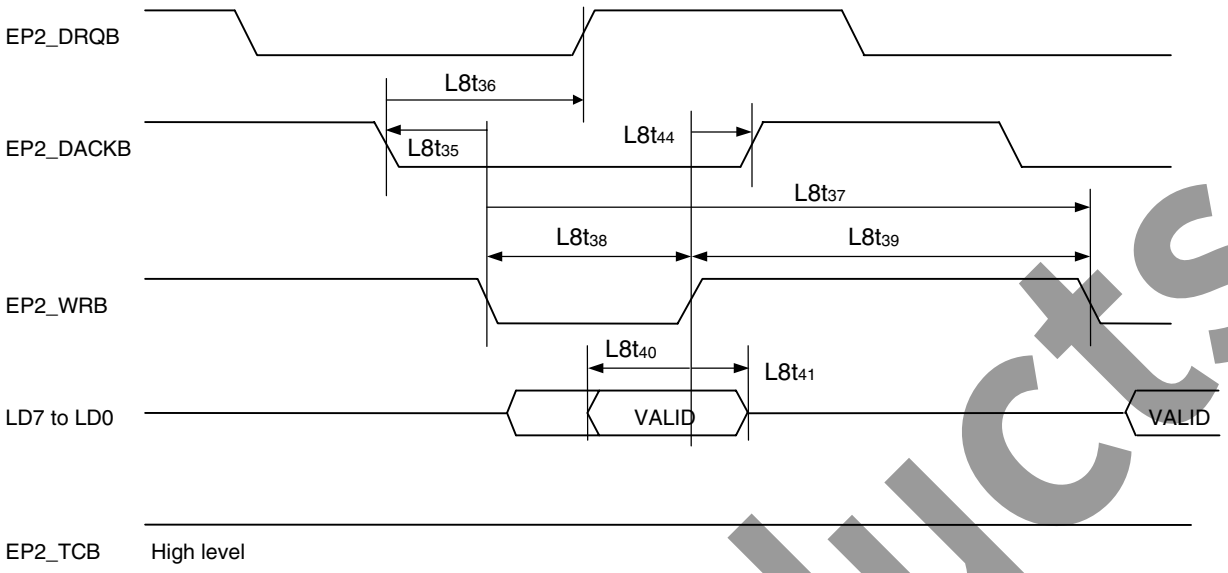
3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

Note The difference in specifications when compared with L8T22 is that BIU processing is performed for EP1 and that EPC2 processing is performed for EP2.

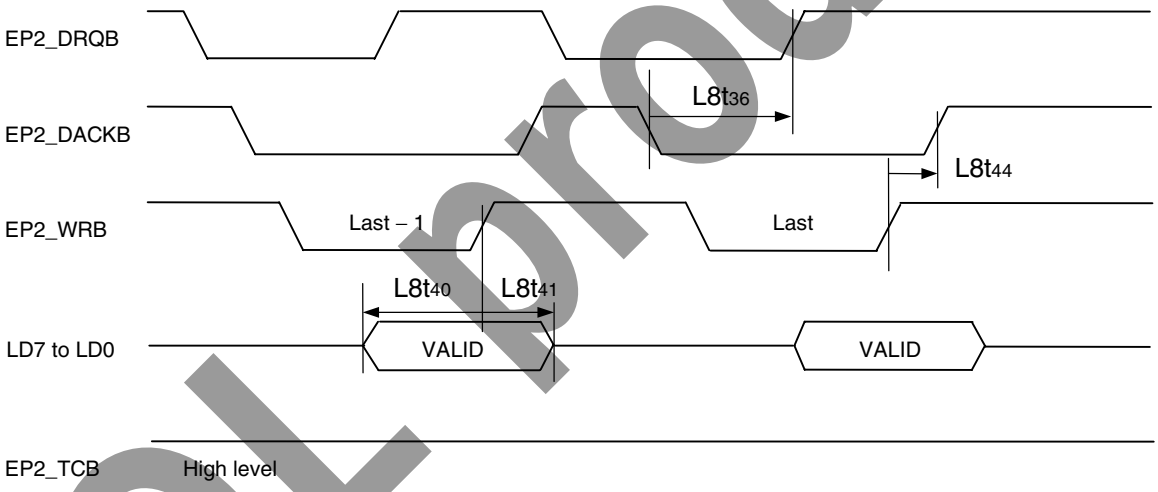
(Overall)



(Start timing)



(End timing)



(c) External local bus 8-bit mode DMA demand read transfer timing

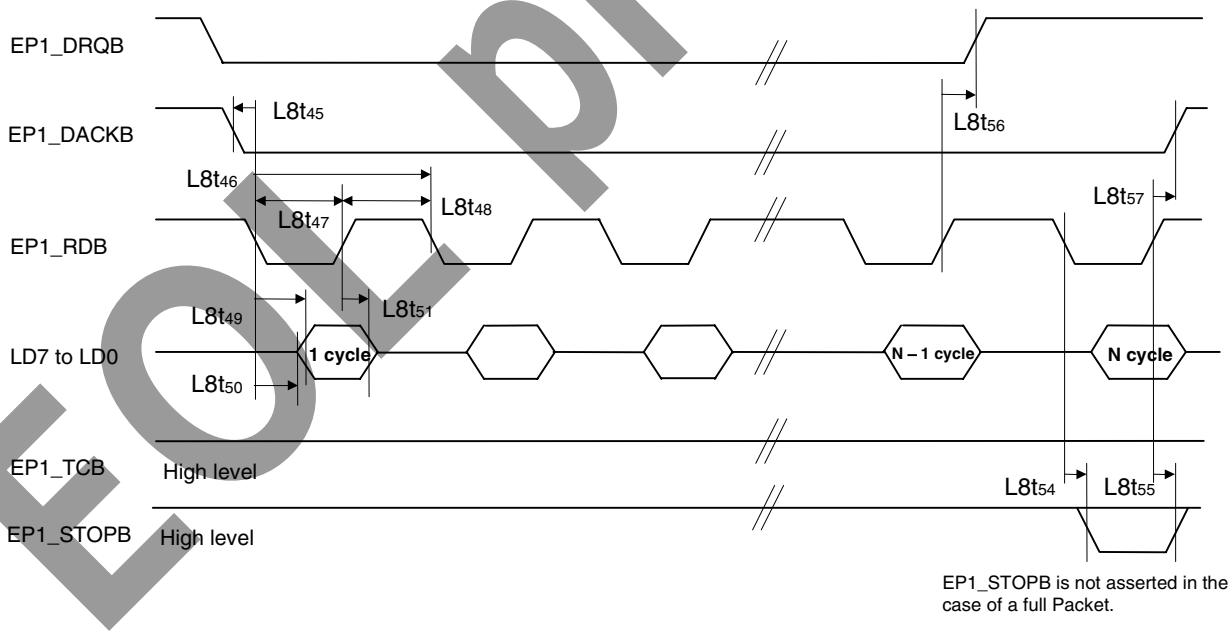
Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T45	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L8T46	DMA demand mode read transfer cycle time	90		∞	ns
L8T47	Read command width	56		∞	ns
L8T48	Read command inactive time	34		∞	ns
L8T49	Read data delay time (EP1_RDB↓)	–		56	ns
L8T50	Buffer direction change time (EP1_RDB↓)	–		14	ns
L8T51	Read data hold time (EP1_RDB↑)	4		–	ns
L8T54	EP1_STOPB delay time (EP1_RDB↓)	–		15	ns
L8T55	EP1_STOPB delay time (EP1_RDB↑)	3		–	ns
L8T56	DMA request off time (EP1_RDB↑)	–		60	ns
L8T57	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns

Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

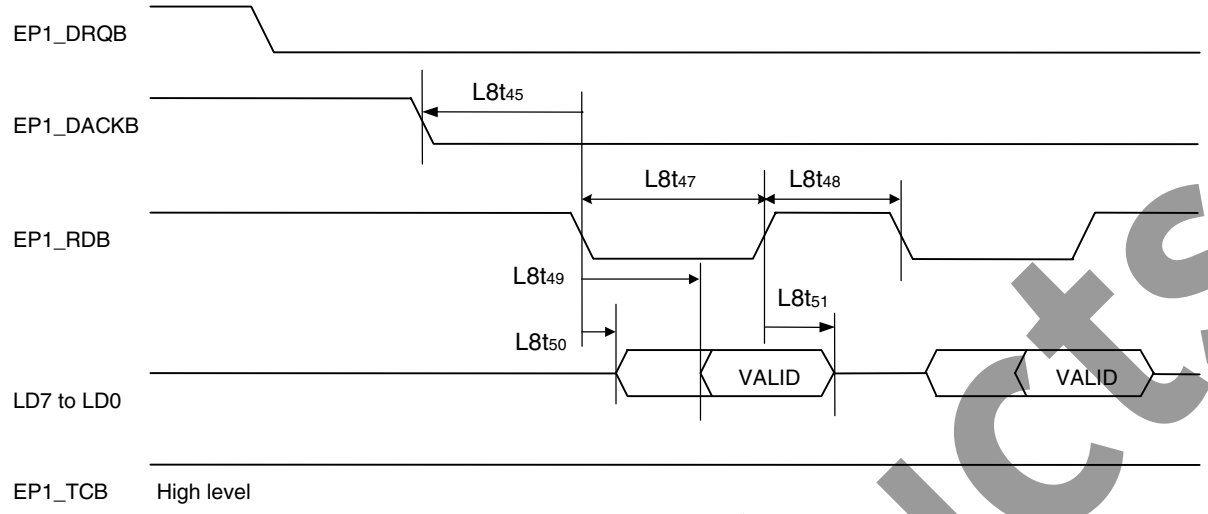
2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

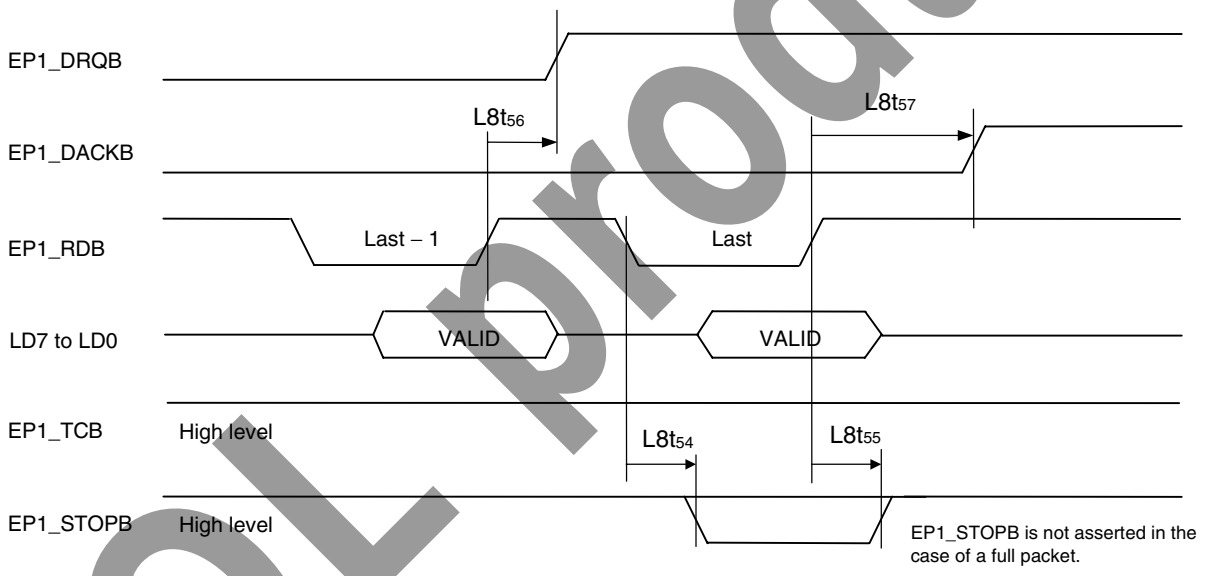
(Overall)



(Start timing)



(End timing)



(d) External local bus 8-bit mode DMA demand write transfer timing

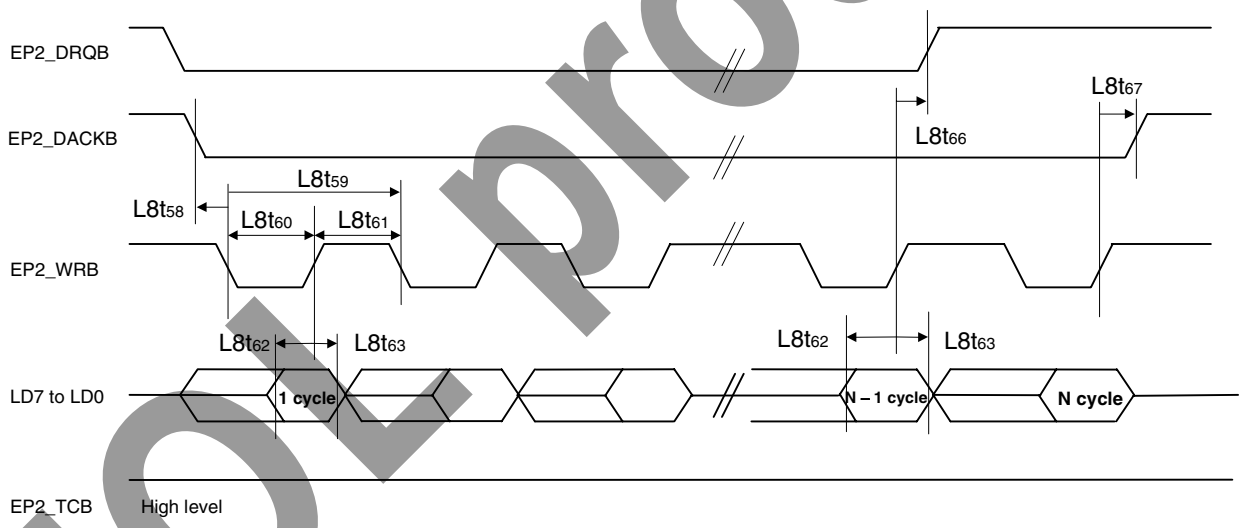
Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T58	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L8T59	DMA demand mode write transfer cycle time	72		∞	ns
L8T60	Write command width	38		∞	ns
L8T61	Write command inactive time	34		∞	ns
L8T62	Write data setup time (EP2_WRB↑)	10		∞	ns
L8T63	Write data hold time (EP2_WRB↑)	0		∞	ns
L8T66	DMA request off time (EP2_WRB↑)	–		60	ns
L8T67	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns

Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

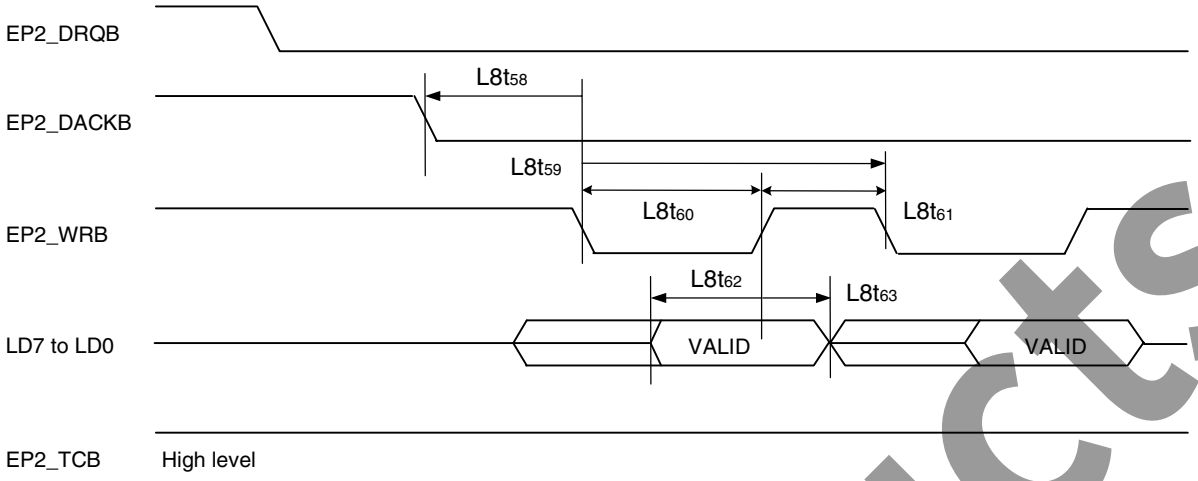
2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

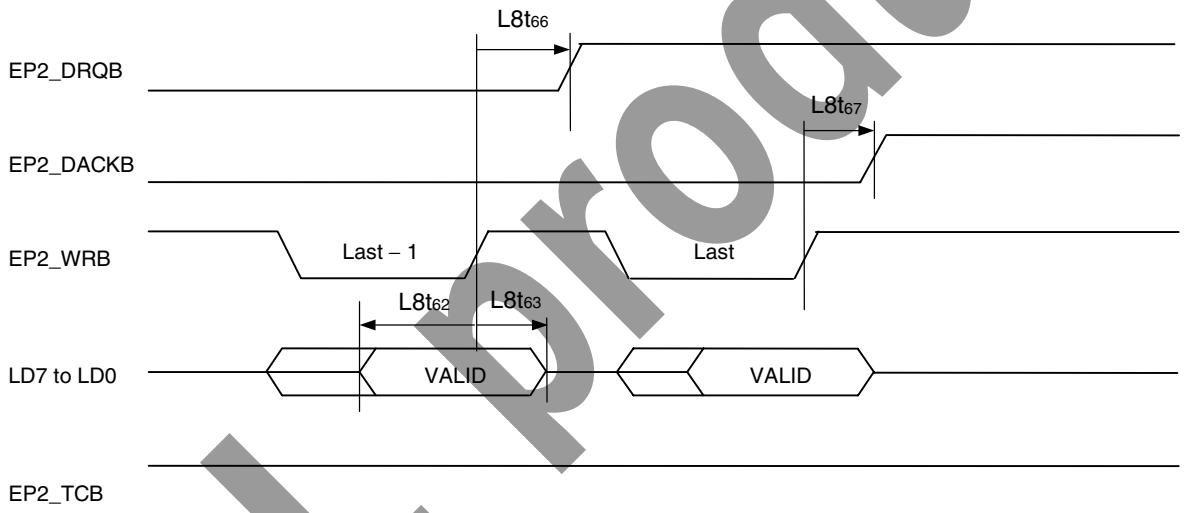
(Overall)



(Start timing)



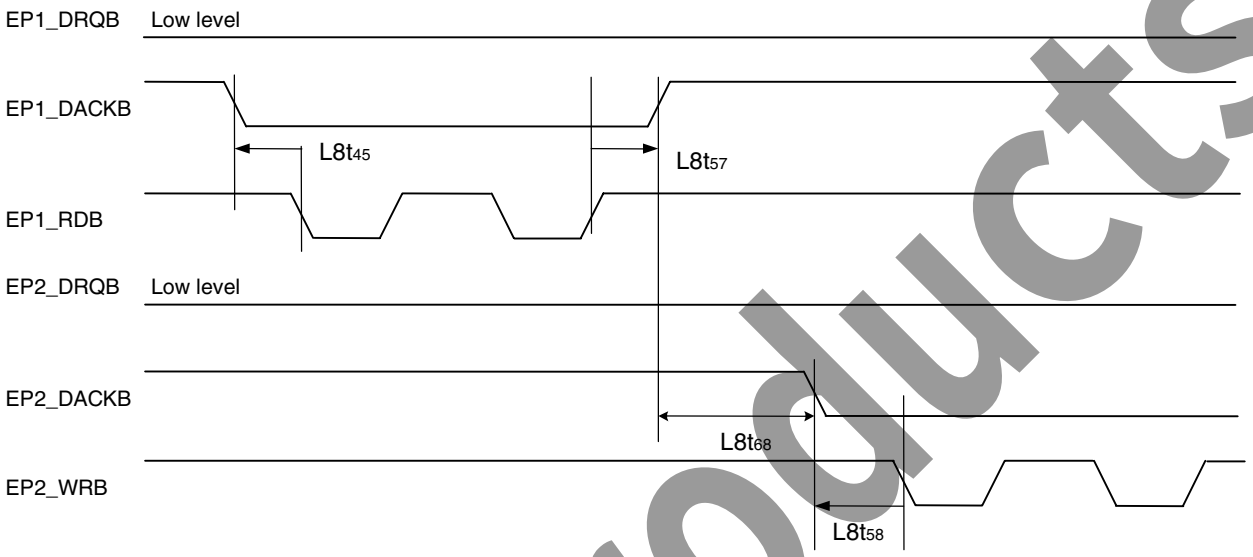
(End timing)



(e) External local bus 8-bit mode DMA EP1_Read transfer vs. EP2_Write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T68	EP1_RDB vs. EP2_WRB command inactive time	34		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).



2.6.5 USB interface timing

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed source electrical characteristics					
Rise time	T_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time	T_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	T_{FRFM}	(T_{FR}/T_{FF})	90	111.11	%
Full-speed data rate for hubs and devices that are high-speed capable	$T_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mb/s
Frame interval	T_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	T_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance):					
To next transition	T_{DJ1}		−3.5	3.5	ns
For paired transitions	T_{DJ2}		−4.0	4.0	ns
Source jitter for differential transition to SE0 transition	T_{FDEOP}		−2	5	ns
Receiver jitter:					
To next transition	T_{JR1}		−18.5	18.5	ns
For paired transitions	T_{JR2}		−9	9	ns
Source SE0 interval of EOP	T_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	T_{FEOPR}		82		ns
Width of SE0 interval during differential transition	T_{FST}			14	ns
High-speed source electrical characteristics					
Rise time (10% to 90%)	T_{HSR}		500		ps
Fall time (10% to 90%)	T_{HSF}		500		ps
Driver waveform requirements	See Figure 2-6				
High-speed data rate	T_{HSDRAT}		479.760	480.240	Mb/s
Microframe interval	T_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	T_{HSRFI}			4 high-speed	Bit times
Data source jitter	See Figure 2-6.				
Receiver jitter tolerance	See Figure 2-4.				

Parameter	Symbol	Conditions	Min.	Max.	Unit
Device event timing					
Time from internal power good to device pulling D+/D– beyond V_{IHZ} (min.) (signaling attach)	T_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach	T_{ATTDB}			100	ms
Inter-packet delay (for low-/full-speed)	T_{IPD}		2		Bit times
Inter-packet delay for device response w/detachable cable for low-/full-speed	$T_{RSPIPD1}$			6.5	Bit times
High-speed detection start time from suspend	T_{SCA}		2.5		μs
Sample time for suspend vs. reset	T_{CSR}		100	875	μs
Power down under suspend	T_{SUS}			10	ms
SUSPEND set time (SPNDOUT)	T_{SSP}		0	–	
SUSPEND clear time (RSUMOUT)	T_{CSP}		0	–	
Reversion time from suspend to high-speed	T_{RHS}			1.333	μs
SUSPEND setup time (RSUMIN)	T_{SRW}		0	–	
RSUMIN active pulse width	T_{RWP}		1	15	ms
Drive chirp K width	T_{CKO}		1		ms
Finish chirp K assertion	T_{FCA}			7	ms
Start sequencing chirp K-J-K-J-K-J	T_{SSC}			100	μs
Finish sequencing chirp K-J	T_{FSC}		–500	–100	μs
Detect sequencing chirp K-J width	T_{CSI}		2.5		μs
Sample time for sequencing chirp	T_{SCS}		1.0	2.5	ms
Reversion time to high-speed	T_{RHA}			500	μs
High-speed detection start time	T_{HDS}		2.5	3000	μs
Reset completed time	T_{DRS}		10		ms

Figure 2-6. Transmit Waveform for Transceiver at D+/D–

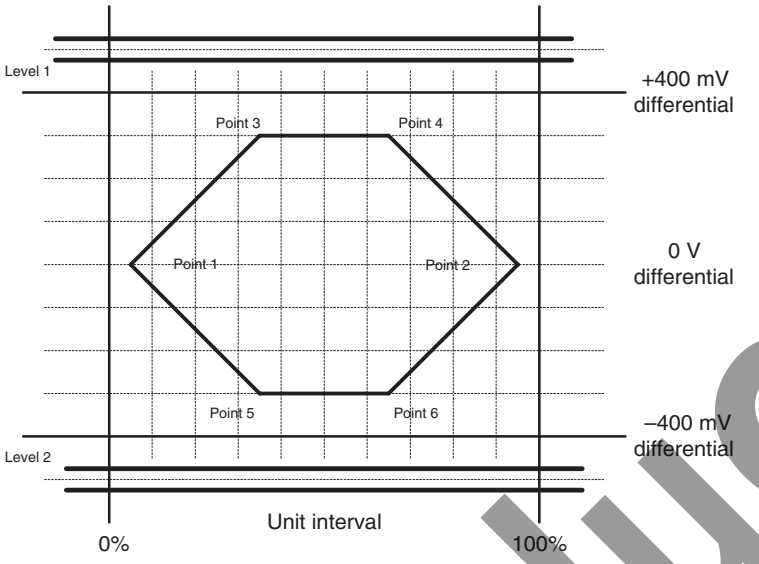
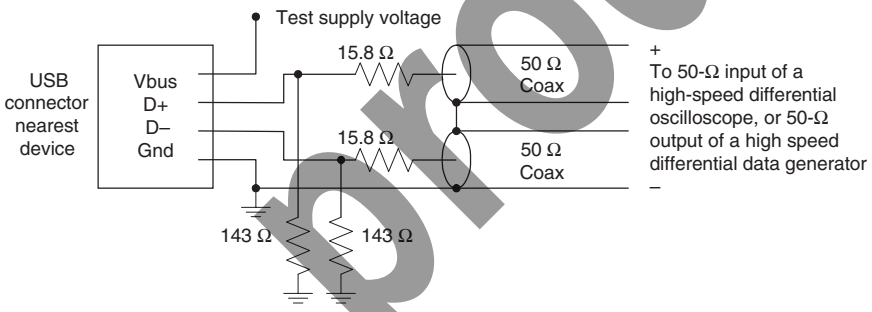
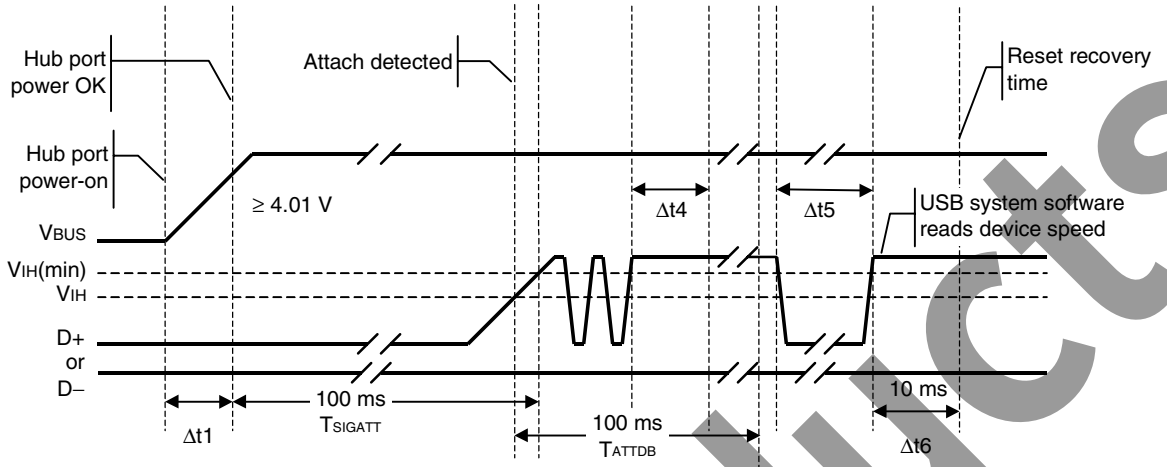


Figure 2-7. Transmitter Measurement Fixtures



(1) Power-on and connection events

Figure 2-8. Power-on and Connection Event Timing



(2) USB signals

Figure 2-9. USB Differential Data Jitter for Full-Speed

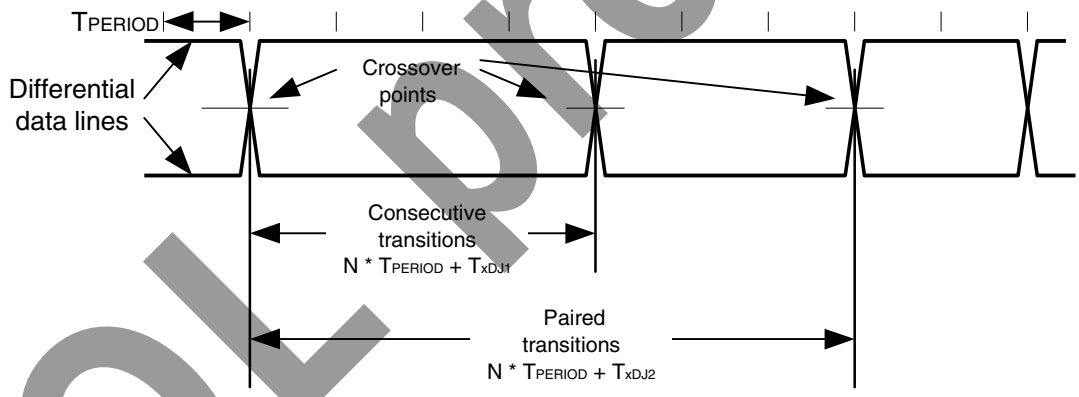


Figure 2-10. USB Differential-to-EOP Transition Skew and EOP Width for Full-Speed

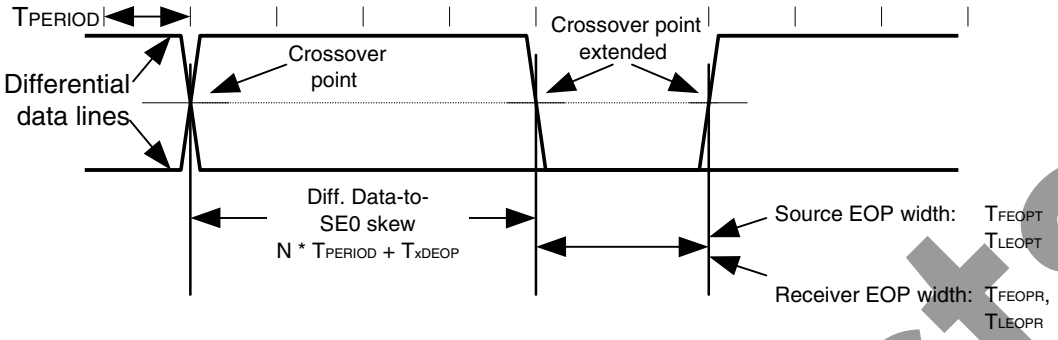
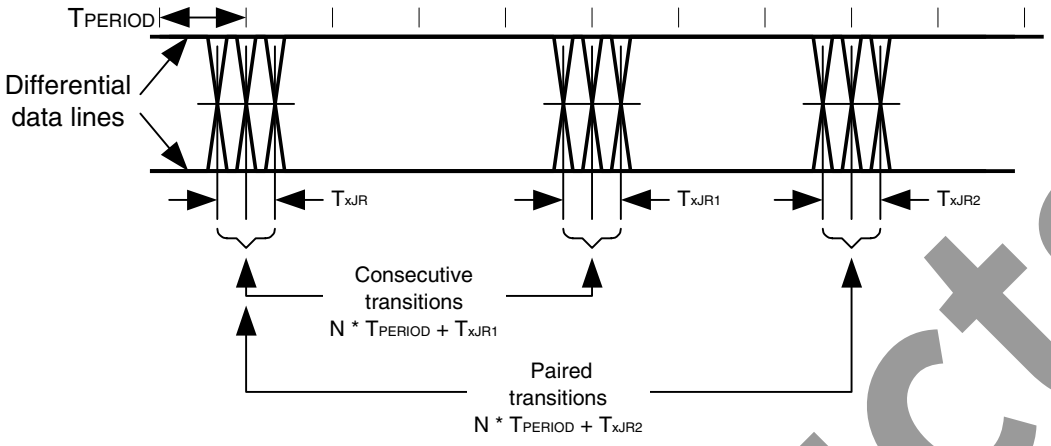


Figure 2-11. USB Receiver Jitter Tolerance for Full-Speed

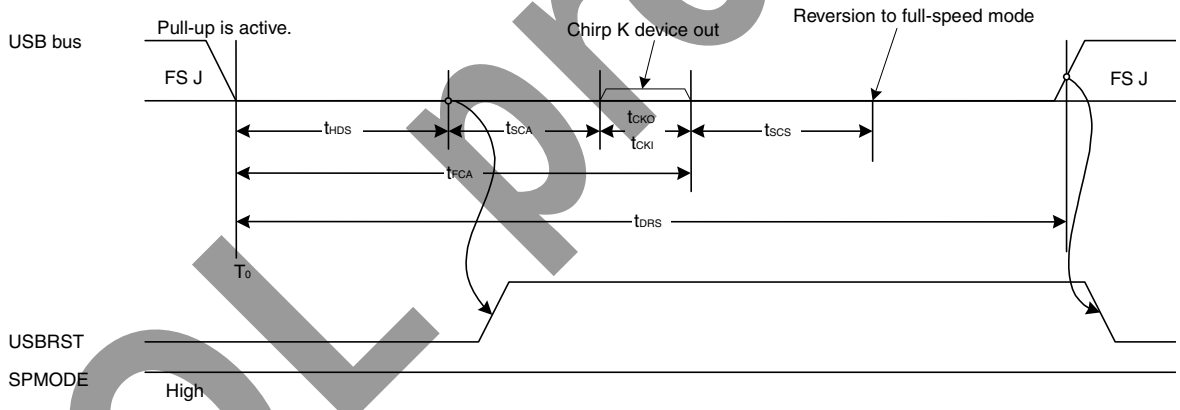


(3) USB connection sequence on USB1.1 bus

The PHY core implemented on the μPD720122 automatically determines the Up port.

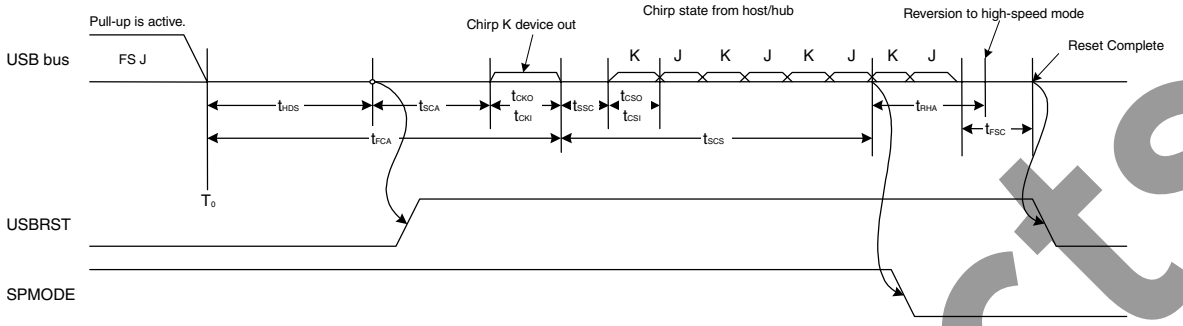
Check the SP_MODE bit (SP_MODE) of the Int Status 2 register after an EPC2_STG bus reset interrupt has occurred to determine whether the USB is connected to FS or HS.

Figure 2-12. USB Connection Sequence on USB 1.1 Bus



(4) USB connection sequence on USB 2.0 bus

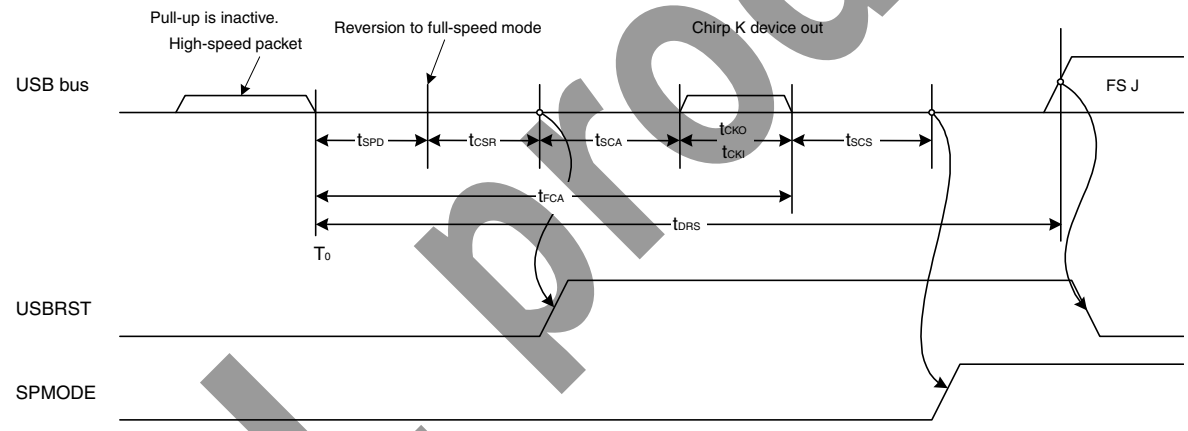
Figure 2-13. USB Connection Sequence on USB 2.0 Bus



(5) Bus reset sequence (1)

The bus reset sequence when connected to a USB 1.1 bus is shown below.

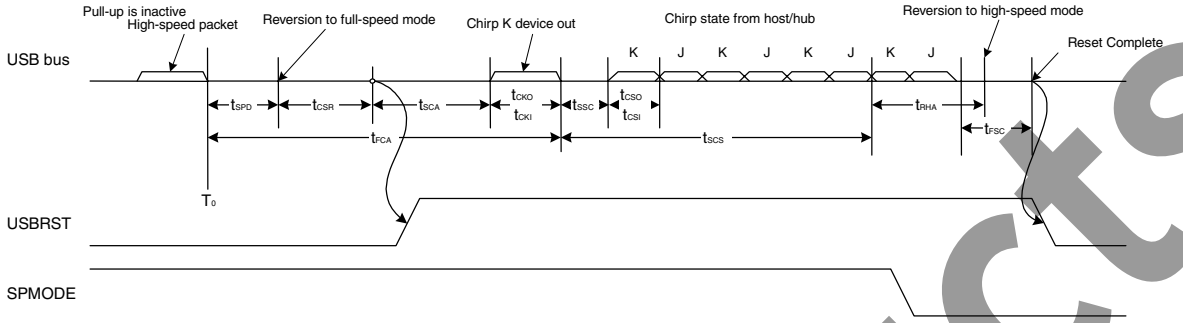
Figure 2-14. Bus Reset Sequence (1)



(6) Bus reset sequence (2)

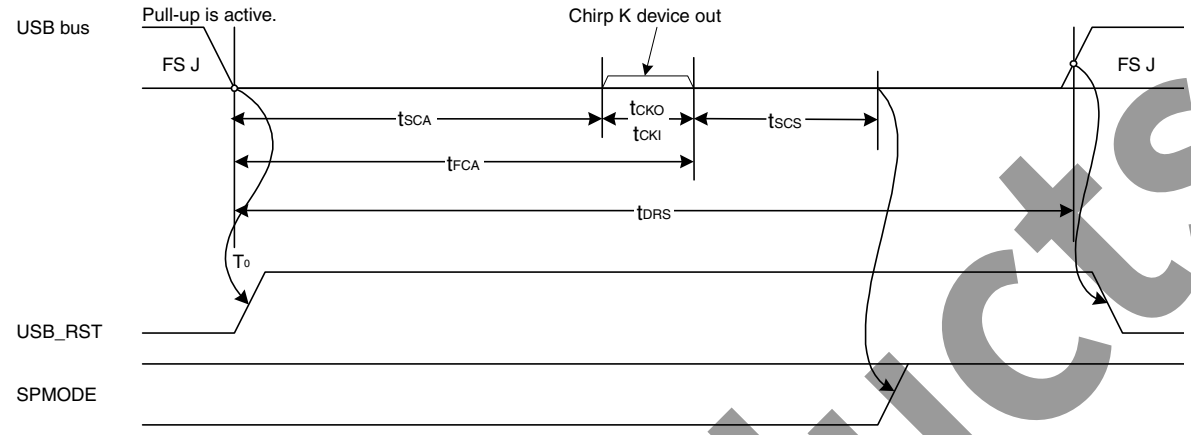
The bus reset sequence when connected to a USB 2.0 bus is shown below.

Figure 2-15. Bus Reset Sequence (2)



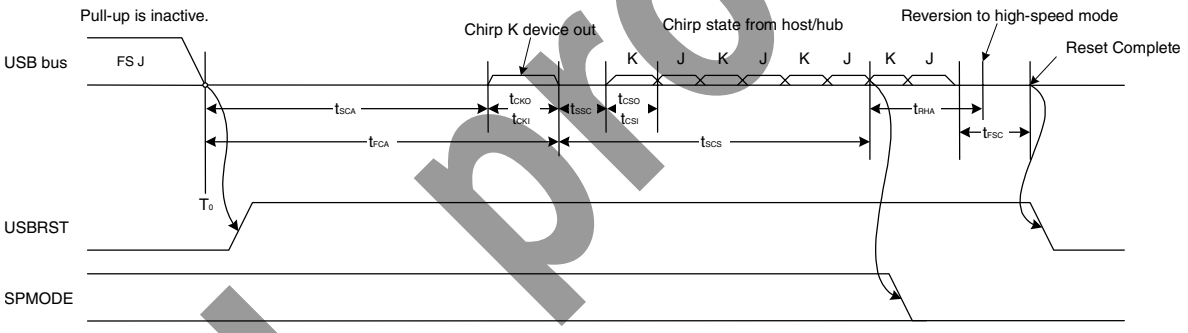
(7) USB reset from suspend state (1)

Figure 2-16. USB Reset from Suspend State (1)



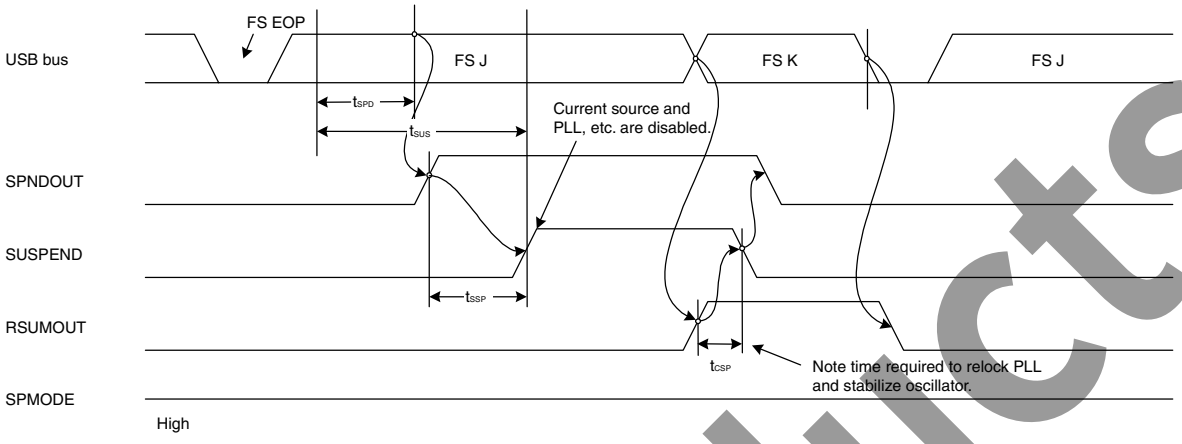
(8) USB reset from suspend state (2)

Figure 2-17. USB Reset from Suspend State (2)



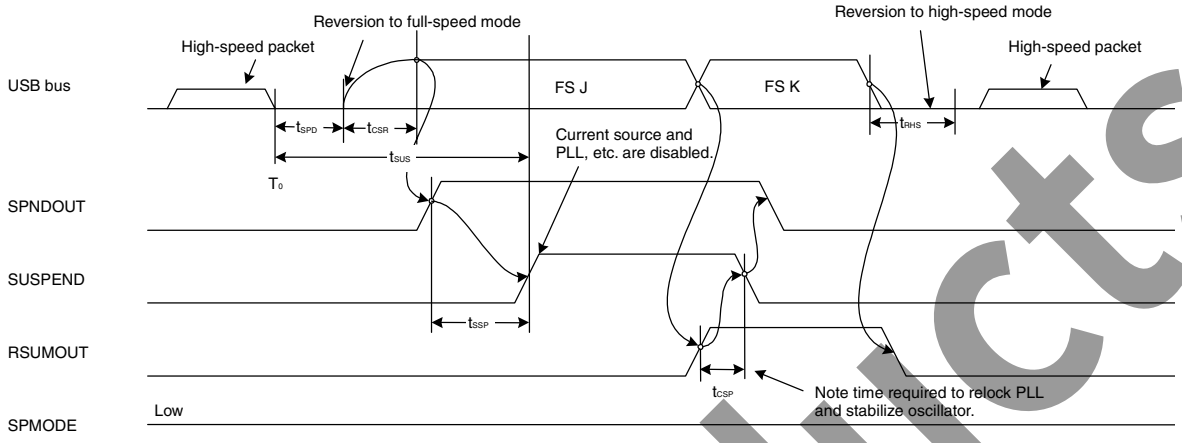
(9) Suspend and resume on USB1.1 bus

Figure 2-18. Suspend and Resume on USB 1.1 Bus



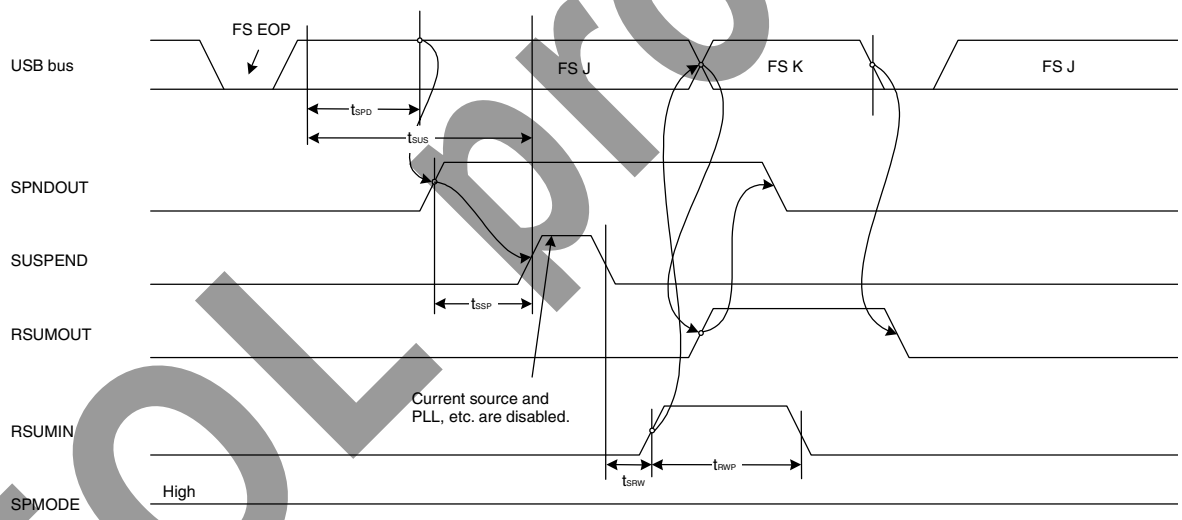
(10) Suspend and resume on USB2.0 bus

Figure 2-19. Suspend and Resume on USB 2.0 Bus



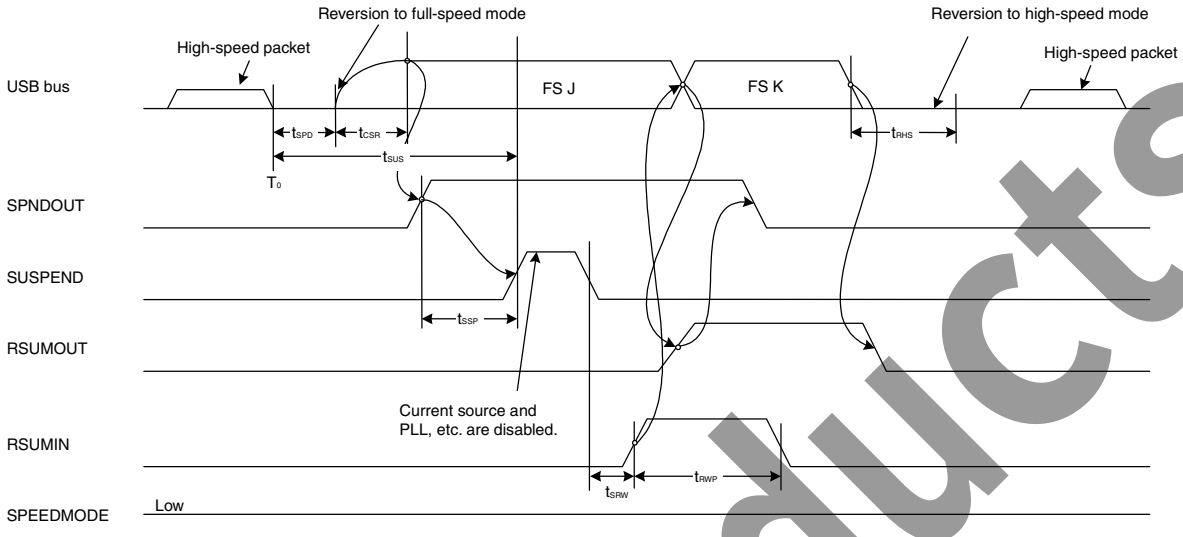
(11) Remote wakeup on USB1.1

Figure 2-20. Remote Wakeup on USB 1.1



(12) Remote wakeup on USB2.0

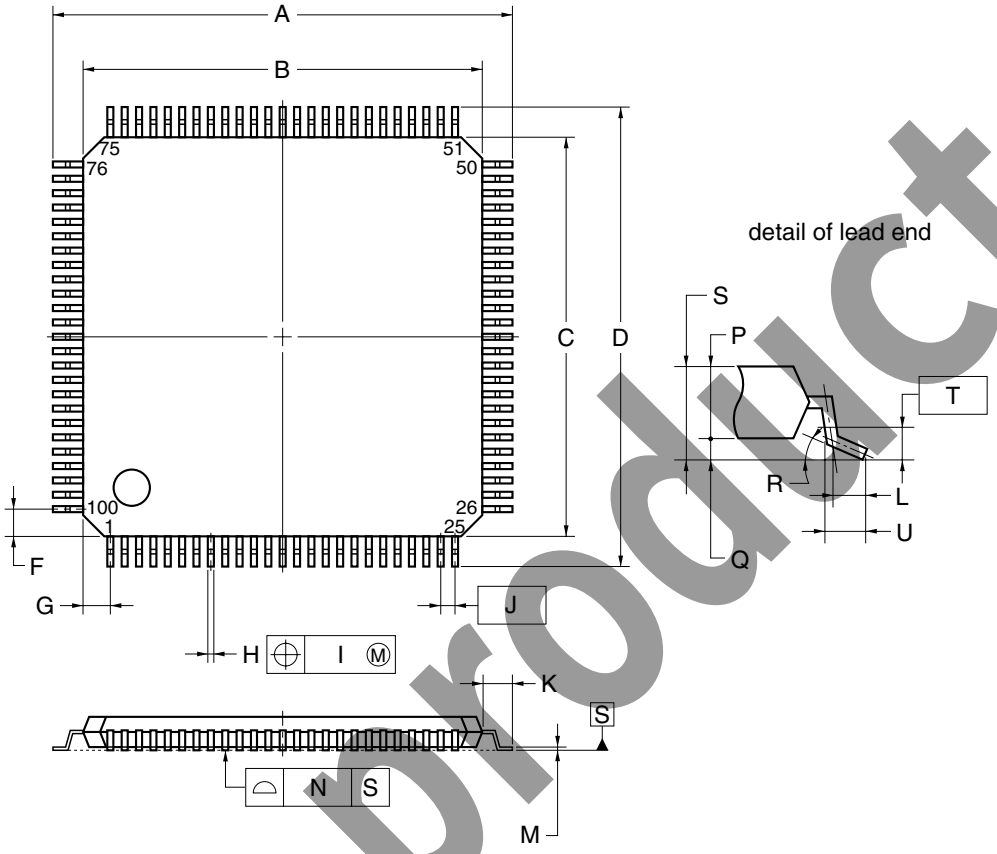
Figure 2-21. Remote Wakeup on USB 2.0



3. PACKAGE DRAWING

★ • μPD720122GC-9EU, 720122GC-9EU-A

100-PIN PLASTIC TQFP (FINE PITCH) (14x14)



NOTE

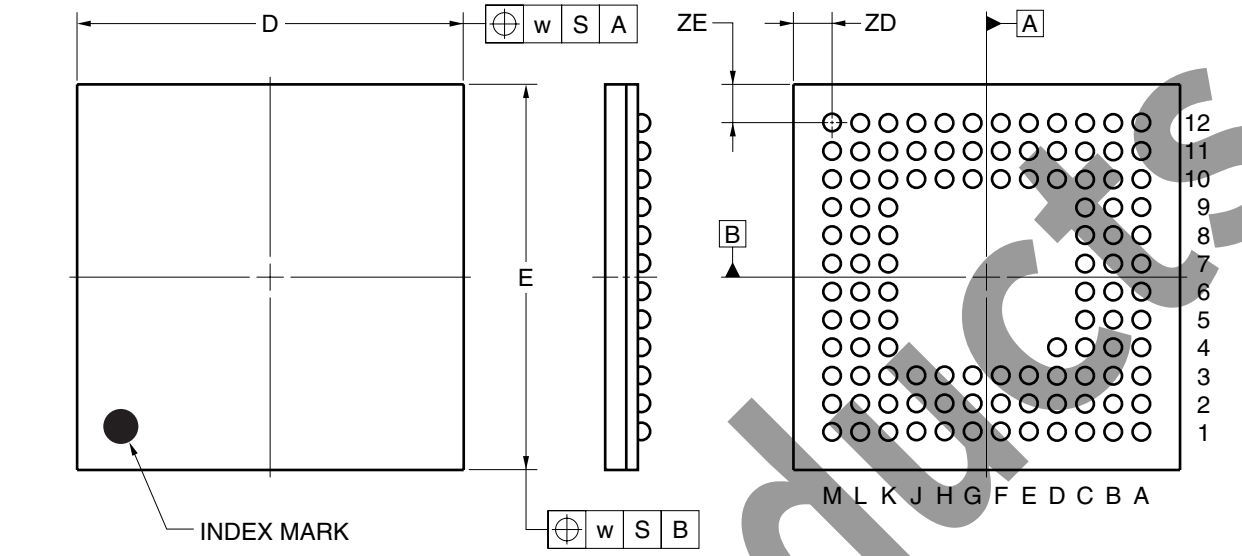
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

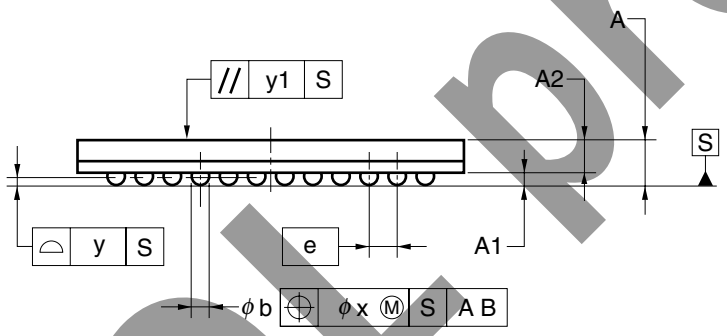
ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P100GC-50-9EU

★ • μPD720122F1-DN2, 720122F1-DN2-A

109-PIN PLASTIC FBGA (11x11)





(UNIT:mm)

ITEM	DIMENSIONS
D	11.00±0.10
E	11.00±0.10
w	0.20
A	1.28±0.10
A1	0.35±0.06
A2	0.93
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.10
ZE	1.10

P109F1-80-DN2

4. RECOMMENDED SOLDERING CONDITIONS

The μPD720122 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact your NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 4-1. Recommended Soldering Conditions of Surface-Mount Type (1/2)

• μPD720122GC-9EU: 100-pin plastic TQFP (Fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Symbol
★ Infrared ray reflow	Peak package's surface temperature: 235° C, Reflow time: 30 seconds or less (210 °C or higher), Maximum allowable number of reflow processes: 3, Exposure limit Note: 3 days (10 hours pre-backing is required at 125C° afterwards). <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-103-3
Partial heating method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per each side of the device).	–

Note The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

★ **• μPD720122GC-9EU-A: 100-pin plastic TQFP (Fine pitch) (14 × 14)**

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 260° C, Reflow time: 60 seconds or less (220 °C or higher), Maximum allowable number of reflow processes: 3, Exposure limit Note: 7 days (10 hours pre-backing is required at 125C° afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3
Partial heating method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per each side of the device).	–

Note The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

Table 4-1. Recommended Soldering Conditions of Surface-Mount Type (2/2)

• μPD720122F1-DN2: 109-pin plastic FBGA (11 × 11)

Soldering Method	Soldering Conditions	Symbol
★ Infrared ray reflow	Peak package's surface temperature: 235° C, Reflow time: 30 seconds or less (210 °C or higher), Maximum allowable number of reflow processes: 3, Exposure limit [Note]: 7 days (10 hours pre-backing is required at 125C° afterwards). <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-107-3

Note The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

★ **• μPD720122F1-DN2-A: 109-pin plastic FBGA (11 × 11)**

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 250° C, Reflow time: 60 seconds or less (220 °C or higher), Maximum allowable number of reflow processes: 2, Exposure limit [Note]: 3 days (10 hours pre-backing is required at 125C° afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR50-103-2

Note The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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