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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD720120

USB2.0 PHY (TRANSCEIVER WITH SIE)

The μPD720120 complies with the Universal Serial Bus Specification Revision 2.0 and works up to 480 Mbps. The μPD720120 integrates serial interface engine and USB2.0 transceiver into a single chip.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.
μPD720120 User's Manual: S15347E

FEATURES

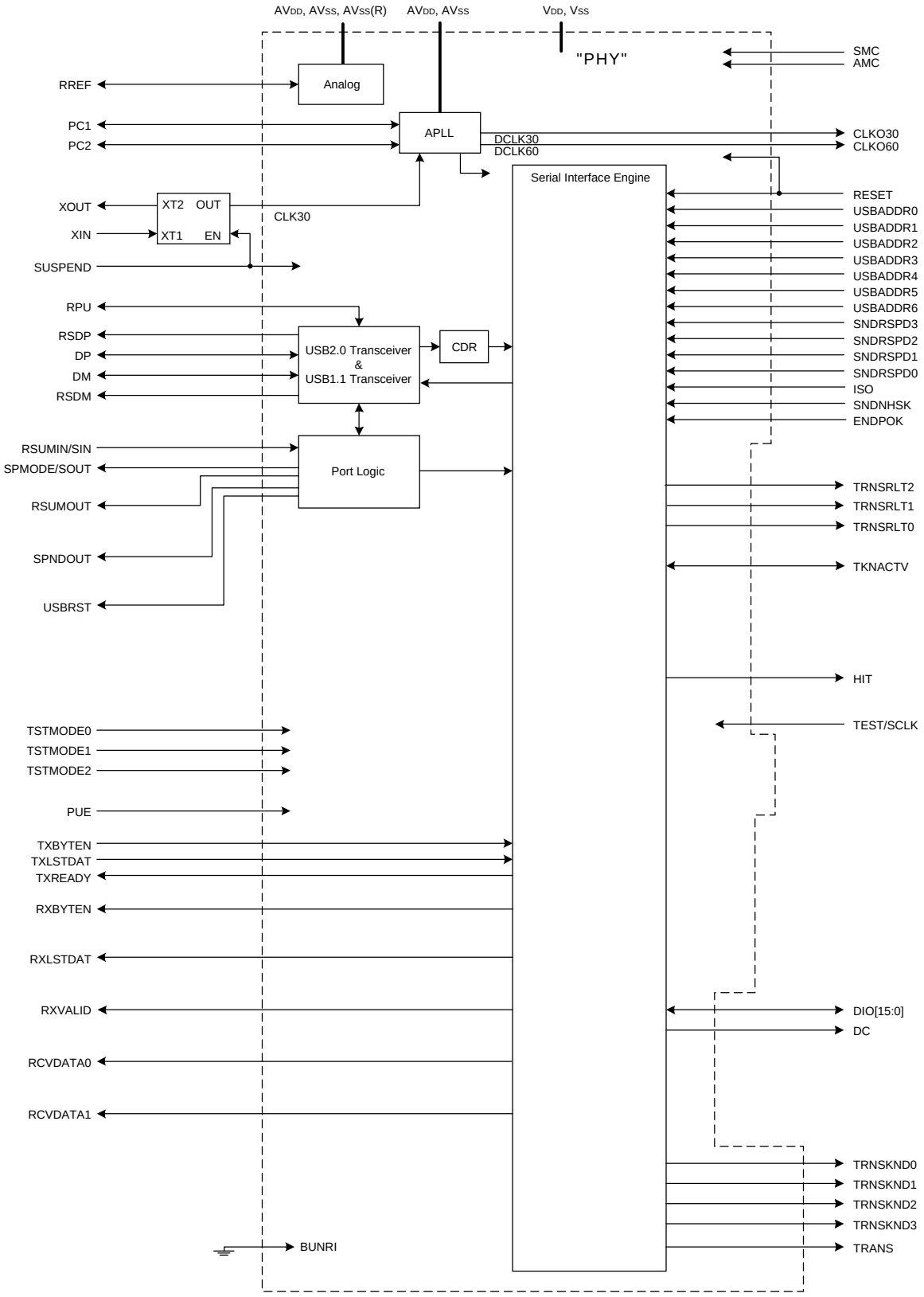
- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 12/480 Mbps)
- 16 bits backend Interface to SIE
- (Micro) SOF detection for High-/Full-speed operation
- One high-speed transceiver / receiver with full-speed transceiver / receiver
- High-speed or Full-speed packet protocol sequencer
- Start / End of packet detection
- NRZI encoding / decoding
- Stuffed bit insertion / recognition and stripping
- CRC checker and generation (5 bits CRC for Token packet and 16bits CRC for Data packet)
- Serial to 16 bits parallel conversion for data reception and 16 bits parallel to serial conversion for data transmission
- Automatic chirp assertion and full-/high-speed mode change
- USB Reset, Suspend and Resume signaling detection
- Supports remote wakeup functionality
- Supports set feature (TEST_MODE) functionality
- System Clock is generated by 30 MHz X'tal
- Several Clock Outputs (30 MHz, 60 MHz) are provided for backend interface.
- 3.3 V power supply

ORDERING INFORMATION

Part Number	Package
μPD720120GC-9EU	100-pin plastic TQFP (Fine pitch) (14 × 14)

Document No. S15386EJ1V0DS00 (1st edition)
Date Published March 2001 NS CP (K)
Printed in Japan

BLOCK DIAGRAM



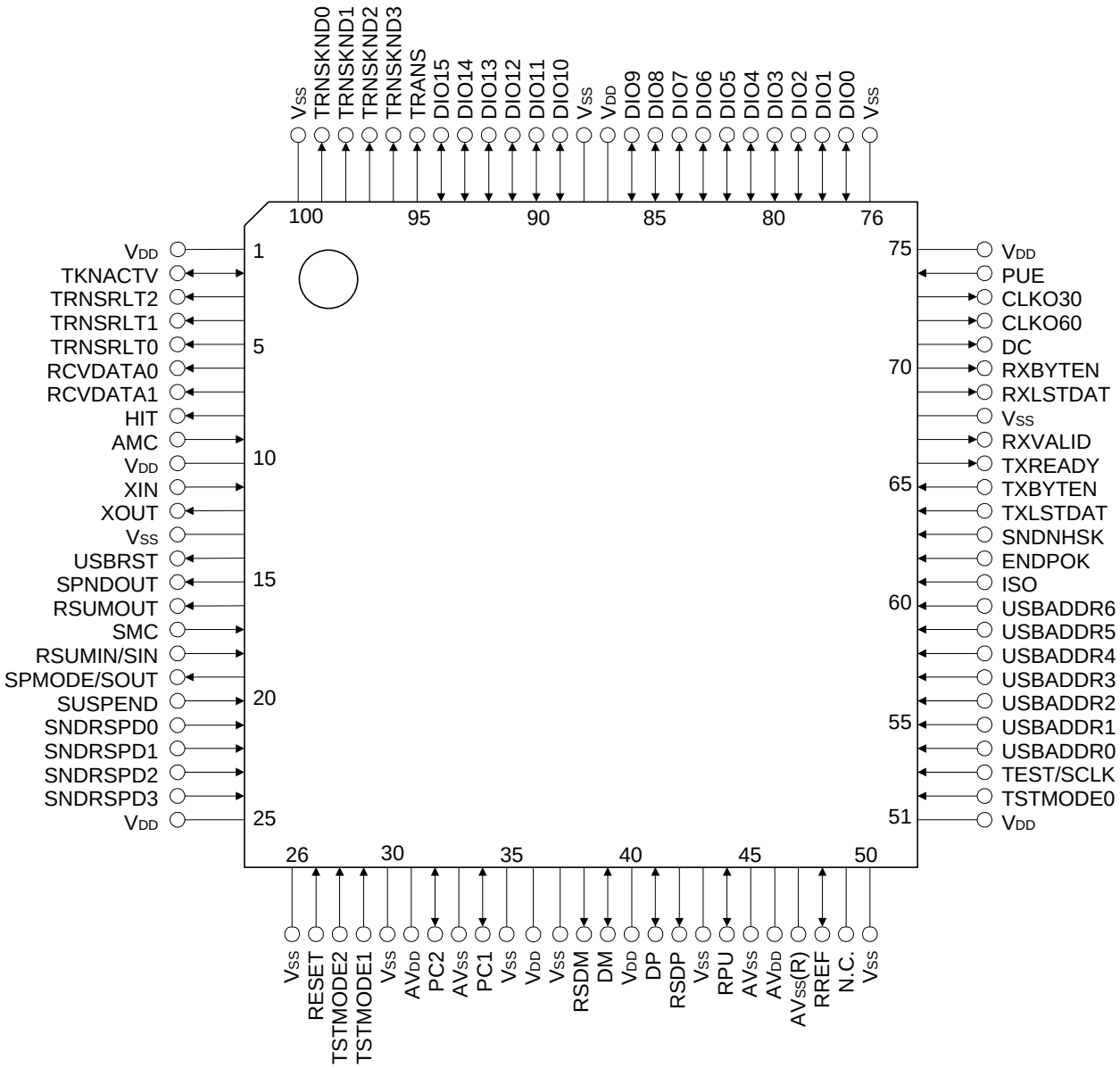
Remark Dot line shows “PHY” core.

Analog	:generates constant voltage and current sources for APLL, USB2.0 transceiver / receiver and etc.
APLL	:generates all clocks of PHY.
CDR	:Data & clock recovery circuit
USB 2.0 Transceiver	:contains all of the transceiver functionality required for high-speed operation. Default data speed is set at 480 Mbps.
USB 1.1 Transceiver	:contains all of the transceiver functionality required for high-speed operation and full-speed operation.
Serial Interface Engine	:controls USB2.0 and 1.1 protocol sequencing.
Port Logic	:Port logic contains USBReset/Suspend/Resume/chirp detection, Resume signal/chirp assertion and speed mode controller, etc.

PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic TQFP (Fine pitch) (14 × 14)**

μPD720120GC-9EU



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD}	26	V_{SS}	51	V_{DD}	76	V_{SS}
2	TKNACTV	27	RESET	52	TSTMODE0	77	DIO0
3	TRNSRLT2	28	TSTMODE2	53	TEST/SCLK	78	DIO1
4	TRNSRLT1	29	TSTMODE1	54	USBADDR0	79	DIO2
5	TRNSRLT0	30	V_{SS}	55	USBADDR1	80	DIO3
6	RCVDATA0	31	AV_{DD}	56	USBADDR2	81	DIO4
7	RCVDATA1	32	PC2	57	USBADDR3	82	DIO5
8	HIT	33	AV_{SS}	58	USBADDR4	83	DIO6
9	AMC	34	PC1	59	USBADDR5	84	DIO7
10	V_{DD}	35	V_{SS}	60	USBADDR6	85	DIO8
11	XIN	36	V_{DD}	61	ISO	86	DIO9
12	XOUT	37	V_{SS}	62	ENDPOK	87	V_{DD}
13	V_{SS}	38	RSDM	63	SNDNHSK	88	V_{SS}
14	USBRST	39	DM	64	TXLSTDAT	89	DIO10
15	SPNDOUT	40	V_{DD}	65	TXBYTEN	90	DIO11
16	RSUMOUT	41	DP	66	TXREADY	91	DIO12
17	SMC	42	RSDP	67	RXVALID	92	DIO13
18	RSUMIN/SIN	43	V_{SS}	68	V_{SS}	93	DIO14
19	SPMODE/ SOUT	44	RPU	69	RXLSTDAT	94	DIO15
20	SUSPEND	45	AV_{SS}	70	RXBYTEN	95	TRANS
21	SNDRSPD0	46	AV_{DD}	71	DC	96	TRNSKND3
22	SNDRSPD1	47	AV_{SS}(R)	72	CLKO60	97	TRNSKND2
23	SNDRSPD2	48	RREF	73	CLKO30	98	TRNSKND1
24	SNDRSPD3	49	N.C.	74	PUE	99	TRNSKND0
25	V_{DD}	50	V_{SS}	75	V_{DD}	100	V_{SS}

Remark AV_{SS} (R) should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.

1. PIN INFORMATION

(1/2)

Pin Name	I/O	Buffer Type	Active Level	Function
XIN	I			30 MHz oscillator-in for X'tal
XOUT	O			30 MHz oscillator-out for X'tal
RESET	I	5 V tolerant schmitt input	High	Asynchronous chip reset
CLKO30	O	3.3 V output (12 mA)		30 MHz clock output
CLKO60	O	3.3 V output (12 mA)		60 MHz clock output
USBADDR[6:0]	I	5 V tolerant input		USB address input
RPU	A	Analog		External 1.5 kΩ pull-up resistor terminal
DP	B	USB high-speed D+		High-speed data D+
DM	B	USB high-speed D-		High-speed data D-
RSDP	O	USB full-speed D+		Full-speed data D+ and R_S resistor terminal
RSDM	O	USB full-speed D-		Full-speed data D- and R_S resistor terminal
PUE	I	5 V tolerant input		External 1.5 kΩ pull-up resistor control
RREF	A	Analog		Reference resistor
PC1	A	Analog		Capacitor for PLL
PC2	A	Analog		Capacitor for PLL
DIO[15:0]	B	5 V tolerant I/O (6 mA)		16 bits transmitted / received data bus
TXBYTEN	I	5 V tolerant input	High	Transmit data byte/word alignment enable
TXLSTDAT	I	5 V tolerant input	High	Last transmit data indication
TXREADY	O	5 V tolerant output (6 mA)	High	Ready to read from transmit data bus
RXBYTEN	O	5 V tolerant output (6 mA)	High	Receive data byte/word alignment enable
RXLSTDAT	O	5 V tolerant output (6 mA)	High	Last receive data indication
RXVALID	O	5 V tolerant output (6 mA)	High	Receive data valid
DC	O	5 V tolerant output (6 mA)		Data I/O indication
TRANS	O	5 V tolerant output (6 mA)	High	Transaction progression
TKNACTV	B	5 V tolerant I/O (6 mA)		Token PID receive indication or USB resume detection input control
TRNSKND[3:0]	O	5 V tolerant output (6 mA)		Receive token PID type
RCVDATA[1:0]	O	5 V tolerant output (6 mA)		Receive data PID type
TRNSRLT[2:0]	O	5 V tolerant output (6 mA)		Transaction result code
HIT	O	5 V tolerant output (6 mA)	High	Device targeted indication
ENDPOK	I	5 V tolerant input	High	Endpoint supported indication
ISO	I	5 V tolerant input	High	Isochronous supported indication
SNDRSPD[3:0]	I	5 V tolerant input		Transmit data or handshake PID type
SNDNHSK	I	5 V tolerant input	High	No handshake control
USBRST	O	5 V tolerant output (6 mA)	High	USB Reset detection
SPMODE/SOUT	O	5 V tolerant output (6 mA)		Full-/High-speed mode indication or SCAN output

(2/2)

Pin Name	I/O	Buffer Type	Active Level	Function
SPNDOUT	O	5 V tolerant output (6 mA)	High	USB Suspend detection
RSUMOUT	O	5 V tolerant output (6 mA)	High	USB Resume detection
SUSPEND	I	5 V tolerant input	High	Suspend request. This also disables PLL, OSC, Current source
RSUMIN/SIN	I	5 V tolerant input	High	Remote wakeup enable or SCAN input
AMC	I	5 V tolerant input with 50 kΩ pull-down R	High	SCAN mode control
SMC	I	5 V tolerant input with 50 kΩ pull-down R	High	SCAN mode control
TEST/SCLK	I	5 V tolerant input with 50 kΩ pull-down R	High	Test mode control SCAN clock-input
TSTMODE[2:0]	I	5 V tolerant input		Set Feature (TEST_MODE) control or test control
V_{DD}				V_{DD}
AV_{DD}				V_{DD} for analog circuit
V_{SS}				V_{SS}
AV_{SS}				V_{SS} for analog circuit
AV_{SS}(R)				V_{SS} for analog circuit (Feedback resistor connection)
N.C.				Not connected

Remark I: Input, O: Output, B: Bi-direction, A: Analog

2. ELECTRICAL SPECIFICATIONS

2.1 Buffer List

- 5 V schmitt buffer
  RESET
- 3.3 V Oscillator block
  XIN, XOUT
- 3.3 V I_{OL} = 12 mA output buffer
  CLKO30, CLKO60
- 5 V input buffer
  USBADDR[6:0], PUE, TXBYTEN, TXLSTDAT, ENDPOK, ISO, SNDRSPD[3:0], SNDNHSK, SUSPEND, RSUMIN/SIN, TSTMODE[2:0]
- 5 V I_{OL} = 6 mA output buffer
  TXREADY, RXBYTEN, RXLSTDAT, RXVALID, DC, TRANS, TRNSKND[3:0], RCVDATA[1:0], TRNSRLT[2:0], HIT, USBRST, SPMODE/SOUT, SPNDOUT, RSUMOUT
- 5 V I_{OL} = 6 mA I/O buffer
  DIO[15:0], TKNACTV
- 5 V input buffer with 50 kΩ pull-down resistor
  TEST/SCLK, SMC, AMC
- USB2.0 interface
  RPU, DP, DM, RSDP, RSDM, RREF, PC1, PC2

Above, “5 V” refers to a 3-V buffer that is 5-V tolerant (has 5-V maximum voltage). Therefore, it is possible to have a 5-V connection for an external bus, but the output level will be only up to 3 V, which is the V_{DD} voltage.

2.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when a current flow out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “MIN.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “MAX.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

2.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I			
3.3 V input voltage		$V_I < V_{DD} + 0.5$ V	–0.5 to +4.6	V
5.0 V input voltage		$V_I < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Output voltage	V_O			
3.3 V output voltage		$V_O < V_{DD} + 0.5$ V	–0.5 to +4.6	V
5.0 V output voltage		$V_O < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Operating temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}		3.0	3.3	3.6	V
High-level input voltage	V_{IH}					
3.3 V High-level input voltage			2.0		V_{DD}	V
5.0 V High-level input voltage			2.0		5.5	V
Low-level input voltage	V_{IL}					
3.3 V Low-level input voltage			0		0.8	V
5.0 V Low-level input voltage			0		0.8	V
Hysteresis voltage	V_H		0.3		1.5	V

DC Characteristics

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Off-state output leakage current	I_{OZ}	$V_O = V_{DD}$ or GND		±10	μA
Output short circuit current	I_{OS} Note			−250	mA
Low-level output current	I_{OL}				
3.3 V Low-level output current		V_{OL} = 0.4 V	12		mA
5.0 V Low-level output current		V_{OL} = 0.4 V	6		mA
High-level output current	I_{OH}				
3.3 V High-level output current		V_{OH} = 2.4 V	−12		mA
5.0 V High-level output current		V_{OH} = 2.4 V	−2		mA

Note The output short circuit time is one second or less and is only for one pin on the LSI.

USB Interface Block

Parameter	Symbol	Conditions	MIN	MAX	Unit
Serial Resistor between DP (DM) and RSDP (RSDM).	R_S		35.64	36.36	Ω
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R_{PU}		1.425	1.575	kΩ
Termination voltage for upstream facing port pullup (full-speed)	V_{TERM}		3.0	3.6	V
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$\lvert(D+) - (D-)\rvert$	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		–50	+500	mV
High-speed differential input signaling level	See Figure 2-4.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		–10.0	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		–10.0	+10	mV
Chirp J level (different signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (different signal)	V_{CHIRPK}		–900	–500	mV

Figure 2-1. Differential Input Sensitivity Range for Low-/full-speed

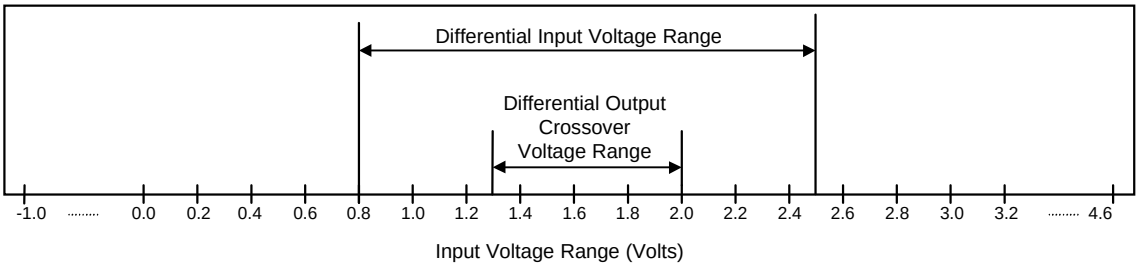


Figure 2-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

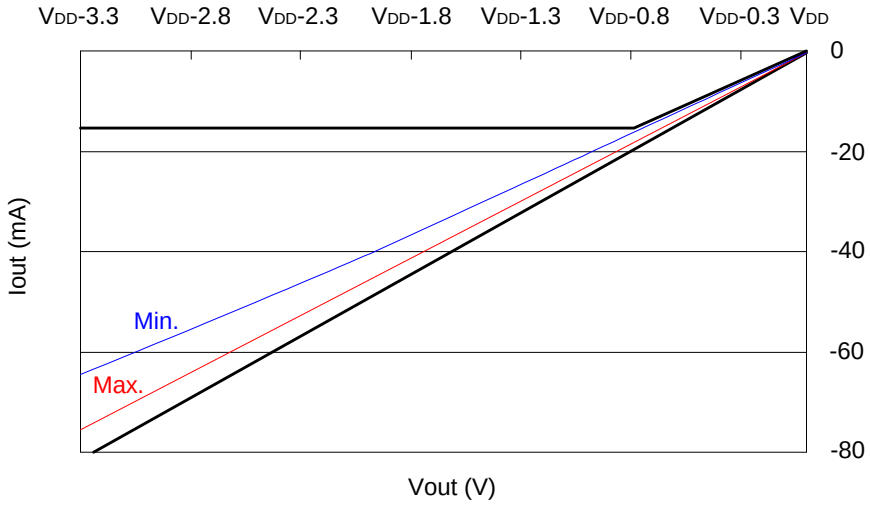


Figure 2-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

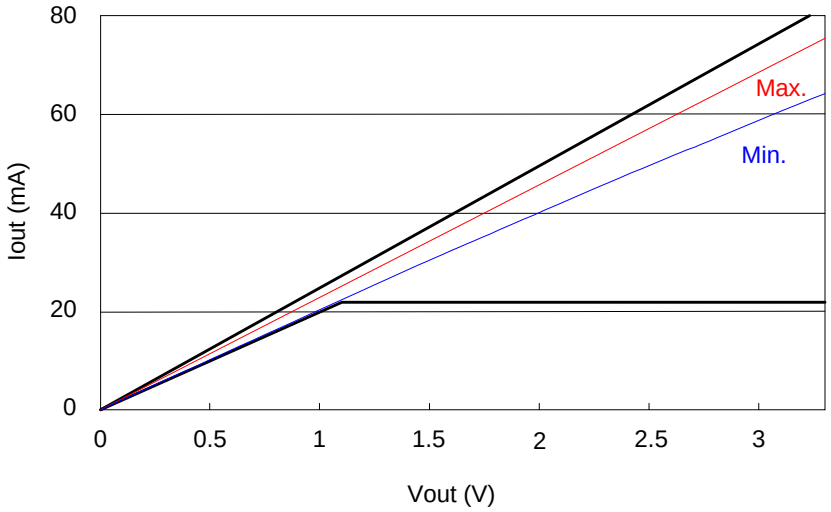


Figure 2-4. Receiver Sensitivity for Transceiver at DP/DM

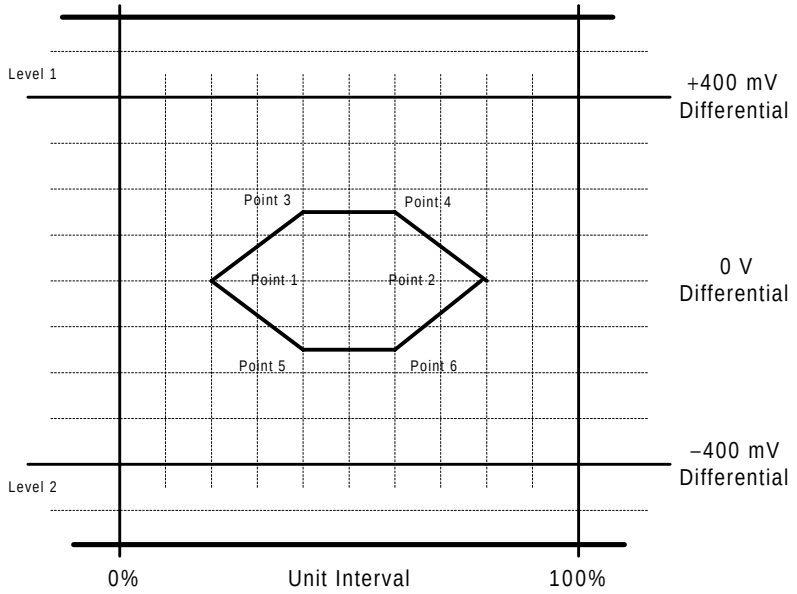
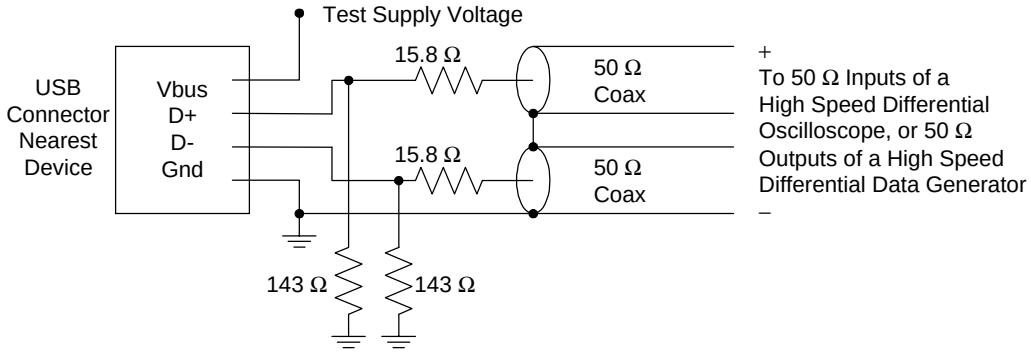


Figure 2-5. Receiver Measurement Fixtures



Pin Capacitance

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}		3		5	pF
Output/Bi-directional capacitance	C_{OUT}		9		11	pF

Remark These are just estimated value.

Power Consumption

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power consumption		Normal mode			300	mA
		Suspend mode			200	μA

Remarks 1. These are just estimated value.

2. Input pins except for TEST, SMC, and AMC must be supplied low or high-level signal. On the other hand, TEST, SMC, and AMC must be opened on board.

System Clock Specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{CLK}		–500 ppm	30	+500 ppm	MHz
Duty cycle	t_{DUTY}		40		60	%

Remarks Recommended accuracy of clock frequency is ± 100 ppm.

AC Characteristics (V_{DD} = 3.0 to 3.6 V, T_A = 0 to +70°C)

Clock

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLKO30 cycle time	t_{C3C}			33.33		ns
CLKO60 cycle time	t_{C6C}			16.67		ns
CLKO30 high level width	t_{C3H}		15.9		17.5	ns
CLKO30 low level width	t_{C3L}		15.9		17.5	ns
CLKO60 high level width	t_{C6H}		7.95		8.75	ns
CLKO60 low level width	t_{C6L}		7.95		8.75	ns
CLKO60 phase time (CLKO30)	t_{P60}		–1.0		+1.0	ns
CLK30/CLKO60 jitter	t_{jitter}		–0.5		+0.5	ns
Reset time	t_{reset}		2			μs
CLKO30 restart time from reset	$t_{restart}$		150			μs

USB Interface Block

(1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Full-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% - 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (Including frequency tolerance): To next transition For paired transitions	 t_{DJ1} t_{DJ2}		 –3.5 –4.0	 +3.5 +4.0	 ns ns
Source jitter for differential transition to SE0 transition	t_{FDEOP}		–2	+5	ns
Receiver jitter: To next transition For paired transitions	 t_{JR1} t_{JR2}		 –18.5 –9	 +18.5 +9	 ns ns
Source SE0 interval of EOP	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

(2/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
High-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{HSR}		500		ps
Fall time (90% - 10%)	t_{HSF}		500		ps
Driver waveform	See Figure 2-6.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See Figure 2-6.				
Receiver jitter tolerance	See Figure 2-4.				
Device Event Timings					
Time from internal power good to device pulling D+ beyond V_{IHZ}	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach	t_{ATTDB}			100	ms
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response for full-speed	$t_{RSPIPD1}$			6.5	Bit times
High-speed detection start time from suspend	t_{SCA}		2.5		μs
Sample time for suspend vs reset	t_{CSR}		100	875	μs
Power down under suspend	t_{SUS}			10	ms
Suspend/reset detection time	t_{SPD}		3.0	3.125	ms
SUSPEND set time (SPNDOUT)	t_{SSP}		0	-	
SUSPEND clear time (RSUMOUT)	t_{CSP}		0	-	
Reversion time from suspend to high-speed	t_{RHS}			1.333	μs
SUSPEND setup time (RSUMIN)	t_{SRW}		0	-	
RSUMIN active pulse width	t_{RWP}		1	15	ms
Drive Chirp K width	t_{CKO}		1		ms
Finish Chirp K Assertion	t_{FCA}			7	ms
Start sequencing Chirp K-J-K-J-K-J	t_{SSC}			100	μs
Finish sequencing Chirp K-J	t_{FSC}		–500	–100	μs
Detect sequencing Chirp K-J width	t_{CSI}		2.5		μs
Sample time for sequencing Chirp	t_{SCS}		1.0	2.5	ms
Reversion time to high-speed	t_{RHA}			500	μs
High-speed detection start time	t_{HDS}		2.5	3000	μs
Reset completed time	t_{DRS}		10		ms

AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RXVALID out time	t_{RVO}	C_L = 15 pF			10.0	ns
RXVALID hold time	t_{RVH}	C_L = 15 pF			10.0	ns
RX_DOUT[15:0] out time	t_{RDO}	C_L = 15 pF			10.0	ns
RX_DOUT[15:0] hold time	t_{RDH}	C_L = 15 pF			10.0	ns
RXBYTEN out time	t_{RBO}	C_L = 15 pF			10.0	ns
RXBYTEN hold time	t_{RBH}	C_L = 15 pF			10.0	ns
RXLSTDAT out time	t_{RLO}	C_L = 15 pF			10.0	ns
RXLSTDAT hold time	t_{RLH}	C_L = 15 pF			10.0	ns
ENDPOK setup time	t_{EPS}		14.0			ns
ENDPOK hold time	t_{EPH}		0			ns
ISO setup time	t_{ISS}		10.0			ns
ISO hold time	t_{ISH}		0			ns
HIT out time for OUT/SETUP	t_{HOO}	C_L = 15 pF			10.0	ns
HIT out time for IN/PING	t_{HIO}	C_L = 15 pF			76.7	ns
HIT hold time	t_{HTH}	C_L = 15 pF			10.0	ns
RCVDATA[1:0] out time	t_{RPO}	C_L = 15 pF			10.0	ns
SNDRSPD[3:0] setup time for OUT/SETUP	t_{SHS}		11.5			ns
SNDRSPD[3:0] setup time for IN/PING	t_{SPS}		11.5			ns
SNDNHSK setup time	t_{SNS}		8.00			ns
SNDNHSK hold time	t_{SNH}		0			ns
TRANS out time	t_{TKO}	C_L = 15 pF			10.0	ns
TRANS hold time	t_{TKH}	C_L = 15 pF			10.0	ns
TRNSRLT[2:0] out time	t_{TTO}	C_L = 15 pF			10.0	ns
TRNSKND[3:0] out time	t_{TDO}	C_L = 15 pF			10.0	ns
TX_DIN[15:0] setup time	t_{TDS}		9.00			ns
TX_DIN[15:0] hold time	t_{TDH}		0			ns
TXBYTEN setup time	t_{TBS}		8.50			ns
TXBYTEN hold time	t_{TBH}		0			ns
TXLSTDAT setup time	t_{TLS}		9.50			ns
TXLSTDAT hold time	t_{TLH}		0			ns
TXLSTDAT setup time for NULL	t_{TNS}		26.2			ns
DC out time	t_{DCO}	C_L = 15 pF			10.00	ns
DC hold time	t_{DCH}	C_L = 15 pF			10.00	ns

Figure 2-6. Transmit Waveform for Transceiver at DP/DM

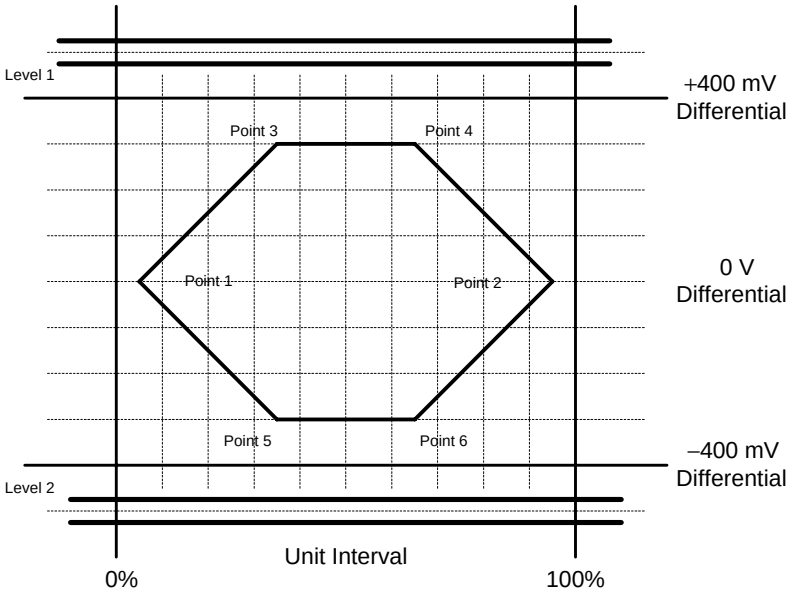
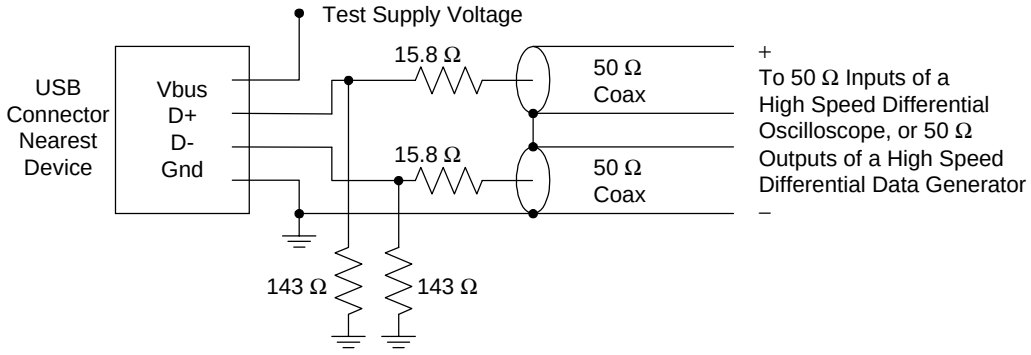
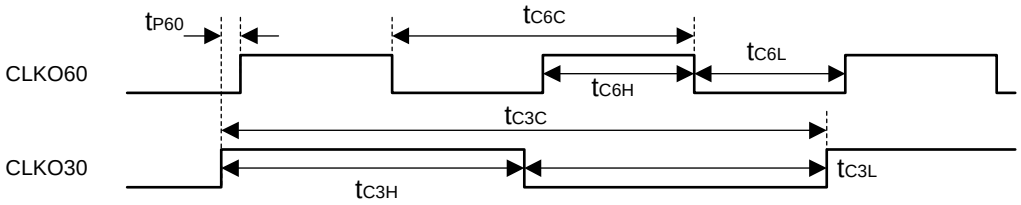


Figure 2-7. Transmitter Measurement Fixtures

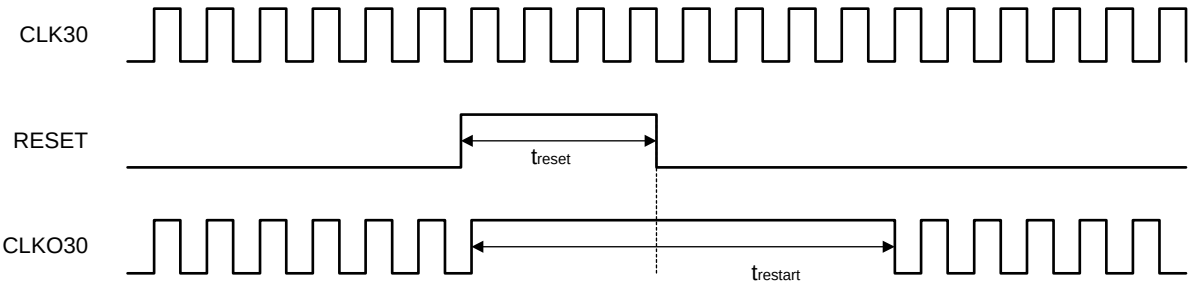


Timing Diagram

Clock Output

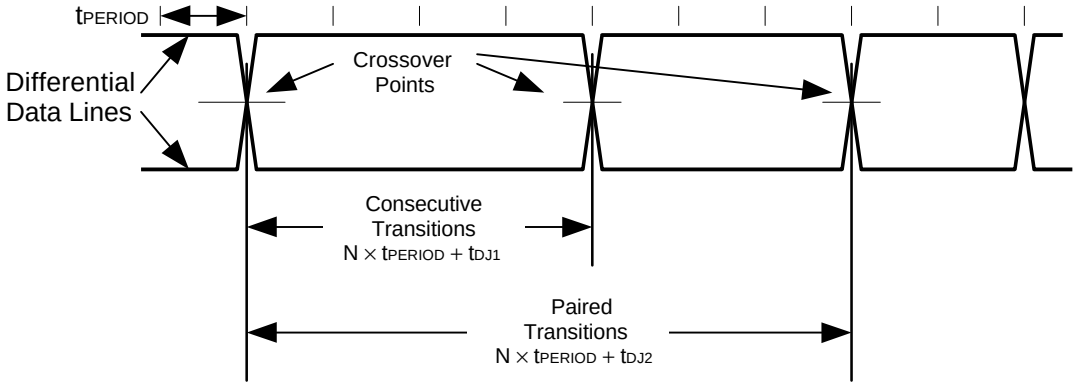


Reset vs Clock Output

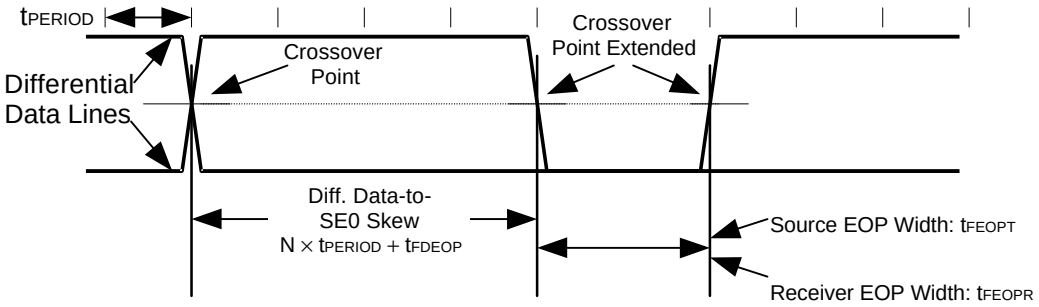


USB Signals

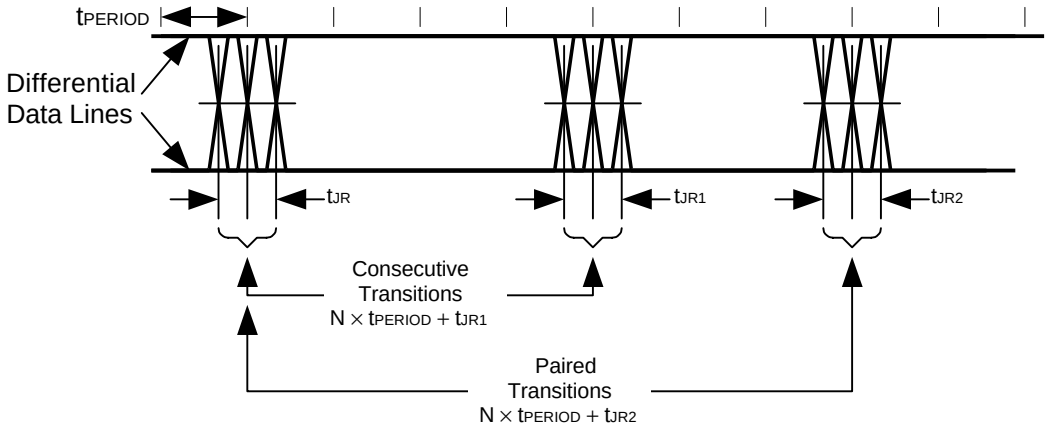
USB Differential Data Jitter for Full-speed



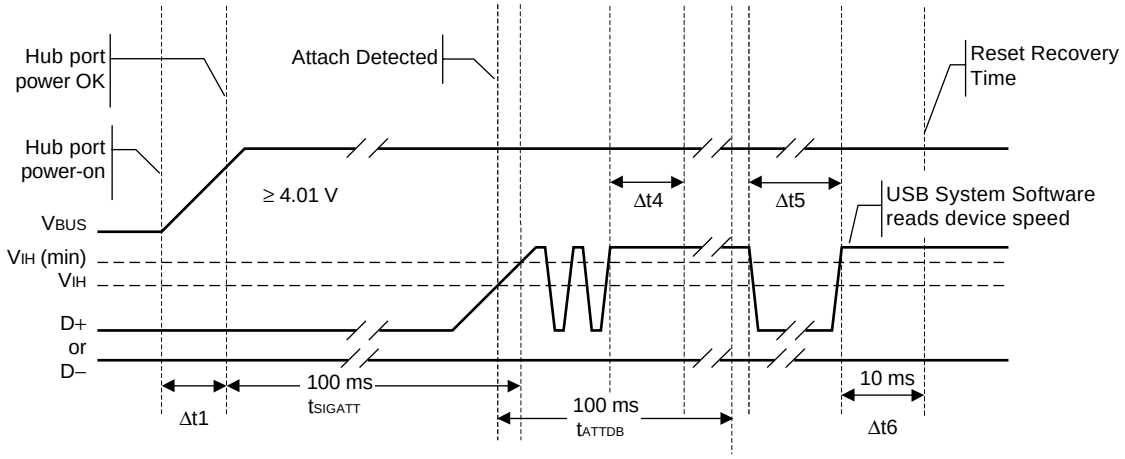
USB Differential-to-EOP Transition Skew and EOP Width for Full-speed



USB Receiver Jitter Tolerance for Full-speed

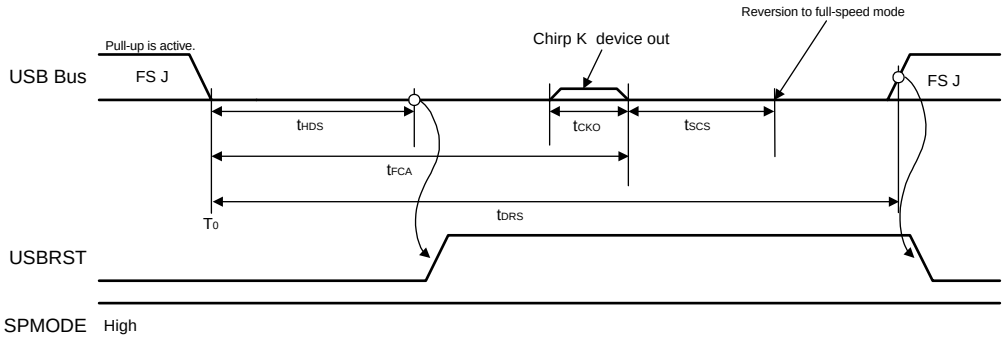


Power-on and Connection Events



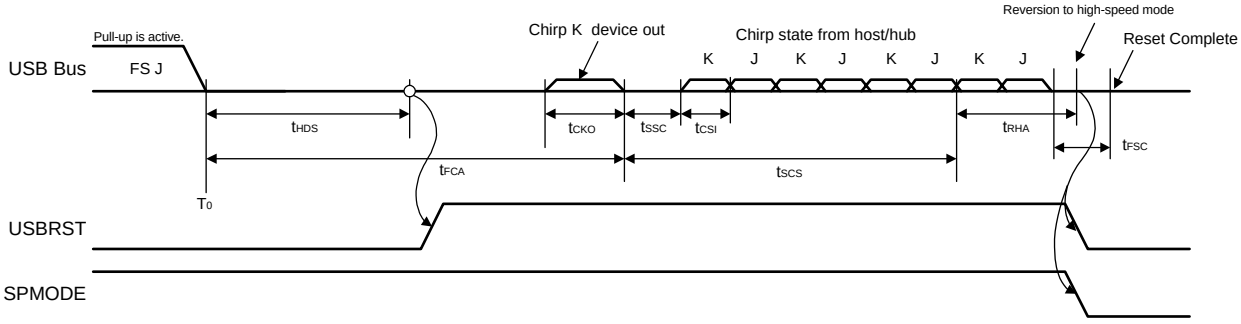
High-speed Connect Detection

USB Connection Sequencing on USB1.1 Bus



Remark Device is connected to hub port, which is operating in full-speed mode.
Hub includes root hub in host controller. This sequencing is the same as reset from USB 1.x host or hub.

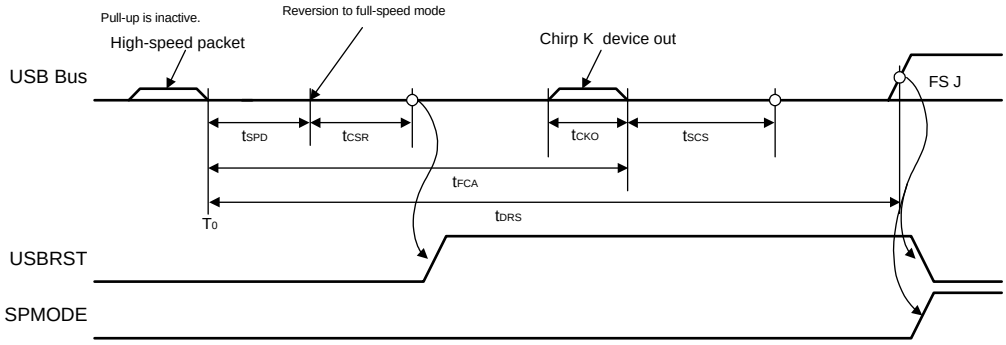
USB Connection Sequencing on USB2.0 Bus



Remark Device is connected to hub port, which is operating in high-speed mode.
Hub includes root hub in host controller. This sequencing is the same as reset for high-speed capable device which is operating in full-speed mode.

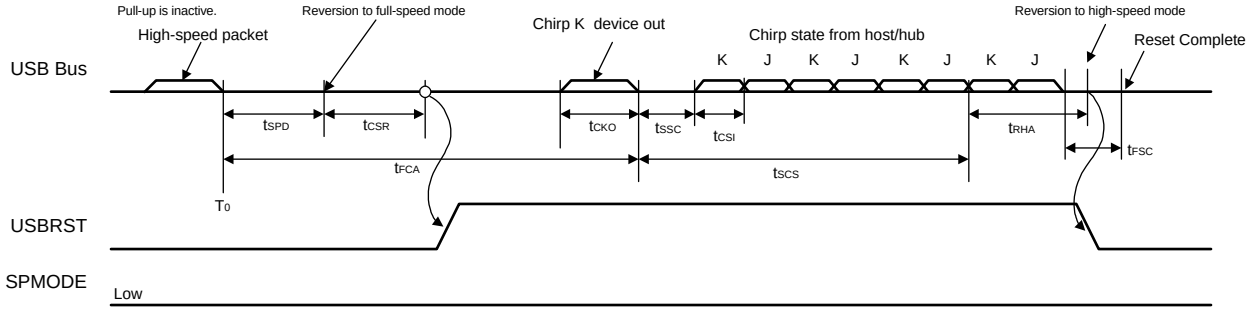
USB Reset

USB Reset on USB2.0 Bus (1)



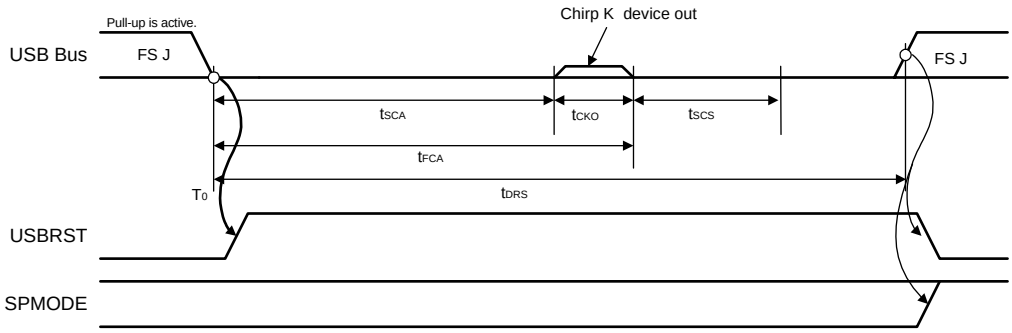
Remark Device is connected to hub port, which is operating in high-speed mode.
Hub includes root hub in host controller. Hub can not find chirp from device.

USB Reset on USB2.0 Bus (2)



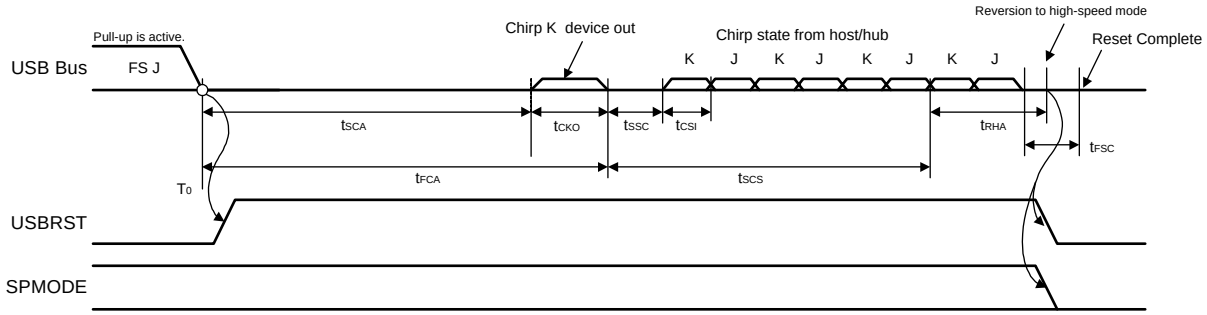
Remark Device is connected to hub port, which is operating in high-speed mode.
Hub includes root hub in host controller.

USB Reset from Suspended State (1)



Remark Device is connected to hub port, which is in suspended state.
Hub includes root hub in host controller. Hub can not find chirp from device.

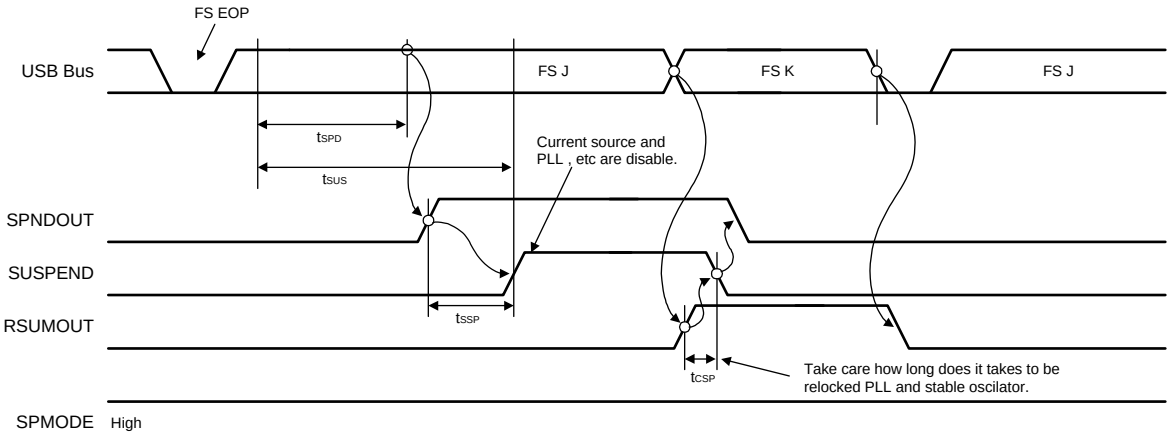
USB Reset from Suspended State (2)



Remark Device is connected to hub port, which is in suspended state.
Hub includes root hub in host controller.

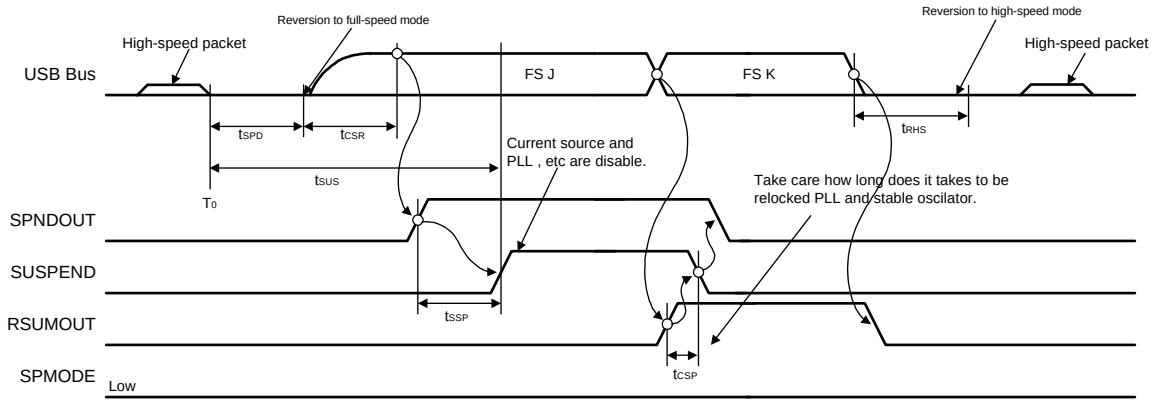
USB Suspend/resume

USB Suspend / resume on USB1.1 Bus



Remark Device is connected to hub port, which is operating in full-speed mode.
Hub includes root hub in host controller.

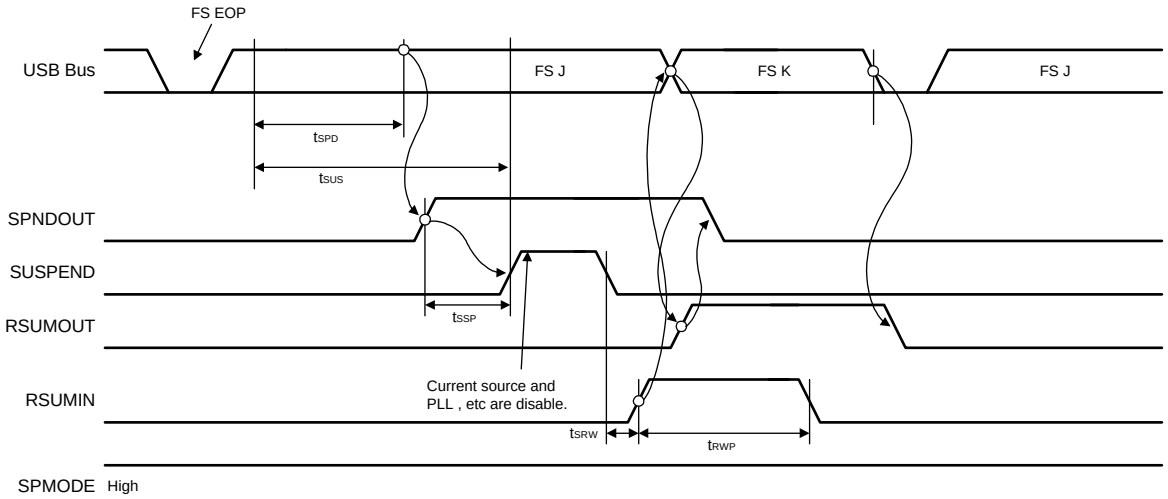
USB Suspend / resume on USB2.0 Bus



Remark Device is connected to hub port, which is operating in high-speed mode.
Hub includes root hub in host controller.

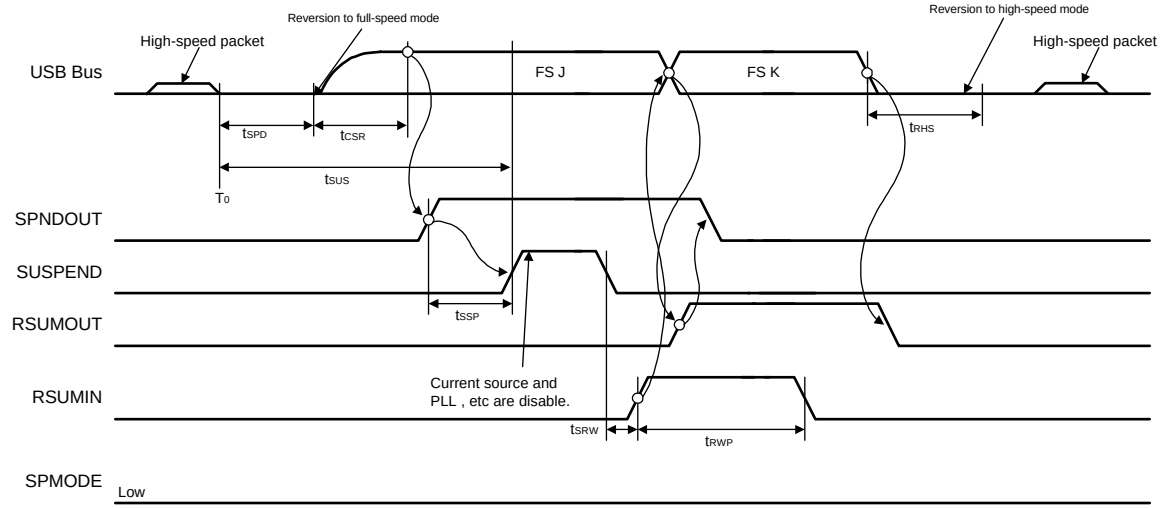
USB Remote Wakeup

USB Remote Wakeup on USB1.1 Bus



Remark Device is connected to hub port, which is operating in full-speed mode.
Hub includes root hub in host controller.

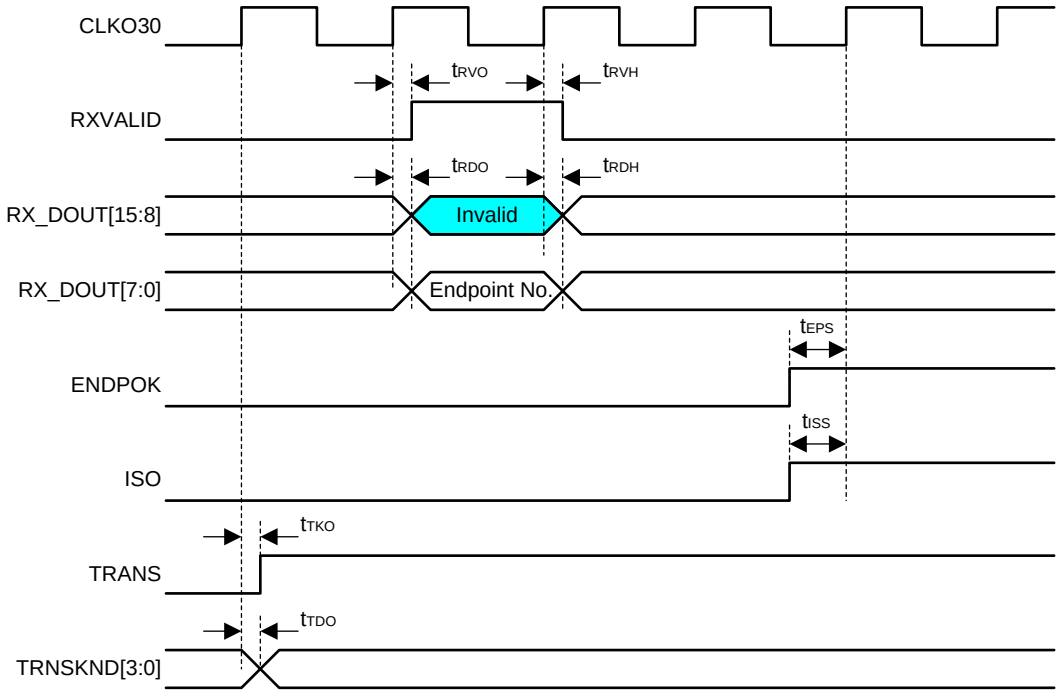
USB Remote Wakeup on USB2.0 Bus



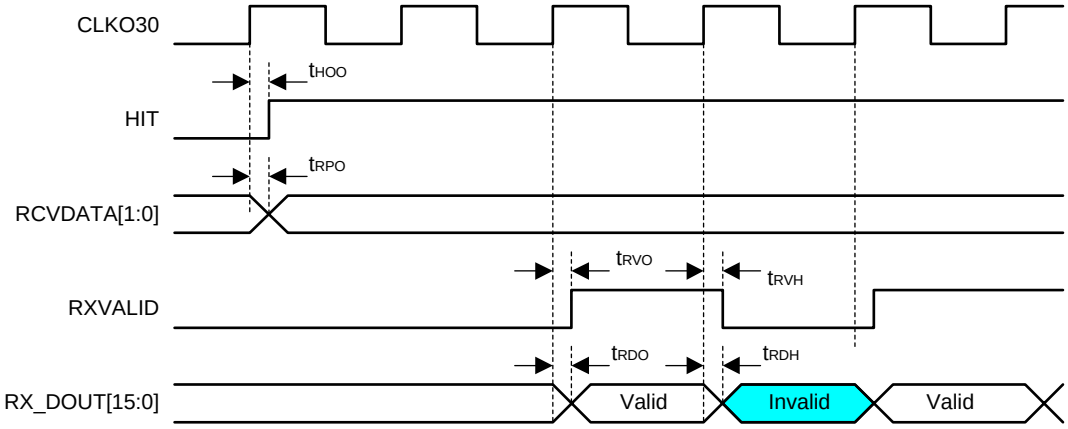
Remark Device is connected to hub port, which is operating in high-speed mode.
Hub includes root hub in host controller.

USB OUT/SETUP Transaction

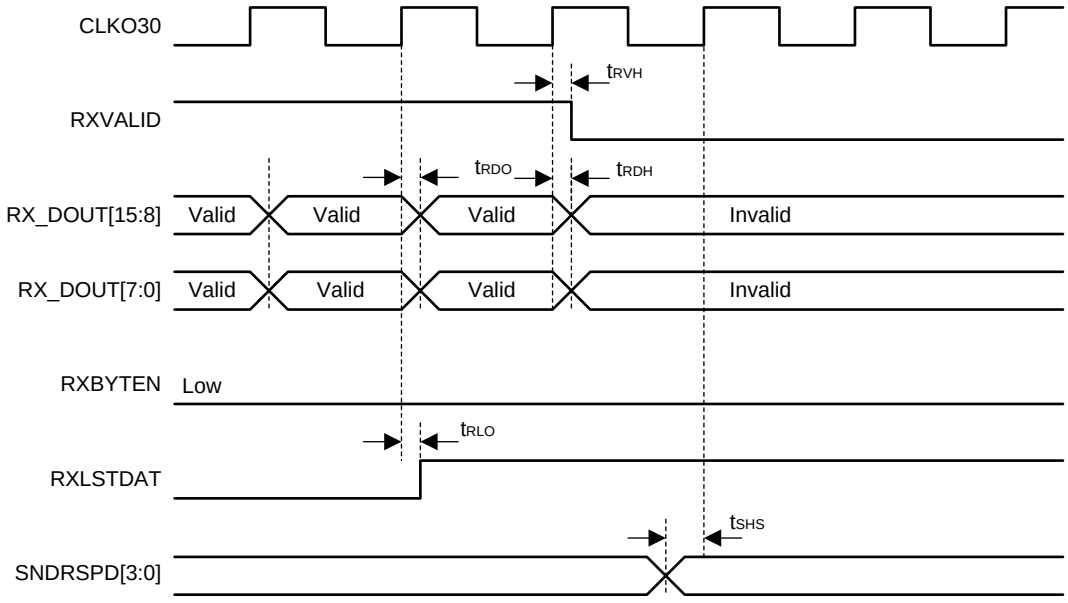
USB OUT/SETUP Token Phase



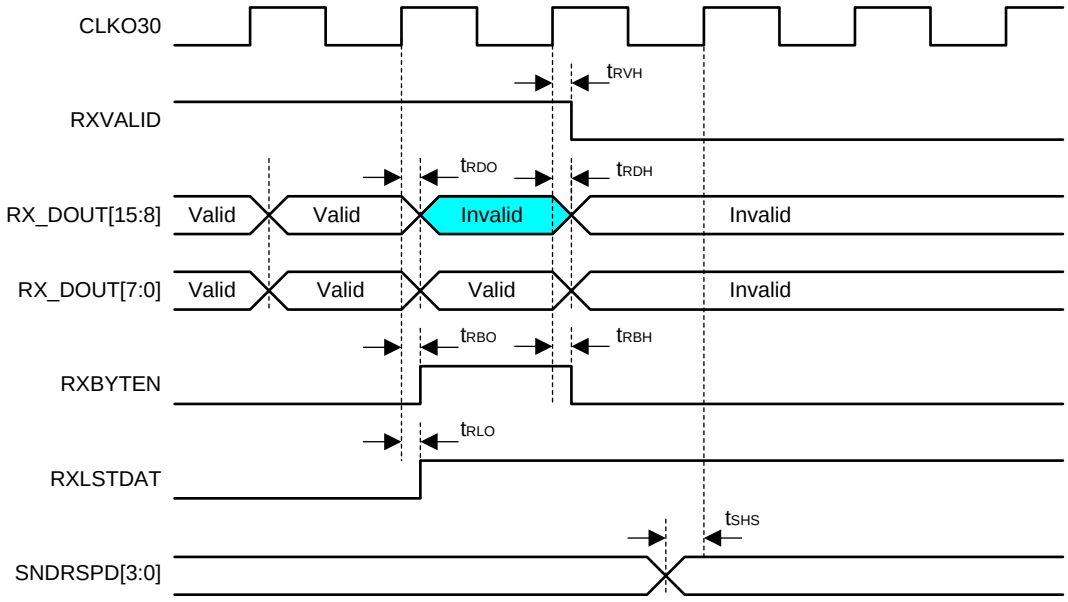
USB OUT/SETUP Start of Data Phase



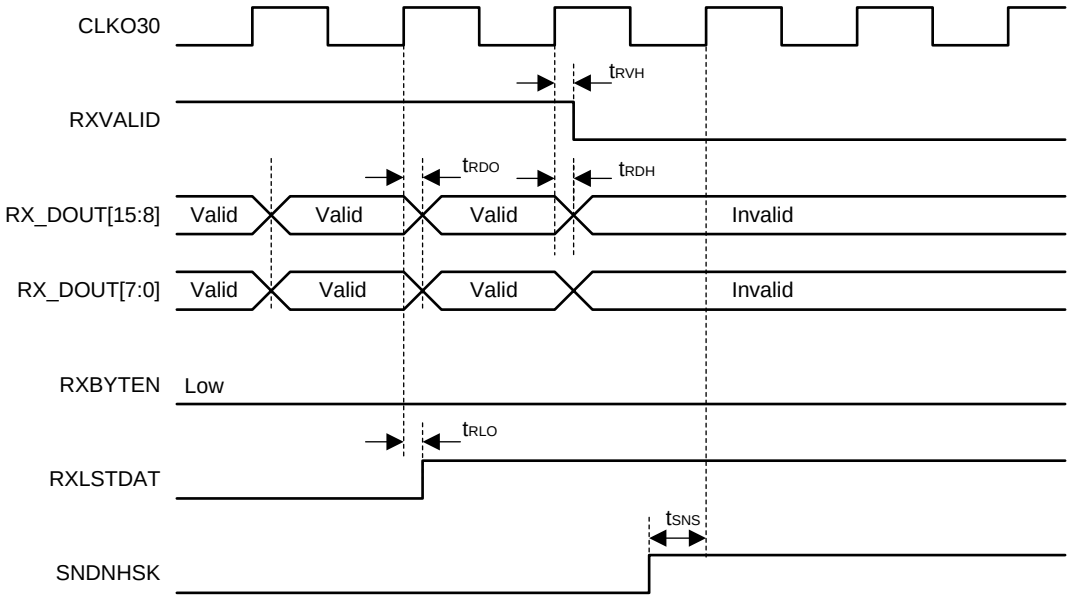
USB OUT/SETUP End of Data Phase (Word Boundary)



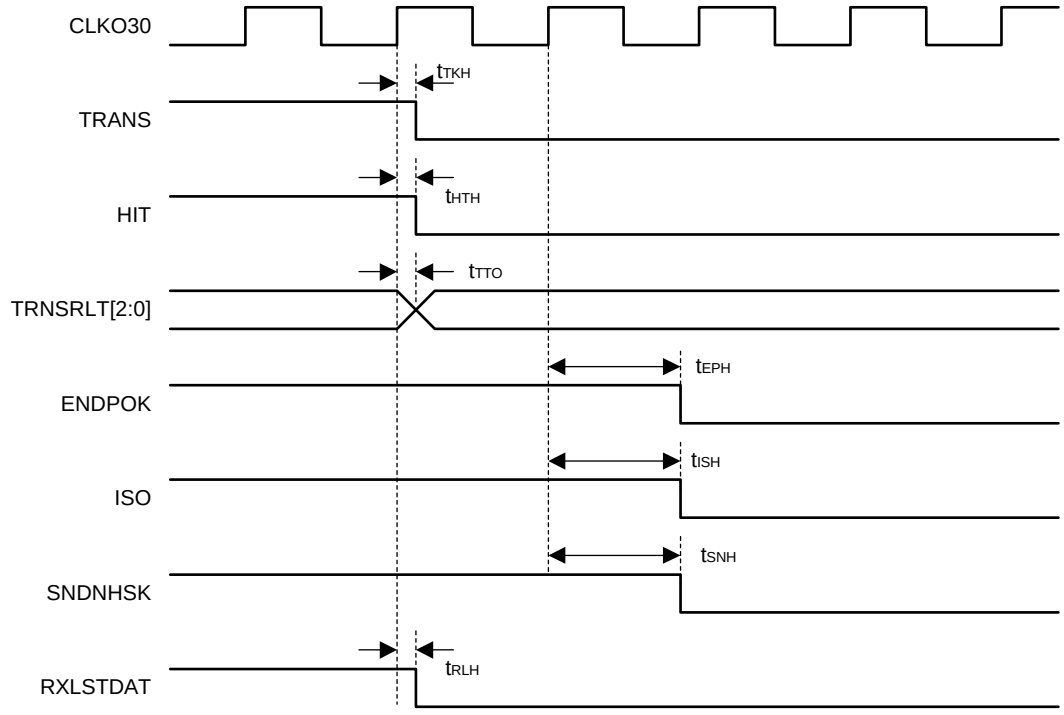
USB OUT/SETUP End of Data Phase (Byte Boundary)



USB OUT/SETUP No Respond for Host Issued Packet

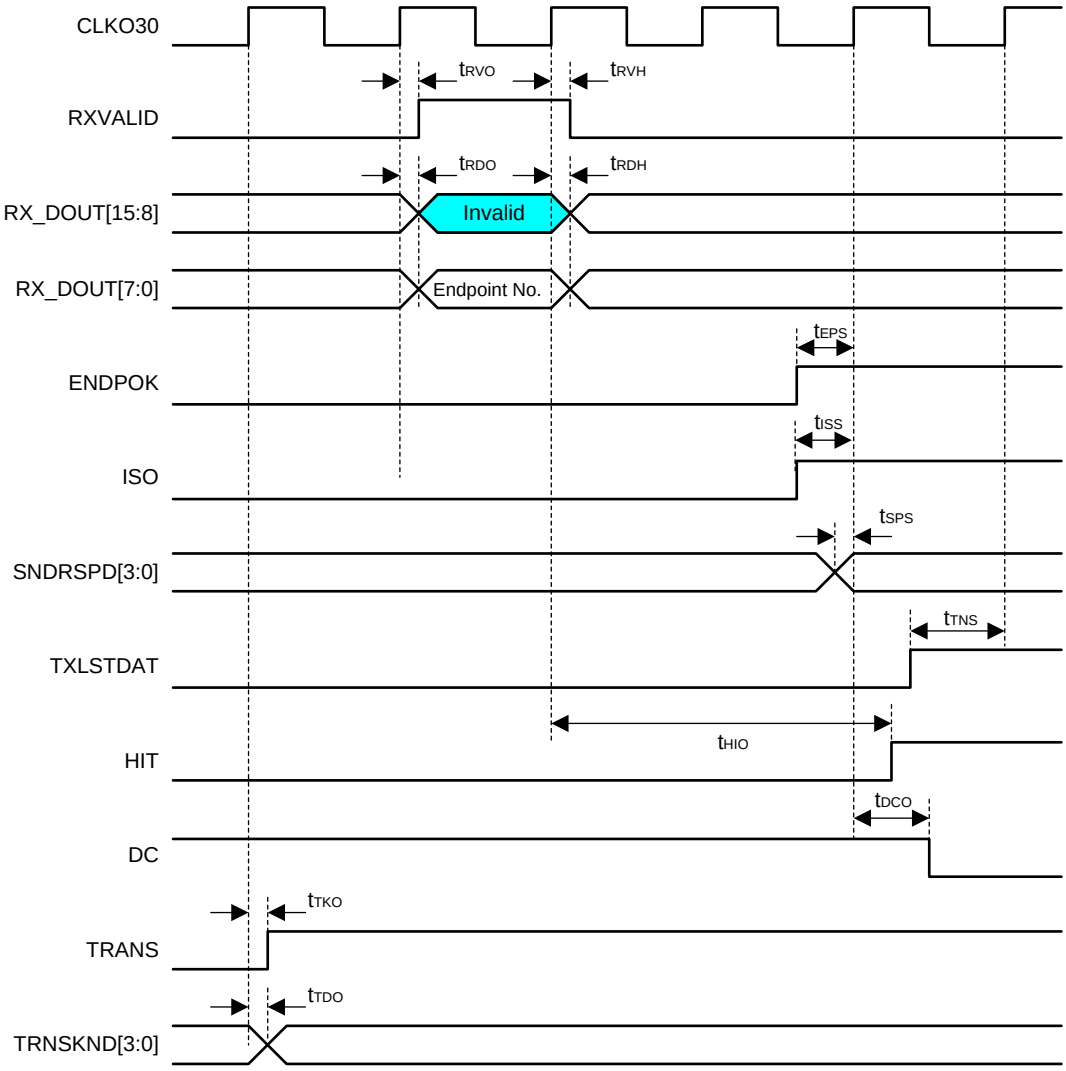


USB OUT/SETUP End of Handshake Phase

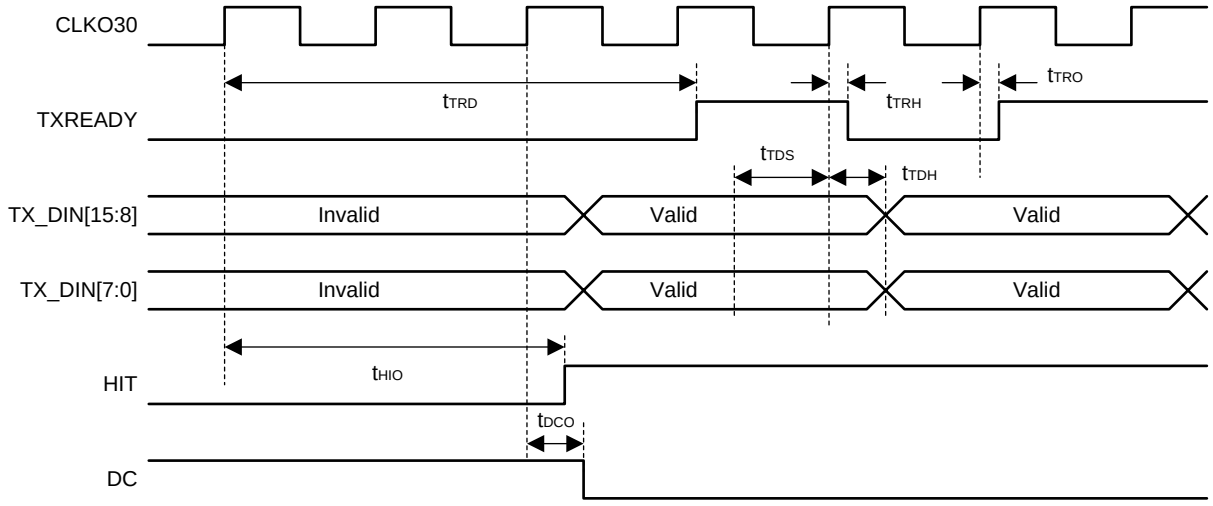


USB IN/PING Transaction

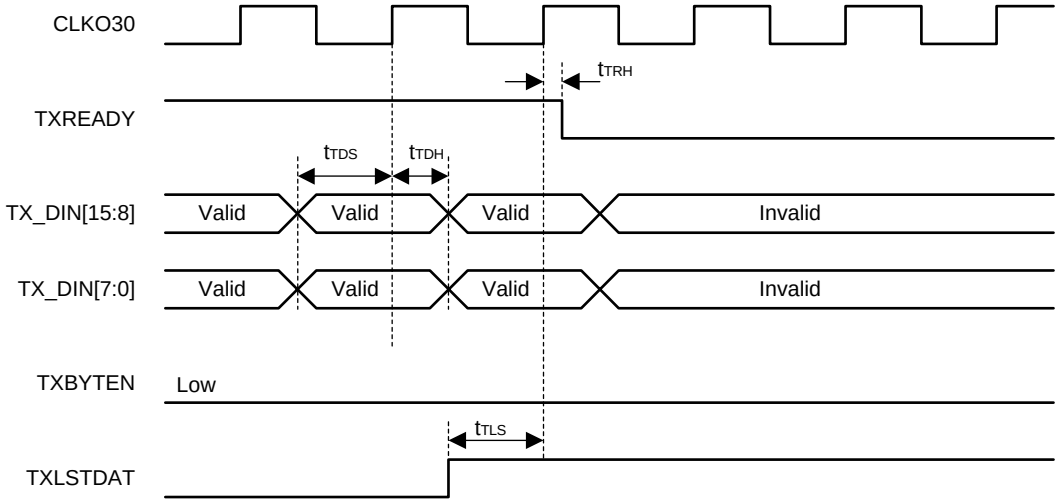
USB IN/PING Token Phase (Null Data Transfer)



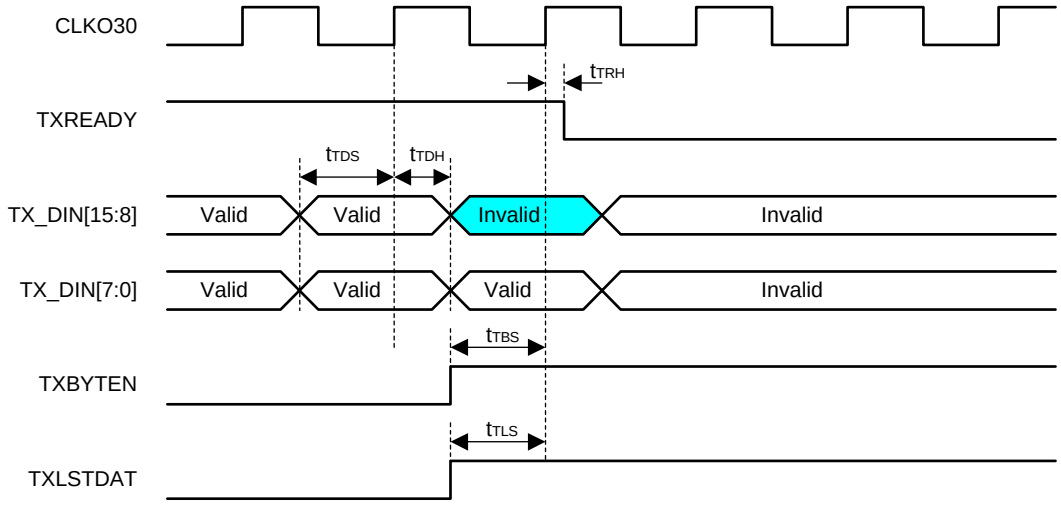
USB IN Start of Data Phase



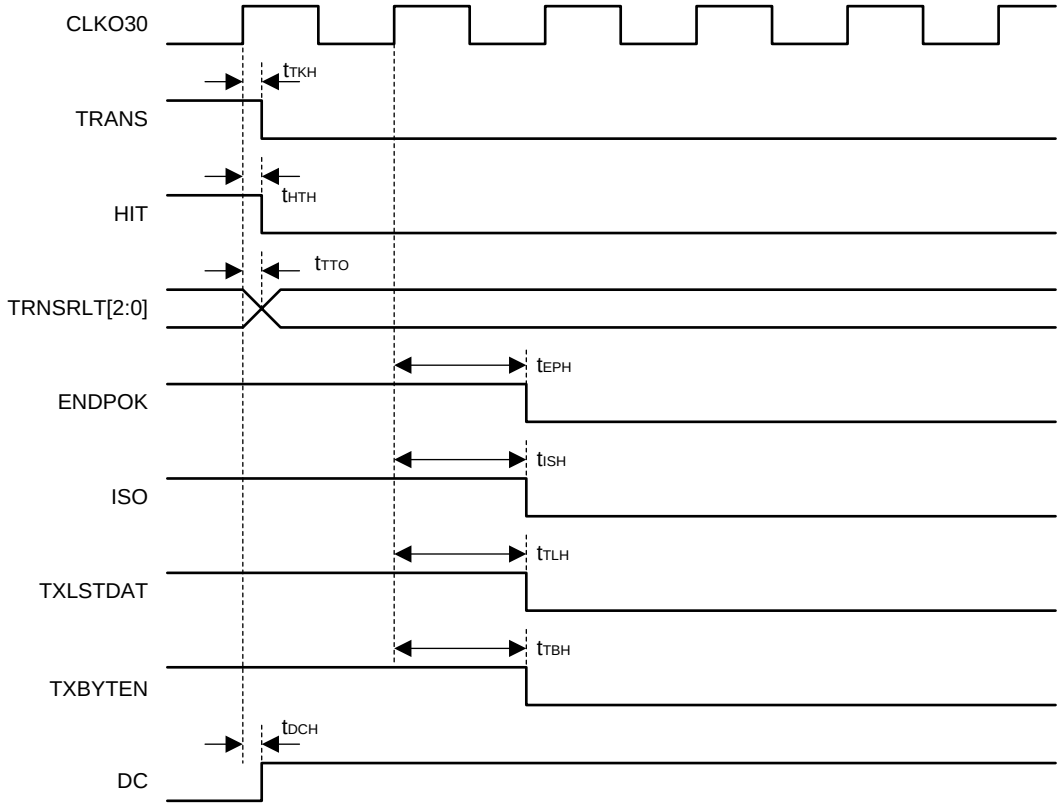
USB IN End of Data Phase (Word Boundary)



USB IN End of Data Phase (Byte Boundary)

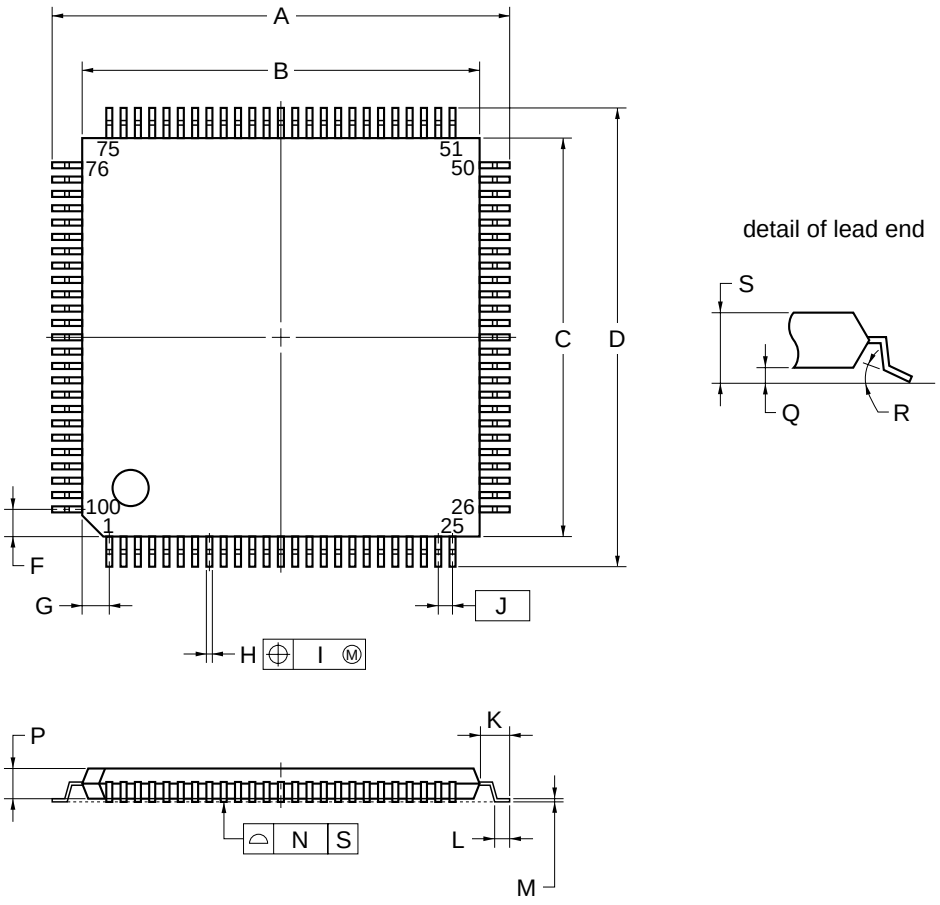


USB IN End of Handshake Phase



3. PACKAGE DRAWING

100-PIN PLASTIC TQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

S100GC-50-9EU-2

4. RECOMMENDED SOLDERING CONDITIONS

The μPD720120 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

μPD720120GC-9EU: 100-pin plastic TQFP (Fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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