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April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

# μPD720100A

## USB 2.0 HOST CONTROLLER

The μPD720100A complies with the Universal Serial Bus Specification Revision 2.0 and Open Host Controller Interface Specification for full-/low-speed signaling and Intel's Enhanced Host Controller Interface Specification for high-speed signaling and works up to 480 Mbps. The μPD720100A is integrated three host controller cores with PCI interface and USB 2.0 transceivers into a single chip.

**Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.**
**μPD720100A User's Manual: S15534E**

### FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- Compliant with Open Host Controller Interface Specification for USB Rev 1.0a
- Compliant with Enhanced Host Controller Interface Specification for USB Rev 0.95
- PCI multi-function device consists of two OHCI host controller cores for full-/low-speed signaling and one EHCI host controller core for high-speed signaling.
- Root hub with five (max.) downstream facing ports which are shared by OHCI and EHCI host controller core
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Configurable number of downstream facing ports (2 to 5)
- 32-bit 33 MHz host interface compliant to PCI Specification release 2.2.
- Supports PCI Mobile Design Guide Revision 1.1.
- Supports PCI-Bus Power Management Interface Specification release 1.1.
- PCI Bus bus-master access
- System clock is generated by 30 MHz X'tal or 48 MHz clock input.
- Operational registers direct-mapped to PCI memory space
- Legacy support for all downstream facing ports. Legacy support features allow easy migration for motherboard implementation.
- 3.3 V power supply, PCI signal pins have 5 V tolerant circuit.

### ORDERING INFORMATION

| | Part Number | Package | Remark |
|---|---|---|---|
| | μPD720100AGM-8ED | 160-pin plastic LQFP (Fine pitch) (24 × 24) | |
| | μPD720100AGM-8EY | 160-pin plastic LQFP (Fine pitch) (24 × 24) | |
| ★ | μPD720100AGM-8EY-A | 160-pin plastic LQFP (Fine pitch) (24 × 24) | Lead-free product |
| | μPD720100AS1-2C | 176-pin plastic FBGA (15 × 15) | |
| ★ | μPD720100AS1-2C-A | 176-pin plastic FBGA (15 × 15) | Lead-free product |

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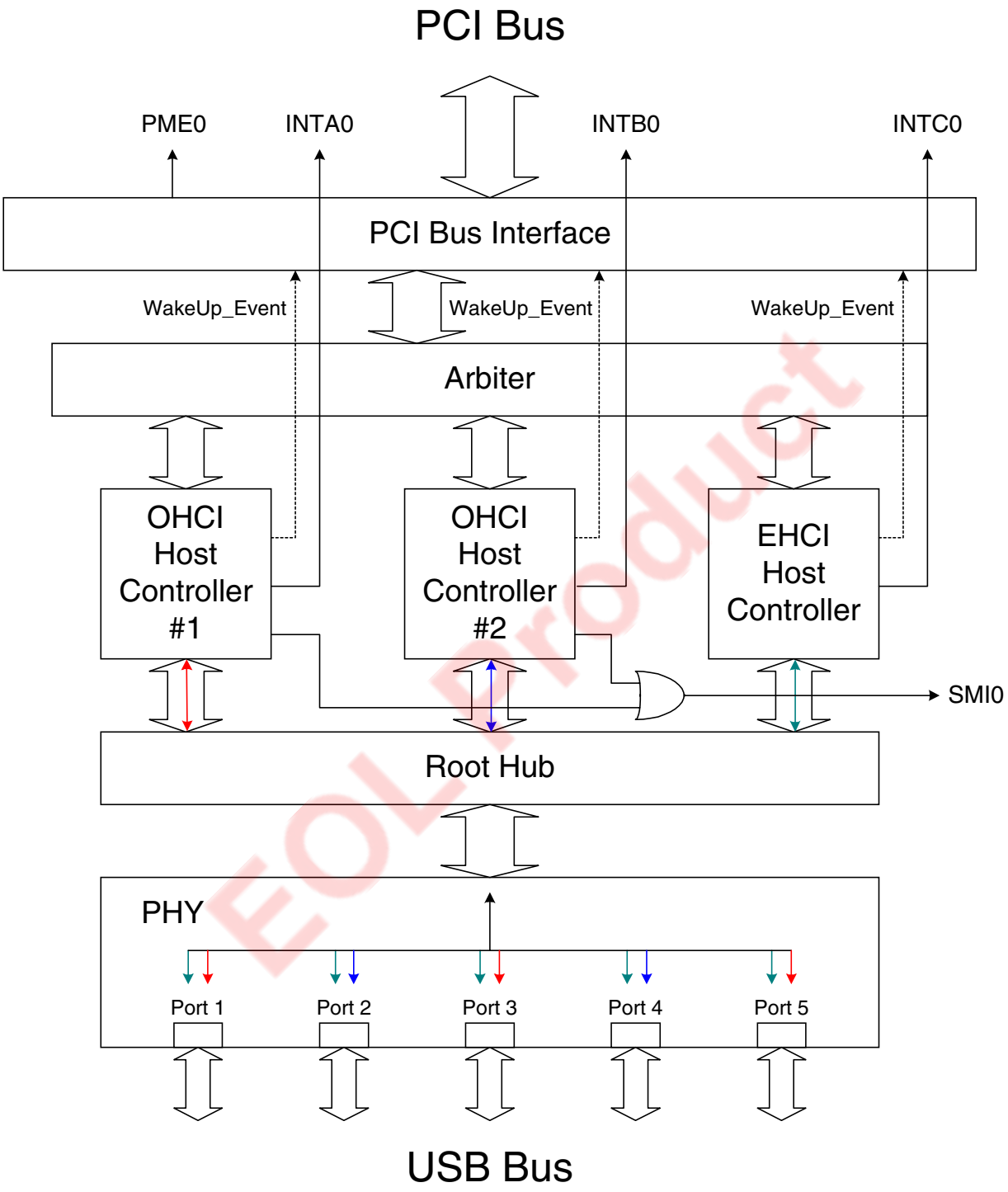
**Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**

Document No. S15535EJ3V0DS00 (3rd edition)
Date Published March 2005 NS CP (K)
Printed in Japan

**The mark ★ shows major revised points.**

## BLOCK DIAGRAM



| | |
|---|---|
| PCI Bus Interface | :handles 32-bits 33 MHz PCI Bus master and target function which comply with PCI specification release 2.2. The number of enabled ports are set by bit in configuration space. |
| Arbiter | :arbitrates among two OHCI Host controller cores and one EHCI Host controller core. |
| OHCI Host Controller #1 | :handles full- (12 Mbps)/low-speed (1.5 Mbps) signaling at port 1, 3, and 5. |
| OHCI Host Controller #2 | :handles full- (12 Mbps)/low-speed (1.5 Mbps) signaling at port 2 and 4. |
| EHCI Host Controller | :handles high- (480 Mbps) signaling at port 1, 2, 3, 4, and 5. |
| Root Hub | :handles USB hub function in Host controller and controls connection (routing) between Host controller core and port. |
| PHY | :consists of high-speed transceiver, full-/low-speed transceiver, serializer, deserializer, etc |
| INTA0 | :is the PCI interrupt signal for OHCI Host Controller #1. |
| INTB0 | :is the PCI interrupt signal for OHCI Host Controller #2. |
| INTC0 | :is the PCI interrupt signal for EHCI Host Controller. |
| SMI0 | :is the interrupt signal which is specified by Open Host Controller Interface Specification for USB Rev 1.0a. The SMI signal of each OHCI Host Controller appears at this signal. |
| PME0 | :is the interrupt signal which is specified by PCI-Bus Power Management Interface Specification release 1.1. Wakeup signal of each host controller core appears at this signal. |

## PIN CONFIGURATION

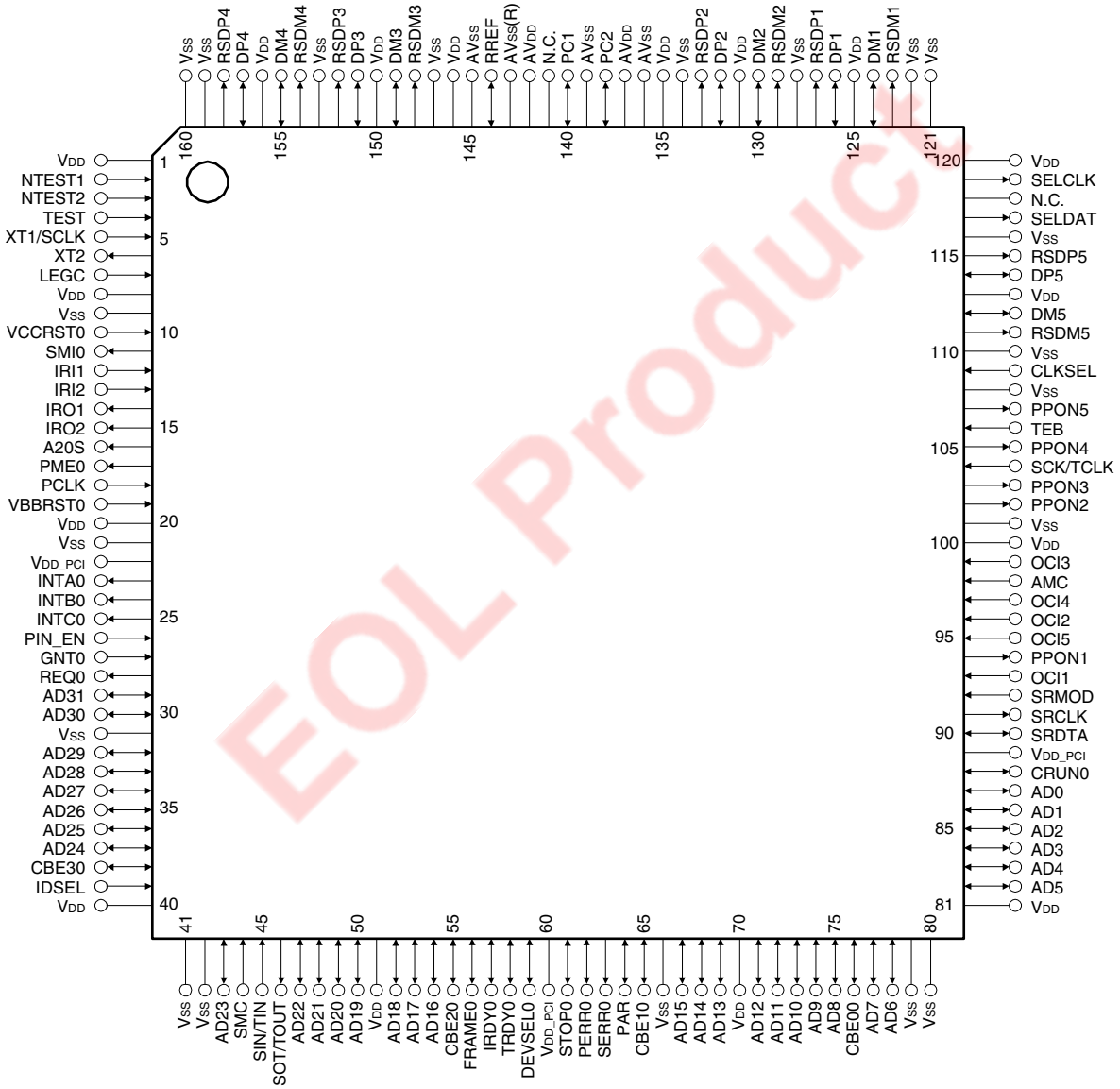
- **160-pin plastic LQFP (Fine pitch) (24 × 24)**

μPD720100AGM-8ED

μPD720100AGM-8EY

★ μPD720100AGM-8EY-A

### Top View



| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | $V_{DD}$ | 41 | $V_{SS}$ | 81 | $V_{DD}$ | 121 | $V_{SS}$ |
| 2 | NTEST1 | 42 | $V_{SS}$ | 82 | AD5 | 122 | $V_{SS}$ |
| 3 | NTEST2 | 43 | AD23 | 83 | AD4 | 123 | RSDM1 |
| 4 | TEST | 44 | SMC | 84 | AD3 | 124 | DM1 |
| 5 | XT1/SCLK | 45 | SIN/TIN | 85 | AD2 | 125 | $V_{DD}$ |
| 6 | XT2 | 46 | SOT/TOUT | 86 | AD1 | 126 | DP1 |
| 7 | LEGC | 47 | AD22 | 87 | AD0 | 127 | RSDP1 |
| 8 | $V_{DD}$ | 48 | AD21 | 88 | CRUN0 | 128 | $V_{SS}$ |
| 9 | $V_{SS}$ | 49 | AD20 | 89 | $V_{DD\_PCI}$ | 129 | RSDM2 |
| 10 | VCCRST0 | 50 | AD19 | 90 | SRDTA | 130 | DM2 |
| 11 | SMI0 | 51 | $V_{DD}$ | 91 | SRCLK | 131 | $V_{DD}$ |
| 12 | IRI1 | 52 | AD18 | 92 | SRMOD | 132 | DP2 |
| 13 | IRI2 | 53 | AD17 | 93 | OCI1 | 133 | RSDP2 |
| 14 | IRO1 | 54 | AD16 | 94 | PPON1 | 134 | $V_{SS}$ |
| 15 | IRO2 | 55 | CBE20 | 95 | OCI5 | 135 | $V_{DD}$ |
| 16 | A20S | 56 | FRAME0 | 96 | OCI2 | 136 | $AV_{SS}$ |
| 17 | PME0 | 57 | IRDY0 | 97 | OCI4 | 137 | $AV_{DD}$ |
| 18 | PCLK | 58 | TRDY0 | 98 | AMC | 138 | PC2 |
| 19 | VBBRST0 | 59 | DEVSEL0 | 99 | OCI3 | 139 | $AV_{SS}$ |
| 20 | $V_{DD}$ | 60 | $V_{DD\_PCI}$ | 100 | $V_{DD}$ | 140 | PC1 |
| 21 | $V_{SS}$ | 61 | STOP0 | 101 | $V_{SS}$ | 141 | N.C. |
| 22 | $V_{DD\_PCI}$ | 62 | PERR0 | 102 | PPON2 | 142 | $AV_{DD}$ |
| 23 | INTA0 | 63 | SERR0 | 103 | PPON3 | 143 | $AV_{SS}$ (R) |
| 24 | INTB0 | 64 | PAR | 104 | SCK/TCLK | 144 | RREF |
| 25 | INTC0 | 65 | CBE10 | 105 | PPON4 | 145 | $AV_{SS}$ |
| 26 | PIN_EN | 66 | $V_{SS}$ | 106 | TEB | 146 | $V_{DD}$ |
| 27 | GNT0 | 67 | AD15 | 107 | PPON5 | 147 | $V_{SS}$ |
| 28 | REQ0 | 68 | AD14 | 108 | $V_{SS}$ | 148 | RSDM3 |
| 29 | AD31 | 69 | AD13 | 109 | CLKSEL | 149 | DM3 |
| 30 | AD30 | 70 | $V_{DD}$ | 110 | $V_{SS}$ | 150 | $V_{DD}$ |
| 31 | $V_{SS}$ | 71 | AD12 | 111 | RSDM5 | 151 | DP3 |
| 32 | AD29 | 72 | AD11 | 112 | DM5 | 152 | RSDP3 |
| 33 | AD28 | 73 | AD10 | 113 | $V_{DD}$ | 153 | $V_{SS}$ |
| 34 | AD27 | 74 | AD9 | 114 | DP5 | 154 | RSDM4 |
| 35 | AD26 | 75 | AD8 | 115 | RSDP5 | 155 | DM4 |
| 36 | AD25 | 76 | CBE00 | 116 | $V_{SS}$ | 156 | $V_{DD}$ |
| 37 | AD24 | 77 | AD7 | 117 | SELDAT | 157 | DP4 |
| 38 | CBE30 | 78 | AD6 | 118 | N.C. | 158 | RSDP4 |
| 39 | IDSEL | 79 | $V_{SS}$ | 119 | SELCLK | 159 | $V_{SS}$ |
| 40 | $V_{DD}$ | 80 | $V_{SS}$ | 120 | $V_{DD}$ | 160 | $V_{SS}$ |

**Remark** $AV_{SS}$ (R) should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.

- **176-pin plastic FBGA (15 × 15)**

μPD720100AS1-2C

★ μPD720100AS1-2C-A

**Bottom View**

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | | 17 |
| 30 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 | 101 | 102 | 103 | 46 | 16 |
| 29 | 88 | 141 | 142 | 143 | 144 | 145 | 146 | 147 | 148 | 149 | 150 | 151 | 152 | 153 | 104 | 47 | 15 |
| 28 | 87 | 140 | | | | | 171 | 172 | 173 | | | | | 154 | 105 | 48 | 14 |
| 27 | 86 | 139 | | | | | | | | | | | | 155 | 106 | 49 | 13 |
| 26 | 85 | 138 | | | | | | | | | | | | 156 | 107 | 50 | 12 |
| 25 | 84 | 137 | | | | | | | | | | | | 157 | 108 | 51 | 11 |
| 24 | 83 | 136 | 170 | | | | | | | | | | 174 | 158 | 109 | 52 | 10 |
| 23 | 82 | 135 | 169 | | | | | | | | | | 175 | 159 | 110 | 53 | 9 |
| 22 | 81 | 134 | 168 | | | | | | | | | | 176 | 160 | 111 | 54 | 8 |
| 21 | 80 | 133 | | | | | | | | | | | | 161 | 112 | 55 | 7 |
| 20 | 79 | 132 | | | | | | | | | | | | 162 | 113 | 56 | 6 |
| 19 | 78 | 131 | | | | | | | | | | | | 163 | 114 | 57 | 5 |
| 18 | 77 | 130 | | | | | 167 | 166 | 165 | | | | | 164 | 115 | 58 | 4 |
| 17 | 76 | 129 | 128 | 127 | 126 | 125 | 124 | 123 | 122 | 121 | 120 | 119 | 118 | 117 | 116 | 59 | 3 |
| 16 | 75 | 74 | 73 | 72 | 71 | 70 | 69 | 68 | 67 | 66 | 65 | 64 | 63 | 62 | 61 | 60 | 2 |
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | 1 |
| U | T | R | P | N | M | L | K | J | H | G | F | E | D | C | B | A | |

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 45 | $V_{DD}$ | 89 | SELCLK | 133 | PPON1 |
| 2 | $V_{SS}$ | 46 | NTEST1 | 90 | $V_{SS}$ | 134 | OCI4 |
| 3 | SMC | 47 | NANDTEST | 91 | RSDM1 | 135 | $V_{SS}$ |
| 4 | AD20 | 48 | TEST | 92 | RSDP1 | 136 | SCK/TCLK |
| 5 | AD18 | 49 | $V_{SS}$ | 93 | DM2 | 137 | PPON5 |
| 6 | CBE20 | 50 | IRI1 | 94 | RSDP2 | 138 | $V_{SS}$ |
| 7 | DEVSEL0 | 51 | IRO2 | 95 | $AV_{SS}$ | 139 | $V_{DD}$ |
| 8 | $V_{DD\_PCI}$ | 52 | VBBRST0 | 96 | PC2 | 140 | RSDP5 |
| 9 | SERR0 | 53 | $V_{DD}$ | 97 | $AV_{SS}$ | 141 | $V_{DD}$ |
| 10 | $V_{SS}$ | 54 | INTA0 | 98 | DM3 | 142 | DP1 |
| 11 | AD14 | 55 | PIN_EN | 99 | DP3 | 143 | $V_{SS}$ |
| 12 | AD11 | 56 | REQ0 | 100 | RSDM4 | 144 | $V_{DD}$ |
| 13 | CBE00 | 57 | AD29 | 101 | DP4 | 145 | $V_{SS}$ |
| 14 | AD6 | 58 | AD25 | 102 | $V_{SS}$ | 146 | $AV_{DD}$ |
| 15 | $V_{SS}$ | 59 | CBE30 | 103 | $V_{SS}$ | 147 | N.C. |
| 16 | AD5 | 60 | N.C. | 104 | $V_{DD}$ | 148 | RREF |
| 17 | N.C. | 61 | IDSEL | 105 | NTEST2 | 149 | $V_{SS}$ |
| 18 | AD3 | 62 | $V_{SS}$ | 106 | LEGC | 150 | $V_{DD}$ |
| 19 | $V_{DD\_PCI}$ | 63 | AD23 | 107 | VCCRST0 | 151 | $V_{SS}$ |
| 20 | SRMOD | 64 | AD22 | 108 | IRI2 | 152 | DM4 |
| 21 | OCI5 | 65 | AD19 | 109 | A20S | 153 | XT1/SCLK |
| 22 | OCI3 | 66 | AD17 | 110 | PCLK | 154 | XT2 |
| 23 | $V_{DD}$ | 67 | FRAME0 | 111 | INTC0 | 155 | $V_{DD}$ |
| 24 | PPON3 | 68 | TRDY0 | 112 | AD31 | 156 | SMI0 |
| 25 | TEB | 69 | CBE10 | 113 | $V_{SS}$ | 157 | IRO1 |
| 26 | $V_{SS}$ | 70 | AD13 | 114 | AD27 | 158 | PME0 |
| 27 | DM5 | 71 | AD12 | 115 | AD24 | 159 | $V_{SS}$ |
| 28 | $V_{SS}$ | 72 | AD9 | 116 | $V_{DD}$ | 160 | INTB0 |
| 29 | N.C. | 73 | AD7 | 117 | SIN/TIN | 161 | GNT0 |
| 30 | N.C. | 74 | $V_{SS}$ | 118 | SOT/TOUT | 162 | AD30 |
| 31 | $V_{SS}$ | 75 | $V_{SS}$ | 119 | AD21 | 163 | AD28 |
| 32 | N.C. | 76 | $V_{DD}$ | 120 | $V_{DD}$ | 164 | AD26 |
| 33 | DM1 | 77 | AD4 | 121 | AD16 | 165 | $V_{SS}$ |
| 34 | RSDM2 | 78 | AD0 | 122 | IRDY0 | 166 | $V_{DD}$ |
| 35 | DP2 | 79 | SRDTA | 123 | STOP0 | 167 | PERR0 |
| 36 | $V_{DD}$ | 80 | OCI1 | 124 | PAR | 168 | $V_{SS}$ |
| 37 | $AV_{SS}$ | 81 | OCI2 | 125 | AD15 | 169 | $V_{SS}$ |
| 38 | PC1 | 82 | AMC | 126 | $V_{DD}$ | 170 | PPON2 |
| 39 | $AV_{SS}$ (R) | 83 | PPON4 | 127 | AD10 | 171 | $V_{SS}$ |
| 40 | $V_{DD}$ | 84 | CLKSEL | 128 | AD8 | 172 | $V_{SS}$ |
| 41 | RSDM3 | 85 | RSDM5 | 129 | AD2 | 173 | $AV_{DD}$ |
| 42 | RSDP3 | 86 | DP5 | 130 | AD1 | 174 | $V_{SS}$ |
| 43 | N.C.($V_{DD}$) | 87 | SELDAT | 131 | CRUN0 | 175 | $V_{DD}$ |
| 44 | RSDP4 | 88 | $V_{DD}$ | 132 | SRCLK | 176 | $V_{DD\_PCI}$ |

**Remarks 1.** Pin 43 can be opened. But this signal is connected to pin 45 in the package. Should not be connected to GND.

**2.** $AV_{SS}$ (R) should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.

## 1. PIN INFORMATION

(1/2)

| Pin Name | I/O | Buffer Type | Active Level | Function |
|---|---|---|---|---|
| AD (31 : 0) | I/O | 5 V PCI I/O | | PCI “AD [31 : 0]” signal |
| CBE (3 : 0)0 | I/O | 5 V PCI I/O | | PCI “C/BE [3 : 0]” signal |
| PAR | I/O | 5 V PCI I/O | | PCI “PAR” signal |
| FRAME0 | I/O | 5 V PCI I/O | | PCI “FRAME#” signal |
| IRDY0 | I/O | 5 V PCI I/O | | PCI “IRDY#” signal |
| TRDY0 | I/O | 5 V PCI I/O | | PCI “TRDY#” signal |
| STOP0 | I/O | 5 V PCI I/O | | PCI “STOP#” signal |
| IDSEL | I | 5 V PCI Input | | PCI “IDSEL” signal |
| DEVSEL0 | I/O | 5 V PCI I/O | | PCI “DEVSEL#” signal |
| REQ0 | O | 5 V PCI Output | | PCI “REQ#” signal |
| GNT0 | I | 5 V PCI Input | | PCI “GNT#” signal |
| PERR0 | I/O | 5 V PCI I/O | | PCI “PERR#” signal |
| SERR0 | O | 5 V PCI N-ch Open Drain | | PCI “SERR#” signal |
| INTA0 | O | 5 V PCI N-ch Open Drain | Low | PCI “INTA#” signal |
| INTB0 | O | 5 V PCI N-ch Open Drain | Low | PCI “INTB#” signal |
| INTC0 | O | 5 V PCI N-ch Open Drain | Low | PCI “INTC#” signal |
| PCLK | I | 5 V PCI Input | | PCI “CLK” signal |
| VBBRST0 | I | 5 V PCI Input | Low | Hardware Reset for Chip |
| CRUN0 | I/O | 5 V PCI I/O | | PCI “CLKRUN#” signal |
| PME0 | O | 5 V PCI N-ch Open Drain | Low | PCI “PME#” signal |
| VCCRST0 | I | 5 V tolerant Input | Low | RESET for Power Management |
| SMI0 | O | 5 V tolerant N-ch Open Drain | Low | System management interrupt output |
| PIN_EN | I | 5 V tolerant Input | High | PCI Interface enable |
| XT1/SCLK | I | Input | | System clock input or Oscillator In |
| XT2 | O | Output | | Oscillator Out |
| DP (5 : 1) | I/O | USB high speed D+I/O | | USB’s high speed D+ signal |
| DM (5 : 1) | I/O | USB high speed D−I/O | | USB’s high speed D− signal |
| RSDP (5 : 1) | O | USB full speed D+ O | | USB’s full speed D+ signal |
| RSDM (5 : 1) | O | USB full speed D− O | | USB’s full speed D− signal |
| OCI (5 : 1) | I (I/O) | 5 V tolerant Input | Low | USB Root Hub Port’s overcurrent status input |
| PPON (5 : 1) | O (I/O) | 5 V tolerant Output | High | USB Root Hub Port’s power supply control output |
| LEGC | I (I/O) | Input | High | Legacy support switch |
| IRI1 | I (I/O) | 5 V tolerant Input | High | INT input from keyboard |
| IRI2 | I (I/O) | 5 V tolerant Input | High | INT input from mouse |
| IRO1 | O | 5 V tolerant Output | High | INT output from keyboard |
| IRO2 | O | 5 V tolerant Output | High | INT output from mouse |
| A20S | O | 5 V tolerant 3-state Output | | GateA20 State output |

(2/2)

| Pin Name | I/O | Buffer Type | Active Level | Function |
|---|---|---|---|---|
| RREF | A | Analog | | Reference resistor |
| PC1 | A | Analog | | Capacitor for PLL |
| PC2 | A | Analog | | Capacitor for PLL |
| NTEST(2:1) | I | Input with 12 kΩ Pull down R | High | Test pin |
| SMC | I | Input with 50 kΩ Pull down R | High | Scan mode control |
| SIN/TIN | I | Input with 50 kΩ Pull down R | | Scan input or RAM BIST input |
| SOT/TOUT | O | Output | | Scan output or RAM BIST output |
| TEB | I | Input with 50 kΩ Pull down R | High | BIST enable |
| AMC | I | Input with 50 kΩ Pull down R | High | ATG mode control |
| SCK/TCLK | I | Input with 50 kΩ Pull down R | | Scan clock or RAM BIST clock |
| CLKSEL | I | Input with 50 kΩ Pull down R | | Clock select signal |
| TEST | I | Input with 50 kΩ Pull down R | High | Test Control |
| NANDTEST | I | Input with 50 kΩ Pull down R | High | NAND Tree Test enable |
| SELDAT | O | Output | | Test signal |
| SELCLK | O | Output | | Test signal |
| SRCLK | O | Output | | Serial ROM Clock Out |
| SRDTA | I/O | I/O | | Serial ROM Data |
| SRMOD | I | Input with 50 kΩ Pull down R | High | Serial ROM Input Enable |
| $AV_{DD}$ | | | | $V_{DD}$ for Analog circuit |
| $V_{DD}$ | | | | $V_{DD}$ |
| $V_{DD\_PCI}$ | | | | 5 V (5 V PCI) or 3.3 V (3.3 V PCI) |
| $AV_{SS}$ | | | | $V_{SS}$ for Analog circuit |
| $V_{SS}$ | | | | $V_{SS}$ |
| N.C. | | | | Not connect |

**Remarks 1.** “5 V tolerant“ means that the buffer is 3 V buffer with 5 V tolerant circuit.

**2.** “5 V PCI” indicates a PCI buffer, which complies with the 3 V PCI standard, has a 5 V tolerant circuit. It does not indicate a buffer that fully complies with 5 V PCI standard. However, this function can be used for evaluating the operation of a device on a 5V add-in card.

**3.** The signal marked as “(I/O)” in the above table operates as I/O signals during testing. However, they do not need to be considered in normal use.

## 2. ELECTRICAL SPECIFICATIONS

### 2.1 Buffer List

- 3 V input buffer with Pull down resister

  NTEST1, NTEST2, TEST, SMC, SIN/TIN, SRMOD, AMC, SCK/TCLK, CLKSEL, TEB

- 3 V output buffer

  SOT/TOUT ($I_{OL}$ = 9 mA), SRCLK ($I_{OL}$ = 3 mA)

- 3 V bi-directional buffer

  LEGC ($I_{OL}$ = 9 mA), SRDTA ($I_{OL}$ = 3 mA)

- 3 V Oscillator interface

  XT1/SCLK, XT2

- 5 V input buffer

  VCCRST0, PIN_EN

- 5 V $I_{OL}$ = 12 mA N-ch Open Drain buffer

  SMI0, PME0, INTA0, INTB0, INTC0, SERR0

- 5 V $I_{OL}$ = 6 mA 3-state Output buffer

  A20S

- 5 V $I_{OL}$ = 12 mA 3-state Output buffer

  IRO1, IRO2

- 5 V PCI Input buffer with enable (OR type)

  PCLK, VBBRST0, GNT0, IDSEL

- 5 V PCI $I_{OL}$ = 12 mA 3-state Output buffer

  REQ0

★ - 5 V PCI $I_{OL}$ = 9 mA bi-directional buffer with input enable (OR-type)

  AD(31:0), CBE(3:0)0, PAR, FRAME0, IRDY0, TRDY0, STOP0, DEVSEL0, PERR0, CRUN0, IRI(1:2), PPON(1:5), OCI(1:5)

- USB interface

  DP(1:5), DM(1:5), RSDP(1:5), RSDM(1:5), PC1, PC2, RREF, SELDAT, SELCLK

Above, “5 V” refers to a 3-V buffer with 5-V tolerant circuit. Therefore, it is possible to have a 5-V connection for an external bus, but the output level will be only up to 3 V, which is the $V_{DD}$ voltage. Similarly, “5 V PCI” above refers to a PCI buffer that has a 5-V tolerant circuit, which meets the 3-V PCI standard; it does not refer to a PCI buffer that meets the 5-V PCI standard.

## 2.2 Terminology

### Terms Used in Absolute Maximum Ratings

| Parameter | Symbol | Meaning |
|---|---|---|
| Power supply voltage | $V_{DD}$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to a $V_{DD}$ pin. |
| Input voltage | $V_I$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin. |
| Output voltage | $V_O$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin. |
| Operating temperature | $T_A$ | Indicates the ambient temperature range for normal logic operations. |
| Storage temperature | $T_{stg}$ | Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device. |

### Terms Used in Recommended Operating Range

| Parameter | Symbol | Meaning |
|---|---|---|
| Power supply voltage | $V_{DD}$ | Indicates the voltage range for normal logic operations occur when $V_{SS}$ = 0V. |
| High-level input voltage | $V_{IH}$ | Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer.<br>* If a voltage that is equal to or greater than the “MIN.” value is applied, the input voltage is guaranteed as high level voltage. |
| Low-level input voltage | $V_{IL}$ | Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer.<br>* If a voltage that is equal to or lesser than the “MAX.” value is applied, the input voltage is guaranteed as low level voltage. |

### Terms Used in DC Characteristics

| Parameter | Symbol | Meaning |
|---|---|---|
| Off-state output leakage current | $I_{OZ}$ | Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance. |
| Output short circuit current | $I_{OS}$ | Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level. |
| Input leakage current | $I_I$ | Indicates the current that flows when the input voltage is supplied to the input pin. |
| Low-level output current | $I_{OL}$ | Indicates the current that flows to the output pins when the rated low-level output voltage is being applied. |
| High-level output current | $I_{OH}$ | Indicates the current that flows from the output pins when the rated high-level output voltage is being applied. |

## 2.3 Electrical Specifications

### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | –0.5 to +4.6 | V |
| ★ | $AV_{DD}$ | | –0.5 to +4.6 | V |
| ★ | $V_{DD\_PCI}$ | | –0.5 to +6.0 | V |
| Input voltage, 5 V buffer | $V_I$ | 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>$V_I$ < $V_{DD}$ + 3.0 V | –0.5 to +6.6 | V |
| Input voltage, 3.3 V buffer | $V_I$ | 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>$V_I$ < $V_{DD}$ + 0.5 V | –0.5 to +4.6 | V |
| Output voltage, 5 V buffer | $V_O$ | 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>$V_O$ < $V_{DD}$ + 3.0 V | –0.5 to +6.6 | V |
| Output voltage, 3.3 V buffer | $V_O$ | 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>$V_O$ < $V_{DD}$ + 0.5 V | –0.5 to +4.6 | V |
| Operating temperature | $T_A$ | | 0 to +70 | °C |
| Storage temperature | $T_{stg}$ | | –65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

### Recommended Operating Ranges

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | $V_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| ★ | $AV_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| ★ | $V_{DD\_PCI}$ | In 3.3 V PCI | 3.0 | 3.3 | 3.6 | V |
| | | In 5 V PCI | 4.75 | 5.0 | 5.25 | V |
| High-level input voltage | $V_{IH}$ | | | | | |
| 3.3 V High-level input voltage | | | 2.0 | | $V_{DD}$ | V |
| 5.0 V High-level input voltage | | | 2.0 | | 5.5 | V |
| Low-level input voltage | $V_{IL}$ | | | | | |
| 3.3 V Low-level input voltage | | | 0 | | 0.8 | V |
| 5.0 V Low-level input voltage | | | 0 | | 0.8 | V |

**DC Characteristics ($V_{DD}$ = 3.0 to 3.6 V, $T_A$ = 0 to +70°C)**

**Control Pin Block**

| Parameter | Symbol | Condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Off-state output current | $I_{OZ}$ | $V_O = V_{DD}$ or $V_{SS}$ | | ±10 | μA |
| Output short circuit current | $I_{OS}$ Note | | | –250 | mA |
| Low-level output current | $I_{OL}$ | | | | |
| 3.3 V Low-level output current | | $V_{OL}$ = 0.4 V | 9.0 | | mA |
| 3.3 V Low-level output current | | $V_{OL}$ = 0.4 V | 3.0 | | mA |
| 5.0 V Low-level output current | | $V_{OL}$ = 0.4 V | 12.0 | | mA |
| 5.0 V Low-level output current | | $V_{OL}$ = 0.4 V | 6.0 | | mA |
| High-level output current | $I_{OH}$ | | | | |
| 3.3 V High-level output current | | $V_{OH}$ = 2.4 V | –9.0 | | mA |
| 3.3 V High-level output current | | $V_{OH}$ = 2.4 V | –3.0 | | mA |
| 5.0 V High-level output current | | $V_{OH}$ = 2.4 V | –2.0 | | mA |
| 5.0 V High-level output current | | $V_{OH}$ = 2.4 V | –2.0 | | mA |
| Input leakage current | $I_I$ | | | | |
| 3.3 V buffer | | $V_I = V_{DD}$ or $V_{SS}$ | | ±10 | μA |
| 3.3 V buffer with 50 kΩ PD | | $V_I = V_{DD}$ | | 191 | μA |
| 5.0 V buffer | | $V_I = V_{DD}$ or $V_{SS}$ | | ±10 | μA |

**Note** The output short circuit time is one second or less and is only for one pin on the LSI.

**PCI Interface Block**

| Parameter | Symbol | Condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{ih}$ | | 2.0 | 5.25 | V |
| Low-level input voltage | $V_{il}$ | | 0 | 0.8 | V |
| Low-level output current | $I_{OL}$ | $V_{OL}$ = 0.4 V | 12.0 | | mA |
| High-level output current | $I_{OH}$ | $V_{OH}$ = 2.4 V | –2.0 | | mA |
| Input high leakage current | $I_{ih}$ | $V_{in}$ = 2.7 | | 70 | μA |
| Input low leakage current | $I_{il}$ | $V_{in}$ = 0.5 | | –70 | μA |
| PME0 leakage current | $I_{off}$ | $V_O$ < 3.6 V<br>$V_{CC}$ off or floating | | 1 | μA |

**USB Interface Block**

| Parameter | Symbol | Conditions | MIN | MAX | Unit |
|---|---|---|---|---|---|
| Serial Resistor between DP (DM) and RSDP (RSDM). | $R_S$ | | 35.64 | 36.36 | Ω |
| Output pin impedance | $Z_{HSDRV}$ | Includes $R_S$ resistor | 40.5 | 49.5 | Ω |
| **Input Levels for Low-/full-speed:** | | | | | |
| High-level input voltage (drive) | $V_{IH}$ | | 2.0 | | V |
| High-level input voltage (floating) | $V_{IHZ}$ | | 2.7 | 3.6 | |
| Low-level input voltage | $V_{IL}$ | | | 0.8 | V |
| Differential input sensitivity | $V_{DI}$ | \|(D+) – (D–)\| | 0.2 | | V |
| Differential Common mode Range | $V_{CM}$ | Includes $V_{DI}$ range | 0.8 | 2.5 | V |
| **Output Levels for Low-/full-speed:** | | | | | |
| High-level output voltage | $V_{OH}$ | $R_L$ of 14.25 kΩ to GND | 2.8 | 3.6 | V |
| Low-level output voltage | $V_{OL}$ | $R_L$ of 1.425 kΩ to 3.6 V | 0.0 | 0.3 | V |
| SE1 | $V_{OSE1}$ | | 0.8 | | V |
| Output signal crossover point voltage | $V_{CRS}$ | | 1.3 | 2.0 | V |
| **Input Levels for High-speed:** | | | | | |
| High-speed squelch detection threshold (differential signal) | $V_{HSSQ}$ | | 100 | 150 | mV |
| High-speed disconnect detection threshold (differential signal) | $V_{HSDSC}$ | | 525 | 625 | mV |
| High-speed data signaling common mode voltage range | $V_{HSCM}$ | | –50 | +500 | mV |
| High-speed differential input signaling level | See Figure 2-4. | | | | |
| **Output Levels for High-speed:** | | | | | |
| High-speed idle state | $V_{HSOI}$ | | –10.0 | +10 | mV |
| High-speed data signaling high | $V_{HSOH}$ | | 360 | 440 | mV |
| High-speed data signaling low | $V_{HSOL}$ | | –10.0 | +10 | mV |
| Chirp J level (different signal) | $V_{CHIRPJ}$ | | 700 | 1100 | mV |
| Chirp K level (different signal) | $V_{CHIRPK}$ | | –900 | –500 | mV |

**Figure 2-1. Differential Input Sensitivity Range for Low-/full-speed**

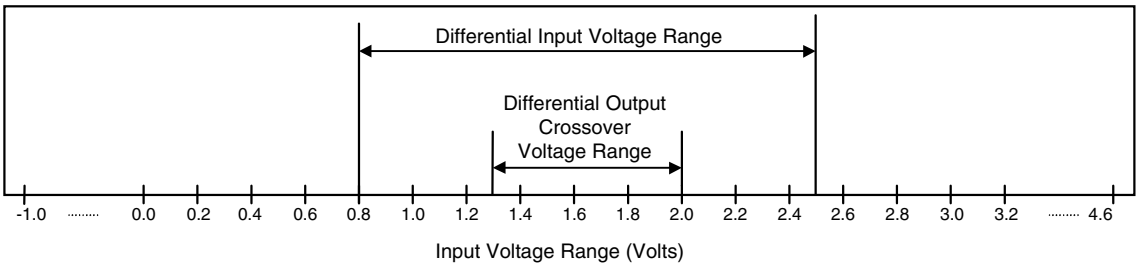



**Figure 2-2. Full-speed Buffer $V_{OH}/I_{OH}$ Characteristics for High-speed Capable Transceiver**

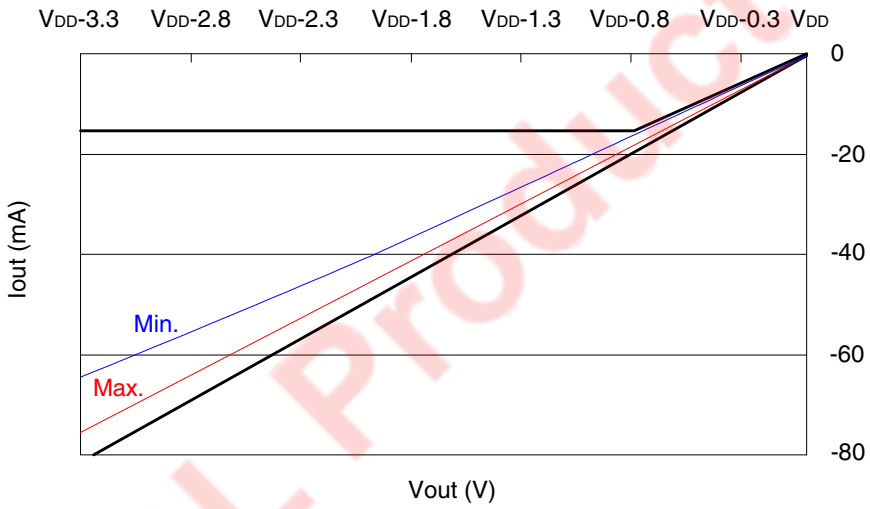



**Figure 2-3. Full-speed Buffer $V_{OL}/I_{OL}$ Characteristics for High-speed Capable Transceiver**

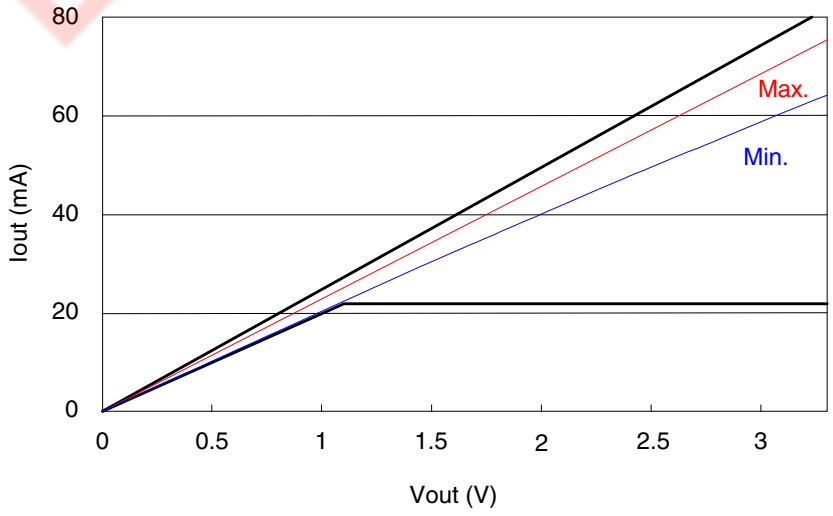


**Figure 2-4. Receiver Sensitivity for Transceiver at DP/DM**

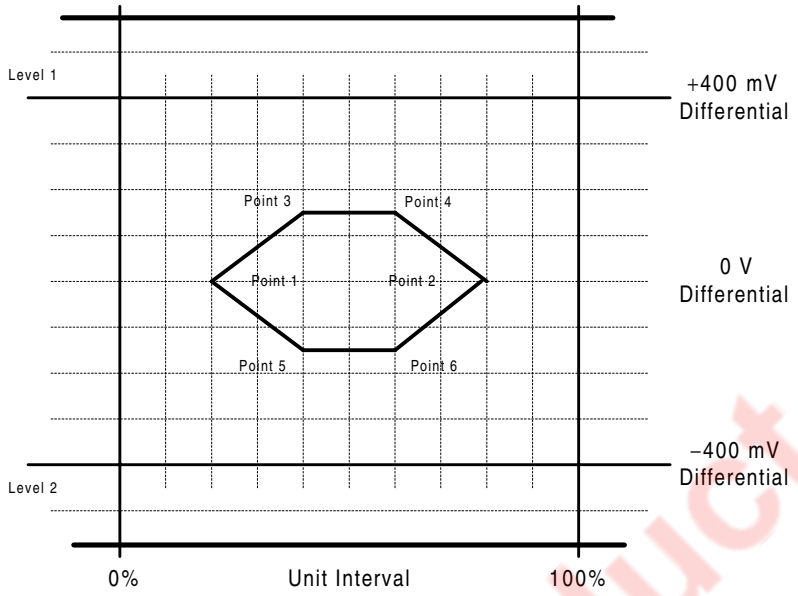
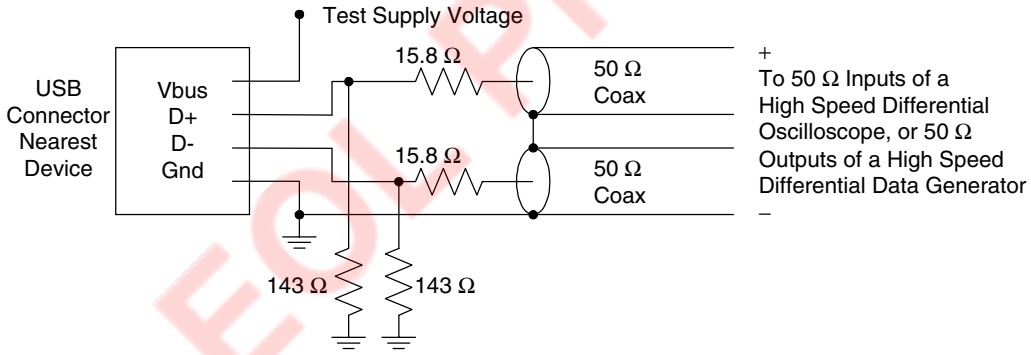



**Figure 2-5. Receiver Measurement Fixtures**






**Pin Capacitance**

| Parameter | Symbol | Condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_I$ | $V_{DD}$ = 0 V, $T_A$ = 25°C | 6 | 8 | pF |
| Output capacitance | $C_O$ | $f_C$ = 1 MHz | 10 | 12 | pF |
| I/O capacitance | $C_{IO}$ | Unmeasured pins returned to 0 V | 10 | 12 | pF |
| PCI input pin capacitance | $C_{in}$ | | | 8 | pF |
| PCI clock input pin capacitance | $C_{clk}$ | | 6 | 8 | pF |
| PCI IDSEL input pin capacitance | $C_{IDSEL}$ | | | 8 | pF |

**Power Consumption**

| Parameter | Symbol | Condition | TYP. | Unit |
|---|---|---|---|---|
| Power Consumption | $P_{WD0-0}$ | The power consumption under the state without suspend. Device state = D0, All the ports does not connect to any function. Note 1 | 168.0 | mA |
| | $P_{WD0-2}$ | The power consumption under the state without suspend. Device state = D0, The number of active ports is 2. Note 2 | | |
| ★ | | Full- or low-speed device(s) is (are) on the port. | 186.2 | mA |
| | | High-speed device(s) is (are) on the port. | 301.6 | mA |
| | $P_{WD0-3}$ | The power consumption under the state without suspend. Device state = D0, The number of active ports is 3. Note 2 | | |
| ★ | | Full- or low-speed device(s) is (are) on the port. | 195.3 | mA |
| | | High-speed device(s) is (are) on the port. | 368.4 | mA |
| | $P_{WD0-4}$ | The power consumption under the state without suspend. Device state = D0, The number of active ports is 4. Note 2 | | |
| ★ | | Full- or low-speed device(s) is (are) on the port. | 204.4 | mA |
| | | High-speed device(s) is (are) on the port. | 435.2 | mA |
| | $P_{WD0-5}$ | The power consumption under the state without suspend. Device state = D0, The number of active ports is 5. Note 2 | | |
| ★ | | Full- or low-speed device(s) is (are) on the port. | 213.5 | mA |
| | | High-speed device(s) is (are) on the port. | 502.0 | mA |
| | $P_{WD0\_S}$ | The power consumption under suspend state. Device state = D0, The internal clock is stopped. Note 3 | 136.2 | mA |
| | $P_{WD0\_C}$ | The power consumption under suspend state during PCI clock is stopped by CRUN0. Device state = D0, The internal clock is stopped. Note 3 | 113.0 | mA |
| | $P_{WD1}$ | Device state = D1, Analog PLL output is stopped. Note 3, 4 | 24.7 | mA |
| | $P_{WD2}$ | Device state = D2, Analog PLL output is stopped. Note 3, 4 | 10.9 | mA |
| | $P_{WD3H}$ | Device state = $D3_{hot}$, PIN_EN = High Analog PLL output is stopped. Note 3, 4 | 10.9 | mA |
| | $P_{WD3C}$ | Device state = $D3_{cold}$ , PIN_EN = Low Oscillator output is stopped. Note 3, 4, 5 | 650 | μA |

**Notes**

1. When any device is not connected to all the ports of HC, the power consumption for HC does not depend on the number of active ports.
2. The number of active ports is set by the value of Port No field in PCI configuration space EXT register.
3. For the condition of clock stop, see **μPD720100A User's Manual 7.3 Control for System Clock Operation**.
4. When the device state = D1, PCI clock is defined as it is running. When the device state = D2 or D3, PCI clock is defined as it is stopped.
5. If 48 MHz oscillator clock-in is used, power consumption for oscillator block + HC chip will be more than 15 mA.

**System Clock Ratings**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | $f_{CLK}$ | X'tal | –500 ppm | 30 | +500 ppm | MHz |
| | | Oscillator block | –500 ppm | 48 | +500 ppm | MHz |
| Clock Duty cycle | $t_{DUTY}$ | | 40 | 50 | 60 | % |

**Remarks 1.** Recommended accuracy of clock frequency is ± 100 ppm.

**2.** Required accuracy of X'tal or Oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

**AC Characteristics ($V_{DD}$ = 3.0 to 3.6 V, $T_A$ = 0 to +70°C)**

**PCI Interface Block**

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| PCI clock cycle time | $t_{cyc}$ | | 30 | | ns |
| PCI clock pulse, high-level width | $t_{high}$ | | 11 | | ns |
| PCI clock pulse, low-level width | $t_{low}$ | | 11 | | ns |
| PCI clock, rise slew rate | $S_{cr}$ | 0.2 $V_{DD}$ to 0.6 $V_{DD}$ | 1 | 4 | V/ns |
| PCI clock, fall slew rate | $S_{cf}$ | 0.2 $V_{DD}$ to 0.6 $V_{DD}$ | 1 | 4 | V/ns |
| PCI reset active time (vs. power supply stability) | $t_{rst}$ | | 1 | | ms |
| PCI reset active time (vs. CLK Start) | $t_{rst-clk}$ | | 100 | | μs |
| Output float delay time (vs. RST0↓) | $t_{rst-off}$ | | | 40 | ns |
| PCI reset rise slew rate | $S_{rr}$ | | 50 | | mV/ns |
| PCI bus signal output time (vs. PCLK↑) | $t_{val}$ | | 2 | 11 | ns |
| PCI point-to-point signal output time (vs. PCLK↑) | $t_{val}$ (ptp) | REQ0 | 2 | 12 | ns |
| Output delay time (vs. PCLK↑) | $t_{on}$ | | 2 | | ns |
| Output float delay time (vs. PCLK↑) | $t_{off}$ | | | 28 | ns |
| Input setup time (vs. PCLK↑) | $t_{su}$ | | 7 | | ns |
| Point-to-point input setup time (vs. PCLK↑) | $t_{su}$ (ptp) | GNT0 | 10 | | ns |
| Input hold time | $t_h$ | | 0 | | ns |

**USB Interface Block**

(1/2)

| | Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| | **Low Source Electrical Characteristics** | | | | | |
| ★ | Rise time (10% - 90%) | $t_{LR}$ | $C_L$ = 200 pF – 600 pF, $R_S$ = 36 Ω | 75 | 300 | ns |
| ★ | Fall time (90% - 10%) | $t_{LF}$ | $C_L$ = 200 pF – 600 pF, $R_S$ = 36 Ω | 75 | 300 | ns |
| | Differential Rise and Fall Time matching | $t_{LRFM}$ | ($t_{LR}/t_{LF}$) | 80 | 125 | % |
| | Low-speed Data Rate | $t_{LDRATHS}$ | Average bit rate | 1.49925 | 1.50075 | Mbps |
| | Source Jitter Total (including frequency tolerance):<br>To Next Transition<br>For Paired Transitions | <br>$t_{DDJ1}$<br>$t_{DDJ2}$ | | <br>–25<br>–14 | <br>+25<br>+14 | <br>ns<br>ns |
| | Source Jitter for Differential Transition to SE0 transition | $t_{LDEOP}$ | | -40 | +100 | ns |
| | Receiver Jitter:<br>To Next Transition<br>For Paired Transitions | <br>$t_{UJR1}$<br>$t_{UJR2}$ | | <br>–152<br>–200 | <br>+152<br>+200 | <br>ns<br>ns |
| | Source SE0 interval of EOP | $t_{LEOPT}$ | | 1.25 | 1.50 | μs |
| | Receiver SE0 interval of EOP | $t_{LEOPR}$ | | 670 | | ns |
| | Width of SE0 interval during differential transition | $t_{FST}$ | | | 210 | ns |
| | **Full-speed Source Electrical Characteristics** | | | | | |
| | Rise time (10% - 90%) | $t_{FR}$ | $C_L$ = 50 pF, $R_S$ = 36 Ω | 4 | 20 | ns |
| | Fall time (90% - 10%) | $t_{FF}$ | $C_L$ = 50 pF, $R_S$ = 36 Ω | 4 | 20 | ns |
| | Differential Rise and Fall Time matching | $t_{FRFM}$ | ($t_{FR}/t_{FF}$) | 90 | 111.11 | % |
| | Full-speed Data Rate | $t_{FDRATHS}$ | Average bit rate | 11.9940 | 12.0060 | Mbps |
| | Frame Interval | $t_{FRAME}$ | | 0.9995 | 1.0005 | ms |
| | Consecutive Frame Interval Jitter | $t_{RFI}$ | No clock adjustment | | 42 | ns |
| | Source Jitter Total (including frequency tolerance):<br>To Next Transition<br>For Paired Transitions | <br>$t_{DJ1}$<br>$t_{DJ2}$ | | <br>–3.5<br>–4.0 | <br>+3.5<br>+4.0 | <br>ns<br>ns |
| | Source Jitter for Differential Transition to SE0 transition | $t_{FDEOP}$ | | –2 | +5 | ns |
| | Receiver Jitter:<br>To Next Transition<br>For Paired Transitions | <br>$t_{JR1}$<br>$t_{JR2}$ | | <br>–18.5<br>–9 | <br>+18.5<br>+9 | <br>ns<br>ns |
| | Source SE0 interval of EOP | $t_{FEOPT}$ | | 160 | 175 | ns |
| | Receiver SE0 interval of EOP | $t_{FEOPR}$ | | 82 | | ns |
| | Width of SE0 interval during differential transition | $t_{FST}$ | | | 14 | ns |

(2/2)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| **High-speed Source Electrical Characteristics** | | | | | |
| Rise time (10% - 90%) | $t_{HSR}$ | | 500 | | ps |
| Fall time (90% - 10%) | $t_{HSF}$ | | 500 | | ps |
| Driver waveform | See Figure 2-6. | | | | |
| High-speed Data Rate | $t_{HSDRAT}$ | | 479.760 | 480.240 | Mbps |
| Microframe Interval | $t_{HSFRAM}$ | | 124.9375 | 125.0625 | μs |
| Consecutive Microframe Interval Difference | $t_{HSRFI}$ | | | 4 high-speed | Bit times |
| Data source jitter | See Figure 2-6. | | | | |
| Receiver jitter tolerance | See Figure 2-4. | | | | |
| **Hub event Timings** | | | | | |
| Time to detect a downstream facing port connect event | $t_{DCNN}$ | | 2.5 | 2000 | μs |
| Time to detect a disconnect event at a downstream facing port: | $t_{DDIS}$ | | 2.0 | 2.5 | μs |
| Duration of driving resume to a downstream port | $t_{DRSMDN}$ | Nominal | 20 | | ms |
| Time from detecting downstream resume to rebroadcast. | $t_{URSM}$ | | | 1.0 | ms |
| Inter-packet Delay for packets traveling in same direction for high-speed | $t_{HSIPDSD}$ | | 88 | | Bit times |
| Inter-packet Delay for packets traveling in opposite direction for high-speed | $t_{HSIPDOD}$ | | 8 | | Bit times |
| Inter-packet delay for root hub response for high-speed | $t_{HSRSPIPD1}$ | | | 192 | Bit times |
| Time for which a Chirp J or Chirp K must be continuously detected during Reset handshake | $t_{FILT}$ | | 2.5 | | μs |
| Time after end of device Chirp K by which hub must start driving first Chirp K | $t_{WTDCH}$ | | | 100 | μs |
| Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream during reset | $t_{DCHBIT}$ | | 40 | 60 | μs |
| Time before end of reset by which a hub must end its downstream chirp sequence | $t_{DCHSE0}$ | | 100 | 500 | μs |

**Figure 2-6. Transmit Waveform for Transceiver at DP/DM**

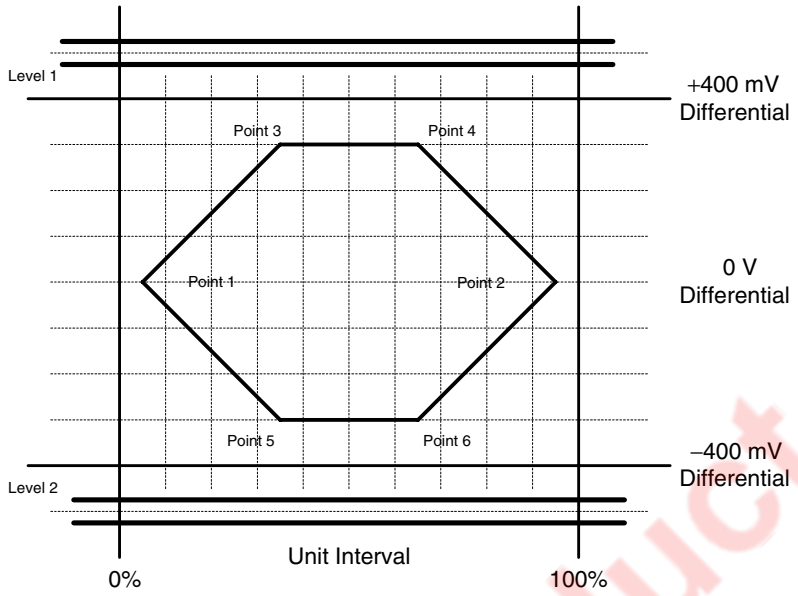
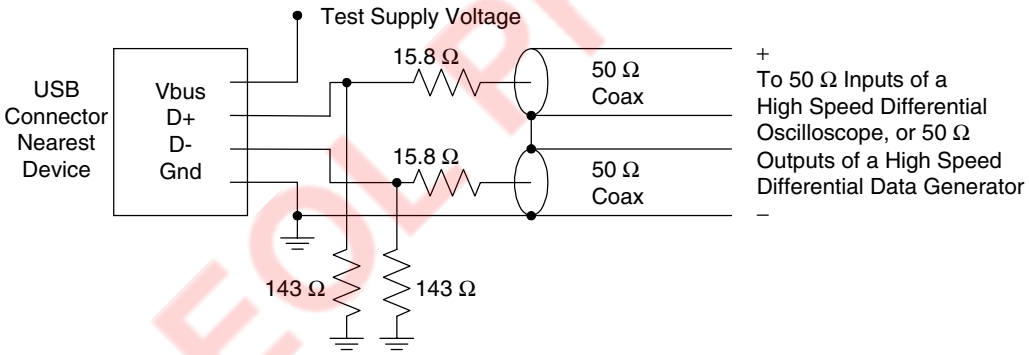
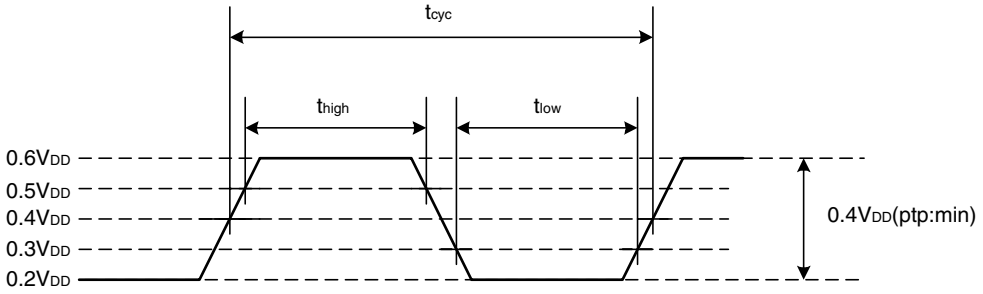



**Figure 2-7. Transmitter Measurement Fixtures**

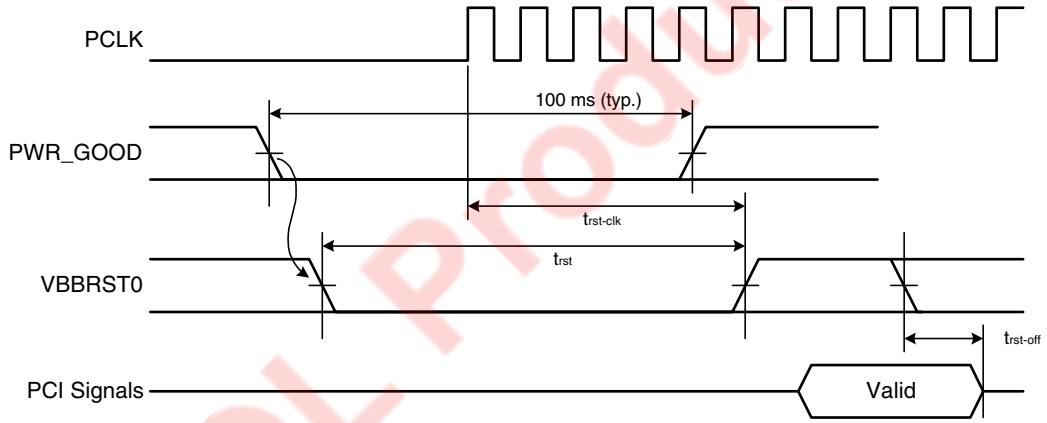


### Timing Diagram

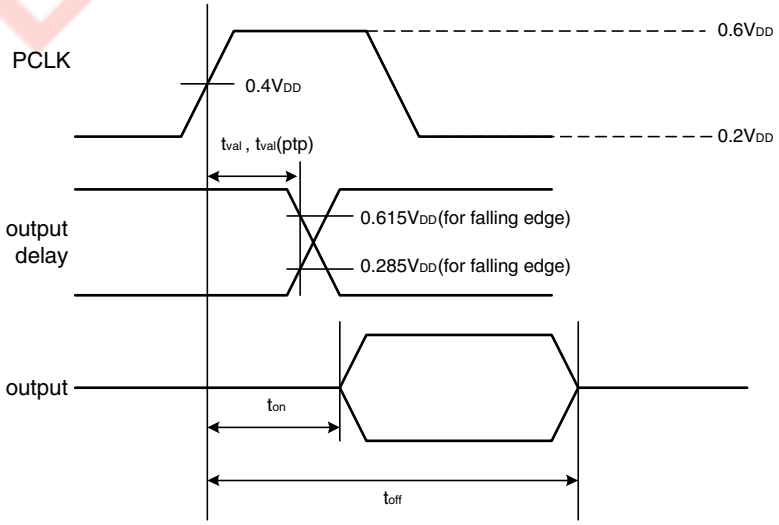
#### PCI Clock



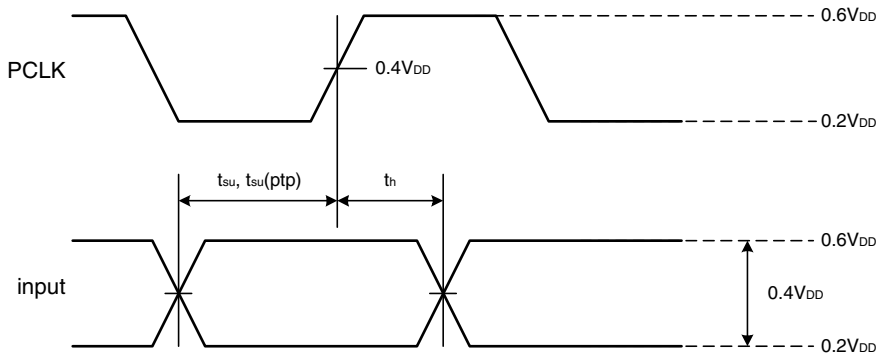

#### PCI Reset



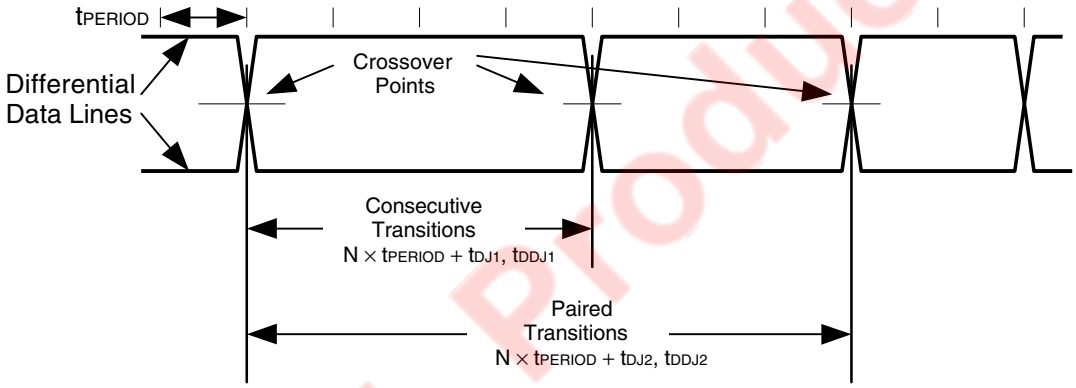

#### PCI Output Timing Measurement Condition



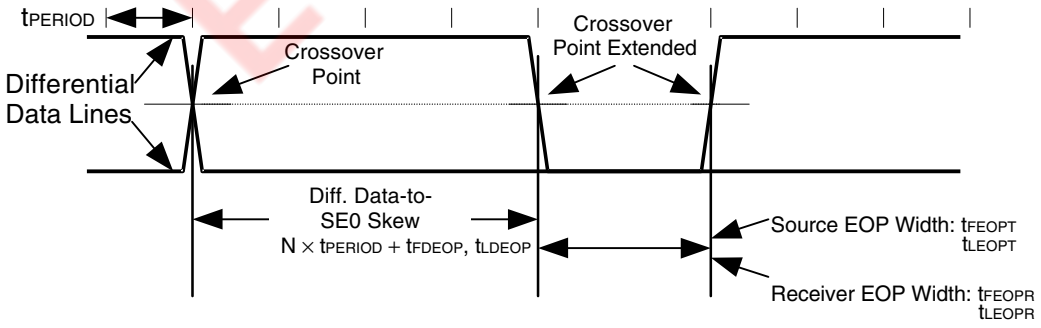
**PCI Input Timing Measurement Condition**



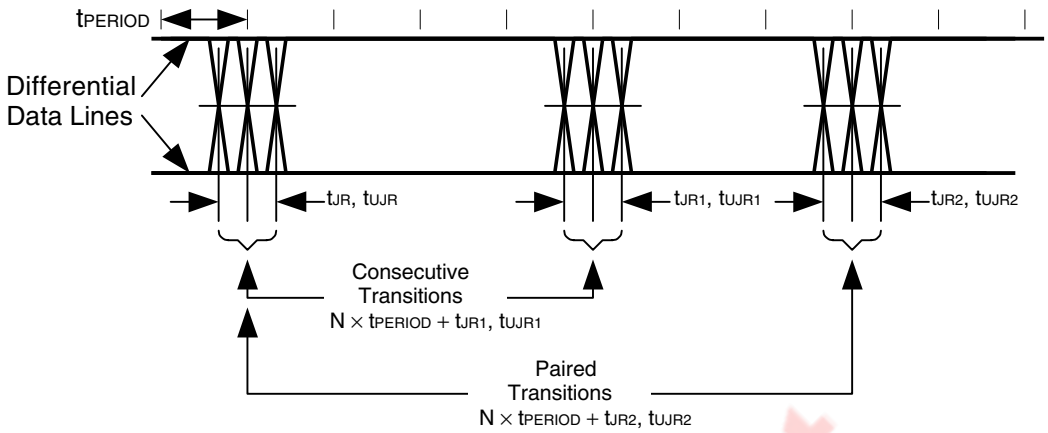

**USB Differential Data Jitter for Low-/full-speed**



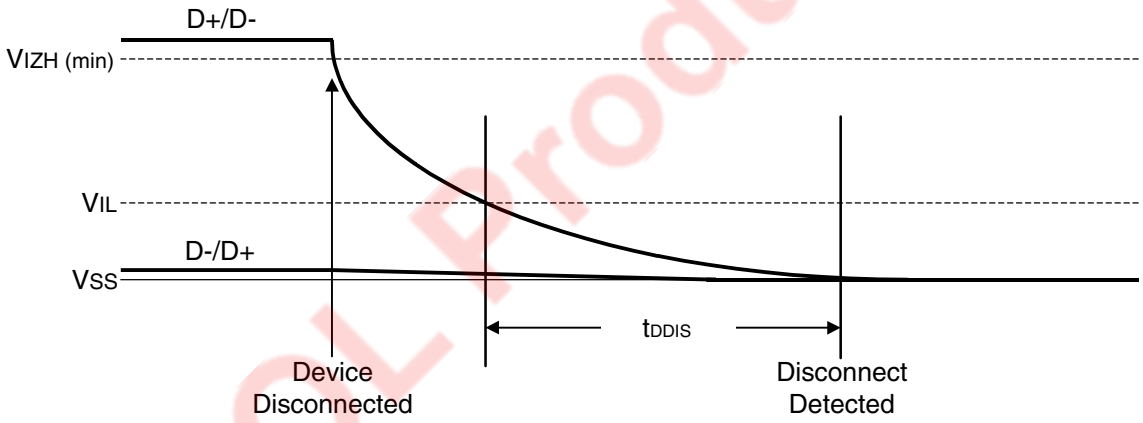

**USB Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed**



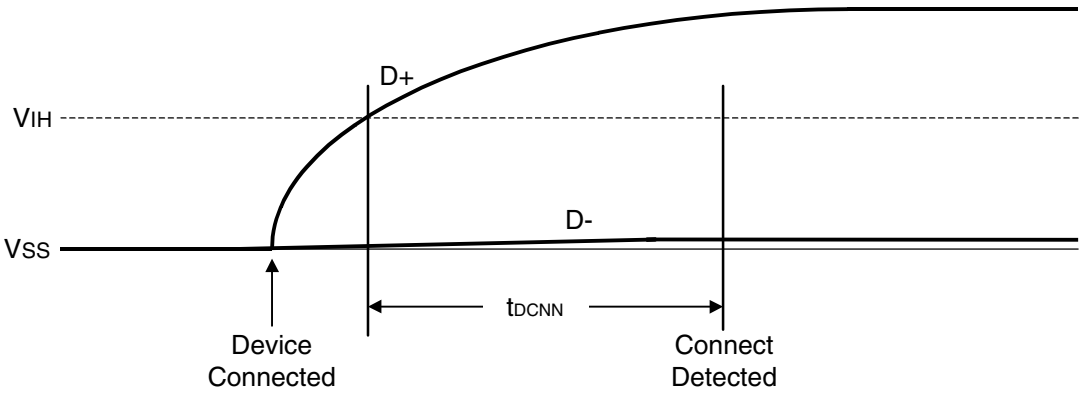
**USB Receiver Jitter Tolerance for Low-/full-speed**



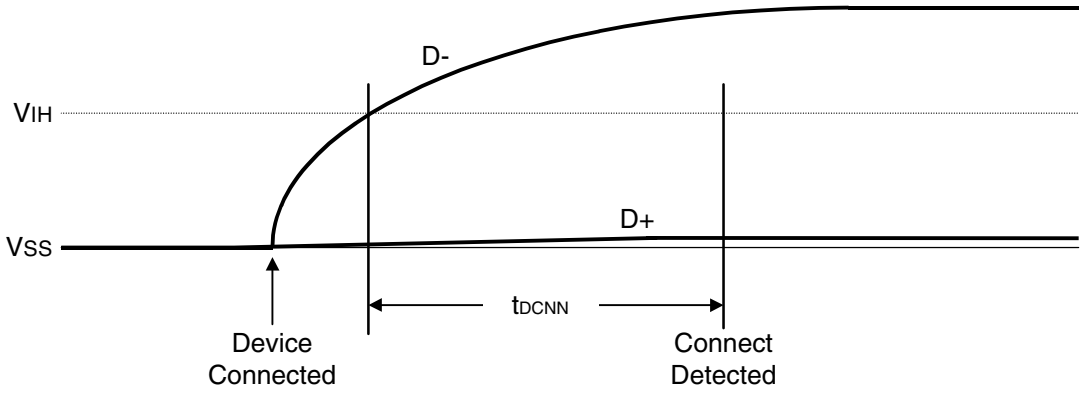

**Low-/full-speed Disconnect Detection**




**Full-/high-speed Device Connect Detection**

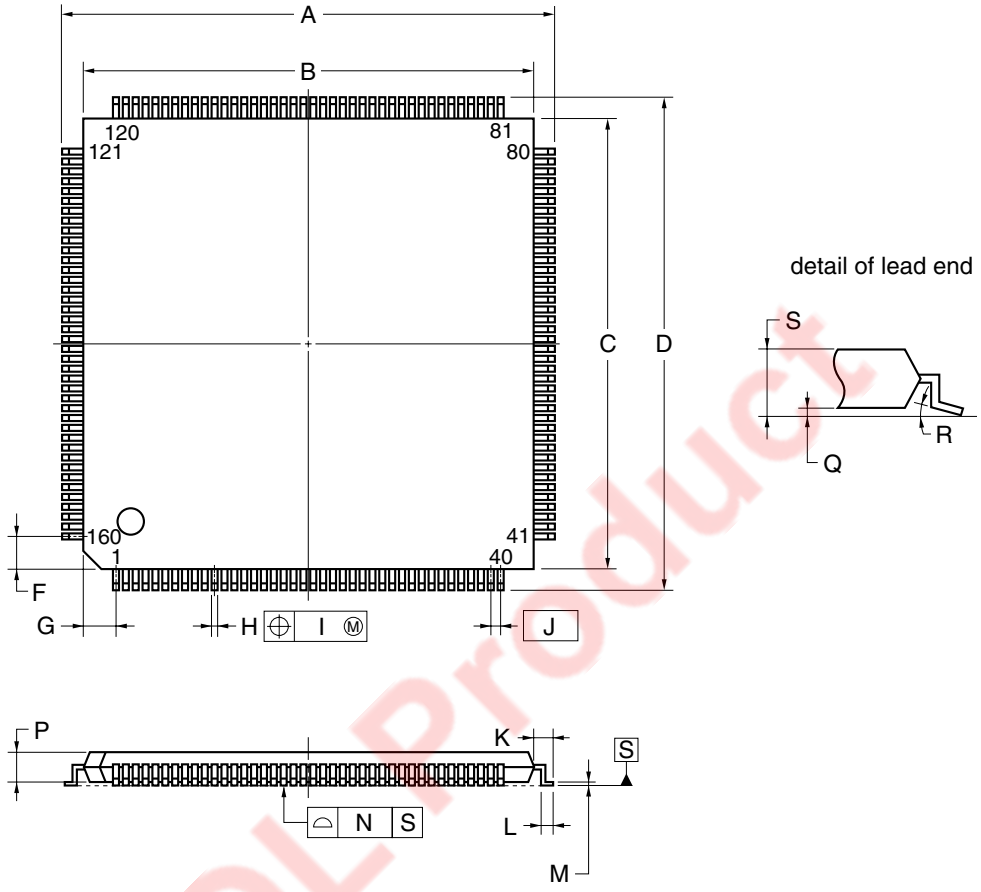


**Low-speed Device Connect Detection**



## 3. PACKAGE DRAWING

### 160-PIN PLASTIC LQFP (FINE PITCH) (24x24)



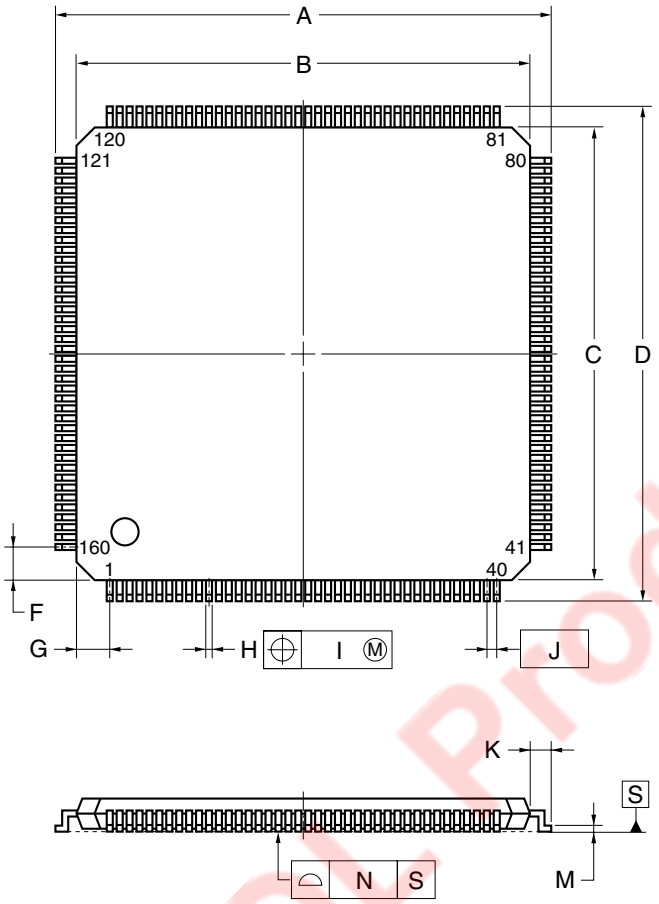

**NOTE**

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

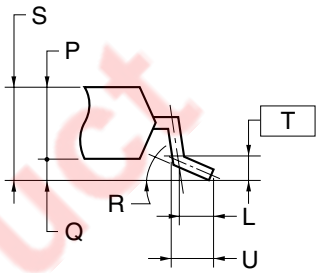
| ITEM | MILLIMETERS |
|---|---|
| A | 26.0±0.2 |
| B | 24.0±0.2 |
| C | 24.0±0.2 |
| D | 26.0±0.2 |
| F | 2.25 |
| G | 2.25 |
| H | $0.22^{+0.05}_{-0.04}$ |
| I | 0.10 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | $0.145^{+0.055}_{-0.045}$ |
| N | 0.10 |
| P | 1.4±0.1 |
| Q | 0.125±0.075 |
| R | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |
| S | 1.7 MAX. |

S160GM-50-8ED-3

## 160-PIN PLASTIC LQFP (FINE PITCH) (24x24)




detail of lead end



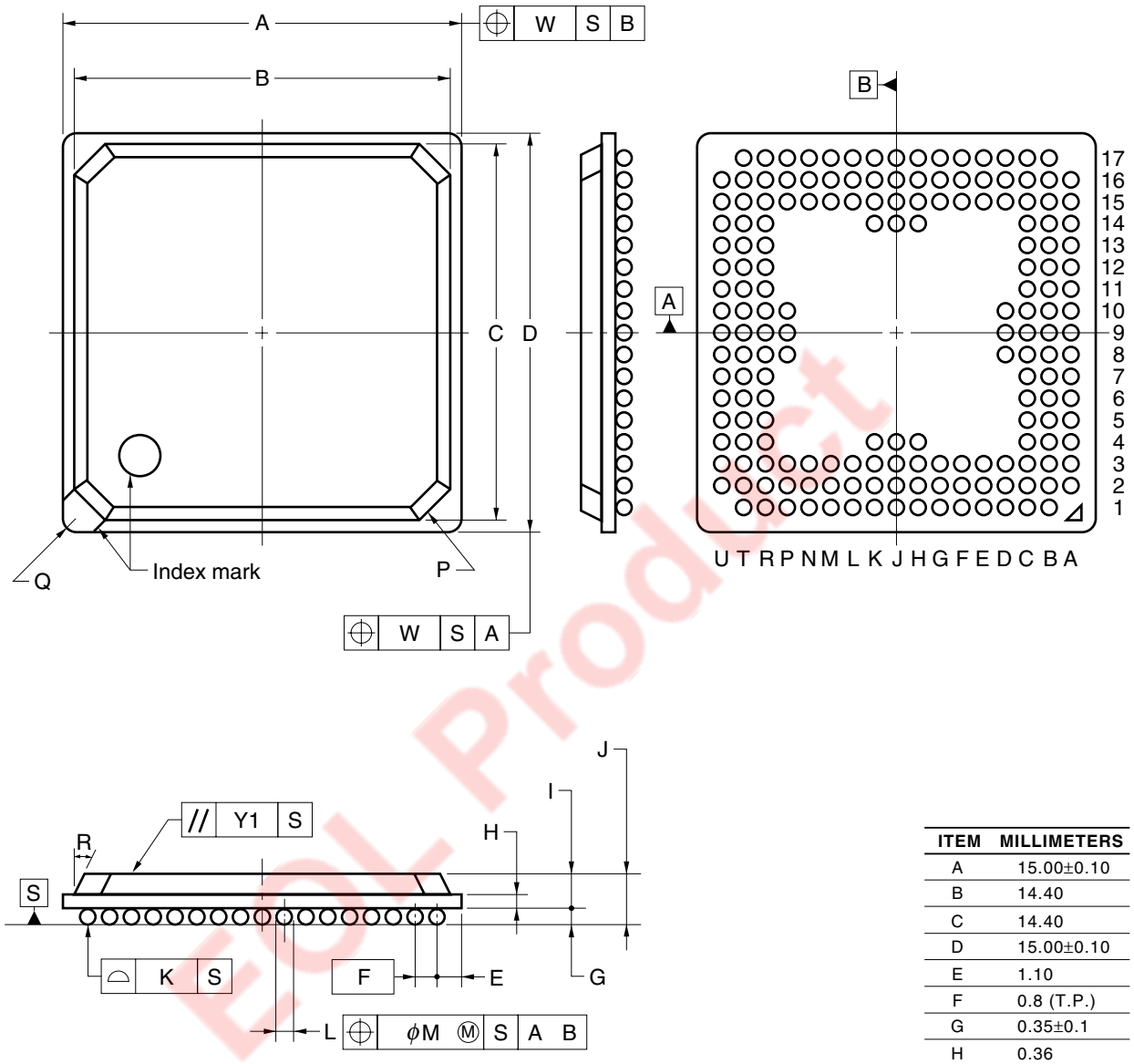

**NOTE**

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 26.0±0.2 |
| B | 24.0±0.2 |
| C | 24.0±0.2 |
| D | 26.0±0.2 |
| F | 2.25 |
| G | 2.25 |
| H | $0.22^{+0.05}_{-0.04}$ |
| I | 0.08 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5 |
| M | $0.17^{+0.03}_{-0.07}$ |
| N | 0.08 |
| P | 1.4±0.05 |
| Q | 0.10±0.05 |
| R | $3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$ |
| S | 1.6 MAX. |
| T | 0.25 (T.P.) |
| U | 0.16±0.15 |

P160GM-50-8EY

## 176-PIN PLASTIC FBGA (15x15)




| ITEM | MILLIMETERS |
|---|---|
| A | 15.00±0.10 |
| B | 14.40 |
| C | 14.40 |
| D | 15.00±0.10 |
| E | 1.10 |
| F | 0.8 (T.P.) |
| G | 0.35±0.1 |
| H | 0.36 |
| I | 1.16 |
| J | 1.51±0.15 |
| K | 0.10 |
| L | $\phi 0.50^{+0.05}_{-0.10}$ |
| M | 0.08 |
| P | C1.0 |
| Q | R0.3 |
| R | 25° |
| W | 0.20 |
| Y1 | 0.20 |

S176S1-80-2C-1

## 4. RECOMMENDED SOLDERING CONDITIONS

The μPD720100A should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

**μPD720100AGM-8ED: 160-pin plastic LQFP (Fine pitch) (24 × 24)**

**μPD720100AGM-8EY: 160-pin plastic LQFP (Fine pitch) (24 × 24)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher),<br>Count: Three times or less<br>Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours) | IR35-103-3 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | – |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

★ **μPD720100AGM-8EY-A: 160-pin plastic LQFP (Fine pitch) (24 × 24) Lead-free product**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher),<br>Count: Three times or less<br>Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) | IR60-107-3 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | – |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**μPD720100AS1-2C: 176-pin plastic FBGA (15 × 15)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher),<br>Count: Three times or less<br>Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) | IR35-107-3 |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

★ **μPD720100AS1-2C-A: 176-pin plastic FBGA (15 × 15) Lead-free product**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher),<br>Count: Three times or less<br>Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) | IR60-107-3 |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

## NOTES FOR CMOS DEVICES

### ① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

### ② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

### ③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

### ④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

### ⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

### ⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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