

MOS INTEGRATED CIRCUIT

μPD70F3320

V850ES/DG2

32-Bit Single-Chip Microcontroller

DESCRIPTION

The V850ES/DG2 single chip microcontroller is a member of NEC's V850 32-bit RISC D_Series family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.

The V850ES/DG2 is a 32-bit System in Package (SiP) microcontroller that includes a V850ES CPU core device of the F_Series (V850ES/FF2) and a Meter Controller/Driver (MTRC) in one package.

The V850ES/DG2 offers an excellent combination of general purpose functions, like different serial interfaces, timers and a multi-channel AD converter. The MTRC supports control of up to 4 stepper motors, making the device ideal for automotive dashboard applications.

FEATURE

- 32-bit RISC CPU with Harvard Architecture
- Internal flash memory: 128 KB
- Internal RAM: 6 KB
- CAN Interface: 1 channel (AFCAN)
- Serial Interfaces: 4 channels
 - clocked serial: 2 channels (CSIB)
 - UARTA: 2 channels (LIN compatible)
- Timers: 6 channels
 - 16-bit interval timer: 1 channel (TMM)
 - 16-bit timer/event counter: 2 channels (TMP)
 - 16-bit timer/event counter: 1 channel (TMQ)
 - Watch timer: 1 channel
 - Watchdog timer: 1 channel (WDT2)
- 10-bit resolution A/D Converter: 10 channels
- GPIO: 60 I/O, 8 O
- Power supply voltage range: 4.0 V to 5.5 V
- Frequency range:
 - Main clock: 16 MHz to 20 MHz
 - Crystal sub clock: 32.768 KHz
 - RC sub clock: 40 KHz (typ.)
 - V850ES/FF2 ring osc clock: 200 KHz (typ.)
 - MTRC ring osc clock: 8 MHz (typ.)
- Built-in low power saving mode:
 - HALT, IDLE1/2, STOP, Sub-clock, Sub-IDLE
- Temperature range: -40°C to +85°C
- Package: 100 LQFP, 0.5 mm pin-pitch (14 × 14 mm)

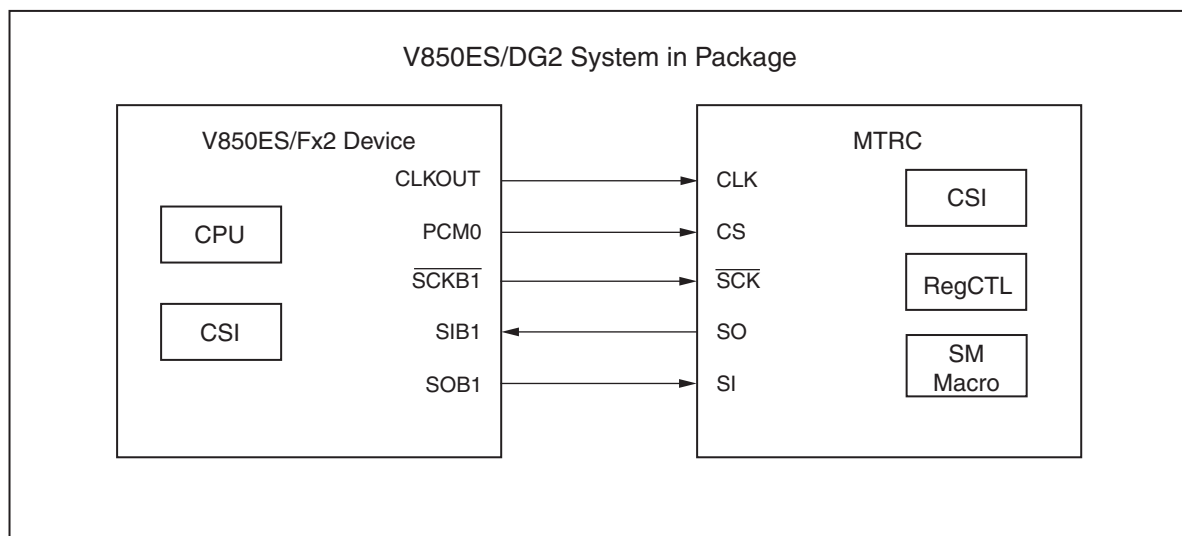
ORDERING INFORMATION

Device	Part Number	Package	Flash	RAM
V850ES/DG2	μPD70F3320GC(A)-8EA	LQFP100 14 × 14 mm	256 KB	12 KB

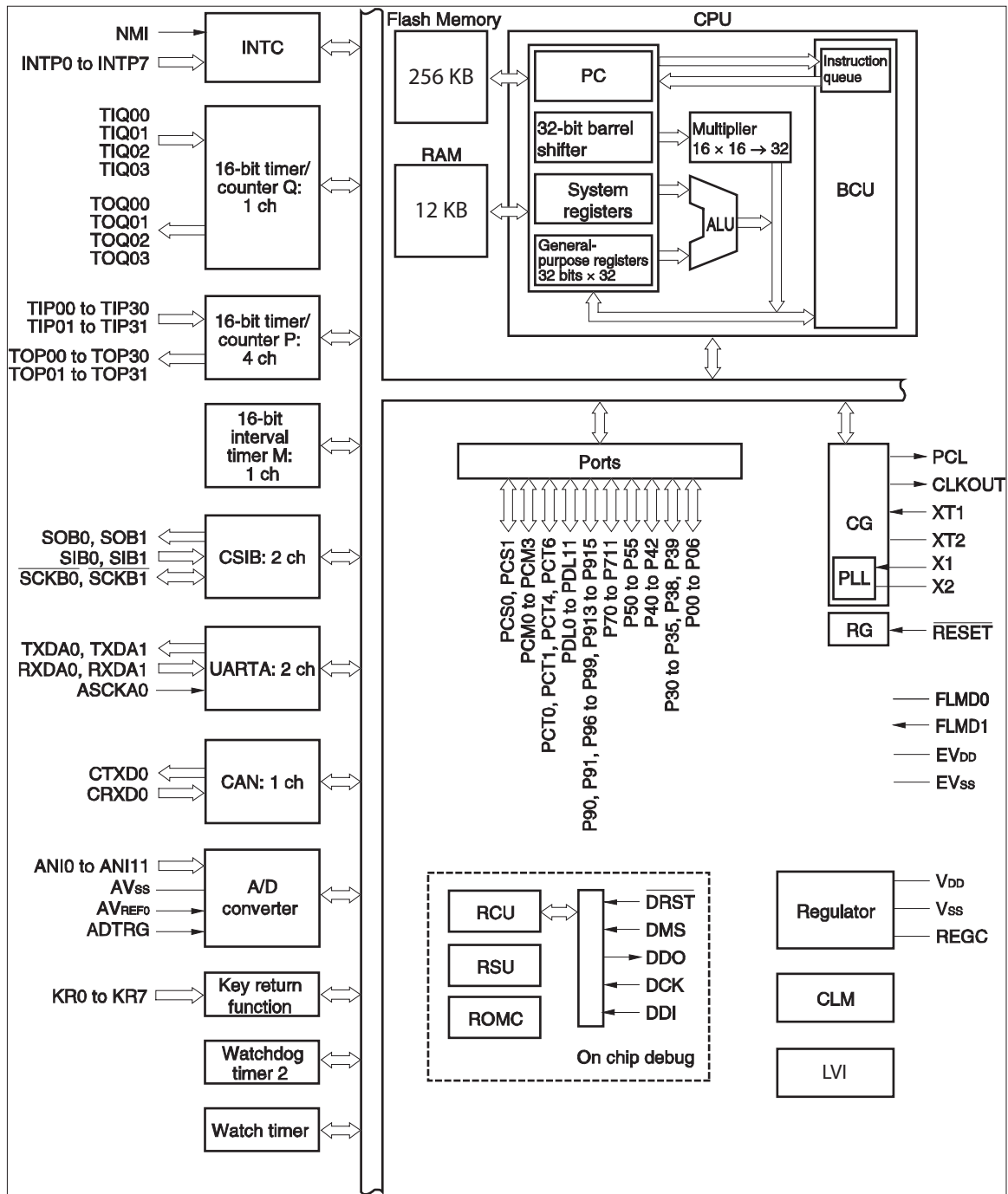
The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

INTERNAL BLOCK DIAGRAM OF V850ES/DG2 - μPD70F3320

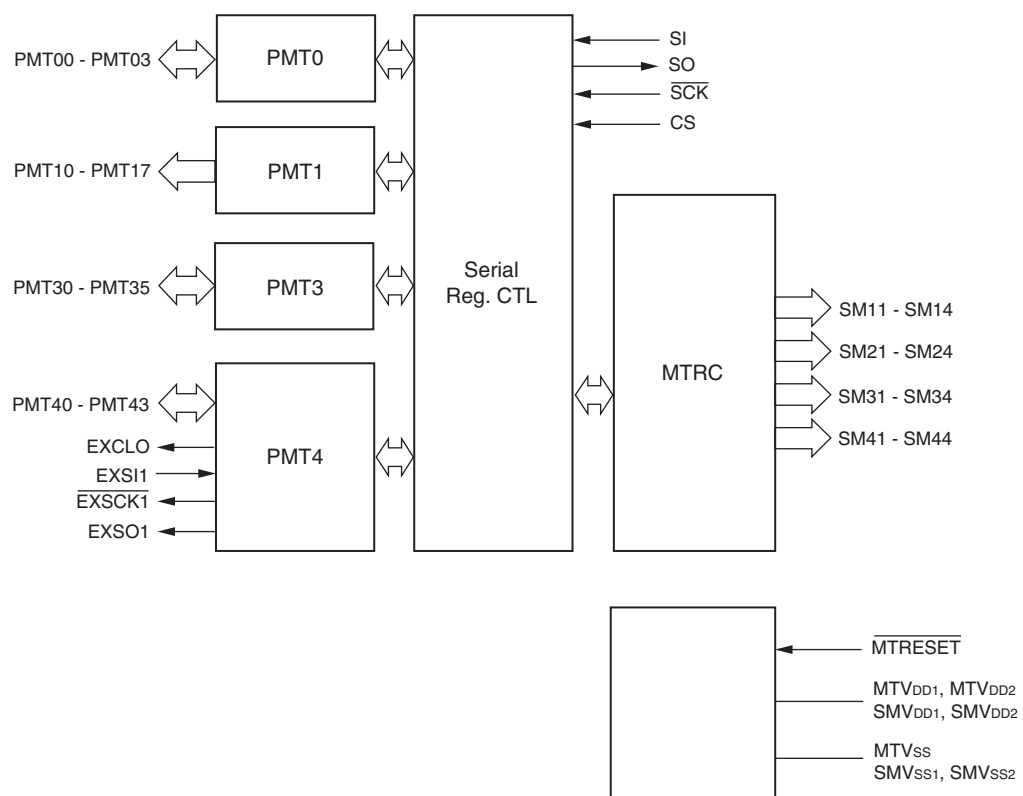


INTERNAL BLOCK DIAGRAM OF V850ES/FF2 - μPD70F3233M1



Note: The CAN macro of this device fulfils the requirements according ISO 11898. Additionally the CAN macro was tested according to the test procedures required by ISO 16845. The CAN macro successfully passed all test patterns. Beyond these test patterns, other tests like robustness tests and processor interface tests as recommended by C&S/FH Wolfenbuettel have successfully been issued.

INTERNAL BLOCK DIAGRAM OF METER CONTROLLER/DRIVER (MTRC)



PIN IDENTIFICATION

ADTRG	A/D trigger input
ANI0 to ANI9	Analog input
ASCKA0	Asynchronous serial clock
AVREF0	Analog reference voltage
AVSS	Analog VSS
CRXD0	Receive data for CAN
CTXD0	Transmit data for CAN
DCK	Debug clock
DDI	Debug data input
DDO	Debug data output
DMS	Debug mode select
$\overline{\text{DRST}}$	Debug reset
EVDD	Power supply for port
EVSS	Power ground for port
EXCLO	Expand pin for system clock
EXSCK1	Expand pin for synchronous serial clock
EXSI1	Expand pin for synchronous serial data in
EXSO1	Expand pin for synchronous serial data out
FLMD0, FLMD1	Flash programming mode
INTP0 to INTP7	Interrupt request from peripherals
KR0 to KR7	Key return
MTCS	MTRC chip select
$\overline{\text{MTRSET}}$	MTRC reset
MTVDD1	Power supply for MTRC ports
MTVDD2	Power supply for MTRC internal circuit
MTVSS	Power ground for MTRC
NMI	Non-maskable interrupt request
P00 to P06	Port 0
P30 to P35	Port 3
P40 to P42	Port 4
P50 to P55	Port 5
P70 to P79	Port 7
P90, P91, P96, P913 to P915	Port 9
PCL	Programmable clock output
PDL0 to PDL7	Port DL
PMT0 to PMT4	Port MT
REGC	Regulator control
$\overline{\text{RESET}}$	Reset

RXDA0 to RXDA1	Receive data for UART
SCKB0	Clock for synchronous serial I/F
SIB0	Input for synchronous serial I/F
SM11 to SM44	Meter PWM outputs
SMVDD1 to SMVDD2	Power supply for Meter outputs
SMVSS1 to SMVSS2	Power ground for Meter outputs
SOB0	Output for synchronous serial I/F
TIP00, TIP01, TIP10, TIP11, TIP21, TIP30, TIP31, TIQ00 to TIQ03	Timer input
TOP00, TOP01, TOP10, TOP11, TOP21, TOP30, TOP31, TOQ01 to TOQ03	Timer output
TXDA0 to TXDA1	Transmit data for UART
VDD	Power supply
VSS	Ground
X1, X2	Crystal for main clock
XT1, XT2	Crystal for subclock

PIN CONFIGURATION

- 100-Pin Plastic LQFP (fine pitch) (14 mm × 14 mm) (Top View)

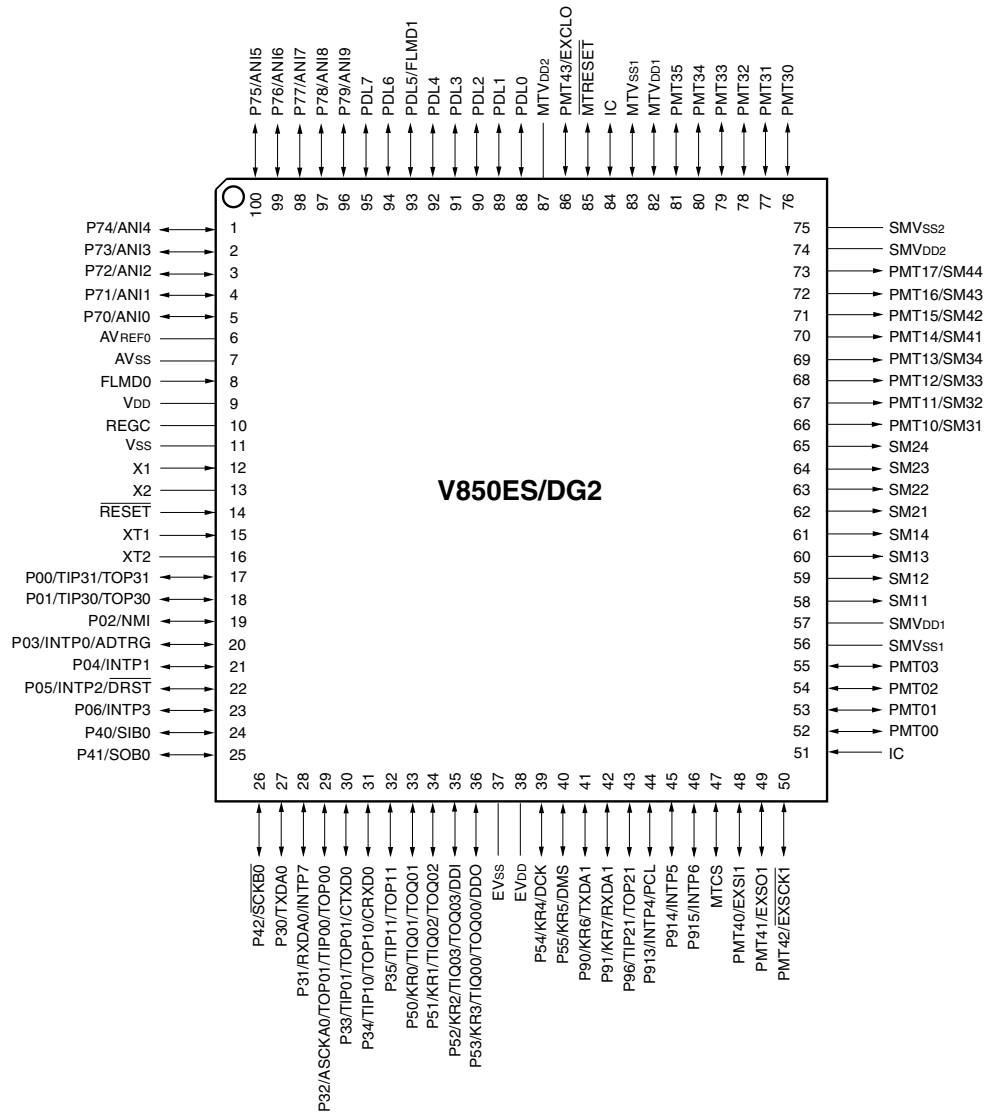


Table of Contents

1. **V850ES/DG2 Pin Functions** 10

 1.1 **Pin Lists** 10

 1.2 **Pin I/O Circuits** 18

2. **Electrical Specification** 22

 2.1 **Absolute Maximum Ratings (T_A = 25°C)** 22

 2.2 **Capacitance** 23

 2.3 **Operation Conditions** 24

 2.4 **Oscillation Circuit** 25

 2.4.1 V850ES/FF2 Main System Clock Oscillation Circuit Characteristics 25

 2.4.2 V850ES/FF2 Sub System Clock Oscillation Circuit Characteristics 26

 2.4.3 MTRC Ring Oscillator Oscillation Circuit Characteristics 27

 2.5 **PLL Characteristics** 27

 2.6 **V850ES/FF2 Ring-OSC Characteristics** 27

 2.7 **Voltage Regulator Characteristics** 28

 2.8 **DC Characteristics** 28

 2.8.1 Input/Output Level 28

 2.8.2 Pin Leak Current 30

 2.8.3 Operation and HALT Mode Supply Current 31

 2.8.4 Power Save Mode Supply Current of V850ES/DG2 (Power Save Modes) 32

 2.8.5 Data Retention Characteristics 33

 2.9 **AC Characteristics** 34

 2.9.1 EXCLO output timing 34

 2.9.2 Reset and interrupt timing 35

 2.9.3 Key Return timing 35

 2.9.4 Timer Input timing 35

 2.9.5 CSI timing 36

 2.9.6 UART timing 37

 2.9.7 CAN timing 37

 2.9.8 AD Converter 38

 2.9.9 LVI 38

 2.9.10 RAM retention flag 38

 2.9.11 Flash Memory Programming characteristics 38

3. **Package Drawings** 40

4. **Recommended Soldering Conditions** 42

5. **Revision History** 44

1. V850ES/DG2 Pin Functions

This section explains the names and functions of the pins of the V850ES/DG2.

Following I/O buffer power supplies are available. The relationship between the power supplies and the pin groups are shown.

Power Supply	Corresponding Pin
AV _{REF0}	Port 7
EV _{DD}	Port 0, Port 3, Port 4, Port 5, Port 9, $\overline{\text{RESET}}$
SMV _{DD1}	Meter1 (SM11 to SM14), Meter2 (SM21 to SM24)
SMV _{DD2}	Port MT1/Meter3 (SM31 to SM34), Meter4 (SM41 to SM44)

1.1 Pin Lists

Table 1-1: V850ES/DG2 Pin List (Port Pins) (1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 7-bit I/O port Input/output can be specified in 1-bit units.	TIP31/TOP31
P01			TIP30/TOP30
P02			NMI
P03			INTP0/ADTRG
P04			INTP1
P05			INTP2/ $\overline{\text{DRST}}$
P06			INTP3
P30	I/O	Port 3 6-bit I/O port Input/output can be specified in 1-bit units.	TXDA0
P31			RXDA0/INTP7
P32			ASCKA0/TIP00/TOP00/ TOP01
P33			TIP01/TOP01/CTXD0
P34			TIP10/TOP10/CRXD0
P35			TIP11/TOP11
P40	I/O	Port 4 3-bit I/O port Input/output can be specified in 1-bit units.	SIB0
P41			SOB0
P42			$\overline{\text{SCKB0}}$
P50	I/O	Port 5 6-bit I/O port Input/output can be specified in 1-bit units.	KR0/TIQ01/TOQ01
P51			KR1/TIQ02/TOQ02
P52			KR2/TIQ03/TOQ03/DDI
P53			KR3/TIQ00/TOQ00/DDO
P54			KR4/DCK
P55			KR5/DMS
P70 to P79	I/O	Port 7 10-bit I/O port Input/output can be specified in 1-bit units.	ANI0 to ANI9

Table 1-1: V850ES/DG2 Pin List (Port Pins) (2/2)

Pin Name	I/O	Function	Alternate Function
P90	I/O	Port 6 6-bit I/O port Input/output can be specified in 1-bit units.	KR6/TXDA1
P91			KR7/RXDA1
P96			TIP21/TOP21
P913			INTP4/PCL
P914			INTP5
P915			INTP6
PDL0 to PDL4	I/O	Port DL 8-bit I/O port Input/output can be specified in 1-bit units.	–
PDL5			FLMD1
PDL6 to PDL7			–
PMT00	I/O	Port MT0 4-bit I/O port (MTRC) ^a Input/output can be specified in 1-bit units.	–
PMT01			–
PMT02			–
PMT03			–
PMT10	Output-HighZ	Port MT1 7-bit O port (MTRC) ^a Output/HighZ can be specified in 1-bit units.	SM31
PMT11			SM32
PMT12			SM33
PMT13			SM34
PMT14			SM41
PMT15			SM42
PMT16			SM43
PMT17			SM44
PMT30	I/O	Port MT3 7-bit I/O port (MTRC) ^a Input/output can be specified in 1-bit units.	–
PMT31			–
PMT32			–
PMT33			–
PMT34			–
PMT35			–
PMT40	I/O	Port MT4 4-bit I/O port (MTRC) ^a Input/output can be specified in 1-bit units.	EXS11
PMT41			EXSO1
PMT42			EXSCK1
PMT43			EXCLO

a. These ports are controlled by the MTRC. The setting can be accessed only via the CSIB1 communication from the V850ES/Fx2 to the MTRC. Thus setting of these ports need more time than a direct access to a V850ES/Fx2 port (depends on clock generator settings and the application).

Table 1-2: V850ES/DG2 Pin List (Non-Port Pins) (1/3)

Pin Name	I/O	Function	Alternate Function
ADTRG	Input	A/D converter external trigger input	P03/INTP0
ANI0 to ANI9	Input	Analog voltage input to A/D converter	P70 to P79
ASCKA0	Input	Baud rate clock input to UARTA0	P32/TIP00/TOP00/TOP01
AV _{REF0}	-	Power supply of A/D converter reference voltage and inputs	-
AV _{SS}		Power ground of A/D converter reference voltage and inputs	
CRXD0	Input	CAN receive data input (CAN0)	P34/TIP10/TOP10
CTXD0	Output	CAN transmit data output (CAN0)	P33/TIP01/TOP01
DCK	Input	Debug clock input	P54/KR4
DDI	Input	Debug data input	P52/KR2/TIQ03/TOQ03
DDO	Output	Debug data output	P53/KR3/TIQ00/TOQ00
DMS	Input	Debug mode select	P55/KR5
DRST	Input	Debug reset input	P05/INTP2
EVDD	-	Power supply for V850ES/Fx2 ports	-
EVSS		Power ground for V850ES/Fx2 ports	
EXCLO	Output	Expand Pin for System Clock	PMT43
EXSCK1	Output	Expand Pin for SCK	PMT42
EXSI1	Input	Expand Pin for SI	PMT40
EXSO1	Output	Expand Pin for SO	PMT41
FLMD0	Input	Flash programming mode setting pins	-
FLMD1			PDL5
INTP0	Input	External interrupt request input (maskable, with analog noise eliminated)	P03/ADTRG
INTP1			P04
INTP2			P05/DRST
INTP3			P06
INTP4			P913/PCL
INTP5			P914
INTP6			P915
INTP7			P31/RXDA0
KR0	Input	Key interrupt input	P50/TIQ01/TOQ01
KR1			P51/TIQ02/TOQ02
KR2			P52/TIQ03/TOQ03/DDI
KR3			P53/TIQ00/TOQ00/DDO
KR4			P54/DCK
KR5			P55/DMS
KR6			P90/TXDA1
KR7			P91/RXDA1
MTCS ^a	Output	MTRC chip select	-
MTRESET	Input	Reset Input (MTRC)	-

Table 1-2: V850ES/DG2 Pin List (Non-Port Pins) (2/3)

Pin Name	I/O	Function	Alternate Function
MTV _{DD1}	-	Power supply for MTRC ports	-
MTV _{DD2}		Power supply for MTRC internal circuit	-
MTV _{SS}		Power ground for MTRC	-
NMI	Input	Non-maskable interrupt	P02
PCL	Output	Programmable clock output	P913/INTP4
REGC	-	Regulator output stabilizing capacitor connection	-
RESET	Input	System reset input	-
RXDA0	Input	Serial receive data input (UARTA0)	P31/INTP7
RXDA1		Serial receive data input (UARTA1)	P91/KR7
SCKB0	I/O	Serial clock I/O (CSIB0)	P42
SIB0	Input	Serial receive data input (CSIB0)	P40
SM11	Output-HighZ	Meter1 PWM Output Signal (sin+)	-
SM12		Meter1 PWM Output Signal (sin-)	
SM13		Meter1 PWM Output Signal (cos+)	
SM14		Meter1 PWM Output Signal (cos-)	
SM21		Meter2 PWM Output Signal (sin+)	
SM22		Meter2 PWM Output Signal (sin-)	
SM23		Meter2 PWM Output Signal (cos+)	
SM24		Meter2 PWM Output Signal (cos-)	
SM31	Output	Meter3 PWM Output Signal (sin+)	PMT10
SM32		Meter3 PWM Output Signal (sin-)	PMT11
SM33		Meter3 PWM Output Signal (cos+)	PMT12
SM34		Meter3 PWM Output Signal (cos-)	PMT13
SM41		Meter4 PWM Output Signal (sin+)	PMT14
SM42		Meter4 PWM Output Signal (sin-)	PMT15
SM43		Meter4 PWM Output Signal (cos+)	PMT16
SM44		Meter4 PWM Output Signal (cos-)	PMT17
SMV _{DD1}	-	Power supply for Meter1, Meter2	-
SMV _{DD2}		Power supply for Meter3, Meter4	
SMV _{SS1}		Power ground for Meter1, Meter2	
SMV _{SS2}		Power ground for Meter3, Meter4	
SOB0	Output	Serial transmit data output (CSIB0)	P41
TIP00	Input	External event/clock input (TMP00)	P32/ASCKA0/TOP00/TOP01
TIP01		External event/clock input (TMP01)	P33/TOP01/CTXD0
TIP10		External event/clock input (TMP10)	P34/TOP10/CRXD0
TIP11		External event/clock input (TMP11)	P35/TOP11
TIP21		External event/clock input (TMP21)	P96/TOP21
TIP30		External event/clock input (TMP30)	P01/TOP30
TIP31		External event/clock input (TMP31)	P00/TOP31

Table 1-2: V850ES/DG2 Pin List (Non-Port Pins) (3/3)

Pin Name	I/O	Function	Alternate Function
TIQ00	Input	External event/clock input (TMQ00)	P53/KR3/TOQ00/DDO
TIQ01		External event input (TMQ01)	P50/KR0/TOQ01
TIQ02		External event input (TMQ02)	P51/KR1/TOQ02
TIQ03		External event input (TMQ03)	P52/KR2/TOQ03/DDI
TOP00	Output	Timer output (TMP00)	P32/ASCKA0/TIP00/TOP01
TOP01		Timer output (TMP01)	P33/TIP01/CTXD0
TOP10		Timer output (TMP10)	P34/TIP10/CRXD0
TOP11		Timer output (TMP11)	P35/TIP11
TOP21		Timer output (TMP21)	P96/TIP21
TOP30		Timer output (TMP30)	P01/TIP30
TOP31		Timer output (TMP31)	P00/TIP31
TOQ00		Output	Timer output (TMQ00)
TOQ01	Timer output (TMQ01)		P50/KR0/TIQ01
TOQ02	Timer output (TMQ02)		P51/KR1/TIQ02
TOQ03	Timer output (TMQ03)		P52/KR2/TIQ03/DDI
TXDA0	Output	Serial transmit data output (UARTA0)	P30
TXDA1		Serial transmit data output (UARTA1)	P90/KR6
V _{DD}	-	Power supply for V850ES/Fx2 internal circuitry	-
V _{SS}		Power ground for V850ES/Fx2 internal circuitry	
X1	Input	Main clock resonator connection	-
X2	-		-
XT1	Input	Subclock resonator connection	-
XT2	-		-

- a. MTCS is connected to the V850ES/FF2's PCM0 pin. PCM0 has to operate in port output mode. MTCS has a pull down resistor to avoid noise effects that could cause malfunction during the initialization of the V850ES/Fx2 device. After $\overline{\text{MTRESET}}$ release, the resistor is active. The resistor will be deactivated after the first rising edge of the MTCS signal. It will be reactivated if $\overline{\text{MTRESET}} = 0$. Therefore this resistor consume some current when it is activated.

Table 1-3: Pin I/O circuit types and recommended connection of unused pins (1/3)

Pin	I/O Circuit Type	Recommended Connection
P00/TIP31/TOP31	5-W	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
P01/TIP30/TOP30		
P02/NMI		
P03/INTP0/ADTRG		
P04/INTP1		
P05/INTP2/ \overline{DRST}	5-AF	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
P06/INTP3	5-W	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
P30/TXDA0	5-A	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
P31/RXDA0/INTP7	5-W	
P32/ASCKA0/TIP00/TOP00/ TOP01		
P33/TIP01/TOP01/CTXD0		
P34/TIP10/TOP10/CRXD0		
P35/TIP11/TOP11		
P40/SIB0	5-W	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
P41/SOB0	5-A	
P42/SCKB0	5-W	
P50/KR0/TIQ01/TOQ01	5-W	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
P51/KR1/TIQ02/TOQ02		
P52/KR2/TIQ03/TOQ03/DDI		
P53/KR3/TIQ00/TOQ00/DDO		
P54/KR4/DCK		
P55/KR5/DMS		
P70/ANI0 to P79/ANI9	11-G	Input: Independently connect to AV _{REF0} or AV _{SS} via a resistor Output: Leave open
P90/KR6/TXDA1	5-W	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
P91/KR7/RXDA1		
P96/TIP21/TOP21		
P913/INTP4/PCL		
P914/INTP5		
P915/INTP6		
PDL0 to PDL4	5	Input: Independently connect to EV _{DD} or EV _{SS} via a resistor Output: Leave open
PDL5/FLMD1		
PDL6 to PDL7		

Table 1-3: Pin I/O circuit types and recommended connection of unused pins (2/3)

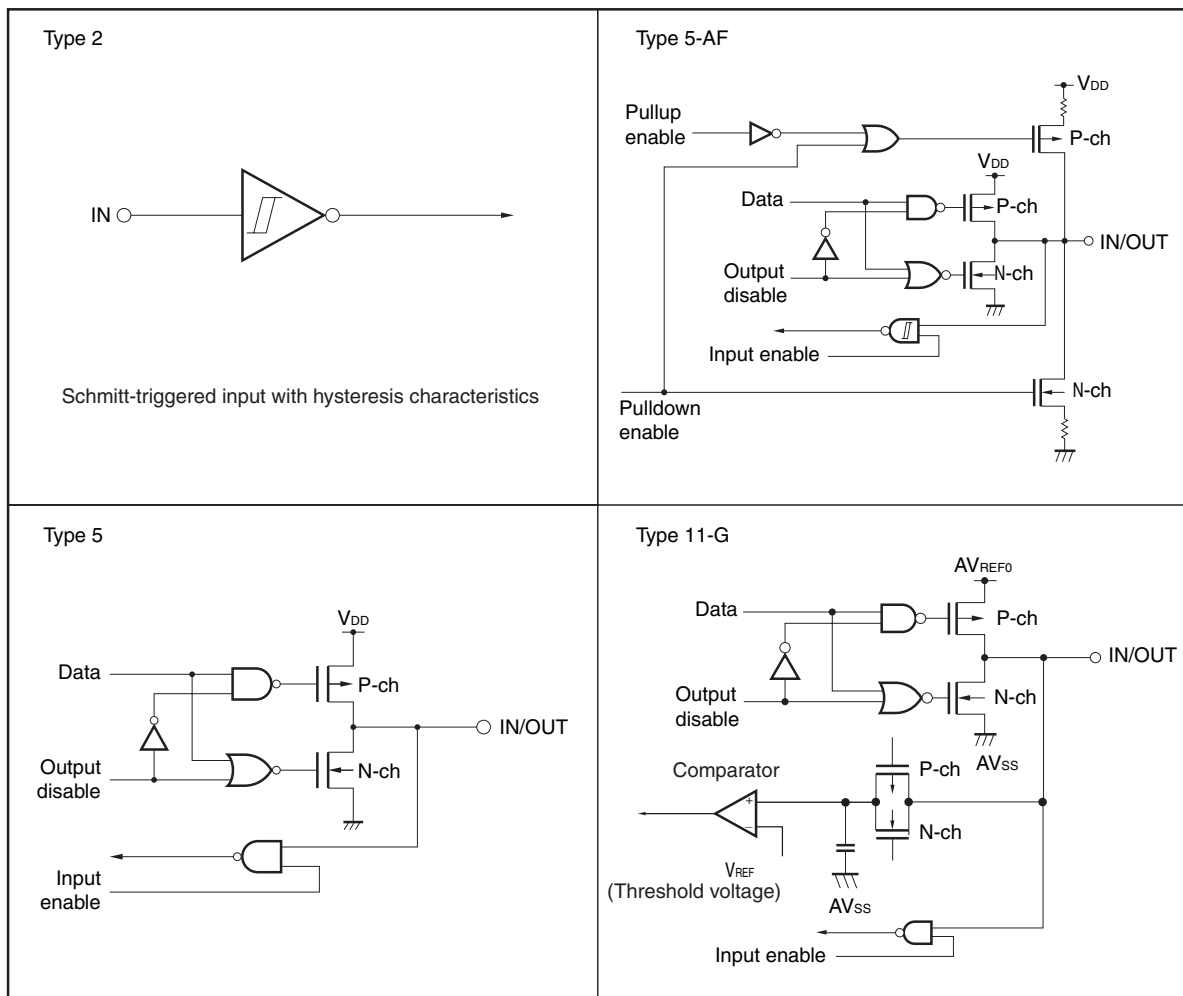
Pin	I/O Circuit Type	Recommended Connection	
PMT00	A-1	Input: Independently connect to MTV _{DD} or MTV _{SS} via a resistor Output: Leave open	
PMT01			
PMT02			
PMT03			
PMT10/SM31	B-2	Leave open	
PMT11/SM32			
PMT12/SM33			
PMT13/SM34			
PMT14/SM41			
PMT15/SM42			
PMT16/SM43			
PMT17/SM44			
PMT30	A-1	Input: Independently connect to MTV _{DD} or MTV _{SS} via a resistor Output: Leave open	
PMT31			
PMT32			
PMT33			
PMT40/EXSI1	D-2		
PMT41/EXSO1	D-1		
PMT42/ $\overline{\text{EXSCK1}}$	D-3		
PMT43/EXCLO	D-4		
SM11	B-1		Leave open
SM12			
SM13			
SM14			
SM21			
SM22			
SM23			
SM24			

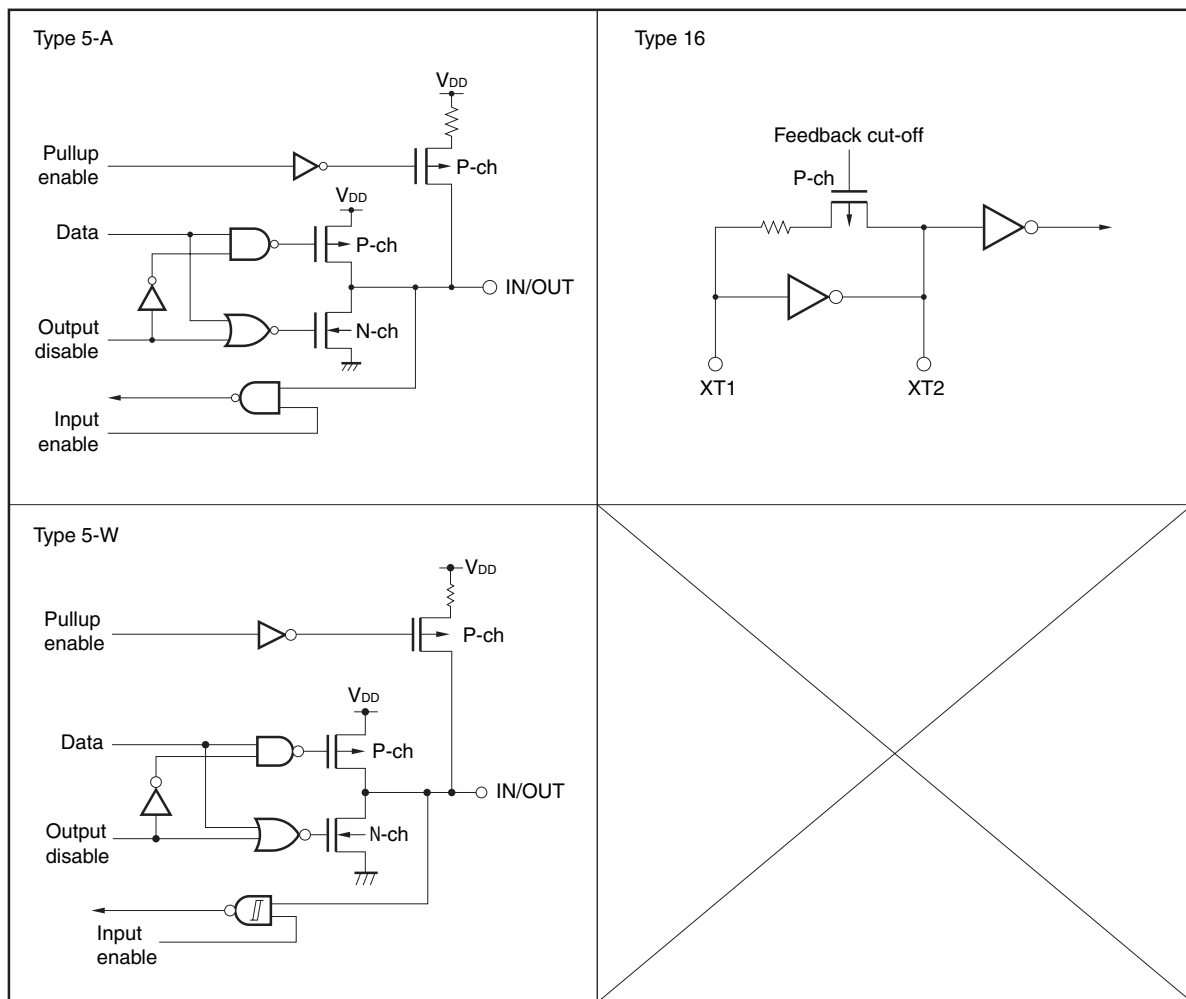
Table 1-3: Pin I/O circuit types and recommended connection of unused pins (3/3)

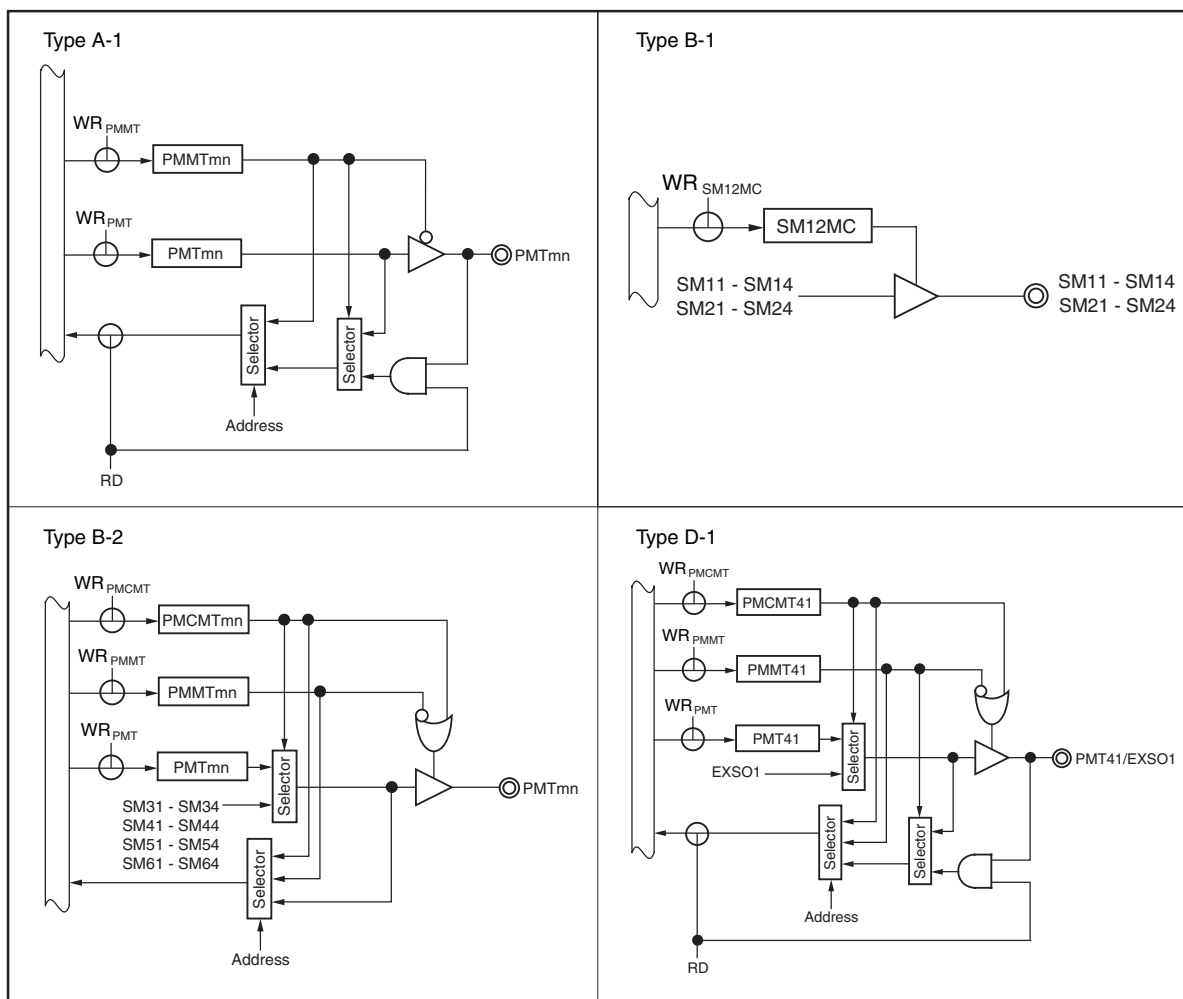
Pin	I/O Circuit Type	Recommended Connection
AV _{REF0}	–	Directly connect to V _{DD}
AV _{SS}	–	–
FLMD0 ^a	–	Directly connect to V _{SS}
REGC	–	–
RESET	2	–
MTCS ^b	5	Leave open
MTRESET	–	–
X1	–	–
X2	–	–
XT1	16	Connect to V _{SS} via a resistor
XT2	16	Leave open
V _{DD}	–	–
V _{SS}	–	–
EV _{DD}	–	–
EV _{SS}	–	–
MTV _{SS}	–	–
MTV _{DD}	–	–
SMV _{DD1}	–	–
SMV _{SS1}	–	–
SMV _{DD2}	–	–
SMV _{SS2}	–	–
IC1, IC2	–	Input: connect to MTV _{SS} directly

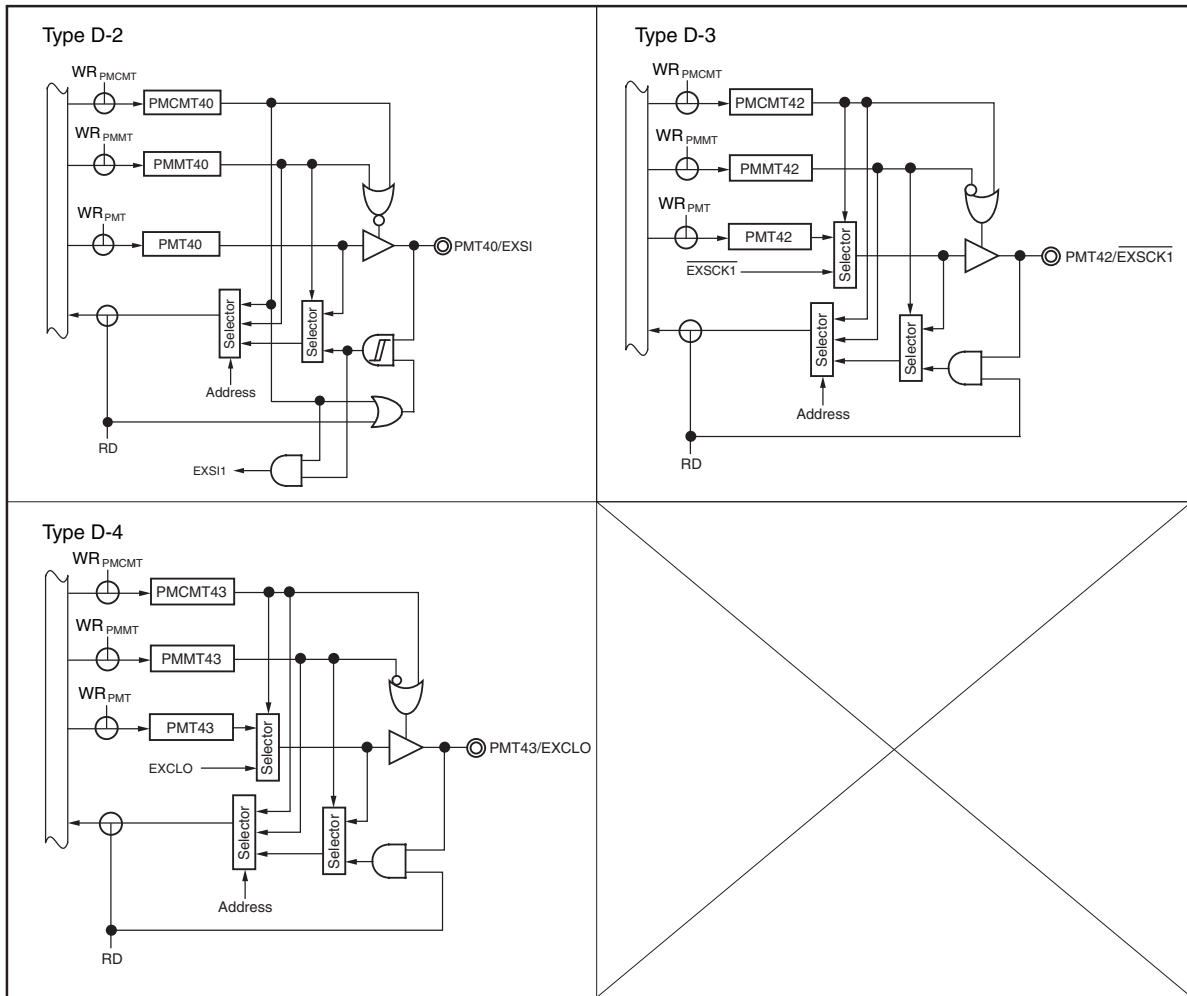
- a. If noise that exceeds the noise elimination width is input to the RESET pin during self programming, the flash on-board mode may be entered depending on the capacitance charge end timing when a capacitor is connected to the FLMD0 pin. Therefore, do not connect a capacitor to the FLMD0 pin.
- b. MTCS is connected to the V850ES/FF2's PCM0 pin. PCM0 has to operate in port output mode. MTCS has a pull down resistor to avoid noise effects that could cause malfunction during the initialization of the V850ES/Fx2 device. After MTRESET release, the resistor is active. The resistor will be deactivated after the first rising edge of the MTCS signal. It will be reactivated if MTRESET = 0. Therefore this resistor consume some current when it is activated.

1.2 Pin I/O Circuits









2. Electrical Specification

2.1 Absolute Maximum Ratings (T_A = 25°C)

Table 2-1: Absolute Maximum Ratings (1/2)

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	V _{DD}	V _{DD} =EV _{DD} =AV _{REF0}	-0.3 to +6.5	V	
	EV _{DD}	V _{DD} =EV _{DD} =AV _{REF0}	-0.3 to +6.5	V	
	MTV _{DD}	MTV _{DD} =SMV _{DD}	-0.3 to +6.5	V	
	SMV _{DD}	MTV _{DD} =SMV _{DD}	-0.3 to +6.5	V	
	AV _{REF0}	V _{DD} =EV _{DD} =AV _{REF0}	-0.3 to +0.3	V	
	V _{SS}	V _{SS} =EV _{SS} =AV _{SS}	-0.3 to +0.3	V	
	EV _{SS}	V _{SS} =EV _{SS} =AV _{SS}	-0.3 to +0.3	V	
	MTV _{SS}	MTV _{SS} =SMV _{SS}	-0.3 to +0.3	V	
	SMV _{SS}	MTV _{SS} =SMV _{SS}	-0.3 to +0.3	V	
	AV _{SS}	V _{SS} =EV _{SS} =AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{I1}	P00-P06, P10-P11, P30-P35, P40-P42, P50-P55, P90, P91, P96, P913-P915, PDL0-PDL7, RESET, FLMD0	-0.3 to EV _{DD} +0.3 ^a	V	
	V _{I3}	X1, X2, XT1, XT2	-0.3 to V _{RO} ^b +0.3 ^a	V	
	V _{I4}	PMT00-PMT03, PMT30-PMT35, PMT40-PMT43, MTRESET	-0.3 to MTV _{DD} +0.3 ^a	V	
	V _{I5}	PMT10-PMT17	-0.3 to SMV _{DD} +0.3 ^a	V	
Analog input voltage	V _{IAN}	P70-P79	-0.3 to AV _{REF0} +0.3 ^a	V	
High level output current	I _{OH}	P00-P06, P30-P35, P40-P42, P50-P55, P90, P91, P96, P913-P915, PDL0-PDL7, MTCS	1 pin	-4	mA
			Total	-50	mA
		P70-79	1 pin	-4	mA
			Total	-20	mA
		PMT10-PMT17	1 pin	-45	mA
			Total	-135	mA
		SM11-SM14, SM21-SM24	1 pin	-45	mA
			Total	-135	mA
		PMT00-PMT03, PMT30-PMT35, PMT40-PMT43	1 pin	-4	mA
			Total	-15	mA

Table 2-1: Absolute Maximum Ratings (2/2)

Parameter	Symbol	Conditions	Ratings	Unit		
Low level output current	I _{OL}	P00-P06, P30-P35, P40-P42, P50-P55, P90, P91, P96, P913-P915, PDL0-PDL7, MTCS	1 pin	4	mA	
			Total	50	mA	
		P70-79	1 pin	4	mA	
			Total	20	mA	
		PMT10-PMT17	1 pin	45	mA	
			Total	135	mA	
		SM11-SM14, SM21-SM24	1 pin	45	mA	
			Total	135	mA	
		PMT00-PMT03, PMT30-PMT35, PMT40-PMT43	1 pin	4	mA	
			Total	30	mA	
		Operating ambient temperature	T _A	Normal operating mode	-40 to +85	°C
				Flash programming mode	-40 to +85	
Storage temperature	T _{STG}		-40 to +125			

- a. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.
- b. V_{RO} is the on-chip regulator output voltage (typ. 2.5 V).

2.2 Capacitance

(T_A=25°C,

V_{DD}=EV_{DD}=AV_{REF0}=MTV_{DD}=SMV_{DD}=V_{SS}=EV_{SS}=AV_{SS}=MTV_{SS}=SMV_{SS}=0 V)

Table 2-2: Capacitance

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _I	f=1 MHz, Other than unmeasured pins:0 V			15	pF
Input / Output capacitance	C _{IO}	f=1 MHz, Other than unmeasured pins:0 V			15	pF
Output capacitance	C _O	f=1 MHz, Other than unmeasured pins:0 V Other than following pins			15	pF
	C _{SMO}	f=1 MHz, Other than unmeasured pins:0 V PMT10-PMT17, SM11-SM14, SM21-SM24			40	pF

2.3 Operation Conditions

($V_{DD}=E_{V_{DD}}=M_{TV_{DD}}=S_{MV_{DD}}=A_{V_{REF0}}=4.0$ to 5.5 V,
 $V_{SS}=E_{V_{SS}}=M_{TV_{SS}}=S_{MV_{SS}}=A_{V_{SS}}=0$ V,
 $T_A=-40$ to $+85^{\circ}\text{C}$)

Table 2-3: Operation Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	$V_{DD}=5$ V \pm 10% PLL mode (OSC=4 MHz to 5 MHz)	16		20	MHz
		$V_{DD} = 4.0$ to 5.5 V PLL mode (OSC=4 MHz)	16	16	16	MHz
		$V_{DD}= 4.0$ to 5.5 V Through-rate mode (OSC=4 MHz to 5 MHz)	4		5	MHz
		$V_{DD}= 4.0$ to 5.5 V Sub-IDLE mode (Crystal) ^a	32		35	KHz
		$V_{DD}= 4.0$ to 5.5 V Sub-IDLE mode (RC) ^a	12.5 ^b		27.5 ^b	KHz

- a. Be sure not to access peripheral, even if switched sub operation mode one time, before go sub-IDLE mode.
- b. The internal system clock is half of the oscillator frequency.

2.4 Oscillation Circuit

2.4.1 V850ES/FF2 Main System Clock Oscillation Circuit Characteristics

($V_{DD}=E_{VDD}=M_{TVDD}=S_{MVDD}=A_{VREF0}=4.0$ to 5.5 V,
 $V_{SS}=E_{VSS}=M_{TVSS}=S_{MVSS}=A_{VSS}=0$ V,
 $T_A=-40$ to $+85^{\circ}\text{C}$)

Table 2-4: Main System Clock Oscillation Circuit Characteristics

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal/ Ceramic resonator		Oscillation frequency		4		5	MHz
		Oscillation stabilization time ^a	After reset is released		$2^{16}/f_X$		s
			After STOP mode is released	0.5 ^b	c		ms
			After IDLE2 mode is released	350 ^b	c		μs

- a. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 4.0 V) to when the crystal resonator stabilizes.
- b. Stabilization time for Flash macro. Setting by OSTs resistor.
- c. Depend on the setting of the oscillation stabilization time select resistor (OSTs).

Cautions: 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

1. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

2.4.2 V850ES/FF2 Sub System Clock Oscillation Circuit Characteristics

($V_{DD}=E_{V_{DD}}=M_{TV_{DD}}=S_{MV_{DD}}=A_{V_{REF0}}=4.0$ to 5.5 V,
 $V_{SS}=E_{V_{SS}}=M_{TV_{SS}}=S_{MV_{SS}}=A_{V_{SS}}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Table 2-5: Sub System Clock Oscillation Circuit Characteristics

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})		32	32.768	35	KHz
		Oscillation stabilization time ^a				10	μs
RC resonator		Oscillation frequency (f_{XT})	$R = 390\text{ k}\Omega \pm 5\%^b$ $C = 47\text{ pF} \pm 10\%^b$	25	40	55	KHz
		Oscillation stabilization time ^a				100	μs

- a. Time required from when V_{DD} reaches oscillation voltage range (MIN.= 4.0 V) to when the crystal resonator stabilizes.
- b. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

Cautions: 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

1. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

2.4.3 MTRC Ring Oscillator Oscillation Circuit Characteristics

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Table 2-6: Ring Oscillation Circuit Characteristics

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ring Oscillator	Oscillation frequency (f_{XR}) ^a		6.8 ^b	8	9.2	MHz
	Oscillation stabilization time ^c				20	μs
Calibration pulse	Calibration high pulse ^d			14		μs
	Calibration low pulse		3			μs
CS ^e	High-Level width		600			ns
	Low-Level width		600			ns
	Analog delay for noise suppression		71	192		ns

- a. if calibration routine was successfully performed
- b. 4 MHz if uncalibrated
- c. Time required when MRON bit is set from "0" to "1"
- d. has to be exact the typ. value
- e. CS is the internal MTRC input, connected to the V850ES/FF2's PCM0 pin.

2.5 PLL Characteristics

($V_{DD}=EV_{DD}=BV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=BV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		4		5	MHz
Output frequency	f_{xx}		16		20	MHz
Clock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			800	μs

2.6 V850ES/FF2 Ring-OSC Characteristics

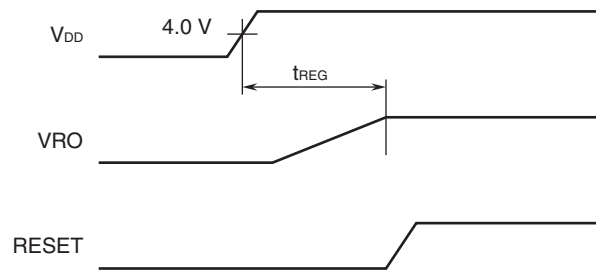
($V_{DD}=EV_{DD}=BV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=BV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_r		100	200	400	KHz

2.7 Voltage Regulator Characteristics

($V_{DD}=EV_{DD}=BV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=BV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{DD}		4.0		5.5	V
Output voltage	V_{RO}			2.5		V
Lock time	t_{REG}	After V_{DD} reaches MIN.: 4.0 V Connect $C = 4.7 \mu F \pm 20\%$ to REGC pin			1	ms



2.8 DC Characteristics

2.8.1 Input/Output Level

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Table 2-7: Input/Output Level (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P30, P34, P41, PDL0-PDL7	$0.7 EV_{DD}$		EV_{DD}	V
	V_{IH2}	P00-P06, P31-P33, P35, P40, P42, P50-P55, P90, P91, P96, P913-P915	$0.8 EV_{DD}$		EV_{DD}	V
	V_{IH4}	P70-P79	$0.7 AV_{REF0}$		AV_{REF0}	V
	V_{IH5}	RESET, FLMD0	$0.8 EV_{DD}$		EV_{DD}	V
	V_{IH6}	PMT40, MTRESET	$0.8 MTV_{DD}$		MTV_{DD}	V
	V_{IH7}	PMT00-PMT03, PMT30-PMT35, PMT41-PMT43	$0.7 MTV_{DD}$		MTV_{DD}	V

Table 2-7: Input/Output Level (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, low	V _{IL1}	P30, P34, P41, PDL0-PDL7	E _{VSS}		0.3 E _{VDD}	V
	V _{IL2}	P00-P06, P31-P33, P35, P40, P42, P50-P55, P90, P91, P96, P913-P915	E _{VSS}		0.2 E _{VDD}	V
	V _{IL4}	P70-P79	A _{VSS}		0.3 A _{REF0}	V
	V _{IL5}	RESE _T , FLMD0	E _{VSS}		0.2 E _{VDD}	V
	V _{IL6}	PMT40, MTRESE _T	M _T V _{SS}		0.2 M _T V _{DD}	V
	V _{IL7}	PMT00-PMT03, PMT30-PMT35, PMT41-PMT43	M _T V _{SS}		0.3 M _T V _{DD}	V
Output voltage, high	V _{OH1} ^a	P00-P06, P30-P35, P40-P42, P50-P55, P90, P91, P96, P913-P915, PDL0-PDL7	I _{OH} =-1.0 mA	E _{VDD} -1.0	E _{VDD}	V
			I _{OH} =-100 μA	E _{VDD} -0.5	E _{VDD}	V
	V _{OH3} ^b	P70-P79	I _{OH} =-1.0 mA	A _{VREF0} -1.0	A _{VREF0}	V
			I _{OH} =-100 μA	A _{VREF0} -0.5	A _{VREF0}	V
	V _{OH4} ^c	PMT10-PMT17, SM11-SM14, SM21-SM24	I _{OH} =-27 mA (T _A =85°C) I _{OH} =-30 mA (T _A =25°C) I _{OH} =-40 mA (T _A =-40°C)	SMV _{DD} -0.7	SMV _{DD} -0.07	V
			I _{OH} =-19 mA (T _A =85°C) I _{OH} =-21 mA (T _A =25°C) I _{OH} =-28 mA (T _A =-40°C)	SMV _{DD} -0.5	SMV _{DD} -0.07	V
V _{OH5} ^d	PMT00-PMT03, PMT30-PMT35, PMT40-PMT43	I _{OH} =-1.0 mA	M _T V _{DD} -1.0	M _T V _{DD}	V	
Output voltage, low	V _{OL1} ^e	P00-P06, P30-P35, P40-P42, P50-P55, P90, P91, P96, P913-P915, PDL0-PDL7	I _{OL} =1.0 mA	0	0.4	V
	V _{OL3} ^f					
	V _{OL4} ^g	PMT10-PMT17, SM11-SM14, SM21-SM24	I _{OL} =27 mA (T _A =85°C) I _{OL} =30 mA (T _A =25°C) I _{OL} =40 mA (T _A =-40°C)	0.07	0.7	V
			I _{OH} =19 mA (T _A =85°C) I _{OH} =21 mA (T _A =25°C) I _{OH} =28 mA (T _A =-40°C)	0.07	0.5	V
	V _{OL5} ^h	PMT00-PMT03, PMT30-PMT35, PMT40-PMT43	I _{OL} =1.0 mA	0	0.4	V
Software pull-up resistor	R1	V _I =0 V	10	30	100	KΩ
Software pull-down resistor ⁱ	R2	V _I =V _{DD}	10	30	100	KΩ

- a. I_{OH} max of V_{OH1} is -20 mA.
- b. I_{OH} max of V_{OH3} is -10 mA.
- c. I_{OH} max of V_{OH4} is -135 mA.
- d. I_{OH} max of V_{OH5} is -14 mA.
- e. I_{OL} max of V_{OL1} is 20 mA.
- f. I_{OL} max of V_{OL3} is 10 mA.
- g. I_{OL} max of V_{OL4} is 135 mA
- h. I_{OL} max of V_{OL5} is 14 mA
- i. Exists only at DRST pin

2.8.2 Pin Leak Current

($V_{DD}=E_{V_{DD}}=M_{TV_{DD}}=S_{MV_{DD}}=A_{V_{REF0}}=4.0$ to 5.5 V,
 $V_{SS}=E_{V_{SS}}=M_{TV_{SS}}=S_{MV_{SS}}=A_{V_{SS}}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Table 2-8: Pin Leak Current

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_I=V_{DD}$	P70-79			0.2	μA
			P00-06, P30-35, P40-42, P50-55, P90,91,96,913-915, PDL0-7, \overline{RESET}			0.5	μA
			PMT00-03, PMT30-35, PMT40-43, $\overline{MTRESET}$			5.0	μA
			FLMD0			2.0	μA
Input leakage current, low	I_{LIL1}	$V_I=0$ V	P70-79			-0.2	μA
			P00-06, P30-35, P40-42, P50-55, P90,91,96,913-915, PDL0-7, \overline{RESET}			-0.5	μA
			PMT00-03, PMT30-35, PMT40-43, $\overline{MTRESET}$			-5.0	μA
			FLMD0			-2.0	μA
Output leakage current, high	I_{LOH1}	$V_O=V_{DD}$	P70-79			0.2	μA
			P00-06, P30-35, P40-42, P50-55, P90,91,96,913-915, PDL0-7			0.5	μA
			PMT00-03, PMT30-35, PMT40-43			5.0	μA
			SM11-14, SM21-24, PMT10-17 (SM31-34, SM41-44), MTCS			5.0	μA
Output leakage current, low	I_{LOL1}	$V_O=0$ V	P70-79			-0.2	μA
			P00-06, P30-35, P40-42, P50-55, P90,91,96,913-915, PDL0-7			-0.5	μA
			PMT00-03, PMT30-35, PMT40-43			-5.0	μA
			SM11-14, SM21-24, PMT10-17 (SM31-34, SM41-44), MTCS			-5.0	μA

2.8.3 Operation and HALT Mode Supply Current

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=4.0$ to 5.5 V
 $AV_{REF0}=4.0$ to 5.5 V
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V
 $T_A=-40$ to $+85^{\circ}C$)

Table 2-9: Power Supply Current

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Supply current ^a	IDD1	Operating mode	$f_{XX}=20$ MHz (OSC=5 MHz) MTRC-Ring Oscillator On		27.5	45	mA
			All peripherals stopped MTRC-Ring Oscillator On		20		mA
	IDD2	HALT mode	$f_{XX}=20$ MHz (OSC=5 MHz) MTRC-Ring Oscillator On		16.5	29	mA
			All peripherals stopped MTRC-Ring Oscillator On		9		mA

a. V_{DD} , EV_{DD} , and MTV_{DD} total current. AV_{REF0} and SMV_{DD} current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistors) are not included.

2.8.4 Power Save Mode Supply Current of V850ES/DG2 (Power Save Modes)

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=4.0$ to 5.5 V

$AV_{REF0}=4.0$ to 5.5 V

$V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V

$T_A=-40$ to $+85^{\circ}C$)

Table 2-10: Power Supply Current

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current ^a	IDD3	IDLE1 mode	$f_{XX}=5$ MHz (OSC=5 MHz) PLL Off MTRC-Ring Oscillator Off		0.6	0.92	mA
	IDD4	IDLE2 mode	$f_{XX}=5$ MHz (OSC=5 MHz) PLL Off MTRC-Ring Oscillator Off		0.25	0.72	mA
	IDD5	Sub Operation mode ^{bd}	Crystal resonator $f_{XT}=32.768$ KHz RC resonator ^c $f_{XT}=40$ KHz MTRC-Ring Oscillator Off		200	420	μA
	IDD6	Sub IDLE mode ^{bd}	Crystal resonator $f_{XT}=32.768$ KHz MTRC-Ring Oscillator Off		20	140	μA
			RC resonator ^c $f_{XT}=40$ KHz MTRC-Ring Oscillator Off		35	160	μA
	IDD7	STOP mode ^{be}	V850ES/FF2 Ring Oscillator On MTRC-Ring Oscillator Off		15	85	μA
			V850ES/FF2 Ring Oscillator Off MTRC-Ring Oscillator Off		7	70	μA

- a. V_{DD} , EV_{DD} , and MTV_{DD} total current. AV_{REF0} and SMV_{DD} current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.
- b. V850ES/FF2 Main Oscillator is Off.
- c. V850ES/FF2 RC Oscillator frequency is typ. 40 KHz. This clock is divided (1/2) internally.
- d. V850ES/FF2 Ring Oscillator is On.
- e. V850ES/FF2 Sub Oscillator is not used.

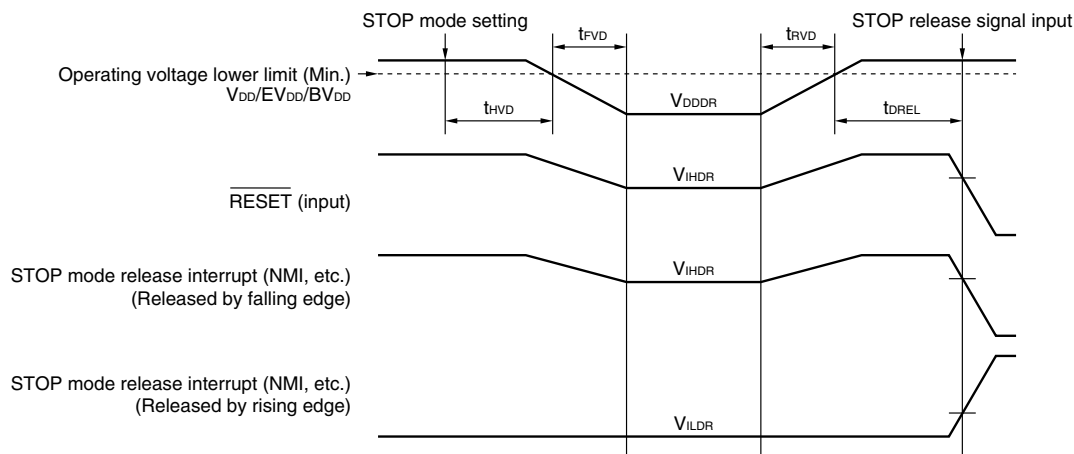
2.8.5 Data Retention Characteristics

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=1.9$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$)

Table 2-11: Data Retention Characteristics

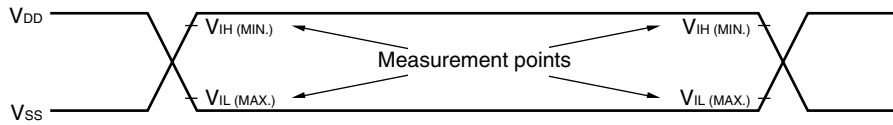
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	In STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	$V_{DDDR} = 2.0$ V		6	65	μA
Supply voltage rise time	t_{RVD}		1			μs
Supply voltage fall time	t_{FVD}		1			μs
Supply voltage retention time	t_{HVD}	After STOP mode release	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches MIN.: 3.5 V	0			μs
Data retention input voltage, high	V_{IHDR}	All input ports	$0.9V_{DDDR}$		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	All input ports	0		$0.1V_{DDDR}$	V

Caution: Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

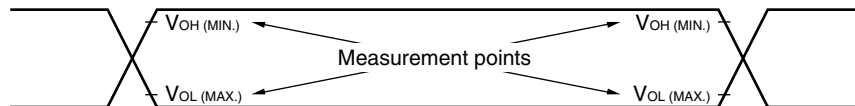


2.9 AC Characteristics

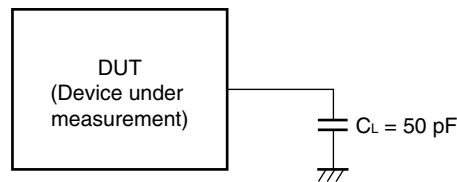
AC Test Input Measurement Points (V_{DD} , AV_{DD} , EV_{DD} , BV_{DD} , MTV_{DD} , MTV_{DD}),



AC Test Output Measurement Points



Load Conditions



Caution: If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

2.9.1 EXCLO output timing

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^\circ\text{C}$, $C_L=50$ pF)

Table 2-12: EXCLO Output Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}		62.5	8000	ns
High level width	t_{WKH}		$t_{CYK}/2-25$		ns
Low level width	t_{WKL}		$t_{CYK}/2-25$		ns
Rising time	t_{KR}			25	ns
Falling time	t_{KF}			25	ns

2.9.2 Reset and interrupt timing

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Table 2-13: Reset and Interrupt Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RESET input low level width	t_{WRSL}		500		ns
MTRESET input low level width	t_{WMRSL}		500		ns
NMI input low level width	t_{WNIL}		500		ns
NMI input high level width	t_{WNIH}		500		ns
INTPn input low level width	t_{WITL}		500		ns
INTPn input high level width	t_{WITH}		500		ns

2.9.3 Key Return timing

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Remark: It is the same specification as V850ES/FF2.

2.9.4 Timer Input timing

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Remark: It is the same specification as V850ES/FF2.

2.9.5 CSI timing

(1) CSI0

(a) Master Mode

($V_{DD}=E_{V_{DD}}=M_{TV_{DD}}=S_{MV_{DD}}=A_{V_{REF0}}=4.0$ to 5.5 V,
 $V_{SS}=E_{V_{SS}}=M_{TV_{SS}}=S_{MV_{SS}}=A_{V_{SS}}=0$ V,
 $T_A=-40$ to $+85^{\circ}\text{C}$, $C_L=50$ pF)

Table 2-14: CSI0 Master Mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKB0}}$ cycle time	t_{KCY0}		125		ns
$\overline{\text{SCKB0}}$ high level width	t_{KH0}		$t_{\text{KCY0}}/2-15$		ns
$\overline{\text{SCKB0}}$ low level width	t_{KL0}		$t_{\text{KCY0}}/2-15$		ns
SIB0 setup time (to $\overline{\text{SCKB0}}$)	t_{SIK0}		30		ns
SIB0 hold time (from $\overline{\text{SCKB0}}$)	t_{KSI0}		25		ns
$\overline{\text{SCKB0}}$ to SOB0 output delay time	t_{KSO0}			25	ns

(b) Slave Mode

($V_{DD}=E_{V_{DD}}=M_{TV_{DD}}=S_{MV_{DD}}=A_{V_{REF0}}=4.0$ to 5.5 V,
 $V_{SS}=E_{V_{SS}}=M_{TV_{SS}}=S_{MV_{SS}}=A_{V_{SS}}=0$ V,
 $T_A=-40$ to $+85^{\circ}\text{C}$, $C_L=50$ pF)

Table 2-15: CSI0 Slave Mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKB0}}$ cycle time	t_{KCY0}		200		ns
$\overline{\text{SCKB0}}$ high level width	t_{KH0}		90		ns
$\overline{\text{SCKB0}}$ low level width	t_{KL0}		90		ns
SIB0 setup time (to $\overline{\text{SCKB0}}$)	t_{SIK0}		50		ns
SIB0 hold time (from $\overline{\text{SCKB0}}$)	t_{KSI0}		50		ns
$\overline{\text{SCKB0}}$ to SOB0 output delay time	t_{KSO0}			50	ns

(2) CSI1

(a) Master Mode

Note: CSI1 can be only used in Master Mode.

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Table 2-16: CSI1 Master Mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{EXSCK1}$ cycle time	t_{KCY1}		250/1000 ^a		ns
$\overline{EXSCK1}$ high level width	t_{KH1}		$t_{KCY1}/2-40$		ns
$\overline{EXSCK1}$ low level width	t_{KL1}		$t_{KCY1}/2-40$		ns
EXS11 setup time (to $\overline{EXSCK1}$)	t_{SIK1}		60		ns
EXS11 hold time (from $\overline{EXSCK1}$)	t_{KSI1}		50		ns
$\overline{EXSCK1}$ to EXSO1 output delay time	t_{KSO1}			50	ns

- a. Be sure to set cycle time ($\overline{EXSCK1}$) over 4 times as the internal system clock cycle ($1/f_{CLK}$). $t_{KCY1} \geq 1/f_{CLK} \times 4$
 If the CSI1 communicate with the uncalibrated MTRC (f_{RO_uncal} min. 4 MHz) t_{KCY1} has to be ≥ 1000 ns.

2.9.6 UART timing

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Remark: It is the same specification as V850ES/FF2.

2.9.7 CAN timing

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Remark: It is the same specification as V850ES/FF2.

2.9.8 AD Converter

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error ^a		$4.0 \leq AV_{REF0} \leq 5.5$ V		±0.15	±0.45	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV_{REF0} current	I_{AREF0}	When using A/D converter		5	10	mA
		When not using A/D converter		1	10	μA

a. Excluding quantization error (±0.05%FSR). Indicates the ratio to the full-scale value (%FSR).

Remark: FSR: Full Scale Range

2.9.9 LVI

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Remark: It is the same specification as V850ES/FF2.

2.9.10 RAM retention flag

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Remark: It is the same specification as V850ES/FF2.

2.9.11 Flash Memory Programming characteristics

($V_{DD}=EV_{DD}=MTV_{DD}=SMV_{DD}=AV_{REF0}=4.0$ to 5.5 V,
 $V_{SS}=EV_{SS}=MTV_{SS}=SMV_{SS}=AV_{SS}=0$ V,
 $T_A=-40$ to $+85^{\circ}C$, $C_L=50$ pF)

Table 2-17: Flash Memory Programming Characteristics

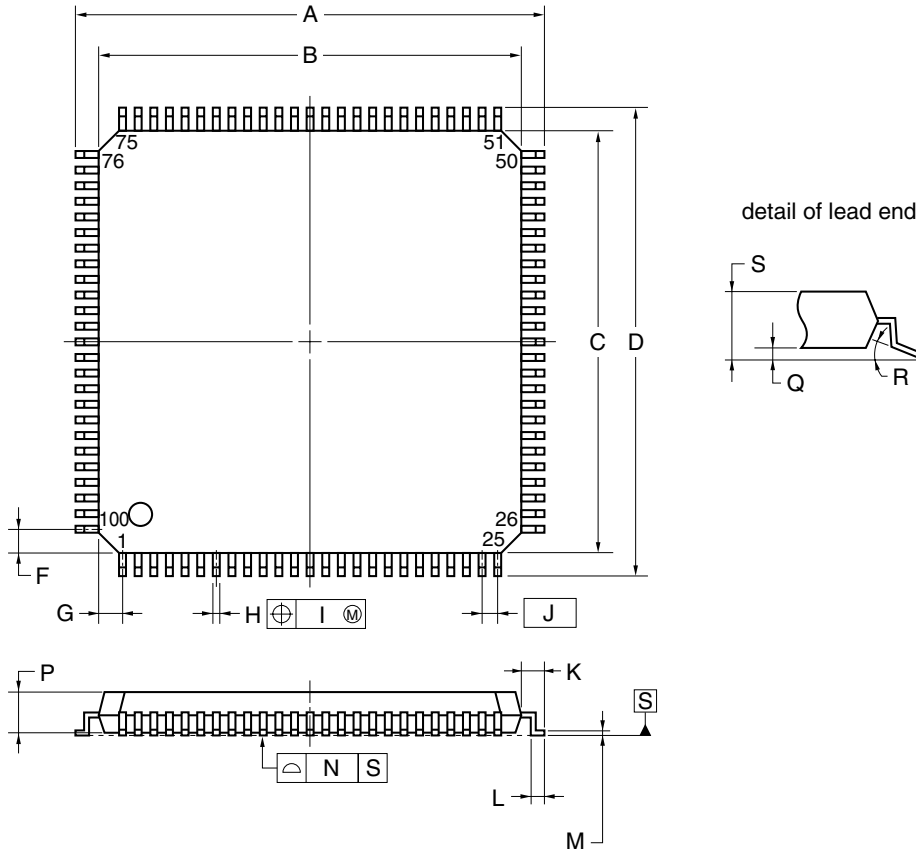
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Supply voltage	V_{DD}		4.0	5.5	V

Remark: It is the same specification as V850ES/FF2

3. Package Drawings

Figure 3-1: V850ES/DG2

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	0.22 ^{+0.05} _{0.04}
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.17 ^{+0.03} _{0.07}
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3° ^{+7°} _{3°}
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

[MEMO]

4. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
 For details of the recommended soldering conditions, refer to information document Semiconductor Device:

Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended please consult NEC.

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235°C	IR35-207-3
Partial heating	350°C	P350

Caution: Do not use two or more soldering methods in combination (except partial heating method).

[MEMO]

5. Revision History

Version	Date	Remarks
2.0	2006/08/01	Initial release
2.1	2006/12/13	chapter 2.8.4: IDD3 condition corrected: PLL Off
		ordering information: part number corrected

[MEMO]

Notes for CMOS Devices

1. Precaution against ESD for semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. Handling of unused input pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. Status before initialization of MOS devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Legal Notes

- The information in this document is current as of December 2006. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such NEC Electronics products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".

The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

"Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact NEC Electronics sales representative in advance to determine NEC Electronics 's willingness to support a given application.

- Notes:**
1. "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
 2. "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).
 3. SuperFlash[®] is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan. This product uses SuperFlash[®] technology licensed from Silicon Storage Technology, Inc.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)

Santa Clara, California

Tel: 408-588-6000

800-366-9782

Fax: 408-588-6130

800-729-9288

NEC Electronics (Europe) GmbH

Duesseldorf, Germany

Tel: 0211-65 03 01

Fax: 0211-65 03 327

Sucursal en España

Madrid, Spain

Tel: 091- 504 27 87

Fax: 091- 504 28 60

Succursale Française

Vélizy-Villacoublay, France

Tel: 01-30-67 58 00

Fax: 01-30-67 58 99

Filiale Italiana

Milano, Italy

Tel: 02-66 75 41

Fax: 02-66 75 42 99

Branch The Netherlands

Eindhoven, The Netherlands

Tel: 040-244 58 45

Fax: 040-244 45 80

Branch Sweden

Taeby, Sweden

Tel: 08-63 80 820

Fax: 08-63 80 388

United Kingdom Branch

Milton Keynes, UK

Tel: 01908-691-133

Fax: 01908-670-290

NEC Electronics Hong Kong Ltd.

Hong Kong

Tel: 2886-9318

Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch

Seoul, Korea

Tel: 02-528-0303

Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

Singapore

Tel: 65-6253-8311

Fax: 65-6250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan

Tel: 02-2719-2377

Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division

Guarulhos, Brasil

Tel: 55-11-6465-6810

Fax: 55-11-6465-6829

[MEMO]

Facsimile Message

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

From:

Name

Company

Tel. FAX

Address

Thank you for your kind support.

North America NEC Electronics America Inc. Corporate Communications Dept. Fax: 1-800-729-9288 1-408-588-6130	Hong Kong, Philippines, Oceania NEC Electronics Hong Kong Ltd. Fax: +852-2886-9022/9044	Asian Nations except Philippines NEC Electronics Singapore Pte. Ltd. Fax: +65-6250-3583
Europe NEC Electronics (Europe) GmbH Market Communication Dept. Fax: +49(0)-211-6503-1344	Korea NEC Electronics Hong Kong Ltd. Seoul Branch Fax: 02-528-4411	Japan NEC Semiconductor Technical Hotline Fax: +81- 44-435-9608
	Taiwan NEC Electronics Taiwan Ltd. Fax: 02-2719-5951	

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Technical Accuracy	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Organization	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

[MEMO]