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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT
µPD703177(A) / µPD703445(A)

V850E/CG2™ CarGate-F / V850E/CG5™CarGate-S 32-/16-BIT ROMLESS MICROCONTROLLER

DESCRIPTION

The V850E/CG2 (“CarGate-F“) and V850E/CG5 (“CarGate-S”) ROM-less microcontroller, are members of NEC's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs. The V850E/CG2 (“CarGate-F“) and V850E/CG5 (“CarGate-S”) are specially designed for the high performance requirements of sophisticated algorithms and calculations. They combine a powerful CPU-Core with a 32-bit wide external memory interface and iCache. The V850E/CG2 (“CarGate-F“) has an additional hardware FPU. Furthermore, they offer an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI) and measurement inputs (A/D converter), with dedicated CAN network support. Thus equipped, the V850E/CG2 (“CarGate-F“) and V850E/CG5 (“CarGate-S”) are ideally suited for automotive applications, like CAN Gateways. They are also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

FEATURES

- 32-bit RISC CPU with Harvard Architecture
- 8 K iCache (2-way associative)
- Full-CAN Interface: 5 channels
- Serial Interfaces: 5 channels
  - 3-wire mode: 3 channels
  - UART mode: 2 channels
- Timers: 2 channels
  - 16-bit multi purpose timer/event counter: channels: 2 channels
- 10-bit resolution A/D Converter: 6 channels
- External Bus Interface (32- / 16- / 8-bit data / 24-bit address)
- I/O lines: max. 71
  - 5 V tolerant: 13 ×
- Power supply voltage range:
  - +3.0 V ≤ V_{DD3} ≤ +3.6 V
- Frequency range: up to 40 MHz
- Built-in low power saving mode
- Built-in clock oscillator circuit with internal PLL
- Built-in clock oscillator circuit with internal spread spectrum PLL for CPU/ BCU clock operation
- Temperature range:
  - -40 °C to +85 °C
- Package:
  - 144 LQFP, 0.5 mm pin-pitch (20 × 20 mm)

ORDERING INFORMATION

Device	Part Number	Package	ROM	RAM	FCAN Option	Operating Temperature (T_A)
V850E/CG2	µPD703177(A)	LQFP144 20 × 20 mm	ROM-less	32 K	5 Channels	-40°C ~ +85°C
V850E/CG5	µPD703445(A)	LQFP144 20 × 20 mm	ROM-less	32 K	5 Channels	-40°C ~ +85°C

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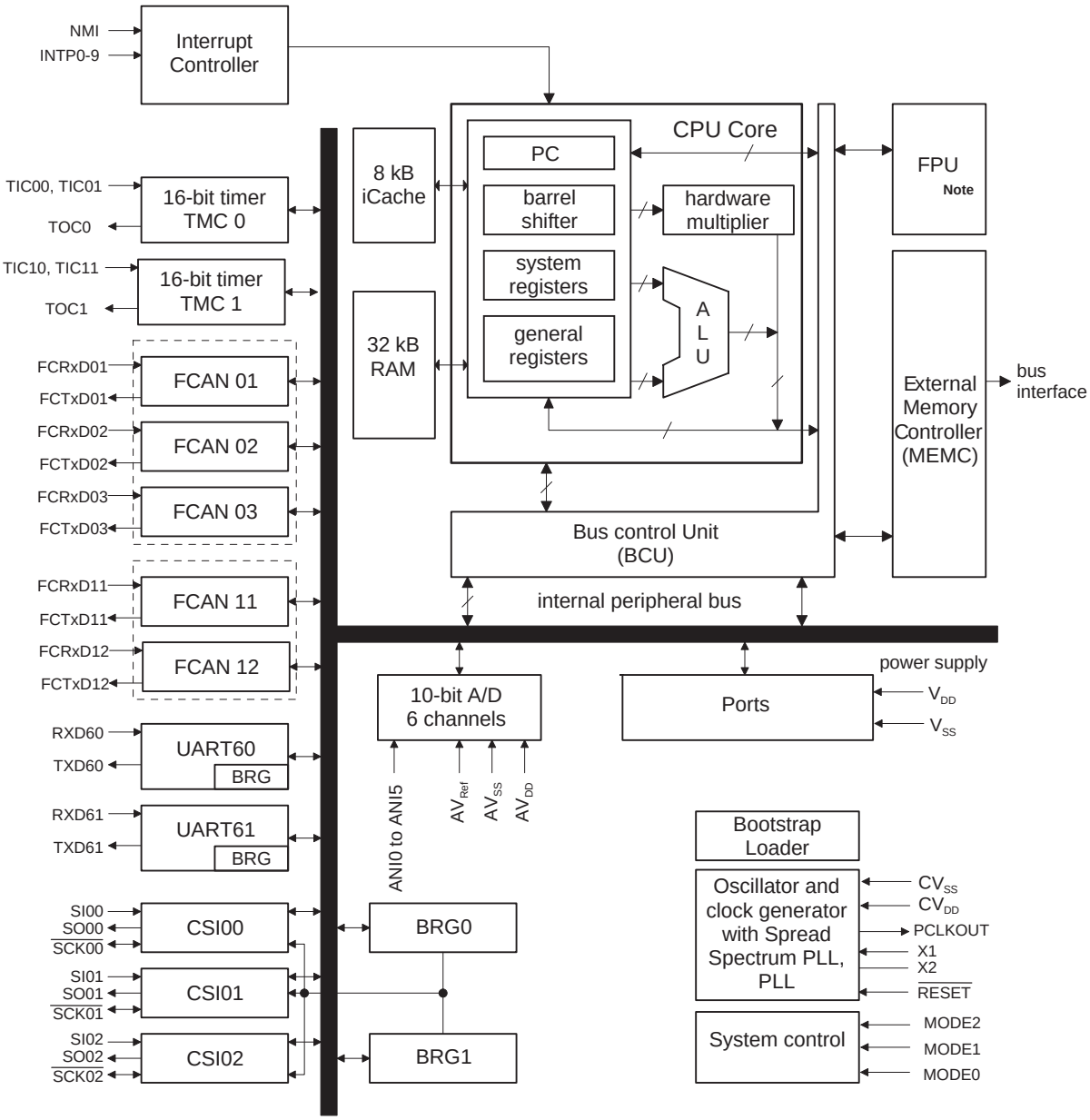
Data Published: February 2006

INTERNAL BLOCK DIAGRAM

Figure IN-1: V850E/CG2 CarGate-F / V850E/CG5 CarGate-S Internal Block Diagram



Note: The Floating Point Unit is only available on V850E/CG2 (“CarGate-F”)

PIN IDENTIFICATION

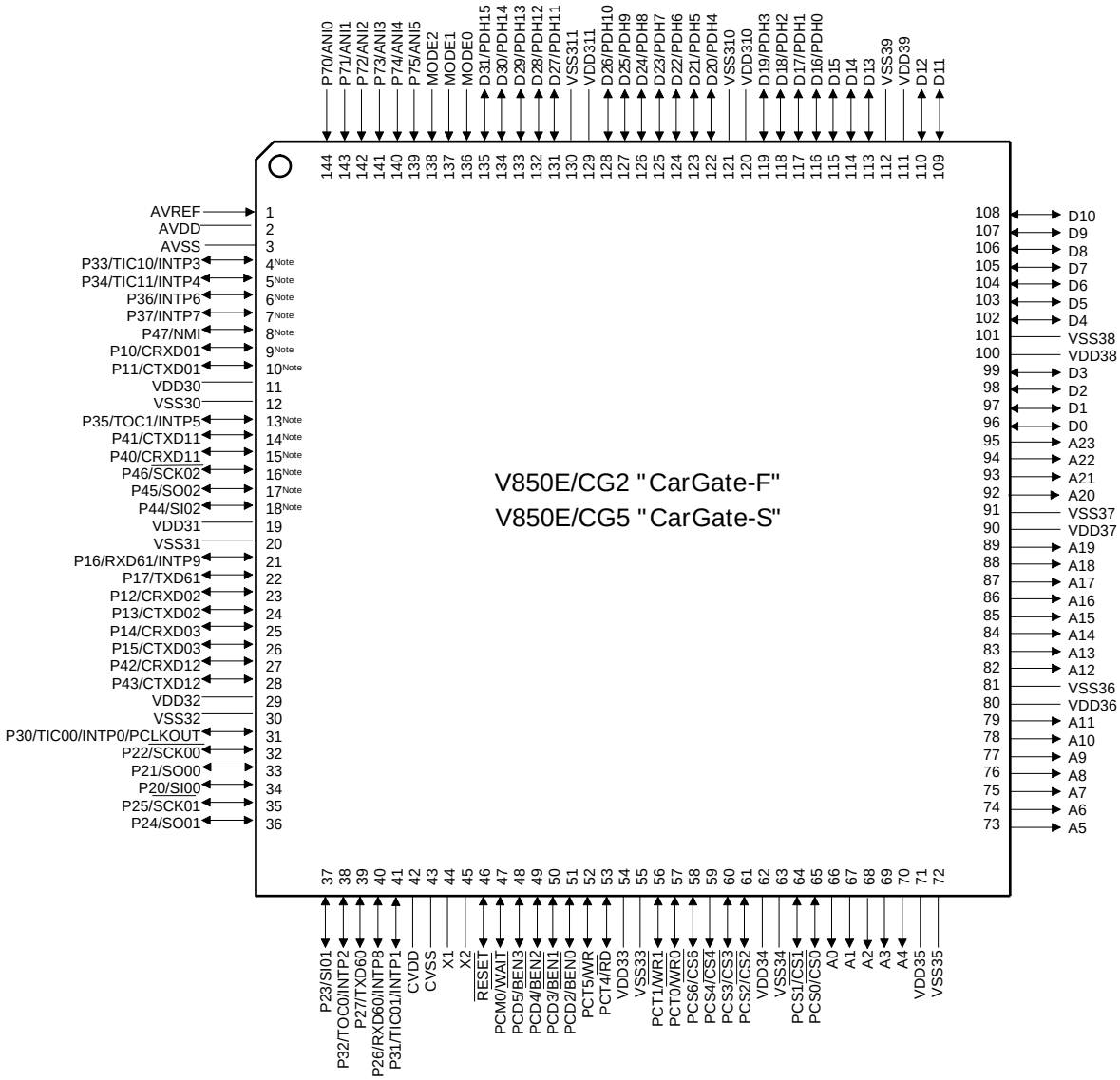
A0 to A23	Address Bus	PCLKOUT	Peripheral Clock Output
D0 to D31	Data Bus	PCM0	Port CM0
ANI0 to ANI5	Analog Input	PCS0-PCS4, PCS6	Port CS
AV_{DD}	Analog Power Supply	PCT0, PCT1, PCT4, PCT5	Port CT
AV_{REF}	Analog Reference Voltage	PCD2 to PCD5	Port CD
AV_{SS}	Analog Ground	PDH0 to PDH16	Port DH
CV_{DD}	Clock Generator Power Supply	RXD60 to RXD61	Receive Data Input
CV_{SS}	Clock Generator Ground	$\overline{SCK00}$ to $\overline{SCK02}$	Serial Clock
FCRXD01 to FCRXD03	CAN Receive Line Input 0	SI00 to SI02	Serial Input
FCTXD01 to FCTXD03	CAN Transmit Line Output0	SO00 to SO02	Serial Output
FCRXD11 to FCRXD12	CAN Receive Line Input 1	TIC00, TIC01, TIC10, TIC11	Timer Input
FCTXD11 to FCTXD12	CAN Transmit Line Output1	TOC0, TOC1	Timer Output
GND_3	Ground for 3 V Power Supply	TXD60 to TXD61	Transmit Data Output
INTP0 to INTP9	External interrupt request	V_{DD3}	3 V Power Supply
MODE0 to MODE2	Mode Inputs	$\overline{RESET}$	Reset
NMI	Non-Maskable Interrupt Request	$\overline{WAIT}$	Wait
P10 to P17	Port 1	$\overline{WRZ}$, $\overline{WRZ0}$, $\overline{WRZ1}$	Write Enable
P20 to P27	Port 2	$\overline{RDZ}$	Read
P30 to P37	Port 3	$\overline{CS0}$-$\overline{CS4}$, $\overline{CS6}$	Chip Select
P40 to P47	Port 4	X1, X2	Crystal (Main-OSC)
P70 to P75	Port 7		

PIN CONFIGURATION (Top View)

- 144 pin QFP (fine pitch) (20 × 20 × 1.4 mm)

  - μPD703177(A)
  - μPD703445(A)

Figure IN-2: V850E/CG2 CarGate-F / V850E/CG5 CarGate-S Pin Configuration



Note: Marked Pins are 5 V tolerant

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1. Pin Functions

1.1 Port Pins

Table 1-1: Pin Function (1/2)

Port	I/O	Function	Port Type	Alternate
P10	I/O	Port 1 8-bit input/output port	5-K	CRXD01**Note**
P11			5-K/ 19	CTXD01**Note**
P12			5-K	CRXD02
P13			5-K	CTXD02
P14			5-K	CRXD03
P15			5-K	CTXD03
P16			5-K	RXD61/INTP9
P17			5-K	TXD61
P20	I/O	Port 2 8-bit input/output port	5-K	SI00
P21			5-K	SO00
P22			5-K	$\overline{\text{SCK00}}$
P23			5-K	SI01
P24			5-K	SO01
P25			5-K	$\overline{\text{SCK01}}$
P26			5-K	RXD60/INTP8
P27			5-K	TXD60
P30	I/O	Port 3 8-bit input/output port	5-K	TIC00/INTP0/ PCLKOUT
P31			5-K	TIC01/ INTP1
P32			5-K	TOC0 / INTP2
P33			5-K	TIC10/INTP3**Note**
P34			5-K	TIC11 / INTP4**Note**
P35			5-K	TOC1 / INTP5**Note**
P36			5-K	INTP6**Note**
P37			5-K	INTP7**Note**
P40	I/O	Port 4 8-bit input/output port	5-K	CRXD11**Note**
P41			5-K / 19	CTXD11**Note**
P42			5-K	CRXD12
P43			5-K	CTXD12
P44			5-K	SI02**Note**
P45			5-K	SO02**Note**
P46			5-K	$\overline{\text{SCK02}}$**Note**
P47			5-K	NMI**Note**

Note: Marked pins are 5 V tolerant

Table 1-1: Pin Function (2/2)

Port	I/O	Function	Port Type	Alternate
P70	I	Port 7 6-bit input port	9-C	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
PDH0	I/O	Port DH[Note] 16-bit input/output port	5	D16
PDH1				D17
PDH2				D18
PDH3				D19
PDH4				D20
PDH5				D21
PDH6				D22
PDH7				D23
PDH8				D24
PDH9				D25
PDH10				D26
PDH11				D27
PDH12				D28
PDH13				D29
PDH14				D30
PDH15				D31
PCS0	I/O	Port CS 6-bit input/output port	5	$\overline{CS0}$
PCS1				$\overline{CS1}$
PCS2				$\overline{CS2}$
PCS3				$\overline{CS3}$
PCS4				$\overline{CS4}$
PCS6				$\overline{CS6}$
PCD2	I/O	Port CD 4-bit input/output port	5	$\overline{BEN0}$
PCD3				$\overline{BEN1}$
PCD4				$\overline{BEN2}$
PCD5				$\overline{BEN3}$
PCM0	I/O	Port CM 1-bit input/output port	5	$\overline{WAIT}$
PCT0	I/O	Port CT 4-bit input/output port	5	$\overline{WR0}$
PCT1				$\overline{WR1}$
PCT4				$\overline{RD}$
PCT5				$\overline{WR}$

Note: PDH is only available for ROM-less mode 1 (16-bit wide external bus at reset)

1.2 Non-Port Pins

Table 1-2: Non-Port Pins (1/3)

Pin Name	I/O	Function	Port Type	Alternate
V_{DD30}-V_{DD36} **Note 2**	–	Power supply 3.3 V	-	-
V_{SS30}-V_{SS36}	–	GND potential for 3.3 V power supply	-	-
CV_{DD} **Note 3**	–	Connection for 3.3 V clock oscillator power supply	-	-
CV_{SS}		GND potential for 3.3 V clock oscillator power supply	-	-
X1	input	System clock oscillator connection pins.	16	-
X2	output		16	-
PCKLOUT	output	Peripheral clock output	5-K	P30 / INTP0
MODE0-MODE2	input	Selects operating mode	2	-
$\overline{RESET}$	input	System reset input	2	-
AV_{DD}	–	Power supply for A/D converter	-	-
AV_{SS}	–	Ground potential for A/D converter	-	-
AV_{REF}	input	reference voltage input for A/D converter	-	-
NMI **Note 1**	input	non maskable interrupt input	5-K	P47
ANI0-ANI5	input	analog input to A/D converter	9-C	P70 to P75
SI00	input	serial receive data input to CSI00-CSI02	5-K	P20
SI01			5-K	P23
SI02 **Note 1**			5-K	P44
SO00	output	serial transmit data output from CSI00-CSI02	5-K	P21
SO01			5-K	P24
SO02 **Note 1**			5-K	P45
$\overline{SCK00}$	I/O	serial clock I/O from/to CSI00-CSI02	5-K	P22
$\overline{SCK01}$			5-K	P25
$\overline{SCK02}$ **Note 1**			5-K	P46
RXD60	input	serial receive data input to UART60-UART61	5-K	P26 / INTP8
RXD61			5-K	P16 / INTP9
TXD60	output	serial transmit data output from UART60-UART61	5-K	P27
TXD61			5-K	P17
CRXD01 **Note 1**	input	serial receive data input to FCAN01-FCAN03	5-K	P10
CRXD02			5-K	P12
CRXD03			5-K	P14
CRXD11 **Note 1**	input	serial receive data input to FCAN11-FCAN12	5-K	P40
CRXD12			5-K	P42

Notes: 1. Marked pins are 5 V tolerant

2. All V_{DD3} pins have to be connected to each other. On each pin V_{DD3}, a capacitor containing a very low serial impedance has to be attached as tight as possible to the pin

3. On CV_{DD}, a capacitor containing a very low serial impedance has to be attached as tight as possible to the pin. V_{DD3} and CV_{DD} must be connected to each other

4. PDH is only available for ROM-less mode 1 (16-bit wide ext. bus at reset)

Table 1-2: Non-Port Pins (2/3)

Pin Name	I/O	Function	Port Type	Alternate
CTXD01**Note 1**	output	serial transmit data output to FCAN01-FCAN03	5-K / 19	P11
CTXD02			5-K	P13
CTXD03			5-K	P15
CTXD11**Note 1**	output	serial transmit data output to FCAN01-FCAN03	5-K / 19	P41
CTXD12			5-K	P43
INTP0	input	external interrupt request	5-K	P30 / TIC00/ PCKLOUT
INTP1				P31 / TIC01
INTP2				P32 / TOC0
INTP3**Note 1**				P33 / TIC10
INTP4**Note 1**				P34 / TIC11
INTP5**Note 1**				P35 / TOC1
INTP6**Note 1**				P36
INTP7**Note 1**				P37
INTP8				P26/RXD60
INTP9				P16/RXD61
TIC00	input	Timer C 0 capture input 0	5-K	P30/INTP0/ PCKLOUT
TIC01	input	Timer C 0 capture input 1	5-K	P31/INTP1
TOC0	output	Timer C 0 compare output 1	5-K	P32/INTP2
TIC10**Note 1**	input	Timer C 1 capture input 0	5-K	P33/INTP3
TIC11**Note 1**	input	Timer C 1 capture input 1	5-K	P34/INTP4
TOC1**Note 1**	output	Timer C 1 compare output 1	5-K	P35/INTP5
D0-D15	I/O	Data bus of external bus**Note 4**	5	-
D16-D31	I/O		5	PDH0-PDH15
A0-A7	output	Address bus of external bus	3	-
A8-A15				-
A16-A23				-
WR0	output	Write strobe signal for lower byte (bit 0 - bit 7)	5	PCT0
WR1	output	Write strobe signal for upper byte (bit 0 - bit 7)	5	PCT1
$\overline{RD}$	output	Read strobe signal for external bus	5	PCT4
$\overline{WR}$	output	Write strobe signal for external bus	5	PCT5
$\overline{WAIT}$	input	Control signal input for external bus	5	PCM0

Notes: 1. Marked pins are 5 V tolerant

2. All V_{DD3} pins have to be connected to each other. On each pin V_{DD3}, a capacitor containing a very low serial impedance has to be attached as tight as possible to the pin

3. On CV_{DD}, a capacitor containing a very low serial impedance has to be attached as tight as possible to the pin. V_{DD3} and CV_{DD} must be connected to each other

4. PDH is only available for ROM-less mode 1 (16-bit wide ext. bus at reset)

Table 1-2: Non-Port Pins (3/3)

Pin Name	I/O	Function	Port Type	Alternate
$\overline{CS0}$	output	Chip select output for external bus	5	PCS0
$\overline{CS1}$				PCS1
$\overline{CS2}$				PCS2
$\overline{CS3}$				PCS3
$\overline{CS4}$				PCS4
$\overline{CS6}$				PCS6
$\overline{BEN0}$	output	Byte enable for external bus	5	PCD2
$\overline{BEN1}$				PCD3
$\overline{BEN2}$				PCD4
$\overline{BEN3}$				PCD5

Notes: 1. Marked pins are 5 V tolerant

2. All V_{DD3} pins have to be connected to each other. On each pin V_{DD3}, a capacitor containing a very low serial impedance has to be attached as tight as possible to the pin

3. On CV_{DD}, a capacitor containing a very low serial impedance has to be attached as tight as possible to the pin. V_{DD3} and CV_{DD} must be connected to each other

4. PDH is only available for ROM-less mode 1 (16-bit wide ext. bus at reset)

1.3 I/O Circuits

Figure 1-1: Input / Output Circuits (1/2)

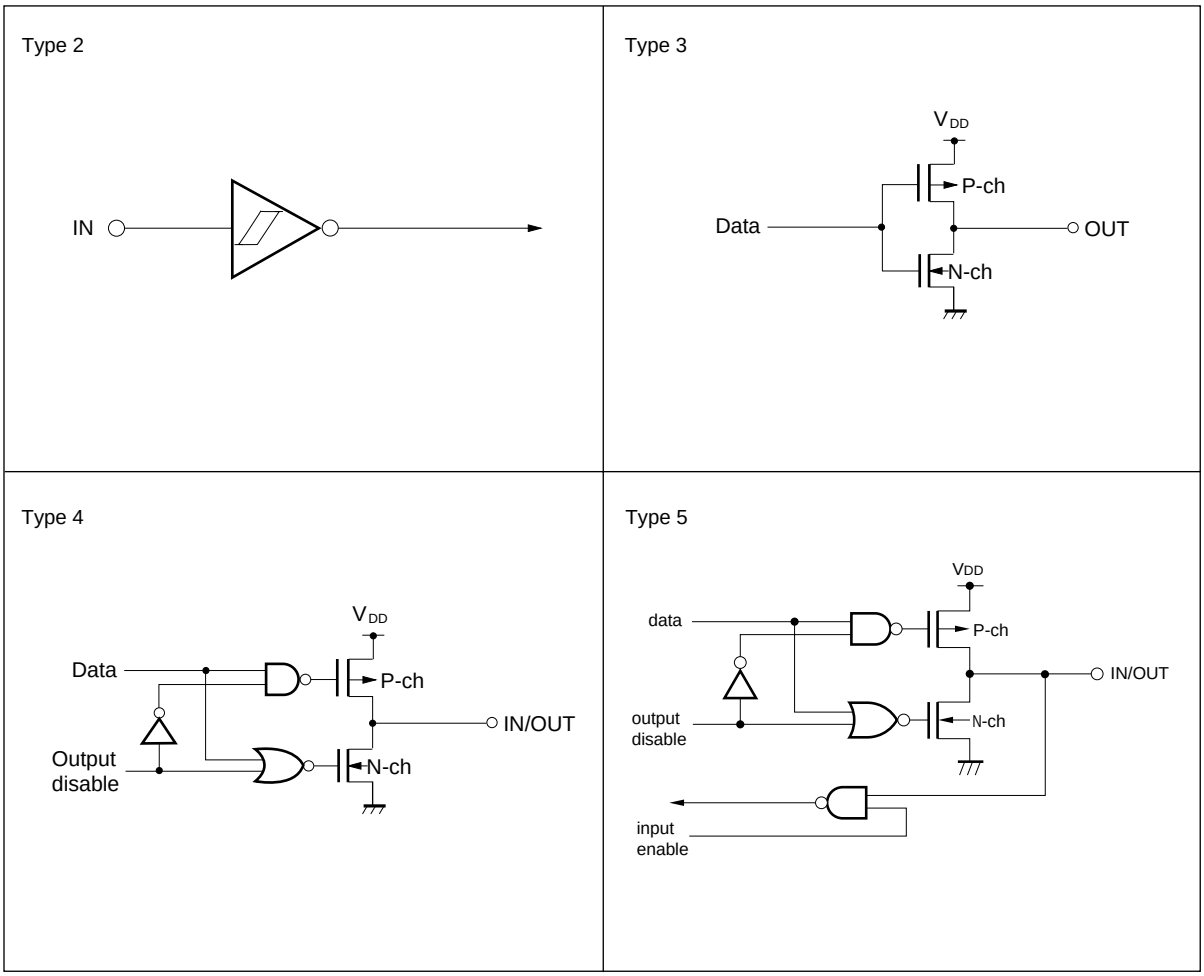
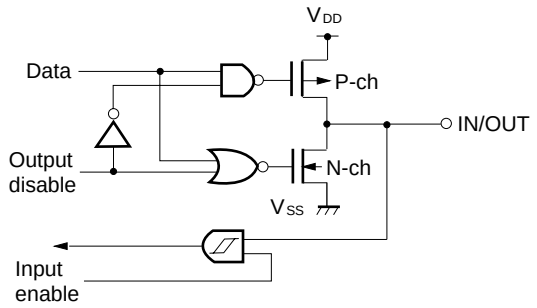
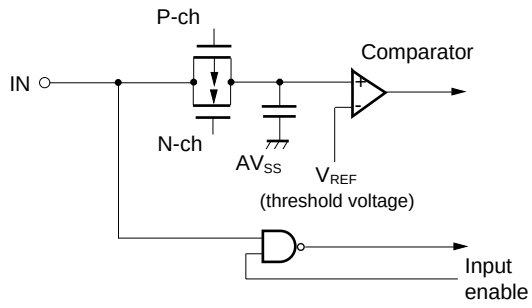


Figure 1-1: Input / Output Circuits (2/2)

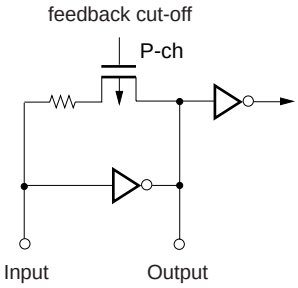
Type 5-K



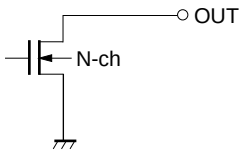
Type 9-C



Type 16



Type 19



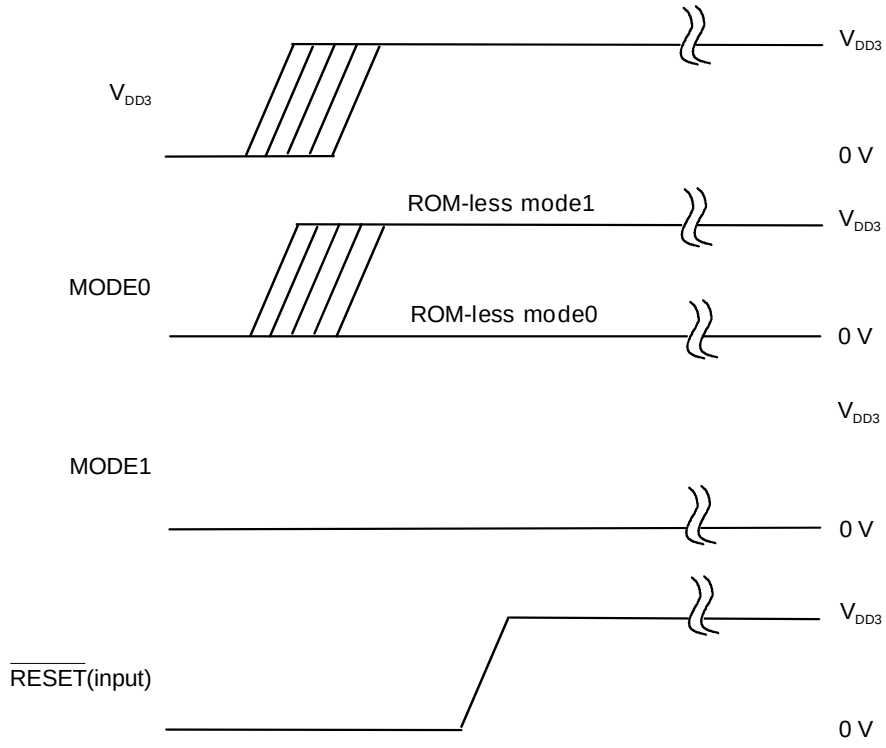
2. Programming External Flash Memory

The devices μPD703177(A) and μPD703445(A) support the programming of external flash memories using 2 dedicated flash-programming mode (ROM-less mode0 & ROM-less mode1), dependent on the used bus width for external flash access. These modes will be entered if the MODE pins have been configured accordingly and in addition a system reset has been performed.
In the flash-programming mode, an integrated Boot-Loader is enabled to download the programming and control algorithms to the CarGate-F's and CarGate-S's iRAM. This feature offers a high flexibility to be able to program various external flash memories.

Naturally, it is also possible to program the external flash memory by performing self-programming software functions and I/O communications.

For programming details, see the User's Manual.

Figure 2-1: Programming Mode Selection Format



Note: Refer to the chapter "RESET (power up/down sequence)" on page 30.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings (T_A = 25°C, V_{SS3x} = 0 V)

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage		AV_{DD}		-0.5 ~ +4.6	V
		AV_{SS}		-0.5 ~ +0.5	V
		V_{DD3}		-0.5 ~ +4.6	V
		CV_{DD}		-0.5 ~ +4.6	V
		CV_{SS}		-0.5 ~ +0.5	V
Input voltage	5 V tolerant pins**Note 1**	V_{I4}	$V_{I4} < V_{DD3}$ + 3.0 V	-0.5 ~ +6.6	V
	3.3 V pins**Note 2**	V_{I3}	$V_{I3} < V_{DD3}$ + 0.5 V	-0.5 ~+4.6	V
	A_{VREF}	V_{IAVREF}	$V_{IAVREF} < AV_{DD}$ +0.3 V	-0.3 ~ +4.6	V
	P7	V_{IA}	$V_{IA} < AV_{DD}$ + 0.3 V	-0.3 ~ +4.6	V
Output current low	1 pin	I_{OL0}		4.0	mA
	All pins	I_{OL1}		50	mA
Output current high	1 pin	I_{OH0}		-4.0	mA
	All pins	I_{OH1}		-50	mA
Output voltage	3.3 V pins**Note 2**	V_{O1}	$V_{O1} < V_{DD3}$ + 0.5 V	-0.5 ~ +4.6	V
Operating temperature		T_{OPR}		-40 ~ +85	°C
Storage temperature		T_{STGB}		-55 ~ +150	°C

Notes: 1. 5 V tolerant pins are P10, P11, P33, P34, P35, P36, P37, P40, P41, P44, P45, P46, P47

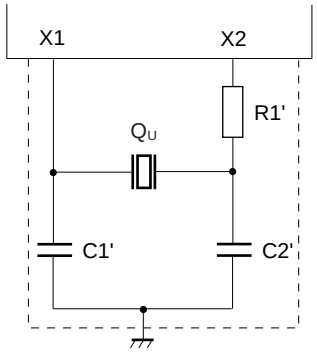
2. 3.3 V pins are Ax, Dx, PCSx, PCM0, PCTx, MODEx, PCDx, P12~P17, P2x, P30~P32, P42, P43, $\overline{\text{RESET}}$

3.2 General Characteristics

3.2.1 Oscillator recommendations (main system clock oscillator)

(1) Ceramic resonator or crystal resonator connection

Figure 3-1: Main Oscillator Recommendations



Remark: Values of capacitors C1', C2' and R1' depend on used resonator and must be specified in cooperation with the manufacturer.

Cautions: 1. External clock input is prohibited.

2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

3.2.2 Oscillator characteristics

(T_A = -40 ~ +85°C, V_{DD3x} = CV_{DD} = AV_{DD} = 3.0 V ~ 3.6 V, V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 3-2: Main Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}		500[Note]			ns
Main oscillator frequency	f_{OSC}		4		5	MHz

Note: The above specified value is the time needed to stabilize internally. It does not include the stabilization time of the external crystal. This value is specified for an external quartz which reached 10% / 90% maximum oscillation level. The oscillation stabilization time for the external crystal has to be added to above specified value.

3.2.3 Peripheral PLL characteristics

(T_A = -40 ~ +85°C, V_{DD3x} = CV_{DD} = AV_{DD} = 3.0 V ~ 3.6 V, V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 3-3: Peripheral PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL lock time	T_{PLL}				1	ms

3.2.4 Spread spectrum PLL characteristics

(T_A = -40 ~ +85°C, V_{DD3x} = CV_{DD} = AV_{DD} = 3.0 V ~ 3.6 V, V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 3-4: Spread Spectrum PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SSCG lock time	T_{SSCG}				3	ms
Frequency multiplication[Note 1]	M_{SSCG}	F_{OSC} = 4 MHz		60/3		-
		F_{OSC} = 5 MHz		48/3		-
Frequency modulation[Note 2]		Dithering enabled		1		%

Notes: 1. Frequency multiplication is given as n/m where
n means setup values for register SCFC0/SCFC1and
m means divider factor determined by register SCFMC
Please refer to CarGate-F UM.

2. Frequency modulation is determined by register values of SCFC0 and SCFC1.

3.2.5 Capacitances

(T_A = 25°C, V_{DD3x} = V_{SS3x} = CV_{DD} = CV_{SS} = AV_{DD} = AV_{SS} = 0 V)

Table 3-5: Capacitances

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

3.3 Operating Conditions

3.3.1 Peripheral clock

(T_A = -40 ~ +85°C, V_{DD3x} = CV_{DD} = AV_{DD} = 3.0 V ~ 3.6 V, V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 3-6: Peripheral Clock

Clock Mode	Inside Peripheral Operation Clock Frequency
PLL on Note 1	16 to 20 MHz
PLL off Note 2	4 to 5 MHz

Notes: 1. The inside peripheral operation clock frequency is the crystal frequency multiplied with the multiplication factor ×4.

2. The inside peripheral operation clock frequency is the crystal frequency.

3.3.2 CPU/BCU clock

(T_A = -40 ~ +85°C, V_{DD3x} = CV_{DD} = AV_{DD} = 3.0 V ~ 3.6 V, V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 3-7: CPU/BCU Clock

Clock Mode	Inside Operation Clock Frequency
SSCG on Note 1	20 & 40 MHz
PLL on Note 2	16 to 20 MHz 32 to 40 MHz
SSCG off, PLL off Note 3	4 to 5 MHz

Notes: 1. The max. inside operation clock frequency is the crystal frequency multiplied with a multiplication factor configured in the SSCG Frequency Control Register 1 (SCFC1) and divided by a factor configured in the SSCG Frequency Modulation Control Register (SCFMC).

2. The inside operation clock frequency is the crystal frequency multiplied with the multiplication factor ×4 or ×8 according to the setting of the Processor Clock Control Register (PCC).

3. The inside operation clock frequency is the crystal frequency.

3.4 DC Characteristics

(T_A = -40 ~ +85°C, V_{DD3x} = CV_{DD} = AV_{DD} = 3.0 V ~ 3.6 V, V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 3-8: DC Characteristics Conditions

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	Pin group 1	V_{IH1}		0.7 V_{DD3}		V_{DD3}	V
Input voltage low	Pin group 1	V_{IL1}		0		0.3 V_{DD3}	V
Input voltage high	Pin group 2	V_{IH3}		0.8 V_{DD3}		V_{DD3}	V
Input voltage low	Pin group 3	V_{IL3}		0		0.2 V_{DD3}	V
Input voltage high	Pin group 4	V_{IH7}		0.8 V_{DD3}		5.5	V
Input voltage high	P7x	V_{IHA}		0.7 AV_{DD}		AV_{DD}	V
Input voltage low	P7x	V_{ILA}		0		0.3 AV_{DD}	V
Output voltage high	Pin group 5	V_{OH1}	I_{OH} = -2.5 mA	V_{DD3} - 1 V			V
	Pin group 4		I_{OH} = -1.0 mA	V_{DD3} - 1 V			V
Output voltage low	Pin group 6	V_{OL1}	I_{OL} = 2.5 mA			0.4	V
Input leakage current high	Pin group 7	I_{LIH1}	V_I = V_{DD3}			5	μA
	Pin group 4	I_{LIH2}	V_I = 5.5 V			5	μA
	P7x	I_{LIHA}	AV_{IN} = AV_{DD}			5	μA
Input leakage current low	Pin group 8	I_{LIL1}	V_I = 0 V			-5	μA
	P7x	I_{LILA}	AV_{IN} = 0 V			-5	μA

Remarks: 1. Pin group 1: D0-15, PDHx, PCSx, PCM0, PCTx
(All pins with CMOS input characteristic)

2. Pin group 2: MODEx, P12~17, P2x, P30~P32, P42, P43, $\overline{\text{RESET}}$
(All 3.3 V pins with SCHMITT input characteristic)

3. Pin group 3: P1x, P2x, P3x, P4x, MODEx, $\overline{\text{RESET}}$
(All pins with SCHMITT input characteristic)

4. Pin group 4: P10, P11, P33, P34, P35, P36, P37, P40, P41, P44, P45, P46, P47
(All 5 V tolerant pins)

5. Pin group 5: Ax, Dx, PDHx, PCSx, PCM0, PCTx, PCDx, P12~P17, P2x, P30~P32, P42, P43
(All 3.3 V pins with output capability)

6. Pin group 6: Ax, Dx, PDHx, PCSx, PCM0, PCTx, PCDx, P1x, P2x, P3x, P4x
(All pins with output capability)

7. Pin group 7: Dx, PDHx, PCSx, PCM0, PCTx, PCDx, MODEx, P12~P17, P2x, P30~P32, P42, P43, $\overline{\text{RESET}}$
(All 3.3 V pins except P7x)

8. Pin group 8: Dx, PDHx, PCSx, PCM0, PCTx, PCDx, MODEx, P1x, P2x, P3x, P4x, $\overline{\text{RESET}}$
(All pins except P7x)

Table 3-9: Power Supply Currents

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1SC1}	Operating (SSCG1) (f_{CPU} = 40 MHz) (f_{Perph} = 20 MHz) SSCG: on; PLL: on		105	158	mA
	I_{DD1SC2}	Operating (SSCG2) (f_{CPU} = 20 MHz) (f_{Perph} = 20 MHz) SSCG: on; PLL: on		73	110	mA
	I_{DD1P1}	Operating (PLL1) (f_{CPU} = 40 MHz) (f_{Perph} = 20 MHz) SSCG: off; PLL: on		97	146	mA
	I_{DD1O}	Operating (OSC) (f_{CPU} = 5 MHz) (f_{Perph} = 5 MHz) SSCG: off; PLL: off		16	24	mA
	I_{DD2SC1}	HALT(SSCG1) (f_{CPU} = 40 MHz) (f_{Perph} = 20 MHz) SSCG: on; PLL: on		70	105	mA
	I_{DD2P1}	HALT (PLL1) (f_{CPU} = 40 MHz) (f_{Perph} = 20 MHz) SSCG: off; PLL: on		63	95	mA
	I_{DD3SC1}	IDLE (SSCG1) (f_{CPU} = 40 MHz) (f_{Perph} = 20 MHz) SSCG: on; PLL: on		6.5	10	mA
	I_{DD3P1}	IDLE (PLL1) (f_{CPU} = 40 MHz) (f_{Perph} = 20 MHz) SSCG: off; PLL: off		2	3	mA
	I_{DD5P}	STOP		100	500	μA

Remark: The current values listed above are valid for current consumed by the chip logic itself, i.e. excluding ADC and I/O buffer power supply.

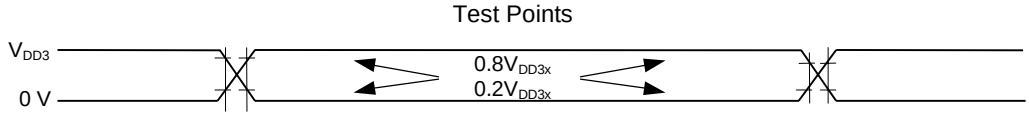
3.5 AC Characteristics

T_A = -40 ~ +85°C,
V_{DD3x} = CV_{DD} = AV_{DD} = 3.0 V ~ 3.6 V,
V_{SS3x} = CV_{SS} = AV_{SS} = 0 V,
output pin load capacitance: C_L= 50 pF

3.5.1 General

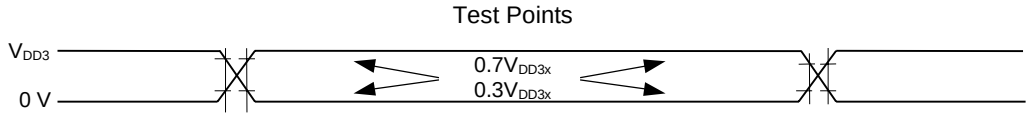
For pins P1x, P2x, P3x, P4x, MODEx, $\overline{\text{RESET}}$
(All 3.3 V pins with SCHMITT input characteristics)

Figure 3-2: AC Test Input/Output Waveform SCHMITT



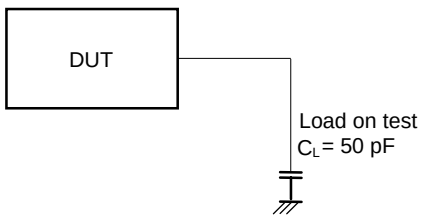
For pins D0-D15, PDHx, PCSx, PCM0, PCTx, P7x
(All pins with CMOS input characteristics)

Figure 3-3: AC Test Input/Output Waveform CMOS



3.5.2 AC test load condition

Figure 3-4: AC Test Load Condition

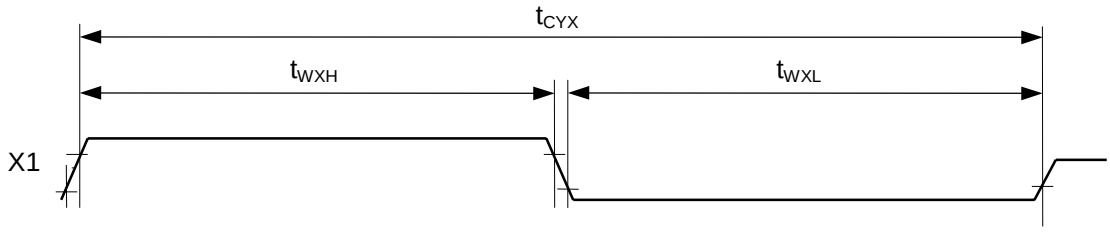


3.5.3 Clock timing

Table 3-10: Clock Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	OSC Mode	200	250	ns
X1 input high-level width	t_{WXH}	OSC Mode	95		ns
X1 input low-level width	t_{WXL}	OSC Mode	95		ns

Figure 3-5: Clock Timing



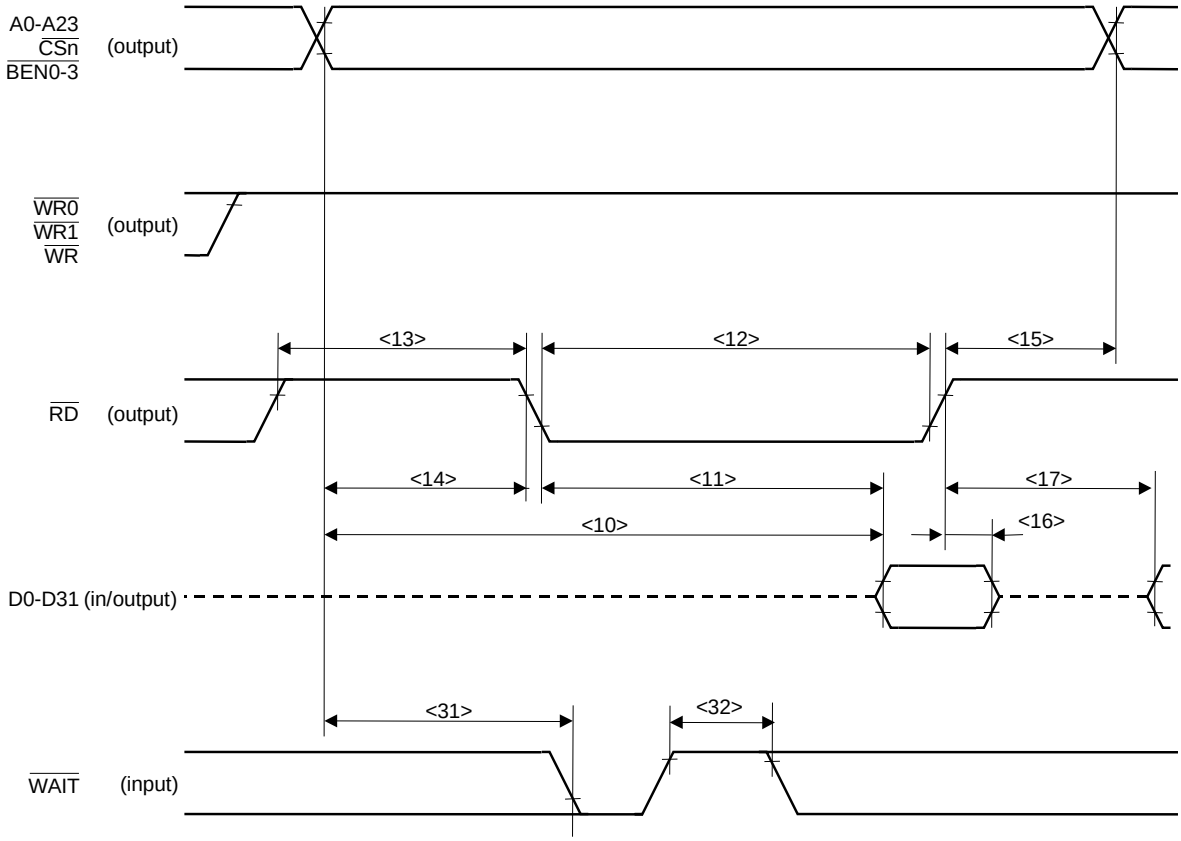
3.5.4 External memory access read timing

Table 3-11: External Memory Access Read Timing

Parameter		Symbol	MIN.	MAX.	Unit
Data input set up time (vs. address)	<10>	T_{SAID}		$(2+W_T)T-23$	ns
Data input set up time (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}		$(1.5+W_D+W)T-20.5$	ns
$\overline{RD}$ Low level width	<12>	T_{WRDL}	$(1.5+W_D+W)T-5$		ns
$\overline{RD}$ High level width	<13>	T_{WRDH}	$(0.5+W_{AS}+i)T-5$		ns
Address, $\overline{CSn} \rightarrow \overline{RD}\downarrow$ delay time	<14>	T_{DARD}	$(0.5+W_{AS})T-12$		ns
$\overline{RD}\uparrow \rightarrow$ address delay time	<15>	T_{DRDA}	iT-2		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	T_{HRDID}	-2		ns
$\overline{RD}\uparrow \rightarrow$ data output delay time	<17>	T_{DRDOD}	(0.5+i)T-6		ns
$\overline{WAIT}$ set up time (vs. address)	< 31>	T_{SAW}		$(1+W_{AS})T-22.5$	ns
$\overline{WAIT}$ high level width	<32>	T_{WWH}	T+10		ns

Remarks:
1. T: $1/f_{CPU}$
2. i: Number of idle states specified by BCC register
3. W_T: Total Number of waits, $W_T=W_{AS}+W_D+W$
4. W_{AS}: Number of waits specified by ASC register
5. W_D: Number of waits specified by DWC1, DWC2 register; $W_D \geq 1$
6. W: Number of waits due to $\overline{WAIT}$

Figure 3-6: External Memory Access Read Timing



3.5.5 External memory access write timing

Table 3-12: External Memory Access Write Timing

Parameter		Symbol	MIN.	MAX.	Unit
Address, $\overline{CSn} \rightarrow \overline{WR0}$, $\overline{WR1}\downarrow$ delay time	<20>	T_{DAWR}	$(0.5+W_{AS})T-8.5$		ns
Address set up (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<21>	T_{SAWR}	$(1.5+W_T)T-8.5$		ns
$\overline{WR0}$, $\overline{WR1}\uparrow \rightarrow$ address delay time	<22>	T_{DWRA}	$(0.5+i)T-10$		ns
$\overline{WR0}$, $\overline{WR1}$ High level width	<23>	T_{WWRH}	$(0.5+i+W_{AS})T-10$		ns
$\overline{WR0}$, $\overline{WR1}$ Low level width	<24>	T_{WWRL}	$(1+W+W_D)T-8.0$		ns
Data output set up time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<25>	T_{SODWR}	$(0.5+W_T)T-6.0$		ns
Data output hold time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<26>	T_{HWROD}	$(0.5+i)-6.0$		ns
$\overline{WAIT}$ set up time (vs. address)	<31>	T_{SAW}		$(1+W_{AS})T-22.5$	ns
$\overline{WAIT}$ high level width	<32>	T_{WWH}	T+10		ns

Remarks:

1. T: $1/f_{CPU}$

2. i: Number of idle states specified by BCC register

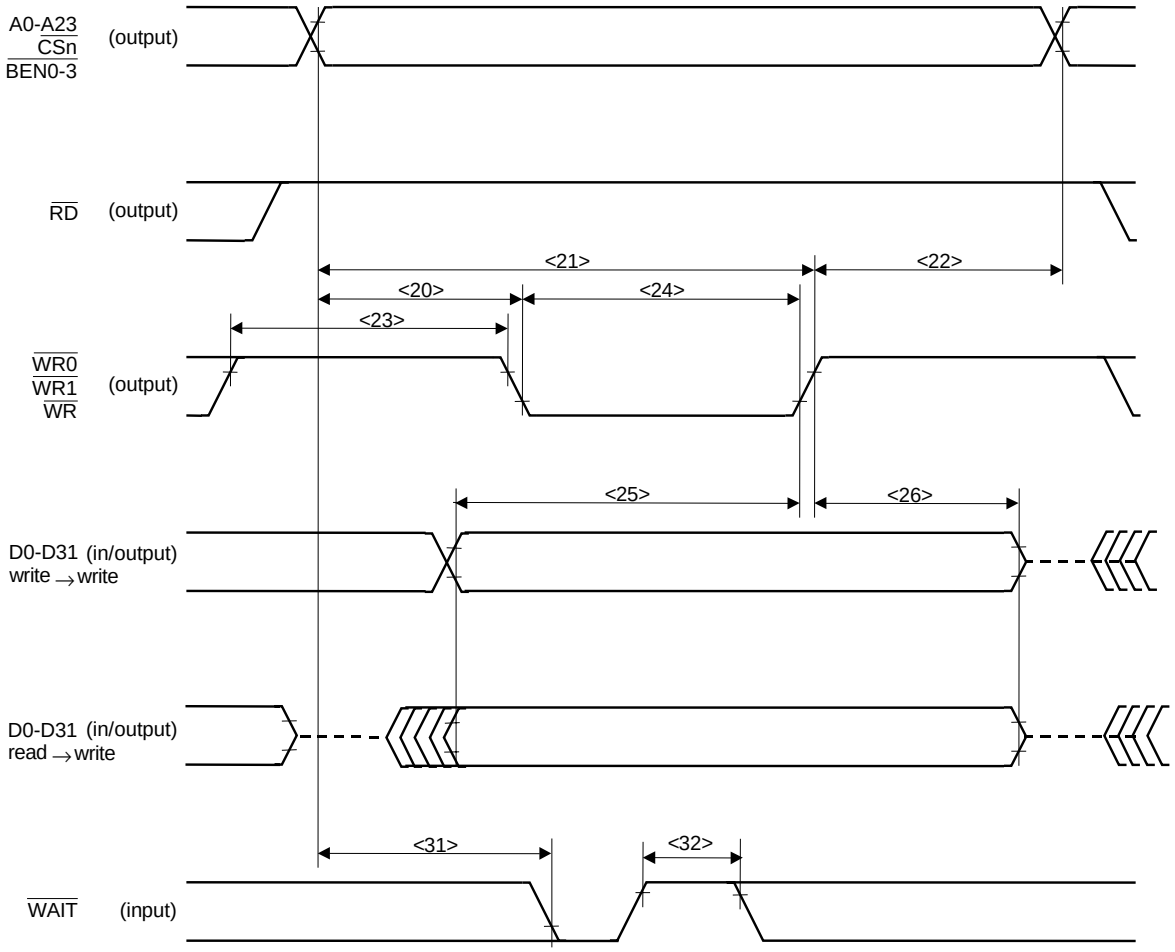
3. W_T: Total Number of waits, $W_T=W_{AS}+W_D+W$

4. W_{AS}: Number of waits specified by ASC register

5. W_D: Number of waits specified by DWC1, DWC2 register; $W_D \geq 1$

6. W: Number of waits due to $\overline{WAIT}$

Figure 3-7: External Memory Access Write Timing



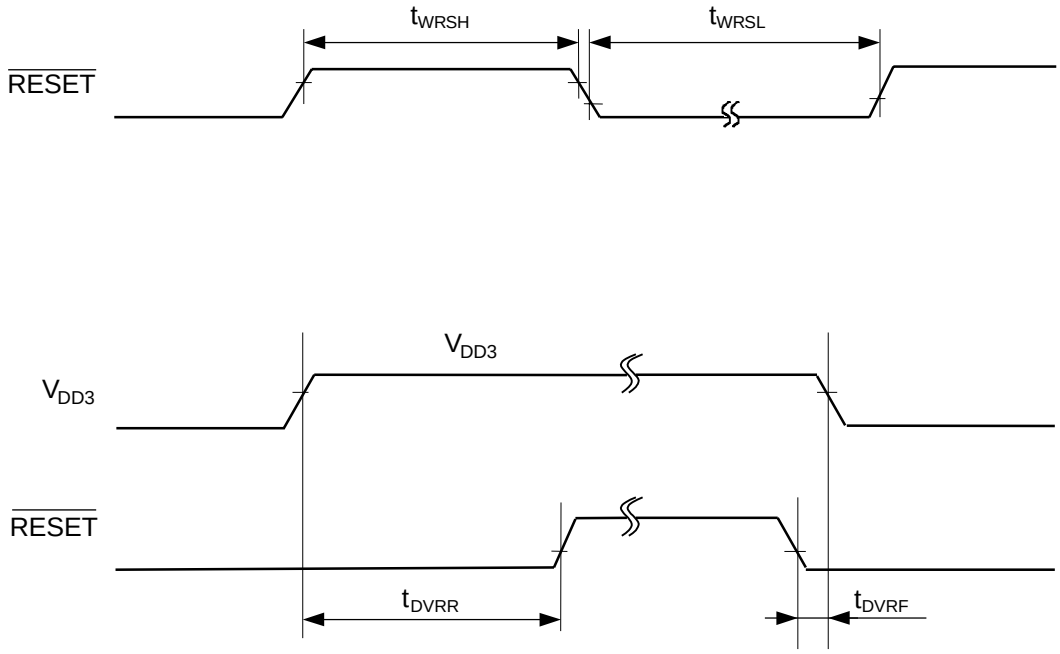
3.5.6 $\overline{\text{RESET}}$ (power up/down sequence)

Table 3-13: $\overline{\text{RESET}}$ Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL0}	STOP mode release	T_{OST} **Note**		ms
	t_{WRSL2}	except STOP Mode release	500		ns
$\overline{\text{RESET}}$ hold time	t_{DVRR}	OSC Mode on power-on	T_{OST} **Note**		ms
$\overline{\text{RESET}}$ setup time	t_{DVRF}	OSC Mode on power-off	0		ns

Note: T_{OST}: Oscillation stabilization time of main oscillator

Figure 3-8: $\overline{\text{RESET}}$ Timing



Caution: $\overline{\text{RESET}}$ must be applied whenever V_{DD3} is out of operating condition.

3.5.7 Interrupt timing

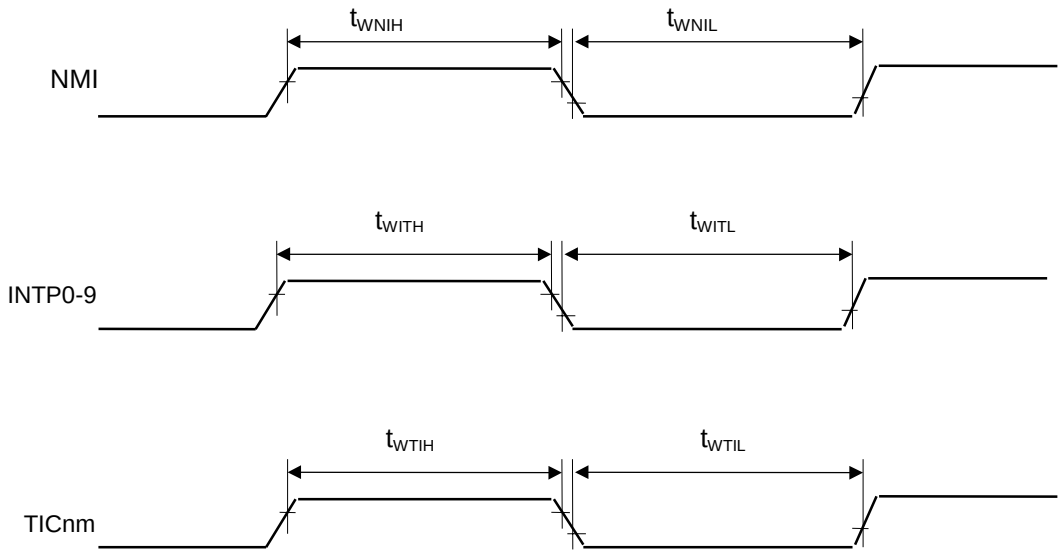
Table 3-14: Interrupt Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI high-level width	t_{WNIH}		500		ns
NMI low-level width	t_{WNIL}		500		ns
INTPi **Note 1** high-level width	t_{WITH}		500		ns
INTPi **Note 1** low-level width	t_{WITL}		500		ns
TICmn **Note 2** high-level width	t_{WTIH}		500		ns
TICmn **Note 2** low-level width	t_{WTIL}		500		ns

Notes: 1. i = 0 to 9

2. m & n = 0 to 1

Figure 3-9: Interrupt Timing



3.6 Peripheral Function Characteristics

3.6.1 Timer C

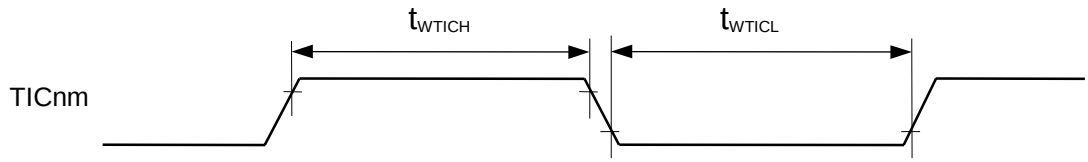
Table 3-15: Timer C Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
TICmn **Note 1** high-level width	t_{WTICH}		100 + T_T **Note 2**		ns
TICmn **Note 1** low-level width	t_{WTICL}		100 + T_T **Note 2**		ns

Notes: 1. m & n = 0 to 1

2. T_T: Depends on selected clock source for the peripheral clock supply and the setup of the respective timer macro clock and timer channel setup

Figure 3-10: Timer C Characteristics



3.6.2 CSI

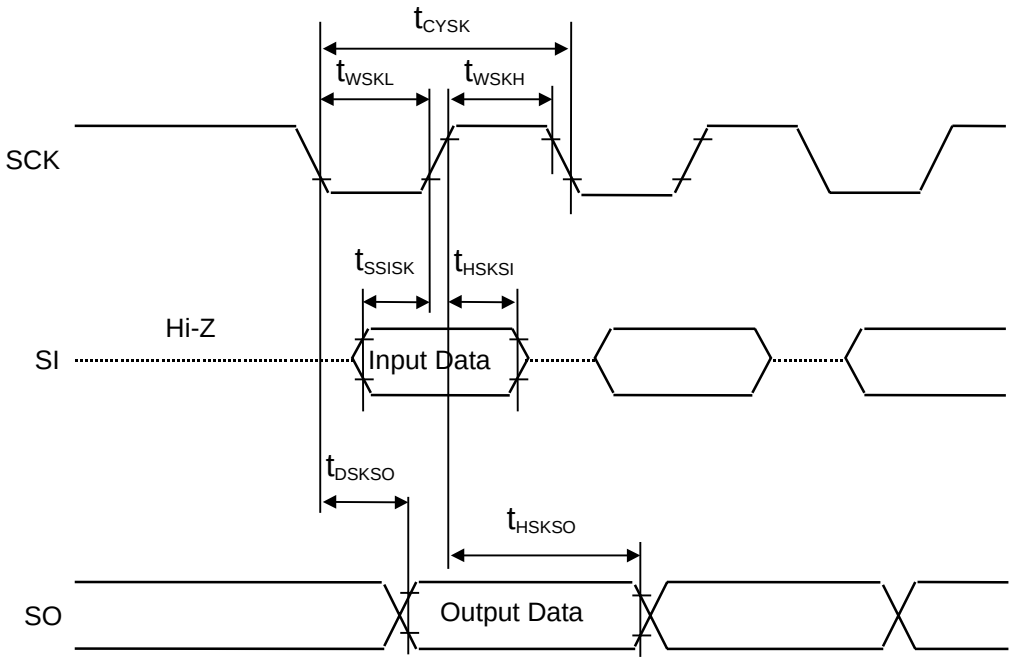
Table 3-16: CSI Master Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSKM}	Output	200		ns
$\overline{SCK}$ high level width	t_{WSKHM}	Output	0.5 t_{CYSK} - 15		ns
$\overline{SCK}$ low level width	t_{WSKLM}	Output	0.5 t_{CYSK} - 15		ns
SI set up time (to $\overline{SCK}$ ↑)	t_{SSISKM}		30		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKSIM}		30		ns
SO output delay time (from $\overline{SCK}$ ↓)	t_{DSKSOM}			30	ns
SO output hold time (from $\overline{SCK}$ ↑)	t_{HSKSOM}		0.5 t_{CYSK} - 5		ns

Table 3-17: CSI Slave Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSKS}	Input	200		ns
$\overline{SCK}$ high level width	t_{WSKHS}	Input	90		ns
$\overline{SCK}$ low level width	t_{WSKLS}	Input	90		ns
SI set up time (to $\overline{SCK}$ ↑)	t_{SSISKS}		15		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKSIS}		15		ns
SO output delay time (from $\overline{SCK}$ ↓)	t_{DSKSOS}			30	ns
SO output hold time (from $\overline{SCK}$ ↑)	t_{HSKSOS}		t_{WSKH}		ns

Figure 3-11: CSI Slave Mode Characteristics



3.6.3 UART6

Table 3-18: UART Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UART6}	$f_{Peripheral} \geq 5$ MHz		312500	bps

3.6.4 FCAN

Table 3-19: FCAN Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FCAN}	$f_{Peripheral} \geq 16$ MHz		1	Mbps

3.6.5 Serial flash programming operating characteristics

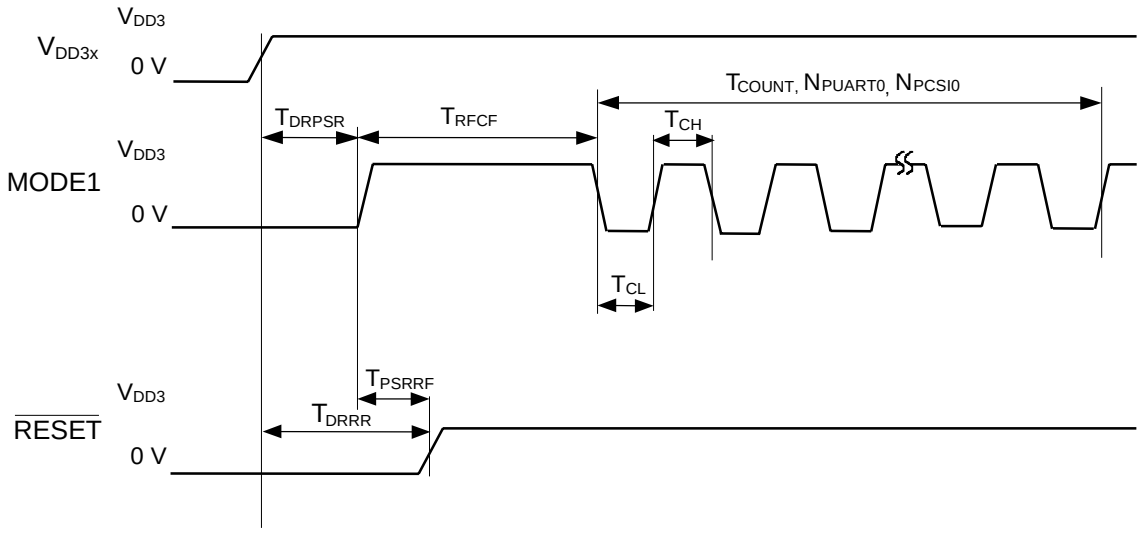
Table 3-20: Serial Flash Programming Operating Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Count start setup time from $\overline{\text{RESET}}\uparrow$	T_{RFCF}		$5T^{\text{Note 1}}$ + 500		μs
Times of MODE1 counting	T_{COUNT}			10	ms
MODE1 count High/Low level width	T_{CH}, T_{CL}		1		μ
$V_{DD3}\uparrow$ setup time MODE1$\uparrow$	T_{DRPSR}		100		ns
$V_{DD3}\uparrow$ setup time $\overline{\text{RESET}}\uparrow$	T_{DRRR}		T_{OST}		ms
MODE1$\uparrow$ setup time $\overline{\text{RESET}}\uparrow$	T_{PSRRF}		T_{OST}		ms
MODE1[Note 2] pulse count for UART0	N_{PUART0}		0		-
MODE1[Note 2] pulse count for CSI0	N_{PCSI0}		8		-

Notes: 1. $T = 1/f_{OSC}$

2. MODE1 input pin is a schmitt-trigger input buffer

Figure 3-12: Serial Flash Programming Operating Characteristics



3.6.6 A/D converter

Table 3-21: A/D Converter Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution	-			10		Bit
Overall error **Note 1**	-	$AV_{REF} = AV_{DD}$			±8	LSB
Conversion time **Note 2**	t_{CONV}		5		12	μs
Sampling time	t_{SAM}			$T_{CONV}/6$		μs
Analogue input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Analogue supply current	I_{AVDD}				3.0	mA
Reference voltage	AV_{REF}		3.0		AV_{DD}	V
Reference voltage input current operation	I_{AVREF}	$AV_{REF} = AV_{DD}$		1	2	mA

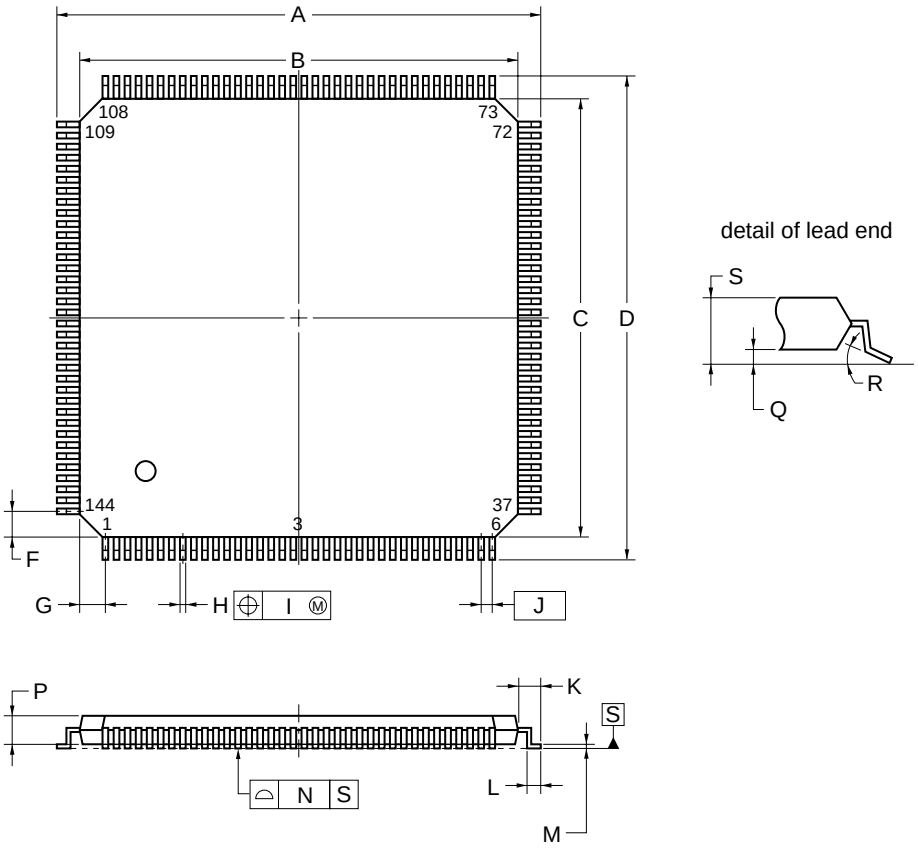
Notes: 1. Quantization error is not included

2. Conversion time is determined by the number of clocks set by the ADM1 register.

4. Package Drawing

Figure 4-1: Package Drawing

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

5. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document Semiconductor Device:
Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended please consult NEC.

Table 5-1: Soldering Conditions

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (210 °C min.), Number of times: 3 max., Number of days: 7 **Note**	IR-35-207-3

Note: After that, prebaking is necessary at 125 °C for 20 hours.
The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution: Do not use two or more soldering methods in combination (except partial heating method).

6. Revision History

Version	Date	Author	Remarks
0.1	06/01/05	S.Vollhardt	First official released version of this document
0.2	30/01/06	S. Vollhardt	Table 1-1 & 1-2 Port Types inserted Figure 1-1 updated Main system clock crystal recommendation removed Oscillation stabilization time changed Soldering conditions added

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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For further information, please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
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Hanover Office
Podbielski Strasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
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Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
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Succursale Française
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78142 Velizy-Villacoublay Cédex
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Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
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5616 HR Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
TEL: 010-8235-1155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
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