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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD703002

V852™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD703002 is a product in the V850 Family™ of 32-bit single-chip microcontrollers for real-time control applications. It integrates a 32-bit CPU, ROM, RAM, interrupt controller, real-time pulse unit, and serial interface on a single chip.

The μPD70P3002 is available as an on-chip PROM version.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

V852 User's Manual Hardware : U10038E
V850 Family User's Manual Architecture : U10243E

FEATURES

- Number of instructions: 74
- Minimum instruction execution time: 40 ns (@ 25-MHz operation)
- General-purpose register: 32 bits x 32
- Instruction set ideal for control application
- Internal memory ROM : 90 Kbytes
  RAM : 3 Kbytes
- High-performance interrupt controller
- Real-time pulse unit ideal for control
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- Power save function

APPLICATIONS

- Audiovisual: Camcorders, VCRs, etc.
- Office equipment: PPCs, LBPs, printers, etc.
- Industry: Motor control, numerical control type machine tools, etc.
- Communication: Cellular phones, etc.

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Document No. U11826EJ3V0DS00 (3rd edition)
Date Published July 1997 N
Printed in Japan

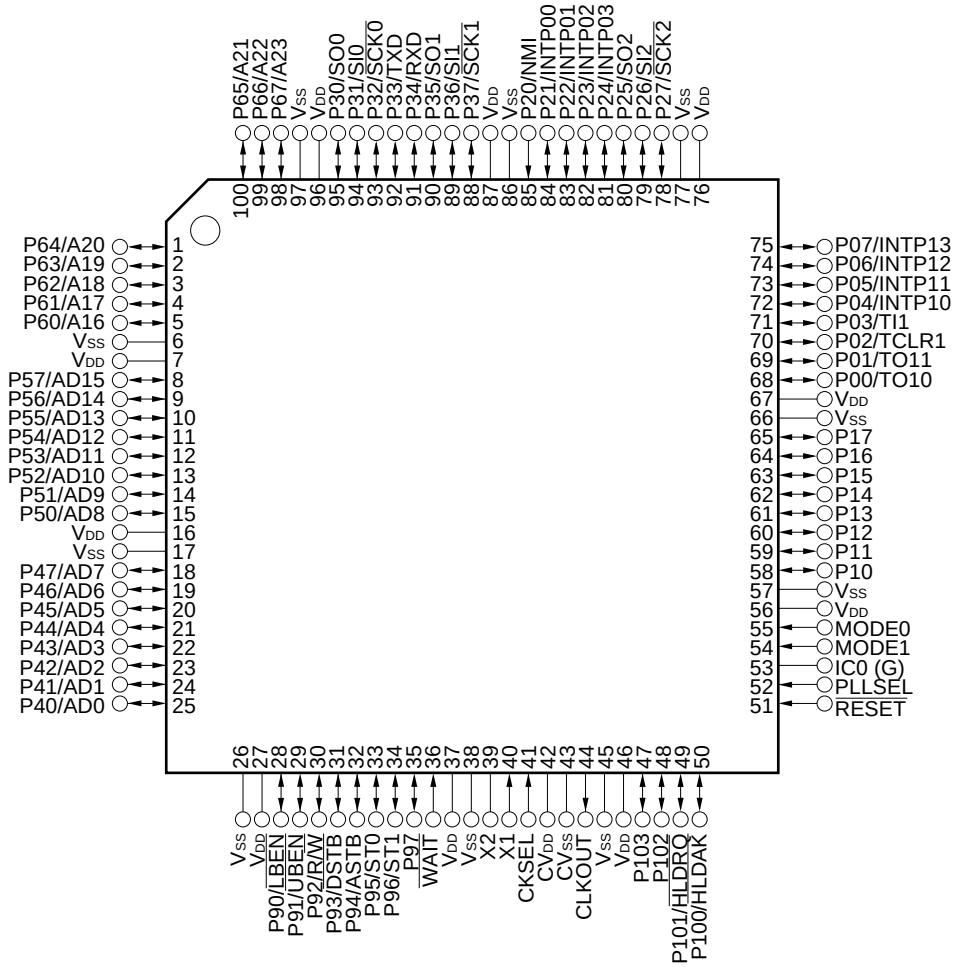
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD703002GC-25-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm) (Resin thickness : 1.45 mm)
★ μPD703002GC-25-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm) (Resin thickness : 1.40 mm)

Remark xxx indicates the ROM code suffix.

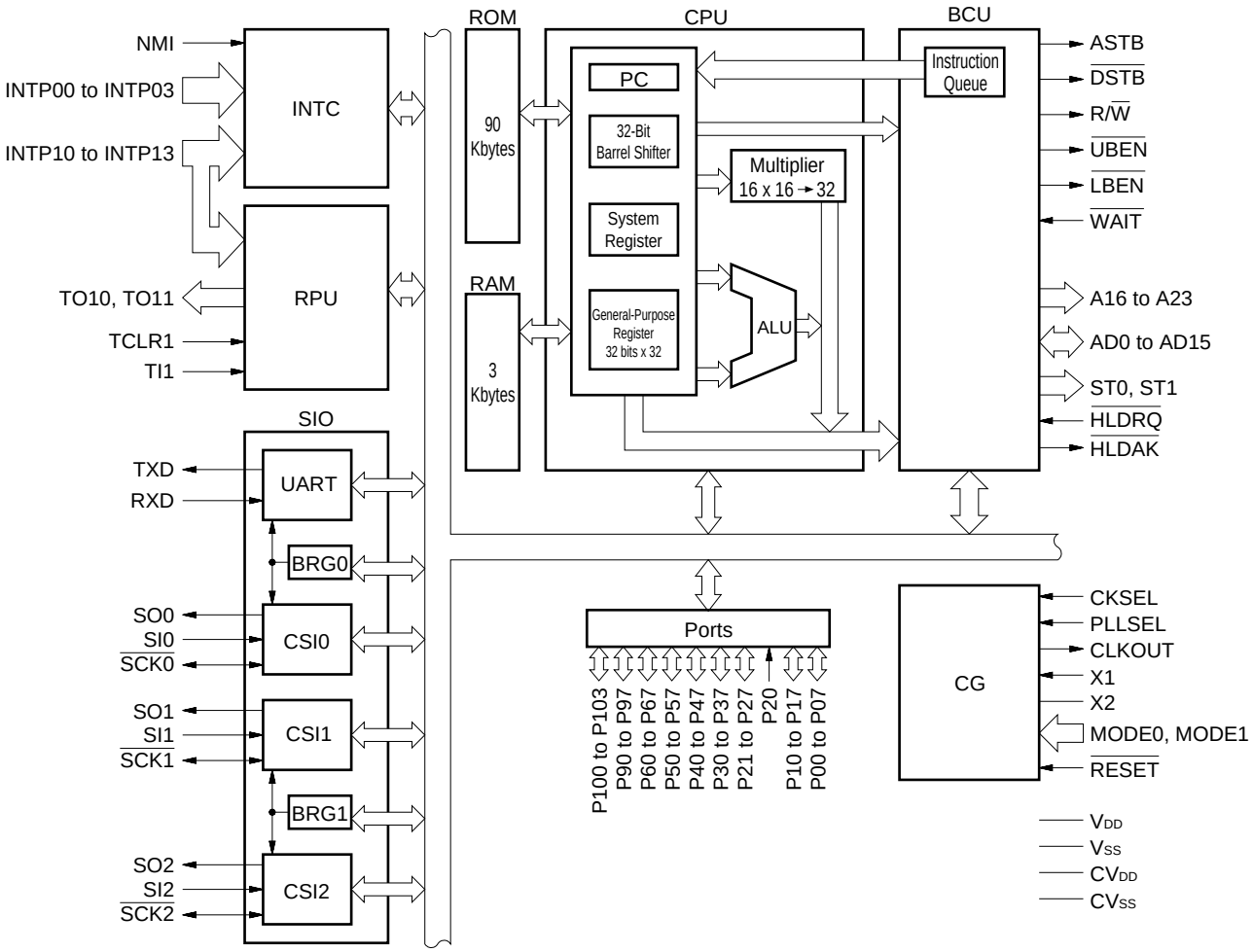
PIN CONFIGURATION



Caution ( ) indicates the processing of the pins not used in the normal operation mode.
G : Directly connect this pin to VSS.

P00 to P07	: Port0
P10 to P17	: Port1
P20 to P27	: Port2
P30 to P37	: Port3
P40 to P47	: Port4
P50 to P57	: Port5
P60 to P67	: Port6
P90 to P97	: Port9
P100 to P103	: Port10
TO10, TO11	: Timer Output
TCLR1	: Timer Clear
TI1	: Timer Input
INTP00 to INTP03, INTP10 to INTP13	: Interrupt Request From Peripherals
NMI	: Non-maskable Interrupt Request
SO0 to SO2	: Serial Output
SI0 to SI2	: Serial Input
$\overline{SCK0}$ to $\overline{SCK2}$	: Serial Clock
TXD	: Transmit Data
RXD	: Receive Data
AD0 to AD15	: Address/Data Bus
A16 to A23	: Address Bus
$\overline{LBEN}$	: Lower Byte Enable
$\overline{UBEN}$	: Upper Byte Enable
R/$\overline{W}$	: Read/Write Status
$\overline{DSTB}$	: Data Strobe
ASTB	: Address Strobe
ST0, ST1	: Status
$\overline{HLDAK}$	: Hold Acknowledge
$\overline{HLDRQ}$	: Hold Request
CLKOUT	: Clock Output
CKSEL	: Clock Select
PLLSEL	: PLL Select
$\overline{WAIT}$	: Wait
MODE0, MODE1	: Mode
$\overline{RESET}$	: Reset
X1, X2	: Crystal
CV_{DD}	: Power Supply for Clock Generator
CV_{SS}	: Ground for Clock Generator
V_{DD}	: Power Supply
V_{SS}	: Ground
IC0	: Internally Connected

FUNCTION BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTION LIST

1.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit input/output port Input/output can be specified bit-wise.	TO10
P01			TO11
P02			TCLR1
P03			TI1
P04			INTP10
P05			INTP11
P06			INTP12
P07			INTP13
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified bit-wise.	—
P20	Input	Port 2 P20 is the port for input only Operates as an NMI input when a valid edge is input. And shows NMI input status at bit 0 of P2 register. P21 to P27 are 7-bit input/output ports. Input/output can be specified bit-wise.	NMI
P21	I/O		INTP00
P22			INTP01
P23			INTP02
P24			INTP03
P25			SO2
P26			SI2
P27			$\overline{\text{SCK2}}$
P30	I/O	Port 3 8-bit input/output port Input/output can be specified bit-wise.	SO0
P31			SI0
P32			$\overline{\text{SCK0}}$
P33			TXD
P34			RXD
P35			SO1
P36			SI1
P37			$\overline{\text{SCK1}}$
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified bit-wise.	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port Input/output can be specified bit-wise.	AD8 to AD15
P60 to P67	I/O	Port 6 8-bit input/output port Input/output can be specified bit-wise.	A16 to A23

(2/2)

Pin Name	I/O	Function	Alternate Function
P90	I/O	Port 9 8-bit input/output port Input/output can be specified bit-wise.	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			R/$\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			ST0
P96			ST1
P97			—
P100	I/O	Port 10 4-bit input/output port Input/output can be specified bit-wise.	$\overline{\text{HLDAK}}$
P101			$\overline{\text{HLDRQ}}$
P102			—
P103			—

1.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO10	Output	Pulse signal output of timer 1	P00
TO11			P01
TCLR1	Input	Timer 1 external clear signal input	P02
TI1		Timer 1 external count clock input	P03
INTP10	Input	External maskable interrupt request input, or timer 1 external capture trigger input (in common use)	P04
INTP11			P05
INTP12			P06
INTP13			P07
NMI	Input	Non-maskable interrupt request input	P20
INTP00	Input	External maskable interrupt request input	P21
INTP01			P22
INTP02			P23
INTP03			P24
SO0	Output	CSI0 serial data transmission output	P30
SI0	Input	CSI0 serial data reception input	P31
$\overline{SCK0}$	I/O	CSI0 serial clock I/O	P32
SO1	Output	CSI1 serial data transmission output	P35
SI1	Input	CSI1 serial data reception input	P36
$\overline{SCK1}$	I/O	CSI1 serial clock I/O	P37
SO2	Output	CSI2 serial data transmission output	P25
SI2	Input	CSI2 serial data reception input	P26
$\overline{SCK2}$	I/O	CSI2 serial clock I/O	P27
TXD	Output	UART serial data transmission output	P33
RXD	Input	UART serial data reception input	P34
AD0 to AD7	I/O	16-bit multiplexed address/data bus when expanding memory externally	P40 to P47
AD8 to AD15			P50 to P57
A16 to A23	Output	Higher address bus when expanding memory externally	P60 to P67
$\overline{LBEN}$	Output	External data bus lower byte enable signal output	P90
$\overline{UBEN}$		External data bus higher byte enable signal output	P91
R/$\overline{W}$		External read/write status output	P92
$\overline{DSTB}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
ST0		External bus cycle status output	P95
ST1			P96
$\overline{HLDAK}$	Output	Bus hold acknowledge output	P100
$\overline{HLDRQ}$	Input	Bus hold request input	P101
CLKOUT	Output	System clock output	—
CKSEL	Input	Clock generator operation mode specification	—
PLLSEL	Input	Input specifying PLL multiplication coefficient input	—

(2/2)

Pin Name	I/O	Function	Alternate Function
$\overline{WAIT}$	Input	Bus cycle wait insertion control signal input	—
MODE0, MODE1	Input	Operation mode specification	—
$\overline{RESET}$	Input	System reset input	—
X1	Input	Connect resonator for system clock. Input external clock to X1.	—
X2	—		—
CV_{DD}	—	Positive power for internal clock generator	—
CV_{SS}	—	Ground potential for internal clock generator	—
V_{DD}	—	Positive power supply	—
V_{SS}	—	Ground potential	—
IC0	—	Internally connected	—

1.3 Pin I/O Circuits and Recommended Connections of Unused Pins

Table 1-1 shows the I/O circuit types of the respective pins in the normal operation mode and recommended connections of unused pins. Figure 1-1 shows the respective circuit types partially simplified.

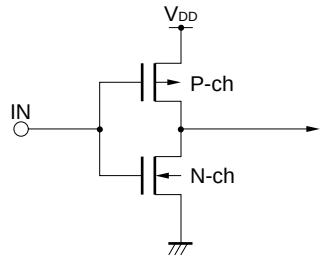
When connecting a pin to V_{DD} or V_{SS} via resistor, use of a resistor of 3 to 10 kΩ is recommended.

Table 1-1. Types of Pin I/O Circuits and Recommended Connections of Unused Pins

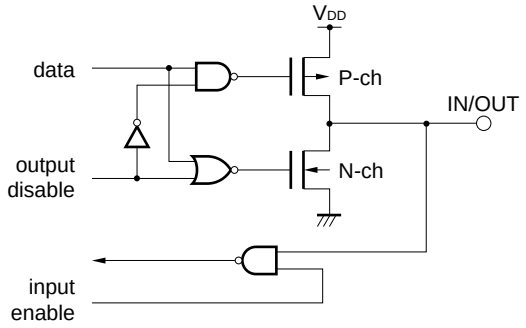
Pin Name	I/O Circuit Type	Recommended Connections
P00/TO10, P01/TO11	5	Input: Individually connect to V_{DD} or V_{SS} via resistor Output: Open
P02/TCLR1, P03/TI1, P04/INTP10 to P07/INTP13	8	
P10 to P17	5	
P20/NMI	2	Directly connect to V_{SS}
P21/INTP00 to P24/INTP03	8	Input: Individually connect to V_{DD} or V_{SS} via resistor Output: Open
P25/SO2	5	
P26/SI2, P27/$\overline{SCK2}$	8	
P30/SO0	5	
P31/SI0, P32/$\overline{SCK0}$	8	
P33/TXD, P34/RXD, P35/SO1	5	
P36/SI1, P37/$\overline{SCK1}$	8	
P40/AD0 to P47/AD7	5	
P50/AD8 to P57/AD15		
P60/A16 to P67/A23		
P90/$\overline{LBEN}$		
P91/$\overline{UBEN}$		
P92/R/$\overline{W}$		
P93/$\overline{DSTB}$		
P94/ASTB		
P95/ST0, P96/ST1		
P97		
P100/$\overline{HLDAK}$		
P101/$\overline{HLDRQ}$		
P102, P103		
CLKOUT	3	Open
CKSEL	2	—
PLLSEL	2	—
$\overline{WAIT}$	1	Directly connect to V_{DD}
MODE0, MODE1	2	—
$\overline{RESET}$		
IC0	—	Directly connect to V_{SS}
★ CV_{DD}	—	Directly connect to V_{DD}
★ CV_{SS}	—	Directly connect to V_{SS}

Figure 1-1. Pin I/O Circuits

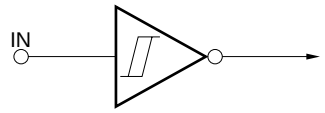
Type 1



Type 5

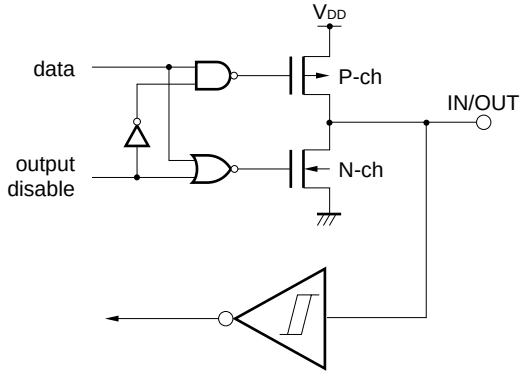


Type 2

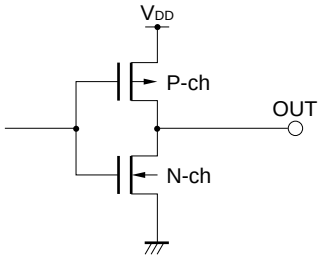


Schmitt trigger input with hysteresis characteristics

Type 8



Type 3



2. FUNCTION BLOCKS

2.1 Internal Units

2.1.1 CPU

Most instructions, such as address calculation, arithmetic and logic operation, and data transfer, are executed in one clock cycle under control of 5-stage pipeline.

The CPU also includes dedicated hardware such as a multiplier (16 by 16) and a 32-bit barrel shifter, aiming at processing complex instructions at high speeds.

In addition, the CPU can access internal ROM (90 Kbytes) and RAM (3 Kbytes) in one clock cycle.

2.1.2 Bus control unit (BCU)

★ The BCU initiates necessary external bus cycles based on the physical address given by the CPU. When an instruction fetch of external memory is executed, if no bus cycle initiation is requested by the CPU, the BCU creates a prefetch address to prefetch an instruction code. The prefetched instruction code is taken into the internal instruction queue.

2.1.3 ROM

The ROM has a capacity of 90 Kbytes and is mapped from the address 00000000H. Access to the ROM is enabled/disabled by setting the MODE0 and MODE1 pins.

The CPU can access any address of the ROM in one clock cycle (to fetch an instruction).

2.1.4 RAM

This RAM has a capacity of 3 Kbytes and is mapped from address FFFFE000H. The CPU can access any address of the RAM in one clock cycle (to access data).

2.1.5 Port

The μPD703000 is provided with a total of 68 input/output port pins (of which one is an input port pin), or ports 0 through 10. These port pins can be used as the control pins.

2.1.6 Interrupt controller (INTC)

The interrupt controller controls various interrupt requests (NMI, INTP00-INTP03, and INTP10-INTP13) issued by peripheral hardware or external devices. Up to eight levels of interrupt priority can be individually specified for each interrupt request. In addition, multiplexed processing control can be performed.

2.1.7 Clock generator (CG)

The clock generator generates a CPU operating clock whose frequency is 1 or 5 times as high as (with the internal PLL) or half (without the internal PLL) the frequency of the resonator connected across the X1 and X2 pins. Instead of connecting a resonator, a clock signal can be input from off-chip.

2.1.8 Real-time pulse unit (RPU)

The RPU which includes a 16-bit timer/event counter and a 16-bit interval timer, measures pulse intervals and pulse frequency, and outputs programmable pulses.

2.1.9 Serial interface (SIO)

The serial interface includes one UART channel (asynchronous serial interface) and three CSI channels (clocked serial interface).

The UART transfers data with the TXD and RXD pins. The baud rate is generated by an on-chip dedicated baud rate generator. The CSI transfers data with the SO0 to SO2, SI0 to SI2, and $\overline{SCK0}$ to $\overline{SCK2}$ pins. The baud rate can be generated from an on-chip dedicated baud rate generator, or supplied from off-chip.

3. CPU FUNCTION

The CPU of the μPD703002 is based on the RISC architecture and executes almost all the instructions in one clock cycle, using a 5-stage pipeline.

3.1 Features

- Minimum instruction execution time: 40 ns (@ internal 25-MHz operation)
- Address space: 16-Mbyte linear
- General registers: 32 bits × 32
- Internal 32-bit architecture
- Five-stage pipeline control
- Multiply/divide instruction
- Saturated operation instruction
- 32-bit shift instruction: 1 clock
- Long/short format
- Internal memory
  - ROM: 90 Kbytes
  - RAM: 3 Kbytes
- Bit manipulate instructions: 4 types
  - Set
  - Clear
  - Not
  - Test

4. BUS CONTROL FUNCTION

4.1 Features

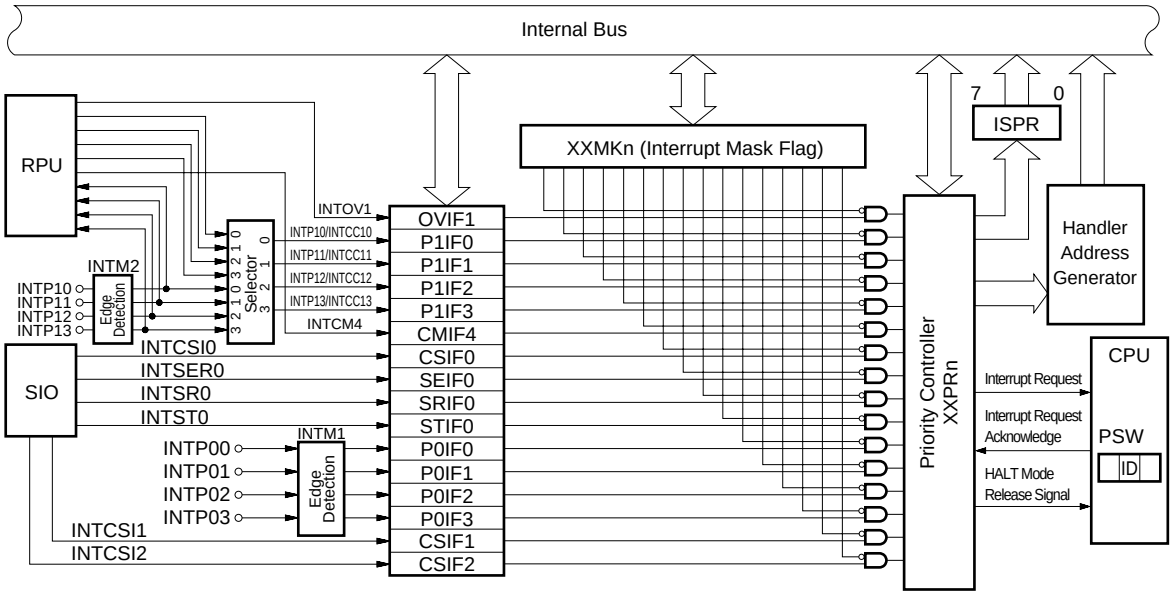
- External device connectable with port pins (using alternate function)
- Wait function
  - Programmable wait function inserting up to 3 states per 2 blocks
  - External wait function effected by $\overline{\text{WAIT}}$ pin
- Idle state inserting function
- Bus arbitration function
- Bus hold function

5. INTERRUPT/EXCEPTION HANDLING

5.1 Features

- Interrupts
  - Non-maskable : 1 source
  - Maskable : 16 sources
  - 8-level programmable priority control
  - Multiplexed processing control according to priority
  - Masking each maskable interrupt request
  - Valid edge specification for external interrupt request
- Exceptions
  - Software exception : 32 sources
  - Exception trap : 1 source (illegal instruction code exception)

5.2 Configuration



XX: Identification name for each peripheral unit (OV, P1, CM, CS, SE, SR, ST, P0, CS)
n : Peripheral unit number (0 to 4)

Table 5-1. Interrupts

Type	Class	Interrupt/Exception Causes				Default Priority	Exception Code	Handler Address	Restore PC
		Name	Control Register	Generation Cause	Generating Unit				
Reset	Interrupt	RESET	—	Reset input	—	—	0000H	00000000H	Undefined
Non-maskable	Interrupt	NMI	—	NMI input	—	—	0010H	00000010H	next PC
Software exception	Exception	TRAP0n[Note]	—	TRAP instruction	—	—	004n[Note]H	00000040H	next PC
	Exception	TRAP1n[Note]	—	TRAP instruction	—	—	005n[Note]H	00000050H	next PC
Exception trap	Exception	ILGOP	—	Illegal instruction code	—	—	0060H	00000060H	next PC
Maskable	Interrupt	INTOV1	OVIC1	Timer 1 overflow	RPU	0	0080H	00000080H	next PC
	Interrupt	INTP10/INTCC10	P1IC0	Match of INTP10 & CC10	Pin/RPU	1	0090H	00000090H	next PC
	Interrupt	INTP11/INTCC11	P1IC1	Match of INTP11 & CC11	Pin/RPU	2	00A0H	000000A0H	next PC
	Interrupt	INTP12/INTCC12	P1IC2	Match of INTP12 & CC12	Pin/RPU	3	00B0H	000000B0H	next PC
	Interrupt	INTP13/INTCC13	P1IC3	Match of INTP13 & CC13	Pin/RPU	4	00C0H	000000C0H	next PC
	Interrupt	INTCM4	CMIC4	Match of CM4	RPU	5	00D0H	000000D0H	next PC
	Interrupt	INTCSI0	CSIC0	CSI0 transmit/receive completion	SIO	6	00E0H	000000E0H	next PC
	Interrupt	INTSER0	SEIC0	UART0 receive error	SIO	7	00F0H	000000F0H	next PC
	Interrupt	INTSR0	SRIC0	UART0 receive completion	SIO	8	0100H	00000100H	next PC
	Interrupt	INTST0	STIC0	UART0 transmit completion	SIO	9	0110H	00000110H	next PC
	Interrupt	INTP00	P0IC0	INTP00 pin	Pin	10	0120H	00000120H	next PC
	Interrupt	INTP01	P0IC1	INTP01 pin	Pin	11	0130H	00000130H	next PC
	Interrupt	INTP02	P0IC2	INTP02 pin	Pin	12	0140H	00000140H	next PC
	Interrupt	INTP03	P0IC3	INTP03 pin	Pin	13	0150H	00000150H	next PC
	Interrupt	INTCSI1	CSIC1	CSI1 transmit/receive completion	SIO	14	0160H	00000160H	next PC
	Interrupt	INTCSI2	CSIC2	CSI2 transmit/receive completion	SIO	15	0170H	00000170H	next PC

Note The "n" in the "Software exception" rows is a value from 0 to FH.

Remarks 1. Default priority: Priority used when two or more maskable interrupt requests having the same priority are simultaneously generated. 0 indicates the highest priority.

Restore PC: PC value saved to EIPC or FEPC when interrupt/exception processing is started. However, the restore PC value saved if an interrupt is accepted while the DIVH (division) instruction is being executed is the PC value of the current instruction (DIVH).

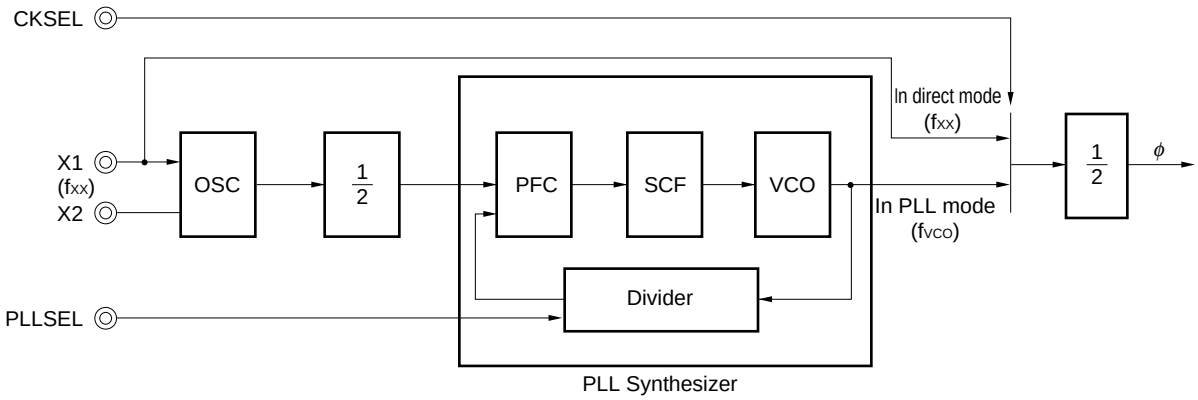
2. The execution address of an illegal instruction when an illegal instruction code exception occurs can be calculated as (restore PC–4).

6. CLOCK GENERATOR

6.1 Features

- Multiply function by PLL clock synthesizer ($f_{XX} = \phi$ or $f_{XX} = \phi/5$)
- Direct mode directly to input external clock
- Power save mode
  - HALT mode
  - IDLE mode
  - Software STOP mode
- Clock output inhibit function

6.2 Configuration



f_{VCO} : VCO oscillation frequency (= 2 • f_{XX} when PLLSEL = 0), (= 10 • f_{XX} when PLLSEL = 1)
ϕ : Internal system clock frequency (= 1/2 • f_{VCO} : in PLL mode)
Internal system clock frequency (= 1/2 • f_{XX} : in direct mode)
OSC : Oscillator (supported in PLL mode only)
PFC : Phase Frequency Comparator
SCF : Switched Capacitor Filter
VCO : Voltage Controlled Oscillator
Divide ratio of the divider (= 1/4 when PLLSEL = 0), (= 1/20 when PLLSEL = 1)

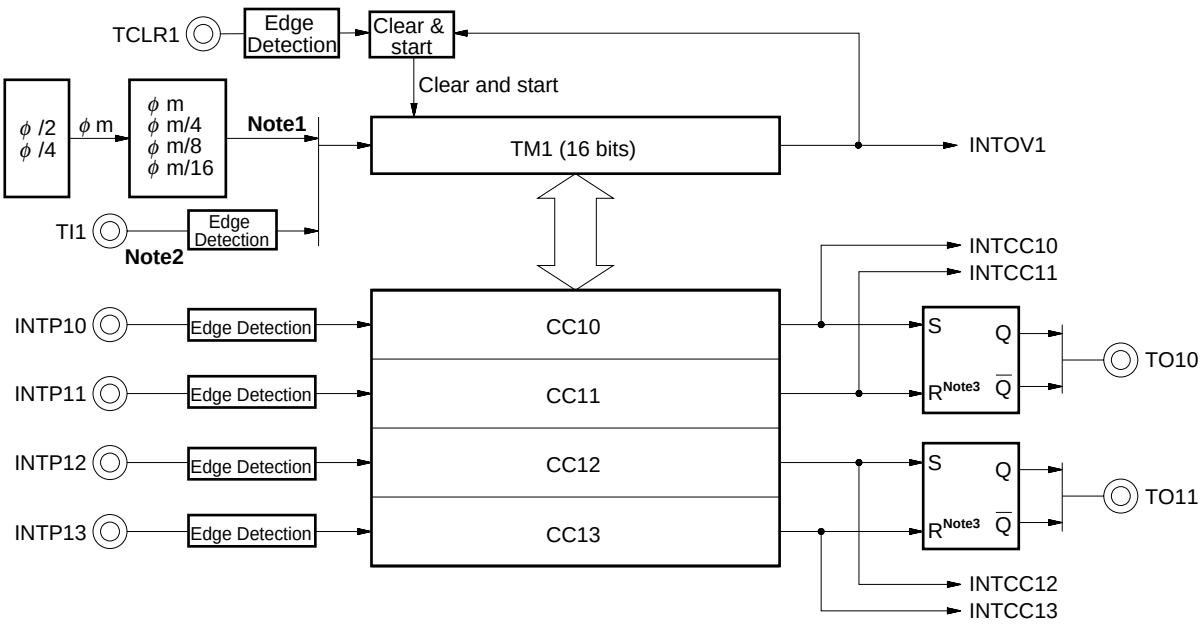
7. TIMER/COUNTER FUNCTION (REAL-TIME PULSE UNIT)

7.1 Features

- Pulse interval and frequency measurement and output of programmable pulse
  - 16-bit measurement possible
  - Pulse can be generated in various shapes (interval pulse, one-shot pulse)
- Timer 1
  - 16-bit timer/event counter
  - Sources of count clock: 2 types (divided system clock or external pulse input)
  - Capture/compare registers: 4
  - Count clear pin: TCLR1
  - Interrupt sources: 5
  - External pulse output: 2
- Timer 4
  - 16-bit interval timer
  - Count clock selected from divided system clock
  - Compare register: 1
  - Interrupt source: 1

7.2 Configuration

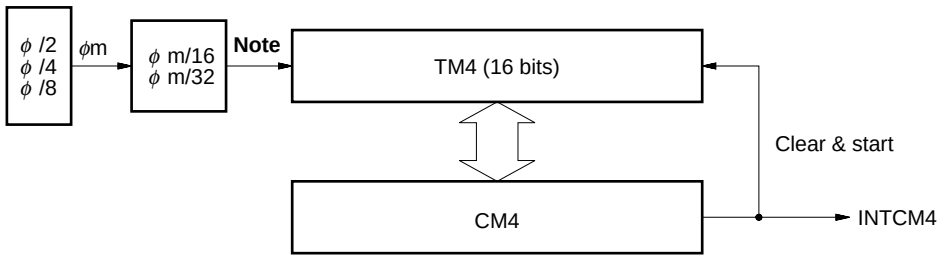
(1) Timer 1 (16-bit timer/event counter)



Notes **1.** Internal count clock
2. External count clock
3. Gives priority to reset

Remark φ indicates the system clock.

(2) Timer 4 (16-bit interval timer)



Note Internal count clock

Remark φ indicates the system clock.

8. SERIAL INTERFACE FUNCTION (SIO)

8.1 Features

The μPD703002 is provided with four independent serial interface channels.

(1) Asynchronous serial interface (UART): 1 channel
(2) Clocked synchronous serial interface (CSI0 to CSI2): 3 channels

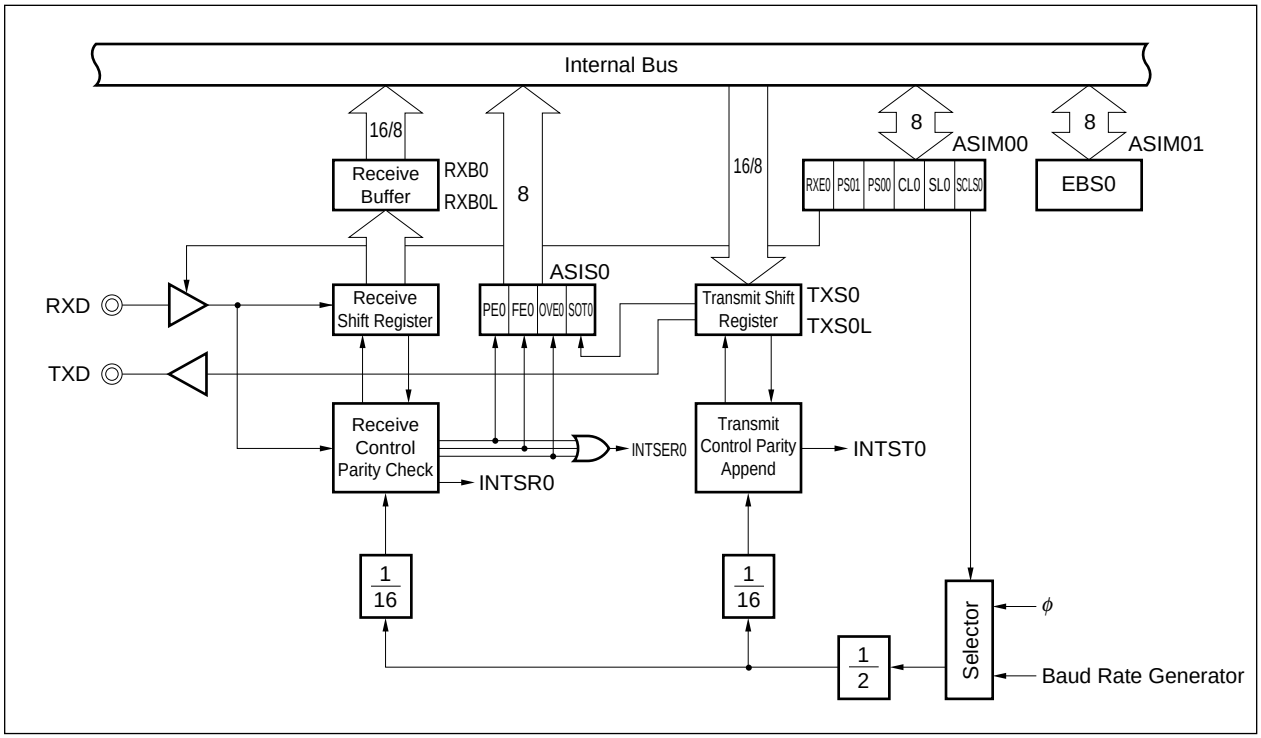
8.2 Asynchronous Serial Interface (UART)

8.2.1 Features

- Transfer rate: 110 to 38400 bps (with BRG, when ϕ = 25 MHz)
  Up to 781 Kbps (with ϕ/2, when ϕ = 25 MHz)
- Full-duplex communication
- 2-pin configuration
  TXD: Transmit data output pin
  RXD: Receive data input pin
- Receive error detection function
  - Parity error
  - Framing error
  - Overrun error
- Three interrupt sources
  - Receive error interrupt (INTSER0)
  - Reception completion interrupt (INTSR0)
  - Transmission completion interrupt (INTST0)
- Character length of transmission/reception data is specified by setting ASIM00, ASIM01 register.
- Character length : 7, 8 bits
  9 bits (with extended bit appended)
- Parity function : odd, even, 0, none
- Transmission stop bit: 1 or 2 bits
- Baud rate generator

Remark ϕ indicates the system clock

8.2.2 Configuration



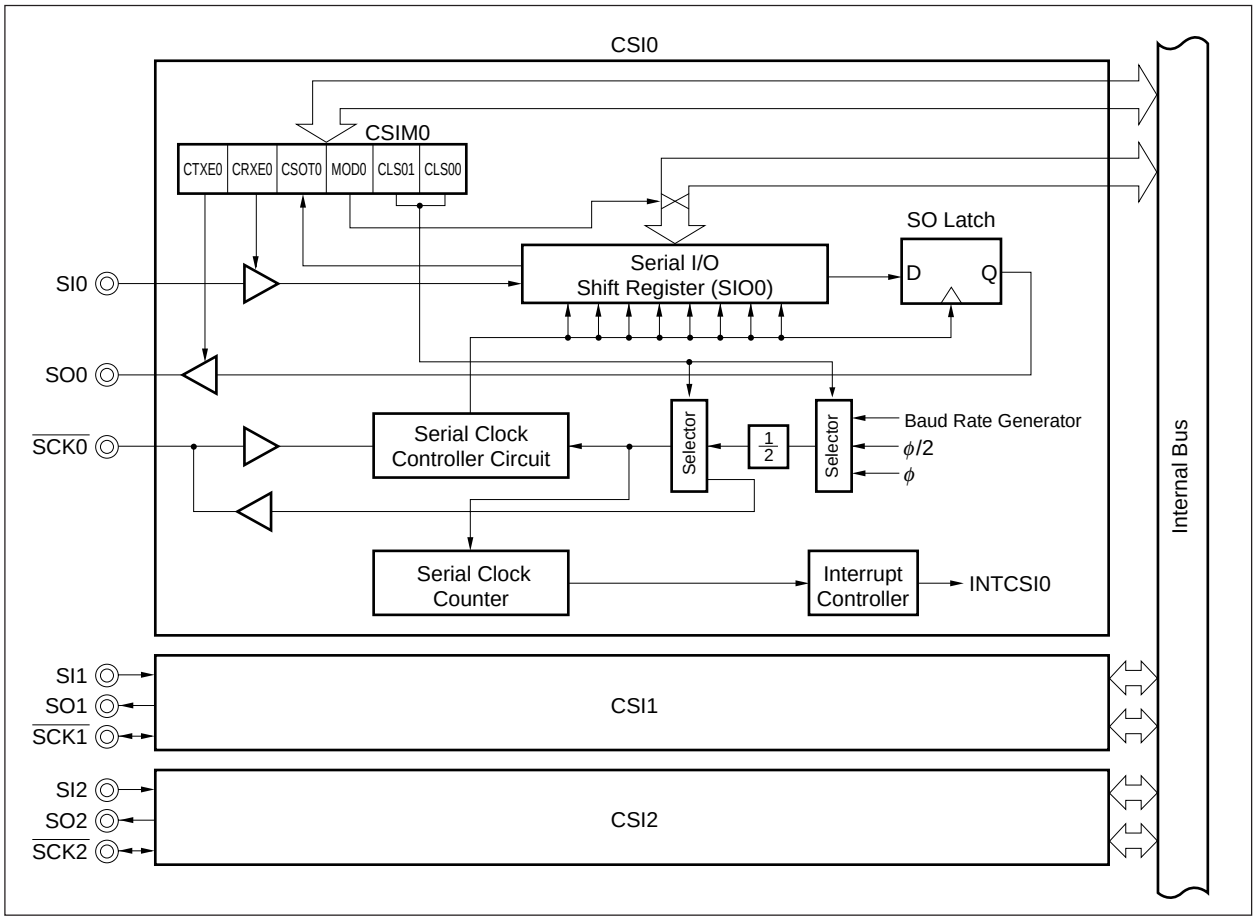
8.3 Clocked Serial Interface 0 to 2 (CSI0 to CSI2)

8.3.1 Features

- Number of channels: 3 (CSIn)
- High-speed transfer rate
  6.25 Mbps MAX. (with ϕ/2, ϕ = 25 MHz)
- Half-duplex communication
- Data length of 8 bits
- MSB first/LSB first can be switched for data
- Selection of external serial clock input/internal serial clock output
- Three pins used
  SOn : Serial data output pin
  SIn : Serial data input pin
  $\overline{\text{SCKn}}$: Serial clock I/O pin
- Three interrupt sources
  - Interrupt request signal (INTCSIn)

Remark **1**. ϕ indicates the system clock.
2. n = 0 to 2

8.3.2 Configuration

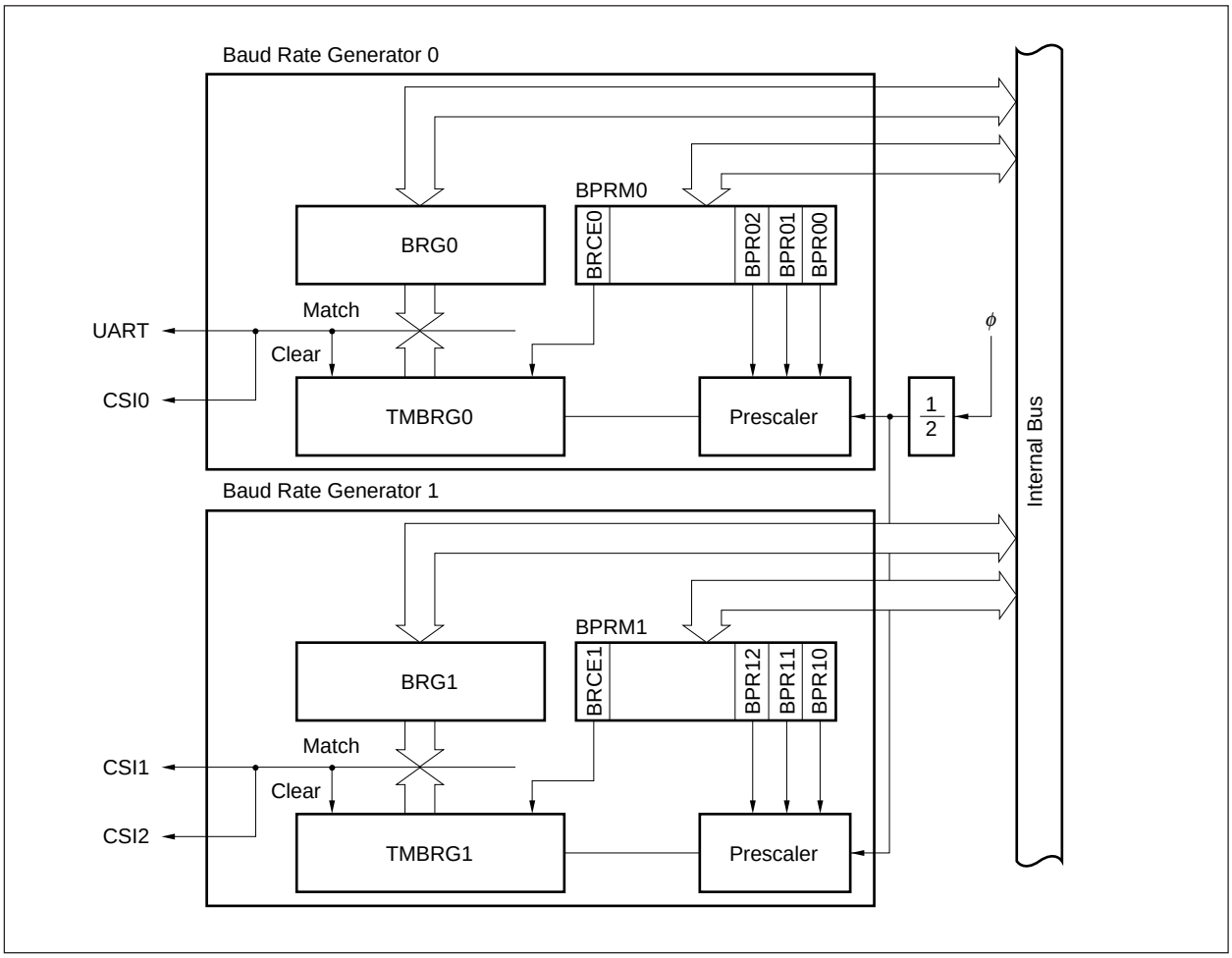


8.4 Baud Rate Generator 0, 1 (BRG0, BRG1)

8.4.1 Features

- Serial clock selectable from baud rate generator output and ϕ (system clock)
- Same baud rate for transmission/reception

8.4.2 Configuration



9. PORT FUNCTION

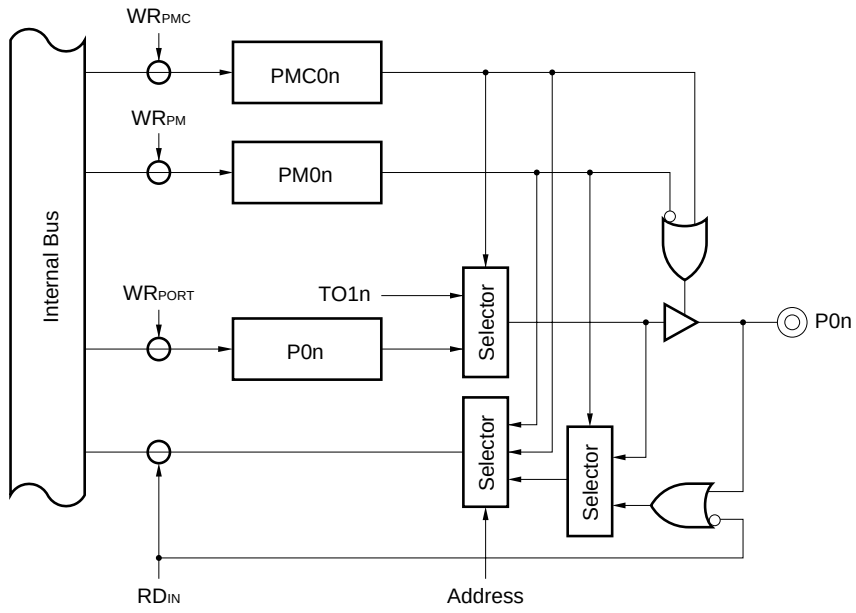
9.1 Features

The ports of the μPD703002 have the following features:

- Number of port pins
  - Input port: 1
  - I/O port: 67
- Shared with I/O pins of other peripheral functions
- Input/output specifiable bitwise
- Noise elimination
- Edge detection

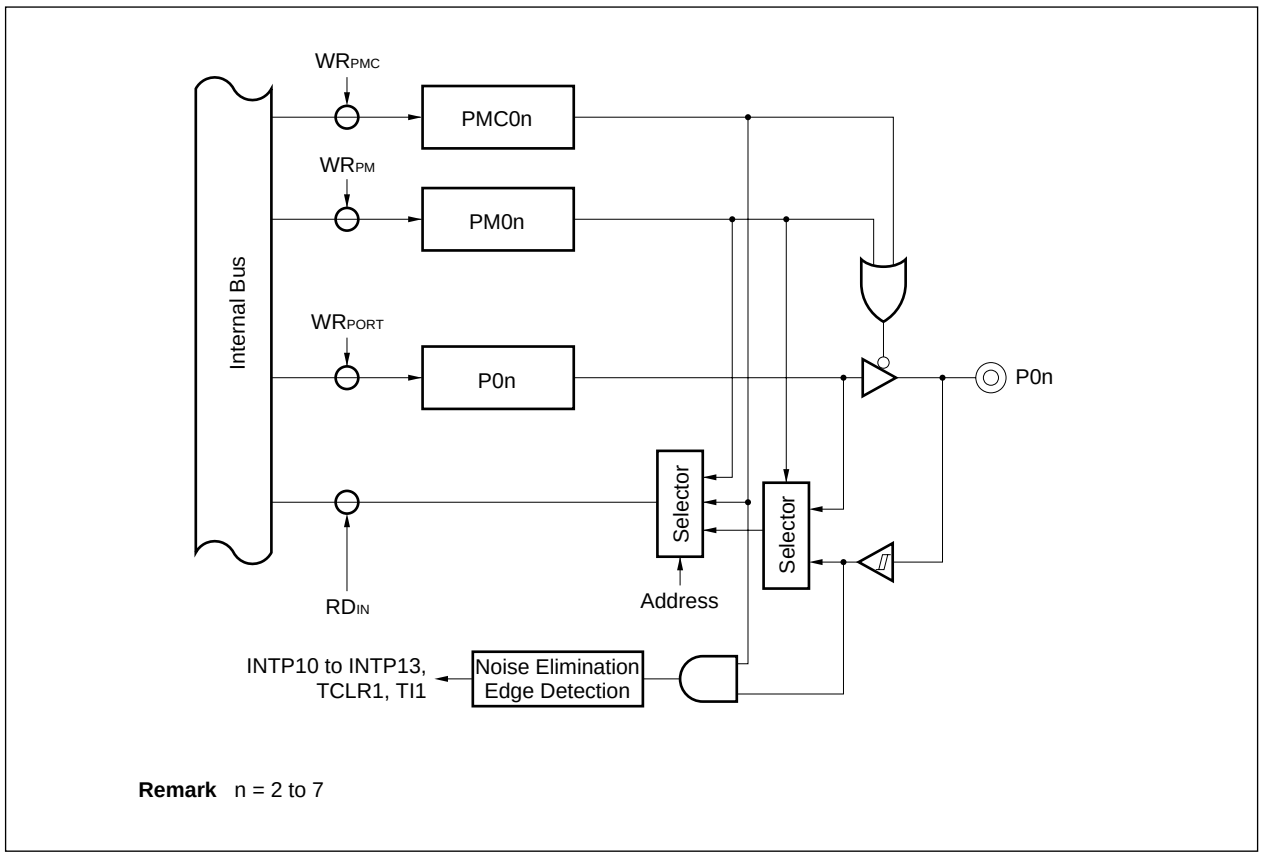
9.2 Configuration

Figure 9-1. Block Diagram of P00, P01 (Port 0)



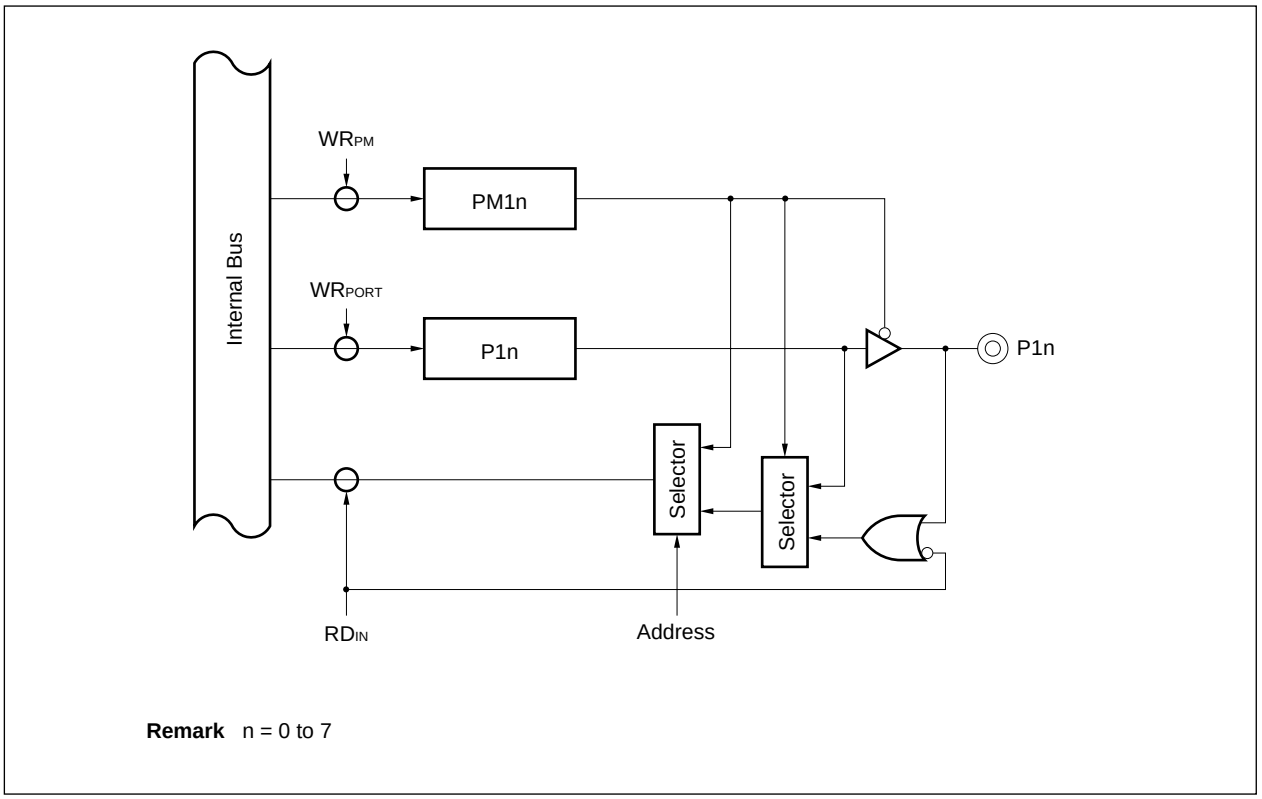
Remark n = 0, 1

Figure 9-2. Block Diagram of P02 to P07 (Port 0)



Remark n = 2 to 7

Figure 9-3. Block Diagram of P10 to P17 (Port 1)



Remark n = 0 to 7

Figure 9-4. Block Diagram of P20 (Port 2)

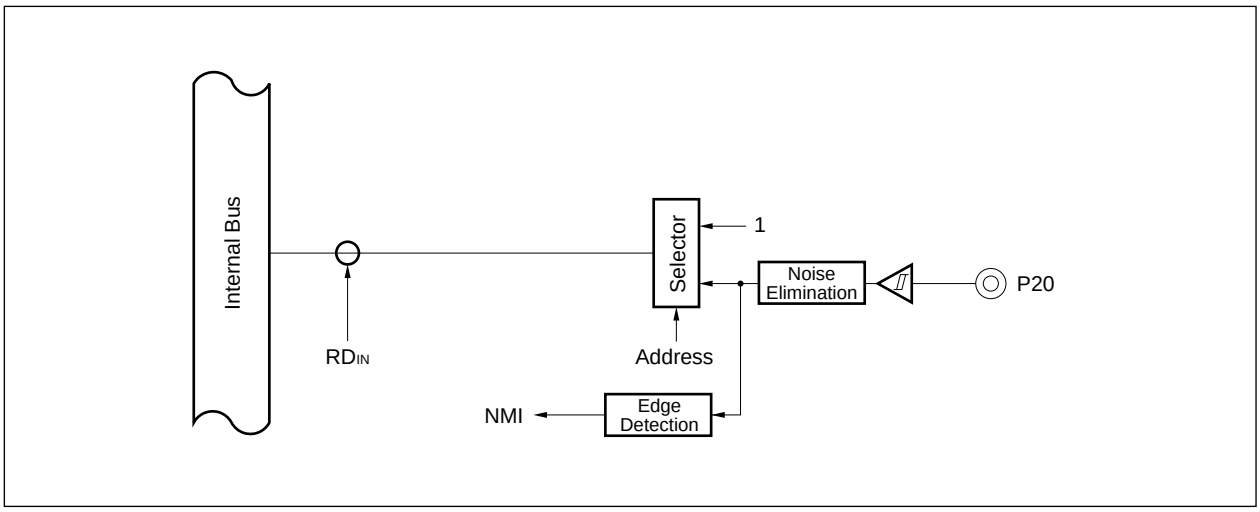
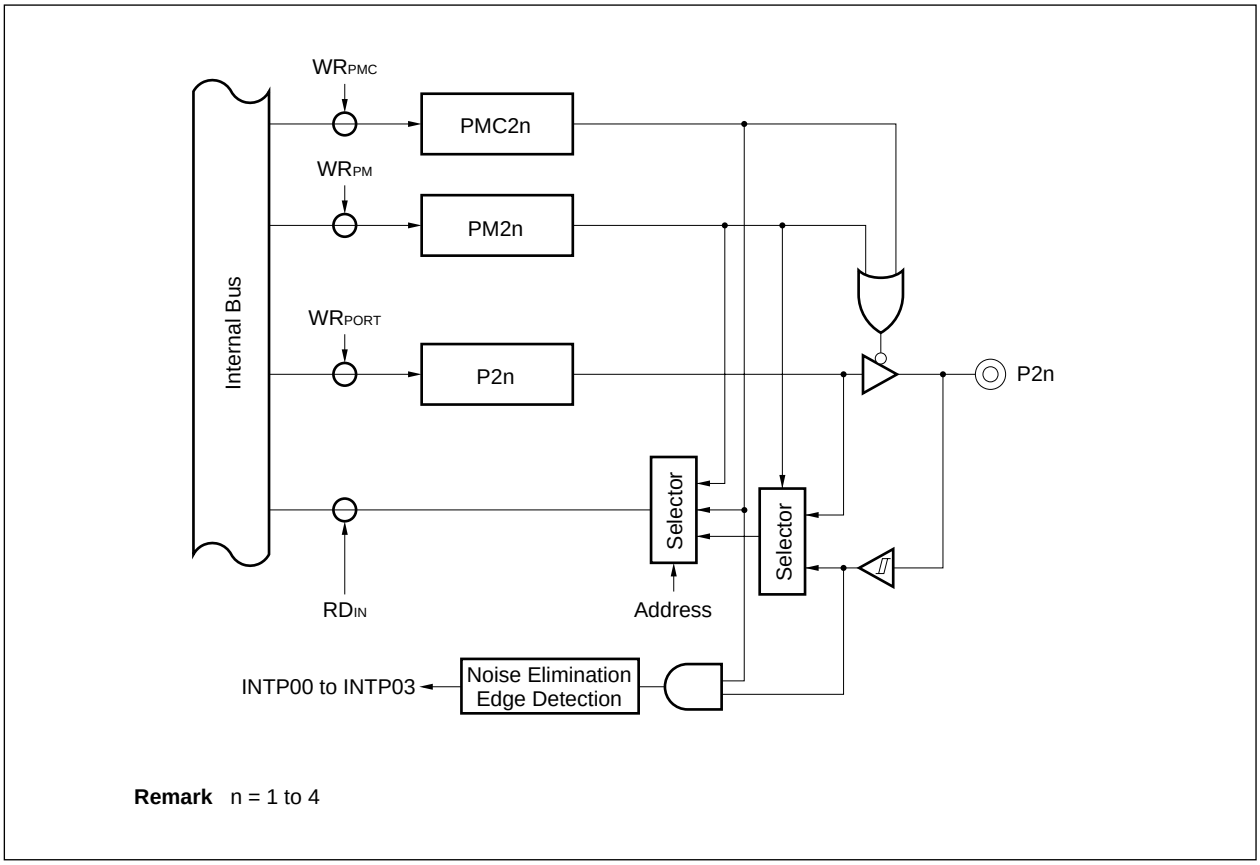


Figure 9-5. Block Diagram of P21 to P24 (Port 2)



Remark n = 1 to 4

Figure 9-6. Block Diagram of P25 (Port 2)

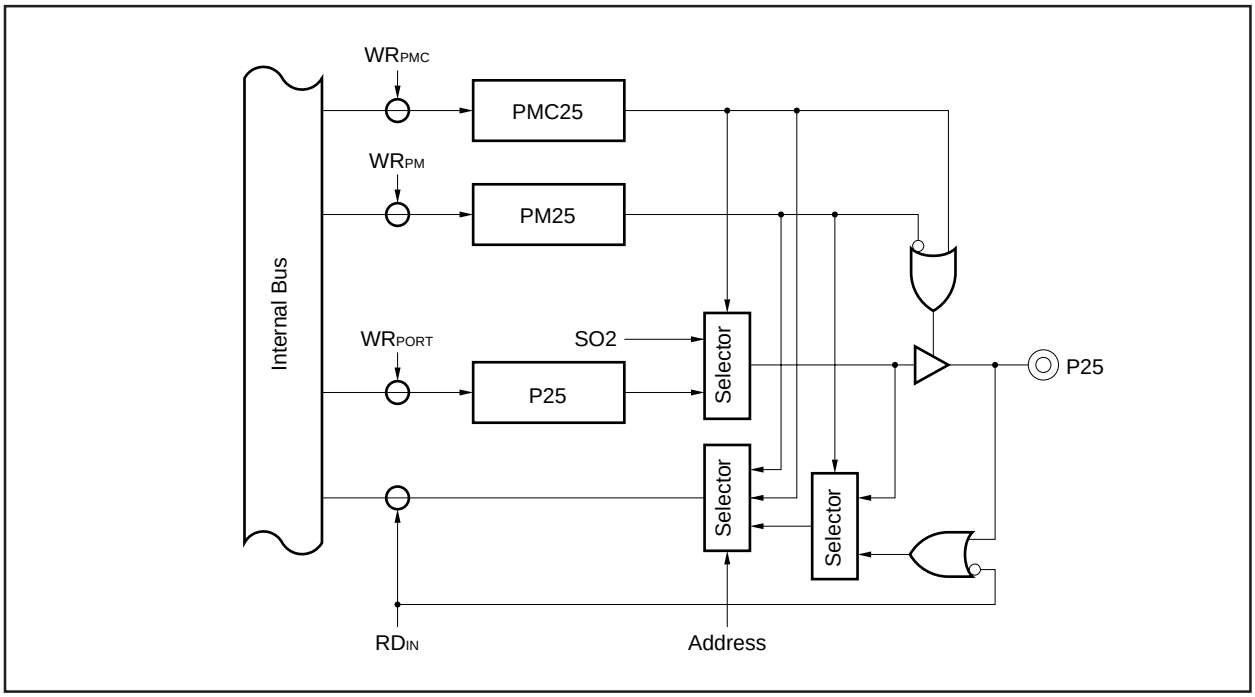


Figure 9-7. Block Diagram of P26 (Port 2)

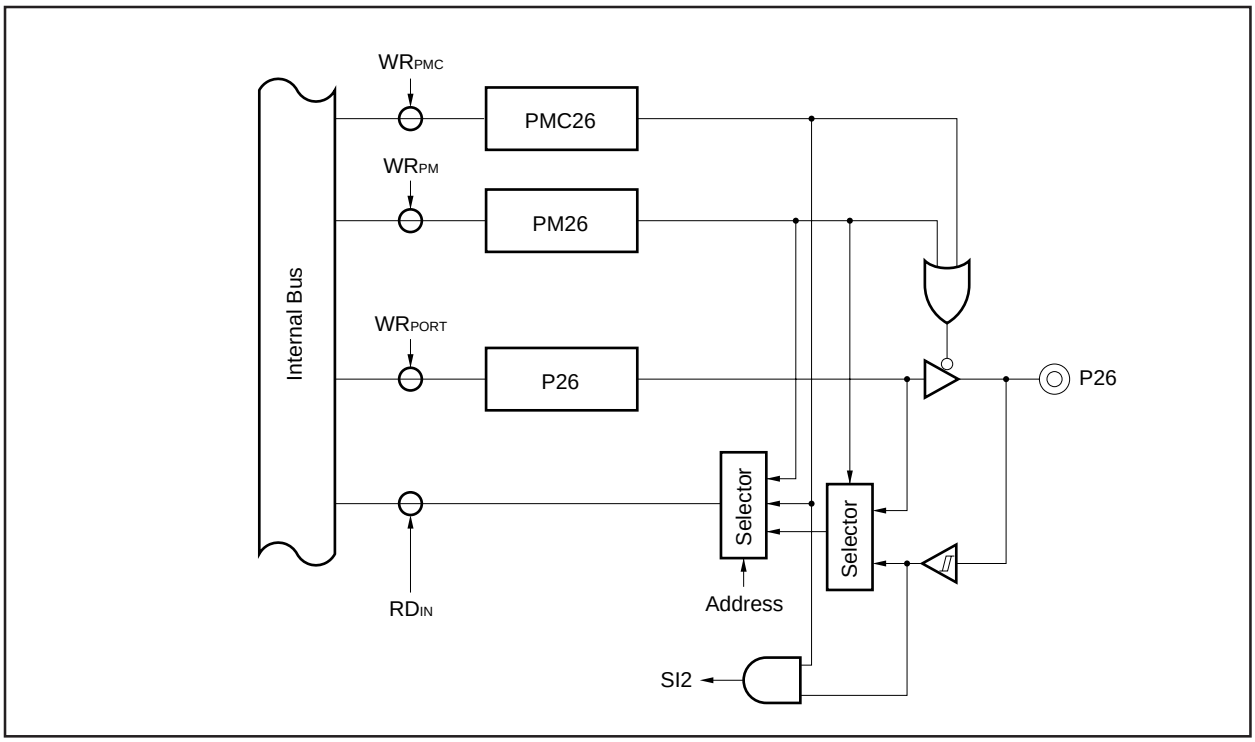


Figure 9-8. Block Diagram of P27 (Port 2)

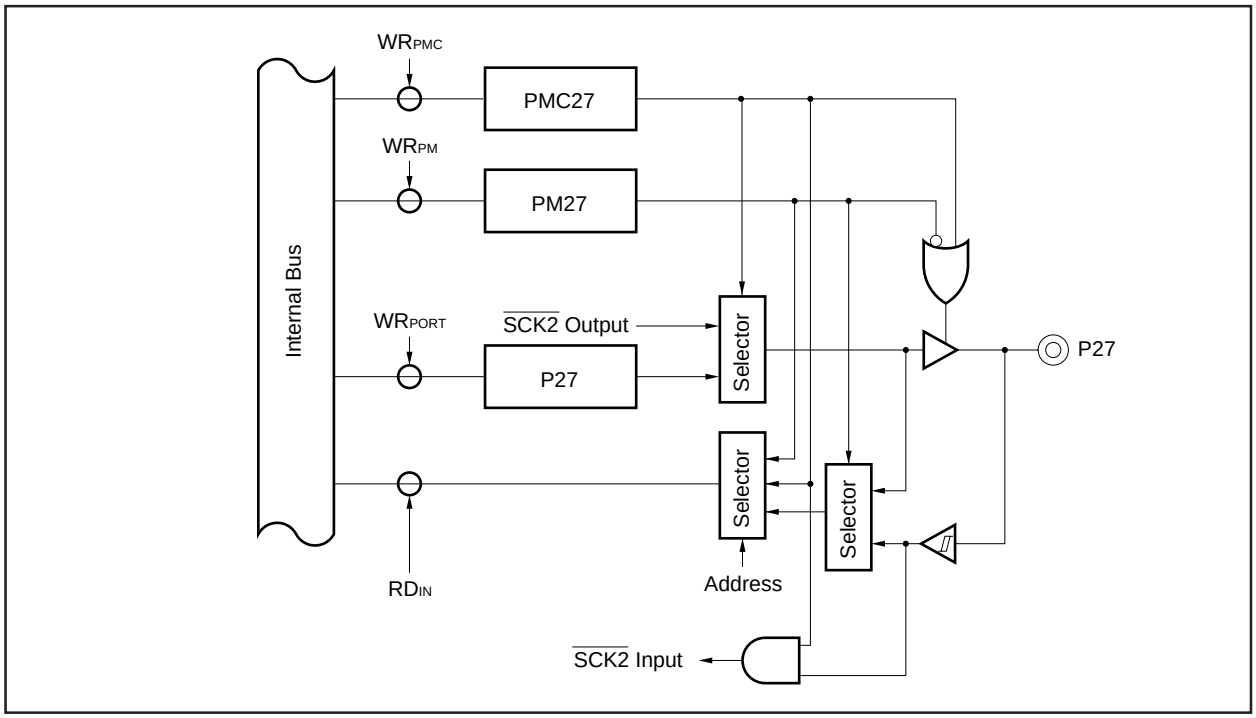
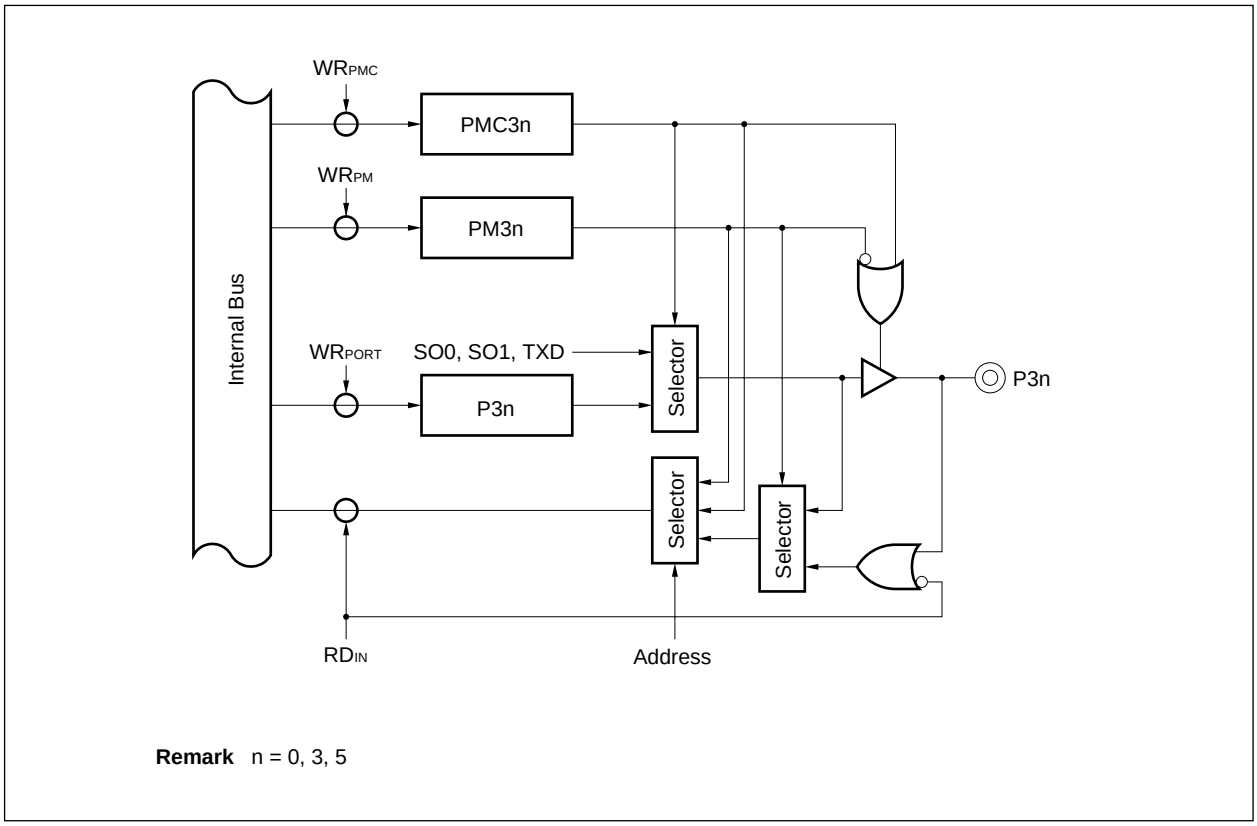
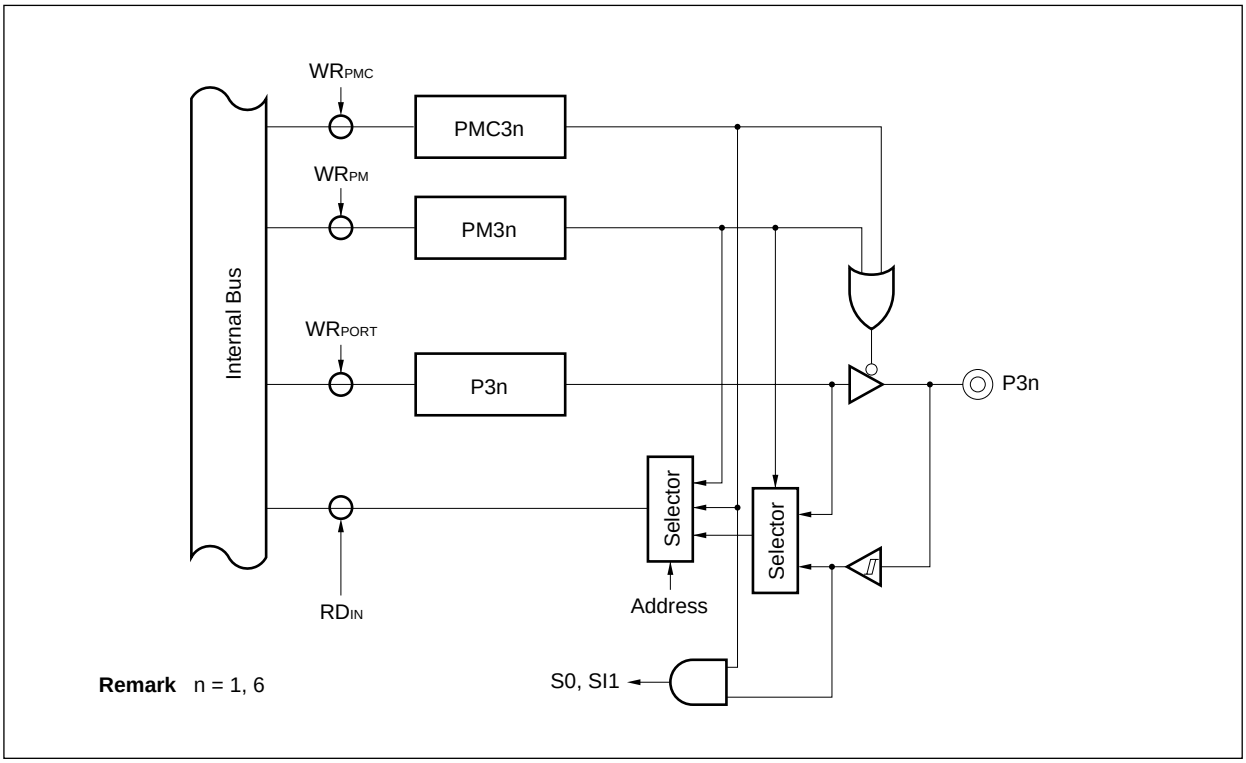


Figure 9-9. Block Diagram of P30, P33, P35 (Port 3)



Remark n = 0, 3, 5

Figure 9-10. Block Diagram of P31, P36 (Port 3)



Remark n = 1, 6

Figure 9-11. Block Diagram of P32, P37 (Port 3)

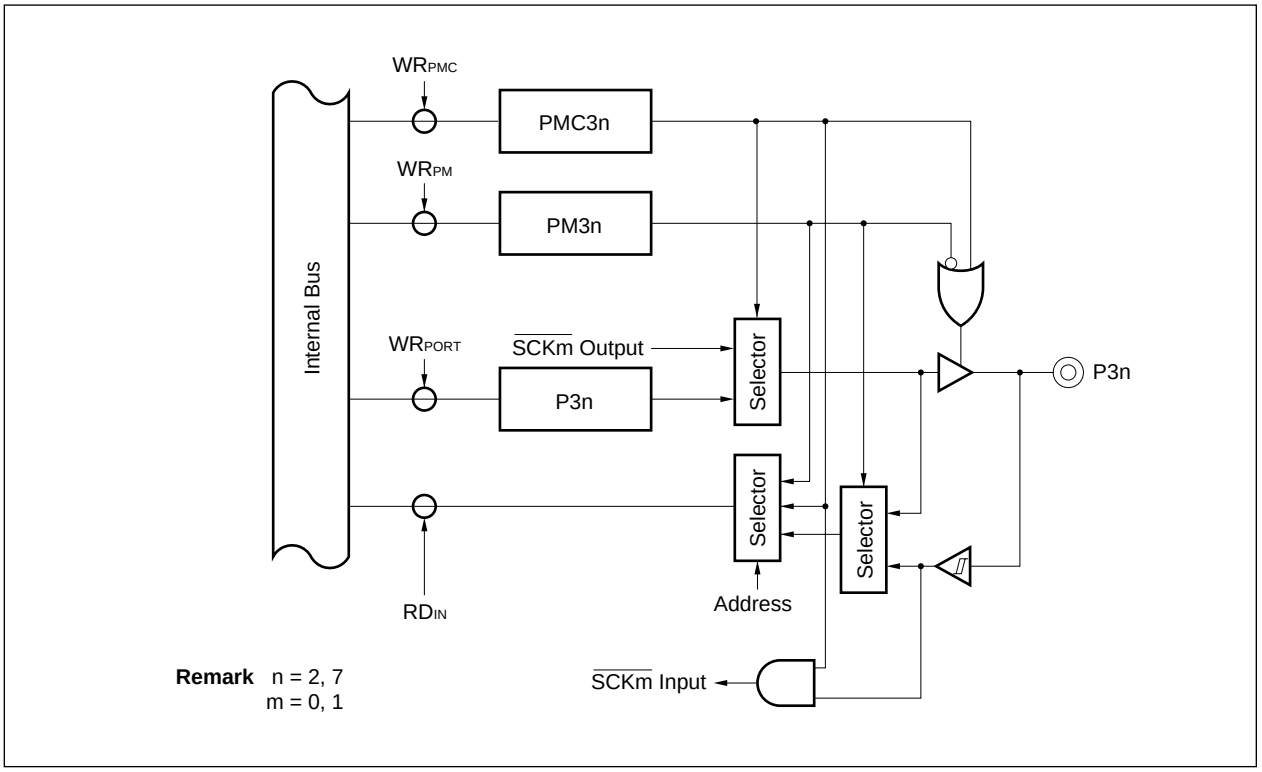


Figure 9-12. Block Diagram of P34 (Port 3)

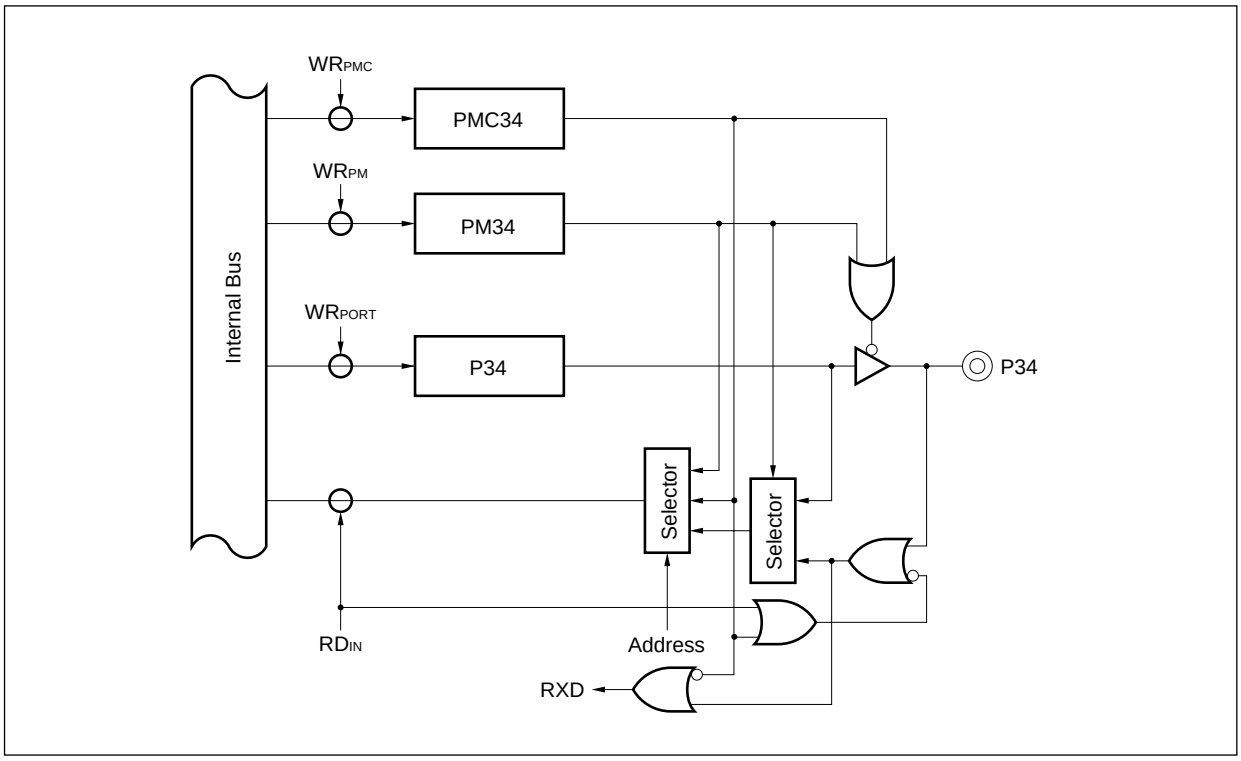
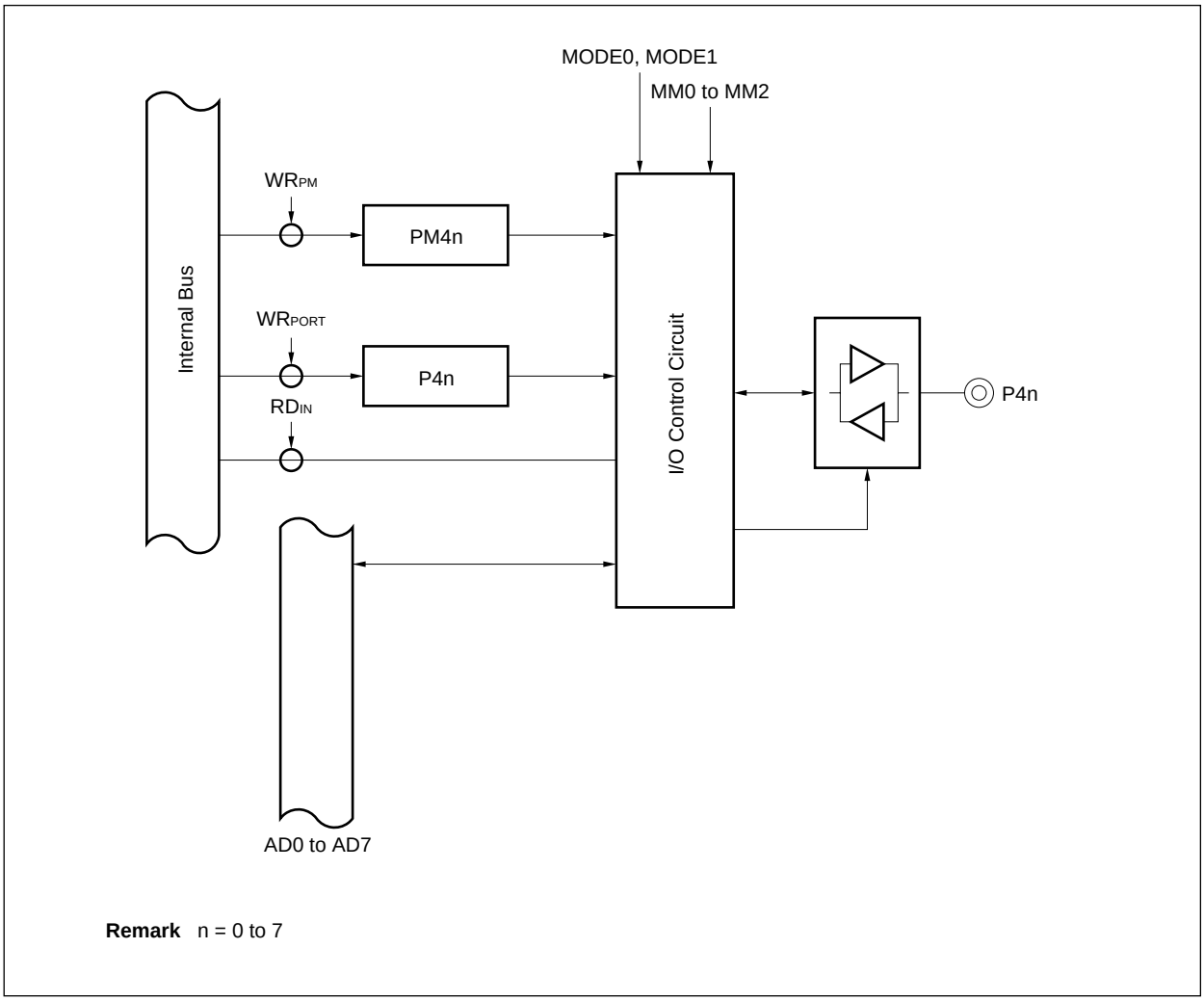
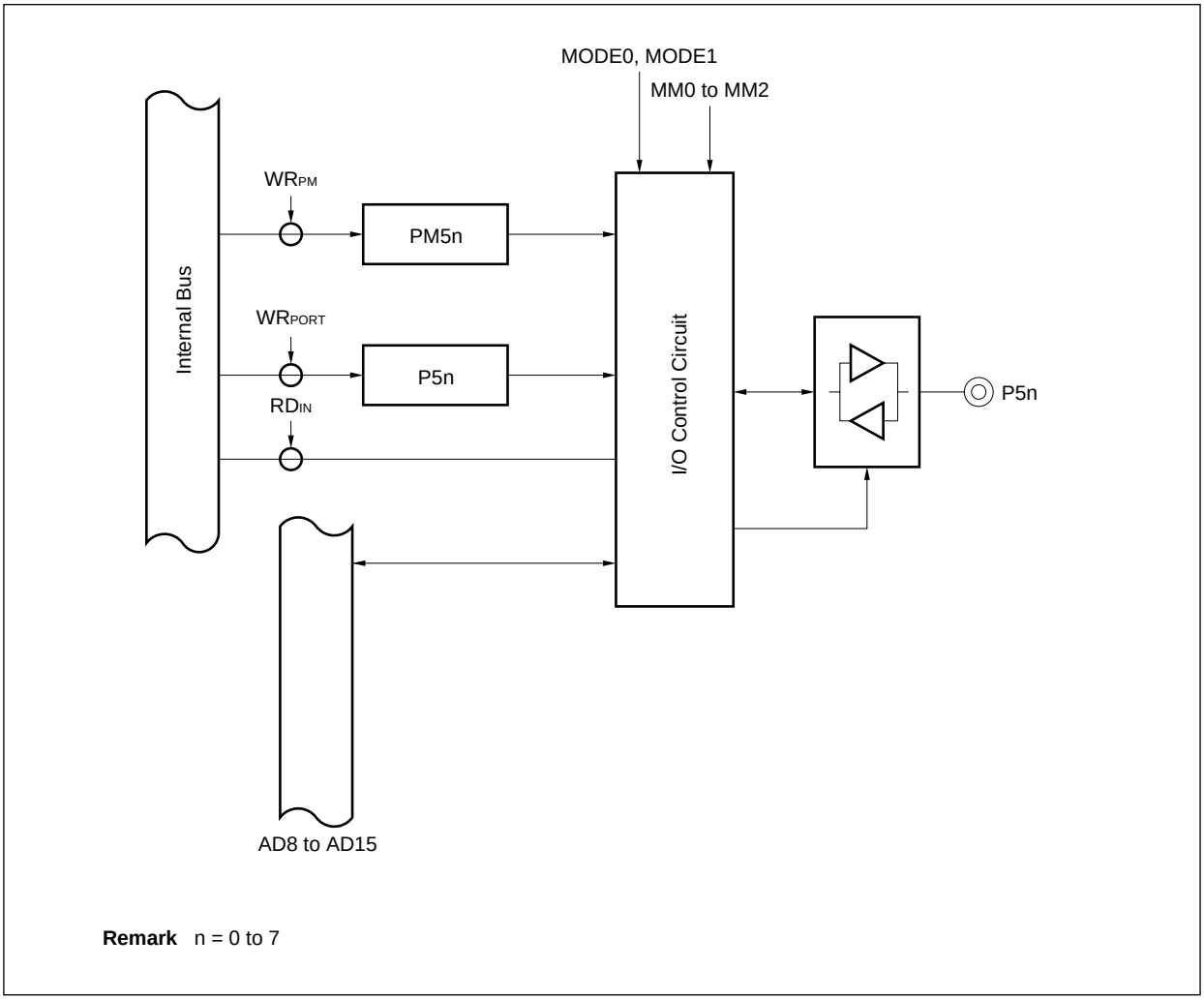


Figure 9-13. Block Diagram of P40 to P47 (Port 4)



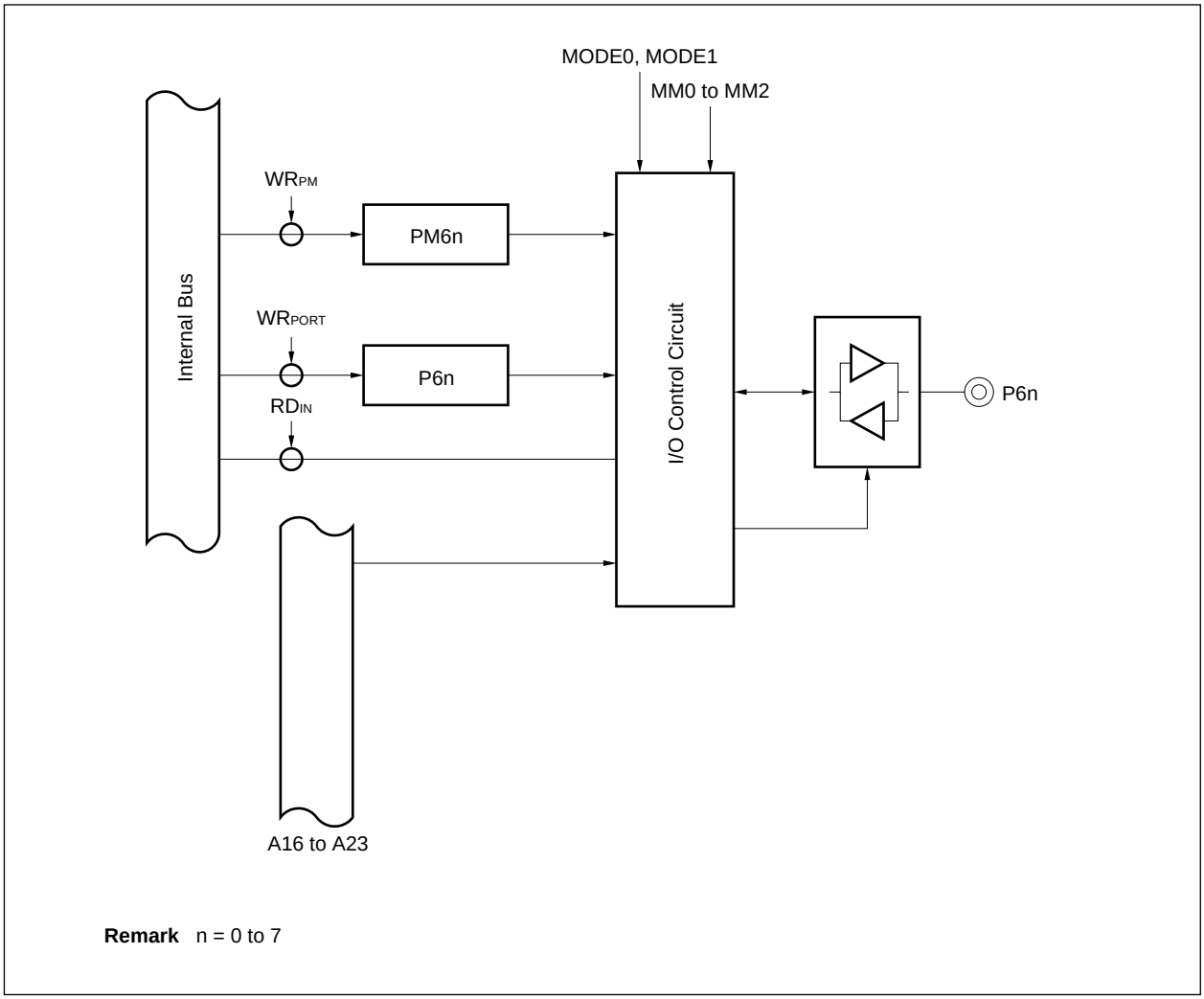
Remark n = 0 to 7

Figure 9-14. Block Diagram of P50 to P57 (Port 5)



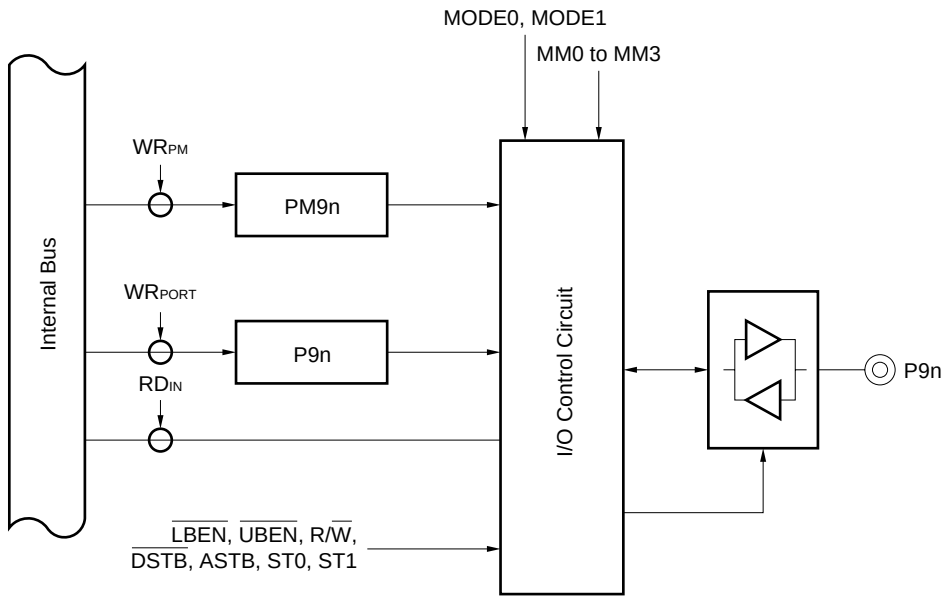
Remark n = 0 to 7

Figure 9-15. Block Diagram of P60 to P67 (Port 6)



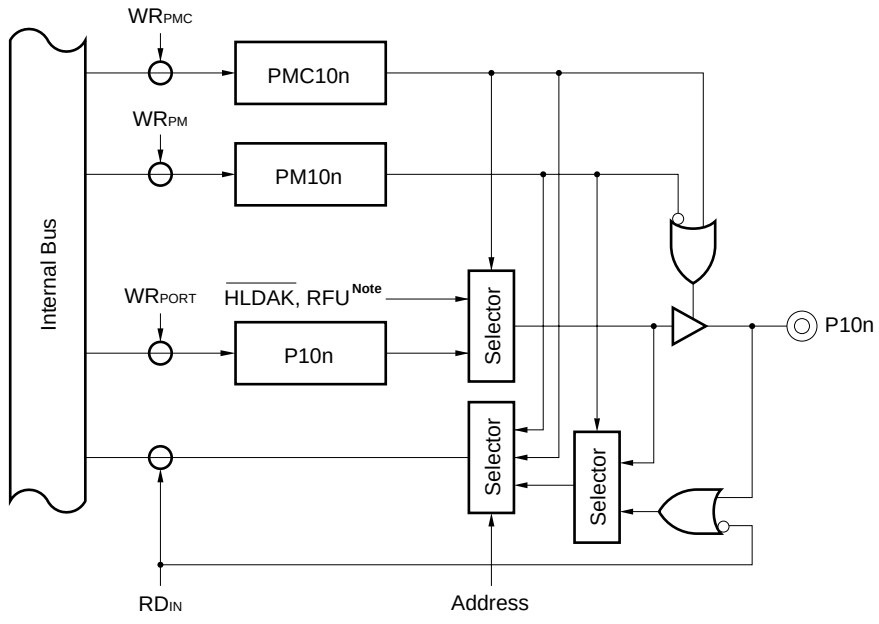
Remark n = 0 to 7

Figure 9-16. Block Diagram of P90 to P97 (Port 9)



Remark n = 0 to 7

Figure 9-17. Block Diagram of P100, P103 (Port 10)



Note RFU is undefined value.

Remark n = 0, 3

Figure 9-18. Block Diagram of P101 (Port 10)

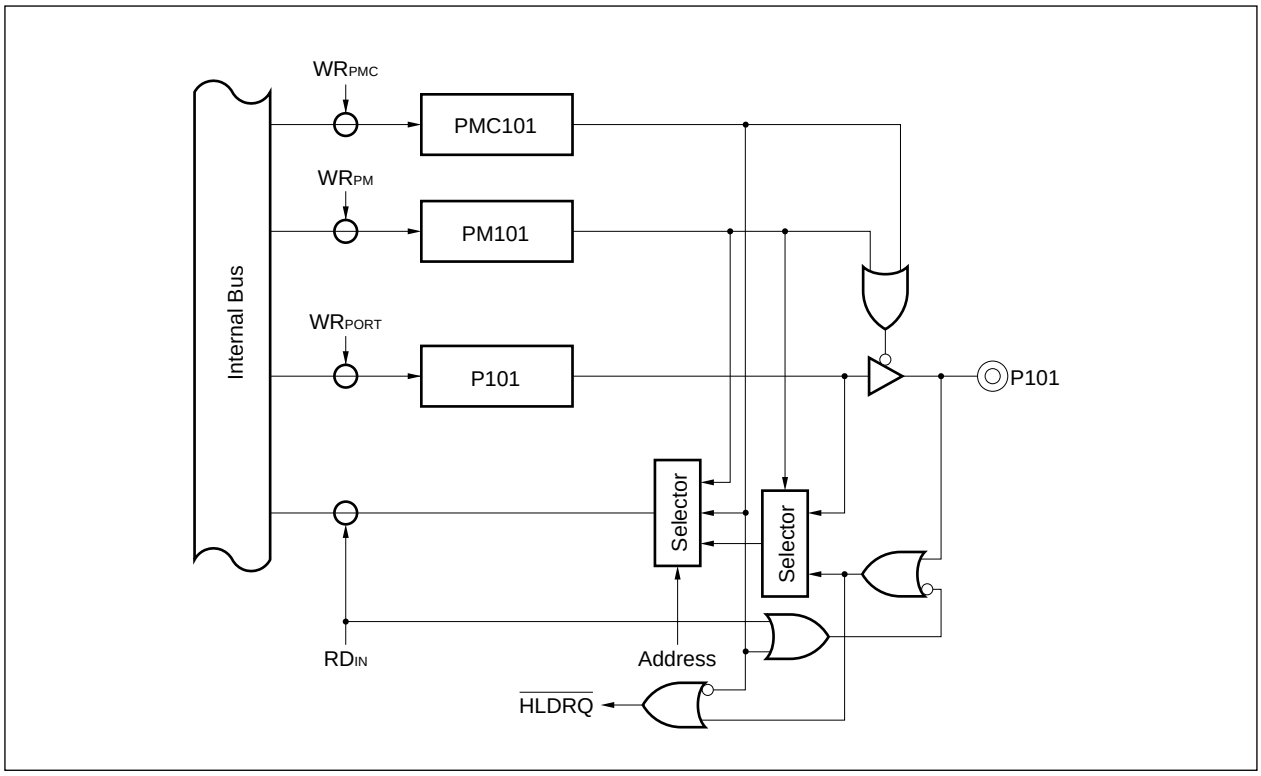
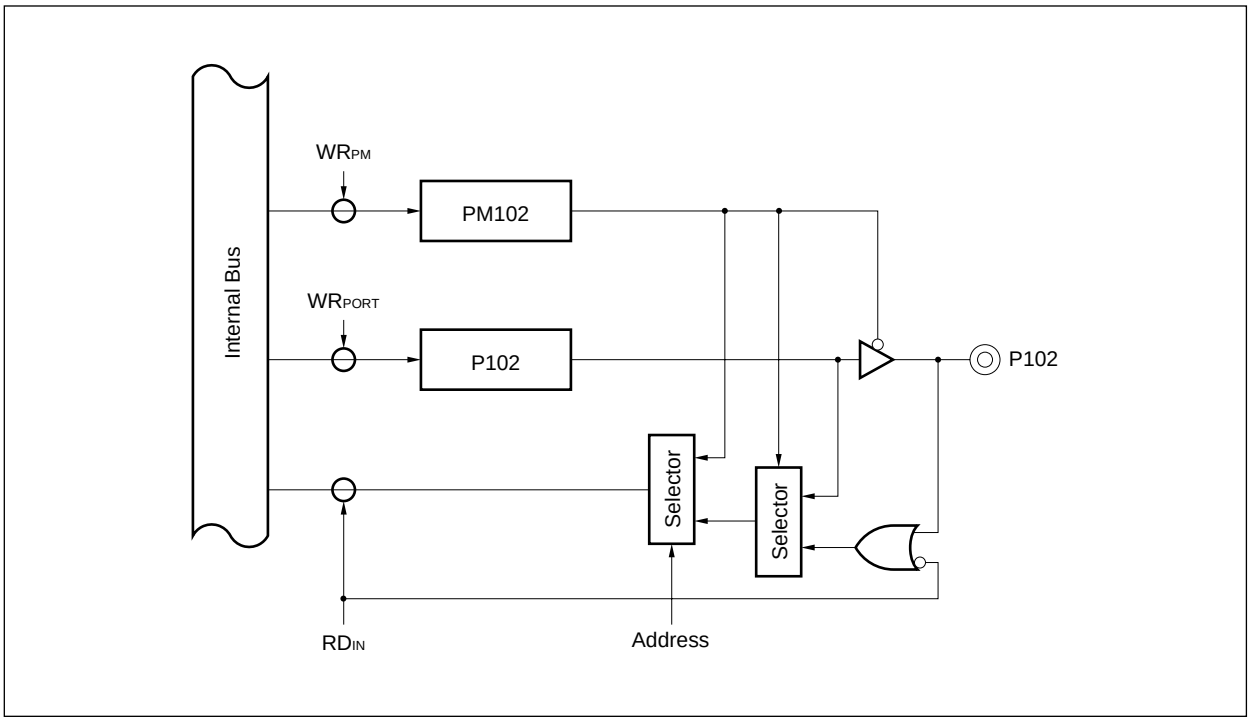


Figure 9-19. Block Diagram of P102 (Port 10)



10. RESET FUNCTION

When the $\overline{\text{RESET}}$ signal is made low, the system is reset, and the on-chip hardware units are initialized.

The reset status is cleared when the $\overline{\text{RESET}}$ signal is made high, and the CPU starts executing the program. Initialize the contents of each register in the program as necessary.

10.1 Features

- Noise elimination circuit of analog delay (60 to 220 ns) provided to the reset pin

11. INSTRUCTION SET

11.1 Instruction Set List

- **How to read instruction set list**

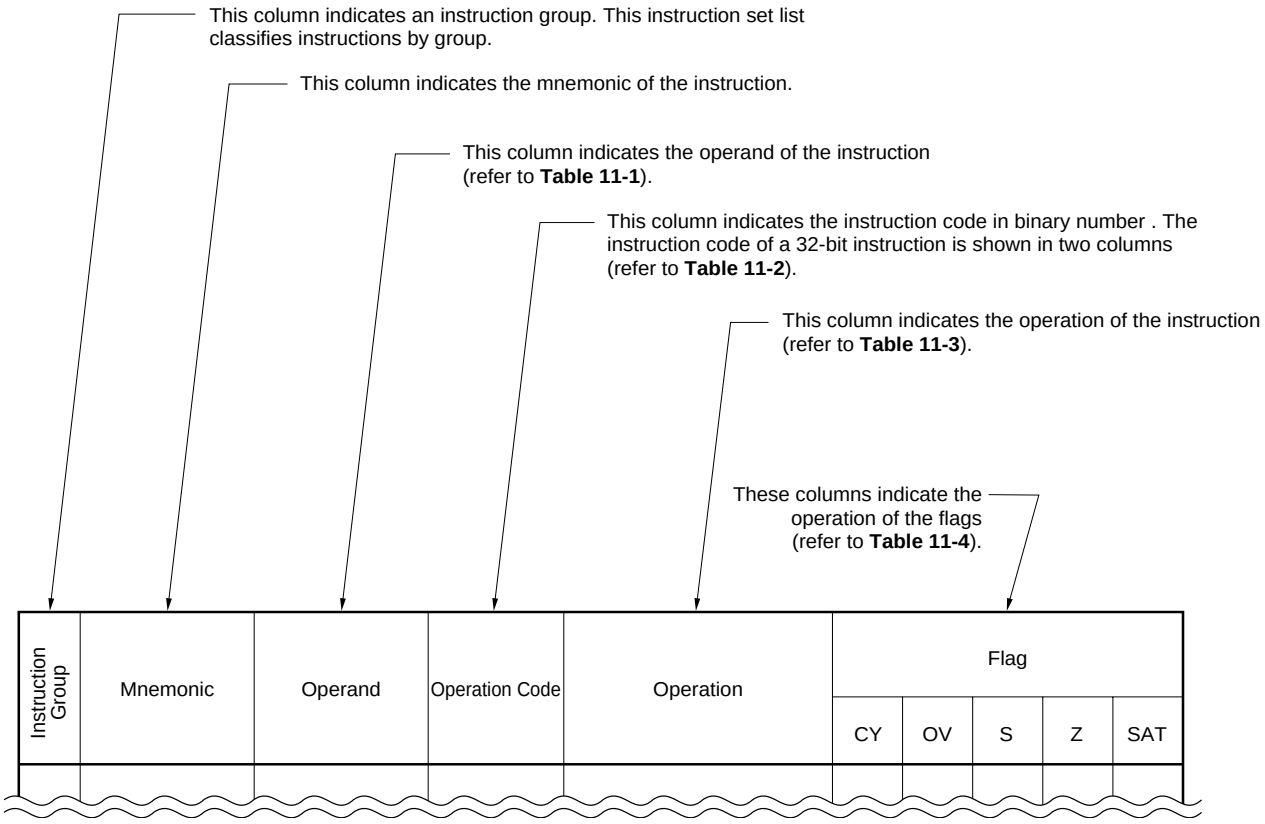


Table 11-1. Symbols Shown in "Operand" Column

Symbol	Description
reg1	General register (used as source register)
reg2	General register (mainly used as destination register. Some are also used as source registers)
ep	Element pointer
bit#3	3-bit data for bit number specification
immX	X-bit immediate
dispX	X-bit displacement
regID	System register number
vector	5-bit data specifying trap vector (00H through 1FH)
cccc	4-bit data indicating condition code

Table 11-2. Symbols Shown in “Operation Code” Column

Symbol	Meaning
R	1-bit-wise data of code specifing reg1 or regID
r	1-bit-wise data of code specifing reg2
d	1-bit-wise data of displacement
i	1-bit-wise data of immediate
cccc	4-bit data indicating condition code
bbb	3-bit data specifing bit number

Table 11-3. Symbols Shown in "Operation" Column

Symbol	Meaning
←	Assignment
GR [ ]	General register
SR [ ]	System register
zero-extend (n)	Zero-extends "n" to word length
sign-extend (n)	Sign-extends "n" to word length
load-memory (a, b)	Reads data of size "b" from address "a"
store-memory (a, b, c)	Writes data "b" of size "c" to address "a"
load-memomy-bit (a, b)	Reads bit "b" of address "a"
store-memory-bit (a, b, c)	Writes "c" to bit "b" of address "a"
saturated (n)	Performs saturated processing of n (n is 2's complement) "n" indicates result of operation. If "n" ≥ 7FFFFFFFH, 7FFFFFFFH If "n" ≤ 80000000H, 80000000H
result	Reflects result on flag
Byte	Byte (8 bits)
Halfword	Halfword (16 bits)
Word	Word (32 bits)
+	Add
–	Subtract
||	Bit concatenation
×	Multiply
÷	Divide
AND	Logical product
OR	Logical sum
XOR	Exclusive logical sum
NOT	Logical negation
logically shift left by	Logical left shift
logically shift right by	Logical right shift
arithmetically shift right by	Arithmetic right shift

Table 11-4. Symbols Shown in "Flag" Column

Identifier	Meaning
(blank)	Not affected
0	Cleared to 0
×	Set or cleared according to result
R	Value once saved is restored

Table 11-5. Condition Codes

Condition Name (cond)	Condition Code (cccc)	Conditional Expression	Meaning
V	0000	OV = 1	Overflow
NV	1000	OV = 0	No overflow
C/L	0001	CY = 1	Carry Lower (Less than)
NC/NL	1001	CY = 0	No carry Not lower (Greater than or equal)
Z/E	0010	Z = 1	Zero Equal
NZ/NE	1010	Z = 0	Not zero Not equal
NH	0011	(CY OR Z) = 1	Not higher (Less than or equal)
H	1011	(CY OR Z) = 0	Higher (Greater than)
N	0100	S = 1	Negative
P	1100	S = 0	Positive
T	0101	–	Always (unconditional)
SA	1101	SAT = 1	Saturated
LT	0110	(S XOR OV) = 1	Less than signed
GE	1110	(S XOR OV) = 0	Greater than or equal signed
LE	0111	((S XOR OV) OR Z) = 1	Less than or equal signed
GT	1111	((S XOR OV) OR Z) = 0	Greater than signed

Instruction Set List

Instruction Group	Mnemonic	Operand	Operation Code	Operation	Flag				
					CY	OV	S	Z	SAT
Load/store	SLD.B	disp7[ep], reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr, Byte))					
	SLD.H	disp8[ep], reg2	rrrrr1000ddddddd **Note 1**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr, Halfword))					
	SLD.W	disp8[ep], reg2	rrrrr1010ddddddd0 **Note 2**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr, Word)					
	LD.B	disp16[reg1], reg2	rrrrr111000RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr, Byte))					
	LD.H	disp16[reg1], reg2	rrrrr111001RRRRR ddddddddddddddd0 **Note 3**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr, Halfword))					
	LD.W	disp16[reg1], reg2	rrrrr111001RRRRR ddddddddddddddd1 **Note 3**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←Load-memory(adr, Word)					
	SST.B	reg2, disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr, GR[reg2], Byte)					
	SST.H	reg2, disp8[ep]	rrrrr1001ddddddd **Note 1**	adr←ep+zero-extend(disp8) Store-memory(adr, GR[reg2], Halfword)					
	SST.W	reg2, disp8[ep]	rrrrr1010ddddddd1 **Note 2**	adr←ep+zero-extend(disp8) Store-memory(adr, GR[reg2], Word)					
	ST.B	reg2, disp16[reg1]	rrrrr111010RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Byte)					
	ST.H	reg2, disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 3**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Halfword)					
	ST.W	reg2, disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 3**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Word)					
Arithmetic	MOV	reg1, reg2	rrrrr000000RRRRR	GR[reg2]←GR[reg1]					
	MOV	imm5, reg2	rrrrr010000iiiii	GR[reg2]←sign-extend(imm5)					
	MOVHI	imm16, reg1, reg2	rrrrr110010RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+(imm16 || 0^{16})					
	MOVEA	imm16, reg1, reg2	rrrrr110001RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)					
	ADD	reg1, reg2	rrrrr001110RRRRR	GR[reg2]←GR[reg2]+GR[reg1]	×	×	×	×	
	ADD	imm5, reg2	rrrrr010010RRRRR	GR[reg2]←GR[reg2]+sign-extend(imm5)	×	×	×	×	
	ADDI	imm16, reg1, reg2	rrrrr110000RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)	×	×	×	×	
	SUB	reg1, reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]–GR[reg1]	×	×	×	×	
	SUBR	reg1, reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]–GR[reg2]	×	×	×	×	

Notes 1. ddddddd = the higher 7 bits of disp8

2. dddddd = the higher 6 bits of disp8

3. dddddddddddddddd = the higher 15 bits of disp16

Instruction Group	Mnemonic	Operand	Operation Code	Operation	Flag				
					CY	OV	S	Z	SAT
Arithmetic	MULH	reg1, reg2	rrrrr000111RRRRR	GR[reg2]←GR[reg2]Note×GR[reg1]Note(signed multiply)					
	MULH	imm5, reg2	rrrrr010111iiiii	GR[reg2]←GR[reg2]Note×sign-extend(imm5) (signed multiply)					
	MULHI	imm16, reg1, reg2	rrrrr110111RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg2]Note×imm16 (signed multiply)					
	DIVH	reg1, reg2	rrrrr000010RRRRR	GR[reg2]←GR[reg2]÷GR[reg1]Note(signed divide)		×	×	×	
	CMP	reg1, reg2	rrrrr001111RRRRR	result←GR[reg2]–GR[reg1]	×	×	×	×	
	CMP	imm5, reg2	rrrrr010011iiiii	result←GR[reg2]–sign-extend(imm5)	×	×	×	×	
	SETF	cccc, reg2	rrrrr1111110cccc 0000000000000000	if conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H					
Saturation operation	SATADD	reg1, reg2	rrrrr000110RRRRR	GR[reg2]←saturated(GR[reg2]+GR[reg1])	×	×	×	×	×
	SATADD	imm5, reg2	rrrrr010001iiiii	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5))	×	×	×	×	×
	SATSUB	reg1, reg2	rrrrr000101RRRRR	GR[reg2]←saturated(GR[reg2]–GR[reg1])	×	×	×	×	×
	SATSUBI	imm16, reg1, reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←saturated(GR[reg1]–sign-extend(imm16))	×	×	×	×	×
	SATSUBR	reg1, reg2	rrrrr000100RRRRR	GR[reg2]←saturated(GR[reg1]–GR[reg2])	×	×	×	×	×
Logical operation	TST	reg1, reg2	rrrrr001011RRRRR	result←GR[reg2]AND GR[reg1]		0	×	×	
	OR	reg1, reg2	rrrrr001000RRRRR	GR[reg2]←GR[reg2]OR GR[reg1]		0	×	×	
	ORI	imm16, reg1, reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]OR zero-extend(imm16)		0	×	×	
	AND	reg1, reg2	rrrrr001010RRRRR	GR[reg2]←GR[reg2]AND GR[reg1]		0	×	×	
	ANDI	imm16, reg1, reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]AND zero-extend(imm16)		0	0	×	
	XOR	reg1, reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2]XOR GR(reg1)		0	×	×	
	XORI	imm16, reg1, reg2	rrrrr110101RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]XOR zero-extend(imm16)		0	×	×	
	NOT	reg1, reg2	rrrrr000001RRRRR	GR[reg2]←NOT(GR[reg1])		0	×	×	
	SHL	reg1, reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2]logically shift left by GR[reg1]	×	0	×	×	
	SHL	imm5, reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2]logically shift left by zero-extend(imm5)	×	0	×	×	
	SHR	reg1, reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2]logically shift right by GR[reg1]	×	0	×	×	
	SHR	imm5, reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2]logically shift right by zero-extend(imm5)	×	0	×	×	
	SAR	reg1, reg2	rrrrr111111RRRRR 0000000010100000	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	×	0	×	×	
	SAR	imm5, reg2	rrrrr010101iiiii	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend(imm5)	×	0	×	×	

Note Only the lower halfword data is valid.

Instruction Group	Mnemonic	Operand	Operation Code	Operation	Flag				
					CY	OV	S	Z	SAT
Branch	JMP	[reg1]	00000000011RRRRR	PC←GR[reg1]					
	JR	disp22	0000011110dddddd ddddddddddddddd0 **Note 1**	PC←PC+sign-extend(disp22)					
	JARL	disp22, reg2	rrrrr11110dddddd ddddddddddddddd0 **Note 1**	GR[reg2]←PC+4 PC←PC+sign-extend(disp22)					
	Bcond	disp9	ddddd1011dddcccc **Note 2**	if conditions are satisfied then PC←PC+sign-extend(disp9)					
Bit manipulate	SET1	bit#3, disp16[reg1]	00bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3, 1)				×	
	CLR1	bit#3, disp16[reg1]	10bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3, 0)				×	
	NOT1	bit#3, disp16[reg1]	01bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3, Z flag)				×	
	TST1	bit#3, disp16[reg1]	11bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3))				×	

Notes 1. ddddddddddddddddddddd = the higher 21 bits of disp22

2. dddddddd = the higher 8 bits of disp9

Instruction Group	Mnemonic	Operand	Operation Code	Operation		Flag				
						CY	OV	S	Z	SAT
Special	LDSR	reg2, regID	rrrrr111111RRRRR 0000000000100000 **Note**	SR[regID]←GR[reg2]	reg ID = EIPC, FEPC reg ID = EIPSW, FEPSW regID = PSW	× × ×	× × ×	× × ×	× × ×	× × ×
	STSR	regID, reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]						
	TRAP	vector	00000111111iiiii 0000000100000000	EIPC←PC+4 (restore PC) EIPSW←PSW ECR.EICC←Interrupt code PSW.EP←1 PSW.ID←1 PC←00000040H(vector=00H-0FH) 00000050H(vector=10H-1FH)						
	RETI		0000011111100000 0000000101000000	if PSW.EP=1 then PC←EIPC PSW←EIPSW else if PSW.NP=1 then PC←FEPC PSW←FEPSW else PC←EIPC PSW←EIPSW		R	R	R	R	R
	HALT		0000011111100000 0000000100100000	Stops						
	DI		0000011111100000 0000000101100000	PSW.ID←1 (disables maskable interrupt)						
	EI		1000011111100000 0000000101100000	PSW.ID←0 (enables maskable interrupt)						
	NOP		0000000000000000	Dissipates 1 clock cycle without doing anything						

Note This instruction uses source register reg2, but its op code actually uses the field of reg1. Therefore, the meanings of the mnemonic description and op code of this instruction are different from those of the others.

rrrrr = regID specification, RRRRR = reg2 specification

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	–0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin	–0.5 to +7.0	V
	CV_{SS}	CV_{SS} pin	–0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 pin, V_{DD} = 5.0 V ±10%	–0.5 to V_{DD} + 0.3	V
Clock input voltage	V_X	X1 pin, V_{DD} = 5.0 ±10%	–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	–4.0	mA
		Total of all pins	–100	mA
Output voltage	V_O	V_{DD} = 5.0 V ±10%	–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect the output (or I/O) pins of IC products, and do not directly connect them to V_{DD}, V_{CC} or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Never exceed or approximate these values when using the product.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_O				15	pF

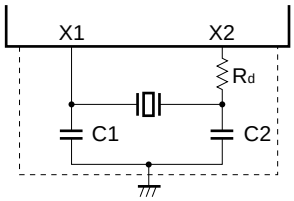
Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Ambient Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 25 MHz	–40 to +85°C	5.0 V ±10%
PLL mode	Freerunning oscillation frequency to 25 MHz	–40 to +85°C	5.0 V ±10%

Recommended Oscillation Circuit

(a) Connecting ceramic resonator (T_A = –20 to +70°C)

(i) Manufacturer: Kyocera, TDK



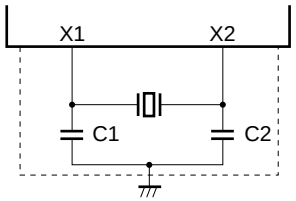
Manufacturer	Part Number		Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time
				C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)	(MAX.) T_{OST} (ms)
Kyocera Corp.	Through-hole type	KBR-2.0MS	2.0	100	100	820	4.5	5.5	0.80
		KBR-2.7MS	2.7	100	100	820	4.5	5.5	0.60
		KBR-3.2MS	3.2	82	82	0	4.5	5.5	0.40
	Surface-mount type	PBRC5.0A	5.0	33	33	680	4.5	5.5	0.20
		PBRC5.0B	5.0	Incorporated	Incorporated	680	4.5	5.5	0.20
TDK Corp.	CCR2.0MC33		2.0	Incorporated	Incorporated	10K	4.5	5.5	0.56
	CCR3.2MC3		3.2	Incorporated	Incorporated	3.3K	4.5	5.5	0.40
	CCR5.0MC3		5.0	Incorporated	Incorporated	680	4.5	5.5	0.38
	FCR5.0MC5		5.0	Incorporated	Incorporated	0	4.5	5.5	0.28
	CCR10.0MC5		10.0	Incorporated	Incorporated	0	4.5	5.5	0.12
	CCR16.0MC6		16.0	Incorporated	Incorporated	2.2K	4.5	5.5	0.34
	FCR25.0MCG		25.0	Incorporated	Incorporated	0	4.5	5.5	0.24

Cautions 1. Connect the oscillation circuit as closely to the X1 and X2 pins as possible.

2. Do not wire any other signal lines in the area indicated by the broken line in the above figure.

3. Thoroughly evaluate the matching between the μPD703002 and oscillator.

(ii) Manufacturer: Murata Mfg.



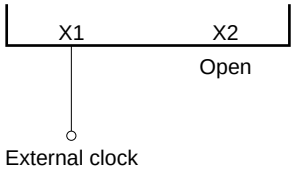
Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg.	CST2.00MG040	2.0	Incorporated	Incorporated	4.5	5.5	0.48
	CSA2.00MG040	2.0	100	100	4.5	5.5	0.48
	CST2.70MGW040	2.7	Incorporated	Incorporated	4.5	5.5	0.47
	CSA2.70MG040	2.7	100	100	4.5	5.5	0.47
	CST3.20MGW040	3.2	Incorporated	Incorporated	4.5	5.5	0.44
	CSA2.20MG040	3.2	100	100	4.5	5.5	0.44
	CST5.00MGW040	5.0	Incorporated	Incorporated	4.5	5.5	0.41
	CSA5.00MG040	5.0	100	100	4.5	5.5	0.41

Cautions 1. Connect the oscillation circuit as closely to the X1 and X2 pins as possible.

2. Do not wire any other signal lines in the area indicated by the broken line in the above figure.

3. Thoroughly evaluate the matching between the μPD703002 and oscillator.

(b) External clock input



Caution Input the voltage at the CMOS level to the X1 pin.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	X1, except **Note 1**	2.2		V_{DD}	V
			Note 1	0.8V_{DD}		V_{DD}	V
Input voltage, low		V_{IL}	X1, except **Note 1**	0		0.8	V
			Note 1	0		0.2V_{DD}	V
X1 clock input voltage, high		V_{XH}	Direct mode	0.8V_{DD}		V_{DD}	V
			PLL mode	0.8V_{DD}		V_{DD}	V
X1 clock input voltage, low		V_{XL}	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input threshold voltage		V_{T^+}	**Note 1** Rising		3.0		V
		V_{T^-}	**Note 1** Falling		2.0		V
Schmitt trigger input hysteresis width		V_{T^+}–V_{T^-}	**Note 1**	0.5			V
Output voltage, high		V_{OH}	I_{OH} = –2.5 mA	0.7V_{DD}			V
			I_{OH} = –100 μA	V_{DD} – 0.4			V
Output voltage, low		V_{OL}	I_{OL} = 2.5 mA			0.45	V
Input leakage current, high		I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			–10	μA
Output leakage current, high		I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low		I_{LOL}	V_O = 0V			–10	μA
Supply current	Operating	I_{DD1}	Direct mode		1.5 × ϕ +6	2.2 × ϕ +10	mA
			PLL mode (f_{XX} = ϕ/5)		1.6 × ϕ +7	2.4 × ϕ +11	mA
			PLL mode (f_{XX} = ϕ)		1.9 × ϕ +9	3.0 × ϕ +15	mA
	HALT	I_{DD2}	Direct mode		0.5 × ϕ +4	0.8 × ϕ +10	mA
			PLL mode (f_{XX} = ϕ/5)		0.6 × ϕ +5	1.0 × ϕ +11	mA
			PLL mode (f_{XX} = ϕ)		0.9 × ϕ +7	1.6 × ϕ +15	mA
	IDLE	I_{DD3}	Direct mode		15 × ϕ +200	26 × ϕ +200	μA
			PLL mode (f_{XX} = ϕ/5)		0.1 × ϕ +0.2	0.2 × ϕ +0.2	mA
			PLL mode (f_{XX} = ϕ)		0.4 × ϕ +3	0.8 × ϕ +5	mA
	STOP	I_{DD4}	–40°C ≤ T_A ≤ +50°C		1	50	μA
			50°C < T_A ≤ 85°C			200	μA

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL

Remarks 1. TYP. value is a value for reference at T_A = 25°C, V_{DD} = 5.0 V.

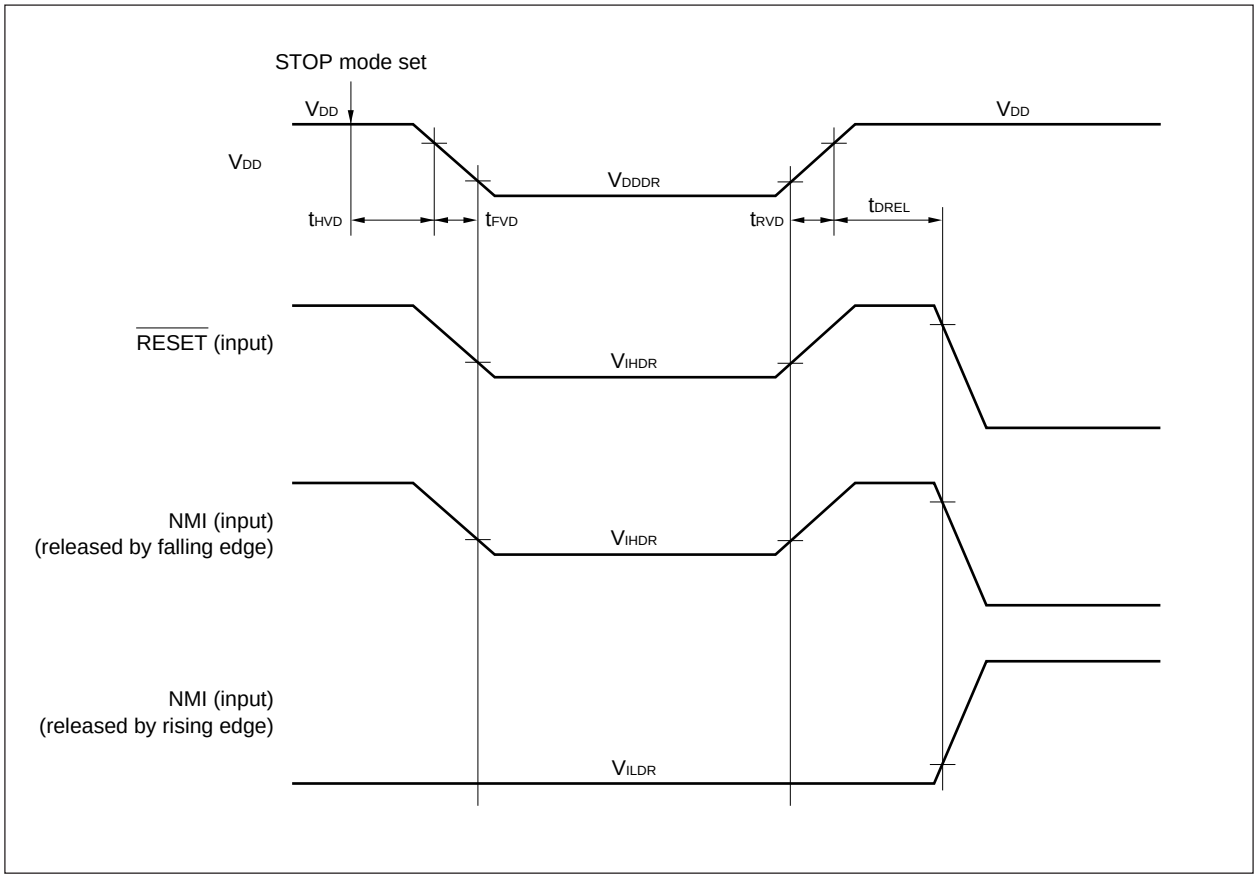
2. ϕ: internal operating clock frequency

Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode	1.5		5.5	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$, –40°C ≤ T_A ≤ +50°C		0.2V_{DDDR}	50	μA
		$V_{DD} = V_{DDDR}$, 50°C < T_A ≤ +85°C		0.2V_{DDDR}	200	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP mode releasing signal input time	t_{DREL}		0			ns
Data hold input voltage, high	V_{IHDR}	**Note**	0.9V_{DDDR}		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	**Note**	0		0.1V_{DDDR}	V

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL, X1

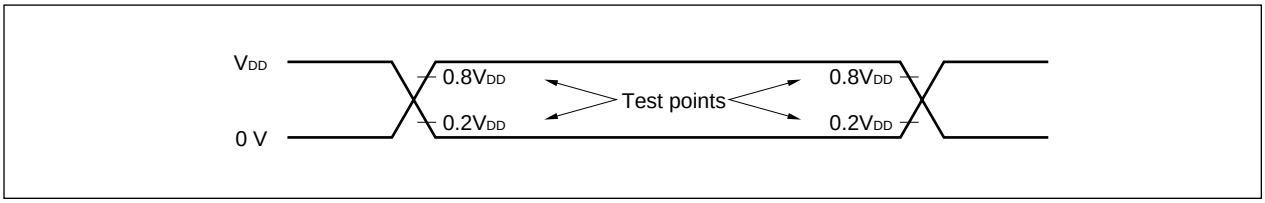
Remark TYP. value is a value for reference at T_A = 25°C, V_{DD} = 5.0 V.



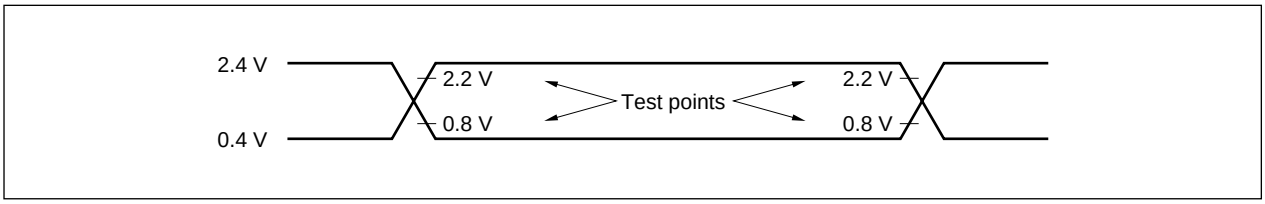
AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, C_L (output pin load capacitance) = 50 pF)

AC test input wave

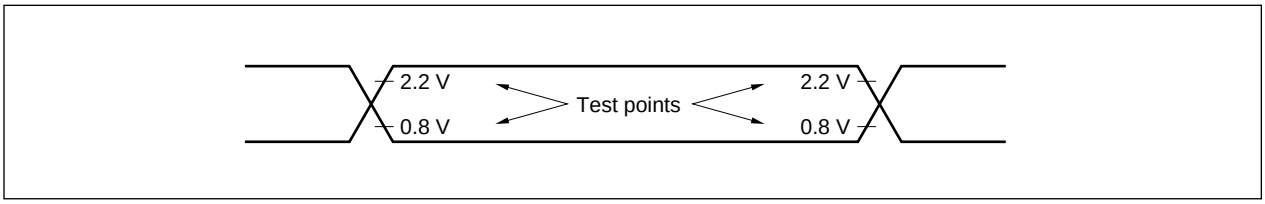
(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL, X1



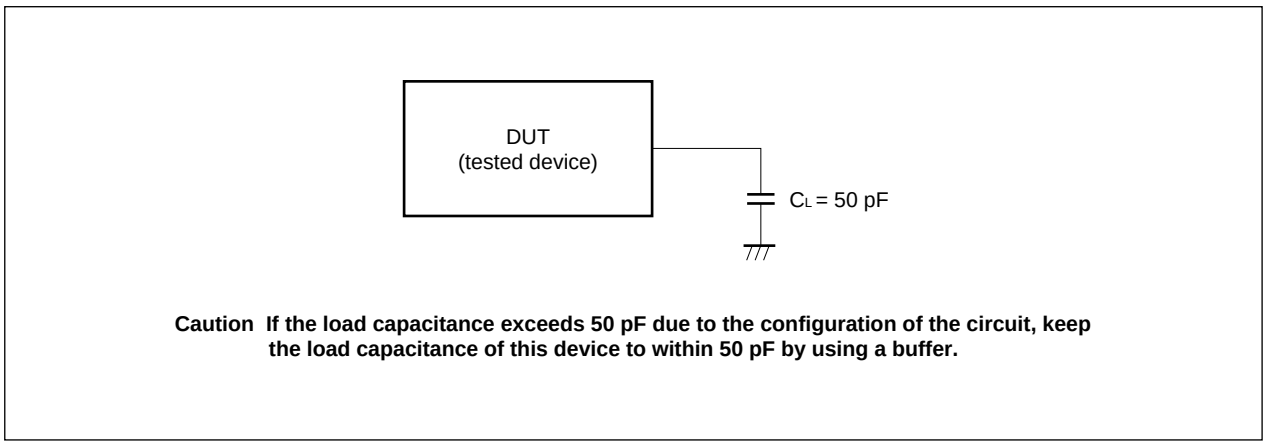
(b) Other than (a) above



AC test output test point



Load condition



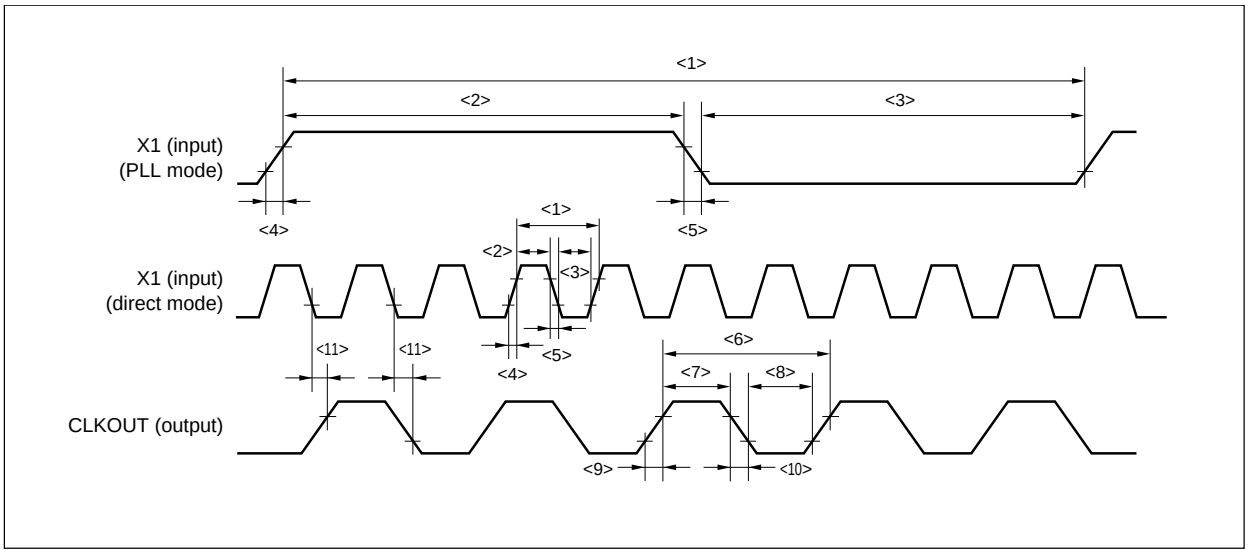
Caution If the load capacitance exceeds 50 pF due to the configuration of the circuit, keep the load capacitance of this device to within 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	20	DC	ns
			PLL mode ($f_{XX} = \phi/5$)	200	285	ns
			PLL mode ($f_{XX} = \phi$)	40	100	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode	7		ns
			PLL mode ($f_{XX} = \phi/5$)	80		ns
			PLL mode ($f_{XX} = \phi$)	10		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode	7		ns
			PLL mode ($f_{XX} = \phi/5$)	80		ns
			PLL mode ($f_{XX} = \phi$)	10		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7	ns
			PLL mode ($f_{XX} = \phi/5$)		15	ns
			PLL mode ($f_{XX} = \phi$)		7	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7	ns
			PLL mode ($f_{XX} = \phi/5$)		15	ns
			PLL mode ($f_{XX} = \phi$)		7	ns
CPU operating frequency	–	ϕ		0	25	MHz
CLKOUT output cycle	<6>	t_{CYK}		40	DC	ns
CLKOUT high-level width	<7>	t_{WKH}		0.5T–10		ns
CLKOUT low-level width	<8>	t_{WKL}		0.5T–10		ns
CLKOUT rise time	<9>	t_{KR}			5	ns
CLKOUT fall time	<10>	t_{KF}			5	ns
X1↓ →CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	17	ns

Remark T = t_{CYK}

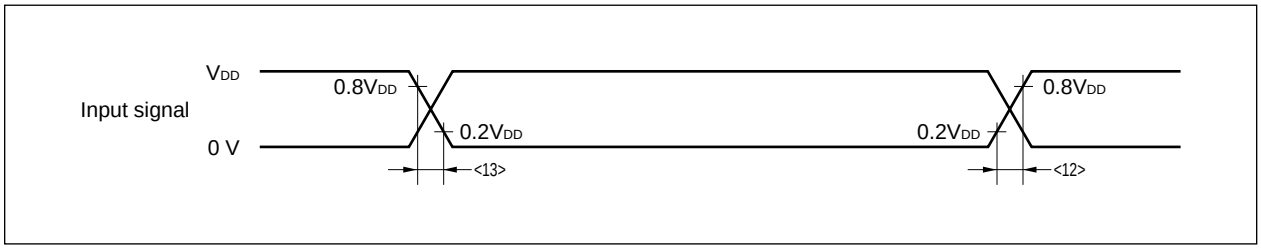
Parameter	Symbol		Condition	TYP.	Unit
Freerunning oscillation frequency	–	ϕ_P	PLL mode	0.6	MHz



(2) Input wave

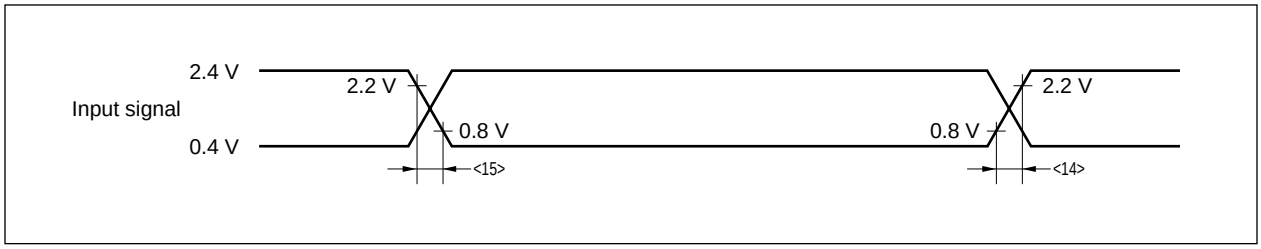
(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL, X1

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<12>	t_{IR2}			20	ns
Input fall time	<13>	t_{IF2}			20	ns



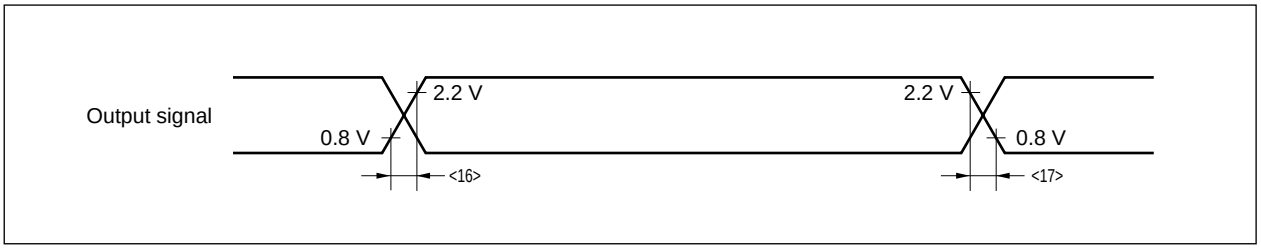
(b) Other than (a) above

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<14>	t_{IR1}			10	ns
Input fall time	<15>	t_{IF1}			10	ns



(3) Output waveform (other than CLKOUT)

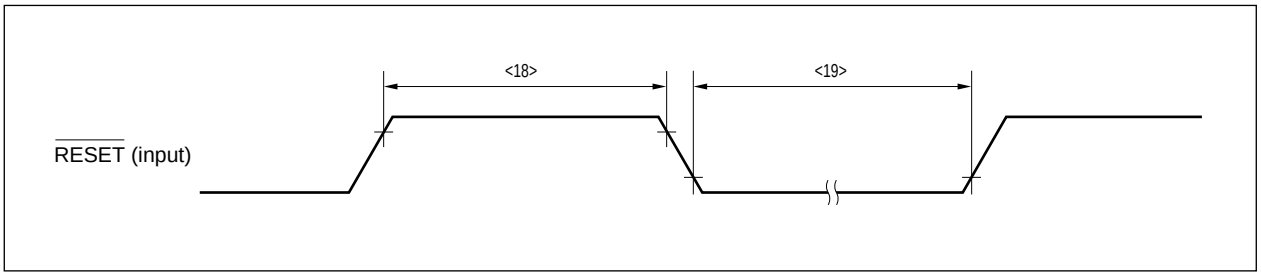
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<16>	t_{OR}			10	ns
Output fall time	<17>	t_{OF}			10	ns



(4) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<18>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	<19>	t_{WRSL}	On power application and on releasing STOP mode	500+T_{OST}		ns
			Except on power application and on releasing STOP mode	500		ns

Remark T_{OST}: Oscillation Stabilization Time



[MEMO]

(5) Read timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑ → Address delay time	<20>	t_{DKA}		3	20	ns
CLKOUT ↑ → Address float time	<21>	t_{FKA}		3	15	ns
CLKOUT ↓ → ASTB delay time	<22>	t_{DKST}		3	15	ns
CLKOUT ↑ → $\overline{\text{DSTB}}$ delay time	<23>	t_{DKD}		3	15	ns
CLKOUT ↑ → Status delay time	<24>	t_{DKS}		3	15	ns
Data input setup time (to CLKOUT ↑)	<25>	t_{SIDK}		5		ns
Data input hold time (from CLKOUT ↑)	<26>	t_{HKID}		5		ns
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<27>	t_{SWTK}		5		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<28>	t_{HKWT}		5		ns
Address hold time (from CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setup time (to ASTB ↓)	<30>	t_{SAST}		0.5T–10		ns
Address hold time (from ASTB ↓)	<31>	t_{HSTA}		0.5T–10		ns
$\overline{\text{DSTB}}$ ↓ → Address float delay time	<32>	t_{FDA}			0	ns
Data input setup time (to address)	<33>	t_{SAID}			(2+n)T–20	ns
Data input setup time (to $\overline{\text{DSTB}}$ ↓)	<34>	t_{SDID}			(1+n)T–20	ns
ASTB ↓ → $\overline{\text{DSTB}}$ ↓ delay time	<35>	t_{DSTD}		0.5T–10		ns
Data input hold time (from $\overline{\text{DSTB}}$ ↑)	<36>	t_{HDID}		0		ns
$\overline{\text{DSTB}}$ ↑ → Address output delay time	<37>	t_{DDA}		(1+i)T		ns
$\overline{\text{DSTB}}$ ↑ → ASTB ↑ delay time	<38>	t_{DDSTH}		0.5T–10		ns
$\overline{\text{DSTB}}$ ↑ → ASTB ↓ delay time	<39>	t_{DDSTL}		(1.5+i)T–10		ns
Status setup time (to ASTB ↓)	<40>	t_{SSST}		0.5T–10		ns
Status hold time (from ASTB ↑)	<41>	t_{HSTS}		0.5T–10		ns
$\overline{\text{DSTB}}$ low-level width	<42>	t_{WDL}		(1+n)T–10		ns
ASTB high-level width	<43>	t_{WSTH}		T–10		ns
$\overline{\text{WAIT}}$ setup time (to address)	<44>	t_{SAWT1}	n ≥ 1		1.5T–20	ns
	<45>	t_{SAWT2}			(1.5+n)T–20	ns
$\overline{\text{WAIT}}$ hold time (from address)	<46>	t_{HAWT1}	n ≥ 1	(0.5+n)T		ns
	<47>	t_{HAWT2}		(1.5+n)T		ns
$\overline{\text{WAIT}}$ setup time (to ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T–15	ns
	<49>	t_{SSTWT2}			(1+n)T–15	ns
$\overline{\text{WAIT}}$ hold time (from ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1+n)T		ns

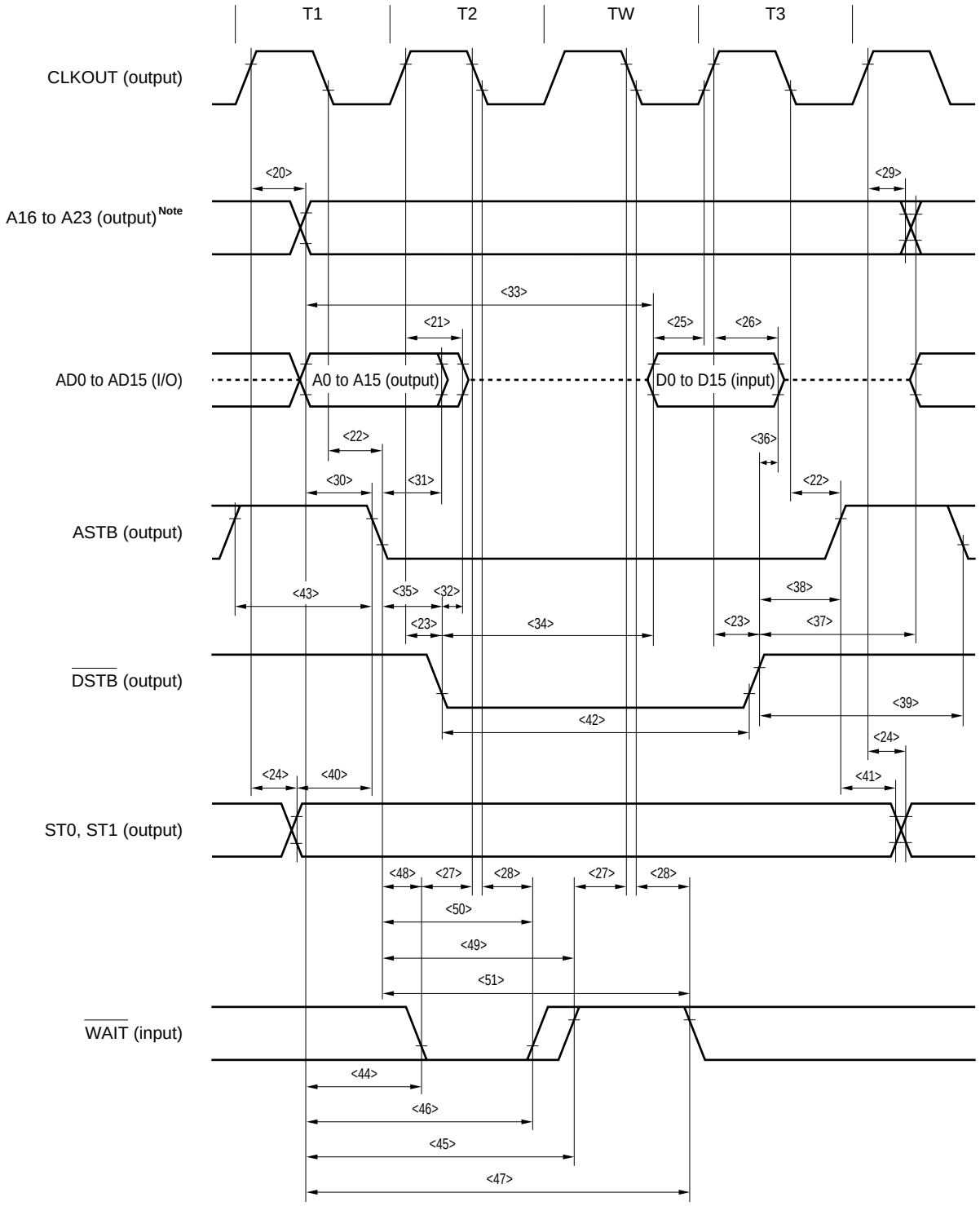
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

3. i indicates the number of idle states (0 or 1) inserted in the read cycle.

4. Satisfy at least one of the data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

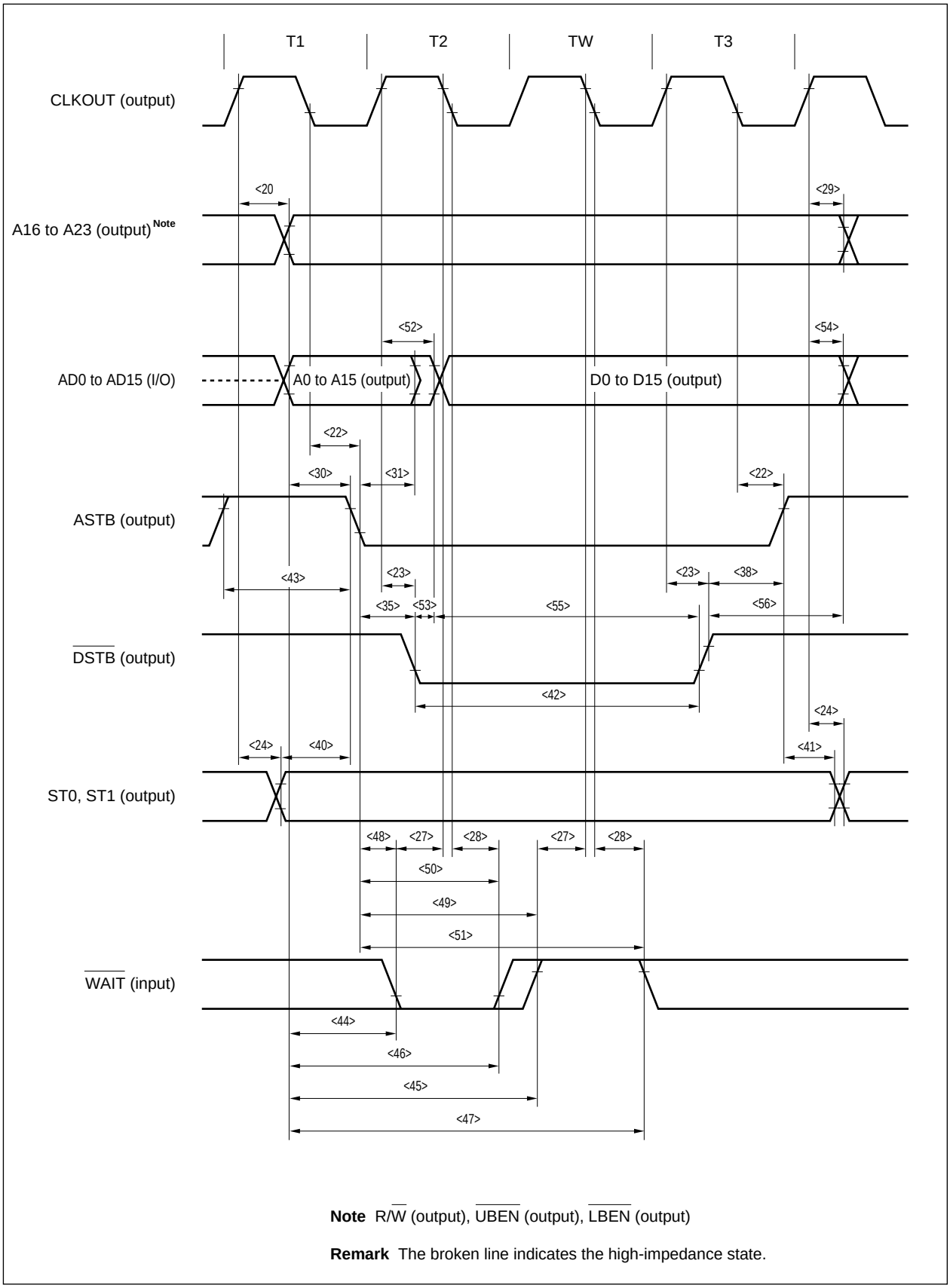
(6) Write timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑ → Address delay time	<20>	t_{DKA}		3	20	ns
CLKOUT ↓ → ASTB delay time	<22>	t_{DKST}		3	15	ns
CLKOUT ↑ → $\overline{\text{DSTB}}$ delay time	<23>	t_{DKD}		3	15	ns
CLKOUT ↑ → Status delay time	<24>	t_{DKS}		3	15	ns
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<27>	t_{SWTK}		5		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<28>	t_{HKWT}		5		ns
Address hold time (from CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setup time (to ASTB ↓)	<30>	t_{SAST}		0.5T–10		ns
Address hold time (from ASTB ↓)	<31>	t_{HSTA}		0.5T–10		ns
ASTB ↓ → $\overline{\text{DSTB}}$ ↓ delay time	<35>	t_{DSTD}		0.5T–10		ns
$\overline{\text{DSTB}}$ ↑ → ASTB ↑ delay time	<38>	t_{DDSTH}		0.5T–10		ns
Status setup time (to ASTB ↓)	<40>	t_{SSST}		0.5T–10		ns
Status hold time (from ASTB ↑)	<41>	t_{HSTS}		0.5T–10		ns
$\overline{\text{DSTB}}$ low-level width	<42>	t_{WDL}		(1+n)T–10		ns
ASTB high-level width	<43>	t_{WSTH}		T–10		ns
$\overline{\text{WAIT}}$ setup time (to address)	<44>	t_{SAWT1}	n ≥ 1		1.5T–20	ns
	<45>	t_{SAWT2}			(1.5+n)T–20	ns
$\overline{\text{WAIT}}$ hold time (from address)	<46>	t_{HAWT1}	n ≥ 1	(0.5+n)T		ns
	<47>	t_{HAWT2}		(1.5+n)T		ns
$\overline{\text{WAIT}}$ setup time (to ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T–15	ns
	<49>	t_{SSTWT2}			(1+n)T–15	ns
$\overline{\text{WAIT}}$ hold time (from ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1+n)T		ns
CLKOUT ↑ → Data output delay time	<52>	t_{DKOD}			20	ns
$\overline{\text{DSTB}}$ ↓ → Data output delay time	<53>	t_{DDOD}			10	ns
Data output hold time (from CLKOUT ↑)	<54>	t_{HKOD}		0		ns
Data output setup time (to $\overline{\text{DSTB}}$ ↑)	<55>	t_{SODD}		(1+n)T–15		ns
Data output hold time (from $\overline{\text{DSTB}}$ ↑)	<56>	t_{HDOD}		T–10		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

(6) Write timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

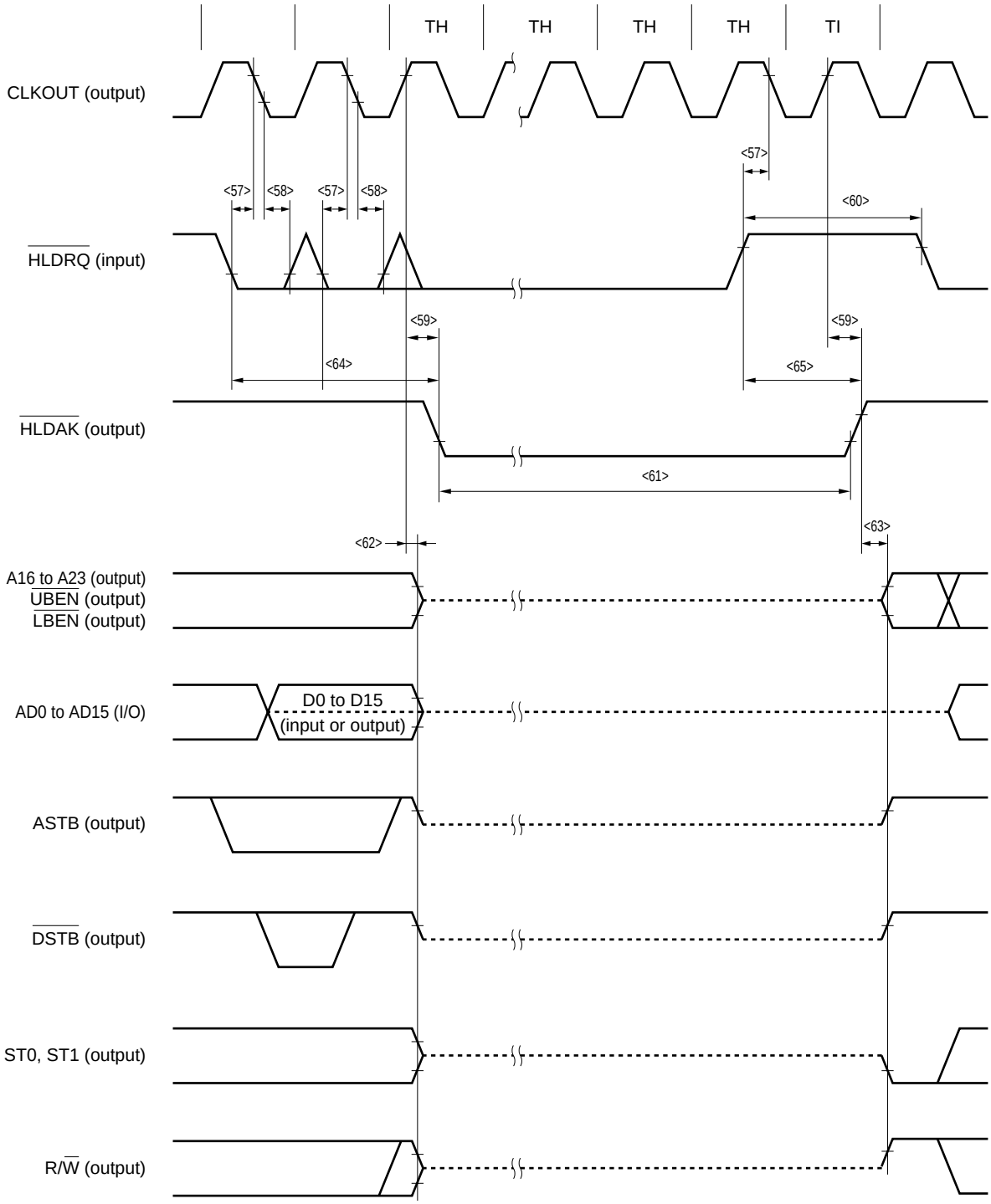
(7) Bus hold timing (1/2)

	Parameter	Symbol		Condition	MIN.	MAX.	Unit
	$\overline{\text{HLDRQ}}$ setup time (to CLKOUT ↓)	<57>	t_{SHQK}		5		ns
	$\overline{\text{HLDRQ}}$ hold time (from CLKOUT ↓)	<58>	t_{HKHQ}		5		ns
	CLKOUT ↑ → $\overline{\text{HLDAK}}$ delay time	<59>	t_{DKHA}			20	ns
	$\overline{\text{HLDRQ}}$ high-level width	<60>	t_{WHQH}		T+10		ns
	$\overline{\text{HLDAK}}$ low-level width	<61>	t_{WHAL}		T–10		ns
★	CLKOUT ↑ → Bus float delay time	<62>	t_{DKF}			20	ns
	$\overline{\text{HLDAK}}$ ↑ → Bus output delay time	<63>	t_{DHAC}		–3		ns
	$\overline{\text{HLDRQ}}$ ↓ → $\overline{\text{HLDAK}}$ ↓ delay time	<64>	t_{DHQHA1}			(2n+7.5)T+20	ns
	$\overline{\text{HLDRQ}}$ ↑ → $\overline{\text{HLDAK}}$ ↑ delay time	<65>	t_{DHQHA2}		0.5T	1.5T+20	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

(7) Bus hold timing (2/2)

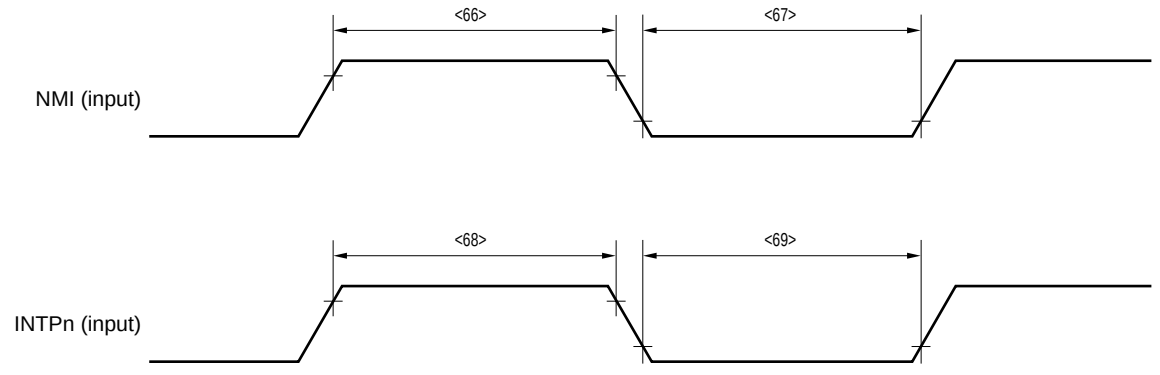


Remark The broken line indicates the high-impedance state.

(8) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<66>	t_{WNIH}		500		ns
NMI low-level width	<67>	t_{WNIL}		500		ns
INTPn high-level width	<68>	t_{WITH}	n = 00, 01, 02, 03, 10, 11, 12, 13	3T+10		ns
INTPn low-level width	<69>	t_{WITL}	n = 00, 01, 02, 03, 10, 11, 12, 13	3T+10		ns

Remark T = t_{CYK}



Remark n = 00, 01, 02, 03, 10, 11, 12, 13

(9) CSI timing

(a) Master mode

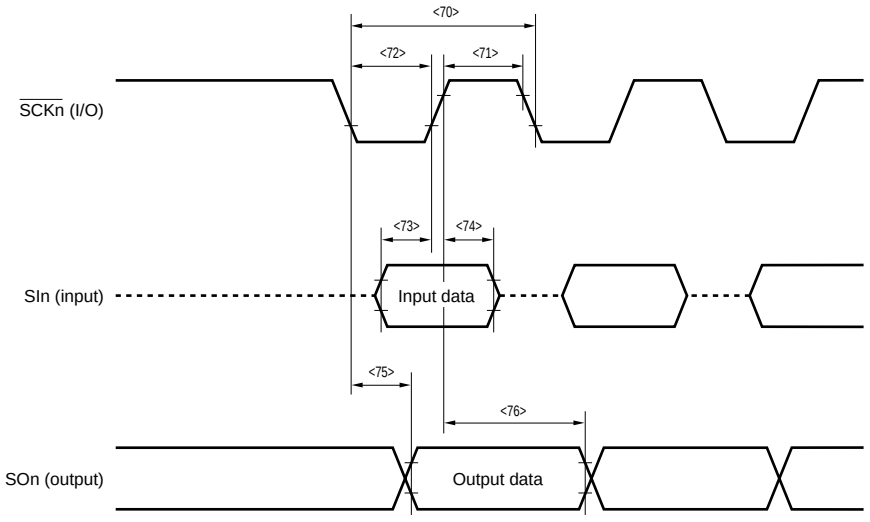
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<70>	t_{CYSK}	Output	250		ns
$\overline{SCKn}$ high-level width	<71>	t_{WSKH}	Output	$0.5t_{CYSK}-20$		ns
$\overline{SCKn}$ low-level width	<72>	t_{WSKL}	Output	$0.5t_{CYSK}-25$		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<73>	t_{SSISK}		45		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<74>	t_{HSKSI}		0		ns
SOn output delay time (from $\overline{SCK0}$ ↓)	<75>	t_{DSKSO}			25	ns
SOn output delay time (from $\overline{SCK0}$ ↑)	<76>	t_{HSKSO}		$0.5t_{CYSK}-5$		ns

Caution When the internal clock is selected as the serial clock, set f to 8 MHz or lower if specifying $\phi/2$, and set ϕ to 16 MHz or lower if specifying $\phi/4$ (ϕ = internal operation clock frequency). To select a higher operating frequency than those indicated above, select the baud rate generator (BRG) output instead of the internal clock.

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<70>	t_{CYSK}	Input	250		ns
$\overline{SCKn}$ high-level width	<71>	t_{WSKH}	Input	70		ns
$\overline{SCKn}$ low-level width	<72>	t_{WSKL}	Input	70		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<73>	t_{SSISK}		10		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<74>	t_{HSKSI}		15		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<75>	t_{DSKSO}			55	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<76>	t_{HSKSO}		t_{WSKH}		ns

Caution When the internal clock is selected as the serial clock, set f to 8 MHz or lower if specifying $\phi/2$, and set ϕ to 16 MHz or lower if specifying $\phi/4$ (ϕ = internal operation clock frequency). To select a higher operating frequency than those indicated above, select the baud rate generator (BRG) output instead of the internal clock.



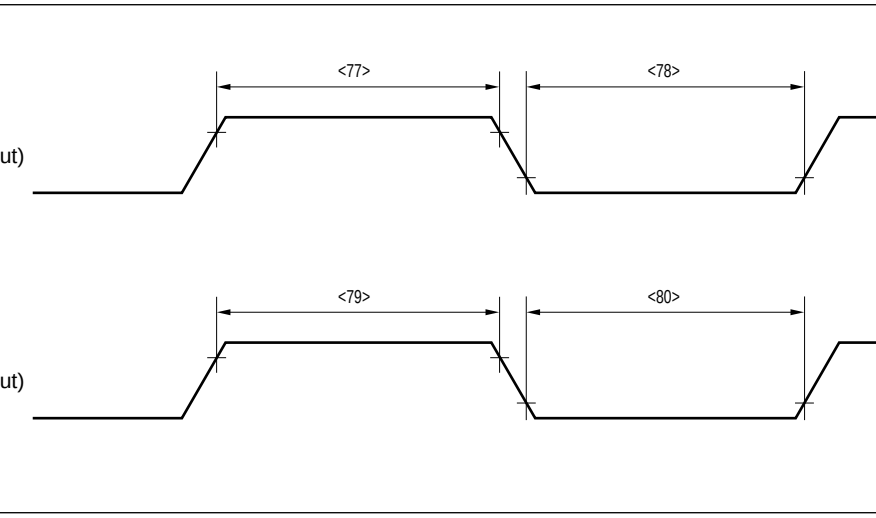
Remarks 1. The broken line indicates the high-impedance state.

2. n = 0 to 2

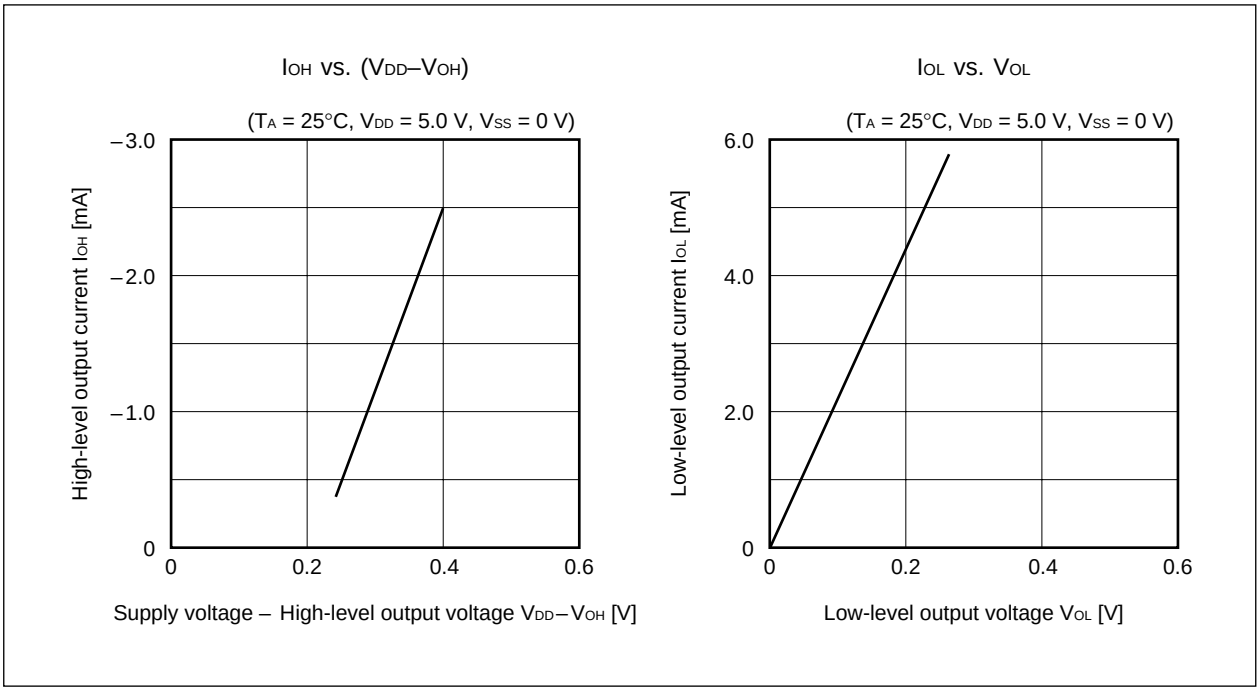
(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1 high-level width	<77>	t_{WTIH}		3T+10		ns
TI1 low-level width	<78>	t_{WTIL}		3T+10		ns
TCLR1 high-level width	<79>	t_{WTCH}		3T+10		ns
TCLR1 low-level width	<80>	t_{WTCL}		3T+10		ns

Remark T = t_{CYK}

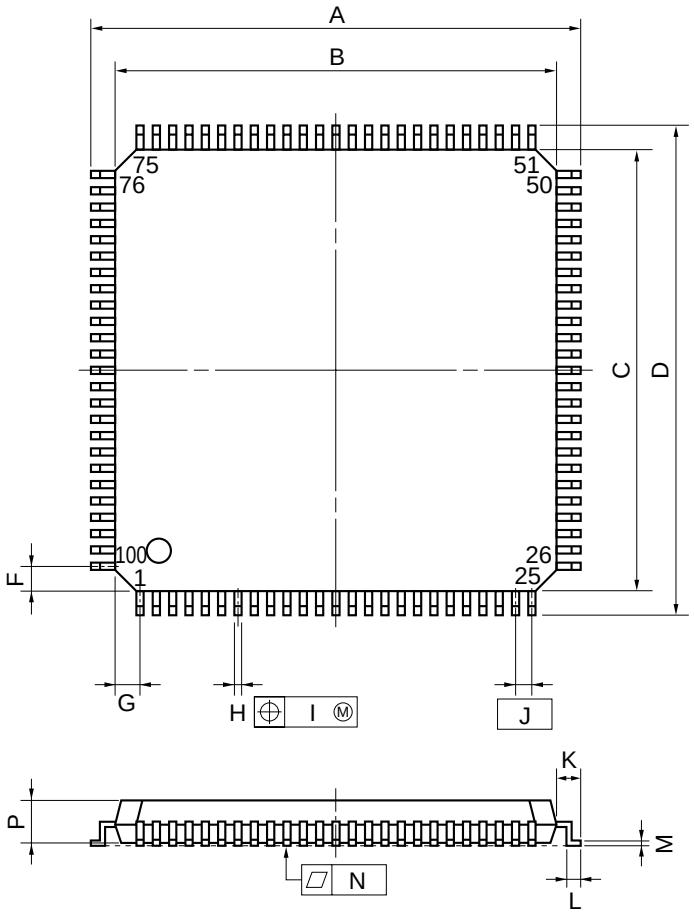


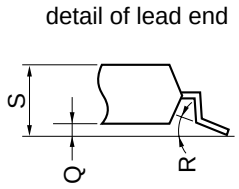
13. CHARACTERISTIC CURVES (REFERENCE)



14. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)





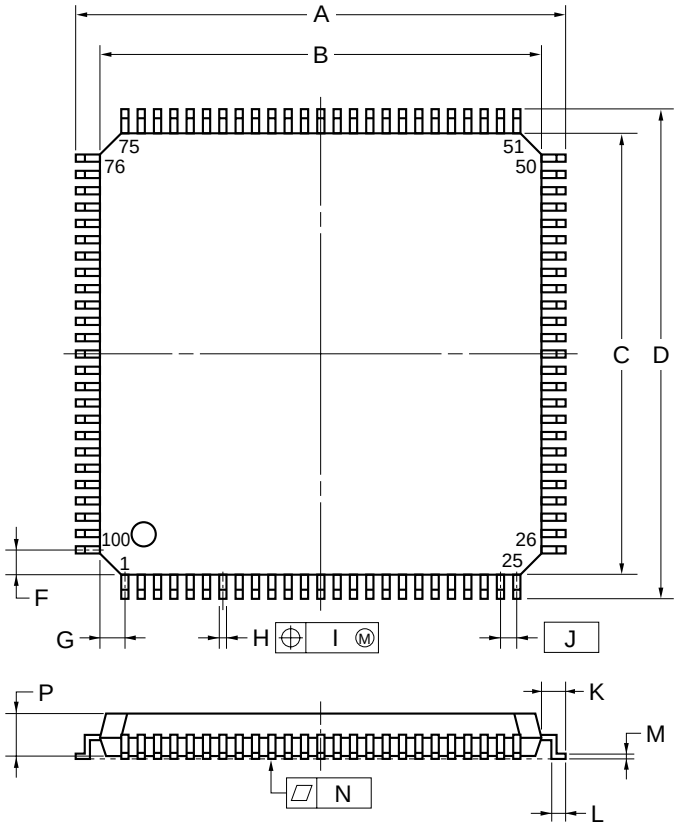
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

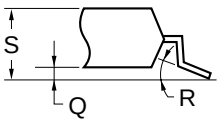
ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

★ 100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

15. RECOMMENDED SOLDERING CONDITIONS

The μPD703002 should be soldered and mounted under the following recommended conditions.

For the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

★ **Table 15-1. Soldering Conditions**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Note Exposure limit after dry-pack is opened. Storage conditions: temperature of 25°C and relative humidity of 65% or less.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Phase-out/Discontinued

Related documents : μPD70P3002 Data Sheet (U11827E)
V850 Family Instruction List (U10229J) (Japanese version)
V852 Register Application Table (U10513J) (Japanese version)

Reference : Electrical Characteristics for Microcomputer (IEI-601) (Japanese version)

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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