To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS Integrated Circuit

μPD65881GB-P02

μPD71051-Compliant Serial Control Unit Gate Array

Following the phase-out of it popular μPD71051 standard serial control unit (USART), NEC Electronics is now offering the μPD65881GB-P02 serial control unit, a functional and low-cost substitute for the μPD71051.

To verify the applicability of the μPD65881GB-P02 gate array as a replacement for the μPD71051, you must first test an equivalent prototype in the system being developed. If the in-system test is deemed successful, then you may proceed to purchase mass production versions of the product.

DESCRIPTION

Internal block functions and commands are the same as those of the μPD71051. Differences between the two products are listed below. Before adopting this product, carefully read the disclaimer below and the caution in section **3 (CAUTIONS WHEN CONSIDERING ADOPTION OF THIS PRODUCT)**.

The μPD65881GB-P02 integrates an NA55A IP macro in a CMOS-N5 gate array that can be used as a peripheral I/O device to transmit serial data synchronously, asynchronously, or bi-synchronously.

The USART receives serial data streams and converts them into parallel data characters for the CPU. While receiving serial data, the USART can also accept parallel data from the CPU, convert it to serial data, and then transmit it. The USART signals the CPU when it has received or transmitted a character and requires service. The CPU may read complete USART status data at any time.

FEATURES

- Synchronous operation
- One or two synchronous characters
- Internal/external synchronization
- Automatic SYNC character insertion
- Asynchronous operation
- Clock rate (baud rate): ×1, ×16, or ×64
  - Send stop bits: 1, 1.5, or 2 bits
  - Break transmission
  - Automatic break detection
  - Valid start bit detection
- Baud rate: DC ~ 660 Kb/s at ×1 clock
- Full-duplex, double-buffered transmitter/receiver
- Error detection: parity, overrun, and framing
- Five- to eight-bit characters
- Low-power standby mode
- Compatible with standard microcontrollers
- Functionally equivalent to (except in standby mode) and can replace the μPD8251AF
- CMOS process technology
- Single +5V ±10% power supply
- Industrial temperature range (Ambient): –40 to 85°C
- 44-pin QFP package
- RoHS-compliant

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Disclaimer

- This product is not functionally equivalent to any similar non-NEC Electronics product. NEC Electronics shall assume no responsibility for any loss or damage incurred by customers or third parties resulting from the replacement of products similar to, but other than, the μPD71051GB-10-3B4.
- NEC Electronics shall assume no responsibility for any loss or damage incurred by customers or third parties resulting from the use of this product outside the conditions described in the absolute maximum ratings, recommended operation range, and quality grades.

COMPARISON OF μPD65881GB-P02 AND μPD71051

Feature	This Product	μPD71051	Reference
Part number (mark)	μPD65881GB-P02-3BS-A (658N51)	μPD71051GB-10-3B4 (standard NEC Electronics mark)	–
Package type	Only 44-pin QFP	QFP, DIP, SOP, PLCC (QFJ)	–
Package shape (comparison of 44-pin QFP)	The body size and package width are the same, but the pin lengths and pin bending method are different.		**4. PACKAGE DRAWING**
Function of pin 39	IC (connection with external pin prohibited)	NC	**1. PIN LAYOUT**
Lead-free support	Yes	No	**ORDERING INFORMATION**
Recommended soldering conditions	IR60-207-3, partial heating	IR35-00-3, VP15-00-3, WS60-00-1, partial heating	**5. RECOMMENDED SOLDERING CONDITIONS**
Absolute maximum ratings			**2. ELECTRICAL SPECIFICATIONS**
Power supply voltage	–0.5 to +6.0 (V)	–0.5 to +7.0 (V)	
Input voltage	–0.5 to +6.0 (V)	–0.5 to V_{DD}+0.3 (V)	
Output voltage	–0.5 to +6.0 (V)	–0.5 to V_{DD}+0.3 (V)	
Recommended operating range	T_A = –40 to +85°C, V_{DD} = 5 V±10% This product does not guarantee operation at less than 4.5 V.		
DC characteristics	Partially different		
AC characteristics	This product has the following restrictions on load capacitance. D7 to D0: 100 pF or less TXDATA, SYNC/BRK, RXRDY, TXEMP, TXRDY: 40 pF or less		

ORDERING INFORMATION

Part Number	Package
μPD65881GB-P02-3BS-A	44-pin plastic QFP (10 x 10 mm)

Remark Products with -A at the end of the part number are lead-free products.

QUALITY GRADES

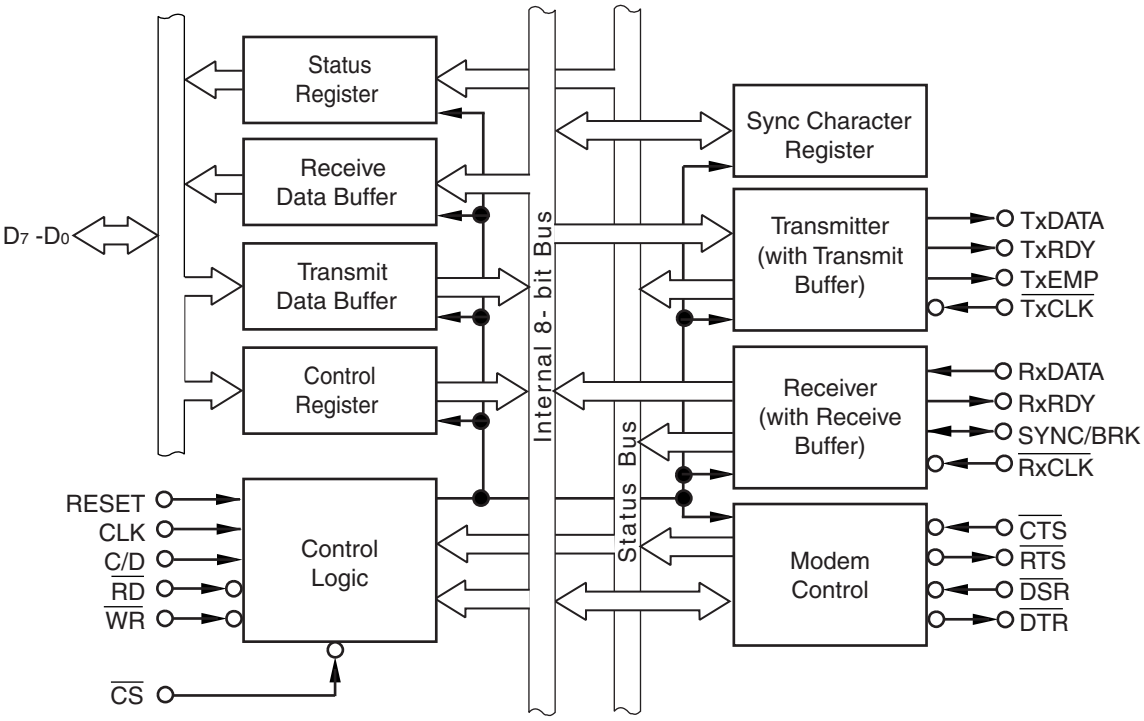
"Standard"

This product is intended to be used for applications such as computers, office equipment, communications equipment, test and measurement equipment, and home electronic appliances. It therefore cannot be used for the following applications.

Applications requiring special or specific grades, such as transportation equipment (automobiles, trains, ships, etc.), traffic control systems, medical equipment, aircraft equipment, and aerospace equipment.

Remark For details of quality grades, refer to **Quality Grades on NEC Semiconductor Devices (document number: C11531E)**.

BLOCK DIAGRAM (μPD71051)



1. PIN LAYOUT

For a description of pin functions, refer to the μPD71051 Data Sheet (document number: IC-6494) (Japanese version).

Pin No.	I/O	Pin Name	Name of Pin on μPD71051	Pin No.	I/O	Pin Name	Name of Pin on μPD71051
1	–	NC	←	23	–	NC	←
2	–	NC	←	24	–	NC	←
3	O	TXD	TxDATA	25	I/O	D4	←
4	I	CLK	←	26	I/O	D5	←
5	I	RESET	←	27	I/O	D6	←
6	–	NC	←	28	–	NC	←
7	I	DSRB	$\overline{\text{DSR}}$	29	I/O	D7	←
8	O	RTSB	$\overline{\text{RTS}}$	30	I	TXCLK	$\overline{\text{TxCLK}}$
9	O	DTRB	$\overline{\text{DTR}}$	31	I	WRB	$\overline{\text{WR}}$
10	–	NC	←	32	–	NC	←
11	–	NC	←	33	–	NC	←
12	–	NC	←	34	–	NC	←
13	I	RXCLK	$\overline{\text{RxCLK}}$	35	I	CSB	$\overline{\text{CS}}$
14	–	V_{DD}	←	36	I	CD	$\overline{\text{CD}}$
15	I/O	D0	←	37	I	RDB	$\overline{\text{RD}}$
16	I/O	D1	←	38	O	RXRDY	RxRDY
17	–	IC (GND) Note	IC	39	–	IC (V_{DD}) Note	NC
18	I/O	D2	←	40	O	TXRDY	TxRDY
19	I/O	D3	←	41	I/O	SYN_BRK	SYNC/BRK
20	I	RXD	RxDATA	42	I	CTSB	$\overline{\text{CTS}}$
21	–	GND	←	43	O	TXEMP	TxEMP
22	–	NC	←	44	–	NC	←

Note This pin is connected to GND or V_{DD} in the chip. To enhance the power supply to handle noise, this pin can be connected to the power supply pin of the board to improve the noise resistance performance.

2. ELECTRICAL SPECIFICATIONS

This section describes only the differences with the μPD71051.

For electrical specifications other than those below, refer to the μPD71051 Data Sheet (document number: IC-6494).

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		–0.5 to +6.0	V
Input voltage	V_I		–0.5 to +6.0	V
Output voltage	V_O		–0.5 to +6.0	V

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. In other words, the absolute maximum ratings are values at which the product may begin to suffer degradation. Therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range

This is the same as the μPD71051. This product does not guarantee operation at less than 4.5 V.

DC Characteristics (V_{DD} = 5 V±10%, T_A = –40 to +85°C)

Parameter	Symbol	This Product				μPD71051				Unit
		Condition	Min.	Typ.	Max.	Condition	Min.	Typ.	Max.	
Input voltage, high	V_{IH}		2.29		V_{DD}		2.2		V_{DD}+0.3	V
Input voltage, low	V_{IL}		0.00		0.77		–0.5		0.8	V
Output voltage, high	V_{OH}	I_{OH} = 0 mA	V_{DD}–0.1			I_{OH} = –400 μA	0.7×V_{DD}			V
		I_{OH} = 3 mA	V_{DD}–0.4							
Output voltage, low	V_{OL}	I_{OL} = 3 mA			0.4	I_{OL} = 2.5 mA			0.4	V
Output current, low	I_{OL}		3.0				2.5			mA

AC Characteristics

These are similar to the μPD71051 characteristics, except for the following restrictions on load capacitance. Operation outside the range of these restrictions is not guaranteed.

D7 to D0: 100 pF or less

TXDATA, SYNC/BRK, RXRDY, TXEMP, TXRDY: 40 pF or less

3. CAUTIONS WHEN CONSIDERING ADOPTION OF THIS PRODUCT

When considering the adoption of this product, note the following points.

(1) Functional check using product samples

Before adopting this product, make sure to request product samples from NEC Electronics to check the functions. Product samples are available free of charge.

When mounting this product onto different multiple printed circuit boards, extensively check the functions by changing the supply voltage to be supplied to the printed circuit boards as well as the temperature conditions for all printed circuit boards.

The standard number of product samples is five. When requesting product samples, provide the following information to your NEC Electronics sales representative.

Your company name, your name, product application, the period of starting adoption, the number of products to be adopted

(2) Submitting the Approval Sheet

When normal operation has been confirmed and the adoption has been decided, complete a copy of the Approval Sheet (Appendix of this document) and submit it to NEC Electronics.

(3) Shipment inspection

Shipment inspection is performed for this product using the μPD71051GB-10-3B4 shipment test pattern. The DC characteristics satisfy the gate array shipment inspection.

(4) Order amount

Orders from a minimum of 100 units, and in units of 100 are accepted.

(5) Package, packing form

The dimensions are partially different from the μPD71051GB-10-3B4. Refer to the package drawing and confirm that the product can actually be mounted. Dry pack tray packing is used for packing.

(6) Price

Contact your local NEC Electronics sales representative for pricing information.

(7) Obtaining the μPD71051 Data Sheet[Note]

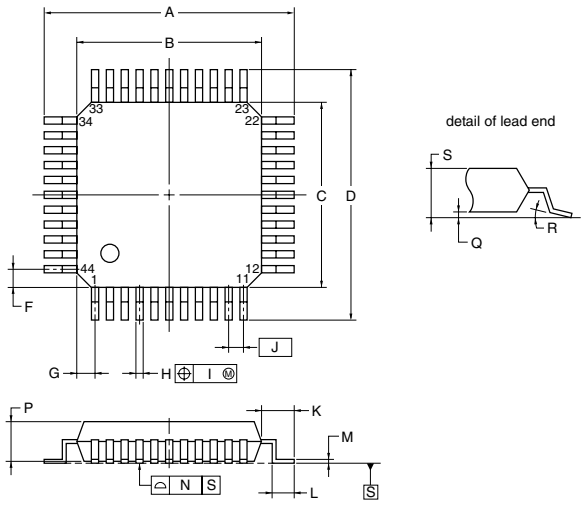
The μPD71051 (original product) Data Sheet is available from the NEC Electronics Web site (http://www.necel.com/) at

http://www.necel.com/nesdis/image/IC-6494D.pdf

Note Please make this data sheet a standalone document. Do not refer customers to the data sheet for an obsolete device.

4. PACKAGE DRAWING

44-PIN PLASTIC QFP (10x10)



NOTE
Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	13.2±0.2
B	10.0±0.2
C	10.0±0.2
D	13.2±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.16
J	0.8 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.17^{+0.06}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.

S44GB-80-3BS-2

5. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronicssales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditons	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C Time: 60 seconds max. (at 220°C or higher) Count: 3 times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Partial heating	Pin temperature: 350°C max. Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX APPROVAL SHEET

Copy this page and complete and confirm the required items.
If you accept the conditions, sign and submit this sheet to NEC Electronics.

Approval Sheet

TO: NEC Electronics ( )

We have confirmed through sample evaluations that the device functions as stated in the specifications and agree to use the device in accordance with the boxes checked below in the "Confirmed Items" section.	
Company :	Date (yy/mm/dd):
Name: Signature:	Department: Title:

Applications (Set)

Check the boxes below, to indicate confirmation of related matters.

Device (Part-Number)	☐ μPD65881GB-P01-3BS-A (μPD71054 function compatible) ☐ μPD65881GB-P02-3BS-A (μPD71051 function compatible) ☐ μPD65881GB-P03-3BS-A (μPD71055 function compatible)	
NEC Electronics Counterpart	Office	
	Name	
Confirmed Items	Confirm the contents below and check the confirmed items. All items must be confirmed and checked. ☐ 1. Differences from the original product (μPD71051/71054/71055) and notes for use of the function-compatible device(s) in the data sheet ☐ 2. Proper operation in the actual application environment, using samples ☐ 3. Necessity of re-evaluation before using in a new or different board or application set ☐ 4. Necessity of using the board with at least four layers and a stable power supply. Conventionally ignored noise entering chips may be interpreted as being normal signals when the function-equivalent product is employed in a more advanced design process.	

Additional Information required:

Demand/Forecast		
M/P starting time	(yy/mm/dd)	
Monthly Run-Rate	(units)	
Comment		

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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