To our customers,

Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD63310

STEREO SOUND CODEC

The μPD63310 is an LSI that features two channels each of on-chip 16-bit ADC and DAC circuits for mutual conversion between digital signals and audio signals (having a maximum signal bandwidth of 24 kHz).

The analog signal input block enables mixed input of four different stereo signals and one monaural signal, and the volume of each signal can be controlled before mixing. The μPD63310 also features two on-chip microphone amplifiers (mic amps) and gain is adjustable between 10 and 30 dB.

The analog signal output block enables mixed output of analog signals output by the DAC and four different stereo analog signals, and the volume of each signal can be controlled before mixing.

The digital audio signal I/O block supports a serial interface for audio applications (two's complement, MSB first).

A 6-bit parallel port are used for the various volume settings, with volume settings selectable (in 1.5-dB steps) from – 46.5 dB to 0 dB, as well as a mute setting.

FEATURES
- Two channels each of $\Delta\Sigma$ type ADC and DAC
- On-chip mixing circuit in analog I/O block
- Low-noise mic amps for two channels on chip
- On-chip reference voltage power supply (1.4 V TYP.)
- ADC and DAC digital filter characteristics
    - Pass band ripple   : ±0.1 dB (0 to 0.454 fs) for ADC and DAC
    - Stop band attenuation : 75 dB (0.546 fs or above) for ADC and DAC
- Sampling frequency (fs): 2 to 48 kHz (256-fs master clock is input from an external source)
- Low voltage operation: +3 to +5.5 V single power supply
- Wide operating ambient temperature: –20 to +80°C
- Low power consumption: 120 mW (when using 3-V power supply), 250 mW (when using 5-V power supply)
- 80-pin plastic TQFP

RECOMMENDED USES
- Speech recognition system, including car navigation system
- PC sound system

ORDERING INFORMATION

Part Number	Package
μPD63310GK-9EU	80-pin plastic TQFP (FINE PITCH) (12 × 12 mm)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

The mark ★ shows major revised points.

BLOCK DIAGRAM

Digital I/O terminals

CSB SELR SO SI BCLK LRCLK RB, WB MCLK DATA5-DATA0 OEB, RBW

2   6   2

I/O interface

Digital filter

Decimeter   Decimeter   Interpolator   Interpolator

Analog loopback
(for test mode selection)

ADC   ADC   DAC   DAC

Mixer   Mixer   Filter   Filter

MIC AMP   MIC AMP

Mixer   Mixer

MICOL MICPL MICNL IN1L IN2L IN3L IN4L IN5 IN1R IN2R IN3R IN4R MICPR MICNR MICOR OUTL DACL OUTR DACR

Analog I/O terminals

PIN CONFIGURATION (Top View)

80-pin plastic TQFP (FINE PITCH) (12 × 12 mm)

- μ**PD63310GK-9EU**

Top-side pins (80 → 61):
NC, NC, MICOR, MICNR, MICPR, AGND1, AGND2, NC, AGND3, VXLO, NC, VXLI, VXRO, VXRI, VRLO, VRLI, VRRO, VRRI, NC, NC

Left pins		Right pins	
IN1R	1	60	AV$_{DD}$
IN2R	2	59	AGND4
IN3R	3	58	AGND5
IN4R	4	57	OUTL
IN5	5	56	DACL
IN4L	6	55	OUTR
IN3L	7	54	DACR
IN2L	8	53	NC
IN1L	9	52	NC
NC	10	51	NC
NC	11	50	NC
NC	12	49	NC
NC	13	48	DATA0
NC	14	47	DATA1
NC	15	46	DATA2
MICOL	16	45	DATA3
MICNL	17	44	DATA4
MICPL	18	43	DATA5
RBW	19	42	DGND2
OEB	20	41	DGND1

Bottom-side pins (21 → 40):
NC, NC, WB, RB, CSB, SELR, TEST1, TEST2, RSTB, NC, MCLK, LRCLK, BCLK, SI, NC, SO, DV$_{DD}$, NC, NC, NC

3

Phase-out/Discontinued

PIN FUNCTIONS

(1/3)

Pin Number	Pin Name	I/O	Function
1	IN1R	I	R-channel analog audio signal input pin 1
2	IN2R	I	R-channel analog audio signal input pin 2
3	IN3R	I	R-channel analog audio signal input pin 3
4	IN4R	I	R-channel analog audio signal input pin 4
5	IN5	I	Analog audio signal (monaural) input pin. This channel accepts audio input which is input to both left and right channels on the chip.
6	IN4L	I	L-channel analog audio signal input pin 4
7	IN3L	I	L-channel analog audio signal input pin 3
8	IN2L	I	L-channel analog audio signal input pin 2
9	IN1L	I	L-channel analog audio signal input pin 1
10-15	NC	—	No connection
16	MICOL	O	L-channel mic amp output pin. If the L-channel mic amp is not being used, connect this pin to MICNL pin.
17	MICNL	I	L-channel mic amp inverting input pin. If the L-channel mic amp is not being used, connect this pin to MICOL pin.
18	MICPL	I	L-channel mic amp noninverting input pin. If the L-channel mic amp is not being used, connect this pin to VXLO pin.
19	RBW	O	Output pin for signal that specifies the bus driver's direction. Output is at high level when DATA5 to DATA0 are input pins and is at low level when DATA5 to DATA0 are output pins. If not used, leave unconnected.
20	OEB	O	Bus driver enable signal output pin. When data input to DATA5 to DATA0 is enabled, output is at low level. If not used, leave unconnected.
21, 22	NC	—	No connection
23	WB	I	Input pin for parallel interface's data write signal. Used for input of low-level signals when addresses are written to the volume setting register and when data is written.
24	RB	I	Input pin for parallel interface's data read signal. Used for input of low-level signals when data is read from the volume setting register.
25	CSB	I	Input pin for parallel interface's chip select signal. Active low. When the input signal is at high level, DATA5 to DATA0 are set for high impedance.
26	SELR	I	Input pin for signal that specifies the target register for parallel data input and output. Specifies an address register when the input signal is at low level, or a data register when the input signal is at high level.
27, 28	TEST1, TEST2	I	Test mode setting pins. These pins set the test mode when at high level. When not used (i.e., during normal operation mode), connect these pins to GND.
★ 29	RSTB	I	Reset signal input pin. A reset occurs when a low pulse (pulse width of 1/(8 fs) or greater) is input after starting MCLK. The case when a reset is necessary is not only power-on but also an occurrence of disturbance in master clock due to changing fs (sampling frequency). When input is at low level, power down mode is set to reduce power consumption.
30	NC	—	No connection

Phase-out/Discontinued

Pin Number	Pin Name	I/O	Function
31	MCLK	I	Master clock input pin. Used for input of 256-fs clock (duty: 40 to 60%).
32	LRCLK	O	Serial interface's frame sync clock output pin. Used for L channel data I/O when LRCLK = low level Used for R channel data I/O when LRCLK = high level
33	BCLK	O	Serial interface's bit sync clock output pin. Used for I/O of audio data from SI and SO in sync with BCLK. BCLK is generated on-chip as MCLK divided by eight.
34	SI	I	Serial interface's data input pin. Used for serial input (synchronized with BCLK) of audio data (two's complement, MSB first).
35	NC	—	No connection
36	SO	O	Serial interface's data output pin. Used for serial output (synchronized with BCLK) of audio data (two's complement, MSB first).
37	DV$_{DD}$	—	Digital power supply pin. Used for input voltage range of +3 to +5.5 V.
38-40	NC	—	No connection
41, 42	DGND1, DGND2	G	Digital ground pins.
43-48	DATA5-DATA0	I/O	Parallel data I/O pins. Used for input/output of address data and volume setting data.
49-53	NC	—	No connection
54	DACR	O	R-channel DAC output pin. When this pin is used, the R-channel DAC output can be monitored without attenuation regardless of the volume setting.
55	OUTR	O	R-channel analog audio output pin.
56	DACL	O	L-channel DAC output pin. When this pin is used, the L-channel DAC output can be monitored without attenuation regardless of the volume setting.
57	OUTL	O	L-channel analog audio output pin.
58, 59	AGND5, AGND4	G	Analog ground pins.
60	AV$_{DD}$	—	Analog power supply pin. Used for input voltage range of +3 to +5.5 V.
61, 62	NC	—	No connection
63	VRRI	I	Reference voltage input pin for R-channel DAC. This pin is usually connected to VRRO pin.
64	VRRO	O	Reference voltage output pin for R-channel DAC. Output is 1.4 V (TYP.). Connects to analog GND via a bypass capacitor.
65	VRLI	I	Reference voltage input pin for L-channel DAC. This pin is usually connected to VRLO pin.
66	VRLO	O	Reference voltage output pin for L-channel DAC. Output is 1.4 V (TYP.). Connects to analog GND via a bypass capacitor.
67	VXRI	I	Reference voltage input pin for R-channel ADC. This pin is usually connected to VXRO pin.
68	VXRO	O	Reference voltage output pin for R-channel ADC. Output is 1.4 V (TYP.). Connects to analog GND via a bypass capacitor.
69	VXLI	I	Reference voltage input pin for L-channel ADC. This pin is usually connected to VXLO pin.
70	NC	—	No connection

Phase-out/Discontinued

(3/3)

Pin Number	Pin Name	I/O	Function
71	VXLO	O	Reference voltage output pin for L-channel ADC. Output is 1.4 V (TYP.). Connects to analog GND via a bypass capacitor.
72	AGND3	G	Analog ground pin.
73	NC	—	No connection
74, 75	AGND2, AGND1	G	Analog ground pins.
76	MICPR	I	R-channel mic amp noninverting input pin. If the R-channel mic amp is not being used, connect this pin to VXRO pin.
77	MICNR	I	R-channel mic amp inverting input pin. If the R-channel mic amp is not being used, connect this pin to MICOR pin.
78	MICOR	O	R-channel mic amp output pin. If the R-channel mic amp is not being used, connect this pin to MICNR pin.
79, 80	NC	—	No connection

1. DESCRIPTION OF OPERATIONS

1.1 Analog Input Block

The analog input block enables signal input from two channels. Four different stereo signals (IN1 to IN4) and a monaural signal (IN5) can be mixed and input via these channels. The volume can be adjusted for each analog signal, and the sum of the volume settings is input to the ADC. A 6-bit signal is used to adjust the volume within an adjustment range (in 1.5-dB steps) from –46.5 dB to 0 dB, plus a mute setting. A low-noise mic amp (variable gain width: 10 to 30 dB) is provided on-chip for mic input.

1.2 Analog Output Block

The analog output block enables signal output from two channels. Five different analog signals (IN1 to IN4 and DAC) can be mixed and output via these channels. The volume can be adjusted for each analog signal, and the sum of the volume settings is output (via OUTL and OUTR pins). A 6-bit signal is used to adjust the volume within an adjustment range (in 1.5-dB steps) from –46.5 dB to 0 dB, plus a mute setting. The output from the DAC (via DACL and DACR pins) can be monitored directly.

1.3 Digital Interface

A serial interface for audio is supported for input and output of digital audio data (two's complement, MSB first). BCLK and LRCLK are automatically generated on chip from the master clock that is supplied to MCLK pin from an external source. BCLK and LRCLK are used by the ADC and DAC. In other words, the ADC's and DAC's sampling frequency is determined based on the master clock and cannot be set independently of it.

A parallel interface is used for input and output of the 6-bit data used for volume adjustments. The target registers for parallel data I/O are selected via the SELR pin. This pin selects an address register when at low level and a data register when at high level.

OEB is output as the bus driver's enable signal and RBW is output as the bus driver's direction specification signal. Use this pin as necessary. If it is not used, leave it unconnected.

When the clock (data) input to the MCLK and SI pins has been stopped, set these pins to either high level or low level (if necessary, connect via a resistance to DV$_{DD}$ or DGND).

(1) Serial interface
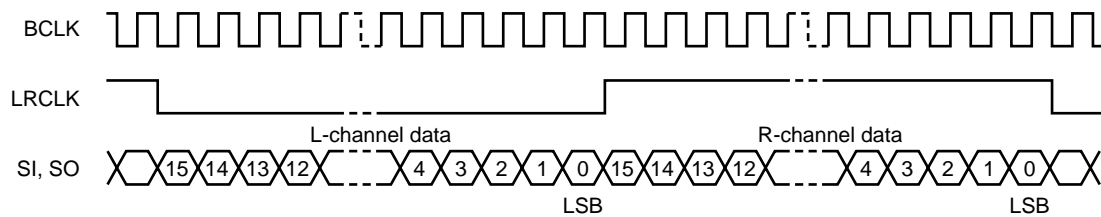
(2) Parallel interface

Phase-out/Discontinued
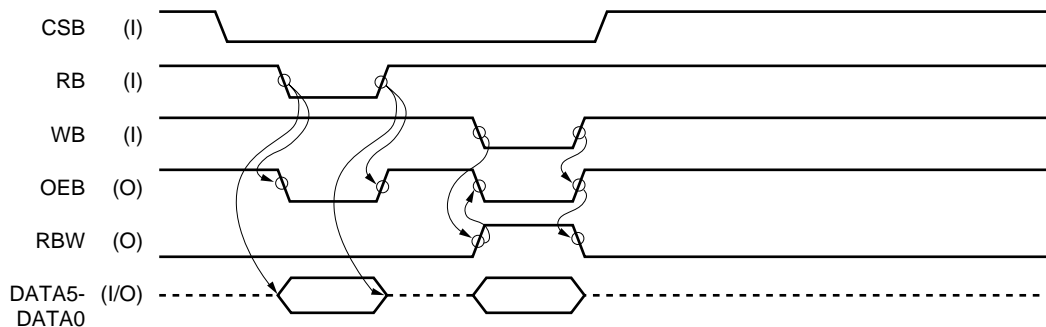
1.4 Volume Setting Register Addresses

After the power is turned on and a reset has been input, all volume settings are set to mute mode. Therefore, it may be necessary to specify volume settings before inputting signals. Write data to the volume setting registers that correspond to the analog input pins and analog output pins to be used.

Since the ADC's full scale analog input signal amplitude voltage is 1.4 V (TYP.), it may be necessary to specify a volume setting whereby the signal amplitude's maximum voltage (after mixing) is no more than 1.4 V, especially when several analog signals are input to the ADC after mixing.

The addresses of the various volume setting registers are specified via the 6-bit parallel data that is input from the DATA5 to DATA0 pins during low-level input to the SELR pin. The volume setting registers corresponding to these addresses are listed below.

  0   : IN1L control register
  1   : IN1R control register
  2   : IN2L control register
  3   : IN2R control register
  4   : IN3L control register
  5   : IN3R control register
  6   : IN4L control register
  7   : IN4R control register
  8   : IN5 control register
  9   : IN1L-OUTL control register
  10 : IN1R-OUTR control register
  11 : IN2L-OUTL control register
  12 : IN2R-OUTR control register
  13 : IN3L-OUTL control register
  14 : IN3R-OUTR control register
  15 : IN4L-OUTL control register
  16 : IN4R-OUTR control register
  17 : DACL-OUTL control register
  18 : DACR-OUTR control register

1.5 Volume Setting Register Data (Command Types)

The data in the volume setting registers is written and read based on 6-bit parallel data that is input and output via the DATA5 to DATA0 pins when the SELR pin is set for high level input. The data (commands) in the various volume setting registers are described below.

0:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN1L register's input signal, with codes corresponding to the gain levels listed in Table 1-1 below. When D5 is "1", mute mode is set.

Table 1-1. Correspondence of Codes and Gain Levels

D5	D4	D3	D2	D1	D0	Gain
0	0	0	0	0	0	0 dB
0	0	0	0	0	1	−1.5 dB
0	0	0	0	1	0	−3.0 dB
0	1	1	1	1	0	−45.0 dB
0	1	1	1	1	1	−46.5 dB
1	0	0	0	0	0	MUTE[Note]
1	×	×	×	×	×	MUTE

Note Default value

Remark × : Don't care

1:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN1R register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

2:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN2L register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

3:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN2R register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

4:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN3L register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

5:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN3R register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

6:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN4L register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

7:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN4R register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

8:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate the data used to control gain in the IN5 register's input signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

9:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN1L register's input signal with the L-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

10:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN1R register's input signal with the R-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

11:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN2L register's input signal with the L-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

12:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN2R register's input signal with the R-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

13:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN3L register's input signal with the L-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

14:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN3R register's input signal with the R-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

15:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN4L register's input signal with the L-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

16:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when mixing the IN4R register's input signal with the R-channel DAC's output signal, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

17:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when outputting the L-channel DAC's output signal to OUTL, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

18:

D5	D4	D3	D2	D1	D0

D4 to D0 indicate data that controls the gain when outputting the R-channel DAC's output signal to OUTR, with codes corresponding to the gain levels listed in Table 1-1. Mute mode is set when D5 = 1.

1.6 Test Mode

Test mode is set (and MCLK input is required) when the TEST1 and TEST2 pins are at high level. When in test mode, the IC internally inputs the ADC's output directly to the DAC (via an analog loopback). This analog loopback enables verification of analog circuit operations and the volume settings.

2. SYSTEM CONNECTIONS

2.1 Analog Input Block

A frequency that is one half of the master clock (MCLK) frequency is used as the ADC's and DAC's oversampling frequency. Accordingly, if there is no input of high-frequency noise that is close to MCLK/2 (= 128 fs), the filter (LPF) inserted before the analog block can be omitted (see **Figure 2-1**).

The analog signal input pins (pins 1 to 9) are internally biased to 1.4 V (TYP.), so a coupling capacitor (1 to 4.7 μF) should be inserted.

The full scale analog input signal level is 1.4 V_{p-p} (TYP.). Adjust the transmitting side's level so that the amplitude of the signal that is input to an analog audio signal input pin does not exceed 1.4 V_{p-p}. In particular, if this signal's amplitude exceeds 2.8 V_{p-p}, the analog signal input pin's voltage may become less than 0 V during negative amplitude, which may prevent the volume control from operating normally (such as when there is signal leakage during mute mode).

Analog signal input pins that are not used should be left unconnected or connected to a GND pin via a capacitor.

Figure 2-1. Analog Input Block Connection Example (Using IN1R Pin)
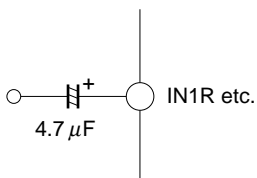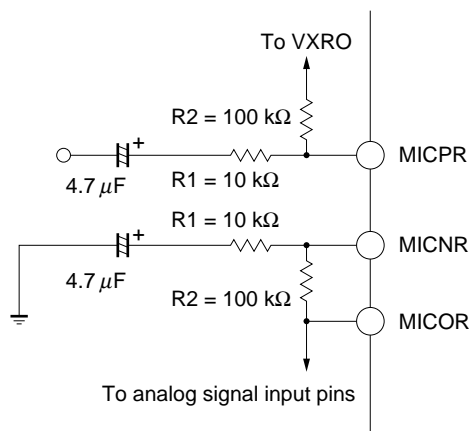

2.2 Mic Amp

The mic amp's gain can be adjusted (between 10 dB (MIN.) and 30 dB (MAX.)) via an external resistor. The gain setting is adjusted by changing R1. R2 is fixed at 100 kΩ (see **Figure 2-2**). Gain is calculated via the following expression.

Mic amp gain calculation: $A_V = 20 \log ((R2 + R1)/R1)$ [dB]

Since the mic amp is independent from other blocks, if the mic amp's output is input to the ADC (or is mixed with output from the DAC), the mic amp's output pin should be connected via a coupling capacitor to one of the analog signal input pins (see **Figure 2-1**).

Separate the unused mic amp from R1 and the electrolytic capacitors (shown in Figure 2-2) and set 0 Ω for R2.

Figure 2-2. Mic Amp Connection Example (Using Right Side)

Remark When the above example is a constant, the mic amp's gain becomes about 21 dB.

2.3 Analog Output Block

The analog audio output pins (OUTL and OUTR) and the DAC output pins (DACL and DACR) are internally biased to 1.4 V (TYP.), so an output coupling capacitor should be inserted to cut the DC component (see **Figure 2-3**).

The out-of-band component of the output signals from these analog pins is attenuated by a post filter (LPF) in the IC, so there is no need for an external LPF.

Set the load resistance to at least 20 kΩ (the speakers cannot be directly driven, so insert a power amp IC before the speaker).

Analog audio output pins and DAC output pins that are not used can be left unconnected.

Figure 2-3. Analog Output Block Connection Example
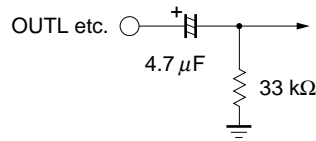
2.4 Use Cautions

When changing the volume (addresses 17 and 18) between the DAC output and the output mixer, noise ("pop noise") may be output from an analog audio output pins (OUTL or OUTR). Such noise is due to the output offset voltage of an on-chip DAC.

If this noise is audible enough to be a problem, take the following measures.

(1) Set mute mode for the volume (addresses 17 and 18) between the DAC output and the output mixer.
(2) Connect the DAC output pins (DACL and DALR) via a capacitor to a pair of unused analog input pins (such as IN4L and IN4R).
(3) Adjust the volume (such as addresses 15 and 16) between the analog input pins connected as described in (2) above and the output mixer to adjust the DAC output volume.

Phase-out/Discontinued

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (unless otherwise specified, DGND = AGND = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	All V_{DD} pins	−0.3 to +7.0	V
Analog input voltage	V_{AIN}	All analog input pins	−0.3 to V_{DD} +0.3	V
Digital input voltage	V_{DIN}	All digital input pins	−0.3 to V_{DD} +0.3	V
Applied voltage to analog output pin	V_{AOUT}	All analog output pins	−0.3 to V_{DD} +0.3	V
Applied voltage to digital output pin	V_{DOUT}	All digital output pins	−0.3 to V_{DD} +0.3	V
Operating ambient temperature	T_A		−20 to +80	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution   If the absolute maximum rating for any of the above parameters is exceeded even momentarily, it may adversely affect the quality of this product. In other words, these absolute maximum ratings have been set to prevent physical damage to the product. Do not use the product in such a way as to exceed any of these ratings.

Recommended Operating Conditions (unless otherwise specified, DGND = AGND = 0 V, load capacitance = 20 pF, and on-chip reference voltage power supply is used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	All V_{DD} pins	3.0		5.5	V
Operating ambient temperature	T_A		−20	25	80	°C
Master clock frequency	f_{MCLK}	256 fs	0.512		12.288	MHz
Sampling frequency	fs		2		48	kHz
Digital input voltage (high level)	V_{IH}	When V_{DD} = 5.0 V	4.5		5	V
Digital input voltage (low level)	V_{IL}	When V_{DD} = 5.0 V	0		1.0	V
Digital input voltage (high level)	V_{IH}	When V_{DD} = 3.3 V	2.64		3.3	V
Digital input voltage (low level)	V_{IL}	When V_{DD} = 3.3 V	0		0.66	V
RSTB rise time	t_{rRSTB}	Time required to change from 10% to 90% of V_{DD}	—		1	μs
Analog input signal voltage	V_I	All analog input pins	—		1.4	$V_{p\text{-}p}$
ADC input signal voltage	V_{IADC}	Mixer output section (before ADC)	—		1.4	$V_{p\text{-}p}$
Analog output signal voltage	V_O	OUTL and OUTR pins (mixer output section)	—		1.4	$V_{p\text{-}p}$
Analog output pin load resistance	RL	All analog output pins	20		—	kΩ
Mic amp voltage gain	A_{VMIC}		10	20	30	dB

DC Characteristics (unless otherwise specified, T$_A$ = –20 to +80°C, DV$_{DD}$ = AV$_{DD}$ = 3.0 to 5.5 V, DGND = AGND = 0 V)

(1) Power consumption

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating current	I$_{DD}$	When V$_{DD}$ = 5.0 V	—	50	70	mA
Operating current	I$_{DD}$	When V$_{DD}$ = 3.0 V	—	40	60	mA
Standby current	I$_{DDstb}$	Power down mode	—	1.5	2	mA

(2) Digital block

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I$_{LI}$	When V$_{DD}$ = 5.0 V and V$_I$ = 5.0 to 0.0 V	–5.0		+5.0	μA
Output leakage current	I$_{LO}$	When V$_{DD}$ = 5.0 V and V$_O$ = 5.0 to 0.0 V (high impedance)	–5.0		+5.0	μA
High-level output current	I$_{OH}$	When V$_{DD}$ = 5.0 V and V$_O$ = 4.0 V	–2.0		—	mA
Low-level output current	I$_{OL}$	When V$_{DD}$ = 5.0 V and V$_O$ = 0.4 V	—		+2.0	mA
High-level output voltage	V$_{OH}$	When V$_{DD}$ = 5.0 V and I$_O$ = –2.0 mA	4.0		—	V
Low-level output voltage	V$_{OL}$	When V$_{DD}$ = 5.0 V and I$_O$ = 2.0 mA	—		0.4	V
High-level output voltage	V$_{OH}$	When V$_{DD}$ = 3.3 V and I$_O$ = –2.0 mA	2.64		—	V
Low-level output voltage	V$_{OL}$	When V$_{DD}$ = 3.3 V and I$_O$ = 2.0 mA	—		0.4	V

(3) Analog block

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference power supply output voltage, AD side	V$_{XL (R)}$	VXRO and VXLO pins	1.35	1.4	1.45	V
Reference power supply output voltage, DA side	V$_{RL (R)}$	VRRO and VRLO pins	1.35	1.4	1.45	V
Input resistance 1	R$_{I1}$	IN1L, IN2L, IN3L, IN4L, IN1R, IN2R, IN3R, and IN4R pins	6.5	10	15	kΩ
Input resistance 2	R$_{I2}$	IN5 pin	13	20	30	kΩ

Transmission Characteristics (unless otherwise specified, T$_A$ = –20 to +80°C, DV$_{DD}$ = AV$_{DD}$ = 3.0 to 5.5 V, DGND = AGND = 0 V, master clock = 12.288 MHz, and on-chip reference voltage power supply is used)

(1) AD side

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
AD peak S/N	SNP$_X$	Signal = 1 kHz, in 0 to 20 kHz bandwidth	60	75	—	dB
AD dynamic range	SN$_X$	–60 dB input	60	75	—	dB
AD idle noise	ICN$_X$		—	–75	–60	dB
AD absolute gain	G$_X$	Signal = 1 kHz, 0 dB input	–1.0	±0.5	+1.0	dB
AD relative gain 1	G$_{VX}$1	–22.5 to –1.5 dB (0-dB reference)	–2.0	±1.0	+2.0	dB
AD relative gain 2	G$_{VX}$2	–46.5 to –24.0 dB (0-dB reference)	–5.0	±2.0	+5.0	dB
AD frequency gain characteristic	GR$_X$	0 to 20 kHz	–0.5	±0.1	+0.5	dB
AD total harmonic distortion	THD$_X$	Signal = 1 kHz, 0 dB input	—	–50	–40	dB
AD full-scale analog input amplitude	VIFS	Signal = 1 kHz, 0 dB input	1.35	1.4	1.45	V$_{p\text{-}p}$
AD offset voltage	V$_{OFFX}$		–100	±10	+100	mV

(2) DA side

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DA peak S/N	SNP$_R$	Signal = 1 kHz, in 0 to 20 kHz bandwidth	60	75	—	dB
DA dynamic range	SN$_R$	–60 dB input	60	75	—	dB
DA idle noise	ICN$_R$		—	–75	–60	dB
DA absolute gain	G$_R$	Signal = 1 kHz, 0 dB input	–1.0	±0.5	+1.0	dB
DA relative gain 1	G$_{VR}$1	–22.5 to –1.5 dB (0-dB reference)	–2.0	±1.0	+2.0	dB
DA relative gain 2	G$_{VR}$2	–46.5 to –24.0 dB (0-dB reference)	–5.0	±3.0	+5.0	dB
DA frequency gain characteristic	GR$_R$	0 to 20 kHz	–0.5	±0.2	+0.5	dB
DA total harmonic distortion	THD$_R$	Signal = 1 kHz, 0 dB input	—	–50	–40	dB
DA full-scale analog output amplitude	VOFS	Signal = 1 kHz, 0 dB input	1.35	1.4	1.45	V$_{p\text{-}p}$
DA offset voltage	V$_{OFFR}$		–100	±30	+100	mV

Phase-out/Discontinued

AC Characteristics (unless otherwise specified, T$_A$ = –20 to +80°C, DV$_{DD}$ = AV$_{DD}$ = 3.0 to 5.5 V, DGND = AGND = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	RSTB-CSB setup time	t$_{RSUC}$		0		—	ns
★	RSTB-SELR setup time	t$_{RSUS}$		0		—	ns
★	CSB-WB setup time	t$_{CSSUW}$		0		—	ns
	SELR-WB setup time	t$_{SESU}$		0		—	ns
	SELR-WB hold time	t$_{SEHD}$		60		—	ns
	Time between SELR and WB	t$_{BSW}$		0		—	ns
	WB-CSB hold time	t$_{CSHD}$		60		—	ns
	WB low-level width	t$_{STW}$		120		—	ns
	RB low-level width	t$_{RSTW}$		200		—	ns
	Data valid time after WB ↓	t$_{WDDV}$		0		90	ns
	DATA-WB setup time	t$_{WDSU}$		30		—	ns
	WB-DATA hold time	t$_{DHDW}$		30		—	ns
	Time between SELR and RB	t$_{BSR}$		0		—	ns
★	RB-SELR hold time	t$_{SEHDR}$		60		—	ns
	Data delay time after RB ↓	t$_{RDDV}$		0		150	ns
	RB-DATA hold time	t$_{DHDR}$		0		20	ns
	DATA-CSB hold time	t$_{CSHDR}$		30		—	ns
	DATA IN setup time	t$_{DIS}$		100		—	ns
	DATA IN hold time	t$_{DIH}$		100		—	ns
	DATA OUT setup time	t$_{DOD}$		–40		+65	ns
	DATA OUT hold time	t$_{BLD}$		0		45	ns

Phase-out/Discontinued

★ **Parallel interface write timing 1**

RSTB	
	t_{RSUC}
CSB	
	t_{CSSUW} ... t_{CSHD}
SELR	
	t_{RSUS} t_{SESU} t_{SEHD} t_{BSW}
WB	
	t_{STW}
DATA5-DATA0	
	t_{WDDV} t_{WDSU} t_{DHDW} t_{WDDV} t_{WDSU} t_{DHDW}
OEB	
RBW	
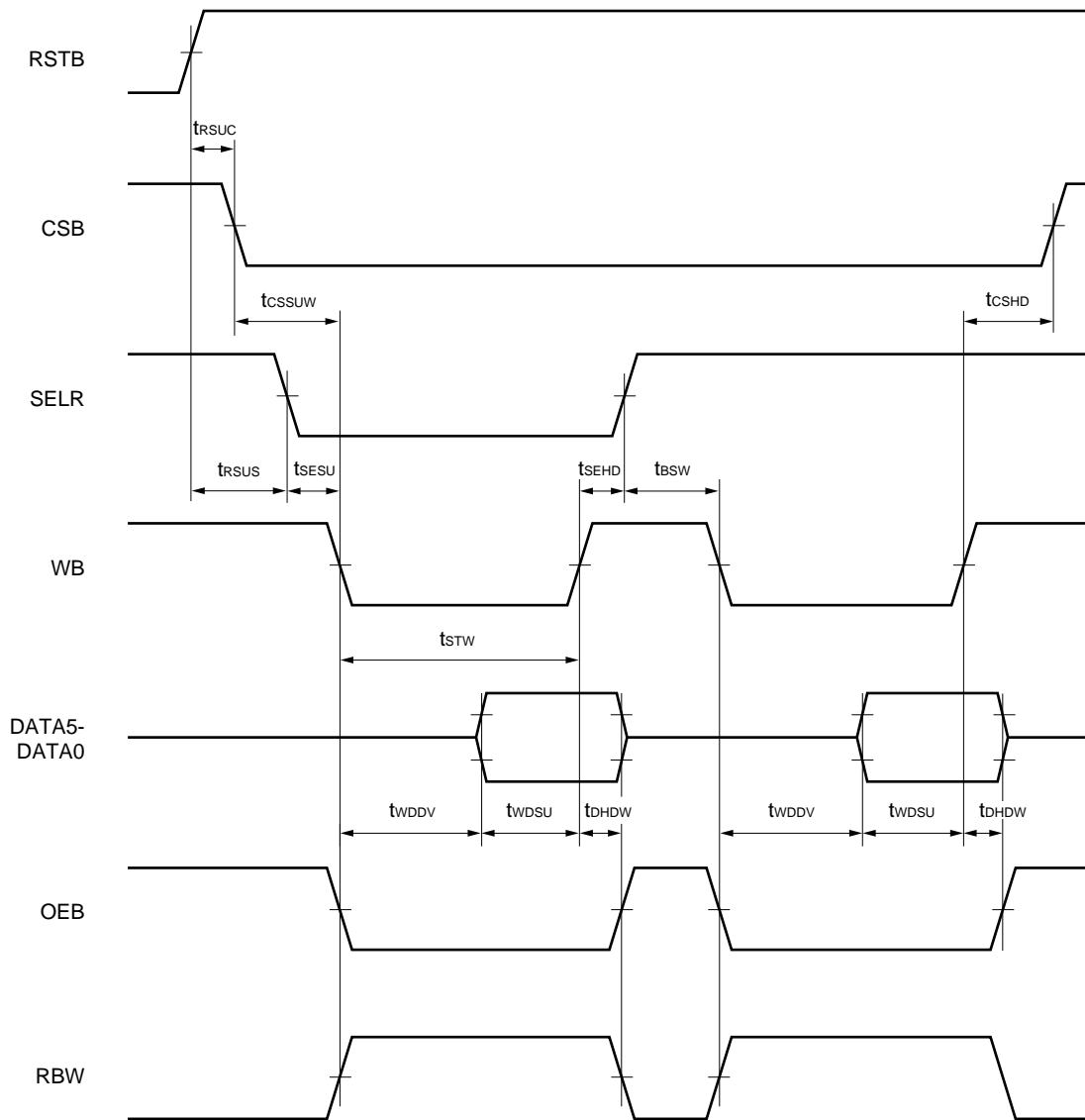
★ **Parallel interface write timing 2 (when there are continual write cycles while CSB is low)**

the different part from "Parallel Interface write timing 1"

Phase-out/Discontinued
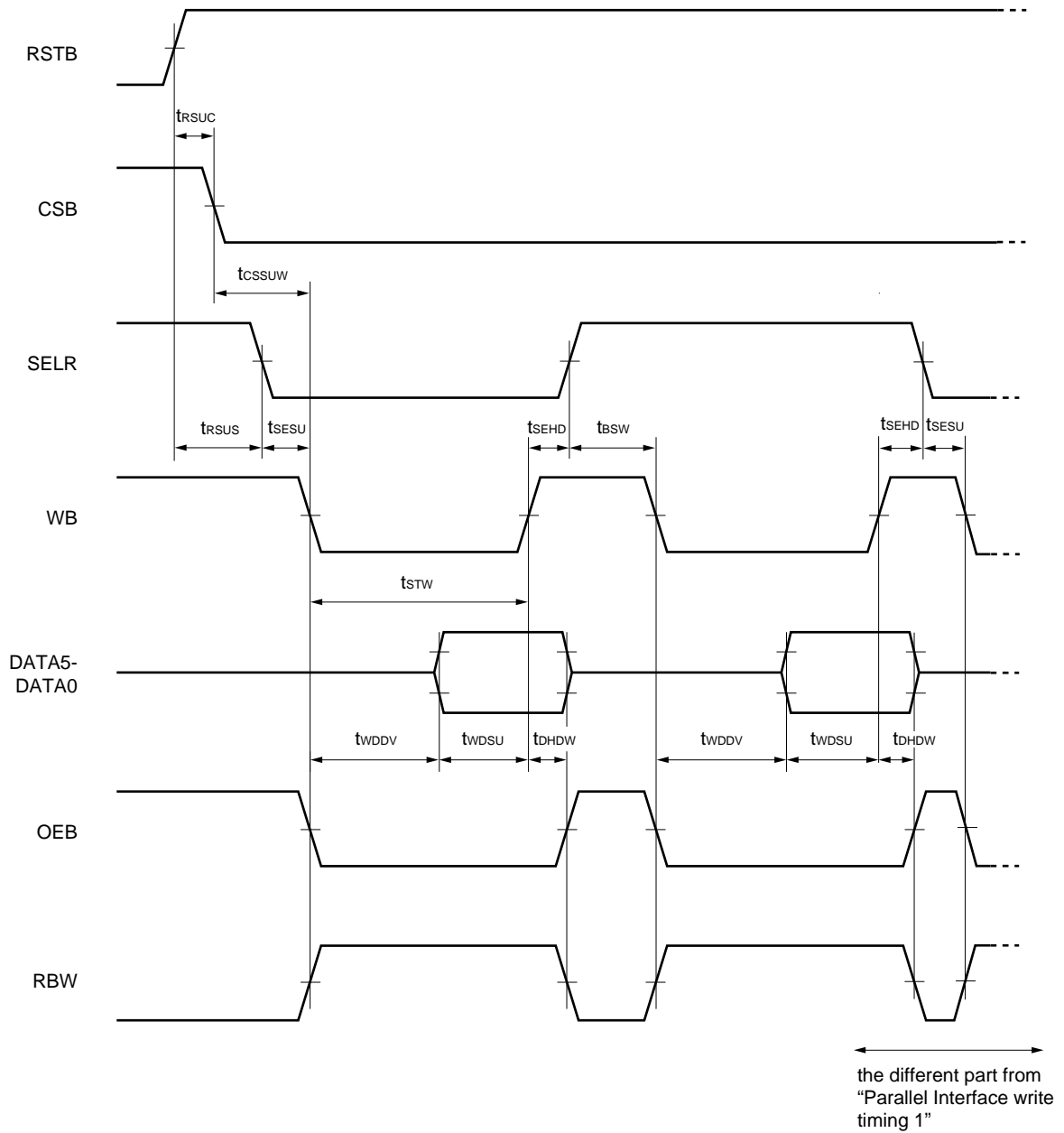
★ **Parallel interface read timing 1**
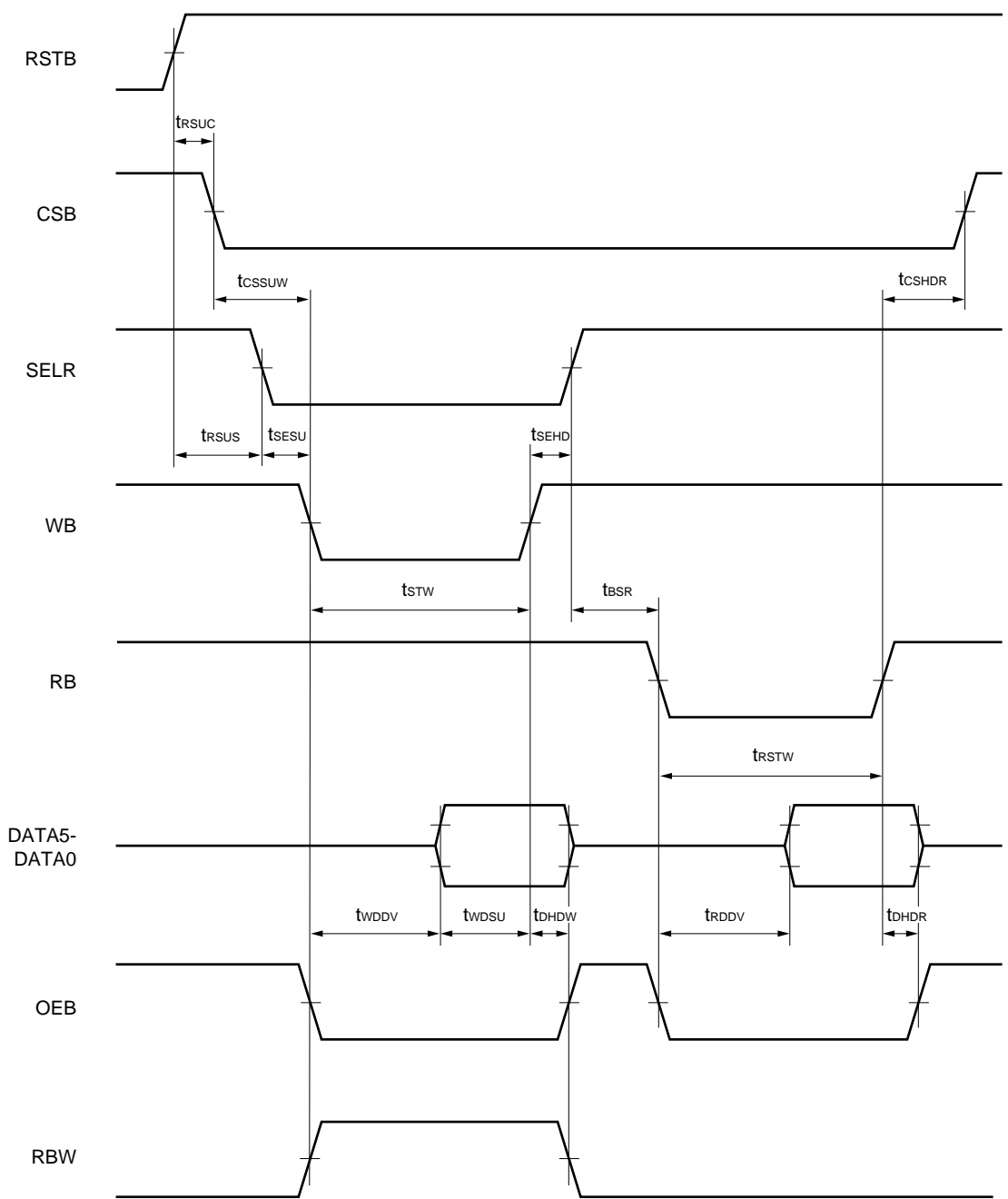
★ **Parallel interface read timing 2 (when there are continual read cycles while CSB is low)**

the different part from
"Parallel Interface read
timing 1"
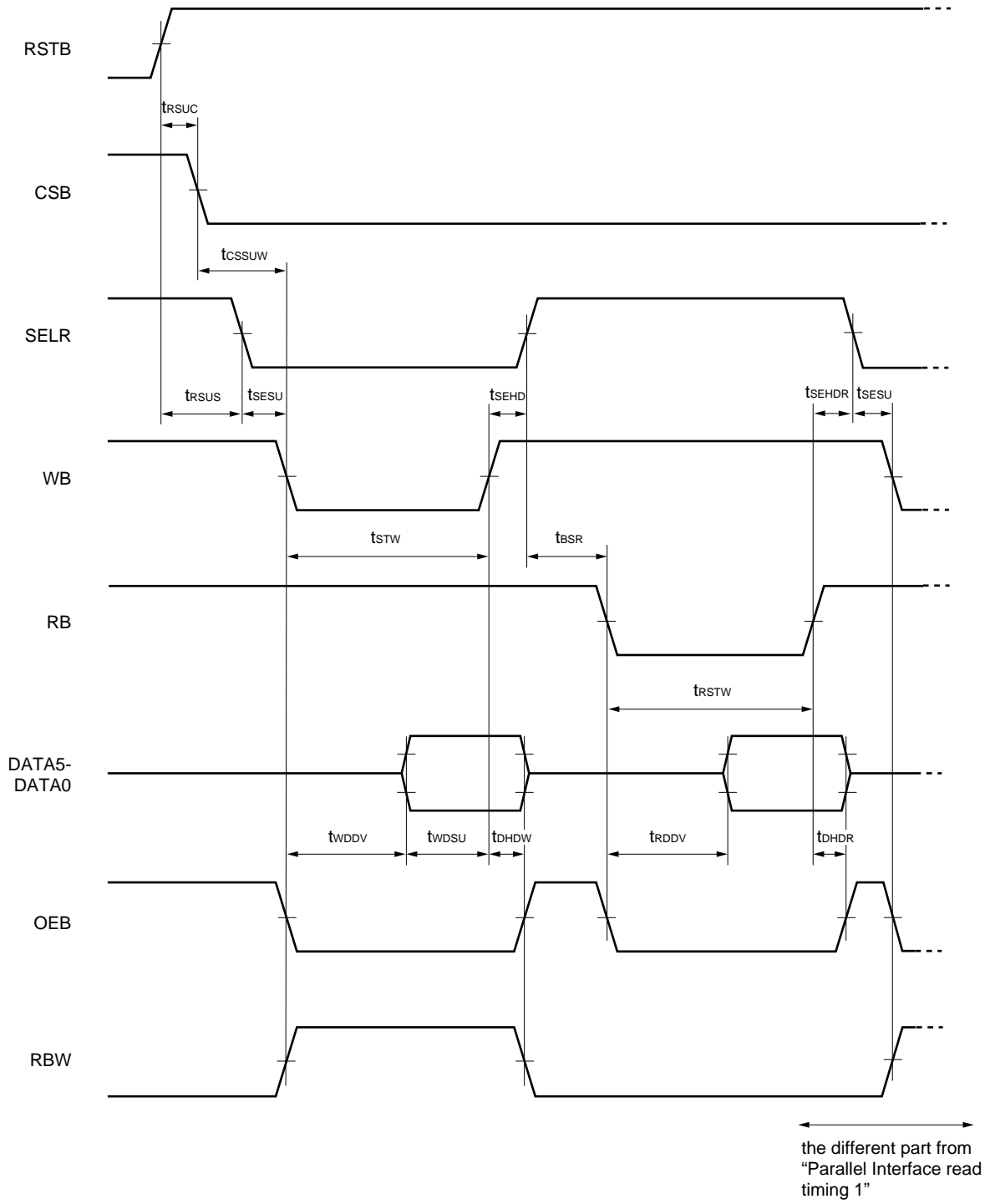
Serial interface input timing

BCLK

t_{DIS} t_{DIH}

SI
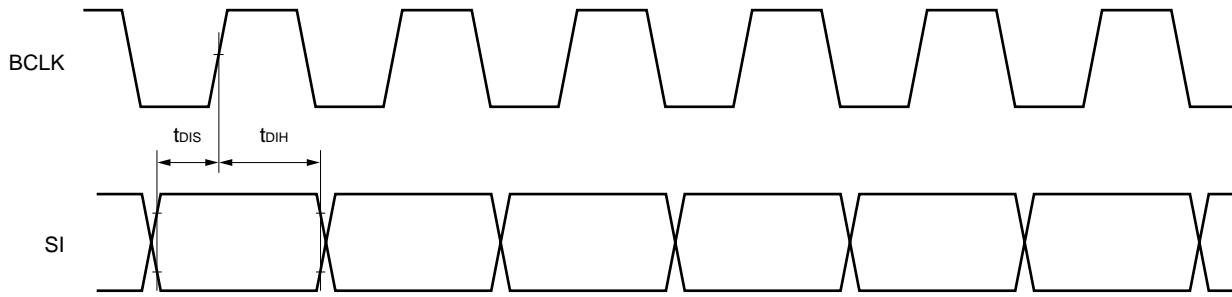
Serial interface output timing

BCLK

t_{DOD}

SO

t_{BLD} t_{BLD}

LRCLK

Phase-out/Discontinued
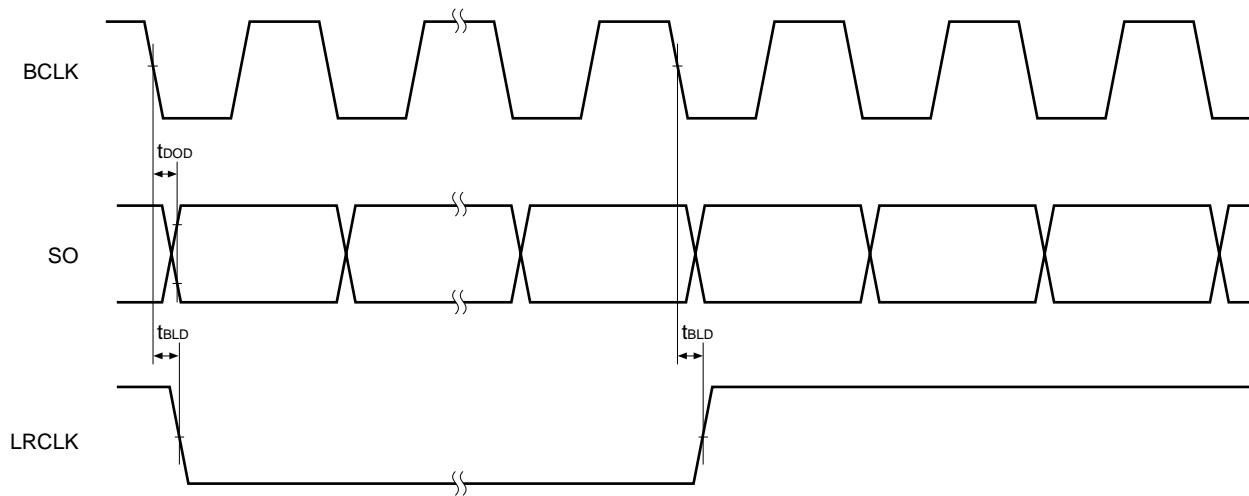
4. APPLICATION CIRCUIT EXAMPLE
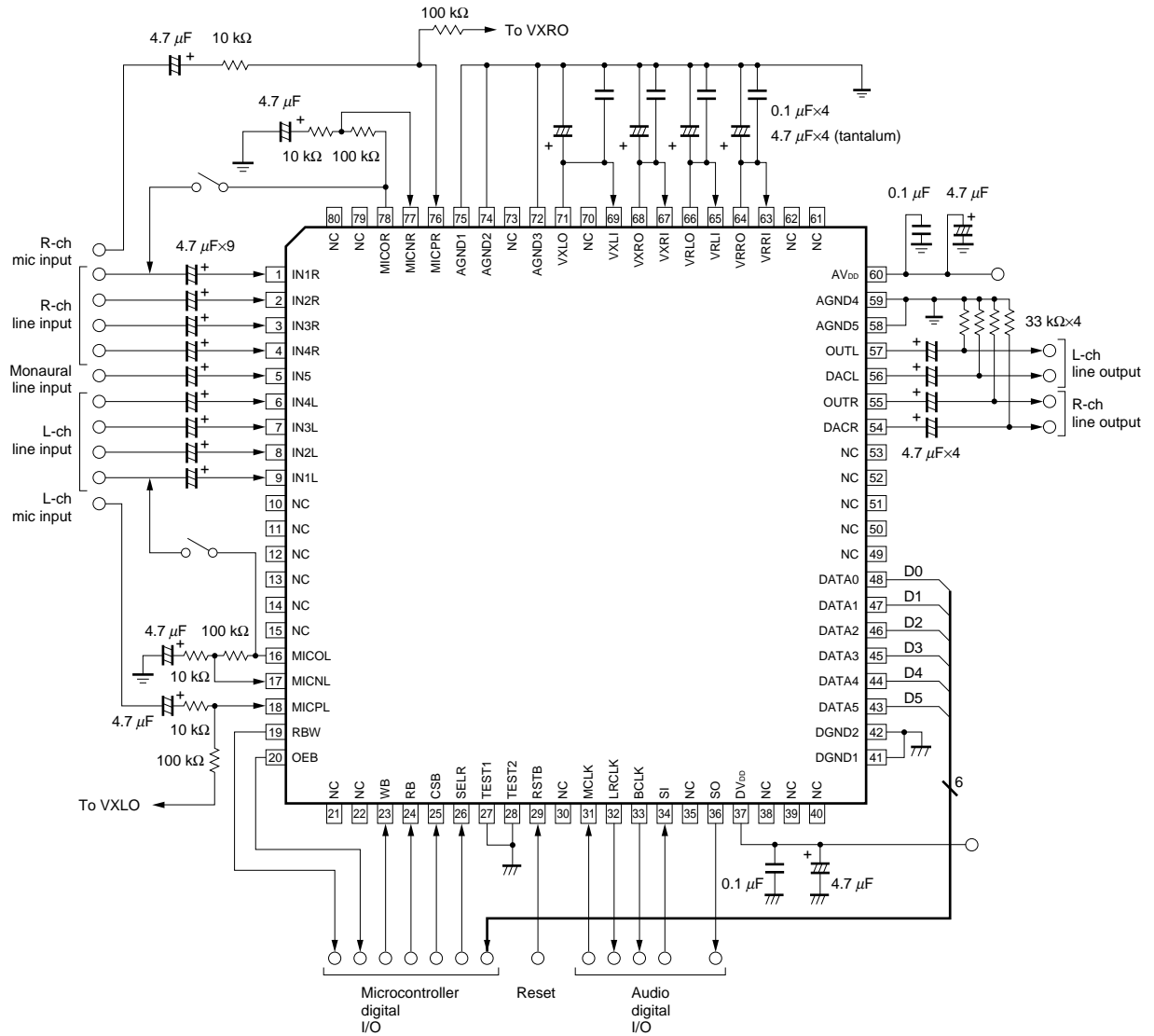
Remark ⏚ : Analog ground

⏚ : Digital ground

Phase-out/Discontinued

5. RECOMMENDED LAYOUT PATTERN

When laying out the power supply lines and GND lines on the circuit board, refer to the following figure concerning the layout of bypass capacitors.

Figure 5-1. Diagram of Recommended Bypass Capacitor Connections (Top View)
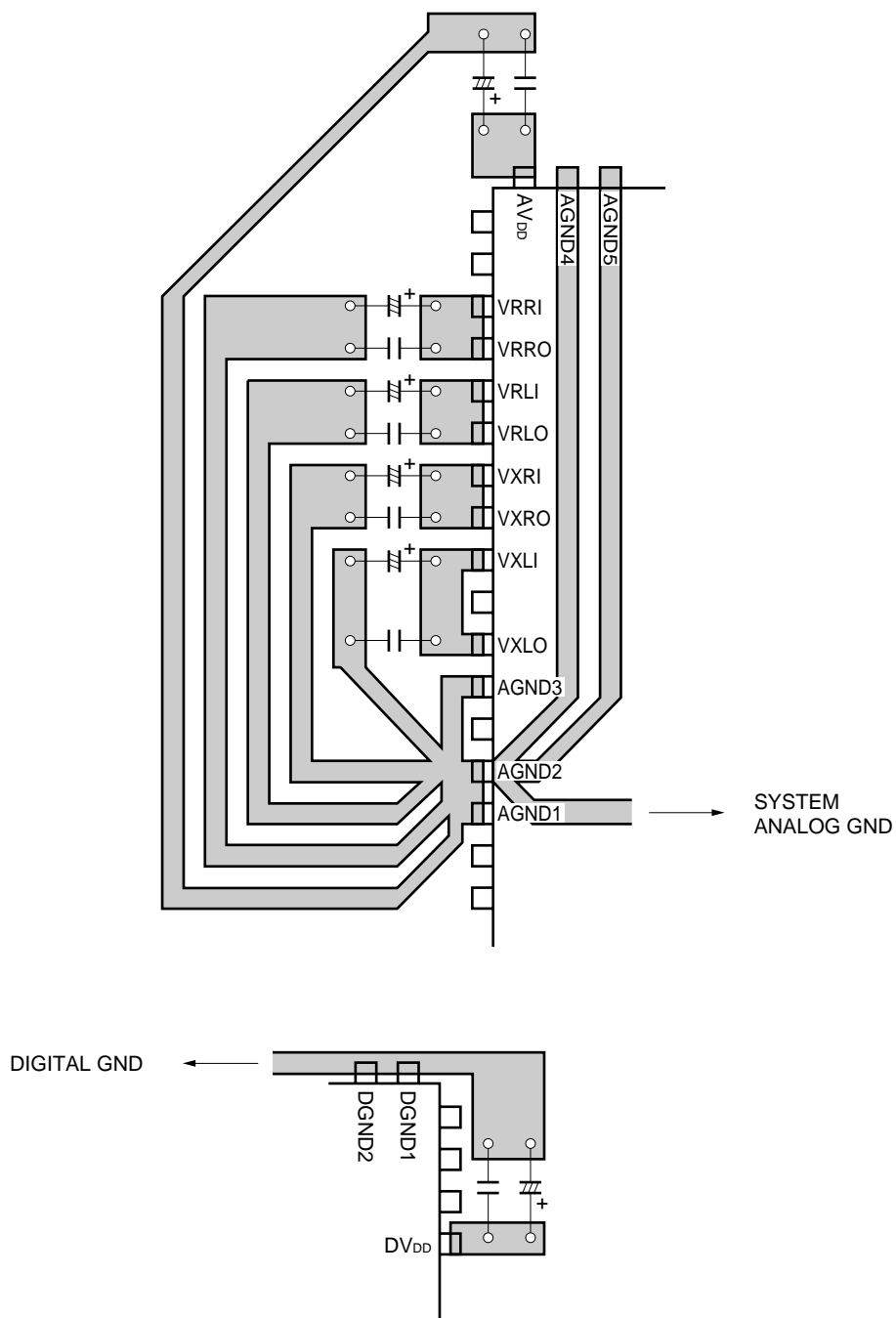
Remark $\overset{+}{\rule[0.5ex]{0pt}{0pt}}\hspace{-0.5em}\parallel$ (4.7 μF) : Tantalum capacitor

$\perp$ (0.1 μF) : Chip ceramic capacitor

Phase-out/Discontinued

6. PACKAGE DRAWING

80 PIN PLASTIC TQFP (FINE PITCH) (□12)

detail of lead end
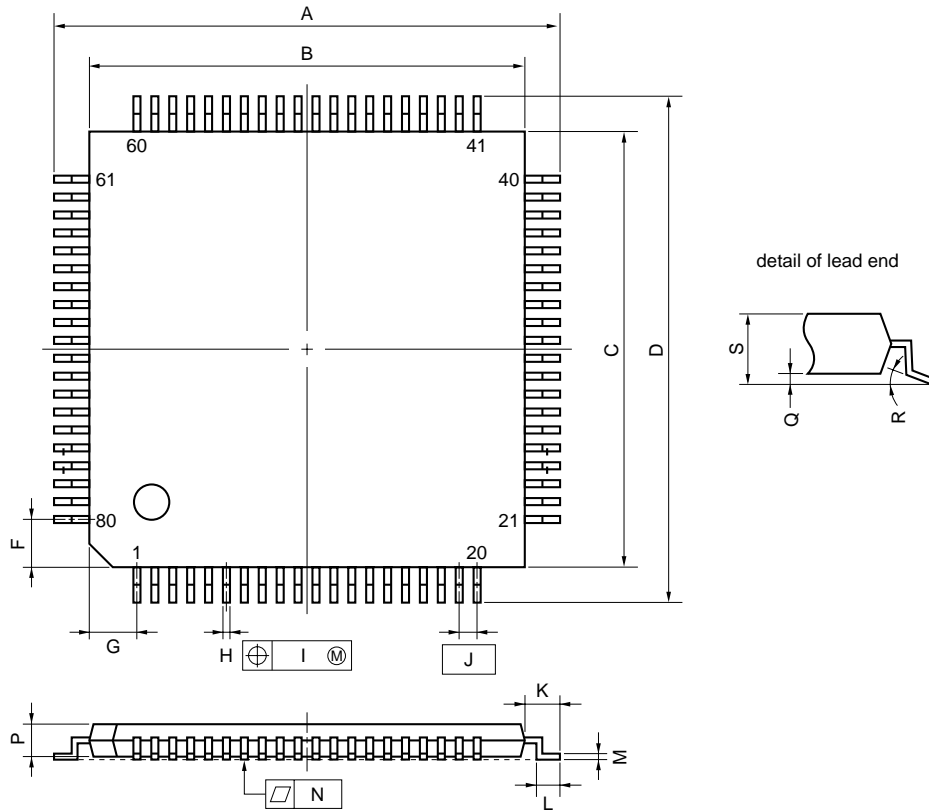
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	0.551±0.008
F	1.25	0.049
G	1.25	0.049
H	0.22±0.05	$0.009^{+0.002}_{-0.003}$
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.145±0.05	$0.006^{+0.002}_{-0.003}$
N	0.10	0.004
P	1.0±0.05	$0.040^{+0.002}_{-0.003}$
Q	0.1±0.05	0.004±0.002
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.2 MAX.	0.048 MAX.

S80GK-50-9EU

7. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our sales representative.

Table 7-1. Soldering Conditions for Surface Mounting Type

μPD63310GK-9EU: 80-pin plastic TQFP (FINE PITCH) (12 × 12 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (at 210°C or higher), Number of reflow processes: 2 max., Exposure limit**Note**: 7 days (after that, prebaking is necessary at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (at 200°C or higher), Number of reflow processes: 2 max., Exposure limit**Note**: 7 days (after that, prebaking is necessary at 125°C for 10 hours)	VP15-107-2
Pin partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per device side)	—

Note The number of days for storage after the dry pack has been opened. Storage conditions are 25°C and 65% RH max.

Caution Do not use two or more soldering methods in combination (except for pin partial heating method).

Phase-out/Discontinued

─── **NOTES FOR CMOS DEVICES** ───

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**
Note:
Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**
Note:
No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**
Note:
Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Phase-out/Discontinued