μPD48288118-A

288M-BIT Low Latency DRAM
Separate I/O

Description

  The μPD48288118-A is a 16,777,216 word by 18 bit synchronous double data rate Low Latency RAM fabricated with advanced CMOS technology using one-transistor memory cell.

  The μPD48288118-A integrates unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (CK and CK#) are latched on the positive edge of CK and CK#.

  These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

Specification

- Density: 288M bit
- Organization
  - Separate I/O: 2M words x 18 bits x 8 banks
- Operating frequency: 400 / 300 MHz
- Interface: HSTL I/O
- Package: 144-pin TAPE FBGA
  - Package size: 18.5 x 11
  - Leaded and Lead free
- Power supply
  - 2.5 V V_{EXT}
  - 1.8 V V_{DD}
  - 1.5 V or 1.8 V V_{DDQ}
- Refresh command
  - Auto Refresh
  - 8192 cycle / 32 ms for each bank
  - 64K cycle / 32 ms for total
- Operating case temperature : Tc = 0 to 95°C

Features

- SRAM-type interface
- Double-data-rate architecture
- PLL circuitry
- Cycle time: 2.5 ns @ t_{RC} = 20 ns
  3.3 ns @ t_{RC} = 20 ns
- Non-multiplexed addresses
- Multiplexing option is available.
- Data mask for WRITE commands
- Differential input clocks (CK and CK#)
- Differential input data clocks (DK and DK#)
- Data valid signal (QVLD)
- Programmable burst length: 2 / 4 / 8
- User programmable impedance output (25 Ω - 60 Ω)
- JTAG boundary scan

Ordering Information

Part number	Cycle Time ns	Clock Frequency MHz	Random Cycle ns	Organization (word x bit)	Core Supply Voltage (V_{EXT}) V	Core Supply Voltage (V_{DD}) V	Output Supply Voltage ($V_{DD}Q$) V	Package
μPD48288118FF-E33-DW1-A	3.3	300	20	16M x 18	2.5 + 0.13	1.8 ± 0.1	1.8 ± 0.1	144-pin TAPE FBGA (18.5 x 11) Lead-free
μPD48288118FF-EF25-DW1-A	2.5	400	20		2.5 − 0.12		1.5 ± 0.1	
μPD48288118FF-EF33-DW1-A	3.3	300	20					

Remark Products with –A at the end of part number are lead-free products.

Pin Configurations

# indicates active LOW signal.

144-pin TAPE FBGA (18.5 x 11)

(Top View) [Separate I/O x18]

	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{REF}	V_{SS}	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TMS	TCK
B	V_{DD}	D4	Q4	V_{SSQ}					V_{SSQ}	Q0	D0	V_{DD}
C	V_{TT}	D5	Q5	V_{DDQ}					V_{DDQ}	Q1	D1	V_{TT}
D	Note 1 (A22)	D6	Q6	V_{SSQ}					V_{SSQ}	QK0#	QK0	V_{SS}
E	Note 1 (A21)	D7	Q7	V_{DDQ}					V_{DDQ}	Q2	D2	Note 1 (A20)
F	A5	D8	Q8	V_{SSQ}					V_{SSQ}	Q3	D3	QVLD
G	A8	A6	A7	V_{DD}					V_{DD}	A2	A1	A0
H	BA2	A9	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A4	A3
J	Note 2 NF	Note 2 NF	V_{DD}	V_{DD}					V_{DD}	V_{DD}	BA0	CK
K	DK	DK#	V_{DD}	V_{DD}					V_{DD}	V_{DD}	BA1	CK#
L	REF#	CS#	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A14	A13
M	WE#	A16	A17	V_{DD}					V_{DD}	A12	A11	A10
N	A18	D14	Q14	V_{SSQ}					V_{SSQ}	Q9	D9	A19
P	A15	D15	Q15	V_{DDQ}					V_{DDQ}	Q10	D10	DM
R	V_{SS}	QK1	QK1#	V_{SSQ}					V_{SSQ}	Q11	D11	V_{SS}
T	V_{TT}	D16	Q16	V_{DDQ}					V_{DDQ}	Q12	D12	V_{TT}
U	V_{DD}	D17	Q17	V_{SSQ}					V_{SSQ}	Q13	D13	V_{DD}
V	V_{REF}	ZQ	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TDO	TDI

Notes 1. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to V_{SS}, or left open.

2. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to V_{SS}, or left open.

CK, CK#	: Input clock	ZQ	: Output impedance matching
CS#	: Chip select	TMS	: IEEE 1149.1 Test input
WE#	: WRITE command	TDI	: IEEE 1149.1 Test input
REF#	: Refresh command	TCK	: IEEE 1149.1 Clock input
A0–A19	: Address inputs	TDO	: IEEE 1149.1 Test output
A20–A22	: Reserved for the future	V_{REF}	: HSTL input reference input
BA0–BA2	: Bank address input	V_{EXT}	: Power Supply
D0–D17	: Data input	V_{DD}	: Power Supply
Q0–Q17	: Data output	V_{DDQ}	: DQ Power Supply
DK, DK#	: Input data clock	V_{SS}	: Ground
DM	: Input data Mask	V_{SSQ}	: DQ Ground
QK0–QK1, QK0#–QK1#	: Output data clock	V_{TT}	: Power Supply
QVLD	: Data Valid	NF	: No function

RENESAS

Pin Identification (1/2)

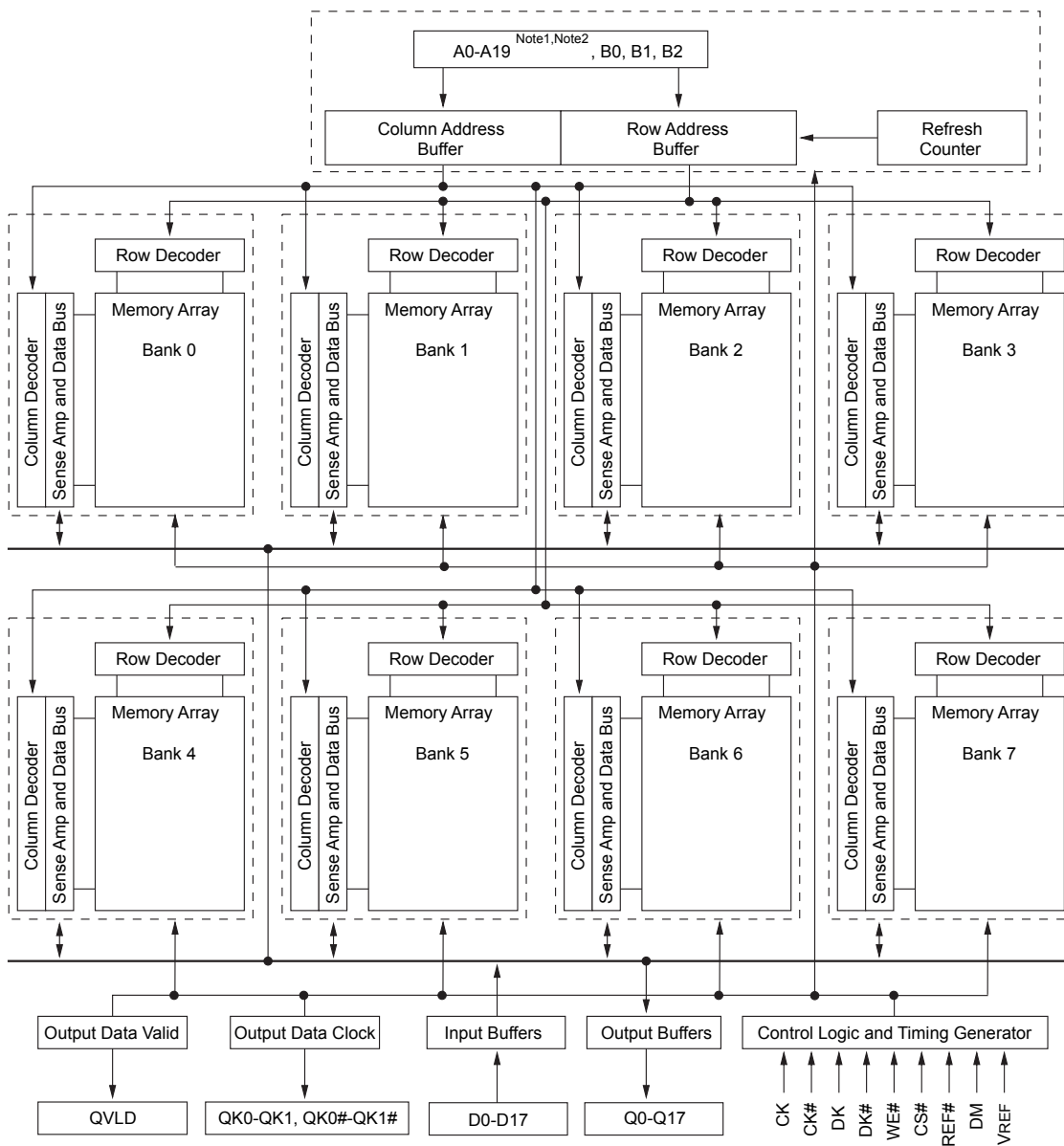| Symbol	Type	Description
CK, CK#	Input	Clock inputs: CK and CK# are differential clock inputs. This input clock pair registers address and control inputs on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip select CS# enables the commands when CS# is LOW and disables them when CS# is HIGH. When the command is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	WRITE command pin, Refresh command pin: WE#, REF# are sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be executed.
A0–A19	Input	Address inputs: A0–A19 define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK.
A20–A22	Input	Reserved for future use: These signals should be tied to Vss or leave open.
BA0–BA2	Input	Bank address inputs; Select to which internal bank a command is being applied.
D0–D17	Input	Data input: The D signals form the 18-bit input data bus. During WRITE commands, the data is referenced to both edges of DK.
Q0–Q17	Output	Data output: The Q signals form the 18-bit output data bus. During READ commands, the data is referenced to both edges of QK.
QKx, QKx#	Output	Output data clocks: QKx and QKx# are opposite polarity, output data clocks. They are always free running and edge-aligned with data output from the μPD48288118-A. QKx# is ideally 180 degrees out of phase with QKx. QK0 and QK0# are aligned with Q0–Q8. QK1 and QK1# are aligned with Q9–Q17.
DK, DK#	Input	Input data clock; DK and DK# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. D0–D17 are referenced to DK and DK#.
DM	Input	Input data mask; The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH along with the WRITE input data. DM is sampled on both edges of DK. The signal should be Vss if not used.
QVLD	Output	Data valid; The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.

RENESAS

Symbol	Type	Description
ZQ	Input /Output	External impedance [25 Ω – 60 Ω]; This signal is used to tune the device outputs to the system data bus impedance. Q output impedance is set to 0.2 x RQ, where RQ is a resistor from this signal to V_{SS}. Connecting ZQ to V_{SS} invokes the minimum impedance mode. Connecting ZQ to $V_{DD}Q$ invokes the maximum impedance mode. Refer to **Figure 2-5. Mode Register Bit Map** to activate this function.
TMS , TDI	Input	JTAG function pins: IEEE 1149.1 test inputs: These balls may be left as no connects if the JTAG function is not used in the circuit
TCK	Input	JTAG function pin; IEEE 1149.1 clock input: This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.
TDO	Output	JTAG function pin; IEEE 1149.1 test output: JTAG output. This ball may be left as no connect if JTAG function is not used.
V_{REF}	Input	Input reference voltage; Nominally $V_{DD}Q/2$. Provides a reference voltage for the input buffers.
V_{EXT}	Supply	Power supply; 2.5 V nominal. See **Recommended DC Operating Conditions** for range.
V_{DD}	Supply	Power supply; 1.8 V nominal. See **Recommended DC Operating Conditions** for range.
$V_{DD}Q$	Supply	DQ power supply; Nominally, 1.5 V or 1.8 V. Isolated on the device for improved noise immunity. See **Recommended DC Operating Conditions** for range.
V_{SS}	Supply	Ground
$V_{SS}Q$	Supply	DQ ground; Isolated on the device for improved noise immunity.
V_{TT}	Supply	Power supply; Isolated termination supply. Nominally, $V_{DD}Q/2$. See **Recommended DC Operating Conditions** for range.
NF		No function; These balls may be connected to V_{SS}.

Block Diagram

16M x 18

Notes 1. When the BL=8 setting is used, A18 and A19 are "Don't care".

2. When the BL=4 setting is used, A19 is "Don't care".

Contents

1. Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit	Note
Supply voltage	V_{EXT}		−0.3 to +2.8	V	
Supply voltage	V_{DD}		−0.3 to +2.1	V	
Output supply voltage,	$V_{DD}Q$	1.8 V nominal	−0.3 to +2.1	V	1
Input voltage, Input / Output voltage		1.5 V nominal	−0.3 to +1.975	V	1
Input / Output voltage	V_{IH} / V_{IL}	1.8 V nominal	−0.3 to +2.1	V	1
		1.5 V nominal	−0.3 to +1.975	V	1
Junction temperature	T_j MAX.		110	°C	
Storage temperature	T_{stg}		−55 to +125	°C	

Note 1. The μPD48288118FF-E support 1.8 V $V_{DD}Q$ nominal.
The μPD48288118FF-EF support 1.5 V $V_{DD}Q$ nominal.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

0°C ≤ T_C ≤ 95°C; 1.7 V ≤ V_{DD} ≤ 1.9 V, unless otherwise noted

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{EXT}		2.38	2.5	2.63	V	1
Supply voltage	V_{DD}		1.7	1.8	1.9	V	1
Output supply voltage	$V_{DD}Q$		1.7	1.8	1.9	V	1, 2, 3
			1.4	1.5	1.6	V	1, 3
Reference Voltage	V_{REF}		0.49 x $V_{DD}Q$	0.5 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	1, 4, 5
Termination voltage	V_{TT}		0.95 x V_{REF}	V_{REF}	1.05 x V_{REF}	V	1, 6
Input HIGH voltage	$V_{IH (DC)}$		V_{REF} + 0.1			V	1
Input LOW voltage	$V_{IL (DC)}$				V_{REF} − 0.1	V	1

Notes 1. All voltage referenced to V_{SS}(GND).

2. During normal operation, $V_{DD}Q$ must not exceed V_{DD}.

3. The μPD48288118FF-E support 1.8 V $V_{DD}Q$ nominal.
The μPD48288118FF-EF support 1.5 V $V_{DD}Q$ nominal.

4. Typically the value of V_{REF} is expect to be 0.5 x $V_{DD}Q$ of the transmitting device. V_{REF} is expected to track variations in $V_{DD}Q$.

5. Peak-to-peak AC noise on V_{REF} must not exceed ±2% V_{REF}(DC).

6. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

DC Characteristics

$0°C \le T_C \le 95°C$; $1.7\ V \le V_{DD} \le 1.9\ V$, unless otherwise noted

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Note
Input leakage current	I_{LI}		–5	+5	μA	1,2
Output leakage current	I_{LO}		–5	+5	μA	1,2
Reference voltage current	I_{REF}		–5	+5	μA	1,2
Output high current	I_{OH}	$V_{OH} = V_{DD}Q/2$	$(V_{DD}Q/2) / (1.15 \times RQ/5)$	$(V_{DD}Q/2) / (0.85 \times RQ/5)$	mA	3,4
Output low current	I_{OL}	$V_{OL} = V_{DD}Q/2$	$(V_{DD}Q/2) / (1.15 \times RQ/5)$	$(V_{DD}Q/2) / (0.85 \times RQ/5)$	mA	3,4

Notes 1. Outputs are impedance-controlled. $| I_{OH} | = (V_{DD}Q/2)/(RQ/5)$ for values of $125\ \Omega \le RQ \le 300\ \Omega$.

    2. Outputs are impedance-controlled. $I_{OL} = (V_{DD}Q/2)/(RQ/5)$ for values of $125\ \Omega \le RQ \le 300\ \Omega$.

    3. I_{OH} and I_{OL} are defined as absolute values and are measured at $V_{DD}Q/2$. I_{OH} flows from the device, I_{OL} flows into the device.

    4. If MRS bit A8 is 0, use RQ = 250 Ω in the equation in lieu of presence of an external impedance matched resistor.

Capacitance ($T_A = 25\ °C$, f = 1MHz)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Address / Control Input capacitance	C_{IN}	$V_{IN} = 0\ V$	1.5	2.5	pF
I/O, Output, Other capacitance (D, Q, DM, QK, QVLD)	$C_{I/O}$	$V_{I/O} = 0\ V$	3.5	5.0	pF
Clock Input capacitance	C_{clk}	$V_{clk} = 0\ V$	2.0	3.0	pF
JTAG pins	C_J	$V_J = 0\ V$	2.0	5.0	pF

Remark   These parameters are periodically sampled and not 100% tested.

           Capacitance is not tested on ZQ pin.

Recommended AC Operating Conditions

$0°C \le T_C \le 95°C$; $1.7\ V \le V_{DD} \le 1.9\ V$, unless otherwise noted

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Input HIGH voltage	$V_{IH\ (AC)}$		$V_{REF} + 0.2$		V	1
Input LOW voltage	$V_{IL\ (AC)}$			$V_{REF} – 0.2$	V	1

Note 1.   Overshoot: $V_{IH\ (AC)} \le V_{DD}Q + 0.7\ V$ for $t \le t_{CK}/2$

        Undershoot: $V_{IL\ (AC)} \ge - 0.5\ V$ for $t \le t_{CK}/2$

        Control input signals may not have pulse widths less than t_{CKH} (MIN.) or operate at cycle rates less than t_{CK} (MIN.).

DC Characteristics

I_{DD} / I_{SB} Operating Conditions

Parameter	Symbol	Test condition		MAX.		Unit
				−EF25	−E33, −EF33	
Standby current	I_{SB1}	t_{CK} = Idle	V_{DD}	48	48	mA
		All banks idle, no inputs toggling	V_{EXT}	26	26	
Active standby current	I_{SB2}	CS# = HIGH, No commands, half bank / address /	V_{DD}	288	233	mA
		data change once every four clock cycles	V_{EXT}	26	26	
Operating current	I_{DD1}	BL=2, sequential bank access, bank transitions once every t_{RC}, half address transitions once	V_{DD}	365	325	mA
		every t_{RC}, read followed by write sequence, continuous data during WRITE commands.	V_{EXT}	41	36	
Operating current	I_{DD2}	BL=4, sequential bank access, bank transitions once every t_{RC}, half address transitions once	V_{DD}	360	340	mA
		every t_{RC}, read followed by write sequence, continuous data during WRITE commands.	V_{EXT}	48	42	
Operating current	I_{DD3}	BL=8, sequential bank access, bank transitions once every t_{RC}, half address transitions once	V_{DD}	400	360	mA
		every t_{RC}, read followed by write sequence, continuous data during WRITE commands.	V_{EXT}	55	48	
Burst refresh current	I_{REF1}	Eight bank cyclic refresh, continuous	V_{DD}	650	540	mA
		address/data, command bus remains in refresh for all banks	V_{EXT}	133	111	
Disturbed refresh current	I_{REF2}	Single bank refresh, sequential bank access,	V_{DD}	310	260	mA
		half address transitions once every t_{RC}, continuous data	V_{EXT}	48	42	
Operating burst write current	I_{DD2W}	BL=2, cyclic bank access, half of address bits	V_{DD}	970	820	mA
		change every clock cycle, continuous data, measurement is taken during continuous WRITE	V_{EXT}	100	90	
Operating burst write current	I_{DD4W}	BL=4, cyclic bank access, half of address bits	V_{DD}	690	560	mA
		change every two clocks, continuous data, measurement is taken during continuous WRITE	V_{EXT}	88	77	
Operating burst write current	I_{DD8W}	BL=8, cyclic bank access, half of address bits	V_{DD}	600	450	mA
		change every four clocks, continuous data, measurement is taken during continuous WRITE	V_{EXT}	60	51	
Operating burst read current	I_{DD2R}	BL=2, cyclic bank access, half of address bits	V_{DD}	970	840	mA
		change every clock cycle, measurement is taken during continuous READ	V_{EXT}	100	90	
Operating burst read current	I_{DD4R}	BL=4, cyclic bank access, half of address bits	V_{DD}	720	580	mA
		change every two clocks, measurement is taken during continuous READ	V_{EXT}	88	77	
Operating burst read current	I_{DD8R}	BL=8, cyclic bank access, half of address bits	V_{DD}	550	450	mA
		change every four clocks, measurement is taken during continuous READ	V_{EXT}	60	51	

Remarks 1. I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ 95°C; 1.7 V ≤ V_{DD} ≤ 1.9 V, 2.38 V ≤ V_{EXT} ≤ 2.63 V, 1.7 V ≤ $V_{DD}Q$ ≤ 1.9 V (–E), 1.4 V ≤ $V_{DD}Q$ ≤ 1.6 V (–EF), V_{REF} = $V_{DD}Q$/2

    2. t_{CK} = t_{DK} = MIN., t_{RC} = MIN.

    3. Input slew rate is specified in **Recommended DC Operating Conditions** and **Recommended AC Operating Conditions**.

    4. I_{DD} parameters are specified with ODT disabled.

    5. Continuous data is defined as half the D or Q signals changing between HIGH and LOW every half clock cycles (twice per clock).

    6. Continuous address is defined as half the address signals between HIGH and LOW every clock cycles (once per clock).

    7. Sequential bank access is defined as the bank address incrementing by one ever t_{RC}.

    8. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL=4 this is every other clock.

    9. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than per clock cycle.
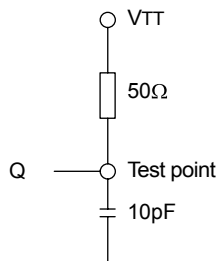
AC Characteristics

AC Test Conditions
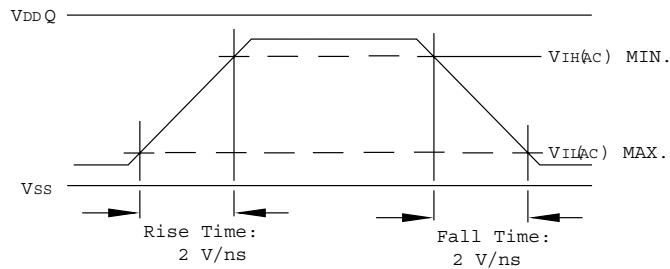
Input waveform

Output waveform
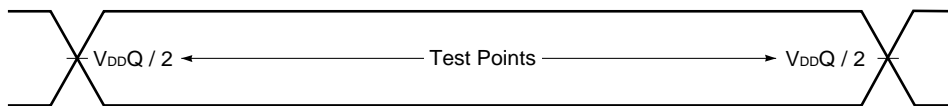
Output load condition

AC Characteristics <Read and Write Cycle>

V_DDQ = 1.8 V

Parameter	Symbol	–E33 (300 MHz)		Unit	Note
		MIN.	MAX.		
Clock					
Clock cycle time (CK,CK#,DK,DK#)	t_{CK}, t_{DK}	3.3	5.7	ns	
Clock frequency (CK,CK#,DK,DK#)	t_{CK}, t_{DK}	175	300	MHz	
Random Cycle time	t_{RC}	20		ns	
Clock Jitter: period	$t_{JIT PER}$	–200	200	ps	1, 2
Clock Jitter: cycle-to-cycle	$t_{JIT CC}$		400	ps	
Clock HIGH time (CK,CK#,DK,DK#)	t_{CKH}, t_{DKH}	0.45	0.55	Cycle	
Clock LOW time (CK,CK#,DK,DK#)	t_{CKL}, t_{DKL}	0.45	0.55	Cycle	
Clock to input data clock	t_{CKDK}	– 0.3	1.0	ns	
Mode register set cycle time to any command	t_{MRSC}	6		Cycle	
PLL Lock time	$t_{CK Lock}$	15		μs	
Clock static to PLL reset	$t_{CK Reset}$	30		ns	
Output Times					
Output data clock HIGH time	t_{QKH}	0.9	1.1	t_{CKH}	
Output data clock LOW time	t_{QKL}	0.9	1.1	t_{CKL}	
QK edge to clock edge skew	t_{CKQK}	– 0.3	0.3	ns	
QK edge to output data edge	t_{QKQ0}, t_{QKQ1}	– 0.25	0.25	ns	3, 5
QK edge to any output data	t_{QKQ}	– 0.35	0.35	ns	4, 5
QK edge to QVLD	t_{QKVLD}	– 0.35	0.35	ns	
Setup Times					
Address/command and input	t_{AS}/t_{CS}	0.5		ns	
Data-in and data mask to DK	t_{DS}	0.3		ns	
Hold Times					
Address/command and input	t_{AH}/t_{CH}	0.5		ns	
Data-in and data mask to DK	t_{DH}	0.3		ns	

Notes 1. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.

    2. Frequency drift is not allowed.

    3. t_{QKQ0} is referenced to Q0–Q8.

       t_{QKQ1} is referenced to Q9–Q17.

    4. t_{QKQ} takes into account the skew between any QKx and any Q.

    5. t_{QKQ}, t_{QKQx} are guaranteed by design.

Remark All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_REF of the command, address, and data signals.

**AC Characteristics <Read and Write Cycle >**

$V_{DD}Q = 1.5$ V

Parameter	Symbol	–EF25 (400 MHz)		–EF33 (300 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Clock							
Clock cycle time (CK,CK#,DK,DK#)	t_{CK}, t_{DK}	2.5	5.7	3.3	5.7	ns	
Clock frequency (CK,CK#,DK,DK#)	t_{CK}, t_{DK}	175	400	175	300	MHz	
Random Cycle time	t_{RC}	20		20		ns	
Clock Jitter: period	$t_{JIT\ PER}$	–150	150	–200	200	ps	1, 2
Clock Jitter: cycle-to-cycle	$t_{JIT\ CC}$		300		400	ps	
Clock HIGH time (CK,CK#,DK,DK#)	t_{CKH}, t_{DKH}	0.45	0.55	0.45	0.55	Cycle	
Clock LOW time (CK,CK#,DK,DK#)	t_{CKL}, t_{DKL}	0.45	0.55	0.45	0.55	Cycle	
Clock to input data clock	t_{CKDK}	– 0.3	0.5	– 0.3	1.0	ns	
Mode register set cycle time to any command	t_{MRSC}	6		6		Cycle	
PLL Lock time	$t_{CK\ Lock}$	15		15		µs	
Clock static to PLL reset	$t_{CK\ Reset}$	30		30		ns	
Output Times							
Output data clock HIGH time	t_{QKH}	0.9	1.1	0.9	1.1	t_{CKH}	
Output data clock LOW time	t_{QKL}	0.9	1.1	0.9	1.1	t_{CKL}	
QK edge to clock edge skew	t_{CKQK}	– 0.25	0.25	– 0.3	0.3	ns	
QK edge to output data edge	t_{QKQ0}, t_{QKQ1}	– 0.2	0.2	– 0.25	0.25	ns	3, 5
QK edge to any output data	t_{QKQ}	– 0.3	0.3	– 0.35	0.35	ns	4, 5
QK edge to QVLD	t_{QKVLD}	– 0.3	0.3	– 0.35	0.35	ns	
Setup Times							
Address/command and input	t_{AS}/t_{CS}	0.4		0.5		ns	
Data-in and data mask to DK	t_{DS}	0.25		0.3		ns	
Hold Times							
Address/command and input	t_{AH}/t_{CH}	0.4		0.5		ns	
Data-in and data mask to DK	t_{DH}	0.25		0.3		ns	

Notes 1. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.

2. Frequency drift is not allowed.

3. t_{QKQ0} is referenced to Q0–Q8.

t_{QKQ1} is referenced to Q9–Q17.

4. t_{QKQ} takes into account the skew between any QKx and any Q.

5. t_{QKQ}, t_{QKQx} are guaranteed by design.

Remark All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_{REF} of the command, address, and data signals.

Figure 1-1. Clock / Input Data Clock Command / Address Timings
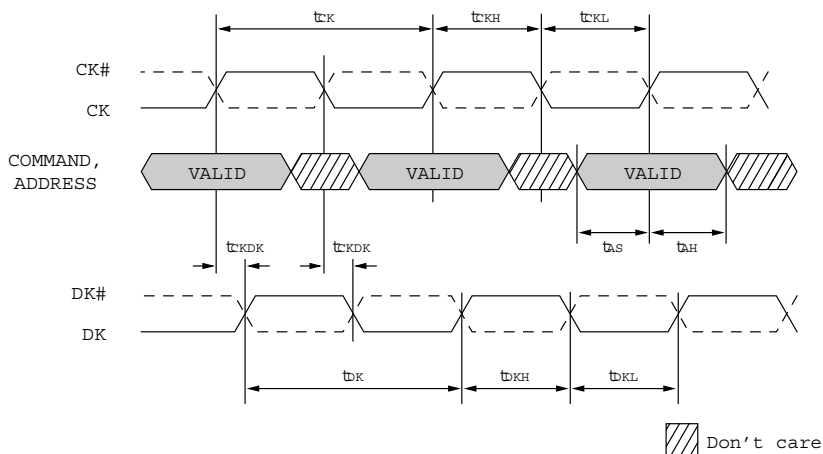
Temperature and Thermal Impedance

Temperature Limits

Parameter	Symbol	MIN.	MAX.	Unit	Note
Reliability junction temperature	T_J	0	+110	°C	1
Operating junction temperature	T_J	0	+100	°C	2
Operating case temperature	T_C	0	+95	°C	3

Notes 1. Temperatures greater than 110°C may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the part.

2. Junction temperature depends upon cycle time, loading, ambient temperature, and airflow.

3. MAX operating case temperature; T_C is measured in the center of the package. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.

Thermal Impedance

Substrate	Ball	θja (°C/W)			θjb (°C/W)	θjc (°C/W)
		Air Flow = 0 m/s	Air Flow = 1 m/s	Air Flow = 2 m/s		
4 - Layer	Lead	32.4	26.8	24.6	23.0	1.8
8 - Layer	Lead	26.5	22.3	20.8	16.8	1.8
4 - Layer	Lead free	32.1	26.6	24.4	22.7	1.8
8 - Layer	Lead free	26.3	22.1	20.6	16.6	1.8

2. Operation

2.1 Command Operation

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

Table 2-1. Address Widths at Different Burst Lengths

Burst Length	Configuration
BL=2	A0–A19
BL=4	A0–A18
BL=8	A0–A17

Table 2-2. Command Table

Operation	Code	CS#	WE#	REF#	A0–A19	BA0–BA2	Notes
Device DESELECT / No Operation	DESEL / NOP	H	X	X	X	X	
MRS: Mode Register Set	MRS	L	L	L	OPCODE	X	1
READ	READ	L	H	H	A	BA	2
WRITE	WRITE	L	L	H	A	BA	2
AUTO REFRESH	AREF	L	H	L	X	BA	

Notes 1. Only A0–A17 are used for the MRS command.
2. See **Table 2-1.**

Remark X = "Don't Care", H = logic HIGH, L = logic LOW, A = valid address, BA = valid bank address

2.2 Description of Commands

DESEL / NOP[Note1]

The NOP command is used to perform a no operation to the μPD48288118-A, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.

MRS

The mode register is set via the address inputs A0–A17. See **Figure 2-5. Mode Register Bit Map** for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.

READ

The READ command is used to initiate a burst read access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A19 selects the data location within the bank.

WRITE

The WRITE command is used to initiate a burst write access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A19 selects the data location within the bank. Input data appearing on the D is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written).

AREF

The AREF is used during normal operation of the *µ*PD48288118-A to refresh the memory content of a bank. The command is non-persistent, so it must be issued each time a refresh is required. The value on the BA0–BA2 inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a "Don't Care" during the AREF command. The *µ*PD48288118-A requires 64K cycles at an average periodic interval of 0.49 *µ*s [Note2] (MAX.). To improve efficiency, eight AREF commands (one for each bank) can be posted to *µ*PD48288118-A at periodic intervals of 3.9 *µ*s [Note3].

Within a period of 32ms, the entire memory must be refreshed. The delay between the AREF command and a subsequent command to same bank must be at least t_{RC} as continuous refresh. Other refresh strategies, such as burst refresh, are also possible.

Notes 1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
2. Actual refresh is 32 ms / 8k / 8 = 0.488 *µ*s.
3. Actual refresh is 32 ms / 8k = 3.90 *µ*s.

2.3 Initialization

The *µ*PD48288118-A must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device. The following sequence is used for Power-Up:

1. Apply power (V_{EXT}, V_{DD}, $V_{DD}Q$, V_{REF}, V_{TT}) and start clock as soon as the supply voltages are stable. Apply V_{DD} and V_{EXT} before or at the same time as $V_{DD}Q$. Apply $V_{DD}Q$ before or at the same time as V_{REF} and V_{TT}. Although there is no timing relation between V_{EXT} and V_{DD}, the chip starts the power-up sequence only after both voltages are at their nominal levels. $V_{DD}Q$ supply must not be applied before V_{DD} supply. CK/CK# must meet $V_{ID(DC)}$ prior to being applied. Maintain all remaining balls in NOP conditions.

    Note No rule of apply power sequence is the design target.

2. Maintain stable conditions for 200 *µ*s (MIN.).

3. Issue three or more back-to-back and clock consecutive MRS commands: two dummies plus one valid MRS. It is recommended that the dummy MRS commands are the same value as the desired MRS.

4. t_{MRSC} after valid MRS, an AUTO REFRESH command to all 8 banks must be issued and wait for 15 µs with CK/CK# toggling in order to lock the PLL prior to normal operation.

5. After t_{RC}, the chip is ready for normal operation.

2.4 Power-On Sequence

Figure 2-1. Power-Up Sequence
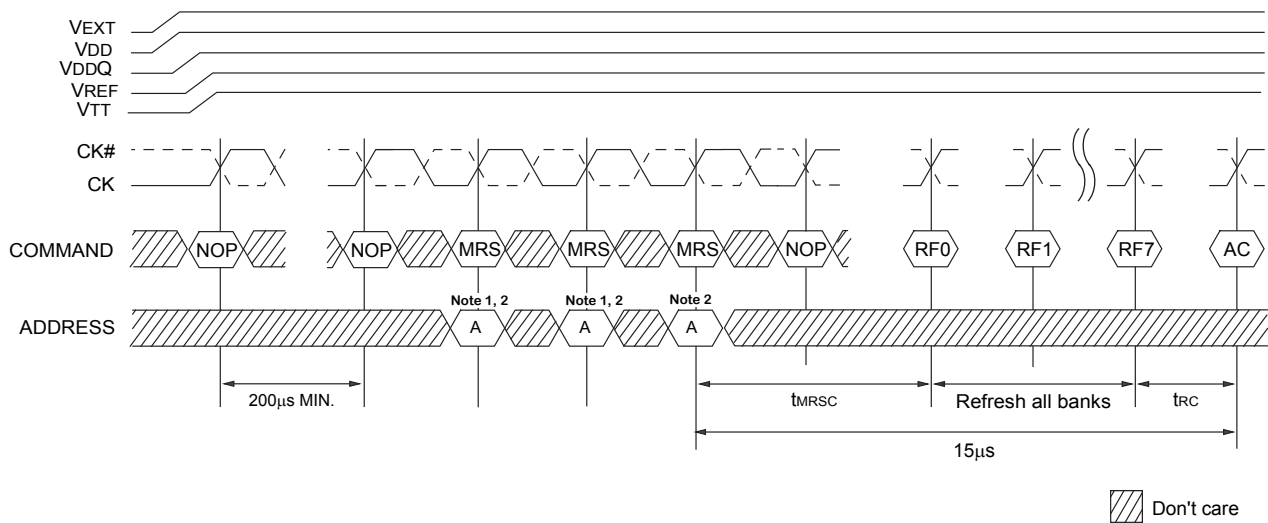
Notes 1. Recommended all address pins held LOW during dummy MRS commands.
      2. A10-A17 must be LOW.

Remark   MRS: MRS command
          RFp : REFRESH bank p
          AC : Any Command

2.5 Programmable Impedance Output Buffer

The μPD48288118-A is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and Vss. The value of the resistor must be five times the desired impedance. For example, a 300 Ω resistor is required for an output impedance of 60 Ω. To ensure that output impedance is one fifth the value of RQ (within 15 percent), the range of RQ is 125 Ω to 300 Ω. Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of RQ. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

2.6 PLL Reset

The μPD48288118-A utilizes internal Phase-locked loops for maximum output, data valid windows. It can be placed into a stopped-clock state to minimize power with a modest restart time of 15 μs. The clock (CK/CK#) must be toggled for 15 μs in order to stabilize PLL circuits for next READ operation.

2.7 Clock Input

Table 2-3. Clock Input Operation Conditions

| Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock Input Voltage Level	$V_{IN (DC)}$	CK and CK#	-0.3	$V_{DD}Q + 0.3$	V	
Clock Input Differential Voltage Level	$V_{ID (DC)}$	CK and CK#	0.2	$V_{DD}Q + 0.6$	V	8
Clock Input Differential Voltage Level	$V_{ID (AC)}$	CK and CK#	0.4	$V_{DD}Q + 0.6$	V	8
Clock Input Crossing Point Voltage Level	$V_{IX (AC)}$	CK and CK#	$V_{DD}Q/2 - 0.15$	$V_{DD}Q/2 + 0.15$	V	9

Figure 2-2. Clock Input
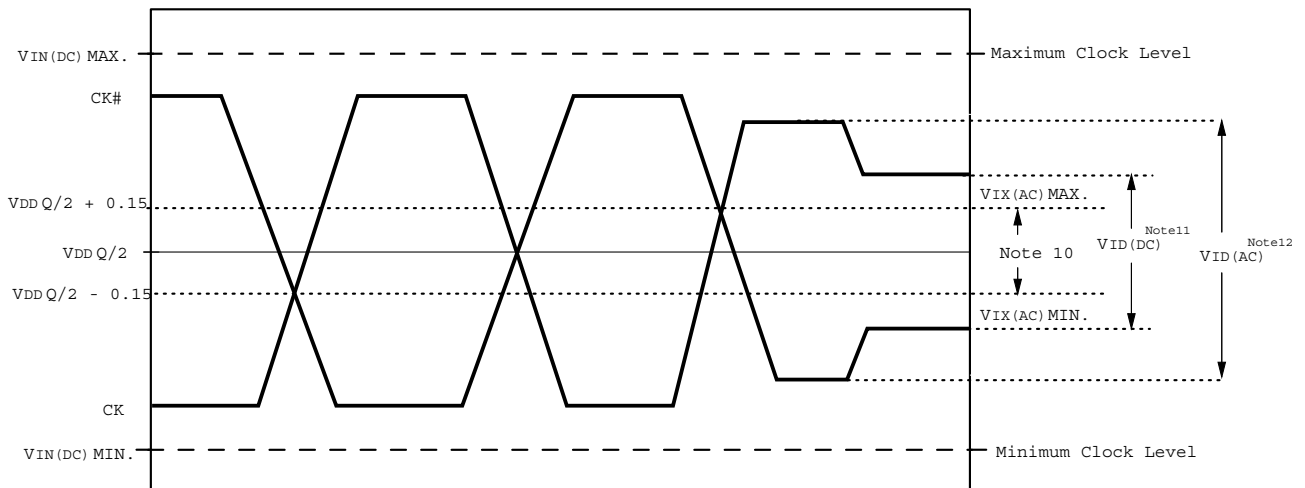
Notes 1. DK and DK# have the same requirements as CK and CK#.

    2. All voltages referenced to V_{SS}.

    3. Tests for AC timing, IDD and electrical AC and DC characteristics may be conducted at normal reference/supply voltage levels; but the related specifications and device operations are tested for the full voltage range specified.

    4. AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or the crossing point for CK/CK#), and parameters specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

    5. The AC and DC input level specifications are as defined in the HSTL Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above[below] the DC input LOW[HIGH] level).

    6. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signal other than CK/CK# is V_{REF}.

    7. CK and CK# input slew rate must be >=2V/ns (>=4V/ns if measured differentially).

    8. V_{ID} is the magnitude of the difference between the input level on CK and input level on CK#.

    9. The value of V_{IX} is expected to equal $V_{DD}Q/2$ of the transmitting device and must track variations in the DC level of the same.

    10. CK and CK# must cross within the region.

    11. CK and CK# must meet at least $V_{ID(DC)}$ (MIN.) when static and centered around $V_{DD}Q/2$.

    12. Minimum peak-to-peak swing.

2.8 Mode Register Set Command (MRS)

The mode register stores the data for controlling the operating modes of the memory. It programs the μPD48288118-A configuration, burst length, and I/O options. During a MRS command, the address inputs A0–A17 are sampled and stored in the mode register. t_{MRSC} must be met before any command can be issued to the μPD48288118-A. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete.

Since MRS is used for internal test mode entry, the designated bit at **Figure 2-5. Mode Register Bit Map** and **Figure 2-27. Mode Register Set Command in Multiplexed Address Mode** should be set.

Figure 2-3. Mode Register Set Timing
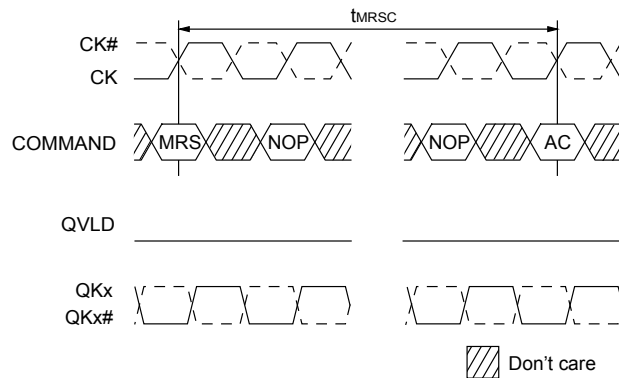
Remark   MRS : MRS command
AC   : any command

Figure 2-4. Mode Register Set
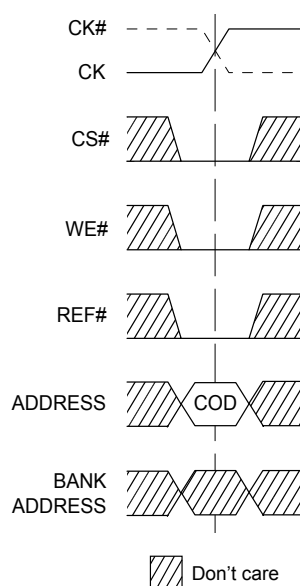
Remark   COD: code to be loaded into the register.

Figure 2-5. Mode Register Bit Map

A17-A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

| Reserved Note 1 | On-Die Termination | Impedance Matching | PLL Reset | Unused | Address Mux | Burst Length | | Configuration | | |

On-Die Termination

A9	Termination
0	Disabled (default)
1	Enabled

Impedance Matching

A8	Resistor
0	Internal 50 Ω Note 3 (default)
1	External Note 4

PLL Reset

A7	PLL Reset
0	PLL reset (default)
1	PLL enabled

Address Mux

A5	Address Mux
0	Nonmultiplexed (default)
1	Address multiplexed

Burst Length

A4	A3	BL
0	0	2 (default)
0	1	4
1	0	8 Note 2
1	1	Not valid

Configuration

A2	A1	A0	Configuration
0	0	0	1 Note 2 (default)
0	0	1	1 Note 2
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes 1. Bits A10-A17 must be set to all '0'. A18-An are "Don't Care".

2. BL=8 is not available for configuration 1.

3. ±30% temperature variation.

4. Within 15%.

2.9 Read & Write configuration (Non Multiplexed Address Mode)

Table 2-4 shows, for different operating frequencies, the different μPD48288118-A configurations that can be programmed into the mode register. The READ and WRITE latency (t_{RL} and t_{WL}) values along with the row cycle times (t_{RC}) are shown in clock cycles as well as in nanoseconds. The shaded areas correspond to configurations that are not allowed.

Table 2-4. Configuration Table

Frequency	Symbol	Configuration			Unit
		1 Note	2	3	
	t_{RC}	4	6	8	Cycles
	t_{RL}	4	6	8	Cycles
	t_{WL}	5	7	9	Cycles
400MHz	t_{RC}			20.0	ns
	t_{RL}			20.0	ns
	t_{WL}			22.5	ns
300MHz	t_{RC}		20.0	26.7	ns
	t_{RL}		20.0	26.7	ns
	t_{WL}		23.3	30.0	ns
200MHz	t_{RC}	20.0	30.0	40.0	ns
	t_{RL}	20.0	30.0	40.0	ns
	t_{WL}	25.0	35.0	45.0	ns

Note BL=8 is not available for configuration 1.

2.10 Write Operation (WRITE)

 Write accesses are initiated with a WRITE command, as shown in **Figure 2-6**. Row and bank addresses are provided together with the WRITE command. During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). A WRITE latency (WL) one cycle longer than the programmed READ latency (RL + 1) is present, with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command. **Figure 2-10. WRITE Followed By READ: BL=2, RL=4, WL=5, Configuration 1** and **Figure 2-11. WRITE Followed By READ: BL=4, RL=4, WL=5, Configuration 1** illustrate the timing requirements for a WRITE followed by a READ for bursts of two and four, respectively.

Setup and hold times for incoming input data relative to the DK edges are specified as t_{DS} and t_{DH}. The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for data mask are also t_{DS} and t_{DH}.

Figure 2-6. WRITE Command
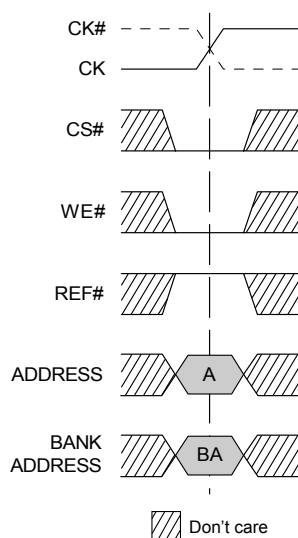
Remark A : Address
   BA : Bank address

Figure 2-7. Basic WRITE Burst / DM Timing

RENESAS
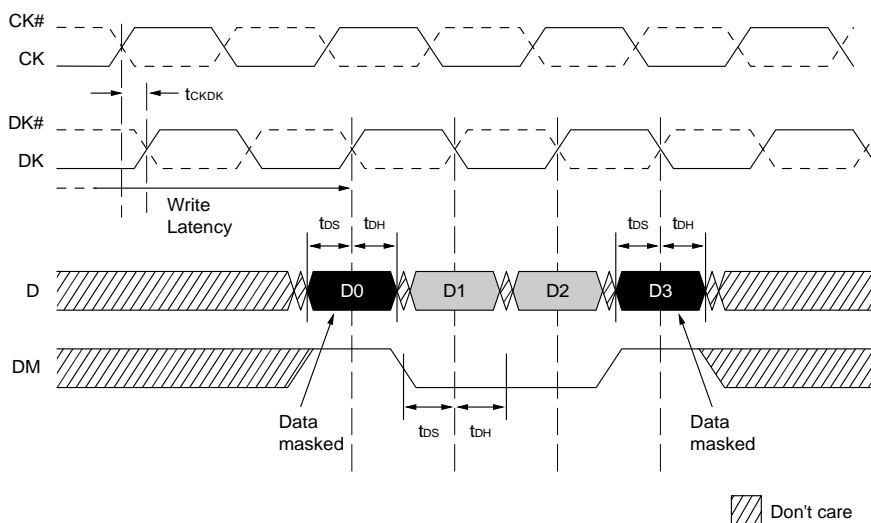
Figure 2-8. WRITE Burst Basic Sequence: BL=2, RL=4, WL=5, Configuration 1
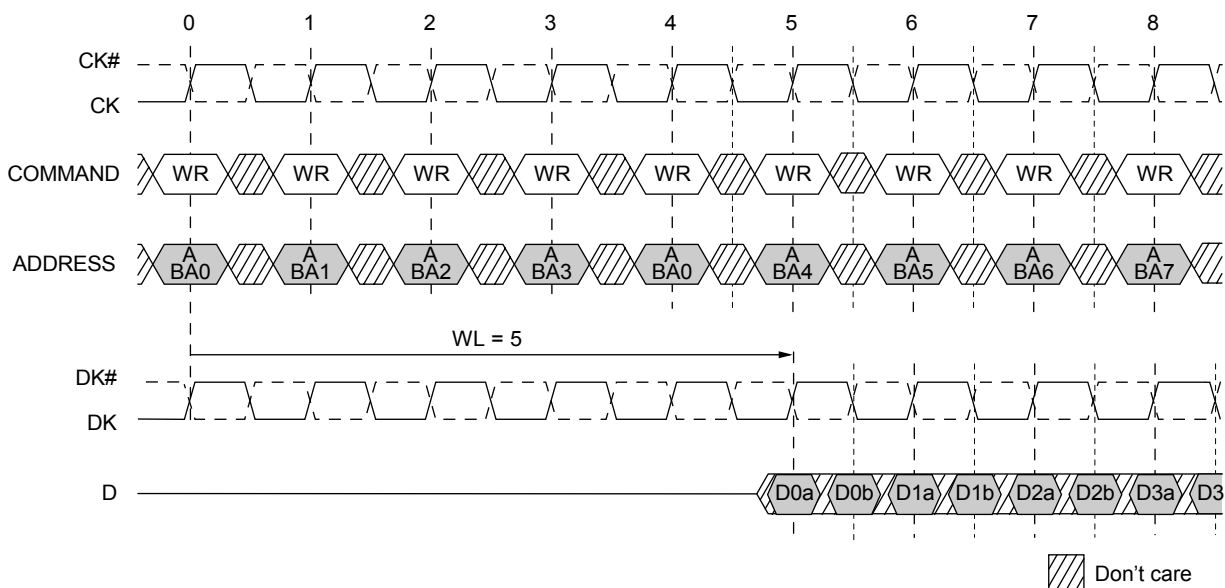
Figure 2-9. WRITE Burst Basic Sequence: BL=4, RL=4, WL=5, Configuration 1
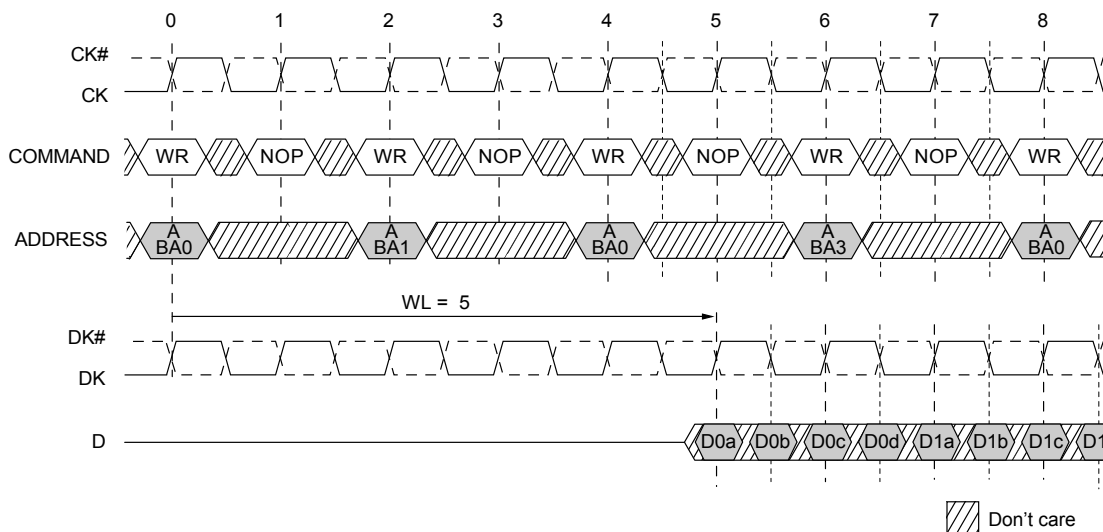
Remarks 1. WR   : WRITE command

A/BAp : Address A of bank p

WL   : WRITE latency

Dpq   : Data q to bank p

2. Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.

Figure 2-10. WRITE Followed By READ: BL=2, RL=4, WL=5, Configuration 1
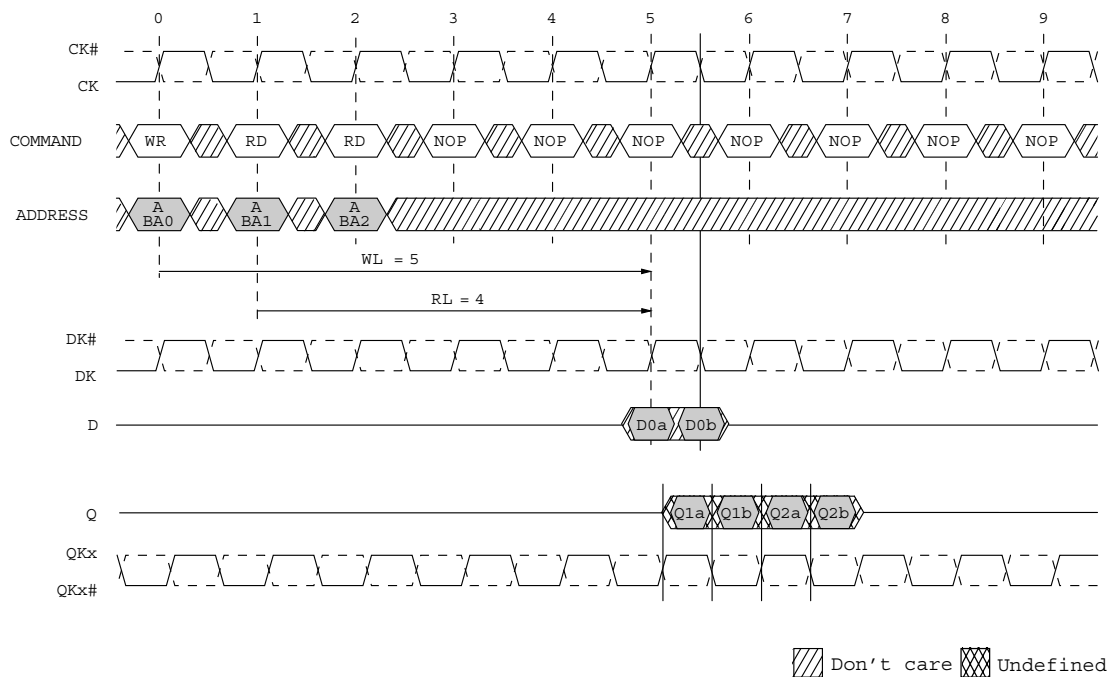
Don't care / Undefined

Figure 2-11. WRITE Followed By READ: BL=4, RL=4, WL=5, Configuration 1

Don't care / Undefined
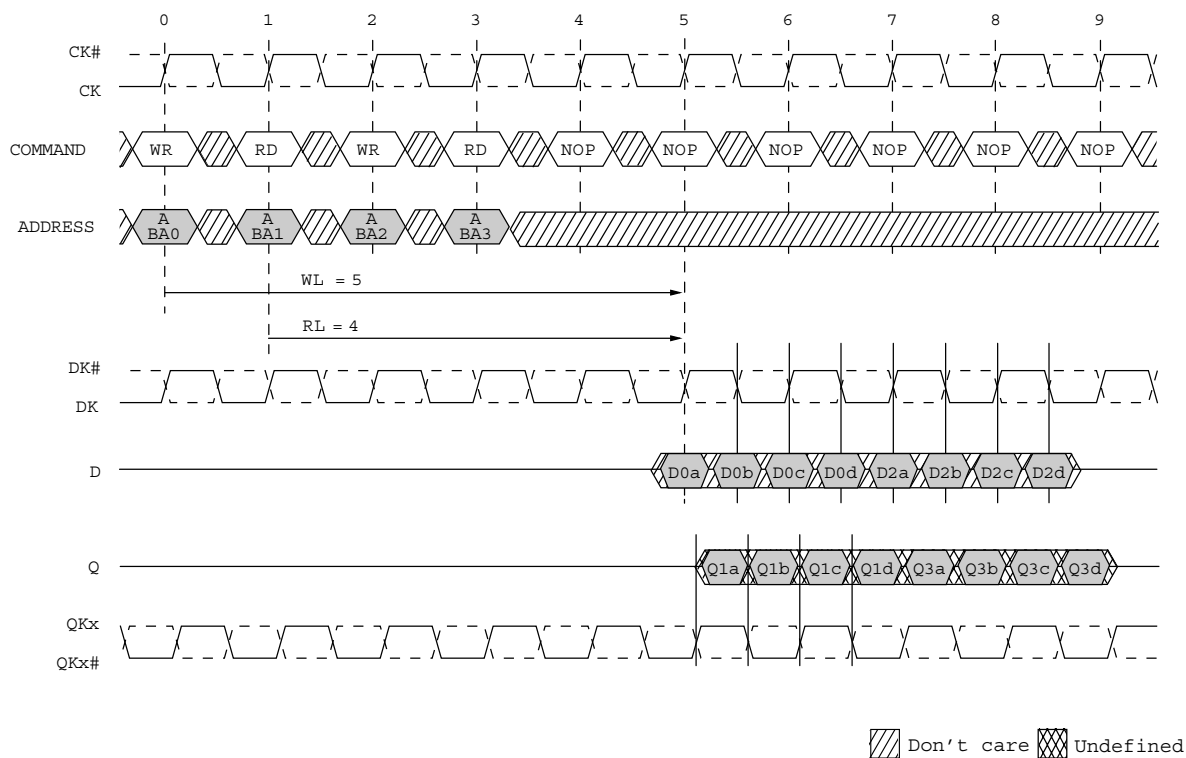
Remark WR : WRITE command
RD : READ command
A/BAp : Address A of bank p
WL : WRITE latency
RL : READ latency
Dpq : Data q to bank p
Qpq : Data q from bank p

2.11 Read Operation (READ)

Read accesses are initiated with a READ command, as shown in **Figure 2-12**. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the QK signal. After a programmable READ latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

The skew between QK and the crossing point of CK is specified as t_{CKQK}. t_{QKQ0} is the skew between QK0 and the last valid data edge considered the data generated at the Q0–Q17 in x36 and Q0–Q8 in x18 data signals. t_{QKQ1} is the skew between QK1 and the last valid data edge considered the data generated at the Q18–Q35 in x36 and Q9–Q17 in x18 data signals. t_{QKQx} is derived at each QKx clock edge and is not cumulative over time. t_{QKQ} is the maximum of t_{QKQ0} and t_{QKQ1}.

After completion of a burst, assuming no other commands have been initiated, Q will go High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

Minimum READ data valid window can be expressed as MIN.(t_{QKH}, t_{QKL}) – 2 x MAX.(t_{QKQx}).

Any READ burst may be followed by a subsequent WRITE command. **Figure 2-16. READ followed by WRITE, BL=2, RL=4, WL=5, Configuration 1** and **Figure 2-17. READ followed by WRITE, BL=4, RL=4, WL=5, Configuration 1** illustrate the timing requirements for a READ followed by a WRITE.

Figure 2-12. READ Command
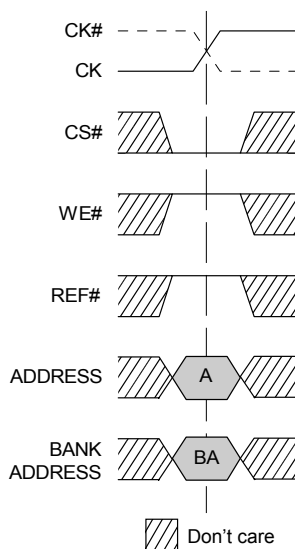
Remark A : Address
BA : Bank address

Figure 2-13. Basic READ Burst Timing

Undefined
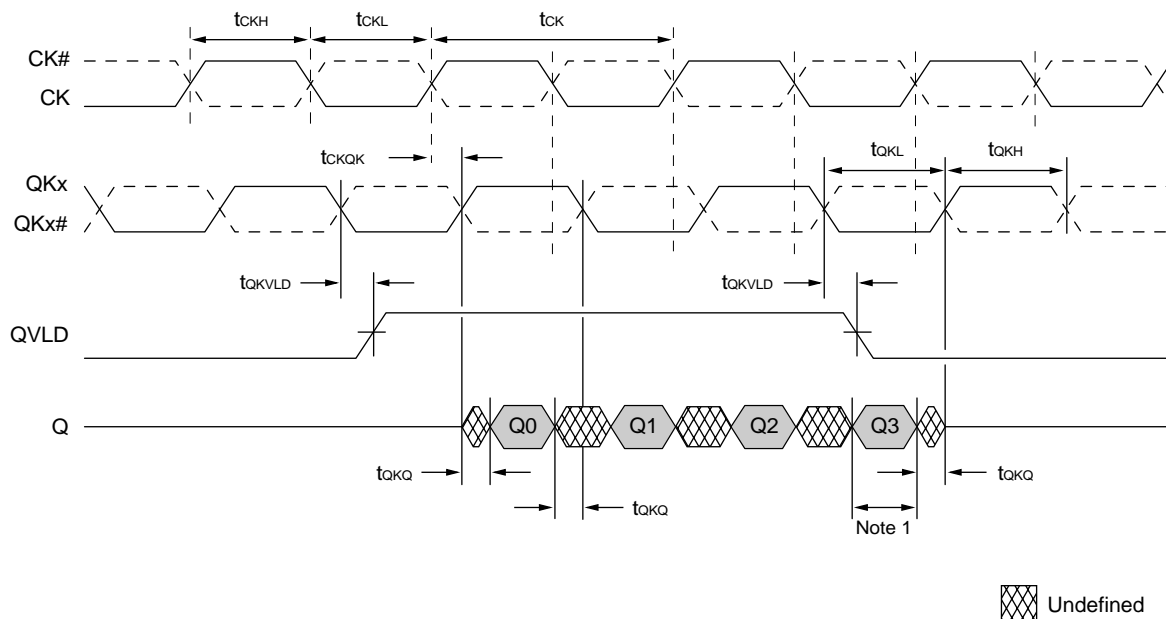
Note 1. Minimum READ data valid window can be expressed as MIN.(t_{QKH}, t_{QKL}) – 2 x MAX.(t_{QKQx}).

t_{CKH} and t_{CKL} are recommended to have 50% / 50% duty.

Remarks 1. t_{QKQ0} is referenced to Q0–Q8.

t_{QKQ1} is referenced to Q9–Q17.

2. t_{QKQ} takes into account the skew between any QKx and any Q.

3. t_{CKQK} is specified as CK rising edge to QK rising edge.

Figure 2-14. READ Burst Basic Sequence: BL=2, RL=4, Configuration 1
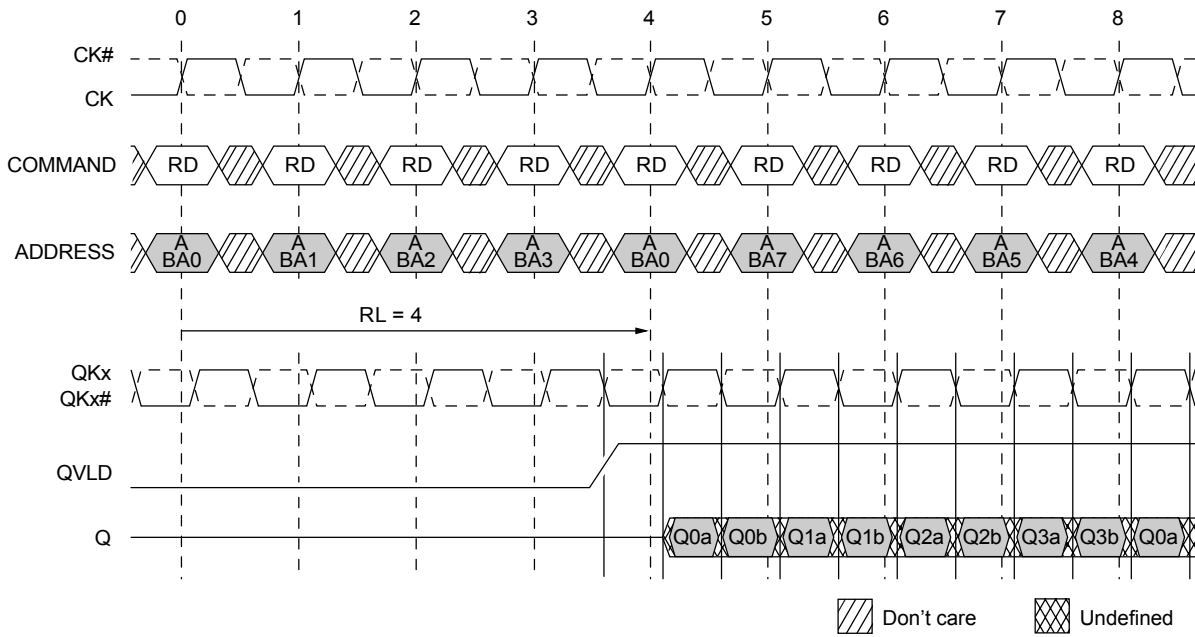
Figure 2-15. READ Burst Basic Sequence: BL=4, RL=4, Configuration 1
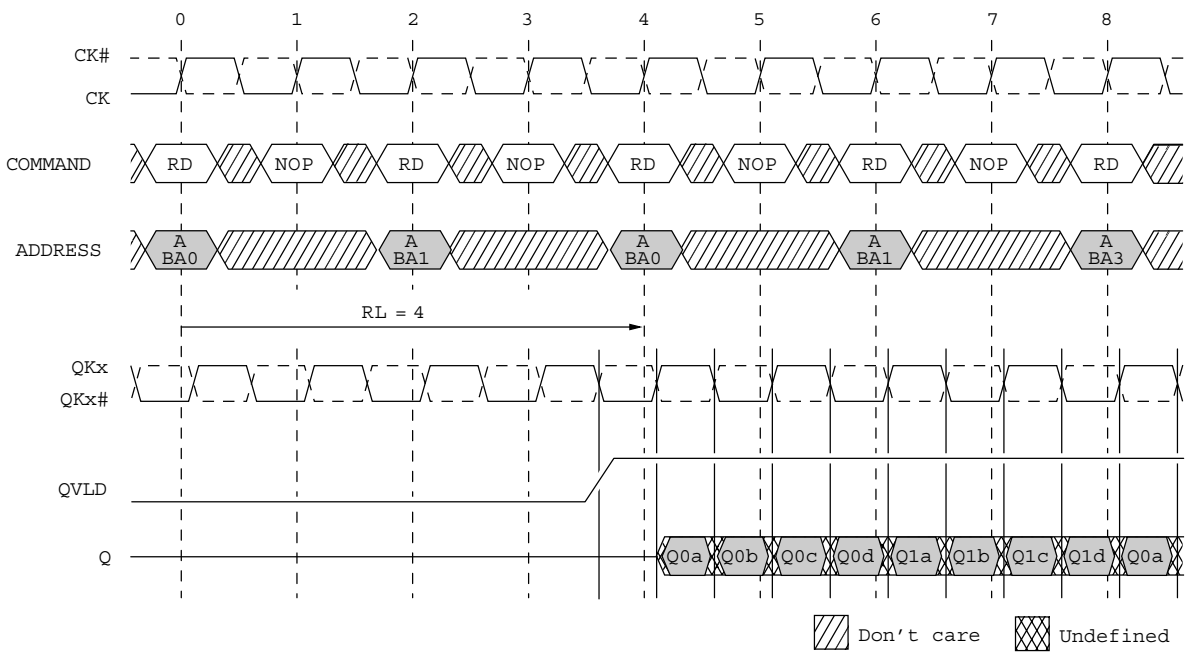
Remark RD : READ command

A/BAp: Address A of bank p

RL : READ latency

Qpq : Data q from bank p

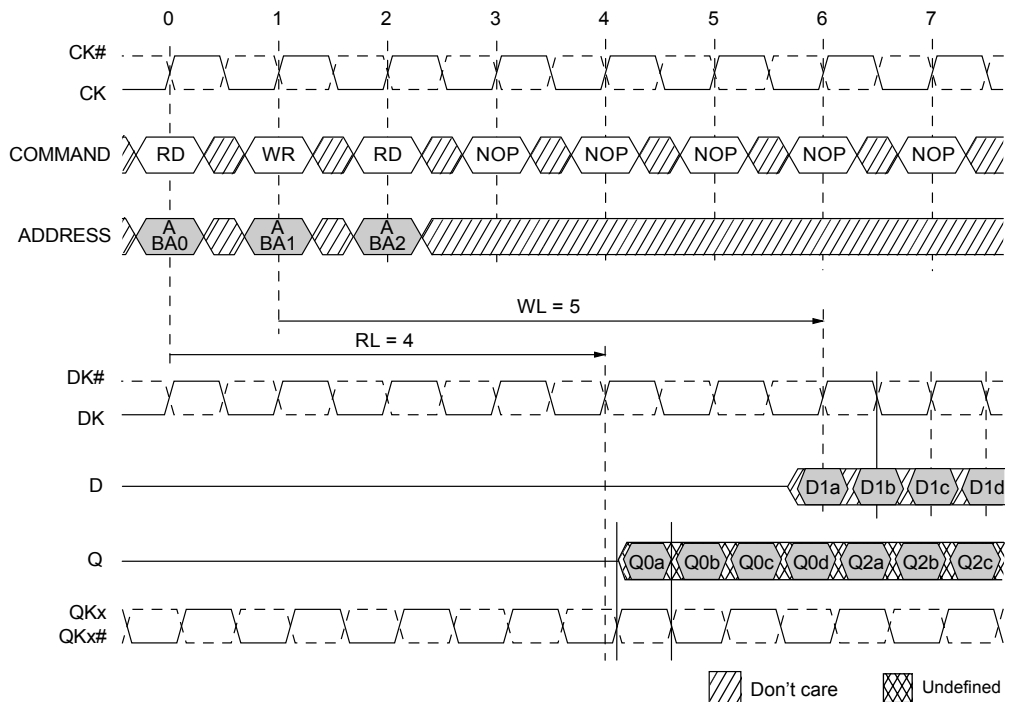### Figure 2-16. READ followed by WRITE, BL=2, RL=4, WL=5, Configuration 1
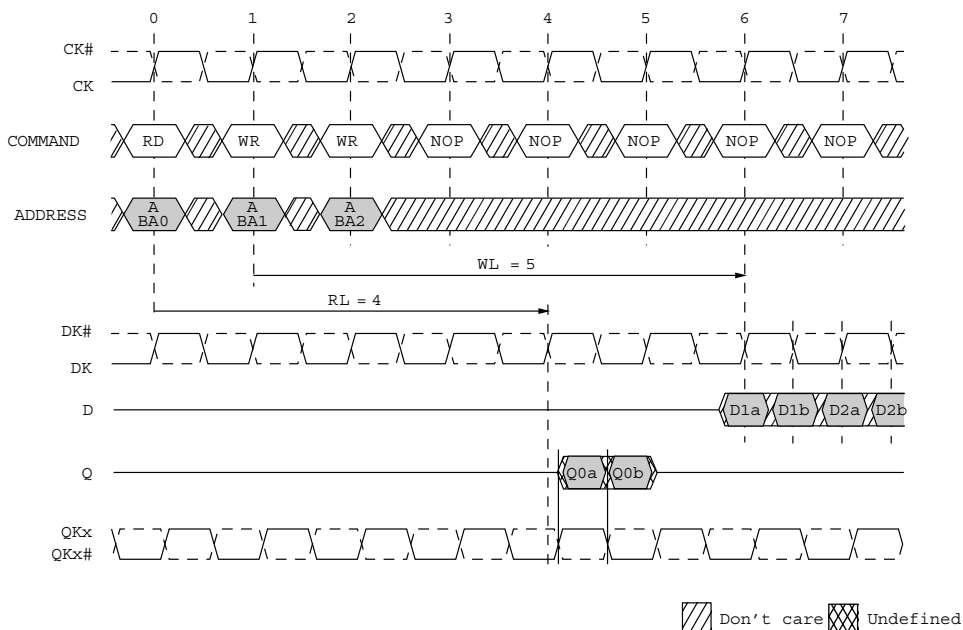
Don't care Undefined

Figure 2-17. READ followed by WRITE, BL=4, RL=4, WL=5, Configuration 1

Don't care Undefined

Remark WR   : WRITE command

RD   : READ command

A/BAp : Address A of bank p

WL   : WRITE latency

RL   : READ latency

Dpq   : Data q to bank p

Qpq   : Data q from bank p

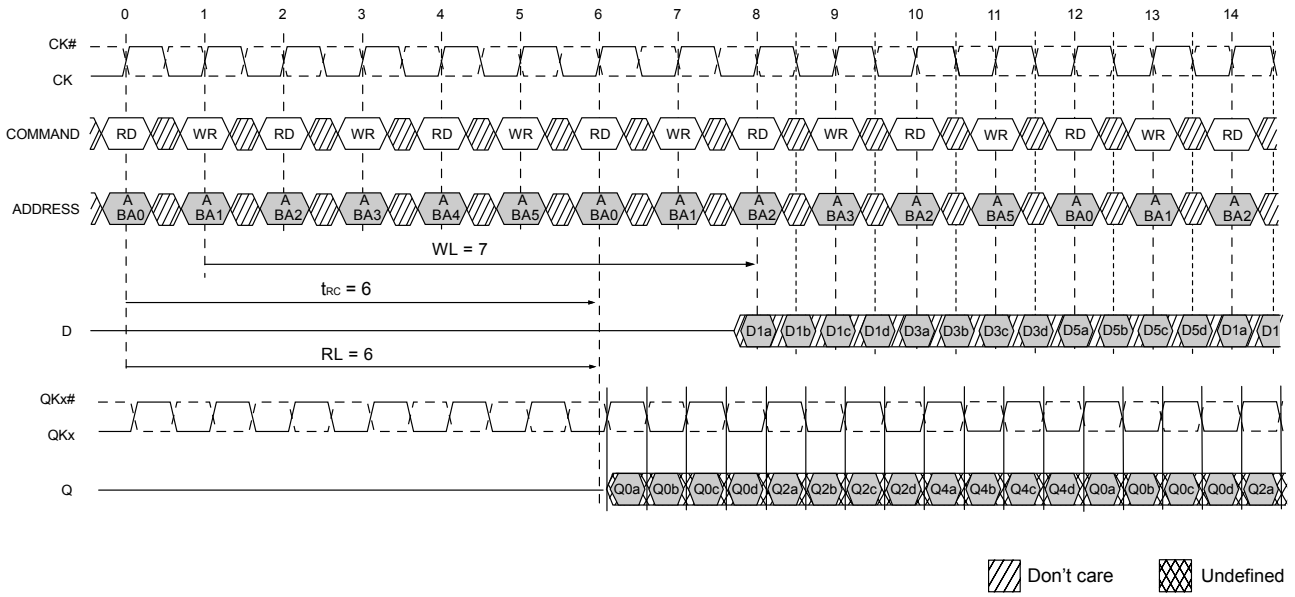### Figure 2-18. READ/WRITE Interleave: BL=4, t$_{RC}$=6, WL=7, Configuration 2
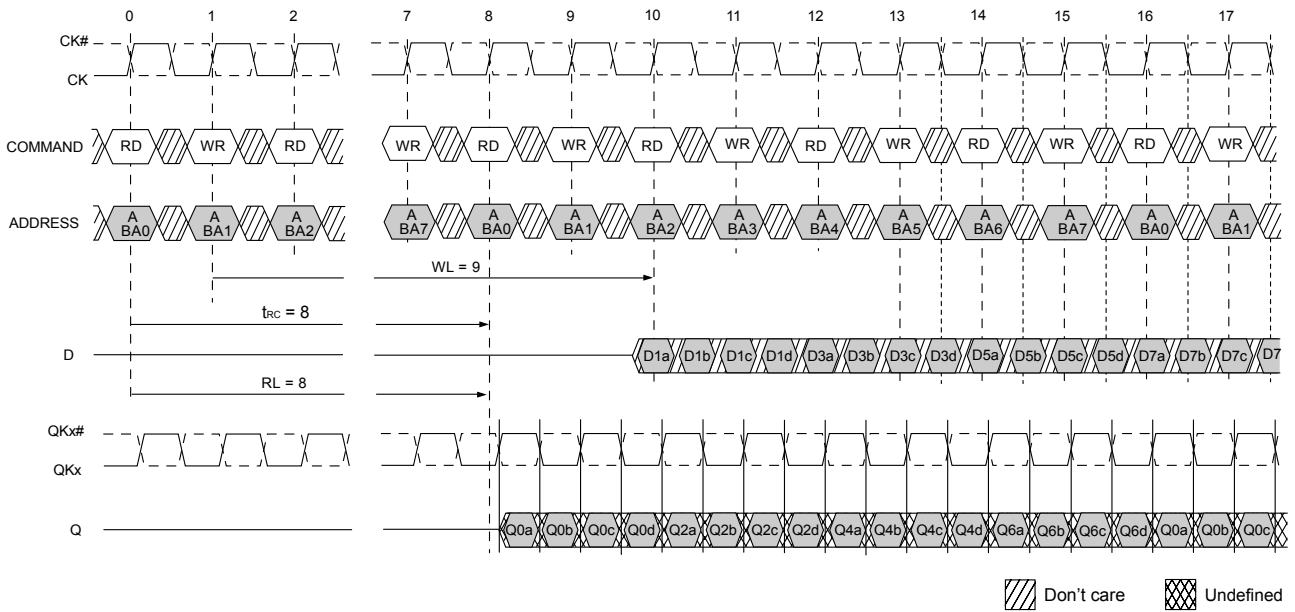

Figure 2-19. READ/WRITE Interleave: BL=4, t$_{RC}$=8, WL=9, Configuration 3

Remark WR   : WRITE command
RD   : READ command
A/BAp: Address A of bank p
WL   : WRITE latency
RL   : READ latency
Dpq : Data q to bank p
Qpq : Data q from bank p

2.12 Refresh Operation: AUTO REFRESH Command (AREF)

AREF is used to perform a REFRESH cycle on one row in a specific bank. The row addresses are generated by an internal refresh counter; external address balls are "Don't Care." The delay between the AREF command and a subsequent command to the same bank must be at least t_{RC}.
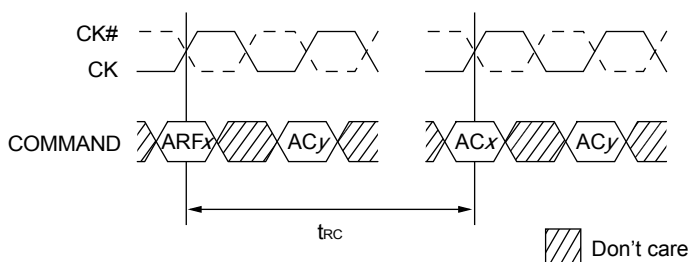
Within a period of 32 ms (t_{REF}), the entire memory must be refreshed. **Figure 2-21.** illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

Figure 2-20. AUTO REFRESH Command
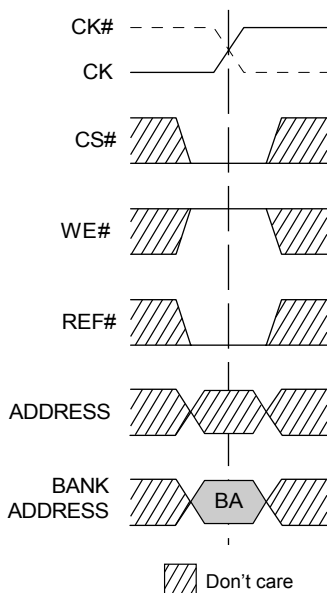
Remark BA: Bank address

Figure 2-21. AUTO REFRESH Cycle

Remarks 1. ACx: Any command on bank x

ARFx: Auto refresh bank x

ACy: Any command on different bank.

2. t_{RC} is configuration-dependent. Refer to **Table 2-4. Configuration Table**.

2.13 On-Die Termination

On-die termination (ODT) is enabled by setting A9 to "1" during an MRS command. With ODT on, all the DQs and DM are terminated to V_{TT} with a resistance R_{TT}. The command, address, and clock signals are not terminated. **Figure 2-22.** below shows the equivalent circuit of a Q receiver with ODT. ODTs are dynamically switched off during READ commands and are designed to be off prior to the μPD48288118-A driving the bus. Similarly, ODTs are designed to switch on after the μPD48288118-A has issued the last piece of data. ODT at the D inputs and DM are always on.

Table 2-5. On-Die Termination DC Parameters

Description	Symbol	MIN.	MAX.	Units	Note
Termination voltage	V_{TT}	0.95 x V_{REF}	1.05 x V_{REF}	V	1,2
On-Die termination	R_{TT}	125	185	Ω	3

Notes 1. All voltages referenced to V_{SS} (GND).

2. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

3. The R_{TT} value is measured at 95°C T_C.

Figure 2-22. On- Die Termination-Equivalent Circuit
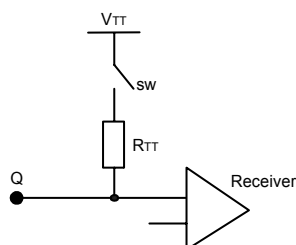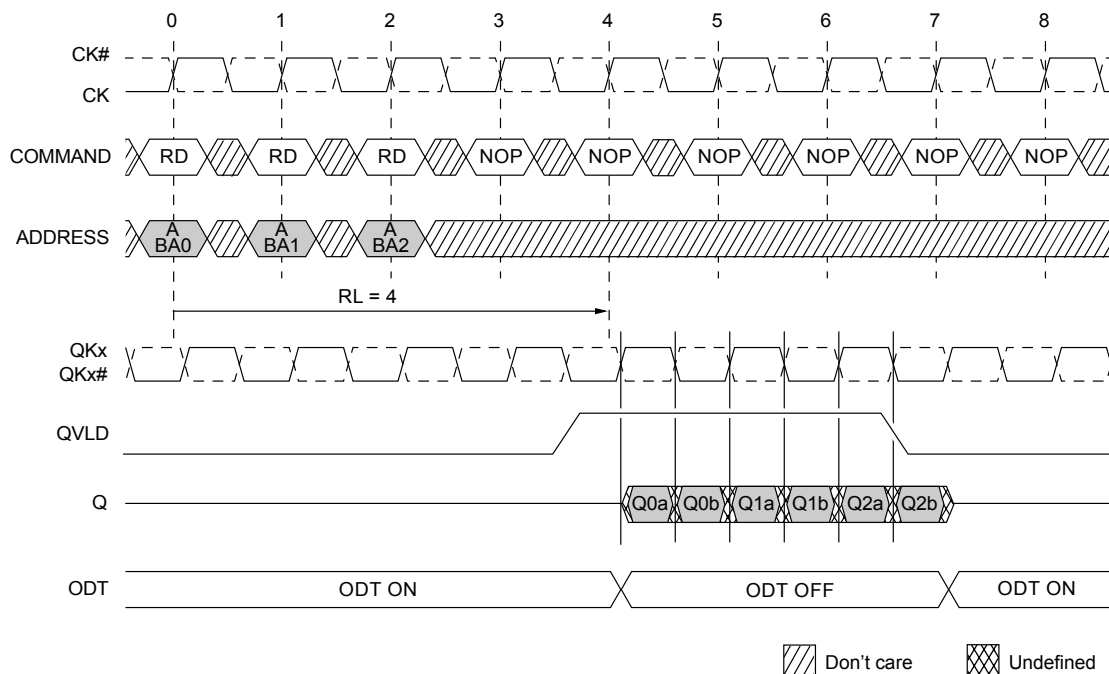

Figure 2-23. READ Burst with ODT: BL=2, Configuration 1

Remark RD : READ command

A/BAp: Address A of bank p

RL : READ latency

Qpq : Data q from bank p

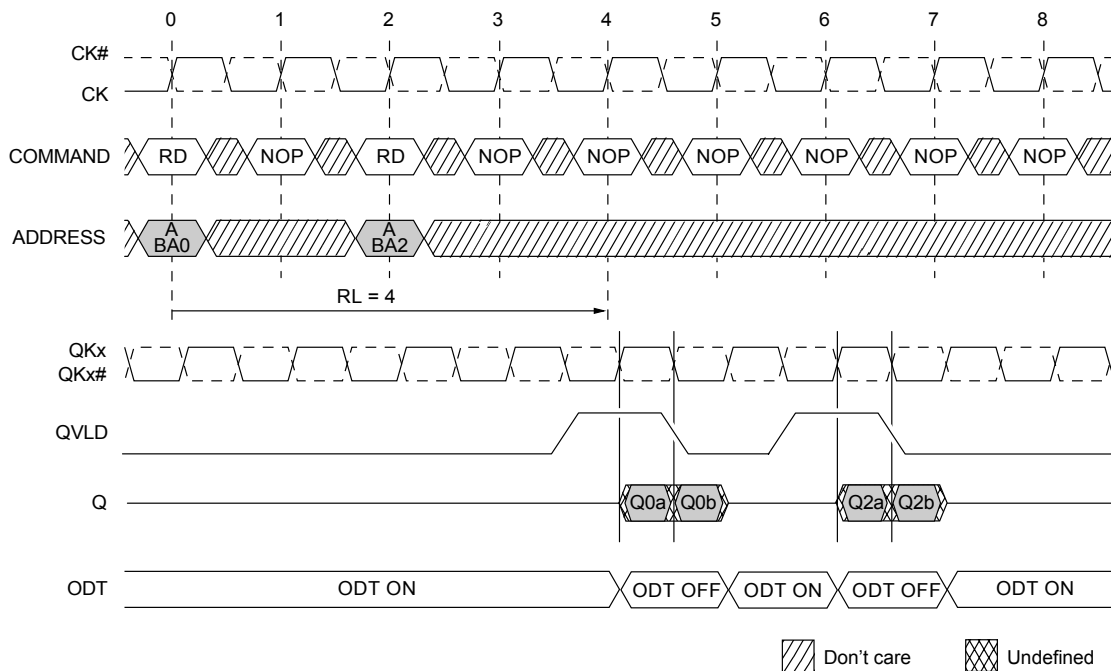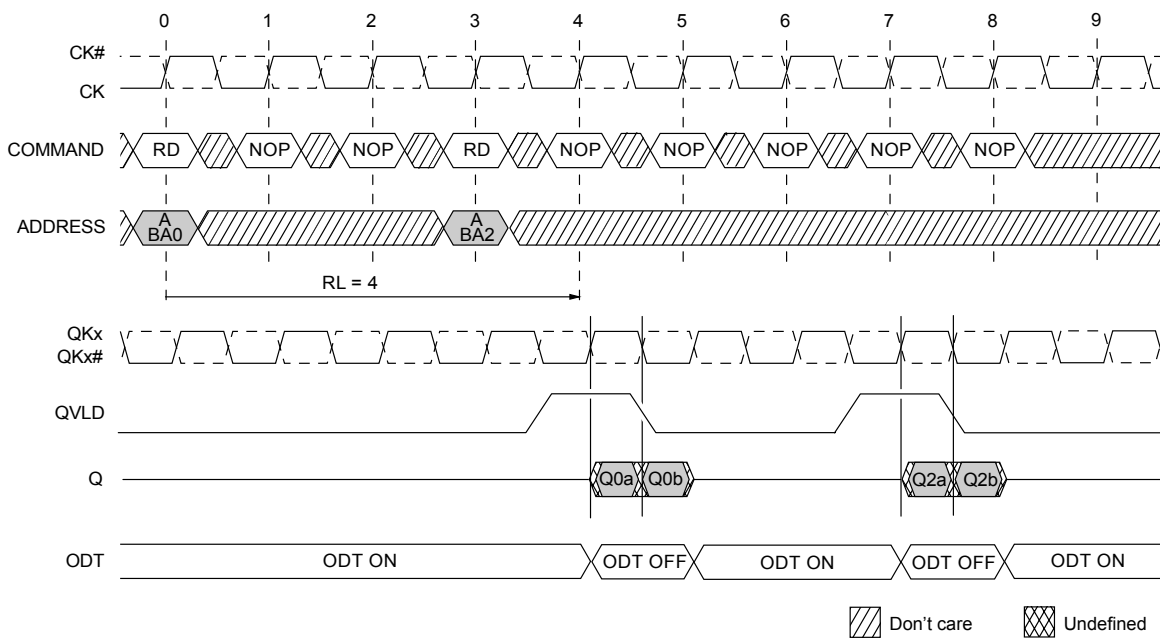**Figure 2-24. READ NOP READ with ODT: BL=2, Configuration 1**

Figure 2-25. READ NOP NOP READ with ODT: BL=2, Configuration 1

**Remark**   RD   : READ command

A/BAp: Address A of bank p

RL   : READ latency

Qpq : Data q from bank p

2.14 Operation with Multiplexed Address

In multiplexed address mode, the address can be provided to the μPD48288118-A in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage that a maximum of 11 address balls are required to control the μPD48288118-A, reducing the number of balls on the controller side. The data bus efficiency in continuous burst mode is not affected for BL=4 and BL=8 since at least two clocks are required to read the data out of the memory. The bank addresses are delivered to the μPD48288118-A at the same time as the WRITE command and the first address part, Ax.

This option is available by setting bit A5 to "1" in the mode register. Once this bit is set, the READ, WRITE, and MRS commands follow the format described in **Figure 2-26**. See **Figure 2-28. Power-Up Sequence in Multiplexed Address Mode** for the power-up sequence.

Figure 2-26. Command Description in Multiplexed
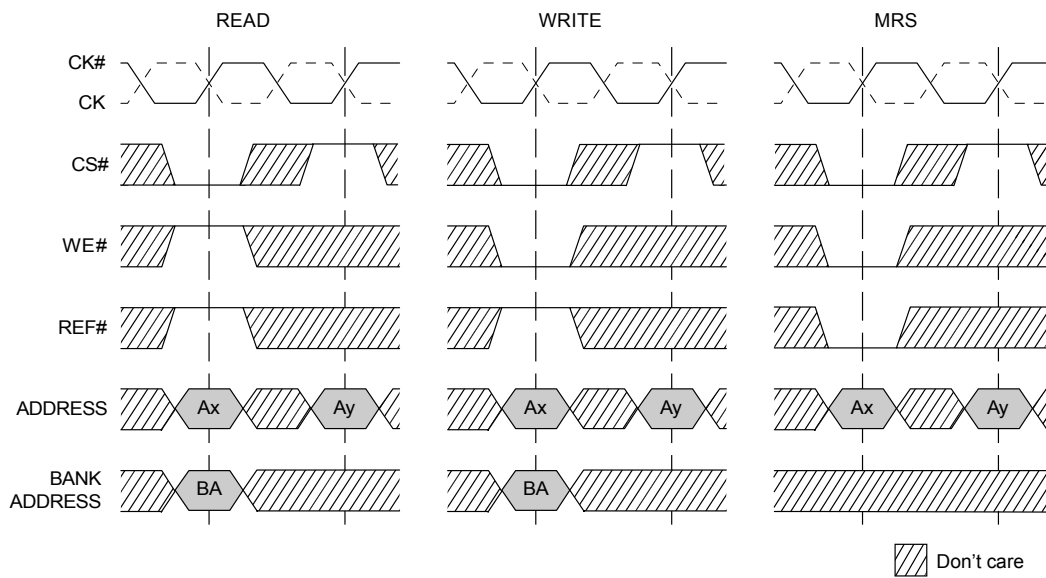
Remarks **1.** Ax, Ay: Address

         BA   : Bank Address

     2. The minimum setup and hold times of the two address parts are defined t_{AS} and t_{AH}.

Figure 2-27. Mode Register Set Command in Multiplexed Address Mode

Ax	A17 ••••• A10	A9	A8			A5	A4	A3			A0
Ay	A17 ••••• A10			A9	A8				A4	A3	

Reserved [Note 1]	On-Die Termination	Impedance Matching	PLL Reset	Unused	Address Mux	Burst Length		Configuration	

On-Die Termination

A9x	Termination
0	Disabled (default)
1	Enabled

PLL Reset

A9y	PLL Reset
0	PLL reset (default)
1	PLL enabled

Burst Length

A4x	A3x	BL
0	0	2 (default)
0	1	4
1	0	8 [Note 2]
1	1	Not valid

Configuration

A4y	A3y	A0x	Configuration
0	0	0	1 [Note 2] (default)
0	0	1	1 [Note 2]
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Impedance Matching

A8x	Resistor
0	Internal 50 Ω [Note 3] (default)
1	External [Note 4]

Address Mux

A5x	Address Mux
0	Nonmultiplexed (default)
1	Address multiplexed

Notes 1. Bits A10–A17 must be set to all '0'.

2. BL=8 is not available for configuration 1.

3. ±30% temperature variation.

4. Within 15%.

Remark The address A0, A3, A4, A5, A8, and A9 must be set as follows in order to activate the mode register in the multiplexed address mode.

Figure 2-28. Power-Up Sequence in Multiplexed Address Mode
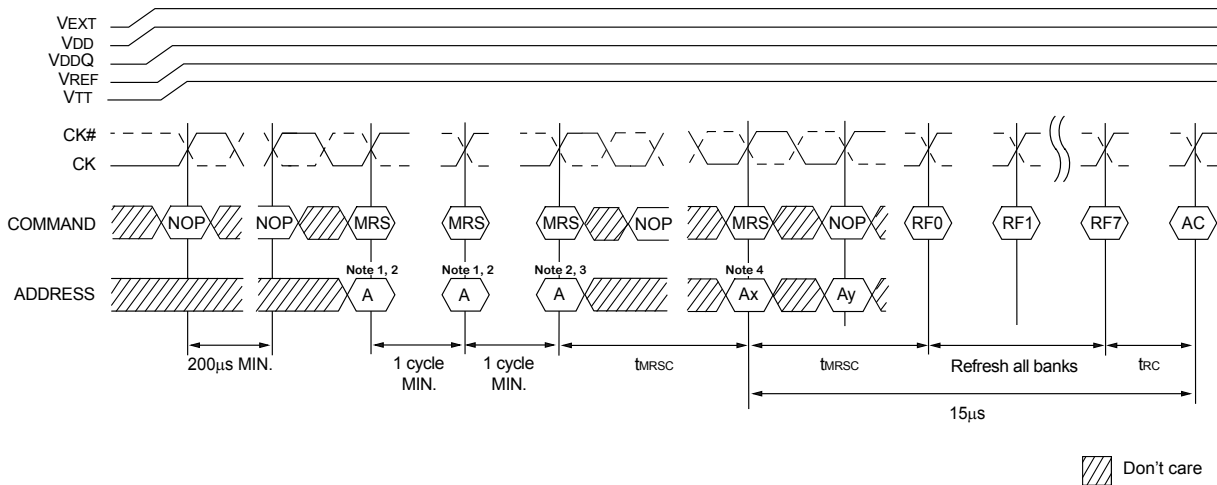
Notes 1. Recommended all address pins held LOW during dummy MRS command.

2. A10-A17 must be LOW.

3. Address A5 must be set HIGH (muxed address mode setting when μPD48288118-A is in normal mode of operation).

4. Address A5 must be set HIGH (muxed address mode setting when μPD48288118-A is already in muxed address mode).

Remark MRS: MRS command

RFp : REFRESH Bank p

AC : any command

2.15 Address Mapping in Multiplexed Mode

The address mapping is described in **Table 2-6** as a function of data width and burst length.

Table 2-6. Address Mapping in Multiplexed Address Mode

Data Width	Burst Length	Ball	Address										
			A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
x18	BL=2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL=4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL=8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

Remark X means "Don't care".

2.16 Read & Write configuration in Multiplexed Address Mode

In multiplexed address mode, the READ and WRITE latencies are increased by one clock cycle. The μPD48288118-A cycle time remains the same, as described in **Table 2-7**.
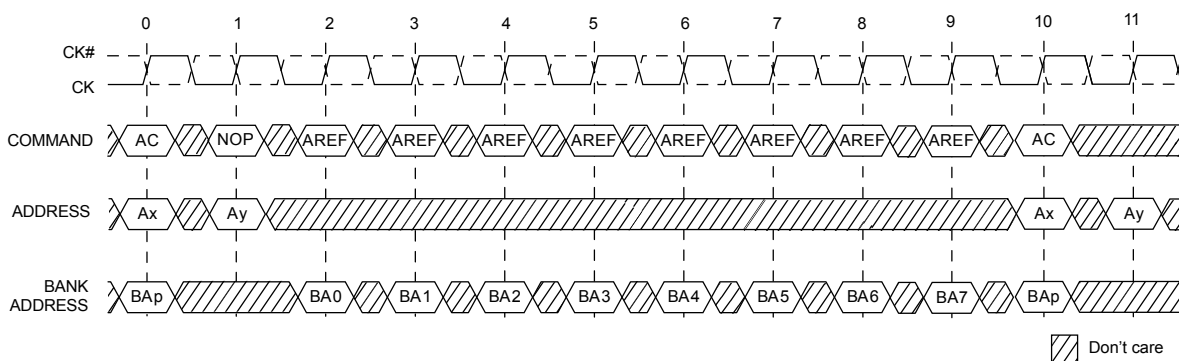
Table 2-7. Configuration in Multiplexed Address Mode

Frequency	Symbol	Configuration			Unit
		1 Note	2	3	
	t_{RC}	4	6	8	Cycles
	t_{RL}	5	7	9	Cycles
	t_{WL}	6	8	10	Cycles
400MHz	t_{RC}			20.0	ns
	t_{RL}			22.5	ns
	t_{WL}			25.0	ns
300MHz	t_{RC}		20.0	26.7	ns
	t_{RL}		23.3	30.0	ns
	t_{WL}		26.7	33.3	ns
200MHz	t_{RC}	20.0	30.0	40.0	ns
	t_{RL}	25.0	35.0	45.0	ns
	t_{WL}	30.0	40.0	50.0	ns

Note BL=8 is not available for configuration 1.

2.17 Refresh Command in Multiplexed Address Mode

Similar to other commands, the refresh command is executed on the next rising clock edge when in the multiplexed address mode. However, since only bank address is required for AREF, the next command can be applied on the following clock. The operation of the AREF command and any other command is represented in **Figure 2-29**.

Figure 2-29. Burst REFRESH Operation

Remark AREF : AUTO REFRESH

AC : Any command

Ax : First part Ax of address

Ay : Second part Ay of address

BAp : Bank p is chosen so that t_{RC} is met.

Figure 2-30. WRITE Burst Basic Sequence: BL=4, with Multiplexed Addresses, Configuration 1
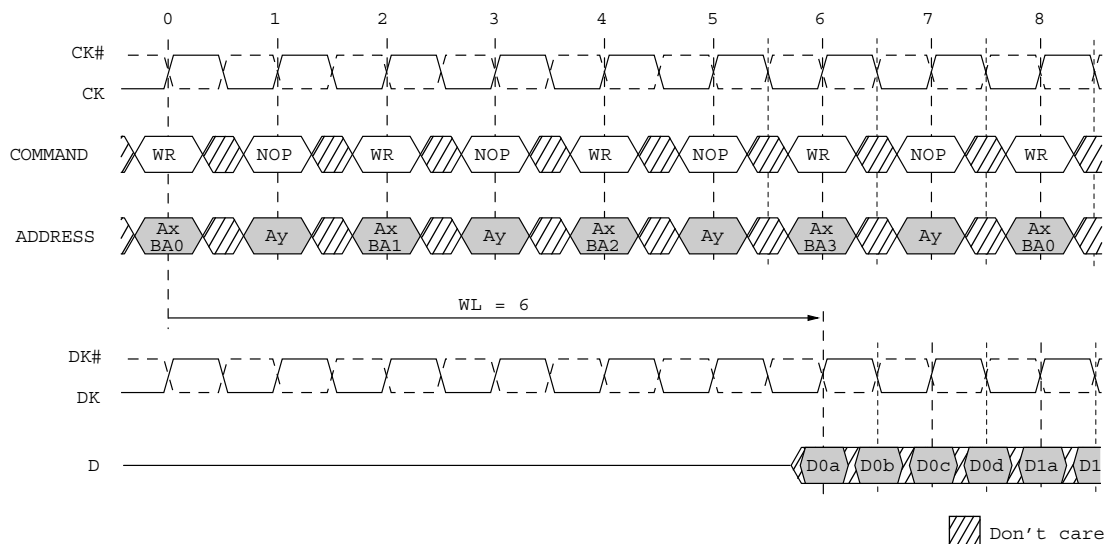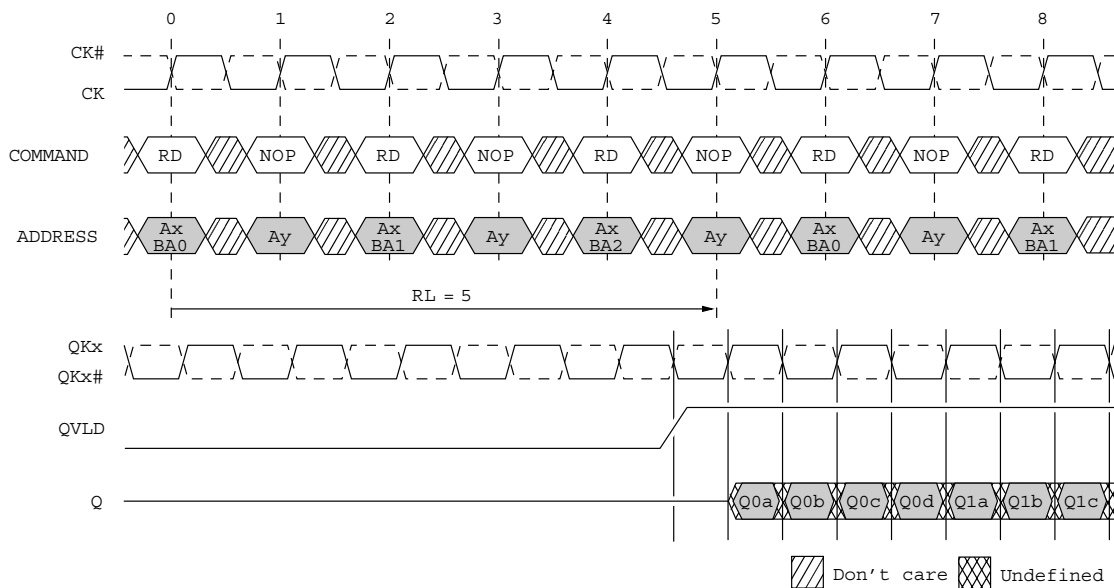

Figure 2-31. READ Burst Basic Sequence: BL=4, with Multiplexed Addresses, Configuration 1, RL=5

Remark   WR   : WRITE command

RD   : READ command

Ax/BAp : Address Ax of bank p

Ay   : Address Ay of bank p

Dpq   : Data q to bank p

Qpq   : Data q from bank p

WL   : WRITE latency

RL   : READ latency

3. JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Table 3-1. Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	12A	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	11A	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	12V	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	11V	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.

Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK. The TAP controller state is also reset on the POWER-UP.
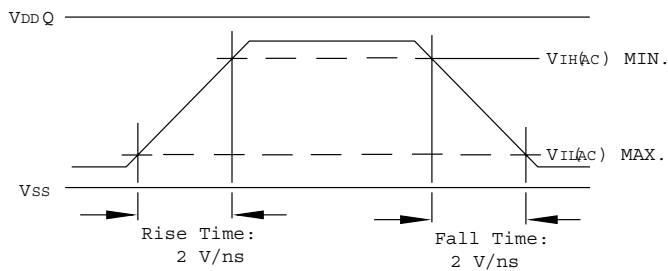
Table 3-2. JTAG DC Characteristics (0°C ≤ T_C ≤ 95°C, 1.7 V ≤ V_{DD} ≤ 1.9 V, unless otherwise noted)

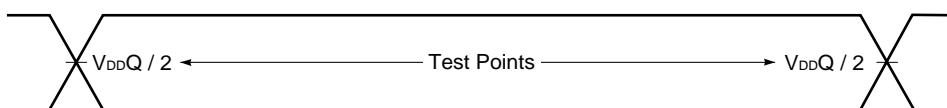| Parameter	Symbol	Conditions	MIN.	MAX.	Unit
JTAG Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}	−5.0	+5.0	μA
JTAG I/O leakage current	I_{LO}	0 V ≤ V_{IN} ≤ $V_{DD}Q$, Outputs disabled	−5.0	+5.0	μA
JTAG input HIGH voltage	V_{IH}		V_{REF} + 0.15	V_{DD} + 0.3	V
JTAG input LOW voltage	V_{IL}		V_{SSQ} − 0.3	V_{REF} − 0.15	V
JTAG output HIGH voltage	V_{OH1}	| I_{OHC} | = 100 μA	V_{DDQ} − 0.2		V
	V_{OH2}	| I_{OHT} | = 2 mA	V_{DDQ} − 0.4		V
JTAG output LOW voltage	V_{OL1}	I_{OLC} = 100 μA		0.2	V
	V_{OL2}	I_{OLT} = 2 mA		0.4	V

Note 1. All voltages referenced to V_{SS} (GND).

  2. Overshoot: $V_{IH\,(AC)}$ ≤ V_{DD} + 0.7 V for t ≤ t_{CK}/2.

  Undershoot: $V_{IL\,(AC)}$ ≥ −0.5 V for t ≤ t_{CK}/2.

  During normal operation, $V_{DD}Q$ must not exceed V_{DD}.

JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 0.3 ns)

Output waveform
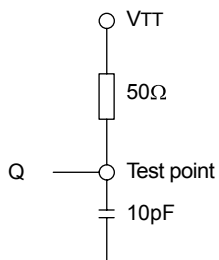

Output load condition

Table 3-3. JTAG AC Characteristics (0°C ≤ Tc ≤ 95°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock						
Clock cycle time	t_{THTH}		20		ns	
Clock frequency	f_{TF}			50	MHz	
Clock HIGH time	t_{THTL}		10		ns	
Clock LOW time	t_{TLTH}		10		ns	
Output time						
TCK LOW to TDO unknown	t_{TLOX}		0		ns	
TCK LOW to TDO valid	t_{TLOV}			10	ns	
Setup time						
TMS setup time	t_{MVTH}		5		ns	
TDI valid to TCK HIGH	t_{DVTH}		5		ns	
Capture setup time	t_{CSJ}		5		ns	1
Hold time						
TMS hold time	t_{THMX}		5		ns	
TCK HIGH to TDI invalid	t_{THDX}		5		ns	
Capture hold time	t_{CHJ}		5		ns	1

Note 1. t_{CSJ} and t_{CHJ} refer to the setup and hold time requirements of latching data from the boundary scan register.
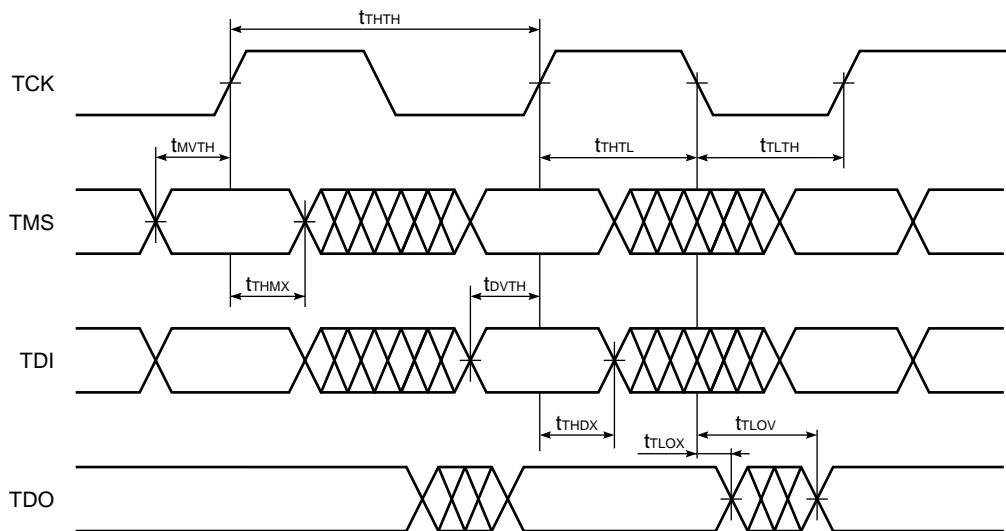
JTAG Timing Diagram

Table 3-4. Scan Register Definition (1)

Register name	Description
Instruction register	The 8 bit instruction registers hold the instructions that are executed by the TAP controller. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible. The bypass register is set LOW (V_{SS}) when the bypass instruction is executed.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Table 3-5. Scan Register Definition (2)

Register name	Bit size	Unit
Instruction register	8	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	113	bit

Table 3-6. ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD48288118-A	16M x 18	0001	0001 1000 1010 0111	00000010000	1

Table 3-7. SCAN Exit Order

Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID
1	DK	K1	39	D11	R11	77	D1	C11
2	DK#	K2	40	D11	R11	78	D1	C11
3	CS#	L2	41	D10	P11	79	Q1	C10
4	REF#	L1	42	D10	P11	80	Q1	C10
5	WE#	M1	43	Q10	P10	81	D0	B11
6	A17	M3	44	Q10	P10	82	D0	B11
7	A16	M2	45	D9	N11	83	Q0	B10
8	A18	N1	46	D9	N11	84	Q0	B10
9	A15	P1	47	Q9	N10	85	Q4	B3
10	Q14	N3	48	Q9	N10	86	Q4	B3
11	Q14	N3	49	DM	P12	87	D4	B2
12	D14	N2	50	A19	N12	88	D4	B2
13	D14	N2	51	A11	M11	89	Q5	C3
14	Q15	P3	52	A12	M10	90	Q5	C3
15	Q15	P3	53	A10	M12	91	D5	C2
16	D15	P2	54	A13	L12	92	D5	C2
17	D15	P2	55	A14	L11	93	Q6	D3
18	QK1	R2	56	BA1	K11	94	Q6	D3
19	QK1#	R3	57	CK#	K12	95	D6	D2
20	D16	T2	58	CK	J12	96	D6	D2
21	D16	T2	59	BA0	J11	97	D7	E2
22	Q16	T3	60	A4	H11	98	D7	E2
23	Q16	T3	61	A3	H12	99	Q7	E3
24	D17	U2	62	A0	G12	100	Q7	E3
25	D17	U2	63	A2	G10	101	D8	F2
26	Q17	U3	64	A1	G11	102	D8	F2
27	Q17	U3	65	(A20)	E12	103	Q8	F3
28	ZQ	V2	66	QVLD	F12	104	Q8	F3
29	Q13	U10	67	Q3	F10	105	(A21)	E1
30	Q13	U10	68	Q3	F10	106	A5	F1
31	D13	U11	69	D3	F11	107	A6	G2
32	D13	U11	70	D3	F11	108	A7	G3
33	Q12	T10	71	Q2	E10	109	A8	G1
34	Q12	T10	72	Q2	E10	110	BA2	H1
35	D12	T11	73	D2	E11	111	A9	H2
36	D12	T11	74	D2	E11	112	NF	J2
37	Q11	R10	75	QK0	D11	113	NF	J1
38	Q11	R10	76	QK0#	D10			

Note Any unused balls that are in the order will read as a logic "0".
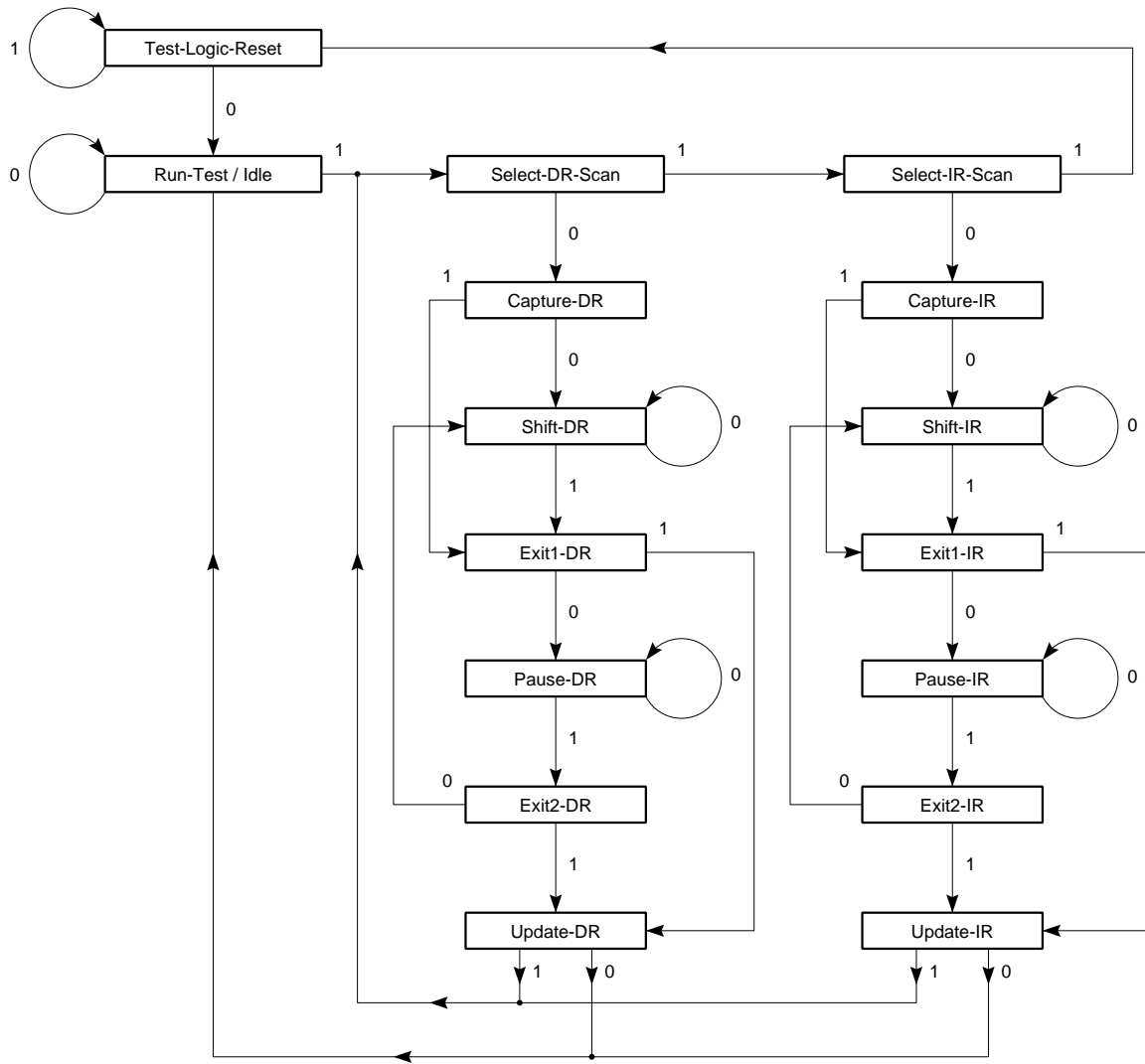
JTAG Instructions

Many different instructions (2^8) are possible with the 8-bit instruction register. All used combinations are listed in **Table 3-8**, Instruction Codes. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RAM is fully compliant to the 1149.1 convention. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.
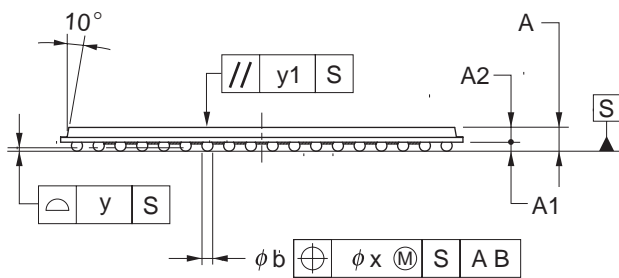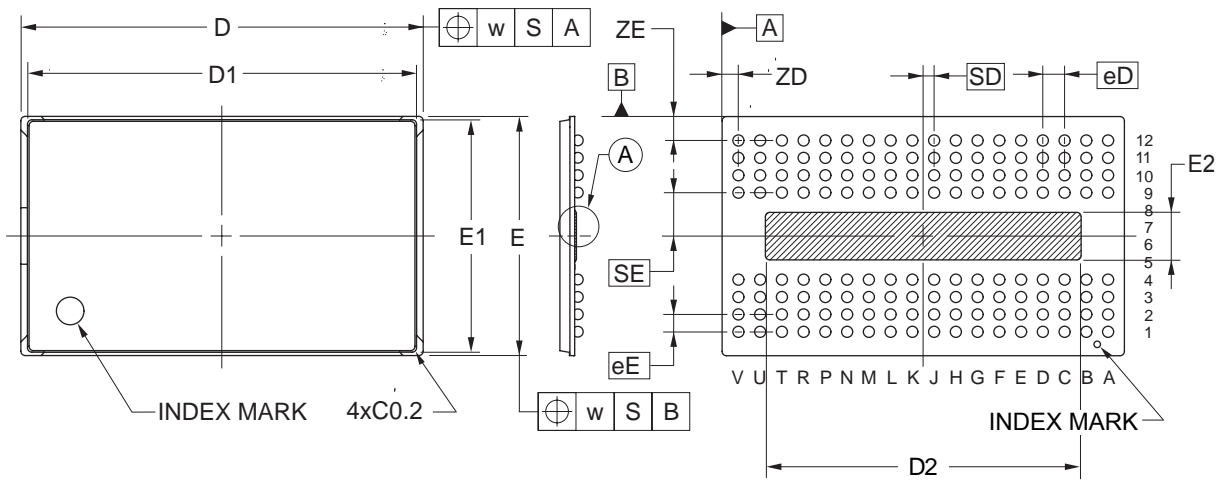
Table 3-8

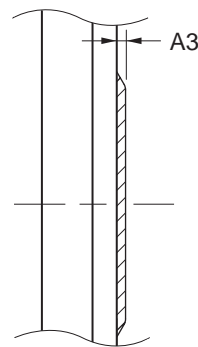| Instructions	Instruction Code [7:0]	Description
EXTEST	0000 0000	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	0010 0001	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
SAMPLE / PRELOAD	0000 0101	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and Q pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
CLAMP	0000 0111	When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register. Selects the bypass register to be connected between TDI and TDO. Data driven by output balls are determined from values held in the boundary scan register.
High-Z	0000 0011	The High-z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RAMs outputs into a High-Z state. Selects the bypass register to be connected between TDI and TDO. All outputs are forced into high impedance state.
BYPASS	1111 1111	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
Reserved for Future Use	–	The remaining instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

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4. Package Drawing

144-PIN TAPE FBGA (μBGA) (18.5x11)

ITEM	DIMENSIONS
D	18.50±0.10
D1	17.90
D2	14.52
E	11.00±0.10
E1	10.70
E2	2.184
w	0.20
A	1.07±0.10
A1	0.39±0.05
A2	0.68
A3	0.08 MAX.
eD	1.00
eE	0.80
SD	0.50
SE	2.00
b	0.51±0.05
x	0.15
y	0.10
y1	0.20
ZD	0.75
ZE	1.10

(UNIT:mm)

P144FF-80-DW1

5. Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

Types of Surface Mount Devices

μPD48288118FF-DW1-A   : 144-pin TAPE FBGA (18.5 x 11)

Quality Grade

• A quality grade of the products is "Standard".

• Anti-radioactive design is not implemented in the products.

• Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the
  ground and so forth.

Revision History	μPD48288118-A

Rev.	Date	Description	
		Page	**Summary**
Rev.1.00	'13.02.01	-	New Data Sheet

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