μPD48011418
μPD48011436

1.1G-BIT Low Latency DRAM-III
Common I/O Burst Length of 4

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Description

The μPD48011418 is a 67,108,864-word by 18-bit and the μPD48011436 is a 33,554,432-word by 36-bit synchronous double data rate Low Latency RAM fabricated with advanced CMOS technology using one-transistor eDRAM memory cell.

The Low Latency DRAM-III chip is a 1.1Gb DRAM capable of a sustained throughput of approximately 57.6 Gbps for burst length of 4 (approximately 51.2 Gbps for applications implementing error correction), excluding refresh overhead and data bus turn-around

With a bus speed of 800 MHz, a burst length of 4, and a t_{RC} of 13.75 ns, the Low Latency DRAM-III chip is capable of achieving this rate when accesses to at least 6 banks of memory are overlapped.

These products are packaged in 180-pin TAPE FBGA.

Specification

- Density: 1,1Gbit
- Organization: 8M words x 18 bits x 8 banks
  4M words x 36 bits x 8 banks
- Operating frequency
  800 MHz (MAX.) @ t_{RC}=13.75 ns
- t_{RC}
  13.75 ns t_{RC} (and 13.75 ns t_{RFC})
- Burst length: 4
- Address bus
  2 cycle DDR address
- Package
  180-pin FBGA (Ball Array: 1 mm x 1 mm Pitch)
  Package size: 18.5 mm x 14 mm
  ROHS 6/6 compliance
- Power supply
  - 2.5 V V_{EXT}
  - 1.5 V V_{DD}
  - 1.0 V $V_{DD}Q$
- Refresh command
  - Auto Refresh : 16384 cycles / 2 ms for each bank
  - Overlapped Refresh with REF# pin
- Operating case temperature: 0 to 95 °C

Features

- 2 cycle 800MHz DDR Muxed Address
- Optional data bus inversion to reduce SSO, SSN, maximum I/O current, and average I/O power
- Training sequence for per-bit deskew
- Selectable Refresh Mode: Auto or Overlapped Refresh
- Programmable PVT-compensated output impedance
- Programmable PVT-compensated on-die input termination
- PLL for improved input jitter tolerance and wide output data valid window

Ordering Information

Part number	Cycle Time ns	Clock Frequency MHz	Random Cycle ns	Output Supply Voltage ($V_{DD}Q$) V	Burst Length	Address Type	Organization (word x bit)	Package
μPD48011418FF-FH12-FF1-A	1.25	800	13.75	1.0	4	DDR	64 M x 18	180-pin
μPD48011418FF-FH15-FF1-A	1.50	667						TAPE FBGA
μPD48011436FF-FH12-FF1-A	1.25	800					32 M x 36	(18.5 x14)
μPD48011436FF-FH15-FF1-A	1.50	667						Lead-free

Pin Configurations

180-pin TAPE FBGA (18.5 x 14) (Top View)

[μPD48011418] (x18)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	TMS	V_{DD}	TCK	$V_{DD}Q$	V_{SS}				V_{SS}	$V_{DD}Q$	V_{EXT}	V_{DD}	QK0
B	V_{SS}	DNU, V_{SS}	V_{SS}	DQ6	V_{DD}		x18		V_{DD}	DNU, V_{SS}	V_{SS}	DQ8	V_{SS}
C	QVLD	$V_{DD}Q$	DNU, V_{SS}	$V_{DD}Q$	DQ4		Burst of 4		DNU, V_{SS}	$V_{DD}Q$	DQ7	$V_{DD}Q$	QK0#
D	V_{SS}	DNU, V_{SS}	V_{SS}	DQ2	V_{SS}		259 sq. mm		V_{SS}	DNU, V_{SS}	V_{SS}	DQ5	V_{SS}
E	DNU, V_{SS}	$V_{DD}Q$	DNU, V_{SS}	$V_{DD}Q$	DQ0				DNU, V_{SS}	$V_{DD}Q$	DQ1	$V_{DD}Q$	DQ3
F	V_{SS}	DINV0	V_{SS}	DNU, $V_{DD}Q$	V_{SS}				V_{SS}	DNU, $V_{DD}Q$	V_{SS}	DNU, V_{SS}	V_{SS}
G	V_{DD}	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	DNU, $V_{DD}Q$				DNU, $V_{DD}Q$	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	V_{DD}
H	V_{SS}	RST#	V_{SS}	A6	V_{SS}		Top View		V_{SS}	A5	V_{SS}	DM	V_{SS}
J	MF	$V_{DD}Q$	DK0	V_{SS}	V_{DD}				CK	V_{SS}	DNU, V_{SS}	$V_{DD}Q$	LBK#
K	V_{REF}	V_{SS}	DK0#	$V_{DD}Q$	V_{DD}				CK#	$V_{DD}Q$	DNU, V_{SS}	V_{SS}	V_{REF}
L	TRST#	CS#	V_{SS}	A4	V_{SS}				V_{SS}	A3	V_{SS}	WE#	V_{SS}
M	V_{DD}	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	A2				REF#	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	V_{DD}
N	V_{SS}	DINV1	V_{SS}	A0	V_{SS}				V_{SS}	A1	V_{SS}	DNU, V_{SS}	V_{SS}
P	DNU, V_{SS}	$V_{DD}Q$	DNU, V_{SS}	$V_{DD}Q$	DQ9				DNU, V_{SS}	$V_{DD}Q$	DQ10	$V_{DD}Q$	DQ12
R	V_{SS}	DNU, V_{SS}	V_{SS}	DQ11	V_{SS}				V_{SS}	DNU, V_{SS}	V_{SS}	DQ14	V_{SS}
T	QK1#	$V_{DD}Q$	DNU, V_{SS}	$V_{DD}Q$	DQ13				DNU, V_{SS}	$V_{DD}Q$	DQ16	$V_{DD}Q$	TDO
U	V_{SS}	DNU, V_{SS}	V_{SS}	DQ15	V_{DD}				V_{DD}	DNU, V_{SS}	V_{SS}	DQ17	V_{SS}
V	QK1	V_{DD}	ZQ	$V_{DD}Q$	V_{SS}				V_{SS}	$V_{DD}Q$	V_{EXT}	V_{DD}	TDI

DQ0–DQ17	: Data inputs / output	REF#	: Refresh Enable
DINV0–DINV1	: Data inversion	LBK#	: Loopback Mode
DM	: Write data mask	MF	: Mirror Function
A0–A6	: Address	TMS	: IEEE 1149.1 Test input
CK, CK#	: Input clock	TDI	: IEEE 1149.1 Test input
DK0, DK0#	: Input data clock	TCK	: IEEE 1149.1 Clock input
QVLD	: Read Data Valid	TDO	: IEEE 1149.1 Test output
QK0–QK1, QK0#–QK1#	: Output data clock	TRST#	: IEEE 1149.1 Test Reset Input
		V_{REF}	: HSTL input reference input
ZQ	: Output impedance & Input termination control	V_{DD}	: Power Supply, 1.5 V nominal
		$V_{DD}Q$	: DQ Power Supply, 1.0 V nominal
RST#	: Master reset	V_{EXT}	: Power Supply, 2.5 V nominal
CS#	: Chip select	V_{SS}	: Ground
WE#	: Write Enable	DNU, V_{SS}	: Must not be used, or must be connected to V_{SS}
		DNU, $V_{DD}Q$	: Must not be used, or must be connected to $V_{DD}Q$

180-pin TAPE FBGA (18.5 x 14) (Top View)

[μPD48011436] (x36)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	TMS	V_{DD}	TCK	$V_{DD}Q$	V_{SS}				V_{SS}	$V_{DD}Q$	V_{EXT}	V_{DD}	QK0
B	V_{SS}	DQ9	V_{SS}	DQ6	V_{DD}		x36		V_{DD}	DQ11	V_{SS}	DQ8	V_{SS}
C	QVLD	$V_{DD}Q$	DQ10	$V_{DD}Q$	DQ4		Burst of 4		DQ13	$V_{DD}Q$	DQ7	$V_{DD}Q$	QK0#
D	V_{SS}	DQ12	V_{SS}	DQ2	V_{SS}		259 sq. mm		V_{SS}	DQ15	V_{SS}	DQ5	V_{SS}
E	DQ16	$V_{DD}Q$	DQ14	$V_{DD}Q$	DQ0				DQ17	$V_{DD}Q$	DQ1	$V_{DD}Q$	DQ3
F	V_{SS}	DINV0	V_{SS}	DNU, $V_{DD}Q$	V_{SS}				V_{SS}	DNU, $V_{DD}Q$	V_{SS}	DINV1	V_{SS}
G	V_{DD}	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	DNU, $V_{DD}Q$				DNU, $V_{DD}Q$	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	V_{DD}
H	V_{SS}	RST#	V_{SS}	A6	V_{SS}		Top View		V_{SS}	A5	V_{SS}	DM	V_{SS}
J	MF	$V_{DD}Q$	DK0	V_{SS}	V_{DD}				CK	V_{SS}	DK1	$V_{DD}Q$	LBK#
K	V_{REF}	V_{SS}	DK0#	$V_{DD}Q$	V_{DD}				CK#	$V_{DD}Q$	DK1#	V_{SS}	V_{REF}
L	TRST#	CS#	V_{SS}	A4	V_{SS}				V_{SS}	A3	V_{SS}	WE#	V_{SS}
M	V_{DD}	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	A2				REF#	$V_{DD}Q$	DNU, $V_{DD}Q$	$V_{DD}Q$	V_{DD}
N	V_{SS}	DINV2	V_{SS}	A0	V_{SS}				V_{SS}	A1	V_{SS}	DINV3	V_{SS}
P	DQ35	$V_{DD}Q$	DQ34	$V_{DD}Q$	DQ18				DQ33	$V_{DD}Q$	DQ19	$V_{DD}Q$	DQ21
R	V_{SS}	DQ32	V_{SS}	DQ20	V_{SS}				V_{SS}	DQ31	V_{SS}	DQ23	V_{SS}
T	QK1#	$V_{DD}Q$	DQ30	$V_{DD}Q$	DQ22				DQ29	$V_{DD}Q$	DQ25	$V_{DD}Q$	TDO
U	V_{SS}	DQ28	V_{SS}	DQ24	V_{DD}				V_{DD}	DQ27	V_{SS}	DQ26	V_{SS}
V	QK1	V_{DD}	ZQ	$V_{DD}Q$	V_{SS}				V_{SS}	$V_{DD}Q$	V_{EXT}	V_{DD}	TDI

DQ0–DQ35	: Data inputs / output	REF#	: Refresh Enable
DINV0–DINV3	: Data inversion	LBK#	: Loopback Mode
DM	: Write data mask	MF	: Mirror Function
A0–A6	: Address	TMS	: IEEE 1149.1 Test input
CK, CK#	: Input clock	TDI	: IEEE 1149.1 Test input
DK0–DK1, DK0#–DK1#	: Input data clock	TCK	: IEEE 1149.1 Clock input
		TDO	: IEEE 1149.1 Test output
QVLD	: Read Data Valid	TRST#	: IEEE 1149.1 Test Reset Input
QK0–QK1, QK0#–QK1#	: Output data clock	V_{REF}	: HSTL input reference input
		V_{DD}	: Power Supply, 1.5 V nominal
ZQ	: Output impedance & Input termination control	$V_{DD}Q$	: DQ Power Supply, 1.0 V nominal
		V_{EXT}	: Power Supply, 2.5 V nominal
RST#	: Master reset	V_{SS}	: Ground
CS#	: Chip select	DNU, V_{SS}	: Must not be used, or must be connected to V_{SS}
WE#	: Write Enable	DNU, $V_{DD}Q$	: Must not be used, or must be connected to $V_{DD}Q$

Pin Identification (1/2)

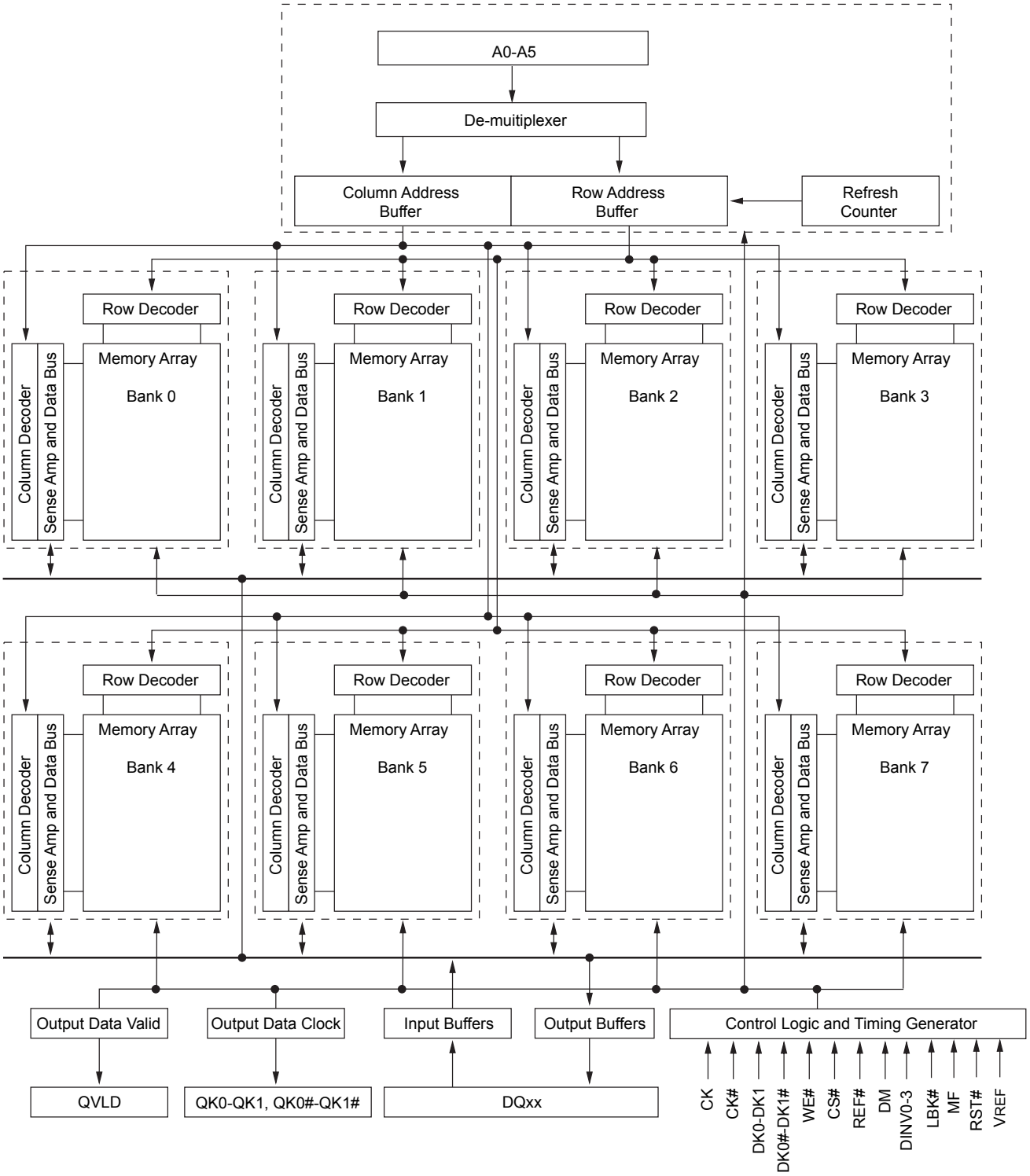
Symbol	Direction	I/O Type	Freq MHz	Description
CK, CK#	Input	1.0 V HSIO	800 / 667	Clock inputs: CK and CK# are differential clock inputs. This input clock pair registers address and control inputs on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
DK0-DK1, DK0#-DK1#	Input	1.0 V HSIO	800 / 667	Differential clocks for DQ inputs: DK0, DK0# => DQ0-DQ17, DM DK1, DK1# => DQ18-DQ35 Note that DK1,DK1# are only active on x36 parts.
CS#	Input	1.0 V HSIO	800 / 667	Chip select CS# enables the commands when CS# is LOW and disables them when CS# is HIGH. When the command is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	1.0 V HSIO	800 / 667	Write enable, Refresh enable : WE#, REF# are sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be executed.
RST#	Input	1.0 V HSIO (no ODT)	-	Master reset Note that this pin has no on-die termination.
LBK#	Input	1.0 V HSIO (no ODT)	-	Loopback mode for control pin de-skew training Note that this pin has no on-die termination.
MF	Input	1.0 V HSIO (no ODT)	DC	Causes “mirroring” of certain pins as described in **2.14 Clam-shell support.** Note that this pin has no on-die termination.
A0-A6	Input	1.0 V HSIO	800 / 667	Address inputs for DDR Address BL4: Address bus, including bank select bits. A 6 is reserved for future use.
DQ0-DQ35	Input /Output	1.0 V HSIO	800 / 667	Data input/output: The DQ signals form the 36 bit data bus. During READ commands, the data is referenced to both edges of QKx. During WRITE commands, the data is sampled at both edges of DKx. Notethat DQ18-DQ35 are only active on x36 parts.
DINV0-DINV3	Input /Output	1.0 V HSIO	800 / 667	Data inversion state for DQ inputs: DINV0 => DQ0-DQ8 DINV1 => DQ9-DQ17 DINV2 => DQ18-DQ26 DINV3 => DQ27-DQ35 Note that DINV2-DINV3 are only active on x36 parts
DM	Input	1.0 V HSIO	800 / 667	Write data mask; disables writing of the corresponding data value. Clocked by DK0.

(2/2)

Symbol	Direction	I/O Type	Freq MHz	Description
QK0-QK1, QK0#-QK1#	Output	1.0 V HSIO	800 / 667	Output data clocks: Differential clocks for DQ, QVLD outputs: QK0/QK0# => x36: DQ0-DQ17, x18: DQ0-DQ8, QVLD QK1/QK1# => x36: DQ18-DQ35, x18: DQ9-DQ17
QVLD	Output	1.0 V HSIO	800 / 667	Data valid; The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.
TMS, TDI	Input	1.0 V HSIO		JTAG function pins: IEEE 1149.1 test inputs: These balls may be left as no connects if the JTAG function is not used in the circuit
TCK	Input	1.0 V HSIO		JTAG function pin; IEEE 1149.1 clock input: This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.
TDO	Output	1.0 V HSIO		JTAG function pin; IEEE 1149.1 test output: JTAG output. This ball may be left as no connect if JTAG function is not used.
TRST#	Input	1.0 V HSIO		JTAG reset; IEEE 1149.1 test rest: This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.
ZQ	Analog			Output impedance and input termination control
V_{REF}	Ref			V_{DD}Qx0.7 V I/O reference voltage.
VEXT	Supply			Power supply; 2.5 V nominal. See **Recommended DC Operating Conditions** for range.
V_{DD}	Supply			Power supply; 1.5 V nominal. See **Recommended DC Operating Conditions** for range.
V_{DD}Q	Supply			DQ power supply; Nominally, 1.0 V. Isolated on the device for improved noise immunity. See Recommended DC Operating Conditions for range.
V_{SS}	Supply			Ground
DNU, V_{SS}				Do Not Use, Or must not be used, or must be connected to V_{SS}.
DNU, V_{DD}Q				Do Not Use, Or must not be used, or must be connected to V_{DD}Q

HSIO is a single-ended 1.0 V high-side terminated I/O described in **1. Electrical Specifications**.

Block Diagram



Contents

1. Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{EXT}	2.5 V nominal	–0.3 to +2.8	V
Supply voltage	V_{DD}	1.5 V nominal	–0.3 to +1.95	V
Output supply voltage, Input voltage, Input / Output voltage	$V_{DD}Q$	1.0 V nominal	–0.3 to +1.35	V
Input / Output voltage	V_{IH} / V_{IL}	1.0 V nominal	–0.3 to +1.35	V
Junction temperature	T_j MAX.		105	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

0°C ≤ T_C ≤ 95°C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Comments	Note
Supply voltage	V_{EXT}	2.3	2.5	2.7	V		1
Supply voltage	V_{DD}	1.395	1.5	1.605	V		1
Output supply voltage	$V_{DD}Q$	0.95	1.0	1.05	V		1
Reference voltage	V_{REF}	$V_{DD}Q$*0.69	$V_{DD}Q$*0.7	$V_{DD}Q$*0.71	V		1,2,4
High level output voltage	$V_{OH (DC)}$	$V_{DD}Q$–0.025			V		1
Low level output voltage	$V_{OL (DC)}$		$V_{DD}Q$*0.4		V	Z_{ol}=40 Ω, R_L=60 Ω	1
High level input voltage	$V_{IH (DC)}$	V_{REF}+0.07		$V_{DD}Q$+0.3	V		1,4
Low level input voltage	$V_{IL (DC)}$	–0.3		V_{REF}–0.07	V		1,4
Clock input voltage	V_{In}	–0.3		$V_{DD}Q$+0.3	V		
Clock differential voltage	V_{ID}	0.2		$V_{DD}Q$+0.6	V		
Output Impedance HIGH	Zoh		60		Ω		3
Output Impedance LOW	Zol		40		Ω		3
Input Impedance LOW	Zi		60		Ω		4

Notes 1. All voltage referenced to V_{SS} (GND)

2. Peak - to - Peak AC noise on V_{REF} must not exceed +/- 2 % $V_{DD}Q$ (DC)

3. Programmable via ZQ and Reset Impedance Control

4. High-side termination (programmable via ZQ and Reset/MRS)

DC Characteristics

0°C ≤ T_C ≤ 95°C; 1.395 V ≤ V_{DD} ≤ 1.605 V, unless otherwise noted

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Note
Input leakage current	I_{LI}		0	50	μA	1
Output leakage current	I_{LO}		0	50	μA	1
3 state leakage current	Ioz		0	50	μA	1

Notes 1. Outputs Driver High-Z and ODT Disabled.

Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Input capacitance (CK,DK, CS#, WE#, REF#, A)	C_{IN}	V_{IN} = 0 V		1.5	pF
I/O, Output, Other capacitance (DQ, DINV, QVLD, DM)	$C_{I/O}$	$V_{I/O}$ = 0 V		1.8	pF
Input capacitance delta between differential clock pins	C_{DCK}	V_{IN} = 0 V		0.15	pF
Input capacitance delta between DQ pins	C_{DDQ}	$V_{I/O}$ = 0 V		0.2	pF
Input capacitance delta between CS#, WE#, REF#, A pins	C_{DCTL}	V_{IN} = 0 V		0.2	pF

Remark These parameters are periodically sampled and not 100% tested.
Capacitance is not tested on ZQ pin.

Recommended AC Operating Conditions

0°C ≤ T_C ≤ 95°C; 1.395 V ≤ V_{DD} ≤ 1.605 V, unless otherwise noted

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Input HIGH voltage	$V_{IH\ (AC)}$		V_{REF}+0.13	$V_{DD}Q$+0.3	V	1
Input LOW voltage	$V_{IL\ (AC)}$		–0.3	V_{REF}–0.13	V	1

Note 1. Overshoot: $V_{IH\ (AC)} \leq V_{DD}Q$+0.3 V for t ≤ t_{CK}/5
Undershoot: $V_{IL\ (AC)} \geq$ –0.3 V for t ≤ t_{CK}/5
Control input signals may not have pulse widths less than t_{CKH} (MIN.) or operate at cycle rates less than t_{CK} (MIN.).

DC Characteristics

Parameter	Symbol	Test condition	Max		Unit	Note
Total power consumption	PD	Nominal supply voltage Sequential bank access Overlapped refresh mode Data inversion enabled Half address and data transitions 30% Write and 70% Read operation ODT=60Ω, Zoh/Zol = 60Ω/40Ω Tc=95°C	x18	2.0	w	1
			x36			

Note 1. Including all the power supply (V_{DD}, $V_{DD}Q$ and V_{EXT})

AC Characteristics

Normal bus timing

Standard bus timing waveforms and values for command and data are shown in **Figure 1-1** through **Figure 1-5** and **Interface AC Parameters**. All timing is measured to/from the crossing point on differential clocks and to/from the V_{REF} crossing point on single-ended signals.

Figure 1-1 Command and DDR Address Input Timing Waveforms

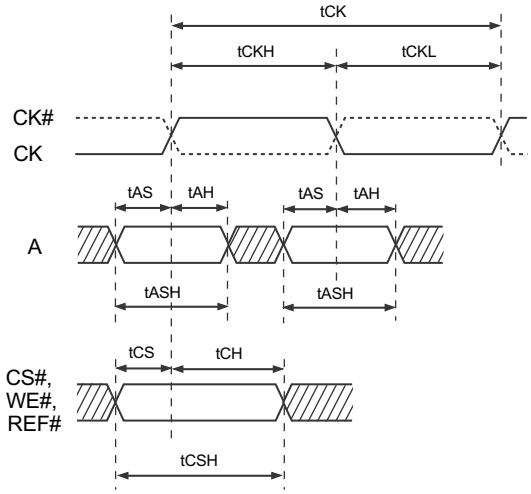


Figure 1-2 Data Input Timing Waveforms

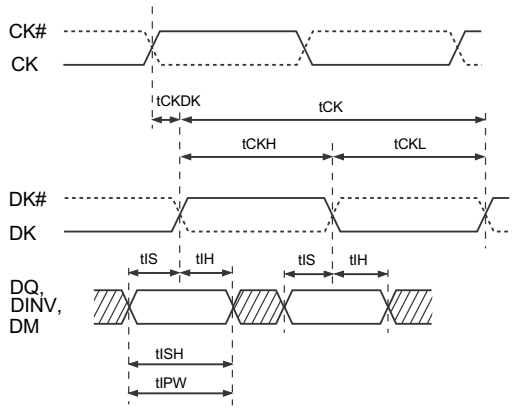


Figure 1-3 Data Output Timing Waveforms

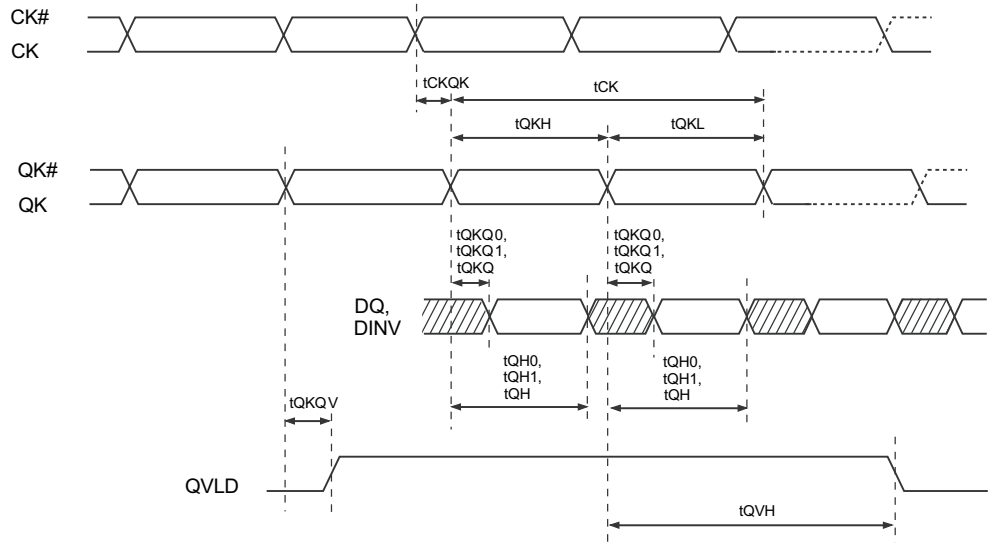


Figure 1-4 Output Driver Enable/Disable Timing

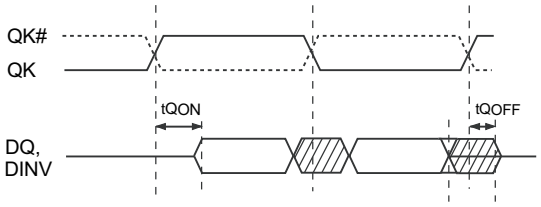
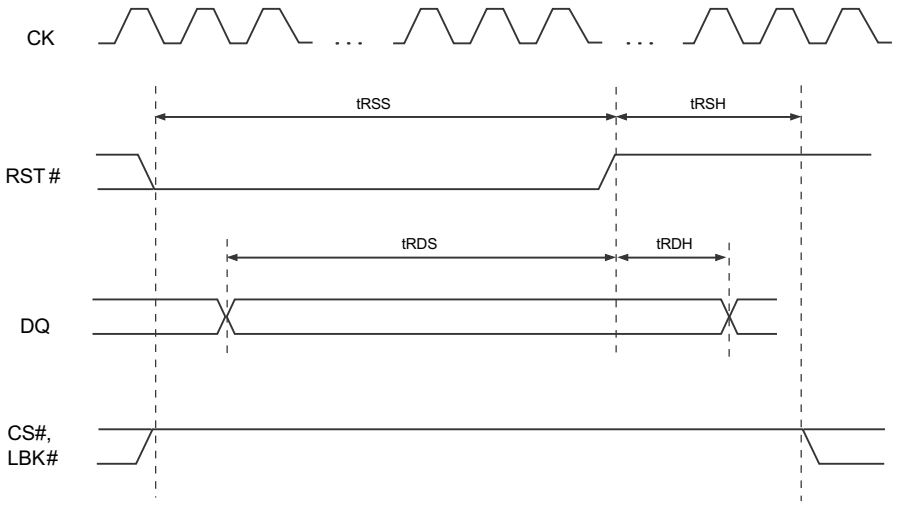


Figure 1-5 Reset Timing Waveforms



Note The clock must be with specification and all other chip inputs must be driven to legal values throughout the t_{RSS} period.

Interface AC Parameters

(1/2)

Parameter	Symbol	–FH12 (800 MHz)		–FH15 (667 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
CK, DK, QK clock period (maximum 800 MHz clock frequency, minimum 400 MHz)	t_{CK}	1.250	2.500	1.587	2.500	ns	
CK, DK LOW time (assumes 5% duty cycle distortion at 800 MHz)	t_{CKL}	0.45*		0.45*		t_{CK}(avg)	5
CK, DK HIGH time (assumed 5% duty cycle distortion at 800 MHz)	t_{CKH}	0.45*		0.45*		t_{CK}(avg)	5
Clock period jitter	t_{JIT}(per)	–0.070	0.070	–0.070	0.070	ns	6,7
Cycle-to-cycle clock jitter	t_{JIT}(cc)		0.140		0.140	ns	
A to CK setup	t_{AS}	0.160		0.192		ns	2
CK to A hold	t_{AH}	0.160		0.192		ns	1
CK to A setup/hold window	t_{ASH}	0.160		0.192		ns	4
A input pulse width	t_{APW}	0.200		0.240		ns	
CS#, WE#, REF# to CK setup	t_{CS}	0.180		0.215		ns	2
CK to CS#, WE#, REF # hold	t_{CH}	0.180		0.215			1
CK to CS#, WE#, REF# setup/hold window	t_{CSH}	0.300		0.358		ns	4
CS#, WE#, REF# input pulse width	t_{CPW}	0.400		0.480		ns	
CK to DK skew	t_{CKDK}	–0.200	0.200	–0.240	0.240	ns	
DQ, DINV, DM to DK setup	t_{IS}	0.160		0.192		ns	2
DK to DQ, DINV, DM hold	t_{IH}	0.160		0.192		ns	1
DK to DQ, DINV, DM setup/hold window	t_{ISH}	0.160		0.192		ns	4
DQ, DINV, DM input pulse width	t_{IPW}	0.200		0.240		ns	
Output signal rise time [See note]	t_{Rise}	2	5	2	5	V/ns	3
Output signal rise time [See note]	t_{Fall}	2	5	2	5	V/ns	3
QK LOW time (assumes 5% duty cycle distortion at 800 MHz)	t_{QKL}	0.45*		0.45*		t_{CK}(avg)	5
QK HIGH time (assumed 5% duty cycle distortion at 800 MHz)	t_{QKH}	0.45*		0.45*		t_{CK}(avg)	5
CK to QK skew	t_{CKQK}	–0.300	0.300	–0.358	0.358	ns	
Additional t_{RL} delay in loopback	t_{CD}		5		5	ns	
QK0 to DQ[17:0], DINV[1:0] (x36) or DQ[8:0], DINV[0] (x18)	t_{QKQ0}		0.100		0.120	ns	8
QK0 to DQ[17:0], DINV[1:0] (x36) or DQ[8:0], DINV[0] (x18)	t_{QH0}	0.4*		0.4*		t_{CK}(avg)	5
QK1 to DQ[35:18], DINV[3:2] (x36) or DQ[17:9],DINV[1] (x18)	t_{QKQ1}		0.100		0.120	ns	8
QK1 to DQ[35:18], DINV[3:2] (x36) or DQ[17:9],DINV[1] (x18)	t_{QH1}	0.4*		0.4*		t_{CK}(avg)	5

(2/2)

Parameter	Symbol	–FH12 (800 MHz)		–FH15 (667 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Any QK to any DQ, DINV	t_{QKQ}		0. 150		0.180	ns	8
Any QK to any DQ, DINV	t_{QH}	0.35*		0.35*		t_{CK}(avg)	5
Any QK to QVLD	t_{QKQV}		0. 150		0.180	ns	
Any QK to QVLD	t_{QVH}	0.85*		0.85*		t_{CK}(avg)	5
QK to DQ output driver turn-on time and ODT turn-on time	t_{QON}		0.100		0.120	ns	
QK to DQ output driver turn-off time and ODT turn-on time	t_{QOFF}	–0.1*	0.100	–0.1*	0.100	t_{CK}(avg)	5
DQ to RST# setup	t_{RDS}	1000 *		1000 *		t_{CK}	2
DQ to RST# hold	t_{RDH}	5 *		5 *		t_{CK}	1
RST# pulse length	t_{RSS}	200		200		μs	
RST# deasserted to CS# or LBK# asserted	t_{RSH}	400000 *		400000 *		t_{CK}	
Time for PLL to stabilize after being enabled	t_{PLL}		20		20	μs	
MRS command start to next CS#, or LBK# assertion; also from previous command to MRS command	t_{MRD}	24 *		24 *		t_{CK}	

Notes 1. All input hold timing assumes rising edge slew rate of 2 V/ns measured from V_{IL}/V_{IH} (DC) to V_{REF}.

2. All input setup timing assumes falling edge slew rate of 2 V/ns measured from V_{REF} to V_{IL}/V_{IH}(AC)

3. All output timing assumes the load shown in **Figure 1-6**.

4. Setup/hold windows, t_{ASH}, t_{CSH}, t_{ISH} are used for de-skew timing budgeting and are based on electrical simulations. These cannot be directly measured without performing de-skew training.

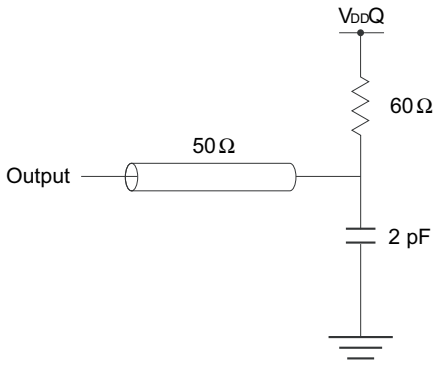
5. t_{CK} (avg) is the value of t_{CK} averaged over 200 clock cycles.

6. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.

7. Frequency drift is not allowed.

8. t_{QKQ}, t_{QKQ0} and t_{QKQ1} are guaranteed by design.

Figure 1-6 Output Load



Temperature and Thermal Impedance

Temperature Limits

Parameter	Symbol	MIN.	MAX.	Unit	Note
Reliability junction temperature	T_J	0	+105	°C	1
Operating junction temperature	T_J	0	+100	°C	2
Operating case temperature	T_C	0	+95	°C	3

Notes 1. Temperatures greater than 105°C may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the part.

2. Junction temperature depends upon cycle time, loading, ambient temperature, and airflow.

3. MAX operating case temperature; T_C is measured in the center of the package. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.

Thermal Impedance

Substrate	θja (°C/W)			θjb	θjc
	Air Flow = 0 m/s	Air Flow = 1 m/s	Air Flow = 2 m/s	(°C/W)	(°C/W)
4 - Layer	17.5	14.0	13.1	8.2	0.8

Impedance Controls

The Low Latency DRAM-III includes programmable impedance control that affects the output impedance of all output and bidirectional pins, as well as the termination of all input and bidirectional pins. The output impedance control affects all output pins and the input termination control affects those pins grouped together as shown in **Table 3-5** and **Table 3-6**. The impedance control affects the drive strengths of both high and low values, as well as the high-side termination impedance. The impedance is controlled via a precision resistor connected between the ZQ and V_{SS} pins. The nominal value of the precision (1%) resistor is 240 Ω, with a supported range of 200 to 240 Ω.

The output impedance accuracy is within 15% of the programmed nominal value, with the linearity measured at the points described in **Impedance Test Parameters**. The actual impedance must remain within the range specified by the linear interpolation of the values at those points.

Normally, the input termination and output impedance are continuously adjusted, such that only minor instantaneous variations in the impedance occur. However, when the FZ bit in the configuration register is set, then the input termination and output impedance will be “frozen” at their current values. If the IM bit in the configuration register is set, then the output impedance will have a nominal value that is not dependent on the value of the resistor connected to the ZQ pin. In this mode, the ZQ pin is ignored by the Low Latency DRAM-III, and the output impedances will not be PVT compensated

Impedance Test Parameters

Parameter	Symbol	MIN.	NORM.	MAX.	Unit
Output HIGH voltage with forced I_{oh} = -($V_{DD}Q$ -0.85 V)/ Z_{oh}	V_{oh}	0.723	0.85	0.978	V
Output HIGH voltage with forced I_{oh} = -($V_{DD}Q$ -0.7 V) / Z_{oh}	V_{oh}	0.595	0.7	0.805	V
Output LOW voltage with forced I_{ol} = 0.7 V / Z_{ol}	V_{ol}	0.595	0.7	0.805	V
Output LOW voltage with forced I_{ol} = 0.55 V / Z_{ol}	V_{ol}	0.468	0.55	0.633	V

2. Operation

2.1 Interface Overview

The primary Low Latency DRAM-III interface consists of a unidirectional command and address bus and a bidirectional data bus. This type of data bus is often referred to as common I/O or CIO. **Pin Identification** contains the list of pins on the Low Latency DRAM-III.

The command bus is a single data rate (SDR) bus consisting of CS#, WE#, and REF#. The μPD480114xx have a double data rate (DDR) address bus consisting of multiplexed A0-A6 in burst length 4 mode. Both the command bus and address bus are clocked by the differential clock pair CK and CK#. READ and WRITE commands can be issued at a rate of one every 2 cycles of CK in burst length 4 mode.

The data interface is a double-rate (DDR) interface that transfers 36 bits of data [Note] on each clock edge for 36-bit parts and 18 bits of data on each clock edge for 18-bit parts. The data interface also includes 4 data inversion pins. In addition to 36 data bits, the inputs to the Low Latency DRAM-III include a DDR data mask, DM, and two differential clock pairs, DK0-DK1 and DK0#-DK1#. The Low Latency DRAM-III outputs two differential clock pairs, QK0-QK1 and QK0#-QK1# that are associated with read data, and a data valid signal, QVLD. Because the data bus is bidirectional, idle cycles are required to implement data bus turn-around as described in **2.7 Data bus turn-around**.

Note For parts with 18-bit data bus, all references in this section should refer to DQ0-DQ17 and DINV0- DINV1 unless otherwise noted. DQ0-DQn is used to represent DQ0-DQ35 or DQ0-DQ17 for 36-bit and 18-bit parts, respectively, and DINV0-DINVm is used to represent either DINV0-DINV3 or DINV0-DINV1 for 36-bit and 18-bit parts.

2.2 Clocking

There are three groups of clock signals: CK/CK#, DK0-DK1/DK0#-DK1#, and QK0-QK1/QK0#-QK1#.
The CK/CK# clock is associated with the address and command pins: A0-A6, CS#, WE#, and REF#. At the Low Latency DRAM-III pins, the CK/CK# transitions are nominally centered with respect to address and command signal transitions.
The DK0-DK1/DK0#-DK1# clocks are associated with write data. DK0/DK0# is used as a source-centered clock for the double data rate DQ0-DQ17, DINV0-DINV1, and DM pins. DK1/DK1# is used as a source-centered clock for the double data rate DQ18-DQ35 and DINV2-DINV3 pins.
The DK0-DK1/DK0#-DK1# clocks must meet the specified t_{CKDK} skew with respect to the CK/CK# clock in order to ensure proper timing relationship between command and data cycles and to enable proper data bus turn-around.
The QK0-QK1/QK0#-QK1# clocks are associated with read data. At the Low Latency DRAM-III pins, and for x36 devices, QK0/QK0# must be source-synchronous with the read data DQ0-DQ17, DINV0-DINV1, and QVLD pins. Similarly, for x36 devices, QK1/QK1# is used as a source-synchronous clock for the read data DQ18-DQ35 and DINV2-DINV3 pins.
For x18 devices, QK0/QK0# must be source-synchronous with DQ0-DQ8, DINV0, and QVLD. Similarly, for x18 devices, QK1/QK1# must be source-synchronous with DQ9-DQ17 and DINV1.
The QK0-QK1/QK0#-QK1# clocks must meet the specified t_{CKQK} skew with respect to the CK/CK# clock in order to ensure proper timing relationship between command and data cycles and to enable proper data bus turn-around.

2.3 Address bus

In Burst of 4 mode two clock cycles are required to load the multiplexed address. In DDR Address mode address inputs are captured by the RAM in two beats per cycle. Three of the bits in the address field select which of the 8 banks in the RAM will be accessed. Note that a 4th bank address bit has been identified anticipating that a 16 bank version of the RAM might someday reach the market. The bit functions as an ordinary address bit in the devices described in this data sheet.

Table 2-1 Address Bit Encoding

Command	Device Width	Beat	A6 Note1	A5	A4	A3	A2	A1	A0
READ or WRITE	x36	0	X	Address		Address Note2	Bank		
		1	X	Address					
		2	X	Address					
		3	X	X Note1	Address				
READ or WRITE	x18	0	X	Address		Address Note2	Bank		
		1	X	Address					
		2	X	Address					
		3	X	Address					
AUTO REFRESH	ANY	0	X	X	X	X	Bank		

Note 1. A6 is reserved for future expansion. For smaller capacity devices, the value is a don't care, but for devices of the designated capacity or larger, the value will be used.

2. Address bit A3 in beat zero is used as an address bit in the current devices, but may be used as a bank address bit in future generations of the part.

2.4 Command encoding

The Low Latency DRAM-III supports five types of command cycles as show in **Table 2-3**.

The NOP command must be used on any cycle where no other commands are requested.

The READ command is used to initiate a burst read from the Low Latency DRAM-III.

The WRITE command is used to initiate a burst write from the Low Latency DRAM-III.

The AUTO REFRESH command is used to initiate a refresh operation on a particular bank of the memory.

The OVERLAPPED REFRESH command is used to initiate a refresh operation, but may be overlapped with other commands.

The MRS command is used to configure the Low Latency DRAM-III following a reset.

Because the overlapped refresh feature can be enabled or disabled, the command decoding and it's associated state diagram have two different forms. **Table 2-2** and **Figure 2-1** show the command encoding for the case when the overlapped refresh feature is disabled. **Figure 2-1** only shows the state diagram for the command decoder; there may be many other states internal to the device.

Because READ and WRITE commands require two cycles to fully transfer their associated address in burst length 4 mode and because the OVERLAPPED REFRESH command may be specified simultaneously with other commands, the command decoder and its state diagram are more complex when the overlapped refresh feature is enabled.. The states associated with the command decoder and how command cycles are interpreted is described in **Table 2-3** and **Figure 2-2**(again, the state diagram only shows the states for the command decoder, not other internal states of the device).

Table 2-2 Command Encoding (Overlapped Refresh Disabled)

State	Command	CS#	WE#	REF#	LBK#	RST#	Length (cycles)	Description
IDLE	NOP	1	-	-	1	1	1	No operation
	READ	0	1	1	1	1	2	Read
	WRITE	0	0	1	1	1	2	Write
	AUTO REFRESH	0	1	0	1	1	1	Auto refresh
	MRS	0	0	0	1	1	2	Mode register set
RD, WR	NOP	1	-	-	1	1	-	No operation
MRS	NOP	1	-	-	1	1	-	No operation
	LOOPBACK	-	-	-	0	1	-	Address/control loopback
	RESET	-	-	-	-	0	-	Reset

Figure 2-1 Command Decode State Diagram (Overlapped Refresh Disabled)

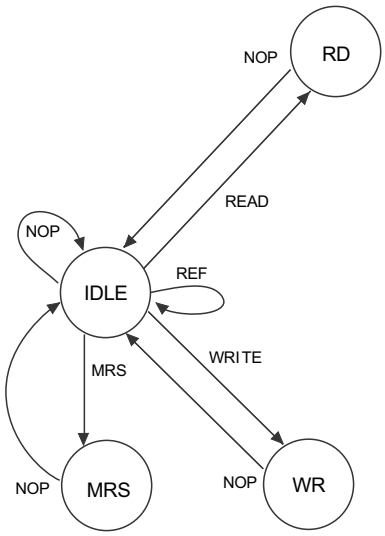
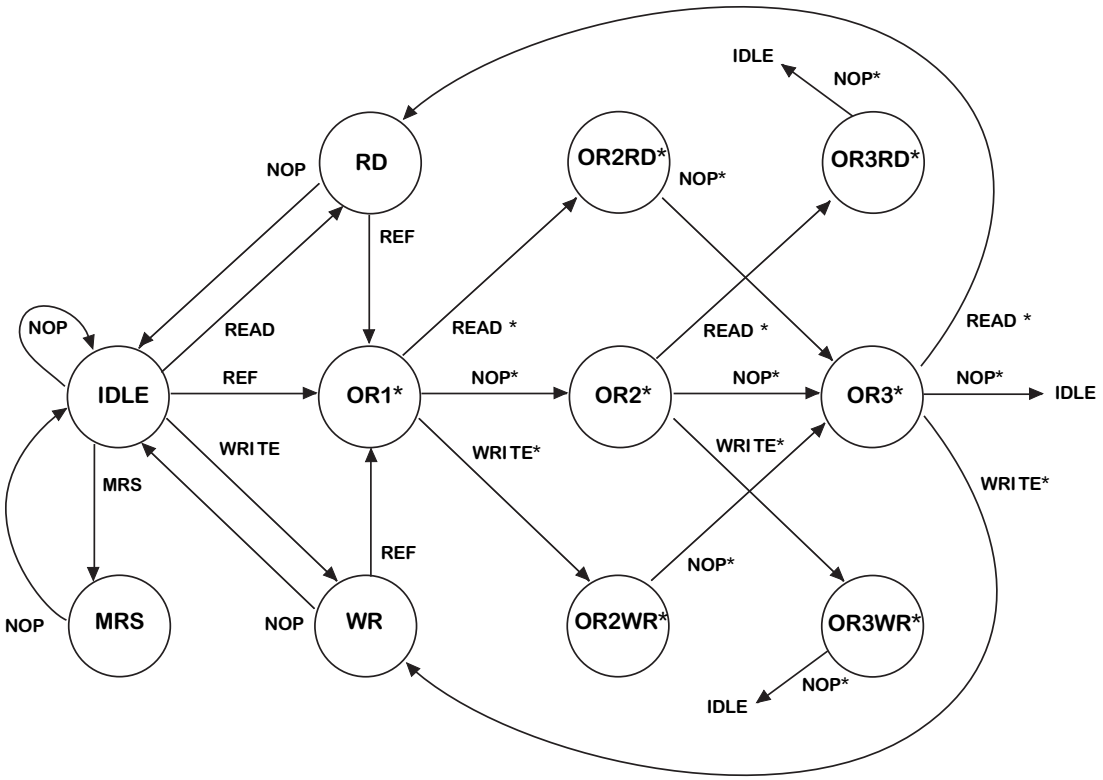


Table 2-3 Command Encoding (Overlapped Refresh Enabled)

State	Command	CS#	WE#	REF#	LBK#	RST#	Length (cycles)	Description
IDLE	NOP	1	-	-	1	1	1	No operation
	READ	0	1	1	1	1	2	Read
	WRITE	0	0	1	1	1	2	Write
	OVERLAPPED REFRESH	0	1	0	1	1	4	Overlapped refresh
	MRS	0	0	0	1	1	2	Mode register set
RD, WR	NOP	1	-	-	1	1	-	No operation
	OVERLAPPED REFRESH	0	1	0	1	1	4	Overlapped refresh
OR1, OR2, OR3	NOP	1	-	- Note	1	1	-	No operation
	READ Note	0	1	- Note	1	1	2	Read (overlapped)
	WRITE Note	0	0	- Note	1	1	2	Write (overlapped)
OR2RD, OR3RD, OR2WR, OR3WR	NOP	1	-	- Note	1	1	-	No operation
MRS	NOP	1	-	-	1	1	-	No operation
	LOOPBACK	-	-	-	0	1	-	Address/control loopback
	RESET	-	-	-	-	0	-	Reset

Note These indicate that the value of the REF# pin is ignored for the purpose of command decoding (the pin is used for conveying bank number during this cycle).

Figure 2-2 Command Decode State Diagram (Overlapped Refresh Enabled)



Note: states and transitions marked with an asterisk (*) indicate that the value of the REFN pin should be ignored, so that neither a REFRESH, nor MRS command will be recognized in that state

2.5 Data mask

The DM pin is used during write cycles to indicate that the corresponding data are to be masked off from writing to the memory. The value of the DM pin is sampled on both edges of DK0/DK0#, and corresponds to the data sampled on that same edge of either DK0/DK0# or DK1/DK1#.

When the DM pin has a logic 0 value, the data will be written to the memory. When the DM pin has a logic 1 value, the data will be ignored and no update to the corresponding memory data will be made.

The value of the DM pin is ignored in all other circumstances. Thus, driving a constant logic 0 to the DM pin can be used in systems where all data cycles in a burst result in writes to the memory.

When the Auto-DM Function (ADM) bit is set via an MRS command, the value of the DM pin is ignored and the device will behave as if it were a logic 0 on only the clock edge specified by the value of the DMP field.

2.6 Data inversion

In order to reduce simultaneous switch noise, I/O current and average I/O power, the Low Latency DRAM-III provides the ability to invert all data pins. Because the nominal design for Low Latency DRAM-III I/O signals is high-side termination to $V_{DD}Q$, signals driven to a logic high state will consume less power than those in a logic low state.

The DINVm-DINV0 pins indicate whether corresponding DQn-DQ0 pins, in groups of nine, represent the true logic value or an inverted logic value. With the ability to invert DQn-DQ0 pins in groups of nine, each group is guaranteed to be driving no more than five pins low on any given cycle. As a result, no more than five pins in each group can switch in the same direction during each bit time, reducing simultaneous switching noise effects.

When data inversion is enabled (DI=1) and a DINV pin is a logic 1, the corresponding DQ pins have been inverted.

When data inversion is disabled (DI=0) then the Atris device will ignore the value of the DINV pins for write data and will drive DINV pins to logic 1 for read data; however, in such a case, the DQ pins are not inverted, regardless of the values of the DINV pins.

2.7 Data bus turn-around

Because the DQn-DQ0 and DINVm-DINV0 pins are bidirectional, care must be taken to ensure that the Low Latency DRAM-III and the system chip connected to it do not drive these pins simultaneously. In order to guarantee this, a rapid DQ and DINV turn-off time is required. The actual bus turn-around time is dependent on many system parameters, including BL, RL, WL, pre-amble, post-amble, controller I/O timing, DRAM I/O timing, PCB delays; and the system must ensure that neither the Low Latency DRAM-III, nor the system chip is driving the bus during that time. This is accomplished by inserting a sufficient number of NOP commands between each READ-to-WRITE command transition and between each WRITE-to-READ transition. Additional NOP commands may be required to allow settling of the bus in order to insure no adverse effect on I/O timing.

Note that a REFRESH command can be used in place of a NOP command to effect the insertion of an idle cycle on the data bus.

2.8 Command cycles

A command to the Low Latency DRAM-III is initiated by driving the CS# pin low at the rising edge of CK and simultaneously driving the WE#, REF#, and A0-A6 pins to the appropriate state corresponding to the command.

READ and WRITE commands each require 2 clocks to send the full command in burst length 4 mode, due to the multiplexed nature of Address loading. The NOP and AUTO REFRESH commands are each a single cycle in length. The OVERLAPPED REFRESH command is four cycles in length.

2.9 Write data cycles

DQ0-DQn, DINV0-DINVm, and DM associated with a WRITE command are received by the Low Latency DRAM-III in a DDR burst, starting on a rising edge of DK that is offset WL clock cycles from rising edge of the CK signal corresponding to the first cycle that the WRITE command was initiated. This delay of WL cycles is intended to ensure that the write data are not driven at the same time that data from a previous READ command are being driven from the Low Latency DRAM-III.

2.10 Read data cycles

DQ0-DQn and DINV0-DINVm associated with a READ command are driven by the Low Latency DRAM-III in a DDR burst by the Low Latency DRAM-III RL clock cycles from the rising edge of the CK signal corresponding to the first cycle that the READ command was initiated. This delay of RL cycles is equal to the delay required for the internal logic and memory within the Low Latency DRAM-III to read data and make it available on the bus.

2.11 READ and WRITE command protocol

Figure 2-3 through **Figure 2-4** show the READ and WRITE command sequences.

Figure 2-3 READ Command Sequence

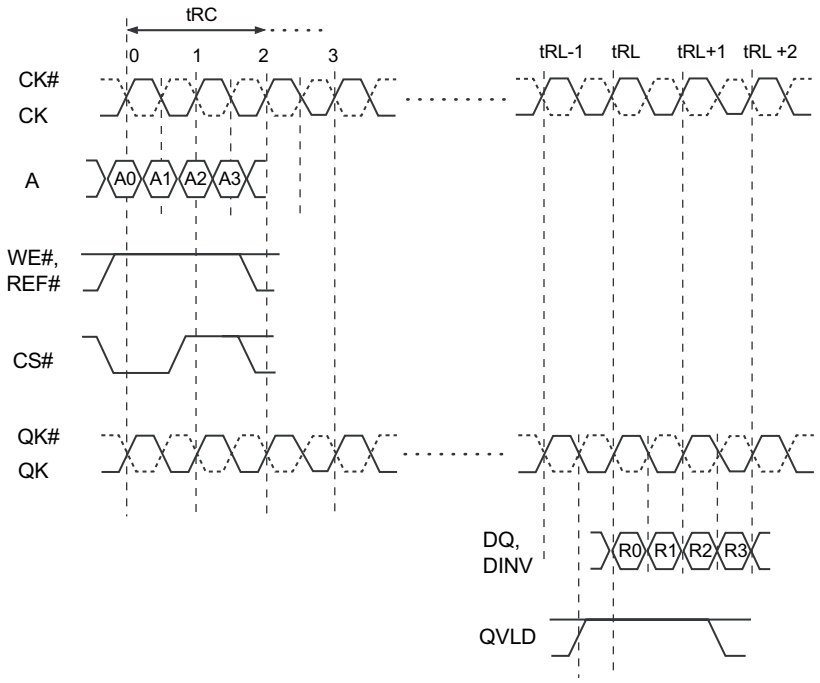


Figure 2-4 WRITE Command Sequence

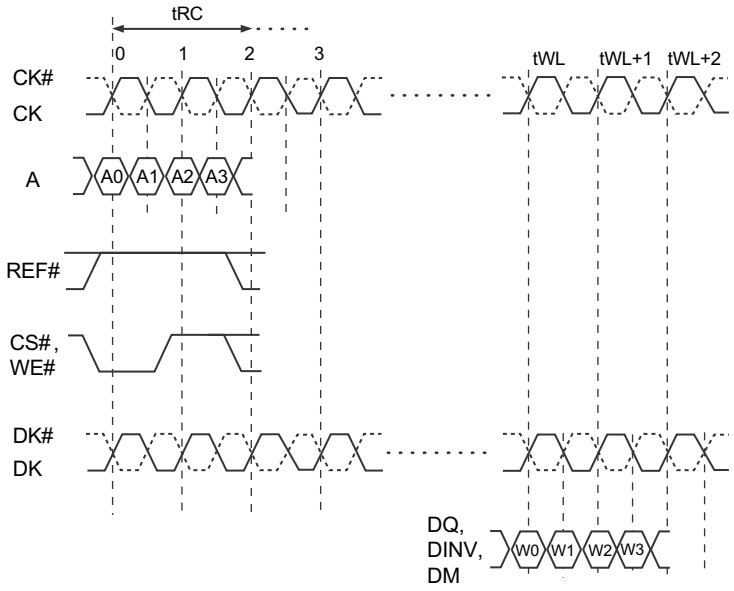


Figure 2-5 shows DDR Address examples of a sequence of 2 READ, 2 WRITE, and 2 READ commands, with the following configuration:

Burst length 4

Speed Config 5: t_{RC}=11, t_{RL}=16, t_{WL}=17

Data inversion is enabled

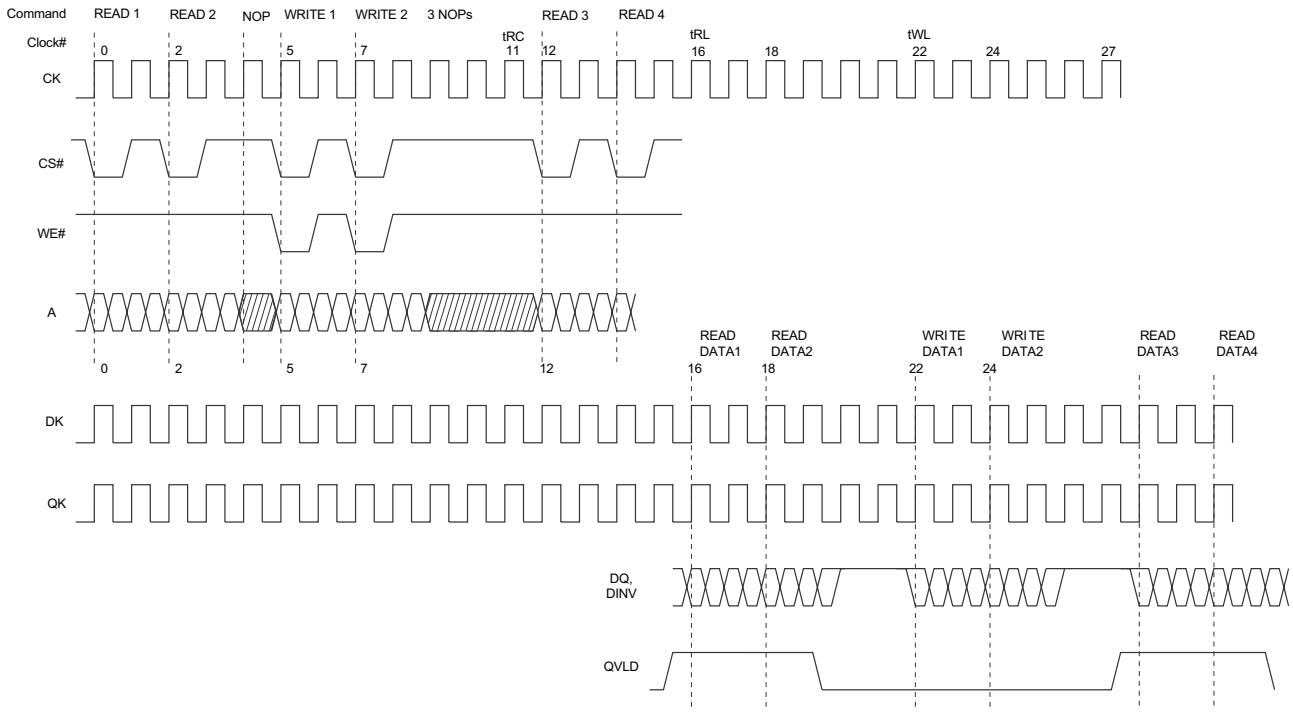
Some observations of this sequence are:

A NOP is inserted between READ2 and WRITE1 to allow for read-to-write bus turn-around

3 NOPs are inserted between WRITE2 and READ3 to allow for write-to-read bus turn-around

Because t_{RC} is 11, READ3 may access the same bank as READ1; however, none of READ2, WRITE1, or WRITE2 may access the same bank as READ1

Figure 2-5 READ/WRITE/READ Command Sequence (Speed Config 5, t_{RC}=11, t_{RL}=16, t_{WL}=17, DI=1)



2.12 Automatic Refresh

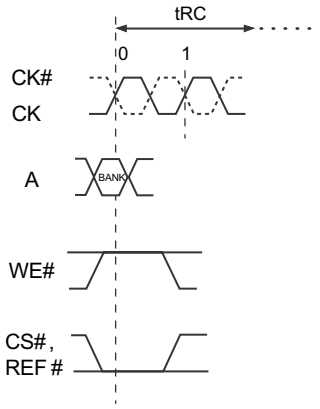
Refresh cycles of the internal memory are initiated via the AUTO REFRESH command. Each refresh command causes a single refresh cycle to occur on the bank specified in the command.

The minimum data retention time is 2 ms over the temperature range specified in **1. Electrical Specifications**, and there are 16384 words in each bank. Therefore, each bank must receive 16384 refresh commands every 2 ms in order to ensure proper data retention.

This means that a refresh command must be received at an average rate of one every 15.3 ns. At a frequency of 800 MHz, this represents 8.2% of the usable bandwidth to the Low Latency DRAM-III.

The refresh command waveforms are shown in **Figure 2-6**. This refresh command is only supported if overlapped refresh is not configured (see **2.13 Overlapped refresh commands**).

Figure 2-6 Automatic Refresh Command Sequence



2.13 Overlapped refresh commands

Refresh commands may be overlapped with READ, WRITE, or NOP commands so that it is possible to design a system that does not require any bus bandwidth to be consumed due to refresh. During the MRS command, overlapped refresh may be enabled.

Once configured for overlapped refresh via an MRS command, the REF# pin is used to both initiate the refresh command as well as to communicate the bank to be refreshed. This is accomplished by indicating one bit of bank address on each rising edge of the CK clock, following the initial assertion of the REF# pin. The AUTO REFRESH command is not supported when the Low Latency DRAM-III is configured for overlapped refresh mode.

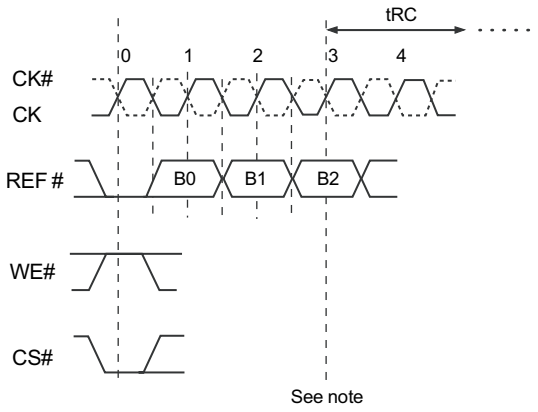
The overlapped refresh command cannot be initiated on the same cycle as a READ or WRITE command; this avoids the potential ambiguity of an overlapped refresh and WRITE command being interpreted as an MRS command. In general, overlapped refresh commands are expected to be initiated one cycle out of phase with READ and WRITE commands.

In addition, once the overlapped refresh command has begun, the state of the REF# pin is ignored for the purposes of command decoding, in order to allow subsequent READ or WRITE commands to begin while the refresh bank address is being specified on the REF# pin.

Figure 2-7 shows the OVERLAPPED REFRESH command sequence.

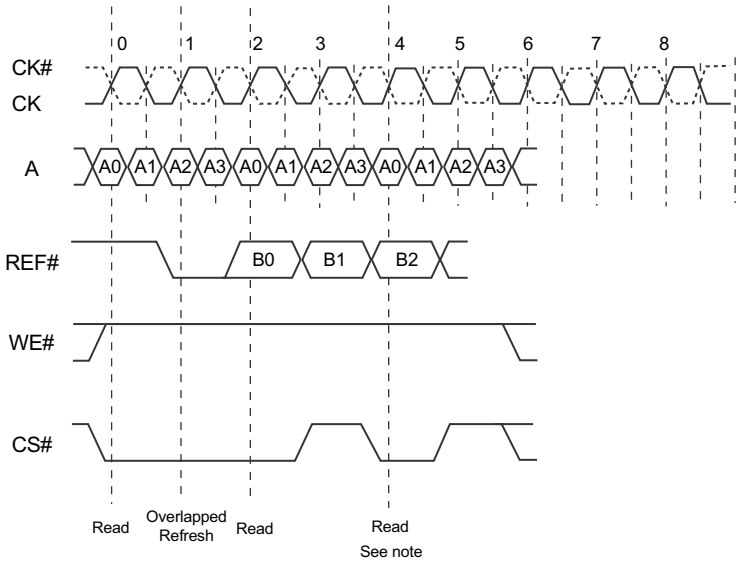
An example of refresh being overlapped with READ commands is shown in **Figure 2-8**.

Figure 2-7 Overlapped Refresh Command Sequence



Note t_{RC} for overlapped refresh begins 3 cycles after the start of the command.

Figure 2-8 Overlapped Refresh with READ Commands



Note t_{RC} for overlapped refresh begins 3 cycles after the start of the command.

2.14 Clam-shell support

In order to support clam-shell mounting on the board, the pin-out of the Low Latency DRAM-III is designed so that most pins that will be interchanged via mirroring are functionally interchangeable. A few pins require their function to be swapped, however. The MF pin causes the pin assignment to be modified to effect those pin swaps. In order to support proper signal integrity, package trace lengths for mirrored pins are matched to within +/- 0.1mm. **Table2-4** shows the pins that are mirrored by the MF pin.

Due to the mirroring of A5 and A6, all devices are required to include an I/O cell on A6 in order to support the mirror function. For lower capacity devices, the A6 pin would remain DNU, $V_{DD}Q$ from a memory controller standpoint, so the system need not actively drive this functionally unused pin.

A3 and A4 are mirrored to support future devices that may use A3 as an additional bank select bit.

All of A0 through A5 must be mirrored in order for MRS commands to be interpreted correctly.

Table 2-4 Pins Affected by MF Pin

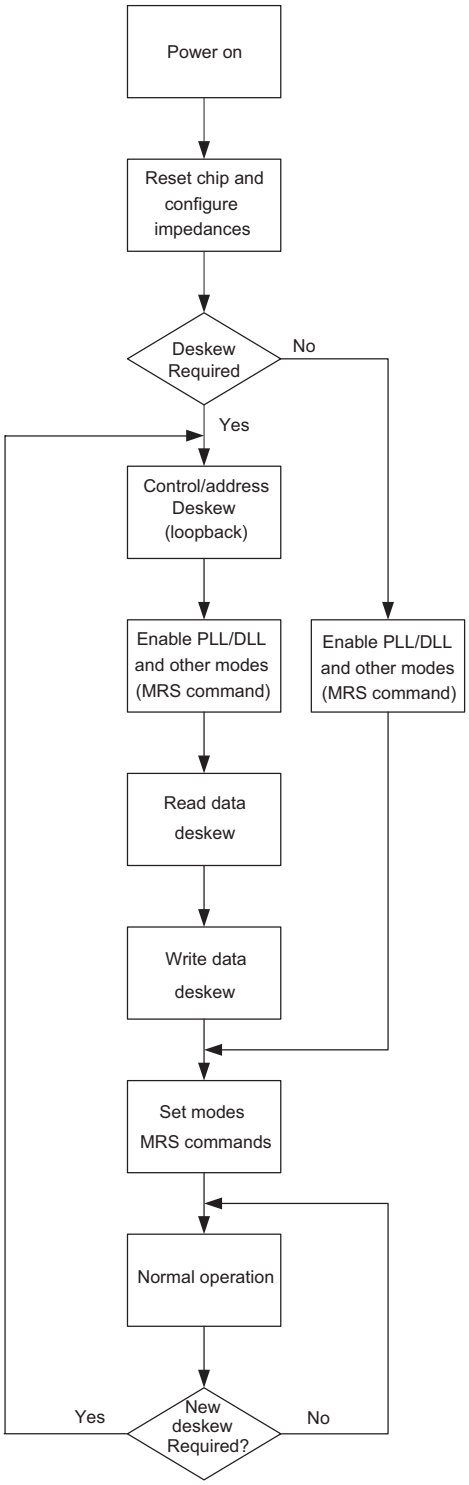
Pin	MF=0	MF=1
N4	A0	A1
N10	A1	A0
L4	A4	A3
L10	A3	A4
M5	A2	REF#
M9	REF#	A2
L2	CS#	WE#
L12	WE#	CS#
H10	A5	A6
H4	A6	A5
H2	RST#	DM
H12	DM	RST#

3. Initialization

Prior to functional use, the Low Latency DRAM-III must be initialized and configured. The steps described in this chapter will ensure that the internal logic of the Low Latency DRAM-III has been properly reset and that the functional timing parameters of the chip have been configured.

Figure 3-1 shows the overall initialization sequence required by the Low Latency DRAM-III. An example of an initialization sequence, showing each of the different phases, is shown in **Figure 3-7**.

Figure 3-1 Initialization Flow



3.1 Power-on

1. There are no restrictions on the sequence of applying the V_{DD}, V_{EXT}, and $V_{DD}Q$ power supplies as long as maintaining RST# = Low and fix MF input state before and during any of the power supplies ramp up.

2. In case when RST# can not be asserted Low and fixed MF input state before and during any of the power supplies ramp up, make sure to ramp up following manners.
   (1) Ramp up VDD and VEXT
   (no ramp up sequence restriction on VDD and VEXT)
   (2) Ramp up VDDQ and VREF following to the VDD and VEXT
   (no ramp up sequence restriction on VDDQ and VREF)
   (3) Make sure to assert RST# for tRSS specified period before initiating any operations

Figure 3-2 Power-on 1

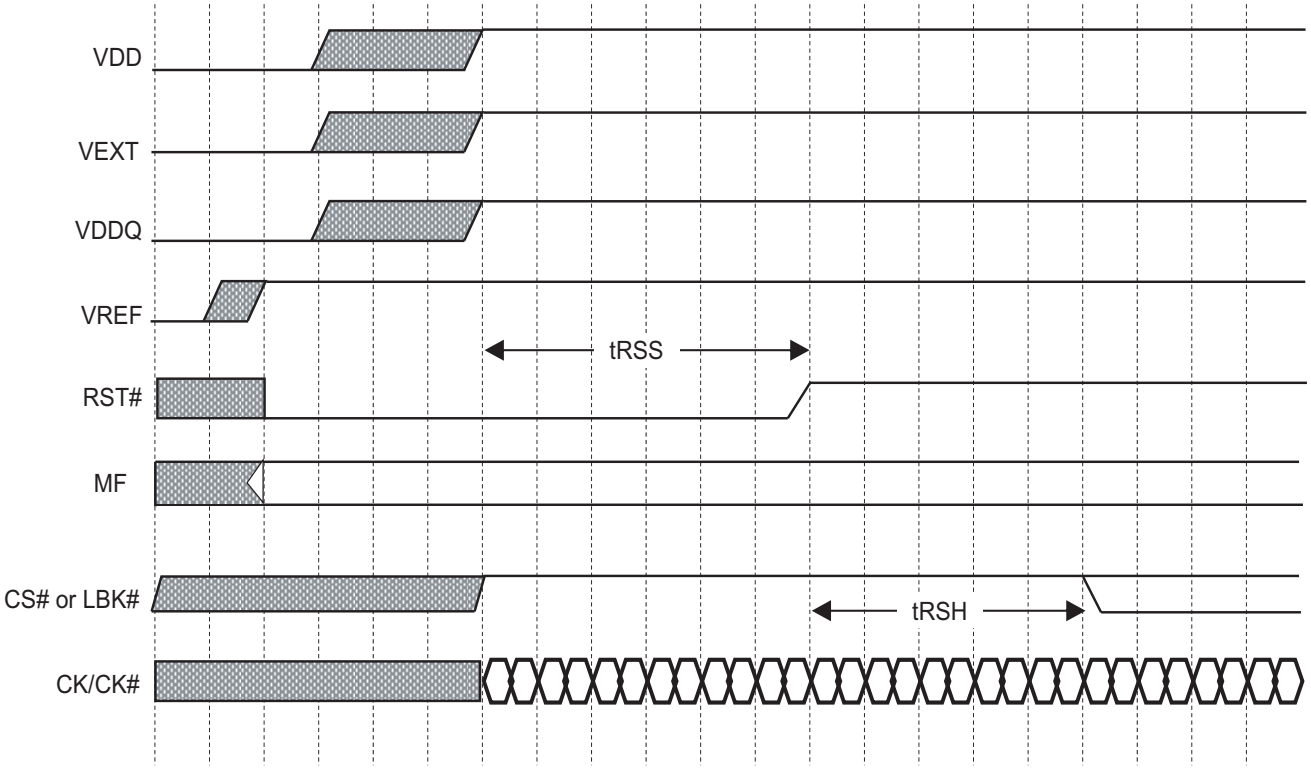
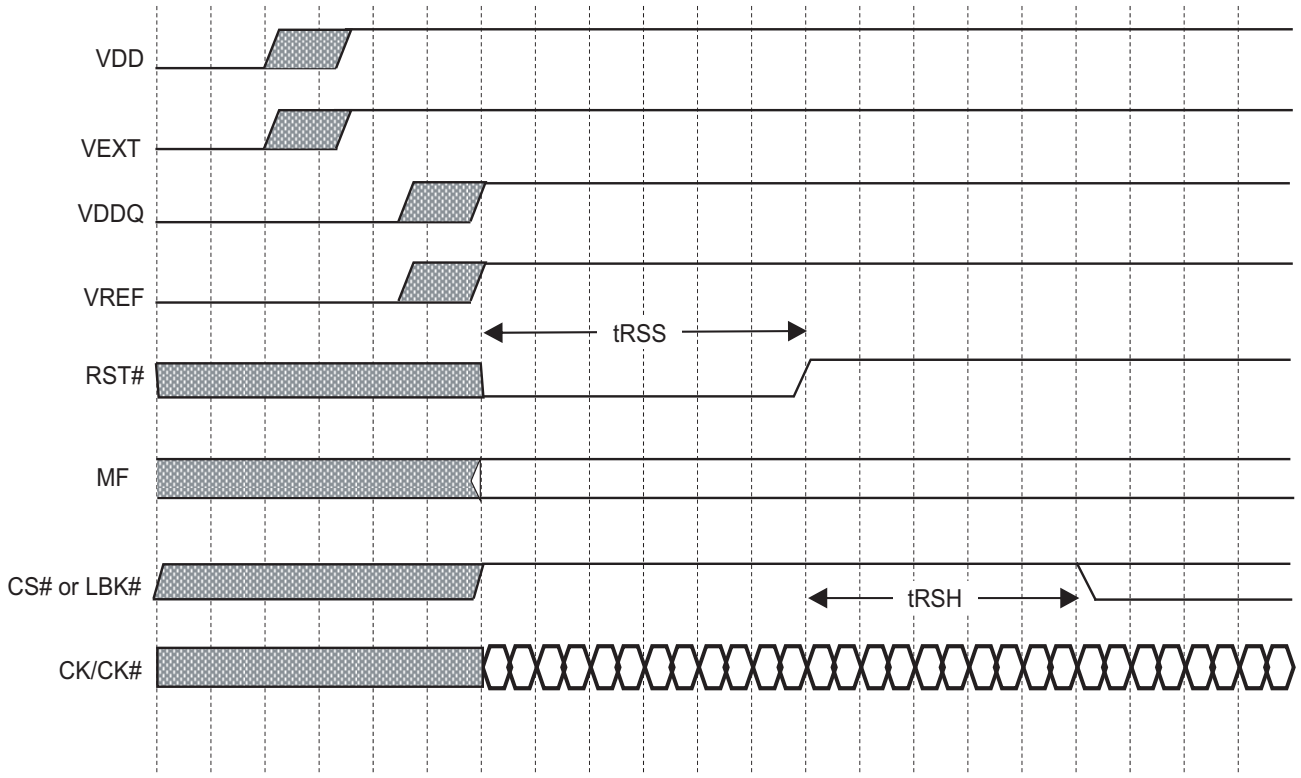


Figure 3-3 Power-on 2



3.2 Reset

Before the Low Latency DRAM-III can be configured, it must be properly reset, to ensure that the Low Latency DRAM-III is in a known and functional state, regardless of any power on anomalies and power supply ramp rates. Reset requires the assertion of the RST# pin for at least 200 μs, during which time the device logic is reset to a known state, and the I/O impedances are programmed as described in **3.3 Initial impedance settings**.

The contents of memory are not guaranteed to be retained when the chip is reset.

3.3 Initial impedance settings

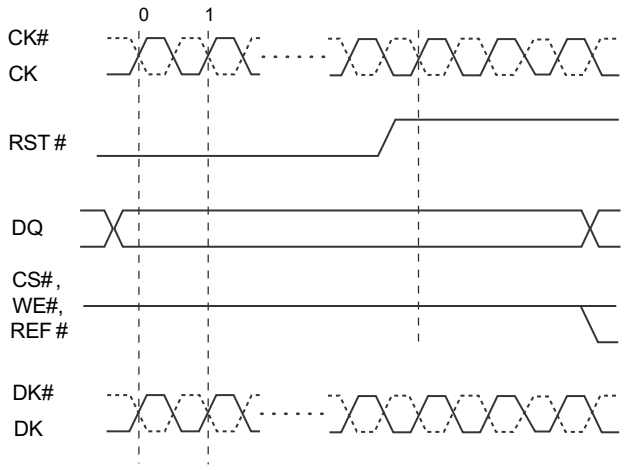
When the RST# pin is deasserted, the value of specific DQ pins is used to configure the input termination and output impedance as shown in **Table 3-1**. The meaning of the bits is the same as the corresponding bits described in **3.5 Configuration**, although their positions in the DQ pins are unrelated to their positions in the corresponding MRS registers. While RST# is asserted, the impedance values are continuously updated based on the values of the DQ pins and on the sampled value of the ZQ impedance programming pin. On the rising edge of RST#, the values will be latched into the device and stored in the appropriate positions in the MRS registers. **Figure 3-4** shows the waveforms associated with this function.

Note that the DINV pins are ignored during reset time and the values of the DQ pins are considered to never be inverted during this time.

Table 3-1 Reset Impedance Control Assignments

Pins	U12	T11	U4	R12	T5	P13	R4	P11	P5	B12	C11	B4	D12	C5	E13	D4	E11	E5
DQ (x18)	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQ (x36)	26	25	24	23	22	21	20	19	18	8	7	6	5	4	3	2	1	0
Reset Reg MSB → LSB	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cell ID			KD		KU		CD		CU		DD		DU		ODT	QD	QU	IM

Figure 3-4 Reset Sequence



3.4 Per-bit de-skew training sequence

The Low Latency DRAM-III device provides support that allows a memory controller to de-skew signals for high-speed operation. If per-bit de-skew is desired, the memory controller must provide the actual de-skew functionality. Per-pin de-skew is normally performed after deassertion of the RST# pin, but may be performed at any time, without affecting the contents of the memory within the device. Furthermore, resetting the device does not necessarily affect the skew characteristics of the device pins; therefore, a reset of the device does not necessarily require repeating the de-skew training sequence that was previously performed.

Per-pin de-skew training is anticipated to be implemented in three steps:

De-skew of the control, address, and clock pins: A0-A6, CS#, WE#, REF#, and DK0-DK1 with respect to CK

De-skew of the read path: DQ0-DQn, DINV0- DINVm and QVLD with respect to QK0-QK1

De-skew of the write path: DQ0-DQn, DINV0- DINVm and DM with respect to DK0-DK1

The first phase, de-skew of the control and related pins, requires support from the device by driving the LBK# pin to a logic 0. When the LBK# pin is a logic 0, the DK0-DK1, CS#, WE#, REF#, and A0-A6 pins are looped back to the various DQ and DINV pins. All pins are sampled by the CK clock, including DK0-DK1. The specific mapping of input pins to output pins during loopback mode is shown in **Table 3-2**.

Table 3-2 Control/Address Pin Mapping When LBK#=0

		x36 part			x18 part		
		Input		Output	Input		Output
Input Pin	Output Pin	MF=0	MF=1		MF=0	MF=1	
H4	E5	A6 (DNU, $V_{DD}Q$)	A5	DQ0	A6 (DNU, $V_{DD}Q$)	A5	DQ0
J1, K1	E11	DK0, DK0#	DK0, DK0#	DQ1	DK0, DK0#	DK0, DK0#	DQ1
L4	P5	A4	A3	DQ18	A4	A3	DQ9
L2	R4	CS#	WE#	DQ20	CS#	WE#	DQ11
M5	T5	A2	REF#	DQ22	A2	REF#	DQ13
N4	U4	A0	A1	DQ24	A0	A1	DQ15
H10	E13	A5	A6 (DNU, $V_{DD}Q$)	DQ3	A5	A6 (DNU, $V_{DD}Q$)	DQ3
J11, K11	E3	DK1, DK1#	DK1, DK1#	DQ14	DNU, V_{SS}	DNU, V_{SS}	DNU, V_{SS}
L10	P11	A3	A4	DQ19	A3	A4	DQ10
L12	P13	WE#	CS#	DQ21	WE#	CS#	DQ12
M9	T11	REF#	A2	DQ25	REF#	A2	DQ16
N10	U12	A1	A0	DQ26	A1	A0	DQ17

Notes:

DK0, DK0# and DK1, DK1# have differential receivers, so the output of the receiver is used as signal being looped back.

For each pin that is looped back, the input pin is sampled on both the rising edge and falling edges of the corresponding input clock. The value output on the rising edge of the corresponding output clock will be the value that was sampled on the rising edge of the input clock. The value output on the falling edge of the corresponding output clock will be the *inverted* value that was sampled on the falling edge of the input clock. Data inversion is *not used* during loopback mode and the value of the corresponding MRS bits are ignored.

The delay from input pins to DQ/DINV output pins, when loopback mode is enabled, is 5 cycles of CK.

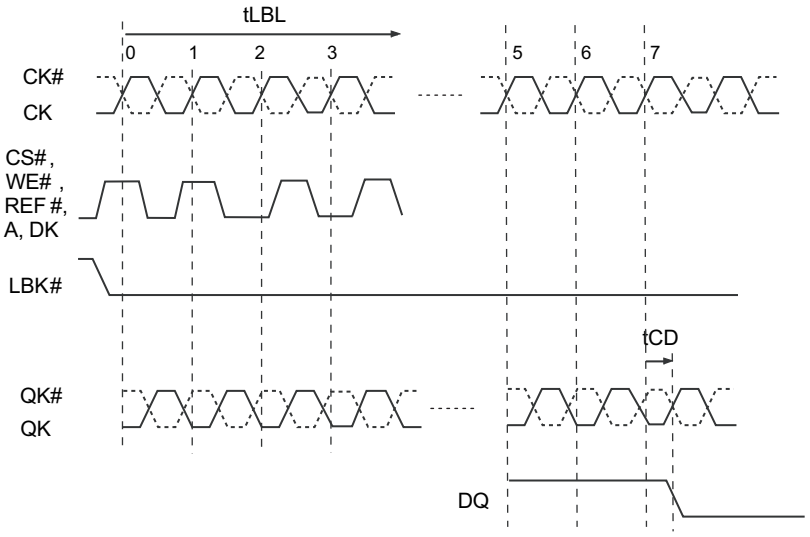
In burst length 4 mode , while LBK# pin is a logic 0 , the DQ/DINV output pins corresponding to unused input pins (see **Table 3-2**) will still meet the AC timing specification (See **Interface AC Parameters**) , but they may have arbitrary logic state and may or may not have a constant logic value.

While the LBK# pin is a logic 0, the device will ignore any apparent commands being presented on the CS#, WE#, and REF# pins and will perform self refresh operations to prevent loss of data during extended periods of de-skew training. In order to ensure that commands are not inadvertently received during entry and exit from de-skew training, no commands may be sent to the device for a period of 16 cycles of CK prior to the LBK# pin being driven to 0, nor for 16 cycles after the LBK# pin is returned to a logic 1. Also, no valid input signals for looped back must be inserted for 16 cycles after LBK# pin being driven to 0 when device just enters into loopback mode.

While LBK# is asserted, the on-chip PLL is ignored; therefore the phase of the QK output clock will be undefined with respect to the CK input clock. However, the QK to DQ timing will still meet its specifications. Note that the PLL will remain enabled or disabled, per its state prior to LBK# being asserted, and after LBK# is deasserted.

An example of a loopback sequence is show in **Figure 3-5**.

Figure 3-5 Loopback De-skew Training Sequence



Parameter	Symbol	-FH12	-FH12	Units
Loopback Latency	tLBL	5	5	Cycle
Maximum CK to QK/DQ Output Delay in Loopback Mode	tCD	5	5	ns

Following de-skew of the control, address, and DK pins, the memory controller drives the LBK# pin to a logic 1, then will likely perform read data and write data de-skew training.
Prior to beginning read path de-skew, the memory controller should issue an MRS command to the Low Latency DRAM-III device to enable the PLL. After the PLL is enabled, the timing of the QK, DQ outputs, and QVLD will be unspecified for a period of t_{PLL}. The MRS command is described in **3.5 Configuration**. While the PLL is stabilizing, refresh commands must continue to be issued to the device in order to ensure proper retention of data.

Read data de-skew requires that a training pattern be written to Low Latency DRAM-III memory. Complex data patterns can be written to the Low Latency DRAM-III memory using the non-de-skewed DQ signals and the auto-DM functions. Auto-DM functions are enabled through MRS, as described in **3.5 Configuration**.
Read data de-skew can be performed by using the de-skewed control and related pins, including the DK pin, and non-switching DQ and DINV pins to write 36-bit values to memory locations in the device. Because the data are held at constant values, the auto-DM modes of the device are used to specify which 36-bit beat (or 18-bit beat for x18 devices) of data on the bus is to be written to the memory. Once written to the memory, these data can then be read out using standard BL4 (or BL2, depending on the configured burst length) READ commands to effect any desired pattern on the DQ bus. This permits the system to de-skew the DQ, DINV, and QVLD signals with respect to the QK clocks.
Write data de-skew can be performed by issuing WRITE commands to the device, then using the de-skewed read bus to determine whether or not data were correctly received by the device. This permits the system to de-skew the DQ, DINV, and DM signals with respect to the DK clocks.

3.5 Configuration

The MRS command is used to configure the Low Latency DRAM-III. Configuration is used to specify the following parameters:
Address Mode
The Address Mode of Low Latency DRAM-III devices from some vendors may be electrically configurable. The default Address Mode may vary from vendor-to-vendor as well. Therefore, systems must configure the desired Address Mode prior to issuing READ or WRITE commands

Mode select for READ latency, WRITE latency, and t_{RC}
The version of the Low Latency DRAM-III covered by this specification only supports modes 4 and 5

Select driver pull-up impedance of 1/4 or 1/6 of reference resistor (default ¼)
Select driver pull-down impedance of 1/4 or 1/6 reference resistor (default 1/6)
Select DQ, DINV, DM, DK, DKN, CK, CK#, RST# terminator pull-up impedance of OFF, 1x, 1/2, or 1/4 of reference resistor (default 1/4)
Select DQ, DINV, DM, DK, DKN, CK, CK#, RST# terminator pull-down impedance of OFF, 1x, 1/2, or 1/4 of reference resistor (default OFF)
Select CS#, WE#, REF#, A, LBK#, TCK, TDI, TMS terminator pull-up impedance of OFF, 1x, 1/2, or 1/4 of reference resistor (default 1/4)
Select CS#, WE#, REF#, A, LBK#, TCK, TDI, TMS terminator pull-down impedance of OFF, 1x, 1/2, or 1/4 of reference resistor (default OFF)

Enable/freeze dynamic PVT compensation (default enabled)
Enable/disable PLL (default disabled)
Enable/disable read/write data inversion (default disabled)

Refresh mode (default AUTO REFRESH)

Select auto-DM modes (default disabled)

The MRS command allows the configuration of one of eight different registers to be configured using SDR timing on the address pins. The MRS command waveforms are shown in **Figure 3-6** and the values of the MRS registers are described in **Table 3-3** through **Table 3-6**. Because an MRS command may change values that significantly affect the behavior of the device, no other commands should be issued to the device for a period of t_{MRD} clock cycles following the MRS command.

MRS commands use the address pins specified in **Table 3-3**. The actual pins used depend on the value of the mirror function (MF) pin.

Table 3-3 MRS Configuration Register Bit Assignments

	Beat 0							**Beat 2**						
Pins (MF=0)	H4	H10	L4	L10	M5	N10	N4	H4	H10	L4	L10	M5	N10	N4
Pins (MF=1)	H10	H4	L10	L4	M9	N4	N10	H10	H4	L10	L4	M9	N4	N10
Address	A6	A5	A4	A3	A2	A1	A0	A6	A5	A4	A3	A2	A1	A0
Mode Register LSB→MSB					Mode Reg #									
Active	X	Configuration			0	0	0	X	0	DI	FZ	RM	BL	
Active	X	DMP		ADM	0	0	1	X	0	0	0	0	0	PLL
Active	X	KU		ODT	0	1	0	X	CD		CU		KD	
Active	X	QD	QU	IM	0	1	1	X	DD		DU		0	0
Reserved	X	0	0	0	1	0	0	X	0	0	0	0	0	0
	X	0	0	0	1	0	1	X	0	0	0	0	0	0
	X	0	0	0	1	1	0	X	0	0	0	0	0	0
	X	0	0	0	1	1	1	X	0	0	0	0	0	0

Table 3-4 MRS Configuration Bit Definitions

Speed Configuration					Clock Cycles		
Config #	Configuration			DI	tRC	tRL	tWL
0	0	0	0	0	Not supported		
1	0	0	1	0	Not supported		
2	0	1	0	0	Not supported		
3	0	1	1	0	Not supported		
4	1	0	0	0	10	12	13
5	1	0	1	0	11	14	15
6	1	1	0	0	Not supported		
7	1	1	1	0	Not supported		
0	0	0	0	1	Not supported		
1	0	0	1	1	Not supported		
2	0	1	0	1	Not supported		
3	0	1	1	1	Not supported		
4	1	0	0	1	10	14	15
5	1	0	1	1	11	16	17
6	1	1	0	1	Not supported		
7	1	1	1	1	Not supported		

Refresh Mode

RM	Operation
0	Auto Refresh Mode (Default)
1	Overlapped Refresh Mode

PLL Control

PLL	Operation
0	PLL Off / Reset (Default)
1	PLL On

Auto-DM Function

ADM	Operation
0	Off / Normal Operation (Default)
1	On

Note: When ADM=0, DMP=Don't Care

Burst Length

BL		Operation
0	0	4
0	1	Not supported
1	0	Reserved
1	1	Reserved

Note: Setting 01,10 & 11 not supported

Auto-DM Pattern

Burst of 4	DMP			
Pattern #	00	10	01	11
Write Beat 0	1	0	0	0
Write Beat 1	0	1	0	0
Write Beat 2	0	0	1	0
Write Beat 3	0	0	0	1

Note: Data to be written =1, Date to be masked =0

Impedance Freeze

FZ	Operation
0	Update active (Default)
1	Update frozen

Data Inversion

DI	Operation
0	Disable data inversion (Default)
1	Enable data inversion

Table 3-5 MRS Input Termination Bit Definitions

Pins
DQ, DIV, DM, DK0, DK0# DK1, DK1#

Data Input On-Die Termination - Up

ODT	DU		Div	200	240	RQ Ohms
1	X	X	**Off**	∞	∞	
X	1	1	**Off**	∞	∞	
0	1	0	**1**	200	240	
0	0	1	**1/2**	100	120	
0	0	0	**1/4**	50	60	

Data Input On-Die Termination - Down

ODT	DD		Div	200	240	RQ Ohms
1	X	X	**Off**	∞	∞	
X	1	1	**Off**	∞	∞	
0	1	0	**1**	∞	∞	(Not Supported)
0	0	1	**1/2**	∞	∞	(Not Supported)
0	0	0	**1/4**	∞	∞	(Not Supported)

Pins
Address, CS#, WE#, REF#

Control Input On-Die Termination - Up

ODT	CU		Div	200	240	RQ Ohms
1	X	X	**Off**	∞	∞	
X	1	1	**Off**	∞	∞	
0	1	0	**1**	200	240	
0	0	1	**1/2**	100	120	
0	0	0	**1/4**	50	60	

Control Input On-Die Termination - Down

ODT	CD		Div	200	240	RQ Ohms
1	X	X	**Off**	∞	∞	
X	1	1	**Off**	∞	∞	
0	1	0	**1**	∞	∞	(Not Supported)
0	0	1	**1/2**	∞	∞	(Not Supported)
0	0	0	**1/4**	∞	∞	(Not Supported)

Pins
CK, CK#

Clock Input On-Die Termination - Up

ODT	KU		Div	200	240	RQ Ohms
1	X	X	**Off**	∞	∞	
X	1	1	**Off**	∞	∞	
0	1	0	**1**	200	240	
0	0	1	**1/2**	100	120	
0	0	0	**1/4**	50	60	

Clock Input On-Die Termination - Down

ODT	KD		Div	200	240	RQ Ohms
1	X	X	**Off**	∞	∞	
X	1	1	**Off**	∞	∞	
0	1	0	**1**	∞	∞	(Not Supported)
0	0	1	**1/2**	∞	∞	(Not Supported)
0	0	0	**1/4**	∞	∞	(Not Supported)

Note . Internal RQ is set to 240Ω when IM=1.

Table 3-6 MRS Output Impedance Bit Definitions

Pins
DQ, DINV, QK0, QK0# QK1, QK1# QVLD

Output Driver Impedance - Up

IM	QU	Div	200	240	RQ Ohms
0	1	**1/4**	50	60	
1	X	**X**	60*	60*	
0	0	**1/6**	NA	40.0	

Note: 60* = 60 Ω +/- 20% no PVT compensation

Output Driver Impedance - Down

IM	QD	Div	200	240	RQ Ohms
0	1	**1/4**	50	60	
1	X	**X**	40*	40*	
0	0	**1/6**	33.3	40.0	

Note: 40* = 40 Ω +/- 20% no PVT compensation

Figure 3-6 MRS Sequence

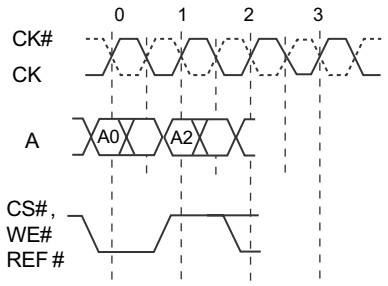
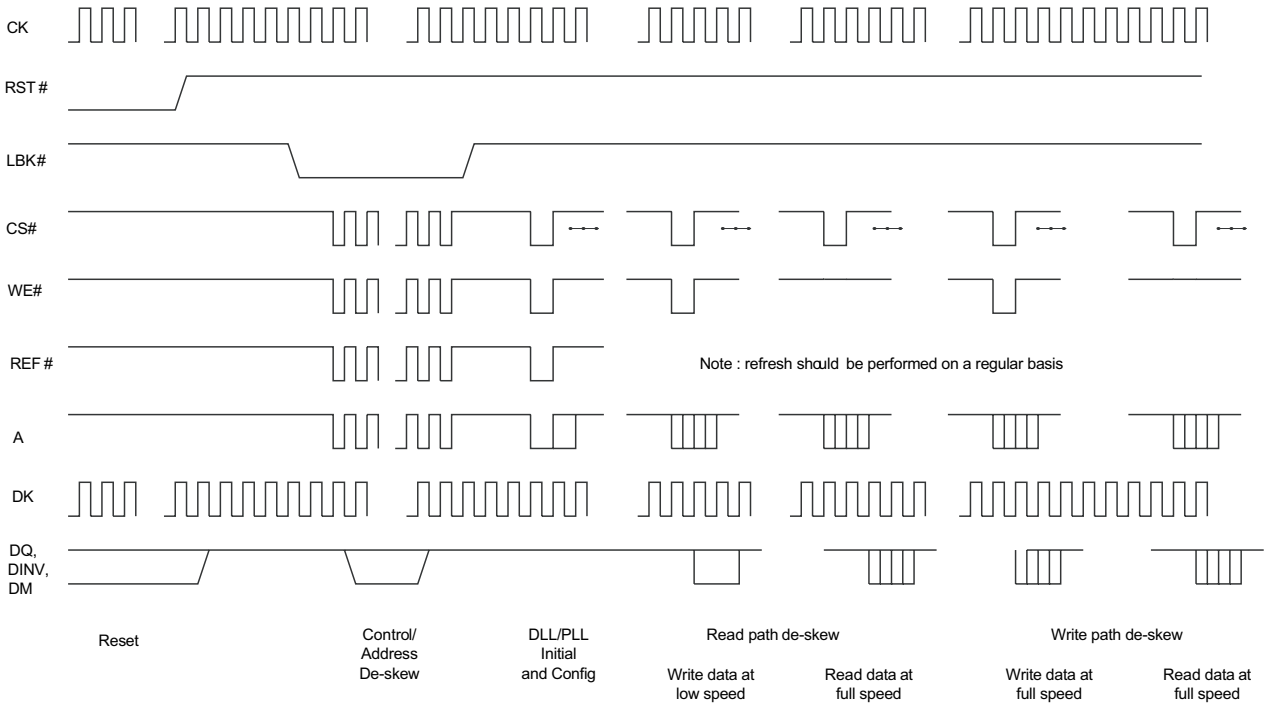


Figure 3-7 Initialization Sequence (DDR Address mode shown)



4.JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

4.1 Test Pins

Table 4-1 Low Latency DRAM-III Test Pins

Pin Name	Test Use	Functional Mode Value	Pull Up/Down in Chip	Pull Up/Down on Board
TDI	JTAG serial chain input	1	1	1
TDO	JTAG serial chain output	1		
TCK	JTAG clock	0	0	0
TMS	JTAG mode	1	1	1
TRST#	JTAG reset	0	0	0

Table 4-2. Test Access Port (TAP) Pins

Pin Name	Pin Assignment	Description
TCK	3A	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	1A	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	13V	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	13T	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.
TRST#	1L	Test Reset Input. This is active-low input asynchronously reset the TAP controller. This pin should be driven low or tied to GND when JTAG function is not in use.

Table 4-3. JTAG DC Characteristics ($0°C \le T_C \le 95°C$, $1.395\ V \le V_{DD} \le 1.605\ V$, unless otherwise noted)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
JTAG Input leakage current	I_{LI}	$0\ V \le V_{IN} \le V_{DD}$	−100	+100	μA
JTAG I/O leakage current	I_{LO}	$0\ V \le V_{IN} \le V_{DD}Q$, Outputs disabled	−100	+100	μA
JTAG input HIGH voltage	$V_{IH\ (DC)}$		V_{REF} + 0.15	V_{DD} + 0.3	V
JTAG input LOW voltage	$V_{IL\ (DC)}$		$V_{SS}Q$ − 0.3	V_{REF} − 0.15	V
JTAG output HIGH voltage	$V_{OH\ (DC)}$	$\lvert I_{OHC} \rvert$ = 100 μA	$V_{DD}Q$ − 0.25		V
JTAG output LOW voltage	$V_{OL\ (DC)}$	I_{OLC} = 100 μA		0.25	V

Note 1. All voltages referenced to V_{SS} (GND).

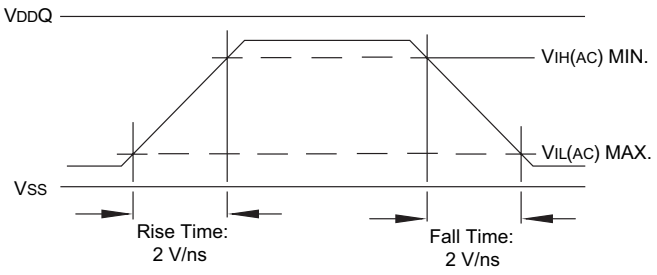
Table 4-4. JTAG Capacitance

Parameter	Symbol	Teat Conditions	MIN.	MAX.	Unit
JTAG Input Capacitance (TCK, TMS and TRST#)	C_{INJ}	V_{IN} = 0V		2.5	pF
JTAG I/O leakage current (TDO)	C_{OJ}	V_{IO} = 0V		2.5	pF

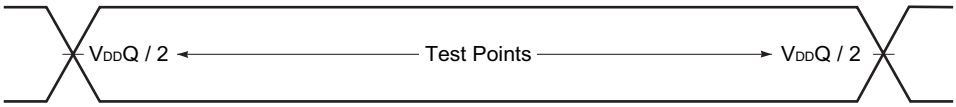
Note 1. Including package.

4.2 JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 0.3 ns)



Output waveform



Output load condition

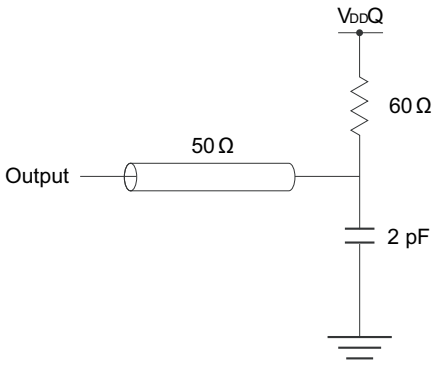


Table 4-5. JTAG AC Characteristics (0°C ≤ T_C ≤ 95°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock						
Clock cycle time	t_{THTH}		20		ns	
Clock frequency	f_{TF}			50	MHz	
Clock HIGH time	t_{THTL}		10		ns	
Clock LOW time	t_{TLTH}		10		ns	
Output time						
TCK LOW to TDO unknown	t_{TLOX}		0		ns	
TCK LOW to TDO valid	t_{TLOV}			10	ns	
Setup time						
TMS setup time	t_{MVTH}		5		ns	
TDI valid to TCK HIGH	t_{DVTH}		5		ns	
TRST High Level to valid riseing edge of TCK	t_{RVTH}		50		ns	
Capture setup time	t_{CSJ}		5		ns	1
Hold time						
TMS hold time	t_{THMX}		5		ns	
TCK HIGH to TDI invalid	t_{THDX}		5		ns	
Capture hold time	t_{CHJ}		5		ns	1
Reset						
TRST LOW pulse width	t_{TRSTW}		100		ns	

Note 1. t_{CSJ} and t_{CHJ} refer to the setup and hold time requirements of latching data from the boundary scan register.

JTAG Timing Diagram

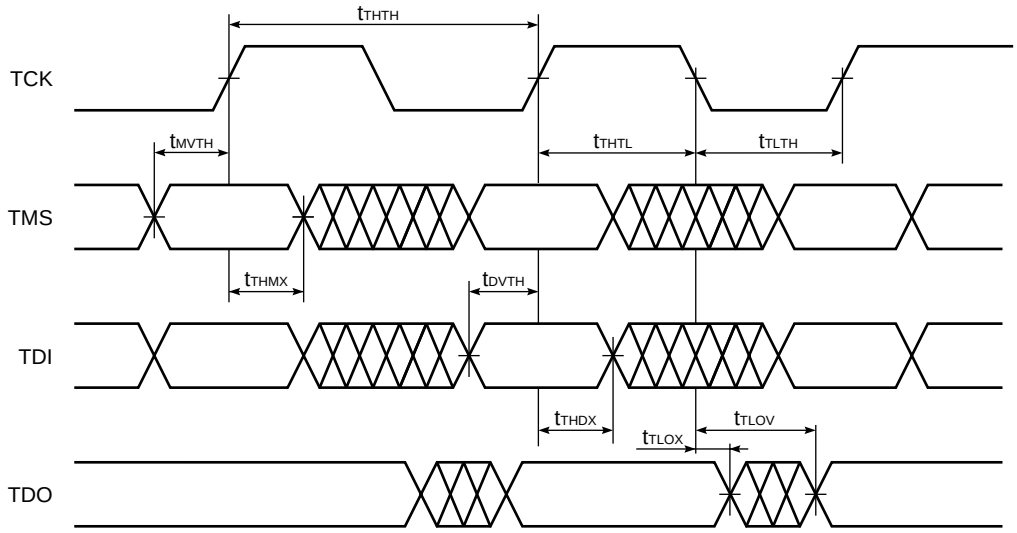


Table 4-6. Scan Register Definition (1)

Register name	Description
Instruction register	The 8 bit instruction registers hold the instructions that are executed by the TAP controller. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible. The bypass register is set LOW (V_{SS}) when the bypass instruction is executed.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Table 4-7. Scan Register Definition (2)

Register name	Bit size	Unit
Instruction register	8	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	113	bit

Table 4-8. ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD48011418	64M x 18	0000	0000 0000 1101 1100	00000010000	1
μPD48011436	32M x 36	0000	0000 0000 1101 1101	00000010000	1

4.3 Boundary Scan

IEEE 1149.1 compliant boundary scan will be implemented on all component I/O pins. High speed I/Os that are differential or AC coupled will be fully compliant to the IEEE 1149.6 standard.

The actual boundary scan order is defined in an underscore (e.g. “CS#_WE#”).

Table 4-9 and **Table 4-10**.

Pins labeled DNU0 are DNU, V_{SS}. Pins labeled DNU1 are DNU, $V_{DD}Q$. Pins that are subject to the mirror function are named with the obverse name and reverse name, separated by an underscore (e.g. “CS#_WE#”).

Table 4-9 Boundary Scan Order, x18

x18	Cell #	Cell	Pin Name	TYPE	Safe Bit	Cntrl Cell	Cntrl Value	Cntrl State
J3	0	BC_1	DK0	input	X			
K3	1	BC_1	DK0#	input	X			
L2	2	BC_1	CS#_WE#	input	X			
L4	3	BC_1	A4_A3	input	X			
M5	4	BC_1	A2_REF#	input	X			
M3	5	BC_1	DNU1(1)	internal	X			
	6	BC_2	*	control	0			
N2	7	BC_7	DINV1	bidir	X	6	0	Z
N4	8	BC_1	A0_A1	input	X			
	9	BC_2	*	control	0			
P5	10	BC_7	DQ9	bidir	X	9	0	Z
	11	BC_2	*	internal	0			
P3	12	BC_7	DNU0(1)	internal	X			
	13	BC_2	*	internal	0			
P1	14	BC_7	DNU0(2)	internal	X			
	15	BC_2	*	internal	0			
R2	16	BC_7	DNU0(3)	internal	X			
	17	BC_2	*	control	0			
R4	18	BC_7	DQ11	bidir	X	17	0	Z
	19	BC_2	*	control	0			
T5	20	BC_7	DQ13	bidir	X	19	0	Z
	21	BC_2	*	internal	0			
T3	22	BC_7	DNU0(4)	internal	X			
T1	23	BC_1	QK1#	output2	X			
	24	BC_2	*	internal	0			
U2	25	BC_7	DNU0(5)	internal	X			
	26	BC_2	*	control	0			
U4	27	BC_7	DQ15	bidir	X	26	0	Z
V1	28	BC_1	QK1	output2	X			
	29	BC_2	*	control	0			
U12	30	BC_7	DQ17	bidir	X	29	0	Z
	31	BC_2	*	internal	0			
U10	32	BC_7	DNU0(6)	internal	X			
	33	BC_2	*	internal	0			
T9	34	BC_7	DNU0(7)	internal	X			
	35	BC_2	*	control	0			
T11	36	BC_7	DQ16	bidir	X	35	0	Z
	37	BC_2	*	control	0			
R12	38	BC_7	DQ14	bidir	X	37	0	Z
	39	BC_2	*	internal	0			
R10	40	BC_7	DNU0(8)	internal	X			
	41	BC_2	*	internal	0			
P9	42	BC_7	DNU0(9)	internal	X			
	43	BC_2	*	control	0			
P11	44	BC_7	DQ10	bidir	X	43	0	Z
	45	BC_2	*	control	0			
P13	46	BC_7	DQ12	bidir	X	45	0	Z
	47	BC_2	*	internal	0			
N12	48	BC_7	DNU0(10)	internal	X			
N10	49	BC_1	A1_A0	input	X			
M9	50	BC_1	REF#_A2	input	X			
M11	51	BC_1	DNU1(2)	internal	X			
L12	52	BC_1	WE#_CS#	input	X			
L10	53	BC_1	A3_A4	input	X			
K9	54	BC_1	CK#	input	X			
K11	55	BC_1	DNU0(11)	internal	X			
J13	56	BC_1	LBK#	input	1			
J11	57	BC_1	DNU0(12)	internal	X			
J9	58	BC_1	CK	input	X			

x18	Cell #	Cell	Pin Name	TYPE	Safe Bit	Cntrl Cell	Cntrl Value	Cntrl State
H10	59	BC_1	A5_A6	input	X			
H12	60	BC_1	DM_RST#	input	X			
G11	61	BC_1	DNU1(3)	internal	X			
G9	62	BC_1	DNU1(4)	internal	X			
F10	63	BC_1	DNU1(5)	internal	X			
	64	BC_2	*	internal	0			
F12	65	BC_7	DNU0(13)	internal	X			
	66	BC_2	*	control	0			
E13	67	BC_7	DQ3	bidir	X	66	0	Z
	68	BC_2	*	control	0			
E11	69	BC_7	DQ1	bidir	X	68	0	Z
	70	BC_2	*	internal	0			
E9	71	BC_7	DNU0(14)	internal	X			
	72	BC_2	*	internal	0			
D10	73	BC_7	DNU0(15)	internal	X			
	74	BC_2	*	control	0			
D12	75	BC_7	DQ5	bidir	X	74	0	Z
C13	76	BC_1	QK0#	output2	X			
	77	BC_2	*	control	0			
C11	78	BC_7	DQ7	bidir	X	77	0	Z
	79	BC_2	*	internal	0			
C9	80	BC_7	DNU0(16)	internal	X			
	81	BC_2	*	internal	0			
B10	82	BC_7	DNU0(17)	internal	X			
	83	BC_2	*	control	0			
B12	84	BC_7	DQ8	bidir	X	83	0	Z
A13	85	BC_1	QK0	output2	X			
	86	BC_2	*	control	0			
B4	87	BC_7	DQ6	bidir	X	86	0	Z
	88	BC_2	*	internal	0			
B2	89	BC_7	DNU0(18)	internal	X			
C1	90	BC_1	QVLD	output2	X			
	91	BC_2	*	internal	0			
C3	92	BC_7	DNU0(19)	internal	X			
	93	BC_2	*	control	0			
C5	94	BC_7	DQ4	bidir	X	93	0	Z
	95	BC_2	*	control	0			
D4	96	BC_7	DQ2	bidir	X	95	0	Z
	97	BC_2	*	internal	0			
D2	98	BC_7	DNU0(20)	internal	X			
	99	BC_2	*	internal	0			
E1	100	BC_7	DNU0(21)	internal	X			
	101	BC_2	*	internal	0			
E3	102	BC_7	DNU0(22)	internal	X			
	103	BC_2	*	control	0			
E5	104	BC_7	DQ0	bidir	X	103	0	Z
F4	105	BC_1	DNU1(6)	internal	X			
	106	BC_2	*	control	0			
F2	107	BC_7	DINV0	bidir	X	106	0	Z
G3	108	BC_1	DNU1(7)	internal	X			
G5	109	BC_1	DNU1(8)	internal	X			
H4	110	BC_1	A6_A5	input	X			
H2	111	BC_1	RST#_DM	input	X			
J1	112	BC_1	MF	input	X			

Table 4-10 Boundary Scan Order, x36

x36	Cell #	Cell	Pin Name	TYPE	Safe Bit	Cntrl Cell	Cntrl Value	Cntrl State
J3	0	BC_1	DK0	input	X			
K3	1	BC_1	DK0#	input	X			
L2	2	BC_1	CS#_WE#	input	X			
L4	3	BC_1	A4_A3	input	X			
M5	4	BC_1	A2_REF#	input	X			
M3	5	BC_1	DNU1(1)	internal	X			
	6	BC_2	*	control	0			
N2	7	BC_7	DINV2	bidir	X	6	0	Z
N4	8	BC_1	A0_A1	input	X			
	9	BC_2	*	control	0			
P5	10	BC_7	DQ18	bidir	X	9	0	Z
	11	BC_2	*	control	0			
P3	12	BC_7	DQ34	bidir	X	11	0	Z
	13	BC_2	*	control	0			
P1	14	BC_7	DQ35	bidir	X	13	0	Z
	15	BC_2	*	control	0			
R2	16	BC_7	DQ32	bidir	X	15	0	Z
	17	BC_2	*	control	0			
R4	18	BC_7	DQ20	bidir	X	17	0	Z
	19	BC_2	*	control	0			
T5	20	BC_7	DQ22	bidir	X	19	0	Z
	21	BC_2	*	control	0			
T3	22	BC_7	DQ30	bidir	X	21	0	Z
T1	23	BC_1	QK1#	output2	X			
	24	BC_2	*	control	0			
U2	25	BC_7	DQ28	bidir	X	24	0	Z
	26	BC_2	*	control	0			
U4	27	BC_7	DQ24	bidir	X	26	0	Z
V1	28	BC_1	QK1	output2	X			
	29	BC_2	*	control	0			
U12	30	BC_7	DQ26	bidir	X	29	0	Z
	31	BC_2	*	control	0			
U10	32	BC_7	DQ27	bidir	X	31	0	Z
	33	BC_2	*	control	0			
T9	34	BC_7	DQ29	bidir	X	33	0	Z
	35	BC_2	*	control	0			
T11	36	BC_7	DQ25	bidir	X	35	0	Z
	37	BC_2	*	control	0			
R12	38	BC_7	DQ23	bidir	X	37	0	Z
	39	BC_2	*	control	0			
R10	40	BC_7	DQ31	bidir	X	39	0	Z
	41	BC_2	*	control	0			
P9	42	BC_7	DQ33	bidir	X	41	0	Z
	43	BC_2	*	control	0			
P11	44	BC_7	DQ19	bidir	X	43	0	Z
	45	BC_2	*	control	0			
P13	46	BC_7	DQ21	bidir	X	45	0	Z
	47	BC_2	*	control	0			
N12	48	BC_7	DINV3	bidir	X	47	0	Z
N10	49	BC_1	A1_A0	input	X			
M9	50	BC_1	REF#_A2	input	X			
M11	51	BC_1	DNU1(2)	internal	X			
L12	52	BC_1	WE#_CS#	input	X			
L10	53	BC_1	A3_A4	input	X			
K9	54	BC_1	CK#	input	X			
K11	55	BC_1	DK1#	input	X			
J13	56	BC_1	LBK#	input	1			
J11	57	BC_1	DK1	input	X			
J9	58	BC_1	CK	input	X			

x36	Cell #	Cell	Pin Name	TYPE	Safe Bit	Cntrl Cell	Cntrl Value	Cntrl State
H10	59	BC_1	A5_A6	input	X			
H12	60	BC_1	DM_RST#	input	X			
G11	61	BC_1	DNU1(3)	internal	X			
G9	62	BC_1	DNU1(4)	internal	X			
F10	63	BC_1	DNU1(5)	internal	X			
	64	BC_2	*	control	0			
F12	65	BC_7	DINV1	bidir	X	64	0	Z
	66	BC_2	*	control	0			
E13	67	BC_7	DQ3	bidir	X	66	0	Z
	68	BC_2	*	control	0			
E11	69	BC_7	DQ1	bidir	X	68	0	Z
	70	BC_2	*	control	0			
E9	71	BC_7	DQ17	bidir	X	70	0	Z
	72	BC_2	*	control	0			
D10	73	BC_7	DQ15	bidir	X	72	0	Z
	74	BC_2	*	control	0			
D12	75	BC_7	DQ5	bidir	X	74	0	Z
C13	76	BC_1	QK0#	output2	X			
	77	BC_2	*	control	0			
C11	78	BC_7	DQ7	bidir	X	77	0	Z
	79	BC_2	*	control	0			
C9	80	BC_7	DQ13	bidir	X	79	0	Z
	81	BC_2	*	control	0			
B10	82	BC_7	DQ11	bidir	X	81	0	Z
	83	BC_2	*	control	0			
B12	84	BC_7	DQ8	bidir	X	83	0	Z
A13	85	BC_1	QK0	output2	X			
	86	BC_2	*	control	0			
B4	87	BC_7	DQ6	bidir	X	86	0	Z
	88	BC_2	*	control	0			
B2	89	BC_7	DQ9	bidir	X	88	0	Z
C1	90	BC_1	QVLD	output2	X			
	91	BC_2	*	control	0			
C3	92	BC_7	DQ10	bidir	X	91	0	Z
	93	BC_2	*	control	0			
C5	94	BC_7	DQ4	bidir	X	93	0	Z
	95	BC_2	*	control	0			
D4	96	BC_7	DQ2	bidir	X	95	0	Z
	97	BC_2	*	control	0			
D2	98	BC_7	DQ12	bidir	X	97	0	Z
	99	BC_2	*	control	0			
E1	100	BC_7	DQ16	bidir	X	99	0	Z
	101	BC_2	*	control	0			
E3	102	BC_7	DQ14	bidir	X	101	0	Z
	103	BC_2	*	control	0			
E5	104	BC_7	DQ0	bidir	X	103	0	Z
F4	105	BC_1	DNU1(6)	internal	X			
	106	BC_2	*	control	0			
F2	107	BC_7	DINV0	bidir	X	106	0	Z
G3	108	BC_1	DNU1(7)	internal	X			
G5	109	BC_1	DNU1(8)	internal	X			
H4	110	BC_1	A6_A5	input	X			
H2	111	BC_1	RST#_DM	input	X			
J1	112	BC_1	MF	input	X			

4.4 JTAG Instructions

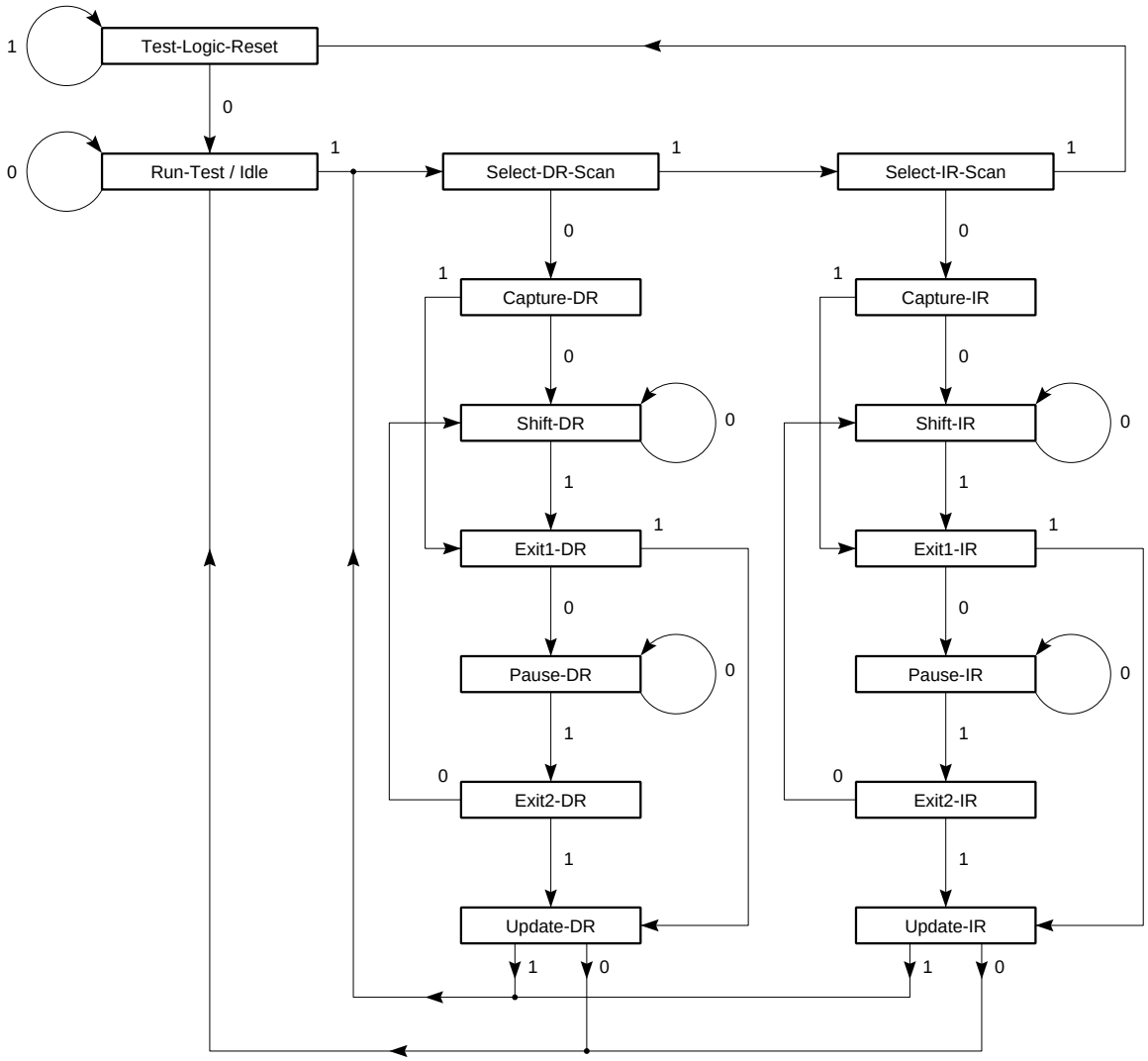
Many different instructions (2^8) are possible with the 8-bit instruction register. All used combinations are listed in **Table 4-11**, Instruction Codes. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RAM is fully compliant to the 1149.1 convention. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

Table 4-11

Instructions	Instruction Code [7:0]	Description
EXTEST	0000 0000	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	0010 0001	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
SAMPLE / PRELOAD	0000 0101	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and Q pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
CLAMP	0000 0111	When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register. Selects the bypass register to be connected between TDI and TDO. Data driven by output balls are determined from values held in the boundary scan register.
High-Z	0000 0011	The High-z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RAMs outputs into a High-Z state. Selects the bypass register to be connected between TDI and TDO. All outputs are forced into high impedance state.
BYPASS	1111 1111	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
Reserved for Future Use	–	The remaining instructions are not implemented but are reserved for future use. Do not use these instructions.

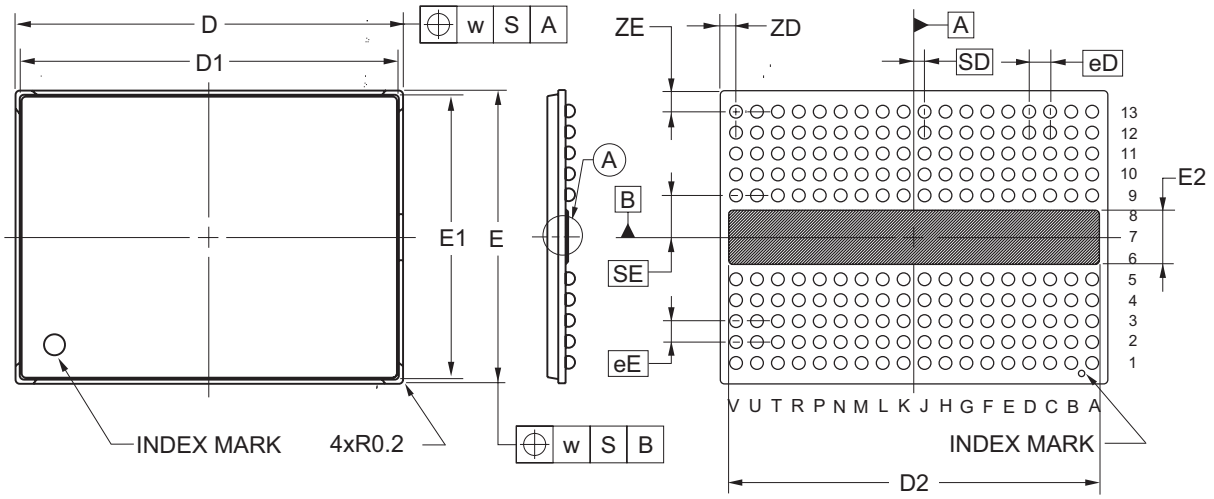
4.5 TAP Controller State Diagram

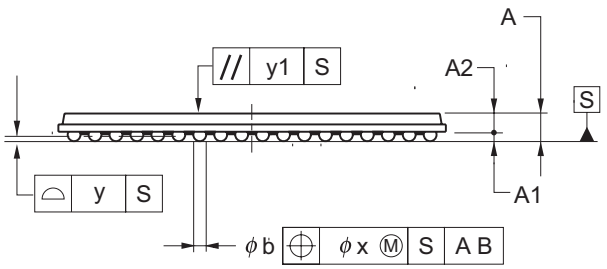


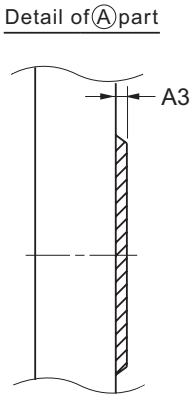
5. Package Drawing

180-PIN TAPE FBGA (BGA) (18.5 x 14)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
T-LBGA180-14x18.5-1.00	TLBG0180FA-A	T180FF-100-FF1	0.60







(UNIT:mm)

ITEM	DIMENSIONS
D	18.50 ± 0.10
D1	18.10
D2	17.70
E	14.00 ± 0.10
E1	13.60
E2	2.59
w	0.20
eD	1.00
eE	1.00
SD	0.50
SE	2.00
A	1.274 ± 0.10
A1	0.47 ± 0.05
A2	0.804
A3	0.135
b	0.61 ± 0.05
x	0.15
y	0.10
y1	0.20
ZD	0.75
ZE	1.00

T180FF-100-FF1

Rev.	Date	Description	
		Page	Summary
Rev.0.01	’10.08.18	-	New Preliminary Data Sheet
Rev.1.00	’12.10.10	- P11 P16 P29 P50	New Data Sheet Update “DC Characteristics” Update “Thermal Impedance” Modified comments for “Power on” Update “Package Drawing”
Rev.2.00	’13.02.01	P7	Update “Block Diagram”