To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD3777

5400 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

The μPD3777 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD3777 has 3 rows of 5400 pixels, and each row has a double-sided readout type of charge transfer register. And it has reset feed-through level clamp circuits, a clamp pulse generation circuit and voltage amplifiers. Therefore, it is suitable for 600 dpi/A4 color image scanners, color facsimiles and so on.

FEATURES

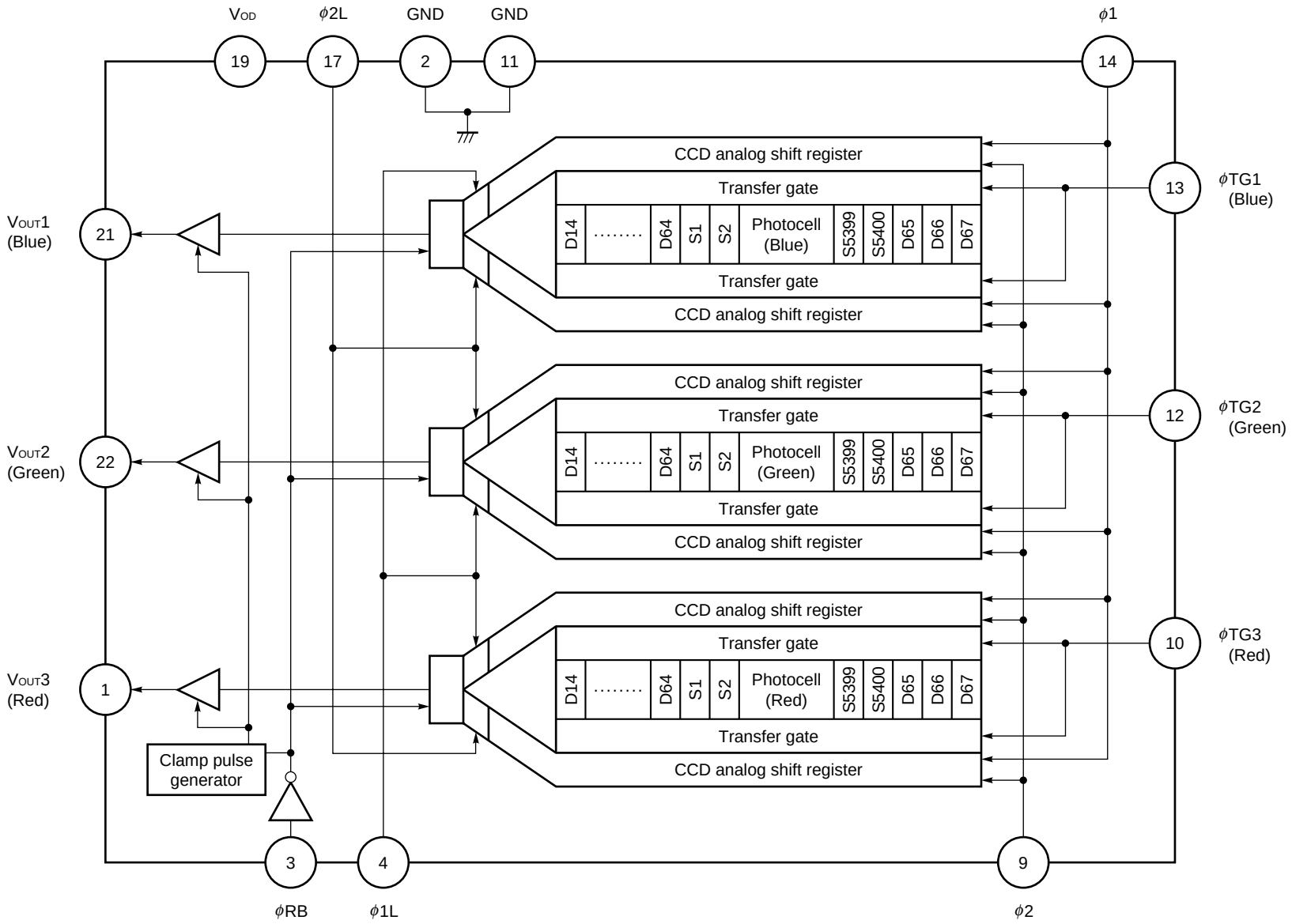
- Valid photocell : 5400 pixels × 3
- Photocell's pitch : 5.25 μm
- Photocell size : 5.25 × 5.25 μm^2
- Line spacing : 42 μm (8 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 24 dot/mm A4 (210 × 297 mm) size (shorter side)
  600 dpi US letter (8.5" × 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 4 MHz MAX.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Clamp pulse generation circuit
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD3777CY	CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Document No. S14583EJ1V0DS00 (1st edition)
Date Published December 1999 NS CP (K)
Printed in Japan

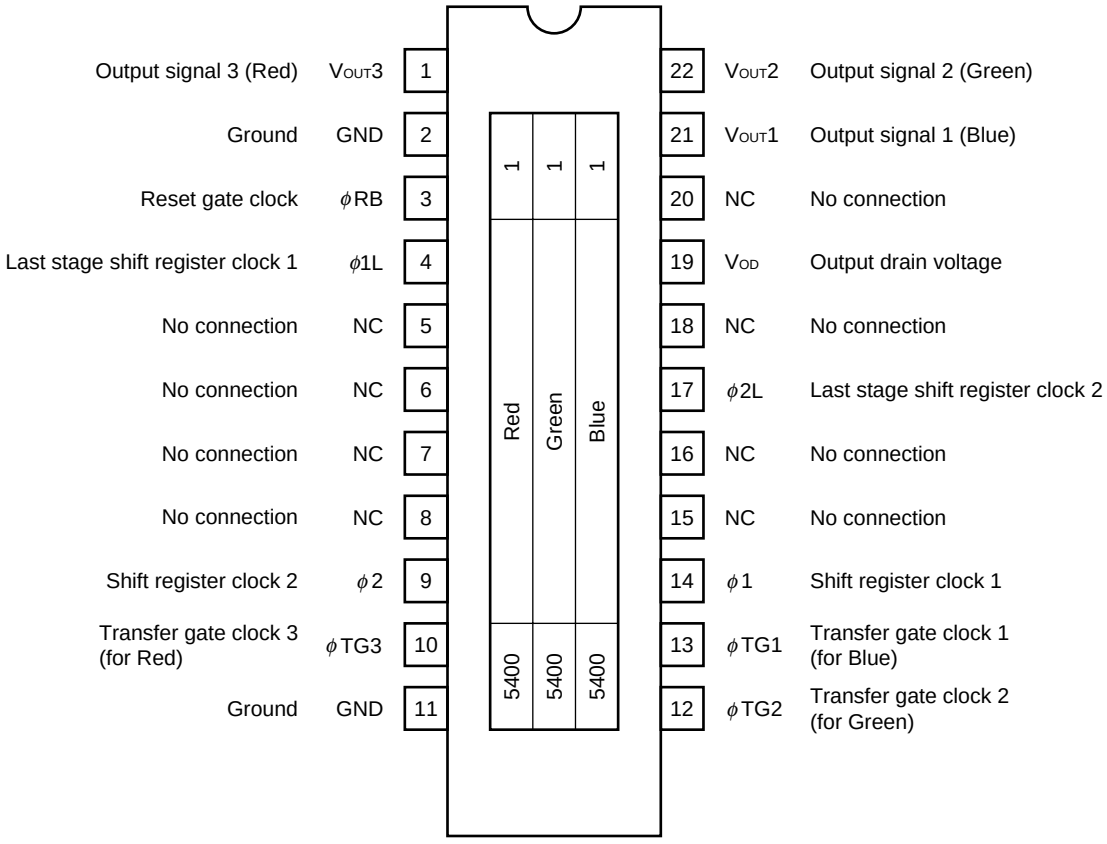
BLOCK DIAGRAM



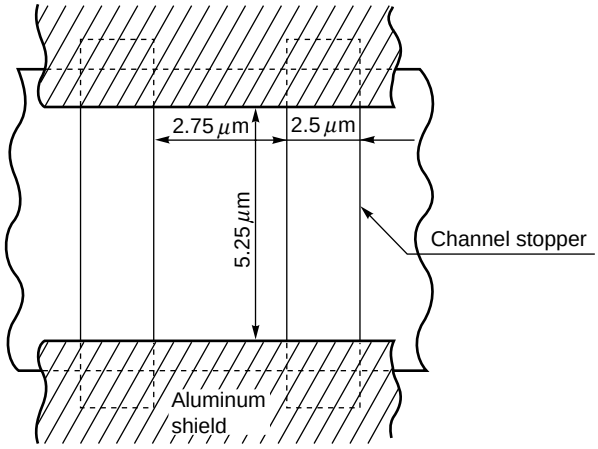
PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

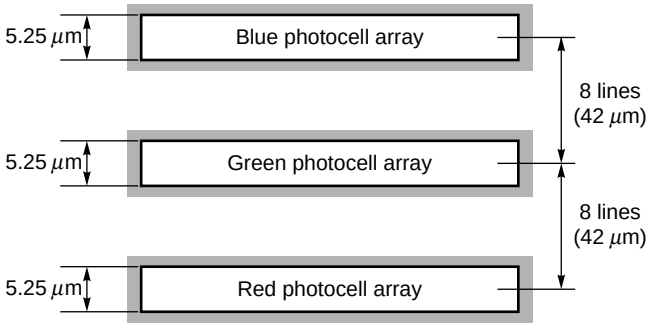
- μPD3777CY



PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$, $V_{\phi 1L}$, $V_{\phi 2L}$	–0.3 to +8	V
Reset gate clock voltage	$V_{\phi RB}$	–0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	–0.3 to +8	V
Operating ambient temperature	T_A	–25 to +60	°C
Storage temperature	T_{stg}	–40 to +70	°C

Caution Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

RECOMMENDED OPERATING CONDITIONS (T_A = +25 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$, $V_{\phi 1LH}$, $V_{\phi 2LH}$	4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$, $V_{\phi 1LL}$, $V_{\phi 2LL}$	–0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	–0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.5	$V_{\phi 1H}$ Note	$V_{\phi 1H}$ Note	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	–0.3	0	+0.5	V
Data rate	$f_{\phi RB}$	–	1.0	4.0	MHz

Note When Transfer gate clock high level ($V_{\phi TG1H}$ to $V_{\phi TG3H}$) is higher than Shift register clock high level ($V_{\phi 1H}$), Image lag can increase.

ELECTRICAL CHARACTERISTICS

(T_A = +25 °C, V_{OD} = 12 V, data rate ($f_{\phi RB}$) = 1 MHz, storage time = 5.5 ms, input signal clock = 5 V_{p-p}, light source : 3200 K halogen lamp + C–500S (infrared cut filter, t = 1 mm) + HA–50 (heat absorbing filter, t = 3 mm))

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		V_{sat}		2.0	2.5	–	V
Saturation exposure	Red	SER			0.420		lx•s
	Green	SEG			0.429		lx•s
	Blue	SEB			0.739		lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V		6	20	%
Average dark signal		ADS	Light shielding		0.2	2.0	mV
Dark signal non-uniformity		DSNU	Light shielding		1.5	5.0	mV
Power consumption		P_W			360	540	mW
Output impedance		Z_O			0.5	1	kΩ
Response	Red	R_R		4.15	5.94	7.72	V/lx•s
	Green	R_G		4.07	5.82	7.57	V/lx•s
	Blue	R_B		2.36	3.38	4.39	V/lx•s
Image lag		IL	V_{OUT} = 1.0 V		2.0	7.0	%
Offset level Note 1		V_{OS}		4.0	5.5	7.0	V
Output fall delay time Note 2		t_d	V_{OUT} = 1.0 V		50		ns
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, data rate = 4 MHz	92	98		%
Register imbalance		RI	V_{OUT} = 1.0 V	0	1.0	4.0	%
Response peak	Red				630		nm
	Green				540		nm
	Blue				460		nm
Dynamic range		DR1	V_{sat}/DSNU		1666		times
		DR2	V_{sat}/σ		2500		times
Reset feed-through noise Note 1		RFTN	Light shielding	–1000	–300	+500	mV
Random noise		σ	Light shielding	–	1.0	–	mV

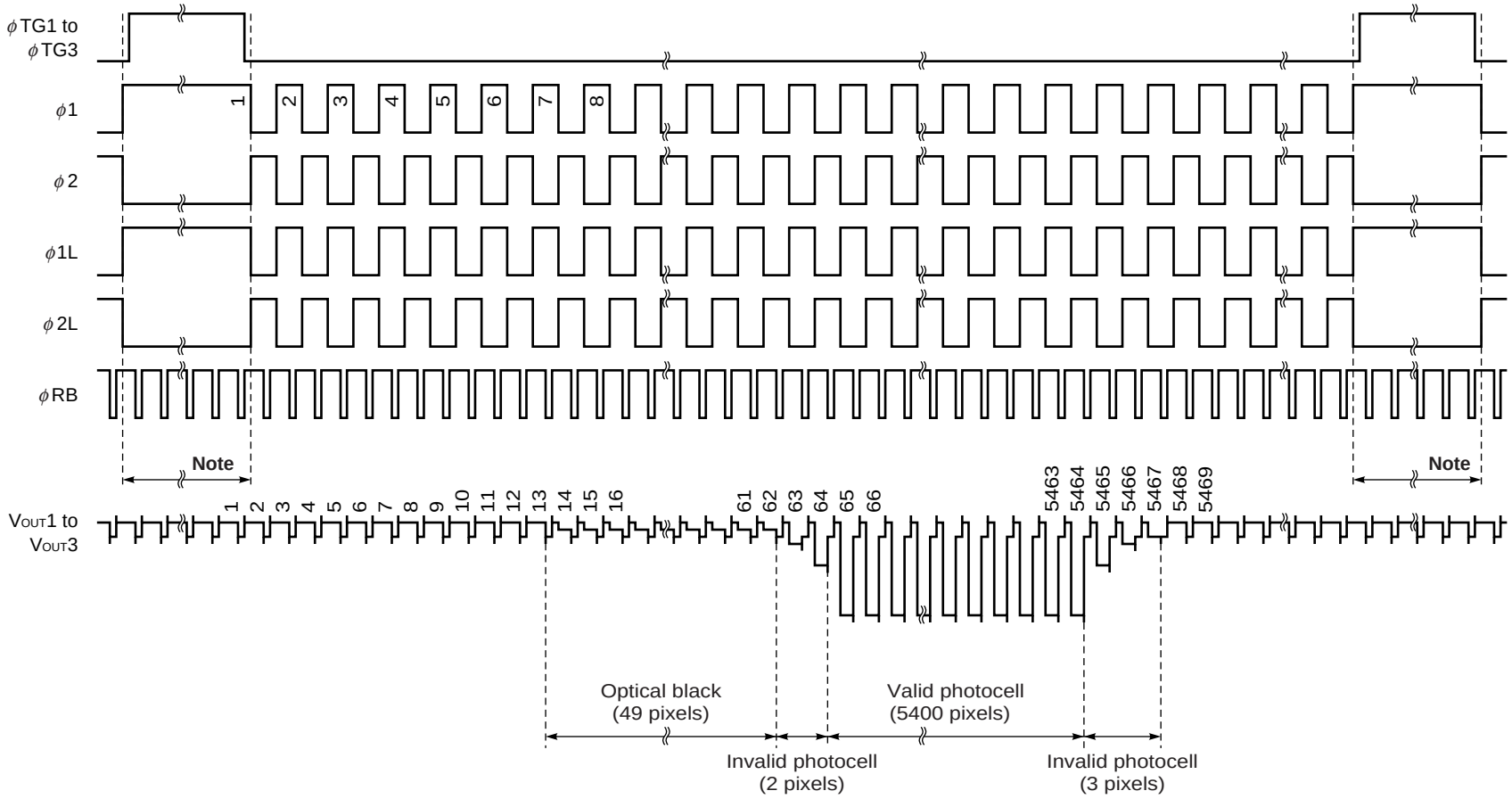
Notes 1. Refer to **TIMING CHART 2**.

2. When each fall time of ϕ 1L and ϕ 2L (t2', t1') is the TYP. value (refer to **TIMING CHART 2**).

INPUT PIN CAPACITANCE (T_A = +25 °C, V_{OD} = 12 V)

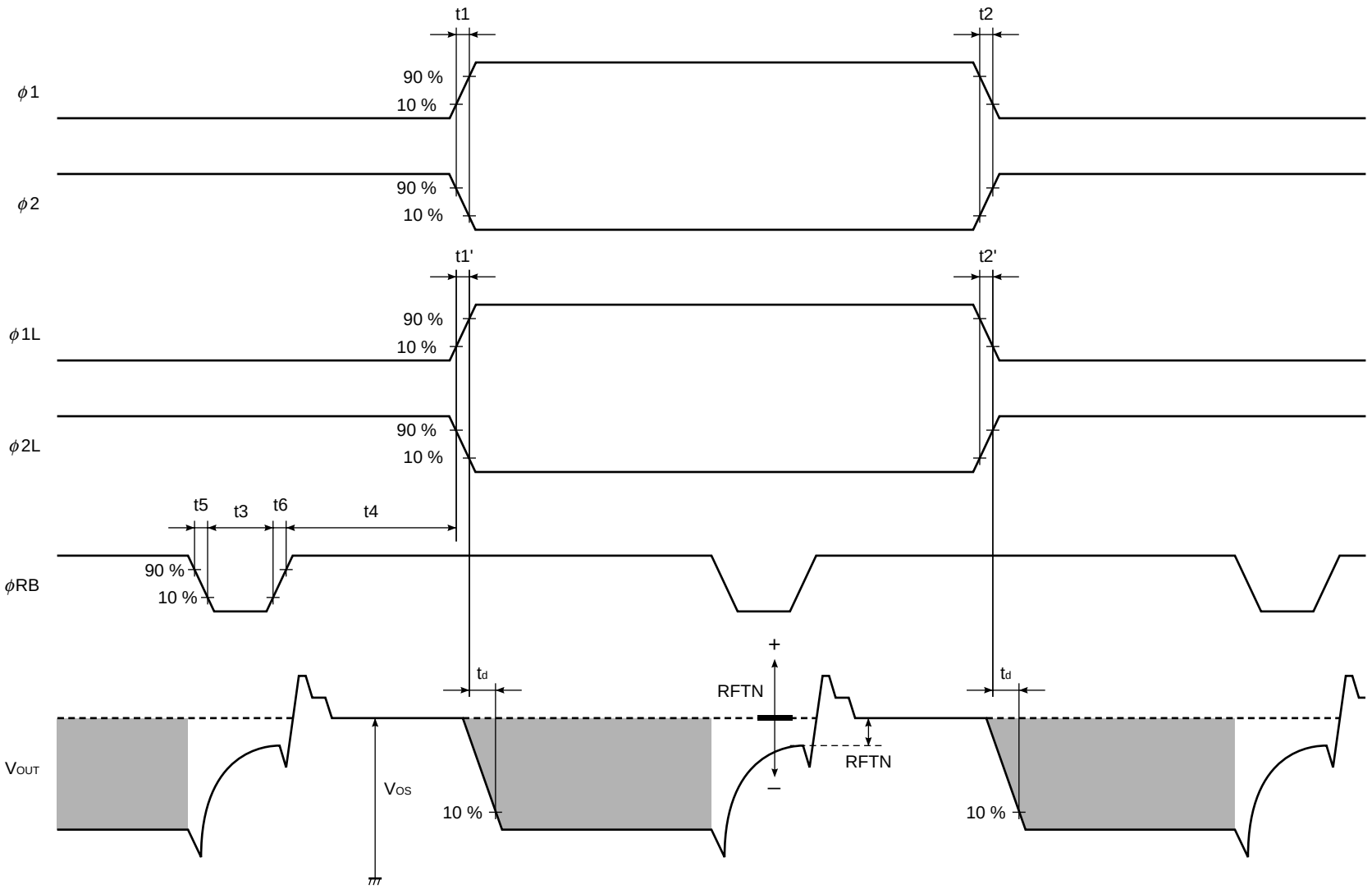
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	14		650		pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	9		650		pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ1L	4		10		pF
		ϕ2L	17		10		pF
Reset gate clock pin capacitance	$C_{\phi RB}$	ϕRB	3		10		pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG1	13		60		pF
		ϕTG2	12		60		pF
		ϕTG3	10		60		pF

TIMING CHART 1 (for each color)

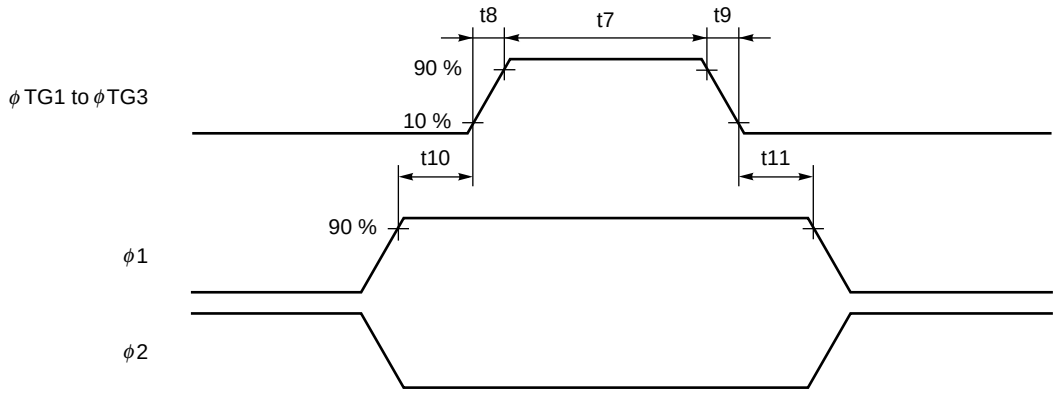


Note Input the φRB pulse continuously during this period, too.

TIMING CHART 2 (for each color)

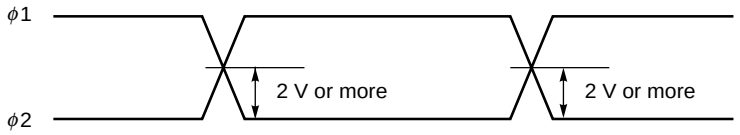


φTG1 to φTG3, φ1, φ2 TIMING CHART

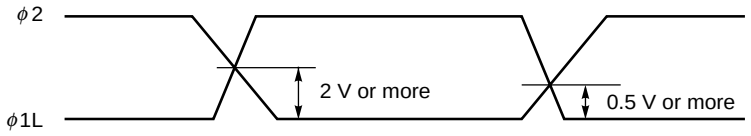


Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t3	20	150	–	ns
t4	130	300	–	ns
t5, t6	0	50	–	ns
t7	3000	10000	–	ns
t8, t9	0	50	–	ns
t10, t11	900	1000	–	ns

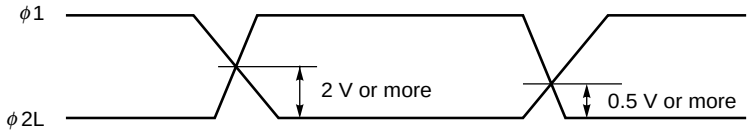
φ1, φ2 cross points



φ1L, φ2 cross points



φ1, φ2L cross points



Remark Adjust cross points (φ1, φ2), (φ1L, φ2) and (φ1, φ2L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

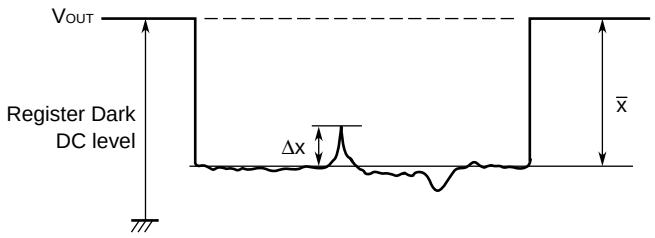
3. Photo response non-uniformity : **PRNU**
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{5400} x_j}{5400}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS\ (mV) = \frac{\sum_{j=1}^{5400} d_j}{5400}$$

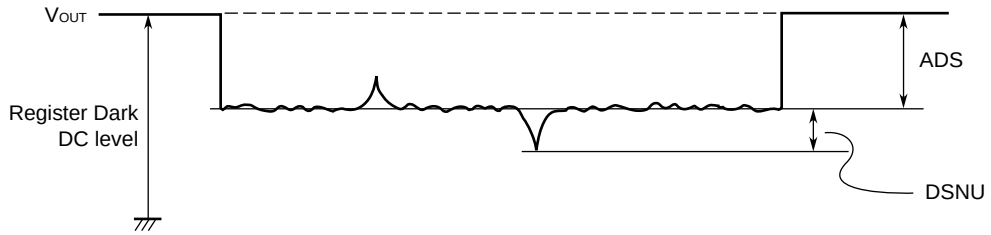
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV) : maximum of $|d_j - ADS|_{j = 1 \text{ to } 5400}$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

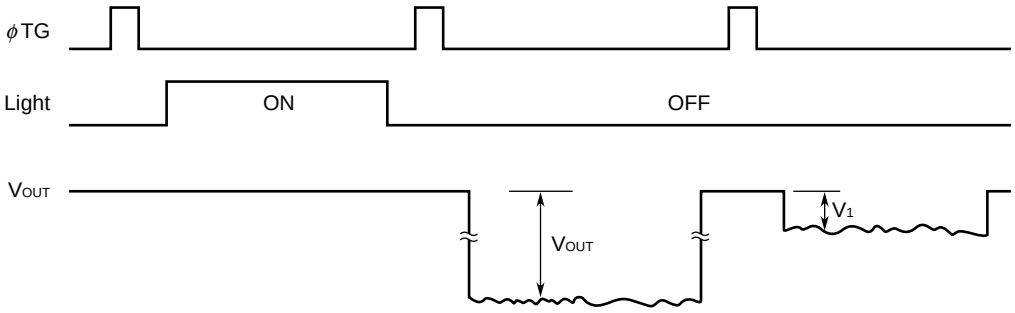
7. Response : **R**

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

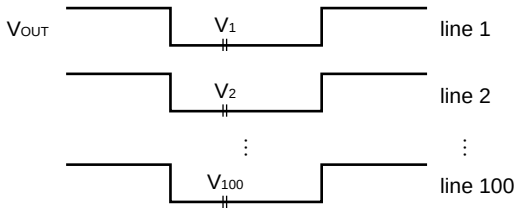
V_j : Output voltage of each pixel

10. Random noise : **σ**

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

$$\sigma\ (\mathrm{mV}) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \ \overline{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

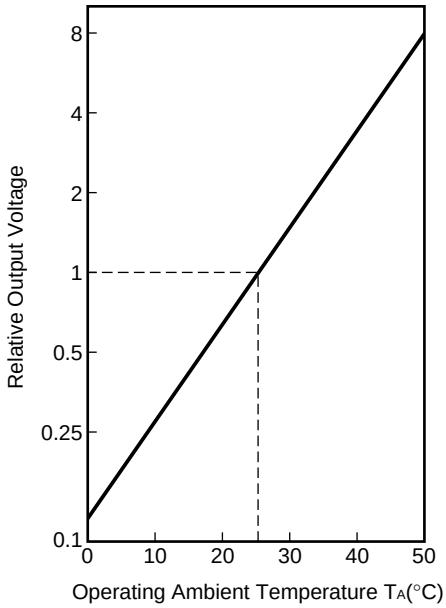
V_i : A valid pixel output signal among all of the valid pixels for each color



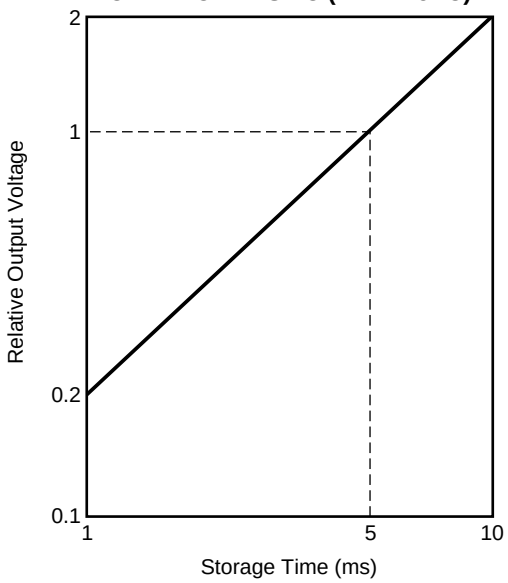
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES (Nominal)

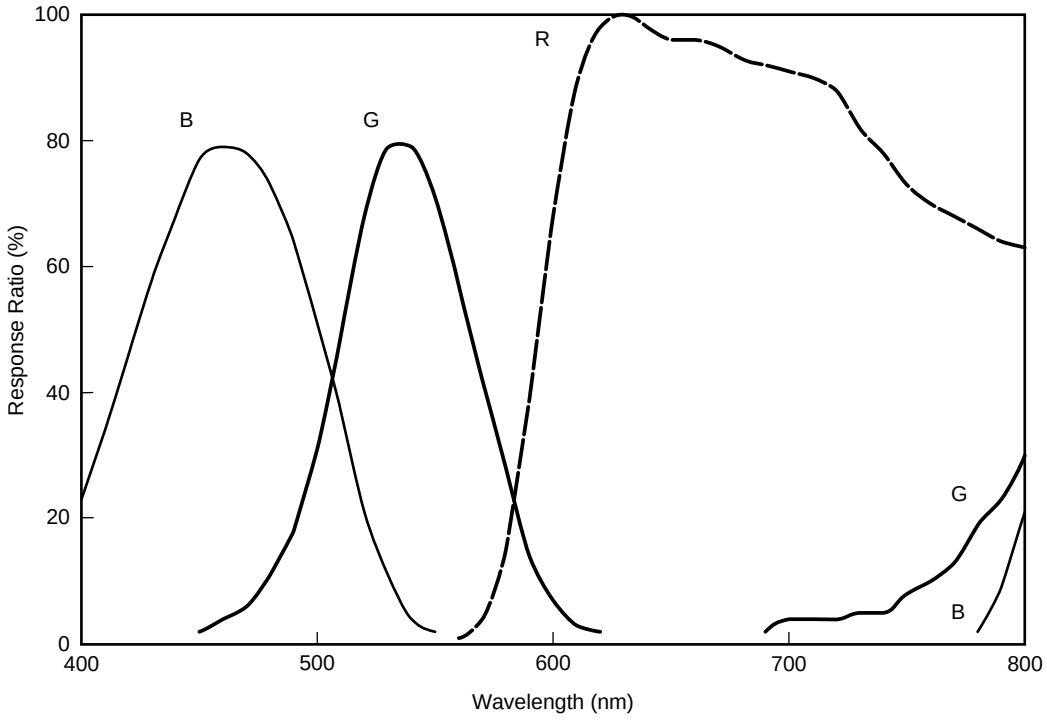
DARK OUTPUT TEMPERATURE CHARACTERISTIC



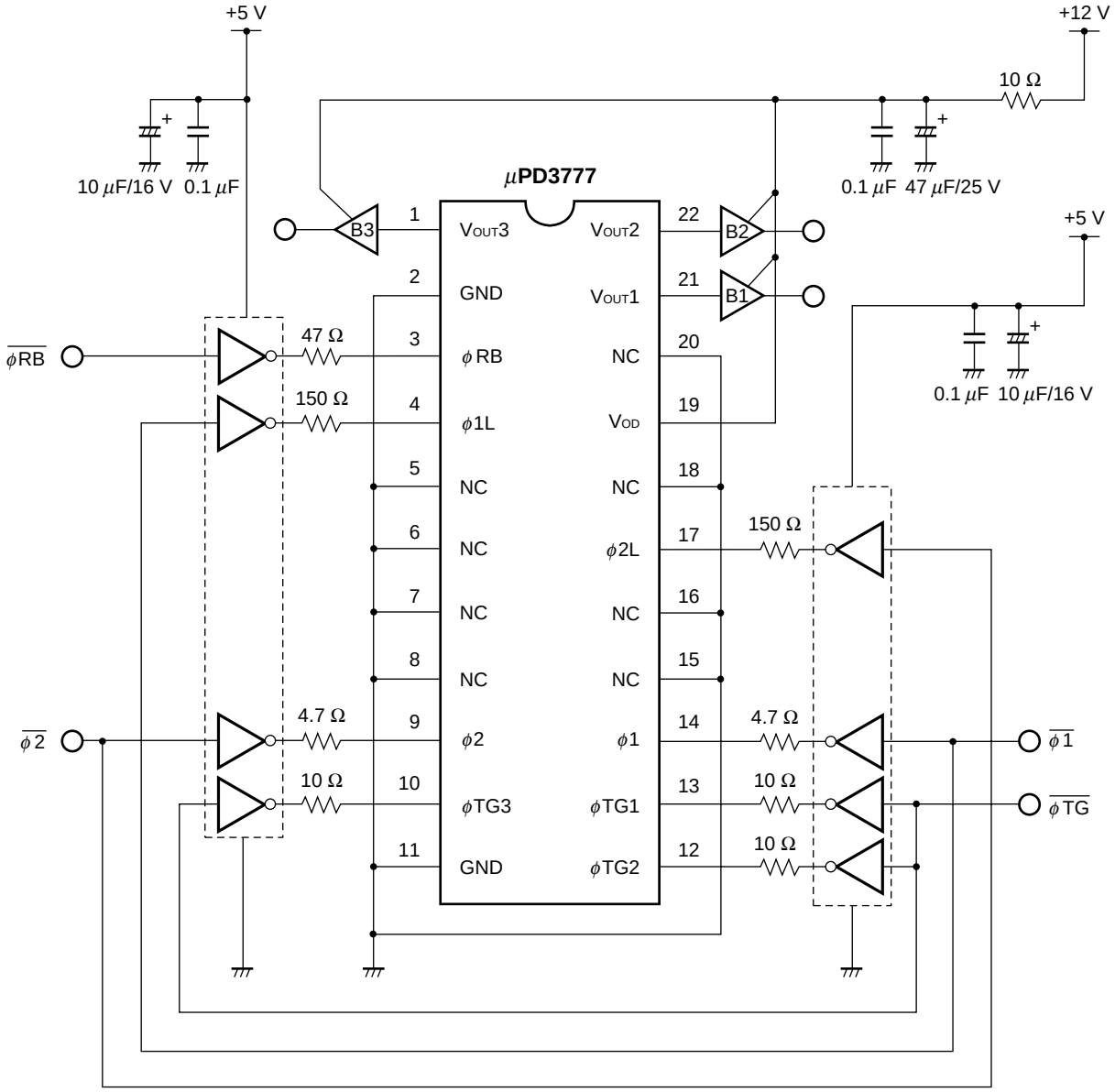
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25 °C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (T_A = +25 °C)

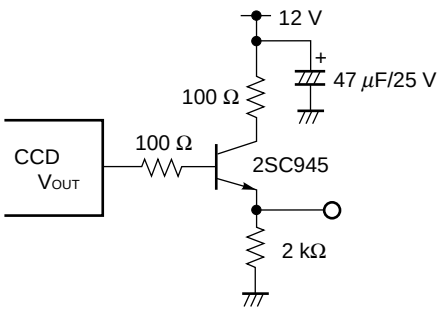


APPLICATION CIRCUIT EXAMPLE



Remark The inverters shown in the above application circuit example are the 74HC04 (data rate < 2 MHz) or the 74AC04 (data rate: 2 to 4 MHz).

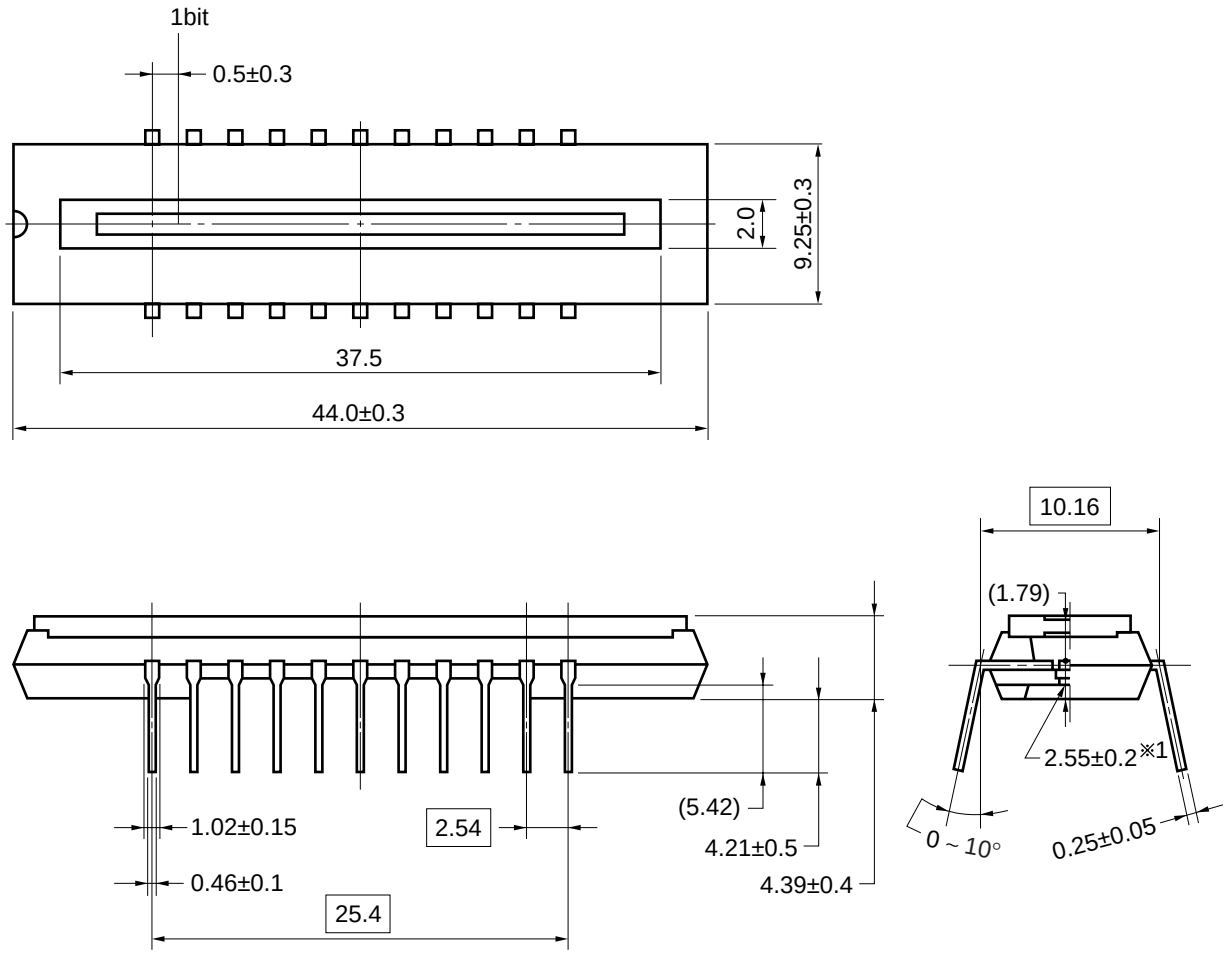
B1 to B3 EQUIVALENT CIRCUIT



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.9 × 8.35 × 0.7※2	1.5

※1 The bottom of the package ←→ The surface of the chip

※2 The thickness of the cap over the chip

22C-1CCD-PKG6-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

Type of Through-hole Device

μPD3777CY : CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

Caution During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

[MEMO]

NOTES ON CLEANING THE PLASTIC CAP

① CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.
The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

② RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap. Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]