

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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**5000 PIXELS  $\times$  3 COLOR CCD LINEAR IMAGE SENSOR**

The  $\mu$ PD3729 is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The  $\mu$ PD3729 has 3 rows of 5000 pixels, and it is a 2-output/color type CCD sensor with 2 rows/color of charge transfer register, which transfers the photo signal electrons of 5000 pixels separately in odd and even pixels. Therefore, it is suitable for 400 dpi/A3 high-speed color digital copiers and so on.

**FEATURES**

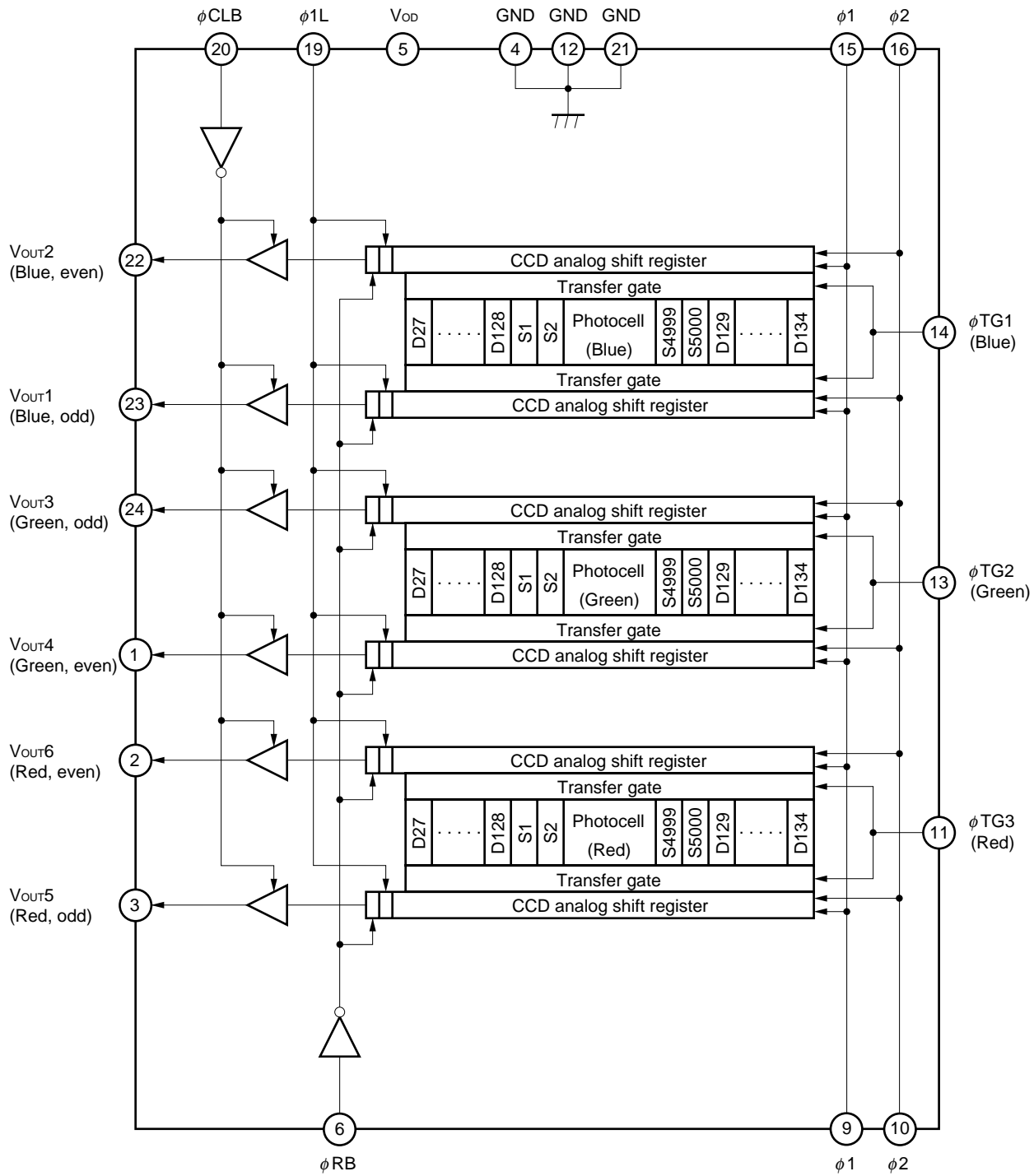
- Valid photocell : 5000 pixels  $\times$  3
- Photocell's pitch : 10  $\mu$ m
- Line spacing : 40  $\mu$ m (4 lines) Red line-Green line, Green line-Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance  $10^7$  lx $\cdot$ hour)
- Resolution : 16 dot/mm (400 dpi) A3 (297  $\times$  420 mm) size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 30 MHz MAX. (15 MHz/1 output)
- Output type : 2 outputs in phase/color
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits  
Voltage amplifiers

**ORDERING INFORMATION**

| Part Number   | Package  |
|---------------|--|
| $\mu$ PD3729D | CCD linear image sensor 24-pin ceramic DIP (400 mil) |

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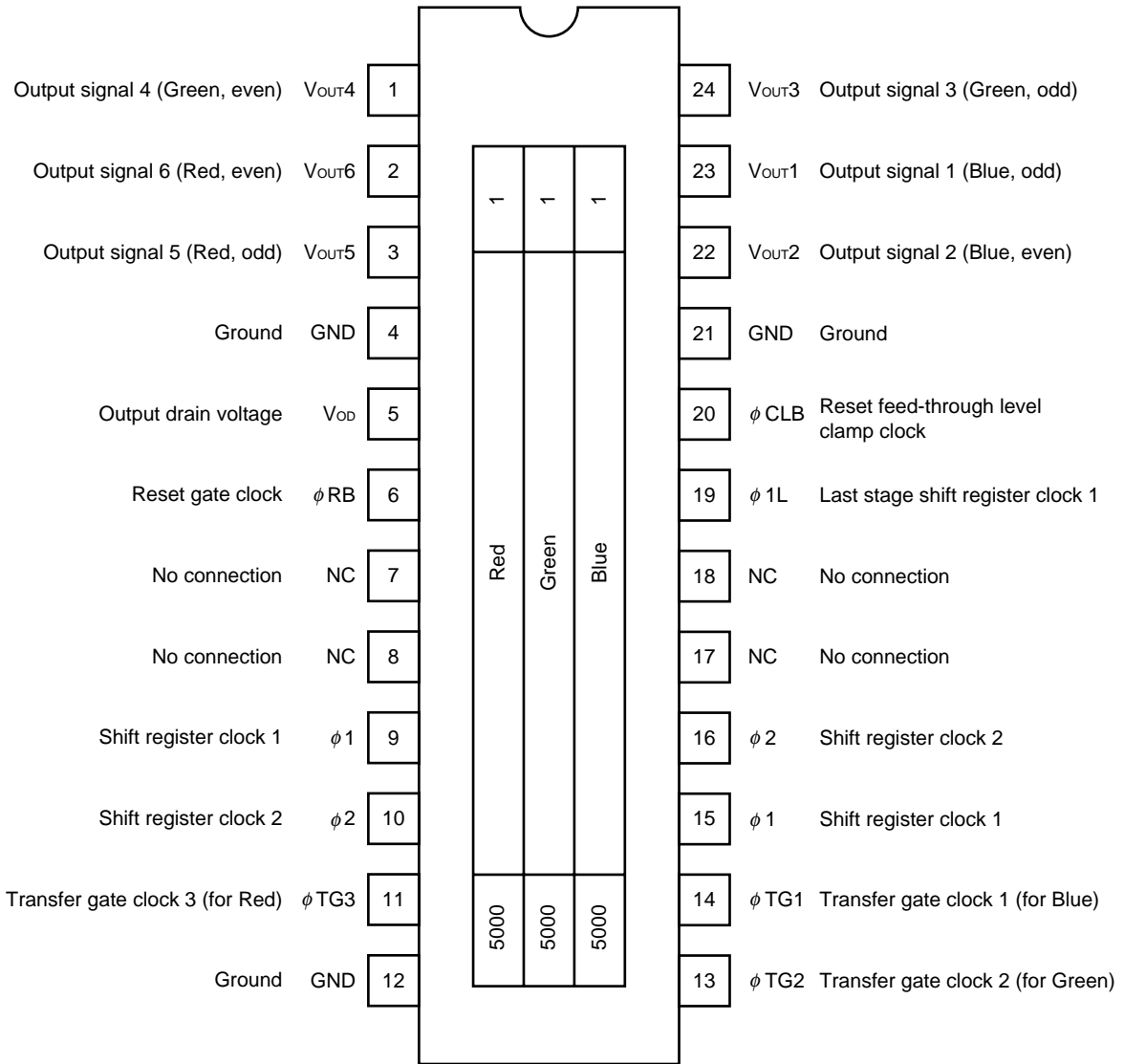
BLOCK DIAGRAM



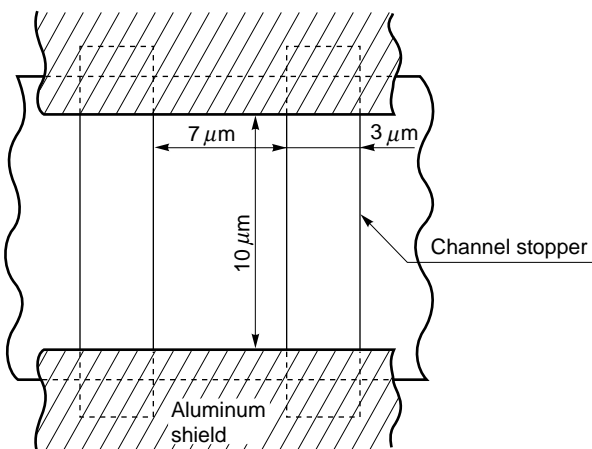
**PIN CONFIGURATION (Top View)**

CCD linear image sensor 24-pin ceramic DIP (400 mil)

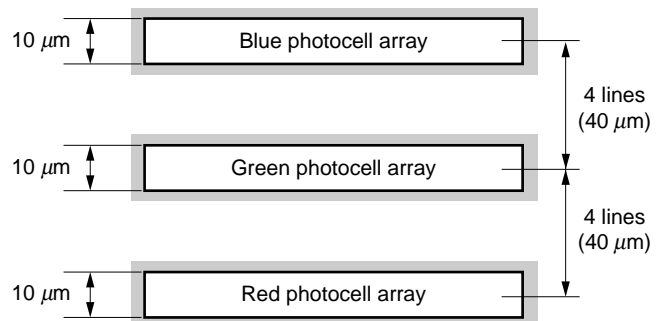
- $\mu$ PD3729D



**PHOTOCELL STRUCTURE DIAGRAM**



**PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)**



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25 °C)**

| Parameter                                    | Symbol   | Ratings     | Unit |
|--|--|-------------|------|
| Output drain voltage                         | V <sub>OD</sub>                                      | -0.3 to +15 | V    |
| Shift register clock voltage                 | V <sub>φ1</sub> , V <sub>φ1L</sub> , V <sub>φ2</sub> | -0.3 to +15 | V    |
| Reset gate clock voltage                     | V <sub>φRB</sub>                                     | -0.3 to +15 | V    |
| Reset feed-through level clamp clock voltage | V <sub>φCLB</sub>                                    | -0.3 to +15 | V    |
| Transfer gate clock voltage                  | V <sub>φTG1</sub> to V <sub>φTG3</sub>               | -0.3 to +15 | V    |
| Operating ambient temperature                | T <sub>A</sub>                                       | -25 to +70  | °C   |
| Storage temperature                          | T <sub>stg</sub>                                     | -40 to +100 | °C   |

**Caution** Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = +25 °C)**

| Parameter                                       | Symbol  | MIN. | TYP.                             | MAX.                             | Unit |
|---|---|------|----------------------------------|----------------------------------|------|
| Output drain voltage                            | V <sub>OD</sub>   | 11.4 | 12.0                             | 12.6                             | V    |
| Shift register clock high level                 | V <sub>φ1H</sub> , V <sub>φ1LH</sub> , V <sub>φ2H</sub> | 4.5  | 5.0                              | 5.5                              | V    |
| Shift register clock low level                  | V <sub>φ1L</sub> , V <sub>φ1LL</sub> , V <sub>φ2L</sub> | -0.3 | 0                                | +0.5                             | V    |
| Reset gate clock high level                     | V <sub>φRBH</sub>                                       | 4.5  | 5.0                              | 5.5                              | V    |
| Reset gate clock low level                      | V <sub>φRBL</sub>                                       | -0.3 | 0                                | +0.5                             | V    |
| Reset feed-through level clamp clock high level | V <sub>φCLBH</sub>                                      | 4.5  | 5.0                              | 5.5                              | V    |
| Reset feed-through level clamp clock low level  | V <sub>φCLBL</sub>                                      | -0.3 | 0                                | +0.5                             | V    |
| Transfer gate clock high level                  | V <sub>φTG1H</sub> to V <sub>φTG3H</sub>                | 4.5  | V <sub>φ1H</sub> <sup>Note</sup> | V <sub>φ1H</sub> <sup>Note</sup> | V    |
| Transfer gate clock low level                   | V <sub>φTG1L</sub> to V <sub>φTG3L</sub>                | -0.3 | 0                                | +0.5                             | V    |
| Data rate                                       | 2f <sub>φRB</sub>                                       | -    | 2                                | 30                               | MHz  |

**Note** When Transfer gate clock high level (V<sub>φTG1H</sub> to V<sub>φTG3H</sub>) is higher than Shift register clock high level (V<sub>φ1H</sub>), Image lag can increase.

**ELECTRICAL CHARACTERISTICS**

( $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{OD} = 12\text{ V}$ ,  $f_{\phi RB} = 1\text{ MHz}$ , data rate = 2 MHz, storage time = 10 ms,  
light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1mm), input signal clock = 5  $V_{p-p}$ )

| Parameter                                | Symbol     | Test Conditions                                | MIN. | TYP. | MAX. | Unit   |
|--|------------|--|------|------|------|--------|
| Saturation voltage                       | $V_{sat}$  |  | 1.5  | 2.0  | –    | V      |
| Saturation exposure                      | Red        | SER  |      | 0.32 |      | lx·s   |
|  | Green      | SEG  |      | 0.37 |      | lx·s   |
|  | Blue       | SEB  |      | 0.29 |      | lx·s   |
| Photo response non-uniformity            | PRNU       | $V_{OUT} = 1\text{ V}$                         |      | 6    | 18   | %      |
| Average dark signal <b>Note 1</b>        | ADS1       | Light shielding                                |      | 1.0  | 5.0  | mV     |
|  | ADS2       |  |      | 0.5  | 5.0  | mV     |
| Dark signal non-uniformity <b>Note 1</b> | DSNU1      | Light shielding                                |      | 2.0  | 5.0  | mV     |
|  | DSNU2      |  |      | 1.0  | 5.0  | mV     |
| Power consumption                        | $P_W$      |  |      | 500  | 700  | mW     |
| Output impedance                         | $Z_O$      |  |      | 0.3  | 0.5  | kΩ     |
| Response                                 | Red        | $R_R$  | 4.3  | 6.2  | 8.1  | V/lx·s |
|  | Green      | $R_G$  | 3.8  | 5.4  | 7.0  | V/lx·s |
|  | Blue       | $R_B$  | 4.7  | 6.8  | 8.9  | V/lx·s |
| Image lag <b>Note 1</b>                  | IL1        | $V_{OUT} = 1\text{ V}$                         |      | 2.0  | 5.0  | %      |
|  | IL2        |  |      | 1.0  | 5.0  | %      |
| Offset level <b>Note 2</b>               | $V_{OS}$   |  | 4.0  | 5.0  | 6.0  | V      |
| Output fall delay time <b>Note 3</b>     | $t_d$      | $V_{OUT} = 1\text{ V}$                         |      | 25   |      | ns     |
| Register imbalance                       | RI         | $V_{OUT} = 1\text{ V}$                         | 0    |      | 4.0  | %      |
| Total transfer efficiency                | TTE        | $V_{OUT} = 1\text{ V}$ ,<br>data rate = 30 MHz | 95   | 98   |      | %      |
| Response peak                            | Red        |  |      | 630  |      | nm     |
|  | Green      |  |      | 540  |      | nm     |
|  | Blue       |  |      | 460  |      | nm     |
| Dynamic range <b>Note 1</b>              | DR11       | $V_{sat} / DSNU1$                              |      | 1000 |      | times  |
|  | DR12       | $V_{sat} / DSNU2$                              |      | 2000 |      | times  |
|  | DR21       | $V_{sat} / \sigma 1$                           |      | 2000 |      | times  |
|  | DR22       | $V_{sat} / \sigma 2$                           |      | 4000 |      | times  |
| Reset feed-through noise <b>Note 2</b>   | RFTN       | Light shielding                                | –500 | +200 | +500 | mV     |
| Random noise <b>Note 1</b>               | $\sigma 1$ | Light shielding                                | –    | 1.0  | –    | mV     |
|  | $\sigma 2$ |  | –    | 0.5  | –    | mV     |

- Notes** 1. ADS1, DSNU1, IL1, DR11 and DR21 show the specification of  $V_{OUT1}$  and  $V_{OUT2}$ .  
ADS2, DSNU2, IL2, DR12 and DR22 show the specification of  $V_{OUT3}$  to  $V_{OUT6}$ .
2. Refer to **TIMING CHART 2**.
3. When the fall time of  $\phi 1L$  ( $t2'$ ) is the TYP. value (refer to **TIMING CHART 2**).

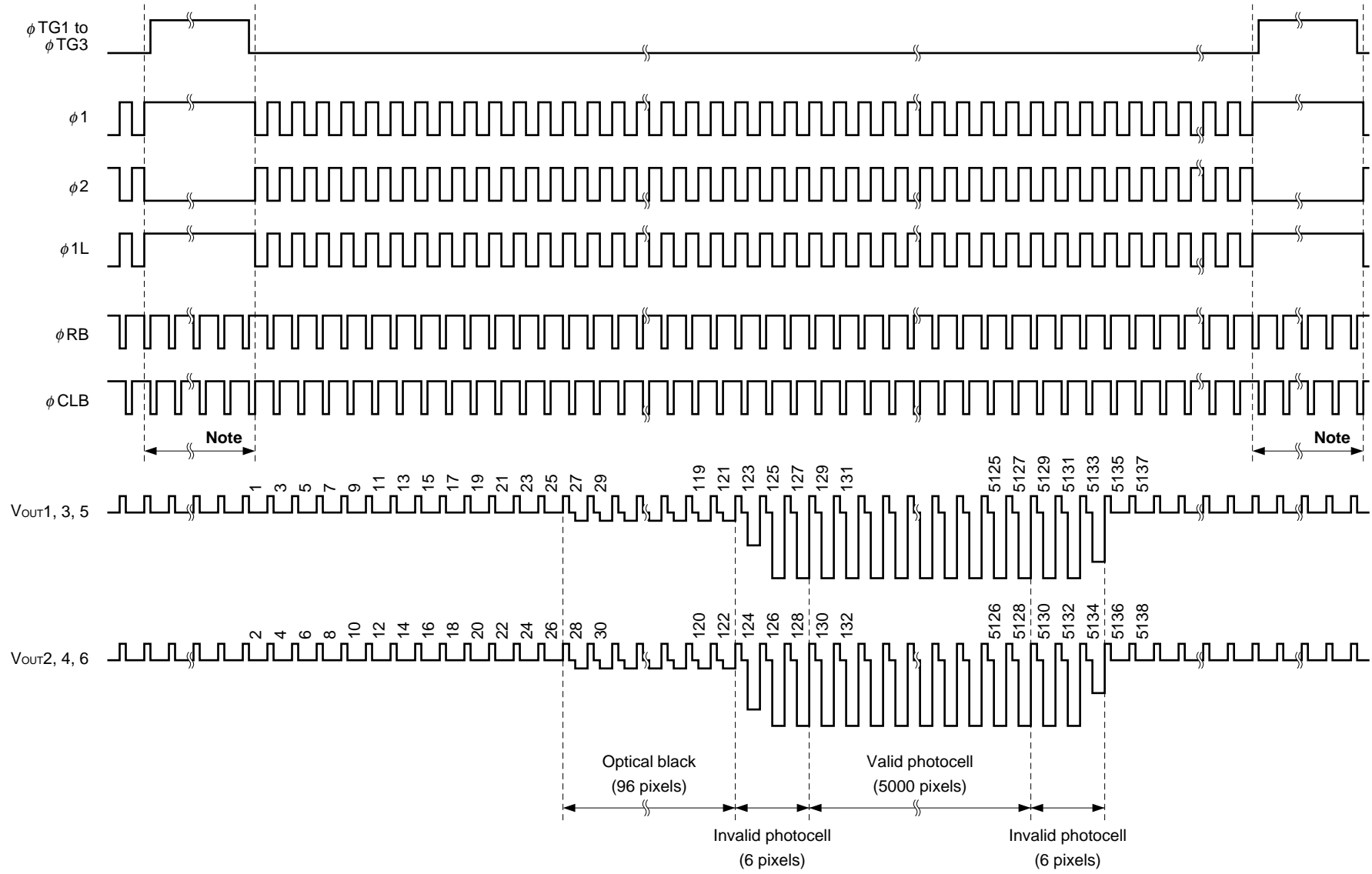
INPUT PIN CAPACITANCE ( $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{OD} = 12\text{ V}$ )

| Parameter  | Symbol         | Pin name   | Pin No.    | MIN. | TYP. | MAX. | Unit |    |
|--|----------------|------------|------------|------|------|------|------|----|
| Shift register clock pin capacitance 1               | $C_{\phi 1}$   | $\phi 1$   | 9          |      | 500  | 800  | pF   |    |
|  |                |            | 15         |      | 500  | 800  | pF   |    |
| Shift register clock pin capacitance 2               | $C_{\phi 2}$   | $\phi 2$   | 10         |      | 500  | 800  | pF   |    |
|  |                |            | 16         |      | 500  | 800  | pF   |    |
| Last stage shift register clock pin capacitance      | $C_{\phi L}$   | $\phi 1L$  | 19         |      | 50   |      | pF   |    |
| Reset gate clock pin capacitance                     | $C_{\phi RB}$  | $\phi RB$  | 6          |      | 50   |      | pF   |    |
| Reset feed-through level clamp clock pin capacitance | $C_{\phi CLB}$ | $\phi CLB$ | 20         |      | 50   |      | pF   |    |
| Transfer gate clock pin capacitance                  | $C_{\phi TG}$  | $\phi TG1$ | 14         |      | 70   |      | pF   |    |
|  |                |            | $\phi TG2$ | 13   |      | 70   |      | pF |
|  |                |            | $\phi TG3$ | 11   |      | 70   |      | pF |

**Remark** Pins 9 and 15 ( $\phi 1$ ), 10 and 16 ( $\phi 2$ ) are each connected inside of the device.

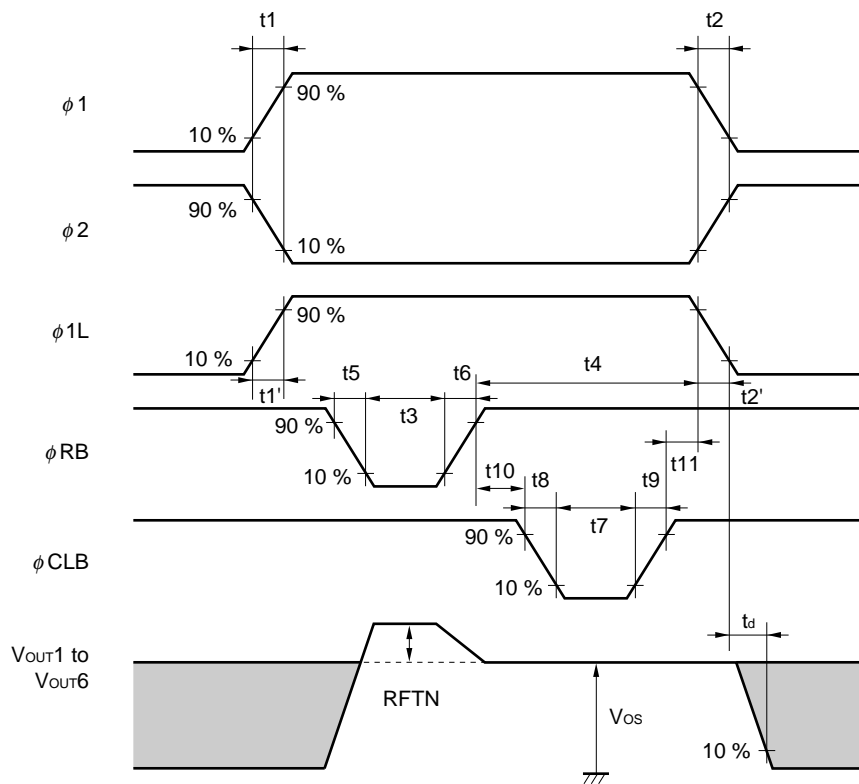


**TIMING CHART 1 (for each color)**

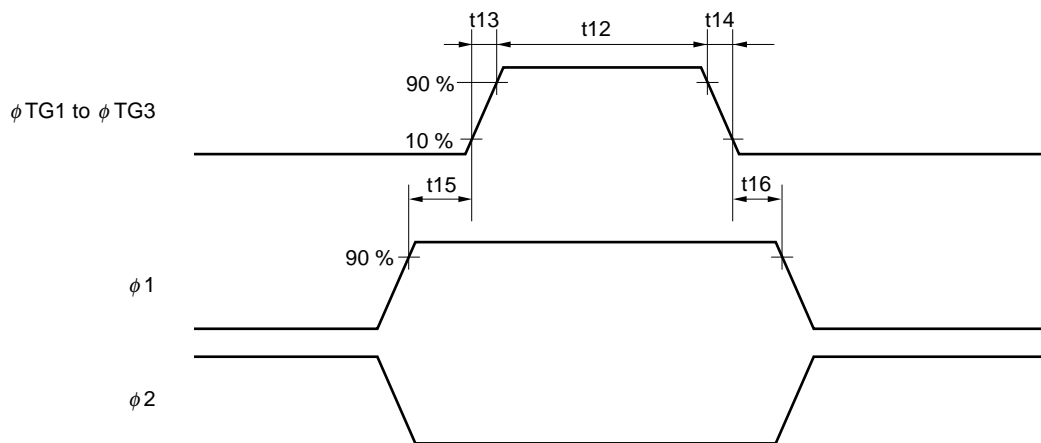


**Note** Input the  $\phi$ RB and  $\phi$ CLB pulses continuously during this period, too.

TIMING CHART 2 (for each color)

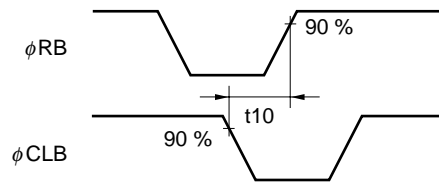


$\phi TG1$  to  $\phi TG3$ ,  $\phi 1$ ,  $\phi 2$  TIMING CHART

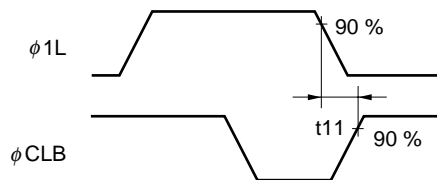


| Symbol   | MIN.                  | TYP.  | MAX. | Unit |
|----------|-----------------------|-------|------|------|
| t1, t2   | 0                     | 50    |      | ns   |
| t1', t2' | 0                     | 5     |      | ns   |
| t3       | 20                    | 50    |      | ns   |
| t4       | 20                    | 100   | –    | ns   |
| t5, t6   | 0                     | 20    |      | ns   |
| t7       | 20                    | 150   |      | ns   |
| t8, t9   | 0                     | 20    |      | ns   |
| t10      | -10 <sup>Note 1</sup> | +50   | –    | ns   |
| t11      | -5 <sup>Note 2</sup>  | +50   |      | ns   |
| t12      | 5000                  | 10000 |      | ns   |
| t13, t14 | 0                     | 50    |      | ns   |
| t15, t16 | 900                   | 1000  |      | ns   |

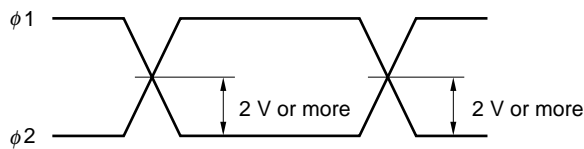
**Notes 1.** MIN. of t10 shows that the φRB and φCLB overlap each other.



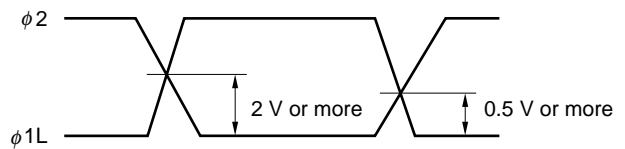
**2.** MIN. of t11 shows that the φ1L and φCLB overlap each other.



**φ1, φ2 cross points**



**φ1L, φ2 cross points**



**Remark** Adjust cross points (φ1, φ2) and (φ1L, φ2) with input resistance of each pin.

**DEFINITIONS OF CHARACTERISTIC ITEMS**

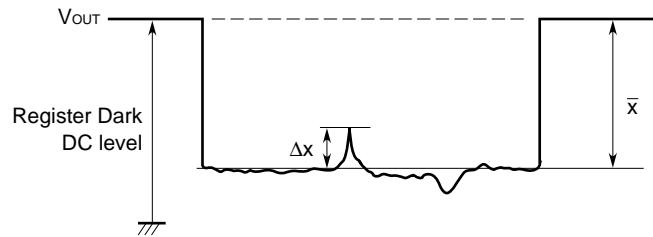
1. Saturation voltage:  $V_{sat}$   
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE  
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU  
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

$\Delta x$  : maximum of  $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{5000} x_j}{5000}$$

$x_j$  : Output voltage of valid pixel number j



4. Average dark signal: ADS  
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{5000} d_j}{5000}$$

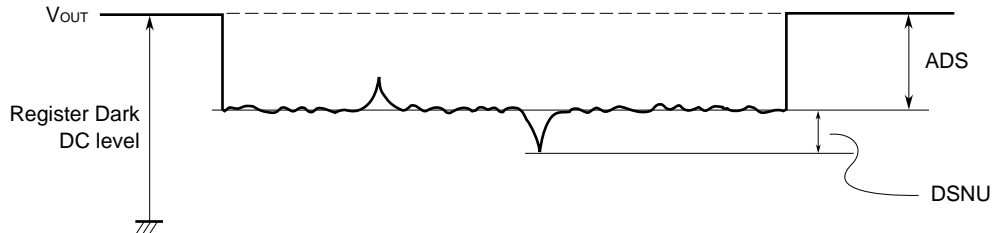
$d_j$  : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV)} : \text{maximum of } |d_j - \text{ADS}|_{j=1 \text{ to } 5000}$$

$d_j$  : Dark signal of valid pixel number  $j$



6. Output impedance:  $Z_o$

Impedance of the output pins viewed from outside.

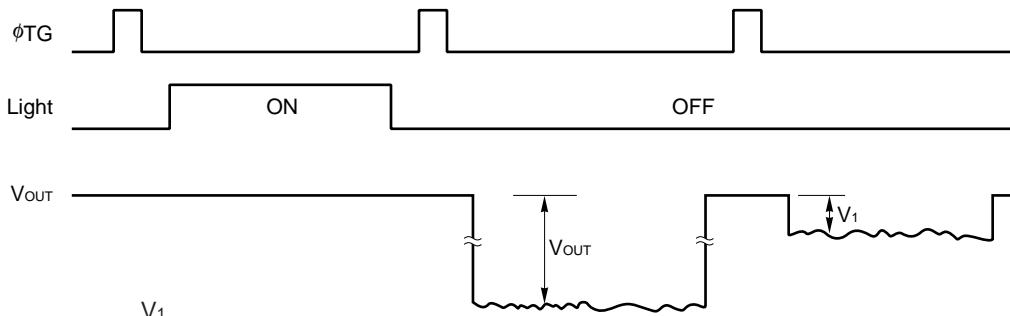
7. Response: R

Output voltage divided by exposure ( $I_x \cdot s$ ).

Note that the response varies with a light source (spectral characteristic).

8. Image lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{\text{OUT}}} \times 100$$

9. Register imbalance: RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

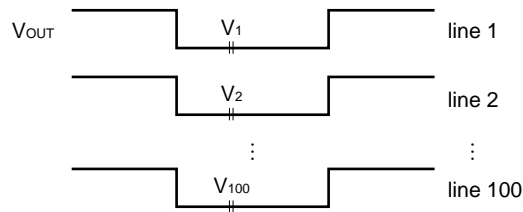
n : Number of valid pixels  
 V<sub>j</sub> : Output voltage of each pixel

10. Random noise: σ

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

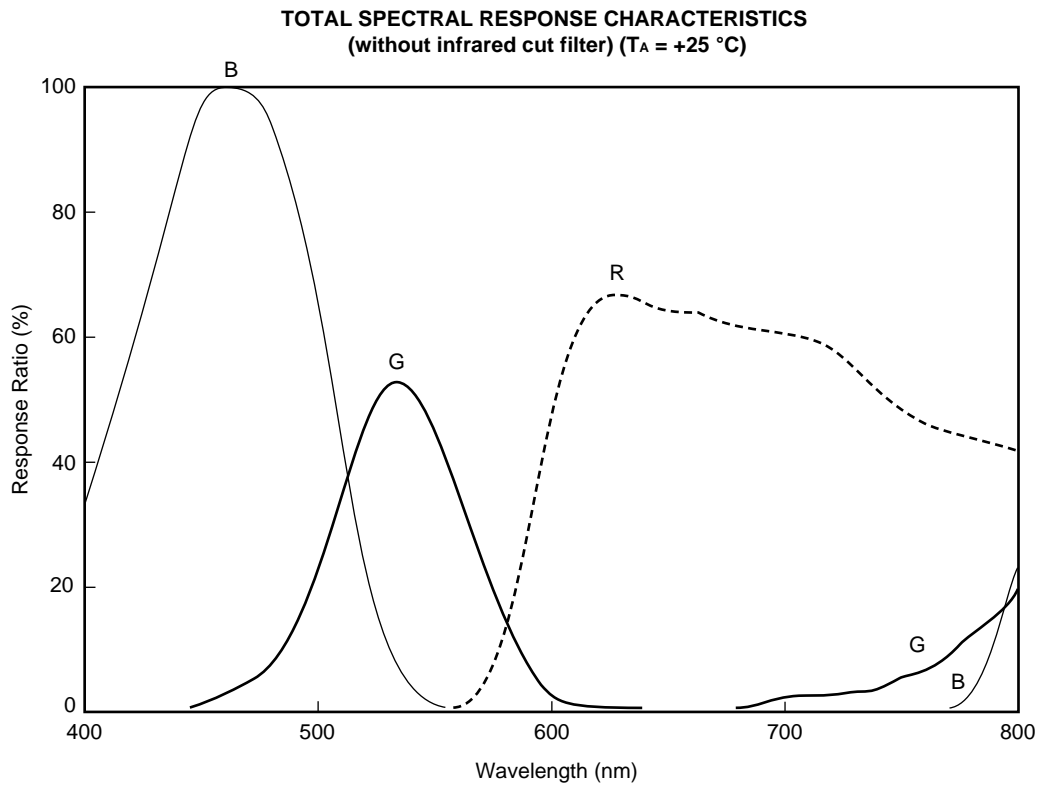
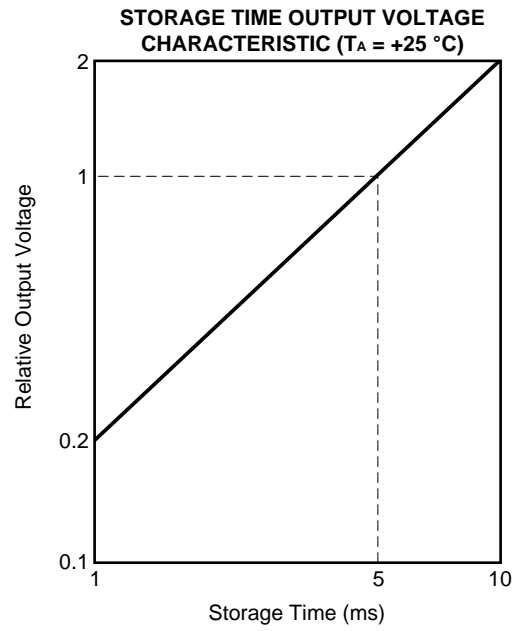
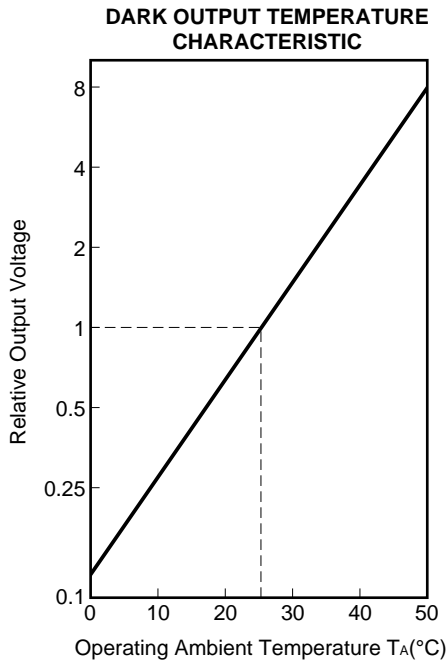
$$\sigma (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V<sub>i</sub>: A valid pixel output signal among all of the valid pixels for each color

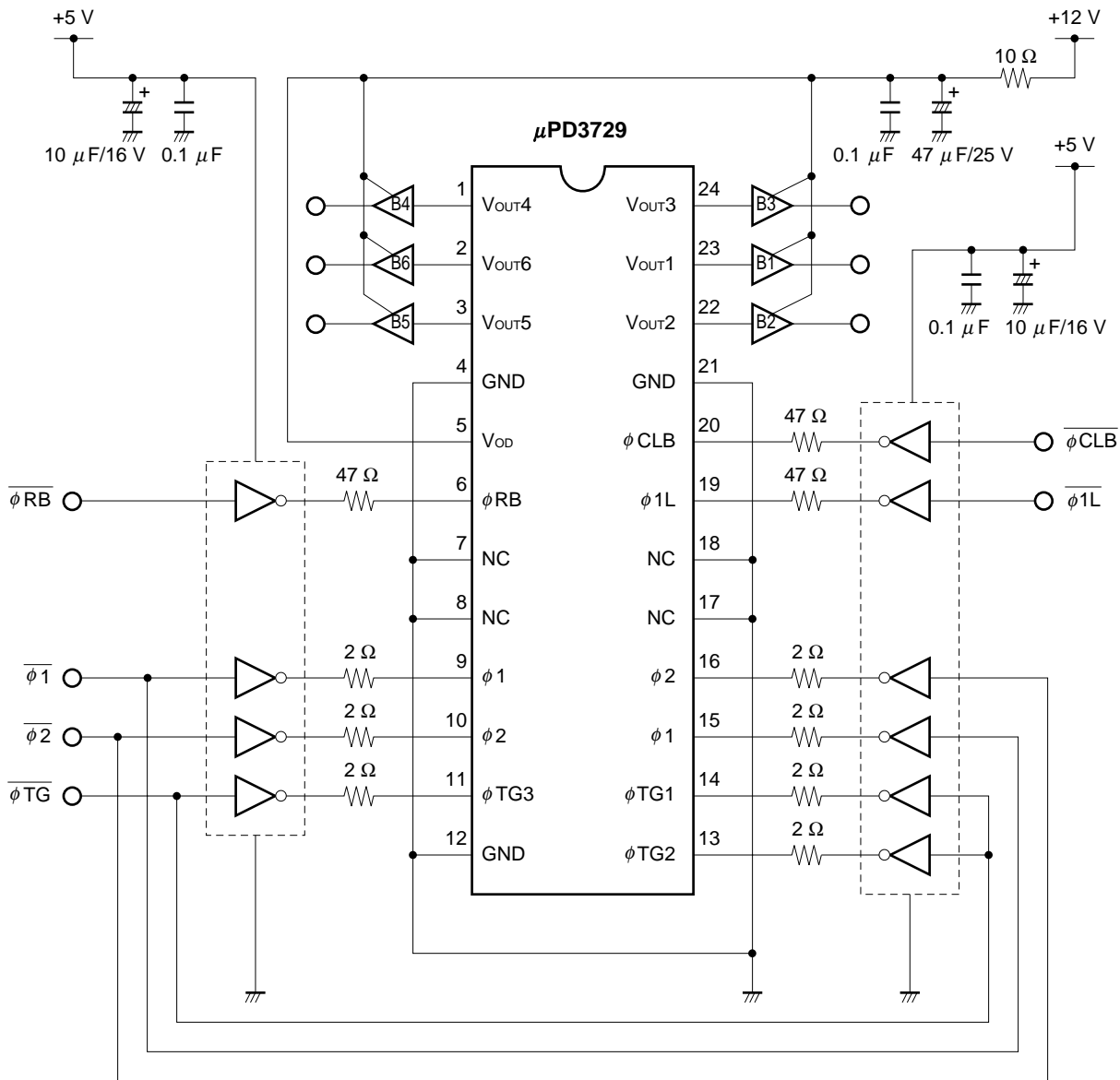


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

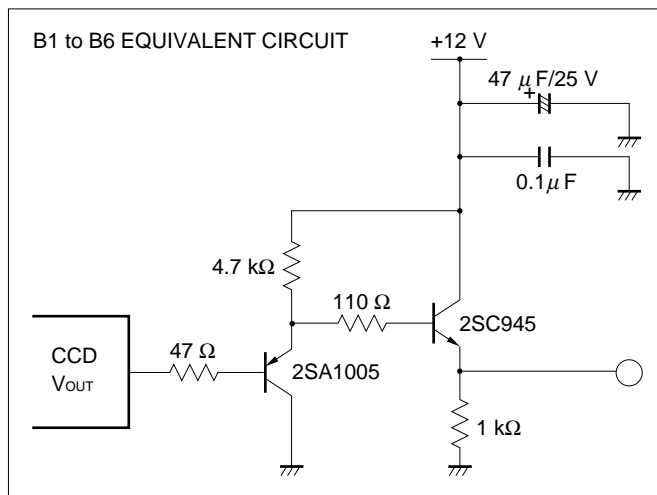
STANDARD CHARACTERISTIC CURVES



APPLICATION CIRCUIT EXAMPLE



**Remark** The inverters shown in the above application circuit example are the 74AC04.

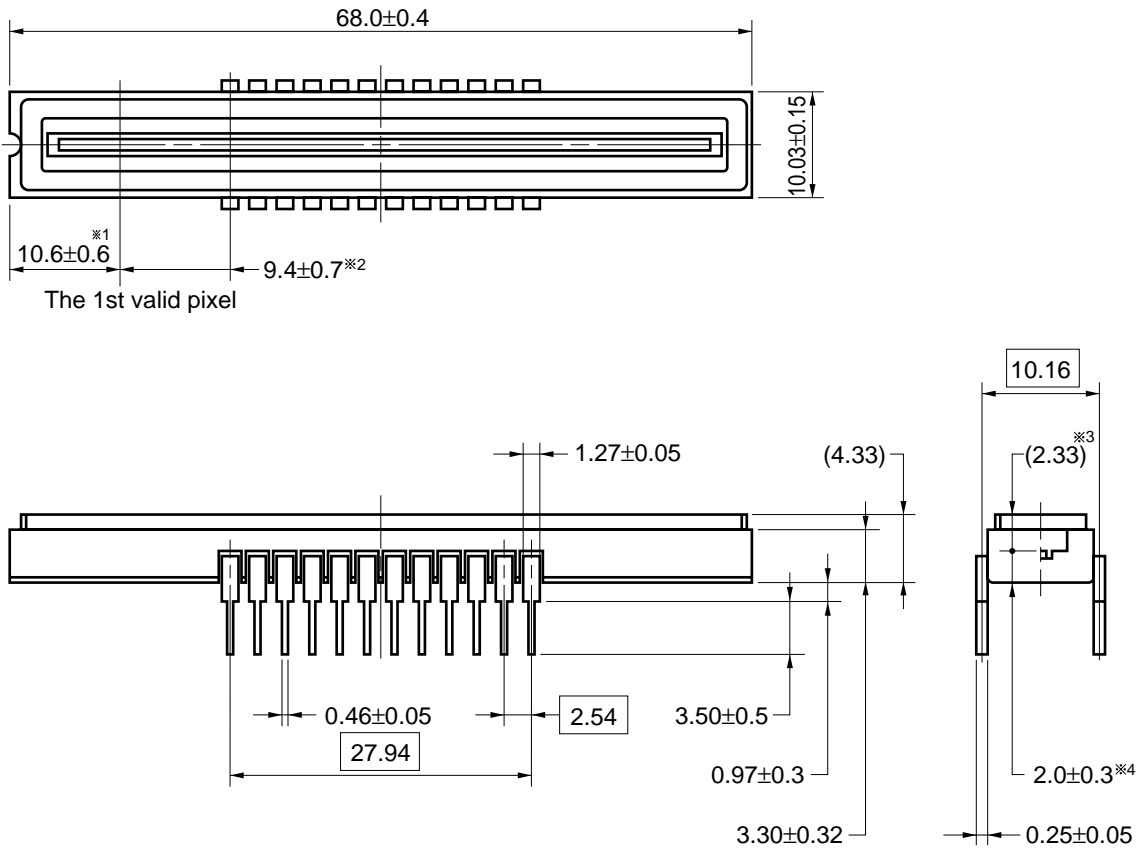




PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 24-PIN CERAMIC DIP (400mil)

(Unit : mm)



| Name      | Dimensions       | Refractive index |
|-----------|------------------|------------------|
| Glass cap | 67.0 × 8.5 × 1.0 | 1.5              |

- ※ 1 The 1st valid pixel ←→ The edge of the package
- ※ 2 The 1st valid pixel ←→ The center of the pin1
- ※ 3 The surface of the chip ←→ The top of the glass cap (Reference)
- ※ 4 The bottom of the package ←→ The surface of the chip

24D-1CCD-PKG1-1

## RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "**Semiconductor Device Mounting Technology Manual**"(C10535E).

### Type of Through-hole Device

$\mu$ PD3729D: CCD linear image sensor 24-pin ceramic DIP (400 mil)

| Process                | Conditions  |
|------------------------|---|
| Partial heating method | Pin temperature: 300 °C or below,<br>Heat time: 3 seconds or less (per pin) |

[MEMO]

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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