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April 1st, 2010
Renesas Electronics Corporation

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NEC

MOS INTEGRATED CIRCUIT

μPD23C128000BL

128M-BIT MASK-PROGRAMMABLE ROM
16M-WORD BY 8-BIT (BYTE MODE) / 8M-WORD BY 16-BIT (WORD MODE)

Description

The μPD23C128000BL is a 134,217,728 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 16,777,216 words by 8 bits, WORD mode : 8,388,608 words by 16 bits). With 44-pin PLASTIC SOP package products, only word mode can be used; it is not possible to switch to byte mode.

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C128000BL is packed in 48-pin PLASTIC TSOP (I) and 44-pin PLASTIC SOP.

Features

- Word organization

  16,777,216 words by 8 bits (BYTE mode) Note

  8,388,608 words by 16 bits (WORD mode) Note

  Note With 44-pin PLASTIC SOP package products, only word mode can be used.
  It is not possible to switch to byte mode.

- Operating supply voltage : V_{CC} = 2.7 to 3.6 V

Operating supply voltage V_{CC}	Access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
3.0 V ± 0.3 V	120	50	30
3.3 V ± 0.3 V	100	55	

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Date Published February 2006 NS CP (K)
Printed in Japan

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Ordering Information

	Part Number	Package
	μPD23C128000BLGY-xxx-MJH	48-pin PLASTIC TSOP(I) (12x18) (Normal bent)
	μPD23C128000BLGY-xxx-MKH	48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)
	μPD23C128000BLGX-xxx	44-pin PLASTIC SOP (15.24 mm (600))
<R>	μPD23C128000BLGY-xxx-MJH-A	48-pin PLASTIC TSOP(I) (12x18) (Normal bent)
<R>	μPD23C128000BLGY-xxx-MKH-A	48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)
<R>	μPD23C128000BLGX-xxx-A	44-pin PLASTIC SOP (15.24 mm (600))

Remarks 1. xxx : ROM code suffix No.

<R> **2.** Products with -A at the end of the part number are lead-free products.

Pin Configurations

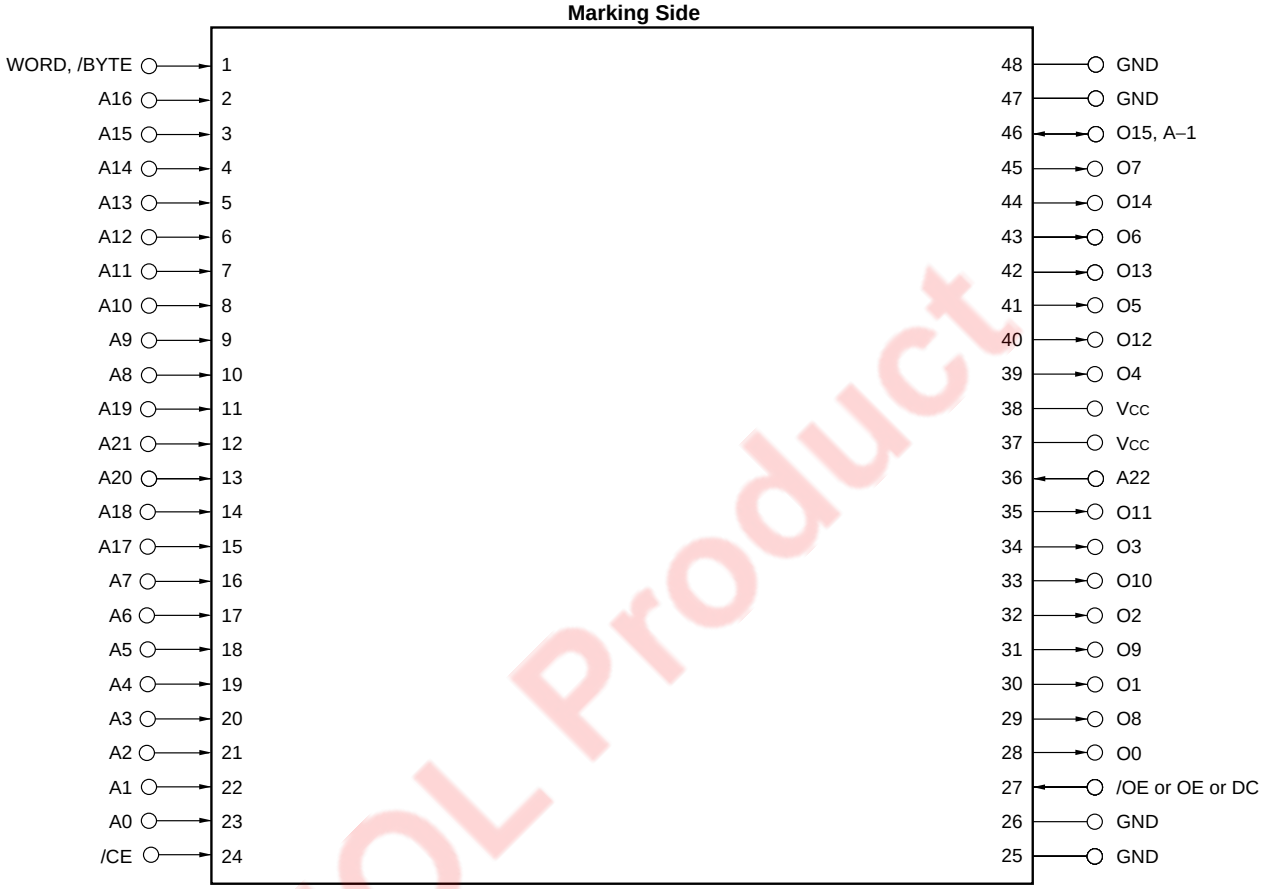
/xxx indicates active low signal.

48-pin PLASTIC TSOP (I) (12x18) (Normal bent)

[μPD23C128000BLGY-xxx-MJH]

<R> **[μPD23C128000BLGY-xxx-MJH-A]**

Marking Side



A0 to A22	:	Address inputs
O0 to O7, O8 to O14	:	Data outputs
O15, A–1	:	Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select input
/CE	:	Chip Enable input
/OE or OE	:	Output Enable input
VCC	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

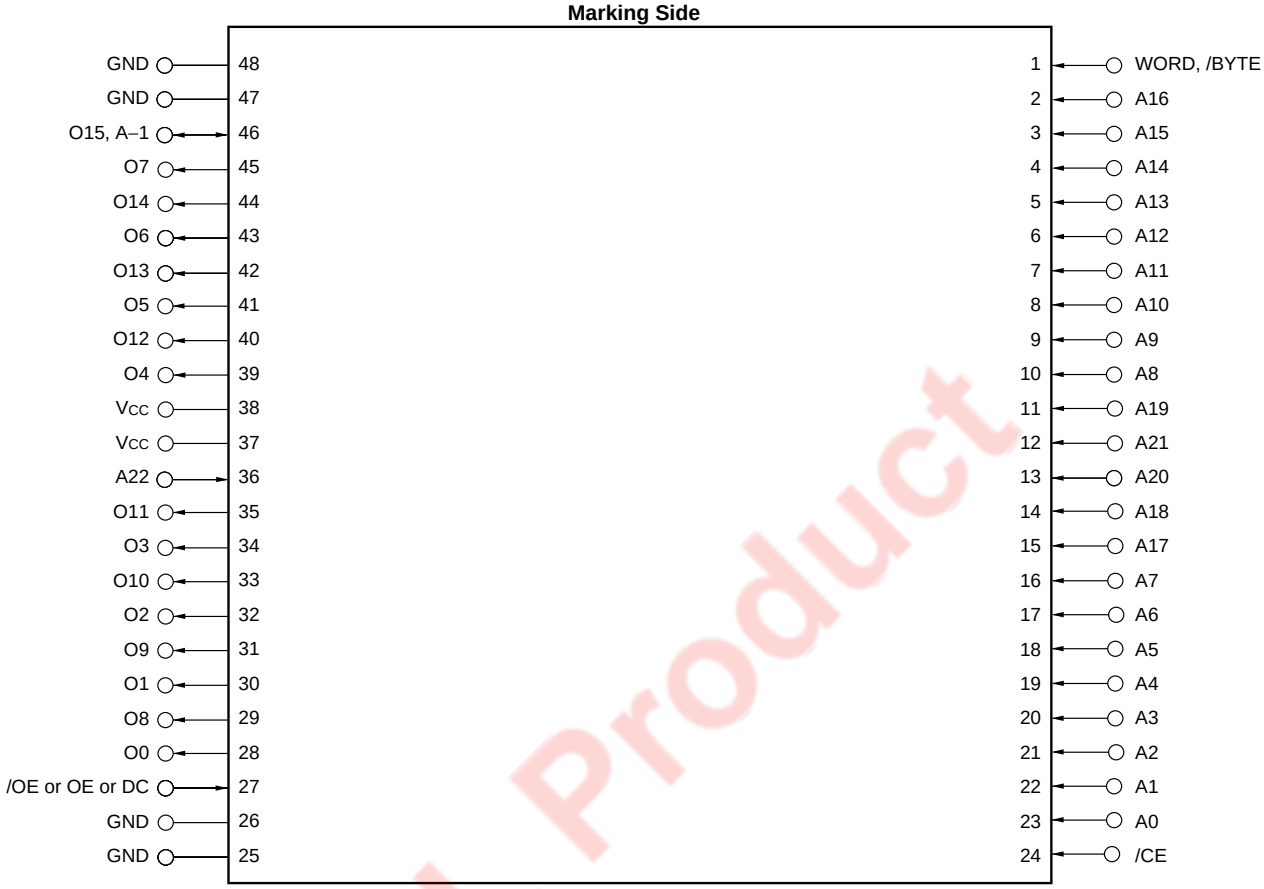
Remark Refer to **Package Drawings** for the 1-pin index mark.

48-pin PLASTIC TSOP (I) (12x18) (Reverse bent)

[μPD23C128000BLGY-xxx-MKH]

<R> **[μPD23C128000BLGY-xxx-MKH-A]**

Marking Side



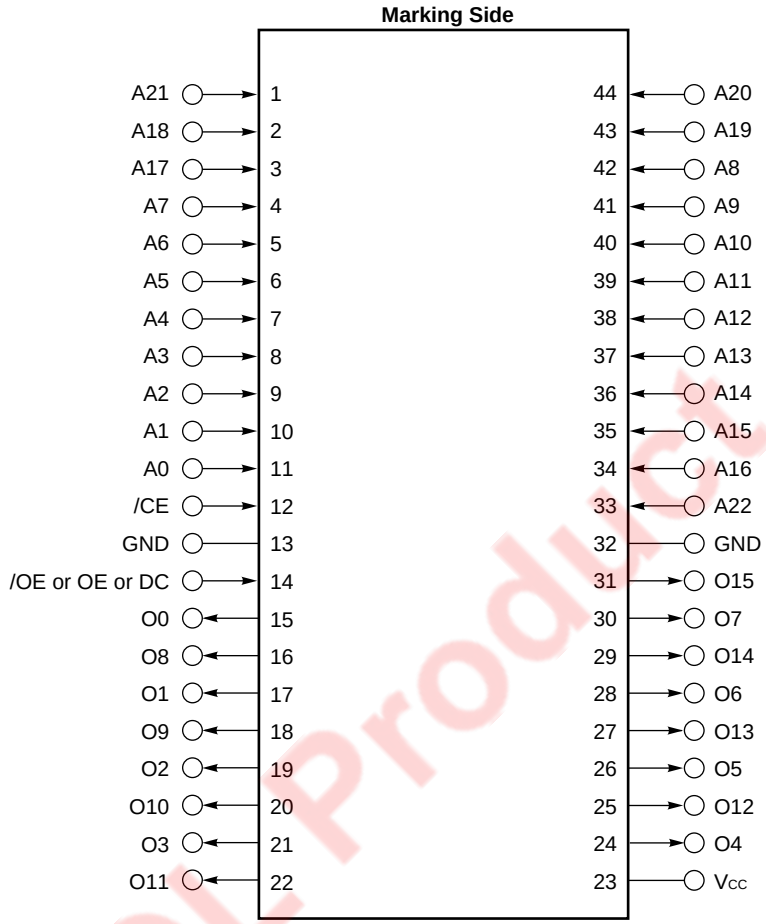
A0 to A22	:	Address inputs
O0 to O7, O8 to O14	:	Data outputs
O15, A–1	:	Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select input
/CE	:	Chip Enable input
/OE or OE	:	Output Enable input
VCC	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

Remark Refer to **Package Drawings** for the 1-pin index mark.

44-pin PLASTIC SOP (15.24 mm (600))

[μPD23C128000BLGX-xxx]

<R> **[μPD23C128000BLGX-xxx-A]**



A0 to A22	:	Address inputs
O0 to O15	:	Data outputs
/CE	:	Chip Enable
/OE or OE	:	Output Enable
V_{CC}	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

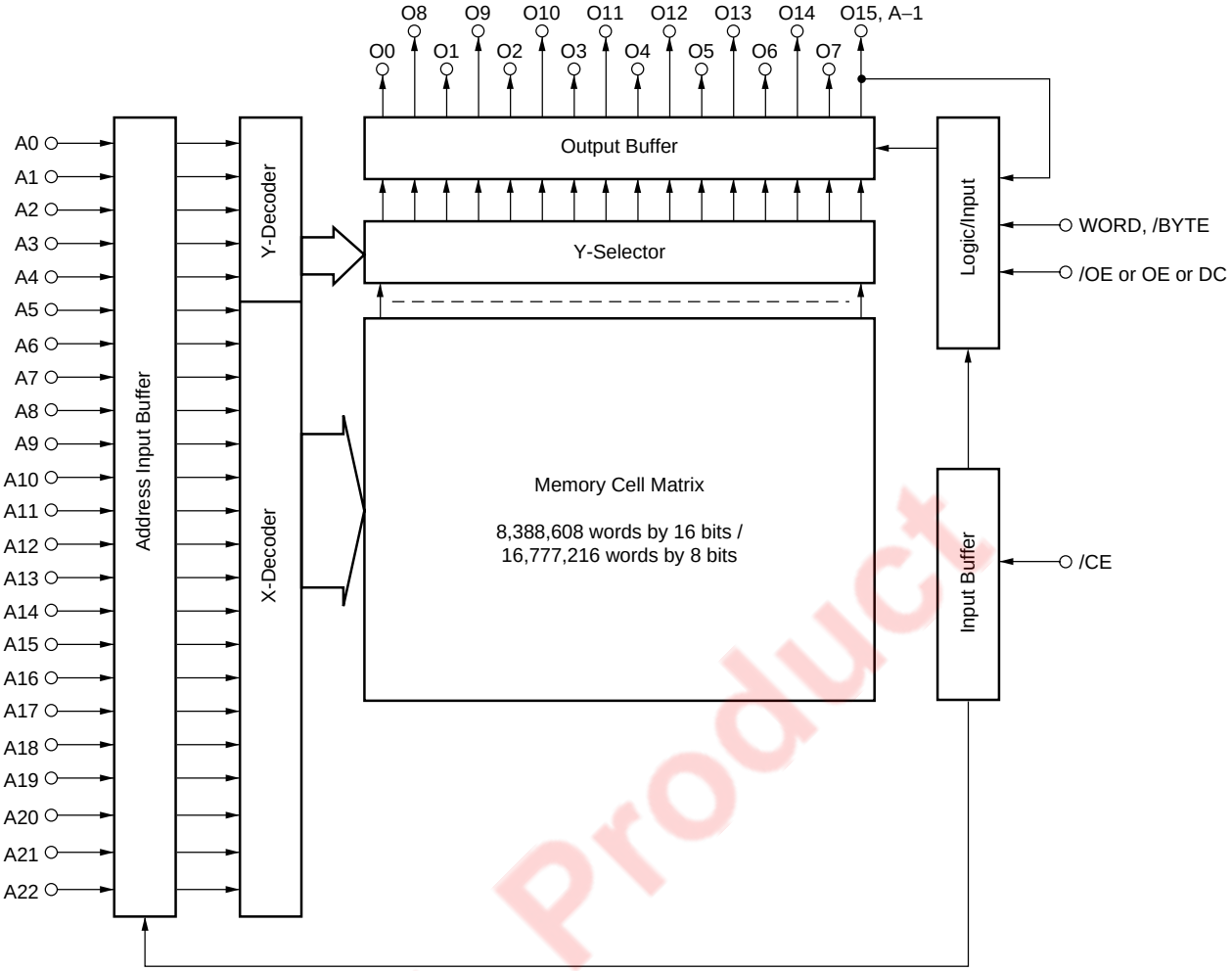
Remarks 1. Refer to **Package Drawings** for the 1-pin index mark.

2. With 44-pin PLASTIC SOP package products, only word mode (8,388,608 words x 16 bits) can be used. There is no mode select (WORD, /BYTE) pin.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. **High level** : WORD mode (8M-word by 16-bit) **Low level** : BYTE mode (16M-word by 8-bit)
A0 to A22 (Address inputs)	Input	Address input pins. A0 to A22 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** A0 to A22 are used as 23 bits address signals. **BYTE mode (16M-word by 8-bit)** A0 to A22 are used as the upper 23 bits of total 24 bits of address signal. (The least significant bit (A–1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.) **BYTE mode (16M-word by 8-bit)** 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A–1 (Data output 15, LSB Address input)	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** The most significant output data bus (O15). **BYTE mode (16M-word by 8-bit)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High-Z **Low level** : Data out
/OE or OE or DC (Output Enable, Don't Care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground

Block Diagram



Mask Option

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High-Z
H	H or L	Standby	High-Z

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	H		Data out
H	H or L	Standby	High-Z

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High-Z

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC}+0.3	V
Output voltage	V_O		–0.3 to V_{CC}+0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}			2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}	V_{CC} = 3.0 V ± 0.3 V		–0.3		+0.5	V
		V_{CC} = 3.3 V ± 0.3 V		–0.3		+0.8	
High level output voltage	V_{OH}	I_{OH} = –100 μA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA				0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}		–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected		–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode),	V_{CC} = 3.0 V ± 0.3 V			50	mA
		I_O = 0 mA	V_{CC} = 3.3 V ± 0.3 V			55	
Standby current	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)				30	μA

AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test condition	V_{CC} = 3.0 V ± 0.3 V			V_{CC} = 3.3 V ± 0.3 V			Unit
			MIN	TYP.	MAX.	MIN	TYP.	MAX.	
Address access time	t_{ACC}				120			100	ns
Address skew time	t_{SKEW}	**Note**			10			10	ns
Chip enable access time	t_{CE}				120			100	ns
Output enable access time	t_{OE}				25			25	ns
Output hold time	t_{OH}		0			0			ns
Output disable time	t_{DF}		0		20	0		20	ns
WORD, /BYTE access time	t_{WB}				120			100	ns

Note t_{SKEW} indicates the following three types of time depending on the condition.

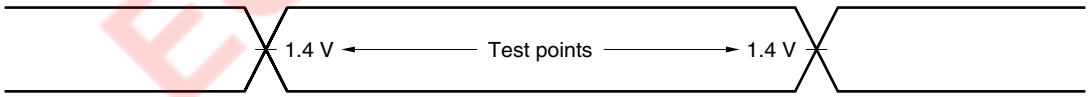
1) When switching /CE from high level to low level, t_{SKEW} is the time from the /CE low level input point until the next address is determined.
2) When switching /CE from low level to high level, t_{SKEW} is the time from the address change start point to the /CE high level input point.
3) When /CE is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CE is active, t_{SKEW} is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

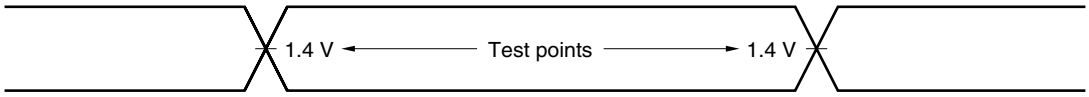
Remark t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

AC Test Conditions

Input waveform (Rise / Fall Time ≤ 5 ns)



Output waveform



Output load

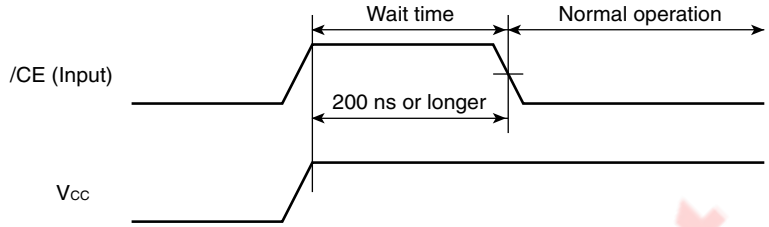
1TTL + 100 pF

Cautions on power application

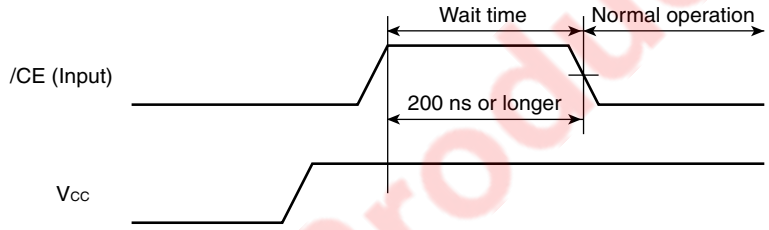
To ensure normal operation, always apply power using /CE following the procedure shown below.

1) Input a high level to /CE during and after power application.
2) Hold the high level input to /CE for 200 ns or longer (wait time).
3) Start normal operation after the wait time has elapsed.

Power Application Timing Chart 1 (When /CE is made high at power application)

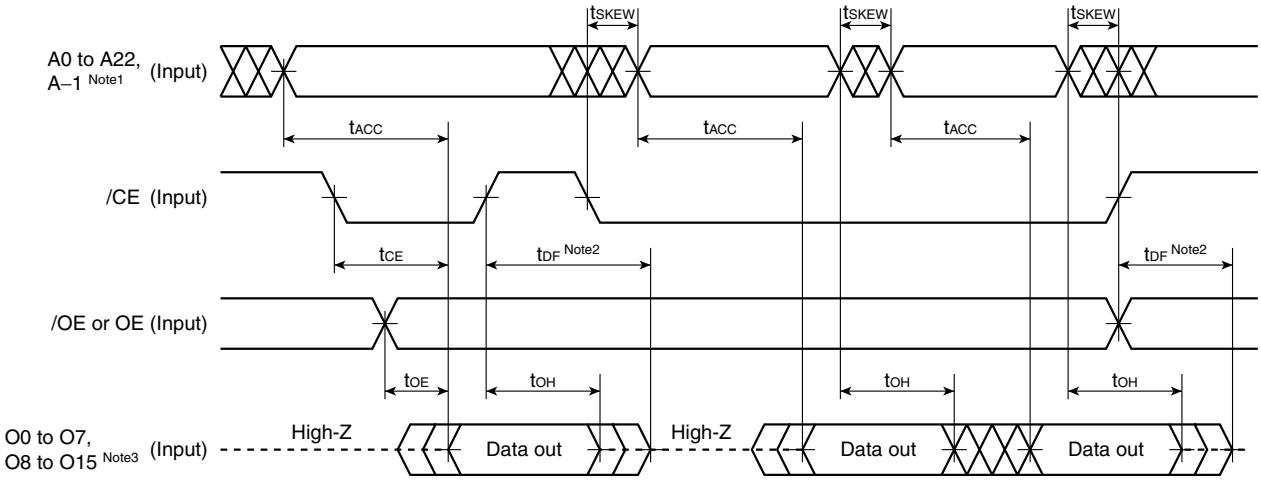


Power Application Timing Chart 2 (When /CE is made high after power application)



Caution Other signals can be either high or low during the wait time.

Read Cycle Timing Chart

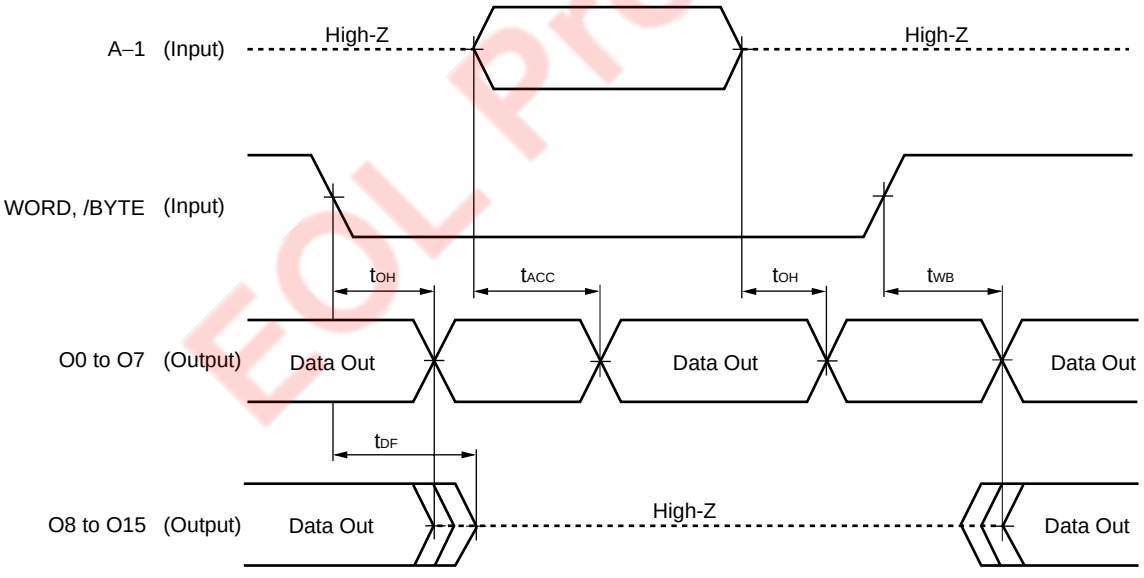


Notes 1. During WORD mode, A–1 is O15.

2. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

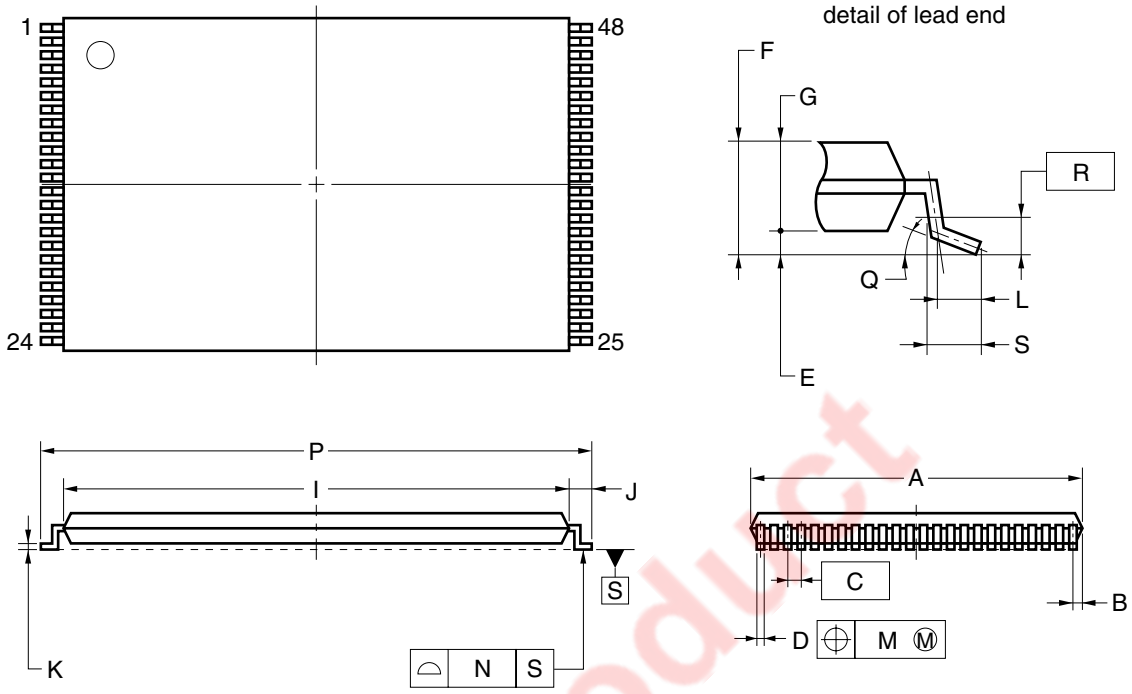
WORD, /BYTE Switch Timing Chart



Remark Chip Enable (/CE) and Output Enable (/OE or OE) : Active.

Package Drawings

48-PIN PLASTIC TSOP(I) (12x18)



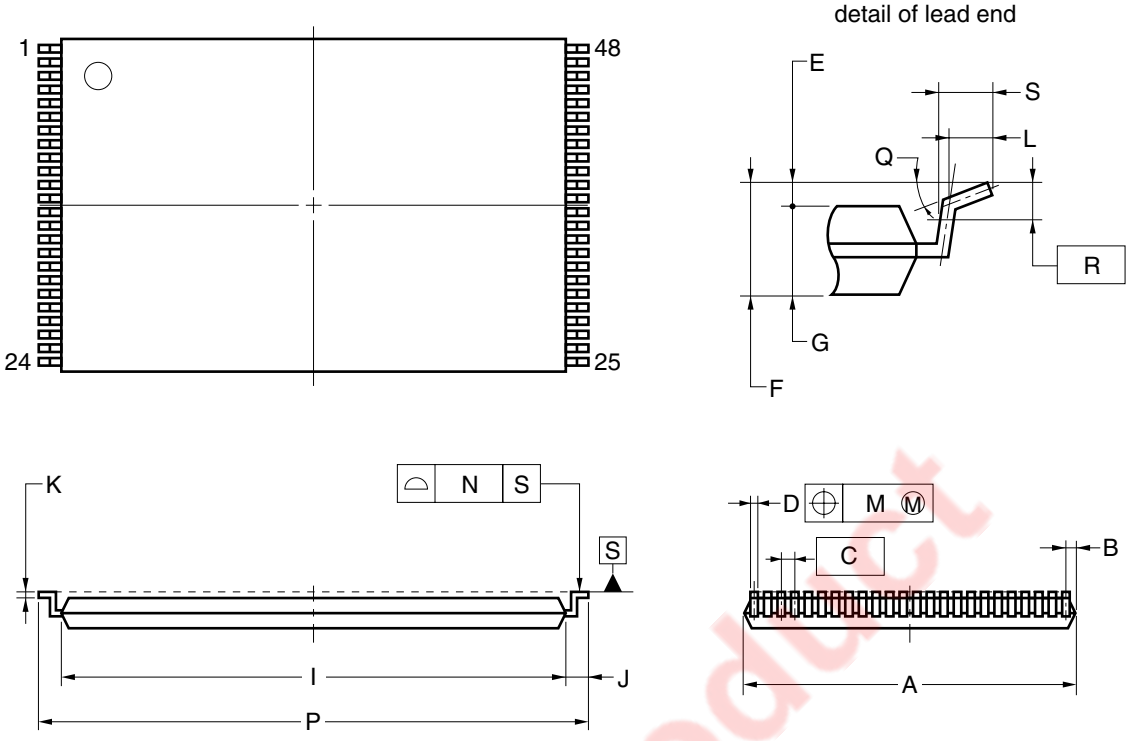
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

48-PIN PLASTIC TSOP(I) (12x18)



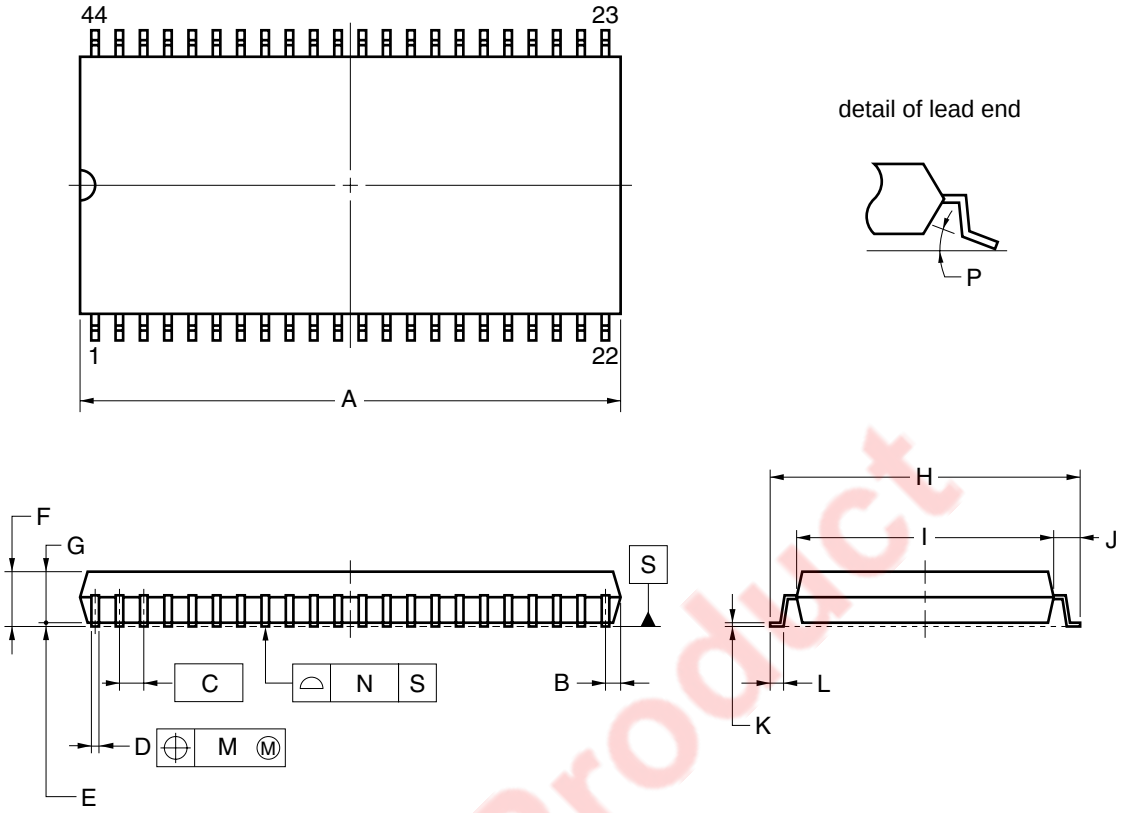
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MKH1-1

44-PIN PLASTIC SOP (15.24 mm (600))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$27.83^{+0.4}_{-0.05}$
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.15±0.1
F	3.0 MAX.
G	2.7±0.05
H	16.04±0.3
I	13.24±0.1
J	1.4±0.2
K	$0.22^{+0.08}_{-0.07}$
L	0.8±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P44GX-50-600A-4

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C128000BL.

Types of Surface Mount Device

μPD23C128000BLGY-xxx-MJH : 48-pin PLASTIC TSOP(I) (12x18) (Normal bent)

μPD23C128000BLGY-xxx-MKH : 48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)

μPD23C128000BLGX-xxx : 44-pin PLASTIC SOP (15.24 mm (600))

<R> μPD23C128000BLGY-xxx-MJH-A : 48-pin PLASTIC TSOP(I) (12x18) (Normal bent)

<R> μPD23C128000BLGY-xxx-MKH-A : 48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)

<R> μPD23C128000BLGX-xxx-A : 44-pin PLASTIC SOP (15.24 mm (600))

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
4th edition/ Feb. 2006	p.2	p.1	Addition	Ordering Information	Lead-free products have been added
	pp.3-5	pp.2-4	Addition	Pin Configuration	Lead-free products have been added
	p.16	p.15	Addition	Recommended Soldering Conditions	Lead-free products have been added

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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