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## 4-BIT SINGLE-CHIP MICROCONTROLLER FOR SMALL GENERAL-PURPOSE INFRARED REMOTE CONTROLLER

### DESCRIPTION

The μPD17P246 is a model of the μPD17246 with a one-time PROM instead of an internal mask ROM.

Since the user can write programs to the μPD17P246, it is ideal for experimental production or small-scale production of the μPD17240, 17241, 17242, 17243, 17244, 17245, or 17246 systems.

When reading this document, also read the documents related to the μPD17240, 17241, 17242, 17243, 17244, 17245, and 17246.

**Detailed function descriptions are provided in the following user's manual. Be sure to read them before designing.**

μPD172×× Subseries User's Manual: U12795E

### FEATURES

- Pin compatible with μPD17240, 17241, 17242, 17243, 17244, 17245, and 17246 (except PROM programming function)
- Carrier generator for infrared remote controller (REM output)
- 17K architecture: General-purpose register method
- Program memory (one-time PROM): 32 KB (16,384 × 16)
- Data memory (RAM): 447 × 4 bits  
RAM retention detector
- Low-voltage detector
- Supply voltage:  $V_{DD} = 2.2$  to 3.6 V (4 μs)

### APPLICATIONS

Preset remote controllers, toys, and portable systems

### ★ ORDERING INFORMATION

Part Number	Package
μPD17P246M1MC-5A4	30-pin plastic SSOP (7.62 mm (300))

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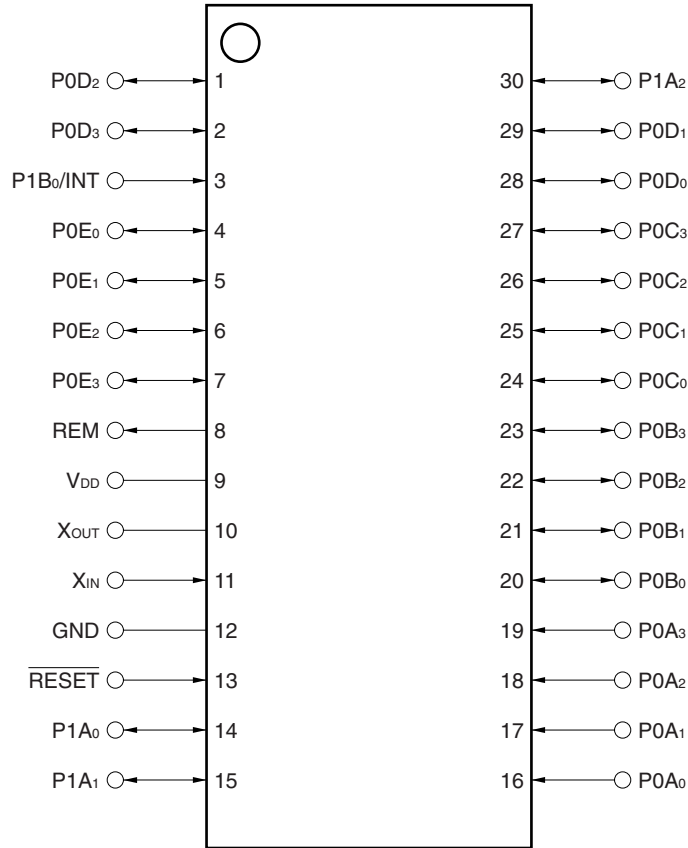
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

**PIN CONFIGURATION (TOP VIEW)**

**(1) Normal operating mode**

**• 30-pin plastic SSOP (7.62 mm (300))**

μPD17P246M1MC-5A4

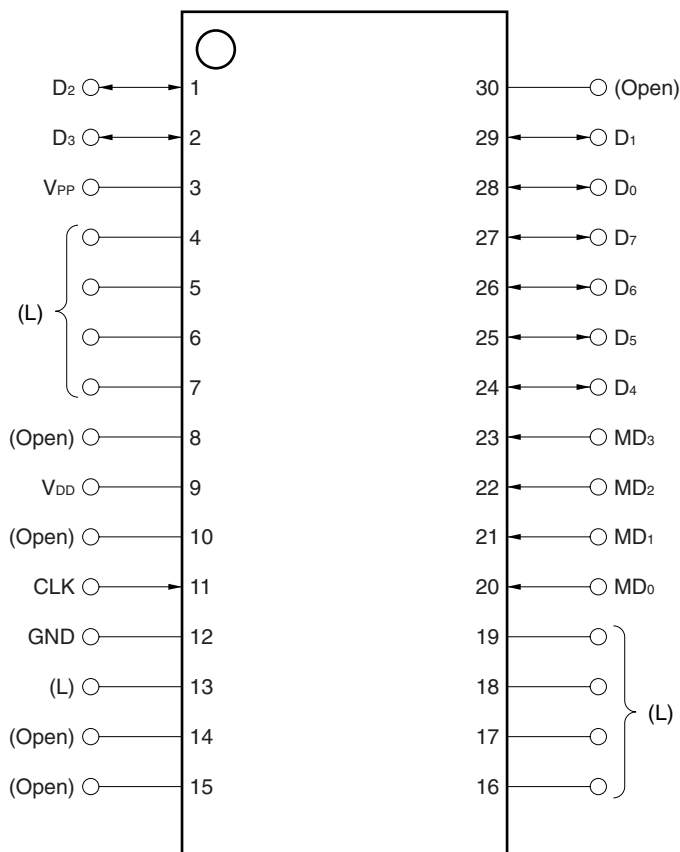


- GND: Ground
- INT: External interrupt request signal input
- P0A0 to P0A3: Input port (CMOS input with pull-up resistor)
- P0B0 to P0B3: I/O port (CMOS input with pull-up resistor/N-ch open-drain output)
- P0C0 to P0C3: I/O port (CMOS input with pull-up resistor/N-ch open-drain output)
- P0D0 to P0D3: I/O port (CMOS input with pull-up resistor/N-ch open-drain output)
- P0E0 to P0E3: I/O port (when key matrix is used: CMOS input with pull-up resistor/N-ch open-drain output, when key matrix is not used: CMOS input/push-pull output)
- P1A0 to P1A2: I/O port (when key matrix is used: CMOS input/N-ch open-drain output, when key matrix is not used: CMOS input/push-pull output)
- P1B0: Input port (CMOS input)
- REM: Remote controllers output (CMOS push-pull output)
- RESET: Reset input
- VDD: Power supply
- XIN, XOUT: Resonator connection

(2) PROM programming mode

• 30-pin plastic SSOP (7.62 mm (300))

μPD17P246M1MC-5A4



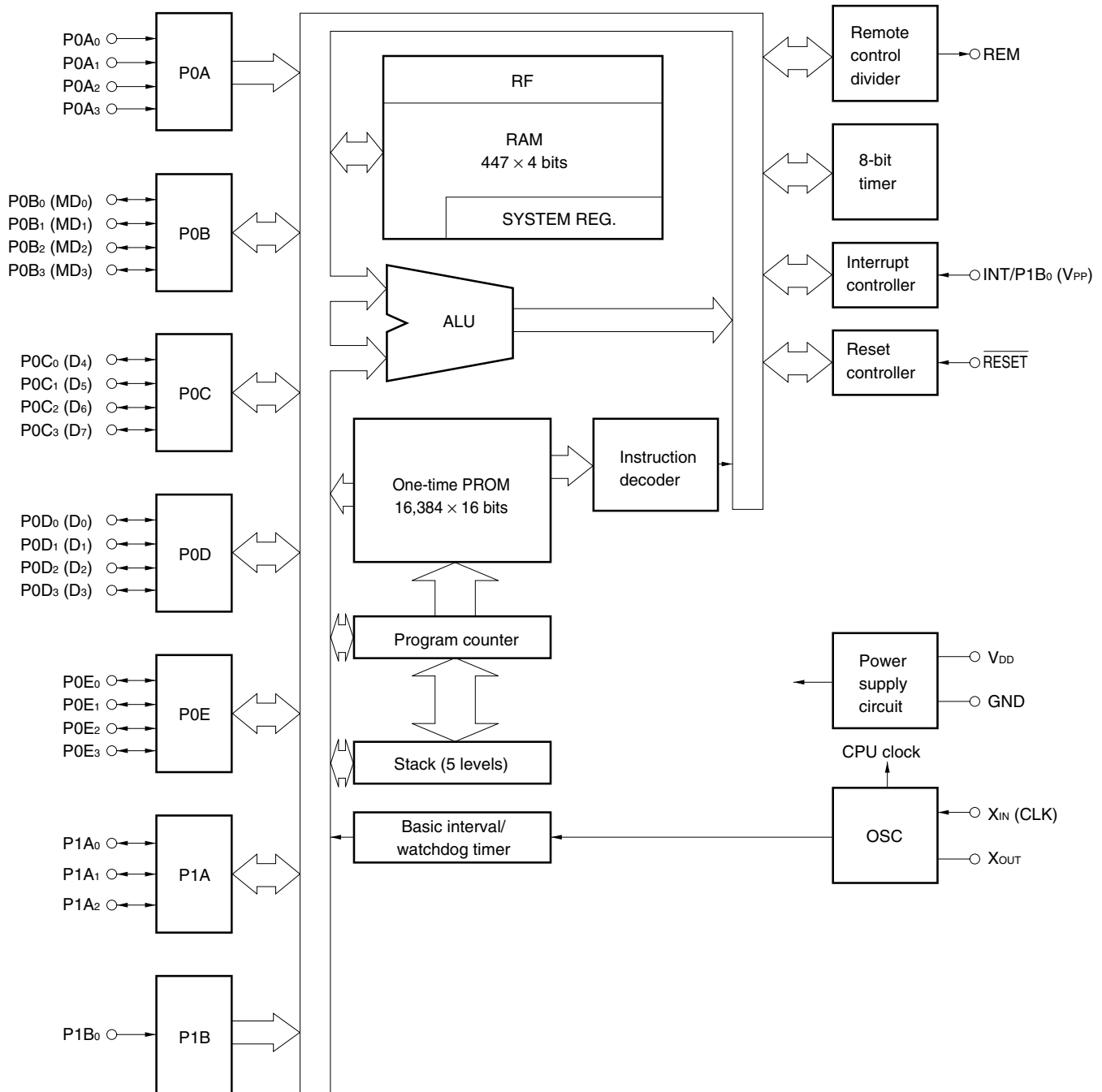
**Caution** Contents in parentheses indicate how to handle unused pins in PROM programming mode.

**L:** Connect to GND via a resistor (470 Ω) separately.

**Open:** Leave unconnected.

- CLK: Clock input for PROM
- D<sub>0</sub> to D<sub>7</sub>: Data input/output for PROM
- GND: Ground
- MD<sub>0</sub> to MD<sub>3</sub>: Mode select input for PROM
- V<sub>DD</sub>: Power supply
- V<sub>PP</sub>: Power supply for PROM writing

**BLOCK DIAGRAM**



**Remark** ( ): During PROM programming mode

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## 1. DIFFERENCES BETWEEN $\mu$ PD17246 AND $\mu$ PD17P246

The  $\mu$ PD17P246 is equipped with one-time PROM to which data can be written by the user instead of the internal mask ROM (program memory) of the  $\mu$ PD17246.

Table 1-1 shows the differences between the  $\mu$ PD17246 and  $\mu$ PD17P246.

The CPU functions and internal hardware of the  $\mu$ PD17P246, 17240, 17241, 17242, 17243, 17244, 17245, and 17246 are identical. Therefore, the  $\mu$ PD17P246 can be used to evaluate the program developed for the  $\mu$ PD17240, 17241, 17242, 17243, 17244, 17245, and 17246 system. **Note, however, that some of the electrical specifications such as supply current and low-voltage detection voltage of the  $\mu$ PD17P246 are different from those of the  $\mu$ PD17240, 17241, 17242, 17243, 17244, 17245, and 17246.**

**Table 1-1. Differences Between  $\mu$ PD17246 and  $\mu$ PD17P246**

Item	Product Name	$\mu$ PD17P246	$\mu$ PD17246
Program memory		One-time PROM	Mask ROM
		32 KB (16,384 $\times$ 16) (0000H to 3FFFH)	
Data memory		447 $\times$ 4 bits	
Low-voltage detector <sup>Note 1</sup>		Provided	Any (mask option)
V <sub>PP</sub> pin, operation mode select pin		Provided	Not provided
Instruction execution time <sup>Note 2</sup>		4 $\mu$ s (V <sub>DD</sub> = 2.2 to 3.6 V)	4 $\mu$ s (V <sub>DD</sub> = 2.0 to 3.6 V)
Supply voltage <sup>Note 2</sup>		V <sub>DD</sub> = 2.2 to 3.6 V	V <sub>DD</sub> = 2.0 to 3.6 V
Package		30-pin plastic SSOP (7.62 mm (300))	

**Notes** 1. Although the circuit configuration is identical, the electrical characteristics differ depending on the product.

★ 2. When  $f_x = 4$  MHz and high-speed mode operation is set.



## 2. PIN FUNCTIONS

### 2.1 Normal Operating Mode (1/3)

Pin No.	Symbol	Function	Output Form	After Reset
28 29 1 2	P0D <sub>0</sub> P0D <sub>1</sub> P0D <sub>2</sub> P0D <sub>3</sub>	<p>These pins constitute a 4-bit I/O port which can be set in the input or output mode in 4-bit units (group I/O).</p> <p>In the input mode, these pins serve as CMOS input pins with a pull-up resistor, and can be used as the key return input lines of a key matrix. The standby status must be released when at least one of the input lines goes low. In the output mode, these pins are used as N-ch open-drain output pins and can be used as the output lines of a key matrix.</p>	N-ch open-drain	Low-level output
3	P1B <sub>0</sub> /INT	<p>This is an input port pin. Whether this pin functions as the P1B<sub>0</sub> pin or the INT pin can be selected by the register file.</p> <ul style="list-style-type: none"> <li>• P1B<sub>0</sub> <p>This is a 1-bit CMOS input port.</p> <p>This port can be used to input a key return signal when a key matrix is used. At this time, whether a pull-up/down resistor is connected to this port and the standby mode release condition (whether it is released when this pin is high or low) can be selected.</p> <ol style="list-style-type: none"> <li>1. If connection of a resistor is specified and if it is specified that the standby mode is released when this pin goes low ... A pull-up resistor is connected. If a low level is input to the P1B<sub>0</sub> pin, the standby mode is released.</li> <li>2. If connection of a resistor is specified and if it is specified that the standby mode is released when this pin goes high ... A pull-down resistor is connected. If a high level is input to the P1B<sub>0</sub> pin, the standby mode is released.</li> <li>3. If connection of a resistor is not specified and if it is specified that the standby mode is released when this pin goes low (or high) ... No resistor is connected. If a low (or high) level is input to the P1B<sub>0</sub> pin, the standby mode is released.</li> </ol> <p>If a key matrix is not used, whether a resistor is connected and whether a pull-up or pull-down resistor is connected can be selected.</p> </li> <li>• INT <p>This is an external interrupt request signal. It can also be used to release the standby mode if an external interrupt request signal is input to this pin while the INT pin interrupt enable flag (IP) is set.</p> </li> </ul>	–	P1B <sub>0</sub> input (when key matrix is not used and no resistor connected)

2.1 Normal Operating Mode (2/3)

Pin No.	Symbol	Function	Output Form	After Reset
4 5 6 7	P0E <sub>0</sub> P0E <sub>1</sub> P0E <sub>2</sub> P0E <sub>3</sub>	<p>These pins constitute a 4-bit I/O port that can be set in the input or output mode in 1-bit units.</p> <p>If this port is set in the input mode when a key matrix is used, it functions as a CMOS input port with a pull-up resistor and can be used to input key return signals. If one of the pins of this port goes low, the standby mode is released.</p> <p>If this port is set in the output mode when a key matrix is used, it functions as an N-ch open-drain output port and can be used to output key matrix signals.</p> <p>If this port is set in the input mode when a key matrix is not used, it functions as a CMOS input port to/from which a resistor can be connected or disconnected in 1-bit units. If this port is set in the output mode when a key matrix is not used, it functions as a high-current CMOS output port.</p>	When key matrix is used: N-ch open-drain, when key matrix is not used: CMOS push-pull	CMOS input (when key matrix is not used and no resistor connected)
8	REM	Outputs transfer signal for infrared remote controller. Active-high output.	CMOS push-pull	Low-level output
9	V <sub>DD</sub>	Power supply	–	–
10 11	X <sub>OUT</sub> X <sub>IN</sub>	Connects ceramic resonator for system clock oscillation	–	(Oscillation stops)
12	GND	Ground	–	–
13	$\overline{\text{RESET}}$	Reset input Turns ON pull-down resistor if POC or watchdog timer overflows and if the stack pointer overflows or underflows, and resets the system. Usually, the pull-down resistor is ON.	–	Input

2.1 Normal Operating Mode (3/3)

Pin No.	Symbol	Function	Output Form	After Reset
14 15 30	P1A <sub>0</sub> P1A <sub>1</sub> P1A <sub>2</sub>	<p>These pins constitute a 3-bit I/O port that can be set in the input or output mode in 1-bit units.</p> <p>If this port is set in the input mode when a key matrix is used, it functions as a CMOS input port and can be used to input key return signals. At this time, whether a pull-up/down resistor is connected to this port and the standby mode release condition (whether it is released when this pin is high or low) can be selected in 1-bit units</p> <ol style="list-style-type: none"> <li>1. If connection of a resistor is specified and if it is specified that the standby mode is released when this port goes low ... A pull-up resistor is connected. If a low level is input to the set pin, the standby mode is released.</li> <li>2. If connection of a resistor is specified and if it is specified that the standby mode is released when this port goes high ... A pull-down resistor is connected. If a high level is input to the set pin, the standby mode is released.</li> <li>3. If connection of a resistor is not specified and if it is specified that the standby mode is released when this port goes low (or high) ... No resistor is connected. If a low (or high) level is input to the set pin, the standby mode is released.</li> </ol> <p>If this port is set in the output mode when a key matrix is used, it functions as an N-ch open-drain output port and can be used to output key matrix signals.</p> <p>If this port is set in the input mode when a key matrix is not used, it functions as a CMOS input port.</p> <p>Connection of a resistor to this port and whether a pull-up or pull-down resistor is connected to the port can be selected in 1-bit units.</p> <p>If this port is set in the output mode when a key matrix is not used, it functions as a high-current CMOS output port.</p>	When key matrix is used: N-ch open-drain, when key matrix is not used: CMOS push-pull	CMOS input (when key matrix is not used and no resistor connected)
16 17 18 19	P0A <sub>0</sub> P0A <sub>1</sub> P0A <sub>2</sub> P0A <sub>3</sub>	<p>These pins are CMOS input pins with a 4-bit pull-up resistor. They can be used as the key return input lines of a key matrix. If any one of these pins goes low, the standby status is released.</p>	–	CMOS input with pull-up resistor
20 21 22 23	P0B <sub>0</sub> P0B <sub>1</sub> P0B <sub>2</sub> P0B <sub>3</sub>	<p>These pins constitute a 4-bit I/O port that can be set in the input or output mode in 1-bit units.</p> <p>In the input mode, these pins are CMOS input pins with a pull-up resistor, and can be used as the key return input lines of a key matrix. The standby status is released when at least one of these pins goes low.</p> <p>In the output mode, they serve as N-ch open-drain output pins and can be used as the output lines of a key matrix.</p>	N-ch open-drain	CMOS input with pull-up resistor
24 25 26 27	P0C <sub>0</sub> P0C <sub>1</sub> P0C <sub>2</sub> P0C <sub>3</sub>	<p>These pins constitute a 4-bit I/O port that can be set in the input or output mode in 4-bit units (group I/O).</p> <p>In the input mode, these pins are CMOS input pins with a pull-up resistor, and can be used as the key return input lines of a key matrix. The standby status is released when at least one of these pins goes low.</p> <p>In the output mode, they serve as N-ch open-drain output pins and can be used as the output lines of a key matrix.</p>	N-ch open-drain	Low-level output

## 2.2 PROM Programming Mode

Pin No.	Symbol	Function	Output Form	After Reset
3	V <sub>PP</sub>	Power supply for PROM programming. Apply +12.5 V to this pin as the program voltage when writing/ verifying program memory.	–	–
9	V <sub>DD</sub>	Power supply. Apply +6 V to this pin when writing/verifying program memory.	–	–
11	CLK	Inputs clock for PROM programming.	–	–
12	GND	Ground.	–	–
20   23	MD <sub>0</sub>   MD <sub>3</sub>	Input pins used to select operating mode when PROM is programmed.	–	Input
24   27 28 29 1 2	D <sub>4</sub>   D <sub>7</sub> D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub>	Input/output 8-bit data for PROM programming	CMOS push-pull	Input

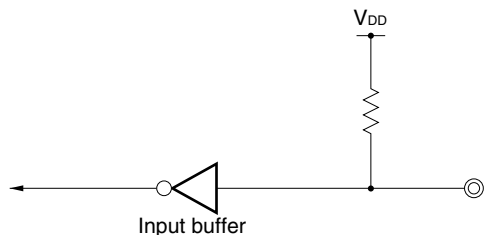
**Remark** The other pins are not used in the PROM programming mode. How to handle the other pins are described in **PIN CONFIGURATION (2) PROM programming mode**.

2.3 I/O Circuits

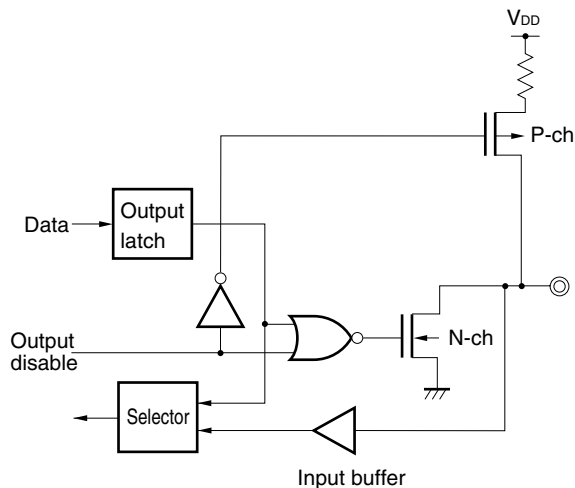
The equivalent I/O circuit for each μPD17P246 pin is shown below.

Figure 2-1. I/O Circuits (1/2)

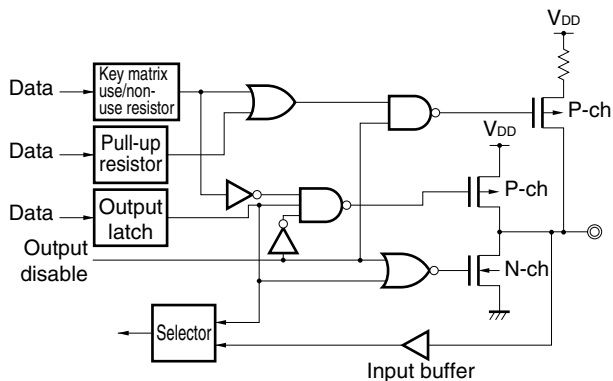
(1) P0A



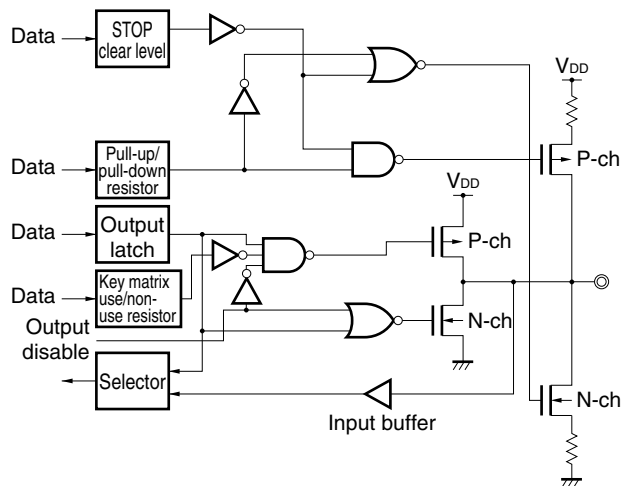
(2) P0B, P0C, P0D



(3) P0E



(4) P1A



(5) P1B

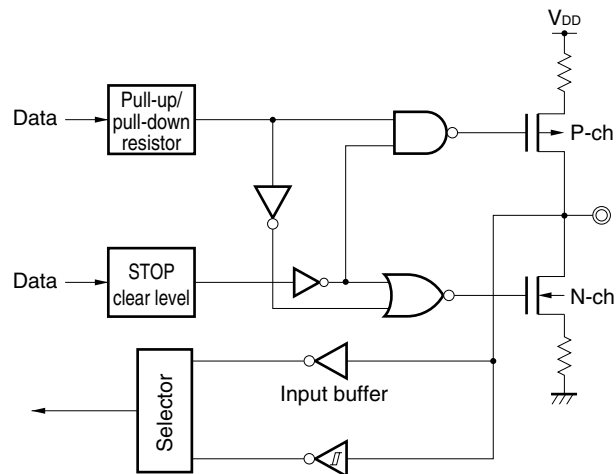
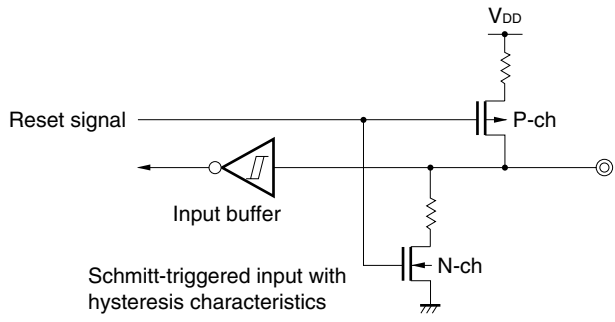
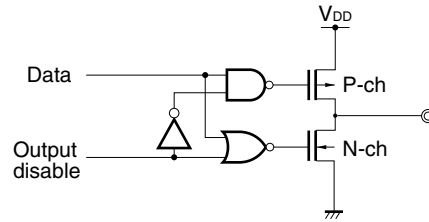


Figure 2-1. I/O Circuits (2/2)

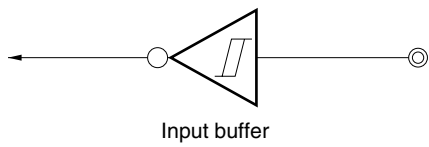
(6)  $\overline{\text{RESET}}$



(8) REM



(7) INT



Schmitt-triggered input with hysteresis characteristics

## 2.4 Connection of Unused Pins

Connect the unused pins as follows.

Table 2-1. Connection of Unused Pins

Pin	Recommended Connection
P0A <sub>0</sub> to P0A <sub>3</sub>	Leave open.
P0B <sub>0</sub> to P0B <sub>3</sub>	
P0C <sub>0</sub> to P0C <sub>3</sub>	
P0D <sub>0</sub> to P0D <sub>3</sub>	
P0E <sub>0</sub> to P0E <sub>3</sub>	Connect to GND (input mode).
P1A <sub>0</sub> to P1A <sub>2</sub>	
P1B <sub>0</sub> /INT	Connect to GND.
REM	Leave open.

## 2.5 Notes on Using the $\overline{\text{RESET}}$ and INT Pins

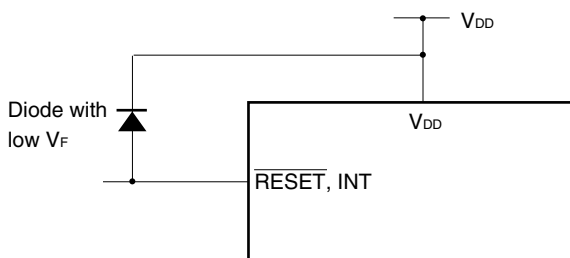
In addition to the functions shown in 2. PIN FUNCTIONS, the  $\overline{\text{RESET}}$  and INT pins also have the function of setting a test mode (for IC testing) in which the internal operations of the μPD17P246 are tested.

When a voltage higher than V<sub>DD</sub> is applied to either of these pins, the test mode is set. This means that, even during normal operation, the μPD17P246 may be set in the test mode if noise exceeding V<sub>DD</sub> is applied.

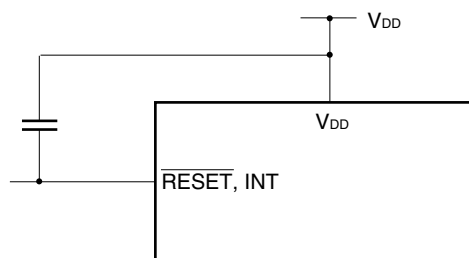
For example, if the wiring length of the  $\overline{\text{RESET}}$  or INT pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- Connect diode with low V<sub>F</sub> between V<sub>DD</sub> and  $\overline{\text{RESET}}$ /INT pin



- Connect capacitor between V<sub>DD</sub> and  $\overline{\text{RESET}}$ /INT pin



### 3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μPD17P246 is one-time PROM of 16,384 × 16 bits.

To write or verify this one-time PROM, the pins shown in Table 3-1 are used. Note that no address input pin is used. Instead, the address is updated by using the clock input from the CLK pin.

**Table 3-1. Pins Used to Write/Verify Program Memory**

Pin Name	Function
V <sub>PP</sub>	Supplies voltage when writing/verifying program memory. Apply +12.5 V to this pin.
V <sub>DD</sub>	Power supply. Supply +6 V to this pin when writing/verifying program memory.
CLK	Inputs clock to update address when writing/verifying program memory. By inputting pulse four times to CLK pin, address of program memory is updated.
MD <sub>0</sub> to MD <sub>3</sub>	Input to select operating mode when writing/verifying program memory.
D <sub>0</sub> to D <sub>7</sub>	Inputs/outputs 8-bit data when writing/verifying program memory.

#### 3.1 Operating Mode When Writing/Verifying Program Memory

The μPD17P246 is set in the program memory write/verify mode when +6 V is applied to the V<sub>DD</sub> pin and +12.5 V is applied to the V<sub>PP</sub> pin after the μPD17P246 has been in the reset status (V<sub>DD</sub> = 5 V,  $\overline{\text{RESET}} = 0 \text{ V}$ ) for a specific time. In this mode, the operating modes shown in Table 3-2 can be set by setting the MD<sub>0</sub> to MD<sub>3</sub> pins. Leave all the pins other than those shown in Table 3-1 unconnected or connect them to GND via a pull-down resistor (470 Ω). (See **PIN CONFIGURATION (2) PROM programming mode.**)

**Table 3-2. Setting Operating Mode**

Setting of Operating Mode						Operating Mode
V <sub>PP</sub>	V <sub>DD</sub>	MD <sub>0</sub>	MD <sub>1</sub>	MD <sub>2</sub>	MD <sub>3</sub>	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

×: don't care (L or H)

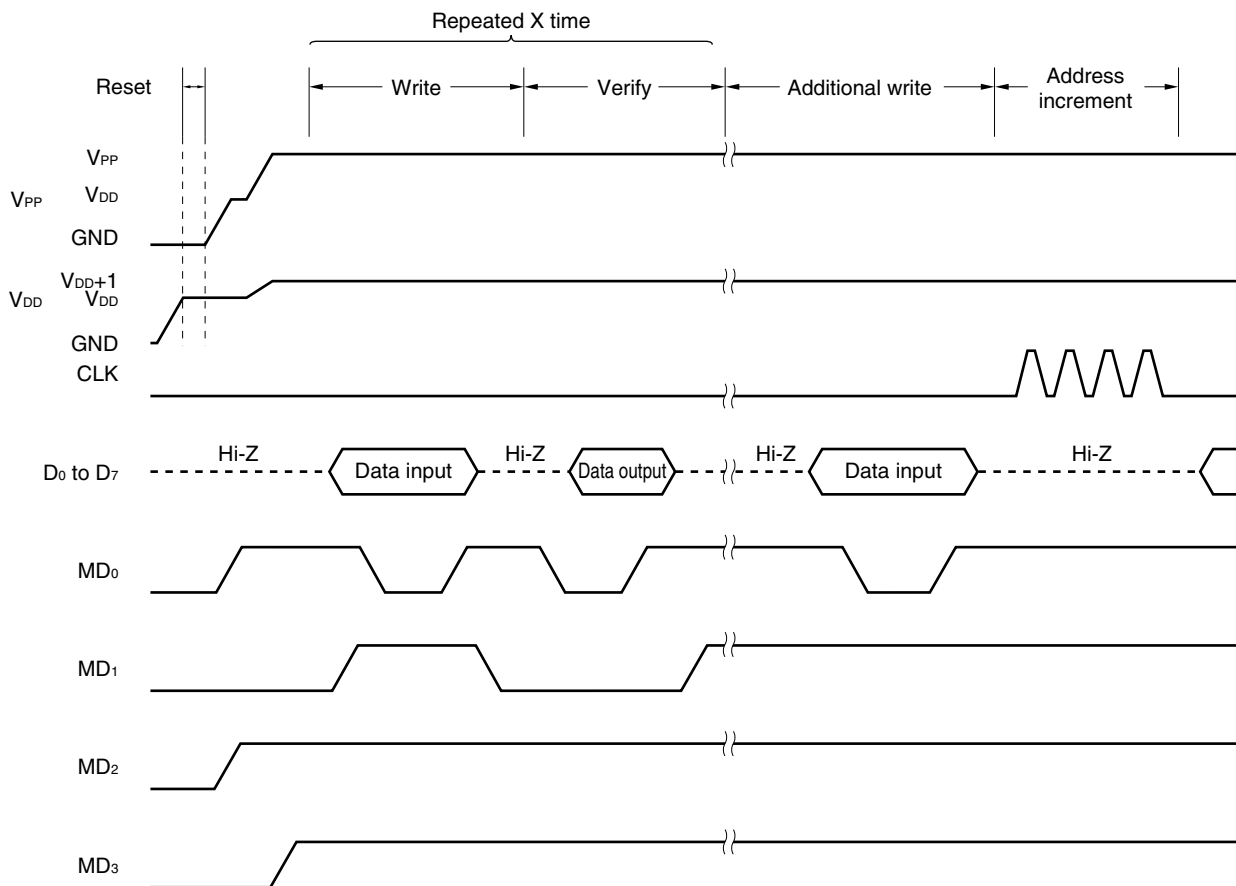


### 3.2 Program Memory Writing Procedure

The program memory is written at high speed in the following procedure.

- (1) Pull down the pins not used to GND via a resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V<sub>DD</sub> pin. Keep the V<sub>PP</sub> pin low.
- (3) Supply 5 V to the V<sub>PP</sub> pin after waiting for 10 μs.
- (4) Set the program memory address 0 clear mode by using the mode setting pins.
- (5) Supply +6 V to V<sub>DD</sub> and +12.5 V to V<sub>PP</sub>.
- (6) Set the program inhibit mode.
- (7) Write data to the program memory in the 1-ms write mode.
- (8) Set the program inhibit mode.
- (9) Set the verify mode. If the data have been written to the program memory, proceed to (10). If not, repeat steps (7) through (9).
- (10) Additional writing of (number of times of writing in (7) through (9): X) × 1 ms.
- (11) Set the program inhibit mode.
- (12) Input a pulse to the CLK pin four times to update the program memory address (+1).
- (13) Repeat steps (7) through (12) up to the last address.
- (14) Set the 0 clear mode of the program memory address.
- (15) Change the voltages on the V<sub>DD</sub> and V<sub>PP</sub> pins to 5 V.
- (16) Turn off power.

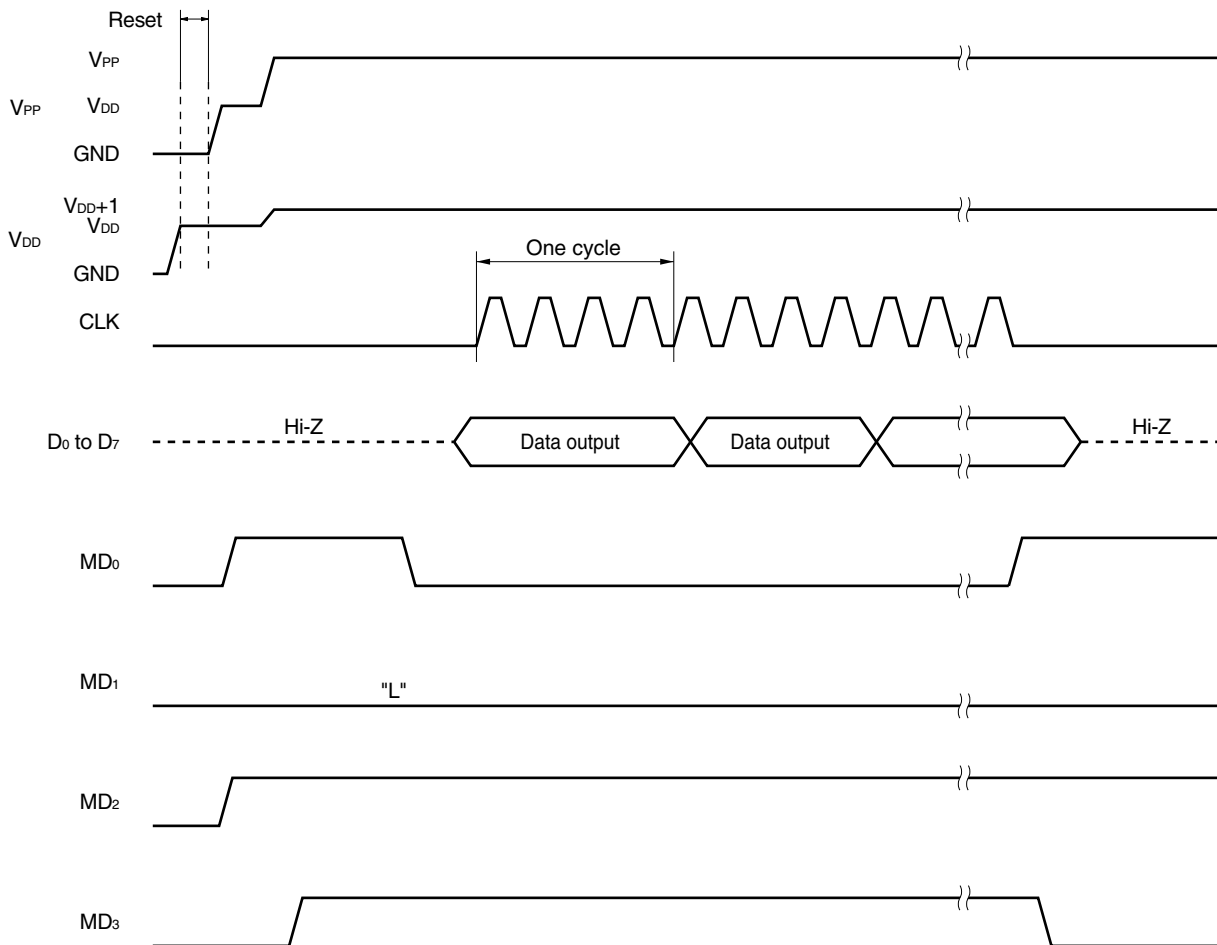
The following figure illustrates steps (2) through (12) above.



### 3.3 Program Memory Reading Procedure

- (1) Pull down the pins not used to GND via a resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V<sub>DD</sub> pin. Keep the V<sub>PP</sub> pin low.
- (3) Supply 5 V to the V<sub>PP</sub> pin after waiting for 10 μs.
- (4) Set the program memory address 0 clear mode by using the mode setting pins.
- (5) Supply +6 V to V<sub>DD</sub> and +12.5 V to V<sub>PP</sub>.
- (6) Set the program inhibit mode.
- (7) Set the verify mode. Data of each address is output sequentially each time the clock pulse is input to the CLK pin four times.
- (8) Set the program inhibit mode.
- (9) Set the program memory address 0 clear mode.
- (10) Change the voltage on the V<sub>DD</sub> and V<sub>PP</sub> pins to 5 V.
- (11) Turn off power.

The following figure illustrates steps (2) through (9) above.



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V <sub>DD</sub>			-0.3 to +7.0	V
PROM power supply	V <sub>PP</sub>			-0.3 to +13.5	V
Input voltage	V <sub>I</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>O</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
Output current, high <sup>Note</sup>	I <sub>OH</sub>	REM pin	Peak value	-36.0	mA
			rms value	-24.0	mA
		1 pin (P0E or P1A pin)	Peak value	-7.5	mA
			rms value	-5.0	mA
		Total of P0E, P1A pins	Peak value	-22.5	mA
			rms value	-15.0	mA
Output current, low <sup>Note</sup>	I <sub>OL</sub>	1 pin (P0B, P0C, P0D, P0E, P1A, or REM pin)	Peak value	7.5	mA
			rms value	5.0	mA
		Total of P0B, P0C, P0D, REM pins	Peak value	22.5	mA
			rms value	15.0	mA
		Total of P0E, P1A pins	Peak value	30.0	mA
			rms value	20.0	mA
Operating temperature	T <sub>A</sub>			-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C
Power dissipation	P <sub>d</sub>	T <sub>A</sub> = 85°C		180	mW

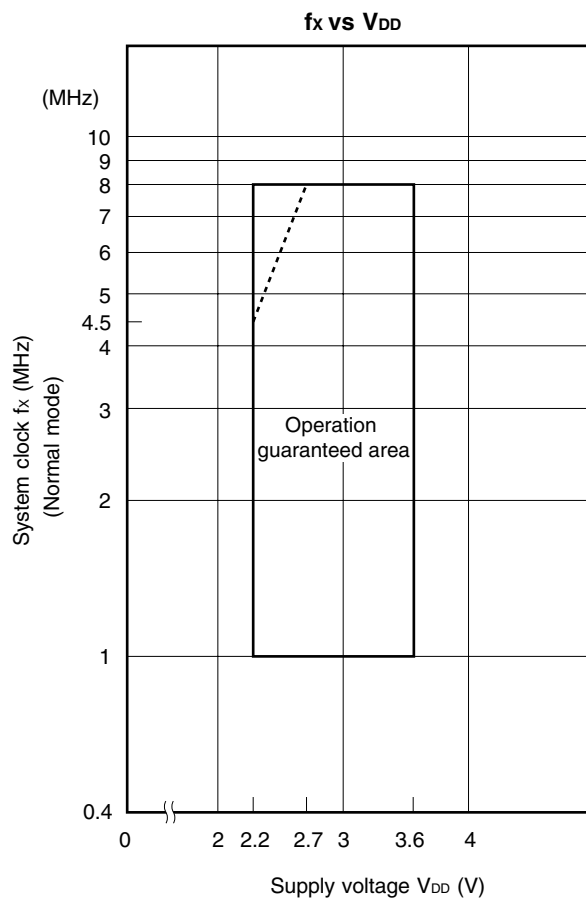
**Note** The rms value should be calculated as follows: [rms value] = [Peak value] × √Duty

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Recommended Operating Ranges (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.2 to 3.6 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★ Supply voltage	V <sub>DD1</sub>	f <sub>x</sub> = 1 MHz	High-speed mode (Instruction execution time: 16 μs)	2.2		3.6	V
	V <sub>DD2</sub>	f <sub>x</sub> = 4 MHz	High-speed mode (Instruction execution time: 4 μs)				
	V <sub>DD3</sub>	f <sub>x</sub> = 8 MHz	Normal mode (Instruction execution time: 4 μs)				
	V <sub>DD4</sub>		High-speed mode (Instruction execution time: 2 μs)	2.7	3.6	V	
★ Oscillation frequency	f <sub>x</sub>	Rf <sub>x</sub> = f <sub>x</sub> /2 or f <sub>x</sub>		1.0	4.0	8.0	MHz
		Rf <sub>x</sub> = 2f <sub>x</sub>		3.5	4.0	4.5	MHz
Operating temperature	T <sub>A</sub>			-40	+25	+85	°C
★ Low-voltage detector <sup>Note</sup>	t <sub>CV</sub>			3.5		32	μs

**Note** Reset if the status of V<sub>DD</sub> = 2.05 V (TYP.) lasts for 1 ms or longer. Program hang-up does not occur even if the voltage drops, until the reset function is effected. A resonator may stop oscillating before the reset function is effected if normal operation under the low voltage is not guaranteed.



**Remark** The region indicated by the broken lines in the above figure is the guaranteed operating range in the high-speed mode.

**System Clock Oscillator Characteristics (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.2 to 3.6 V)**

Resonator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
★ Ceramic resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>		1.0	4.0	8.0	MHz
		Oscillation stabilization time <sup>Note 2</sup>	After V <sub>DD</sub> reached MIN. in oscillation voltage range			4	ms

- Notes**
1. The oscillation frequency only indicates the oscillator characteristics.
  2. The oscillation stabilization time is necessary for oscillation to be stabilized after V<sub>DD</sub> application or STOP mode release.

**Caution** To use a system clock oscillator, perform the wiring in the area enclosed by the dotted line in the above figure as follows, to avoid adverse wiring capacitance influences:

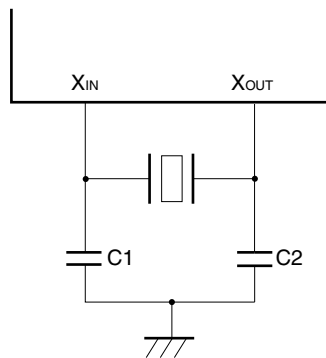
- Keep wiring length as short as possible.
- Do not cross a signal line with some other signal lines. Do not route the wiring in the vicinity of lines through which a large current flows.
- Always keep the oscillator capacitor ground at the same potential as GND. Do not ground the capacitor to a ground pattern, through which a large current flows.
- Do not extract signals from the oscillator.

★ Recommended Oscillator Constant

Ceramic resonator (T<sub>A</sub> = -40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V <sub>DD</sub> )		Remarks	
			C1	C2	MIN.	MAX.		
Murata Mfg. Co., Ltd.	CSBLA1M00J58-B0	1.0	120	120	2.0	3.6	-	
	CSBFB1M00J58-R1							
	CSTLS2M00G56-B0	2.0	-	-	2.3	3.6	On-chip capacitor	
	CSTCC2M00G56-R0							
	CSTLS3M00G53-B0	3.0	-	-	2.3	3.6		
	CSTCC3M00G53-R0							
	CSTLS4M00G53-B0	4.0	-	-	2.3	3.6		
	CSTCR4M00G53-R0							
	CSTLS6M00G53-B0	6.0	-	-	2.3	3.6		
	CSTCR6M00G53-R0							
	CSTLS8M00G53-B0	8.0	-	-	2.3	3.6		
	CSTCE8M00G52-R0							
TDK	FCR4.0MC5	4.0	-	-	2.3	3.6		On-chip capacitor
	FCR6.0MC5	6.0						
	FCR8.0MC5	8.0						

External circuit example



**Caution** The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. The internal operation conditions of the μPD17P246 must be within the specifications of the DC and AC characteristics.

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.2 to 3.6 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V <sub>IH1</sub>	RESET, INT		0.80V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	P0A, P0B, P0C, P0D		0.70V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH3</sub>	P0E, P1A, P1B		0.70V <sub>DD</sub>		V <sub>DD</sub>	V
Input voltage, low	V <sub>IL1</sub>	RESET, INT		0		0.2V <sub>DD</sub>	V
	V <sub>IL2</sub>	P0A, P0B, P0C, P0D		0		0.3V <sub>DD</sub>	V
	V <sub>IL3</sub>	P0E, P1A, P1B		0		0.3V <sub>DD</sub>	V
Input leakage current, high	I <sub>LH</sub>	P0A, P0B, P0C, P0D, P0E, P1A, P1B <sub>0</sub> /INT, RESET	V <sub>IH</sub> = V <sub>DD</sub> w/o pull-down resistor			3.0	μA
Input leakage current, low	I <sub>LIL</sub>	P0E, P1A, P1B <sub>0</sub> /INT	V <sub>IL</sub> = 0 V w/o pull-up resistor			-3.0	μA
Internal pull-up resistor	R <sub>1</sub>	P0E, P1A, P1B, RESET (pulled up)		25	50	100	kΩ
	R <sub>2</sub>	P0A, P0B, P0C, P0D		100	200	400	kΩ
Internal pull-down resistor	R <sub>3</sub>	P1A, P1B		25	50	100	kΩ
Output current, high	I <sub>OH</sub>	REM	V <sub>OH</sub> = 1.0 V, V <sub>DD</sub> = 3 V	-6	-13	-24	mA
Output voltage, high	V <sub>OH</sub>	P0E, P1A, REM	I <sub>OH</sub> = -0.5 mA	V <sub>DD</sub> - 0.3		V <sub>DD</sub>	V
Output voltage, low	V <sub>OL1</sub>	P0B, P0C, P0D, REM	I <sub>OL</sub> = 0.5 mA	0		0.3	V
	V <sub>OL2</sub>	P0E, P1A	I <sub>OL</sub> = 1.5 mA	0		0.3	V
Data retention characteristics	V <sub>DDDR</sub>	RESET = Low level or STOP mode1.3			3.6	V	
Low-voltage detection voltage	V <sub>DT</sub>	RESET pin pulled down, V <sub>DT</sub> = V <sub>DD</sub>			2.05	2.2	V
RAM retention detection voltage	V <sub>ID</sub>	V <sub>ID</sub> = V <sub>DD</sub> , RAMFLAG = 0 (RF21H.0), T <sub>A</sub> = -10 to +60 °C			1.65	1.8	V
Supply current <sup>Note</sup>	I <sub>DD1</sub>	Operating mode (high-speed)	V <sub>DD</sub> = 3 V ±10%	f <sub>X</sub> = 1 MHz	0.55	1.1	mA
				f <sub>X</sub> = 4 MHz	1.0	2.0	mA
				f <sub>X</sub> = 8 MHz	1.3	2.6	mA
	I <sub>DD2</sub>	Operating mode (low-speed)	V <sub>DD</sub> = 3 V ±10%	f <sub>X</sub> = 1 MHz	0.5	1.0	mA
				f <sub>X</sub> = 4 MHz	0.75	1.5	mA
				f <sub>X</sub> = 8 MHz	0.9	1.8	mA
	I <sub>DD3</sub>	HALT mode	V <sub>DD</sub> = 3 V ±10%	f <sub>X</sub> = 1 MHz	0.4	0.8	mA
				f <sub>X</sub> = 4 MHz	0.5	1.0	mA
				f <sub>X</sub> = 8 MHz	0.6	1.2	mA
	I <sub>DD4</sub>	STOP mode	V <sub>DD</sub> = 3 V ±10%		2.0	20.0	μA
built-in POC T <sub>A</sub> = 25°C				2.0	5.0	μA	

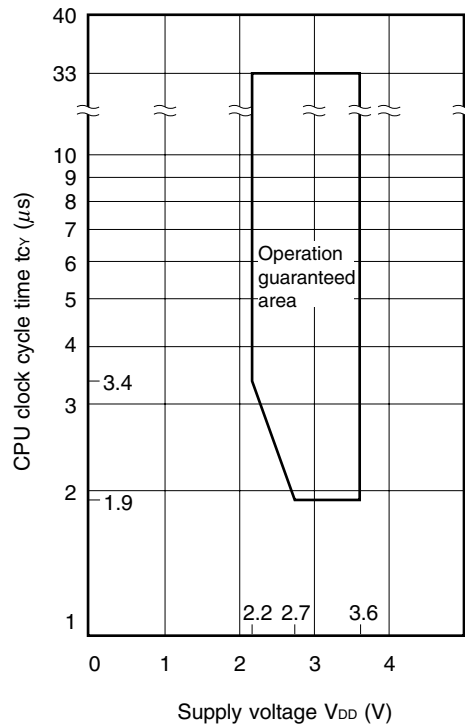
**Note** This does not include the current that flows through the internal pull-up resistors.

**AC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.2 to 3.6 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ CPU clock cycle time <sup>Note</sup> (Instruction execution time)	t <sub>CY1</sub>	V <sub>DD</sub> = 2.2 to 3.6 V	3.4		33	μs
	t <sub>CY2</sub>	V <sub>DD</sub> = 2.7 to 3.6 V	1.9		33	μs
INT high-/low-level width	t <sub>INTH</sub> , t <sub>INTL</sub>		20			μs
RESET low-level width	t <sub>RSL</sub>		10			μs

★ **Note** The CPU clock cycle time (instruction execution time) is determined by the oscillation frequency of the resonator connected and SYSCK (RF: address 02H) of the register file. The figure below shows the CPU clock cycle time t<sub>CY</sub> vs. supply voltage V<sub>DD</sub> characteristics.

**t<sub>CY</sub> vs V<sub>DD</sub>**



**DC Programming Characteristics (T<sub>A</sub> = 25°C, V<sub>DD</sub> = 6.0 ±0.25 V, V<sub>PP</sub> = 12.5 ±0.3 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V <sub>IH1</sub>	Other than CLK	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	CLK	V <sub>DD</sub> - 0.5		V <sub>DD</sub>	V
Input voltage, low	V <sub>IL1</sub>	Other than CLK	0		0.3V <sub>DD</sub>	V
	V <sub>IL2</sub>	CLK	0		0.4	V
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>			10	μA
Output voltage, high	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 1.0			V
Output voltage, low	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>DD</sub> supply current	I <sub>DD</sub>				30	mA
V <sub>PP</sub> supply current	I <sub>PP</sub>	MD <sub>0</sub> = V <sub>IL</sub> , MD <sub>1</sub> = V <sub>IH</sub>			30	mA

- Cautions**
1. Keep V<sub>PP</sub> to within +13.5 V including overshoot.
  2. Apply V<sub>DD</sub> before V<sub>PP</sub> and turns it off after V<sub>PP</sub>.

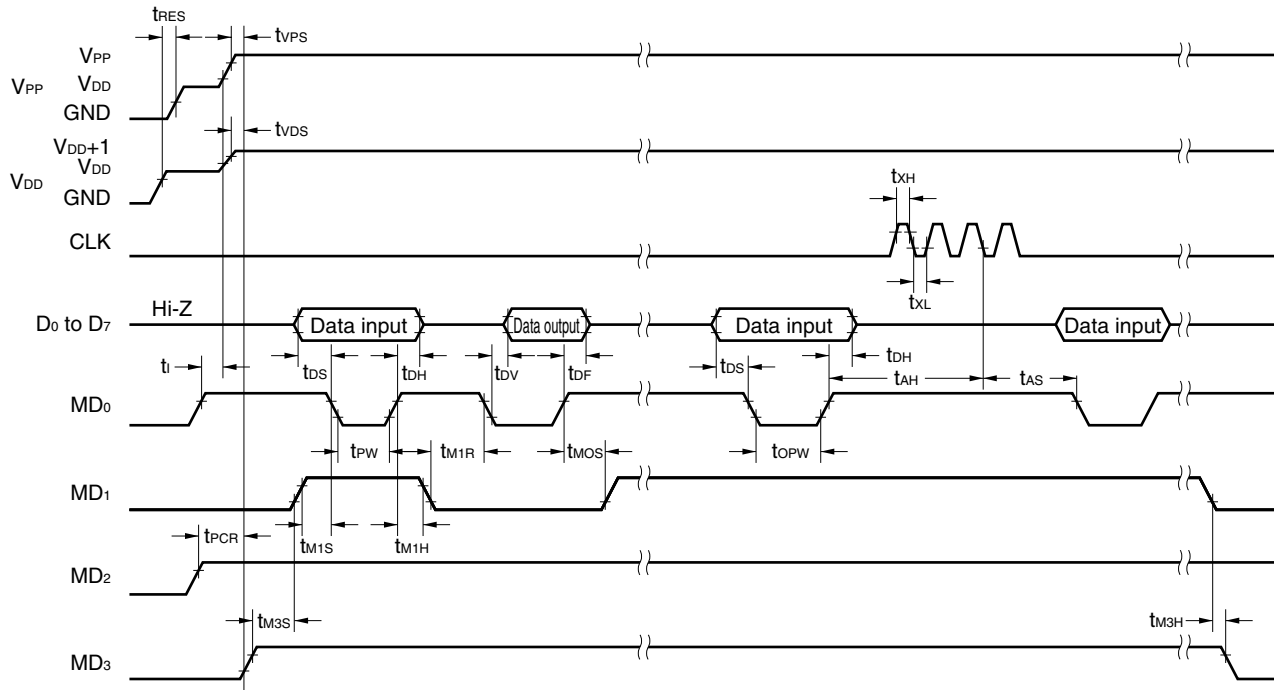


**AC Programming Characteristics ( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 6.0 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ )**

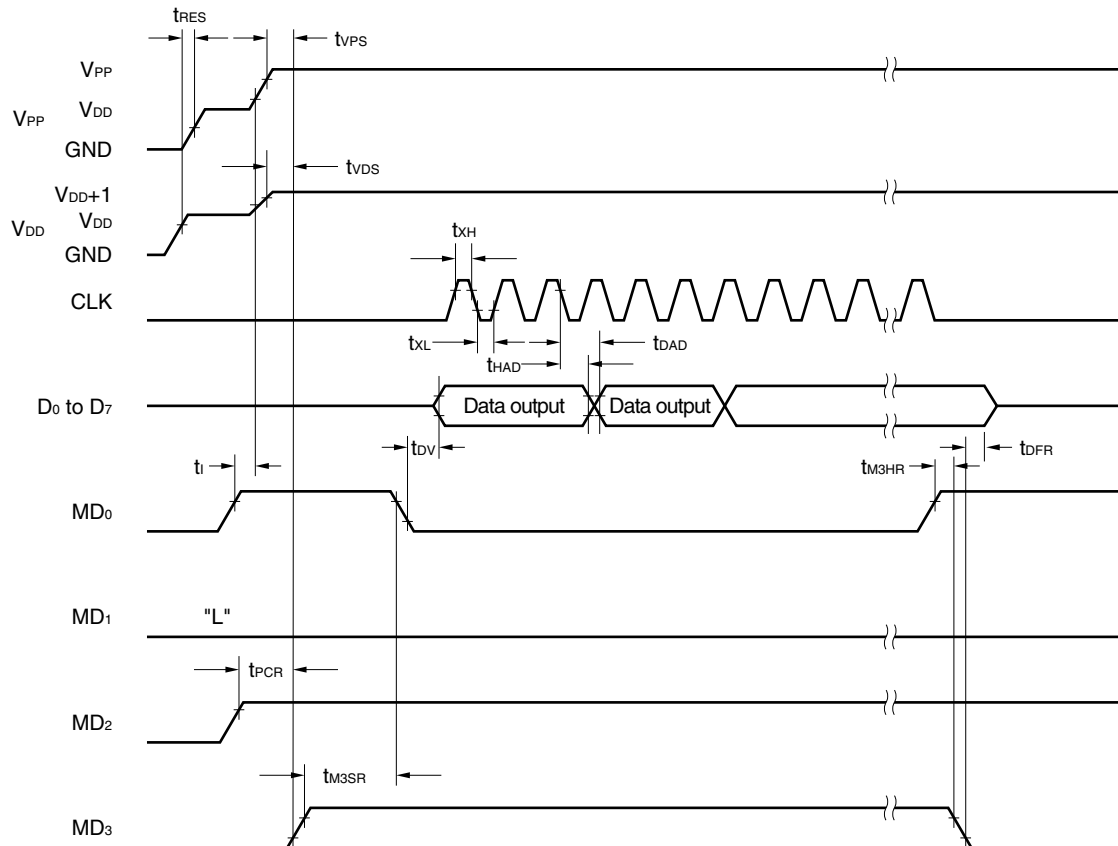
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time <sup>Note</sup> (to MD <sub>0</sub> ↓)	t <sub>AS</sub>		2			$\mu\text{s}$
MD <sub>1</sub> setup time (to MD <sub>0</sub> ↓)	t <sub>M1S</sub>		2			$\mu\text{s}$
Data setup time (to MD <sub>0</sub> ↓)	t <sub>DS</sub>		2			$\mu\text{s}$
Address hold time <sup>Note</sup> (from MD <sub>0</sub> ↑)	t <sub>AH</sub>		2			$\mu\text{s}$
Data hold time (from MD <sub>0</sub> ↑)	t <sub>DH</sub>		2			$\mu\text{s}$
Data output float delay time from MD <sub>0</sub> ↑	t <sub>DF</sub>		0		130	ns
V <sub>PP</sub> setup time (to MD <sub>3</sub> ↑)	t <sub>VPS</sub>		2			$\mu\text{s}$
V <sub>DD</sub> setup time (to MD <sub>3</sub> ↑)	t <sub>VDS</sub>		2			$\mu\text{s}$
Initial program pulse width	t <sub>PW</sub>		0.95	1.0	1.05	ms
Additional program pulse width	t <sub>OPW</sub>		0.95		21.0	ms
MD <sub>0</sub> setup time (to MD <sub>1</sub> ↑)	t <sub>MOS</sub>		2			$\mu\text{s}$
Data output delay time from MD <sub>0</sub> ↓	t <sub>DV</sub>	MD <sub>0</sub> = MD <sub>1</sub> = V <sub>IL</sub>			1	$\mu\text{s}$
MD <sub>1</sub> hold time (from MD <sub>0</sub> ↑)	t <sub>M1H</sub>	t <sub>M1H</sub> + t <sub>M1R</sub> ≥ 50 $\mu\text{s}$	2			$\mu\text{s}$
MD <sub>1</sub> recovery time (from MD <sub>0</sub> ↓)	t <sub>M1R</sub>		2			$\mu\text{s}$
Program counter reset time	t <sub>PCR</sub>		10			$\mu\text{s}$
CLK input high-, low-level width	t <sub>XH</sub> , t <sub>XL</sub>		0.125			$\mu\text{s}$
CLK input frequency	f <sub>X</sub>				4.19	MHz
Initial mode set time	t <sub>I</sub>		2			$\mu\text{s}$
MD <sub>3</sub> setup time (to MD <sub>1</sub> ↑)	t <sub>M3S</sub>		2			$\mu\text{s}$
MD <sub>3</sub> hold time (from MD <sub>1</sub> ↓)	t <sub>M3H</sub>		2			$\mu\text{s}$
MD <sub>3</sub> setup time (to MD <sub>0</sub> ↓)	t <sub>M3SR</sub>	When program memory is read	2			$\mu\text{s}$
Data output delay time from address <sup>Note</sup>	t <sub>DAD</sub>	When program memory is read			2	$\mu\text{s}$
Data output hold time from address <sup>Note</sup>	t <sub>HAD</sub>	When program memory is read	0		130	ns
MD <sub>3</sub> hold time (from MD <sub>0</sub> ↑)	t <sub>M3HR</sub>	When program memory is read	2			$\mu\text{s}$
Data output float delay time from MD <sub>3</sub> ↓	t <sub>DFR</sub>	When program memory is read			2	$\mu\text{s}$
Reset setup time	t <sub>RES</sub>		10			$\mu\text{s}$

**Note** The internal address increment (+1) is performed on the rising edge of the 3rd clock, where 4 clocks comprise one cycle. The internal clock is not connected to a pin.

**Program Memory Write Timing**

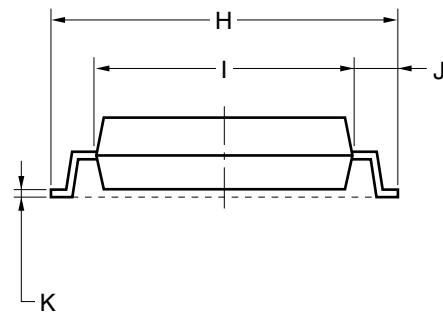
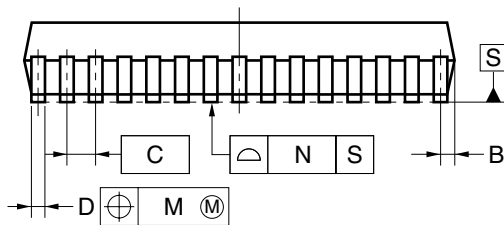
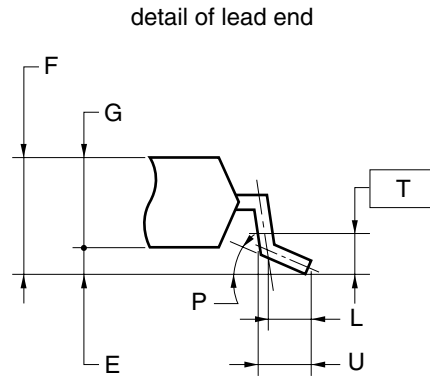
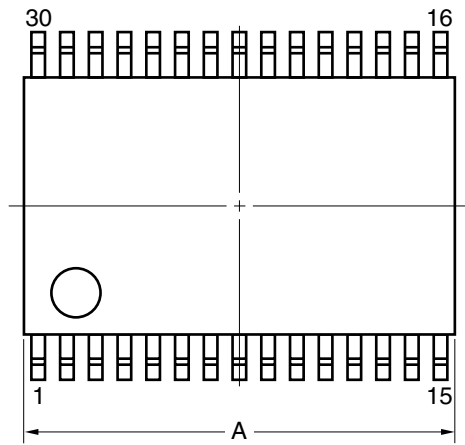


**Program Memory Read Timing**



5. PACKAGE DRAWING

30-PIN PLASTIC SSOP (7.62 mm (300))



**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° <sup>+5°</sup> <sub>-3°</sub>
T	0.25
U	0.6±0.15

S30MC-65-5A4-2

★ 6. RECOMMENDED SOLDERING CONDITIONS

The μPD17P246 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

**Table 6-1. Surface Mounting Type Soldering Conditions**

μPD17P246M1MC-5A4: 30-pin plastic SSOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	VP15-103-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	WS60-103-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

**Note** After opening the dry peak, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

**APPENDIX DEVELOPMENT TOOLS**

To develop the programs for the μPD17P246, the following development tools are available.

**Hardware**

Name	Remarks
In-circuit emulator (IE-17K, IE-17K-ET <sup>Note 1</sup> )	IE-17K and IE-17K-ET are the in-circuit emulators used in common with the 17K Series microcontroller. IE-17K and IE-17K-ET are connected to a PC-9800 series or IBM PC/AT™ compatible machines as the host machine with RS-232C. By using these in-circuit emulators with a system evaluation board (EM board) corresponding to the product, the emulators can emulate the product. A higher level debugging environment can be provided by using man-machine interface <i>SIMPLEHOST</i> ™.
★ EM board (EM-17246 <sup>Note 2</sup> )	This is an EM board for μPD17246 Subseries. It can be used alone to evaluate a system or in combination with an in-circuit emulator for debugging.
Emulation probe (EP-17K30GS)	EP-17K30GS is an emulation probe for 17K Series 30-pin SSOP (MC-5A4). When used with EV-9500GT-30 <sup>Note 3</sup> , it connects an EM board to the target system.
Conversion adapter (EV-9500GT-30 <sup>Note 3</sup> )	The EV-9500GT-30 is a conversion adapter for the 30-pin SSOP (MC-5A4). It is used to connect the EP-17K30GS and target system.
PROM programmer (AF-9706 <sup>Note 4</sup> , AF-9708 <sup>Note 4</sup> , AF-9709 <sup>Note 4</sup> )	AF-9706, AF-9708, and AF-9709 are PROM programmers corresponding to μPD17P246. By connecting program adapter PA-17P246 to this PROM programmer, μPD17P246 can be programmed.
Program adapter (PA-17P236)	PA-17P236 are adapters that is used to program μPD17P246, and is used in combination with AF-9706, AF-9708, or AF-9709.

**Notes** 1. Low-cost model: External power supply type

2. This is a product of Naito Densai Machida Mfg. Co., Ltd. For details, consult Naito Densai Machida Mfg. Co., Ltd. (Tel: +81-45-475-4191).
3. Two EV-9500GT-30 are supplied with the EP-17K30GS. Five EV-9500GT-30 are optionally available as a set.
4. These are products of Ando Electric Co., Ltd. For details, consult Ando Electric Co., Ltd. (Tel: +81-53-576-1560).

**Software**

Name	Outline	Host Machine	OS	Supply Medium	Part number
17K assembler (RA17K)	The RA17K is an assembler common to the 17K Series products. When developing the program of devices, RA17K is used in combination with a device file (AS17246).	PC-9800 series	Japanese Windows™	3.5" 2HD	μSAA13RA17K
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μSAB13RA17K
			English Windows		μSBB13RA17K
Device file (AS17246)	The AS17246 is a device file for μPD17240, 17241, 17242, 17243, 17244, 17245, and 17246 and is used in combination with an assembler for the 17K Series (RA17K).	PC-9800 series	Japanese Windows	3.5" 2HD	μSAA13AS17246
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μSAB13AS17246
			English Windows		μSBB13AS17246
Support software (SIMPLEHOST)	SIMPLEHOST is a software package that enables man-machine interface on the Windows when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	Japanese Windows	3.5" 2HD	μSAA13ID17K
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μSAB13ID17K
			English Windows		μSBB13ID17K

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]



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