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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

μ PD17P136A

SMALL GENERAL-PURPOSE 4 BIT SINGLE-CHIP MICROCONTROLLER

The μ PD17P136A is a one-time PROM version of the μ PD17136A, in which the internal masked ROM of the μ PD17136A is replaced with a one-time PROM that can be written to just once.

Since user programs can be written to the PROM, this microcontroller is suited for program evaluation and small-lot production of the μ PD17134A/ μ PD17136A, or for program evaluation of the μ PD17136A(A)/ μ PD17136A(A1).

The following user's manual describes the details of functions. Be sure to read it before design.
 μ PD17134A Sub-Series User's Manual: IEU-1369

FEATURES

- 17K architecture : General registers
- Pin compatible with the μ PD17136A (except for PROM programming function)
- Internal one-time PROM : 4K bytes (2048 \times 16 bits)
- Instruction execution time : 8 μ s (at fcc = 2 MHz, RC oscillation^{Note})
- Power-on/power-down reset function
- Supply voltage : $V_{DD} = 2.7$ to 5.5 V

Note The capacitor for RC oscillation is contained in the μ PD17P136A.

ORDERING INFORMATION

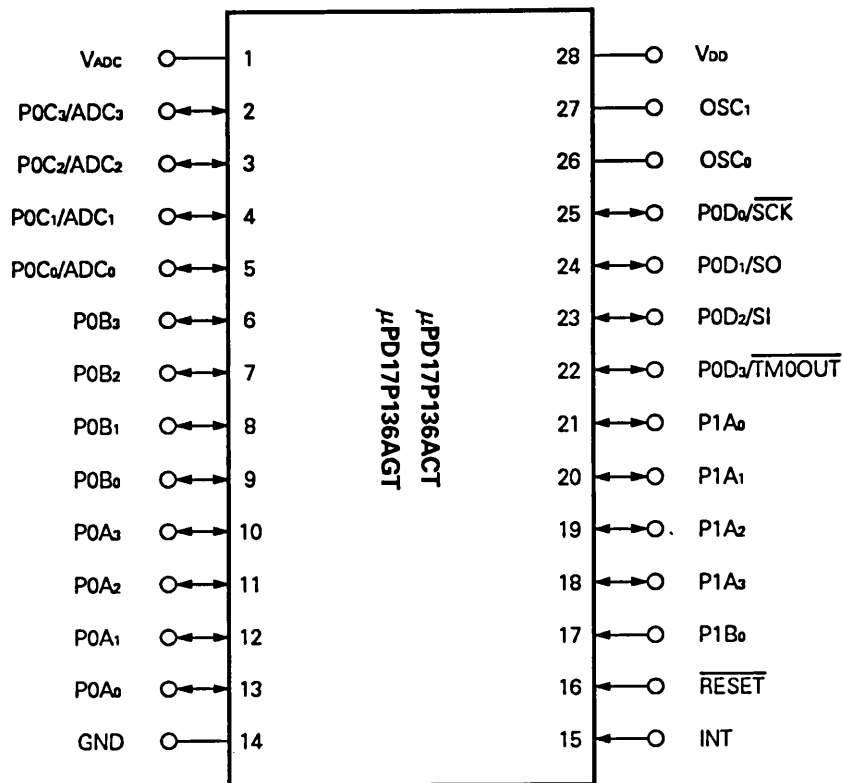
Part number	Package
μ PD17P136ACT	28-pin plastic shrink DIP (400 mil)
μ PD17P136AGT	28-pin plastic SOP (375 mil)

In the program memory write/verify mode, the voltage used for programming is applied to pin No. 17, P1B₀/V_{PP}. If a voltage of V_{DD} plus 0.3 V or more is applied to this pin in the normal operation mode, the microcontroller may crash. Design the circuit so that a voltage of this magnitude is never applied to the pin.

The information in this document is subject to change without notice.

PIN CONFIGURATION (TOP VIEW)

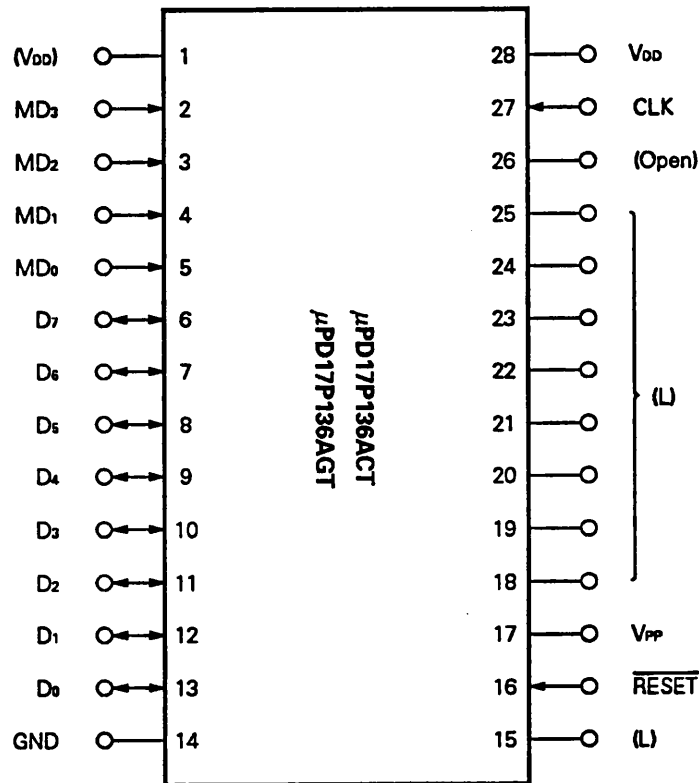
(1) Normal operating mode



- ADC₀-ADC₃ : Analog input
- GND : Ground
- INT : External interrupt input
- OSC₀, OSC₁ : System clock oscillation
- P0A₀-P0A₃ : Port 0A
- P0B₀-P0B₃ : Port 0B
- P0C₀-P0C₃ : Port 0C
- P0D₀-P0D₃ : Port 0D
- P1A₀-P1A₃ : Port 1A

- P1B₀ : Port 1B
- RESET : Reset input
- SCK : Serial clock input/output
- SI : Serial data input
- SO : Serial data output
- TM0OUT : Timer 0 output
- V_{Adc} : Analog power supply
- V_{DD} : Power supply

(2) Program memory write/verify mode



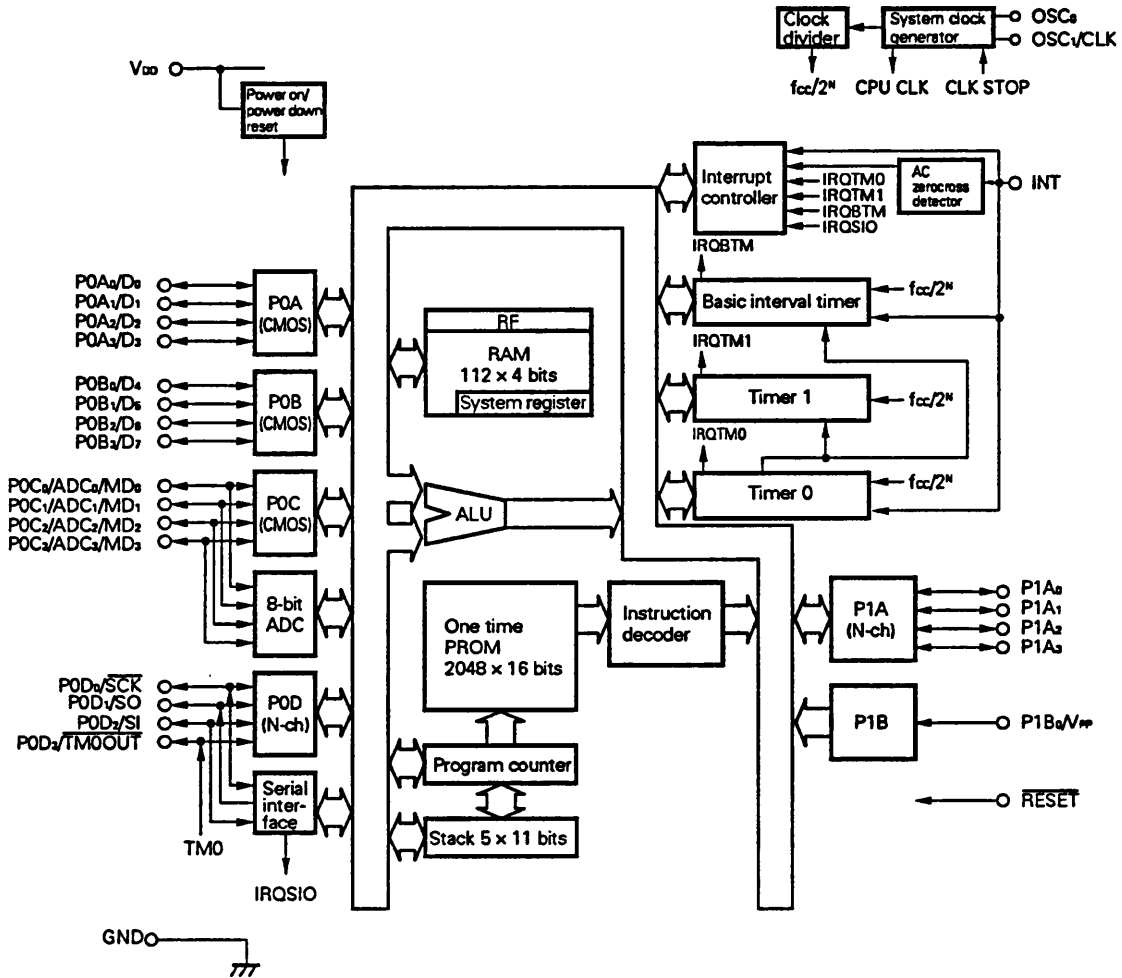
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- | | | | |
|----------------------------------|------------------------------|---------------------------|----------------------------|
| CLK | : Address update clock input | $\overline{\text{RESET}}$ | : Reset input |
| D ₀ -D ₇ | : Data input/output | V _{DD} | : Power supply |
| GND | : Ground | V _{PP} | : Programming power supply |
| MD ₀ -MD ₃ | : Operation mode selection | | |

Caution A symbol in parenthesis indicates that a signal having the specified level should be applied to the corresponding pins in the program memory write/verify mode.

- L** : Connect these pins separately to the GND pin through pull-down resistors.
- $\overline{\text{RESET}}$** : Apply a voltage equal to V_{DD} to this pin in the program write/verify mode. When this pin is used as the system reset input pin before the microcontroller enters the program write/verify mode, apply a voltage equal to V_{DD} to the pin 10 μs after the voltage is applied to the V_{DD} pin. For details, see Chapter 3.

BLOCK DIAGRAM



Remark The terms CMOS and N-ch in parentheses indicate the output interface of the port.
 CMOS: CMOS push-pull output
 N-ch : N-channel open-drain output

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1. PINS

1.1 NORMAL OPERATING MODE

Pin No.	Pin name	Function	Input/output	After power-on reset
1	V _{ADC}	Power voltage for the A/D converter	-	-
2 - 5	P0C ₃ /ADC ₃ - P0C ₀ /ADC ₀	Port 0C or analog input for the A/D converter <ul style="list-style-type: none"> • P0C₃ - P0C₀ • 4-bit input/output port • Each pin is specified as an input or output pin. • ADC₃ - ADC₀ • Analog input for the A/D converter 	CMOS push-pull	Input (P0C)
6 - 9	P0B ₃ - P0B ₀	Port 0B <ul style="list-style-type: none"> • 4-bit input/output port • These four pins are specified together as input or output pins. • Connection to pull-up resistors can be specified by program in units of 4 bits 	CMOS push-pull	Input
10 - 13	P0A ₃ - P0A ₀	Port 0A <ul style="list-style-type: none"> • 4-bit input/output port • These four pins are specified together as input or output pins. • Connection to pull-up resistors can be specified by program in units of 4 bits 	CMOS push-pull	Input
14	GND	Ground	-	-
15	INT	Input of external interrupt requests or input of signal for releasing standby mode	-	-
16	RESET	System reset input pin	-	-
17	P1B ₀	Port 1B <ul style="list-style-type: none"> • 1-bit input port 	-	Input
18 - 21	P1A ₃ - P1A ₀	Port 1A <ul style="list-style-type: none"> • 4-bit input/output port • These four pins are specified together as input or output pins. 	N-ch open drain	Input
22 23 24 25	P0D ₃ /TM0OUT P0D ₂ /SI P0D ₁ /SO P0D ₀ /SCK	Pin for port 0D, timer 0 output, serial data input, serial data output, and serial clock input/output <ul style="list-style-type: none"> • P0D₃ - P0D₀ • 4-bit input/output port • Each pin is specified as an input or output pin. • TM0OUT <ul style="list-style-type: none"> • Timer 0 output • SI <ul style="list-style-type: none"> • Serial data input • SO <ul style="list-style-type: none"> • Serial data output • SCK <ul style="list-style-type: none"> • Serial clock input/output 	N-ch open drain	Input (P0D)
26 27	OSC ₀ OSC ₁	For system clock oscillation Connect a resistor between OSC ₀ and OSC ₁ .	-	-
28	V _{DD}	Power supply	-	-

1.2 PROGRAM MEMORY WRITE/VERIFY MODE

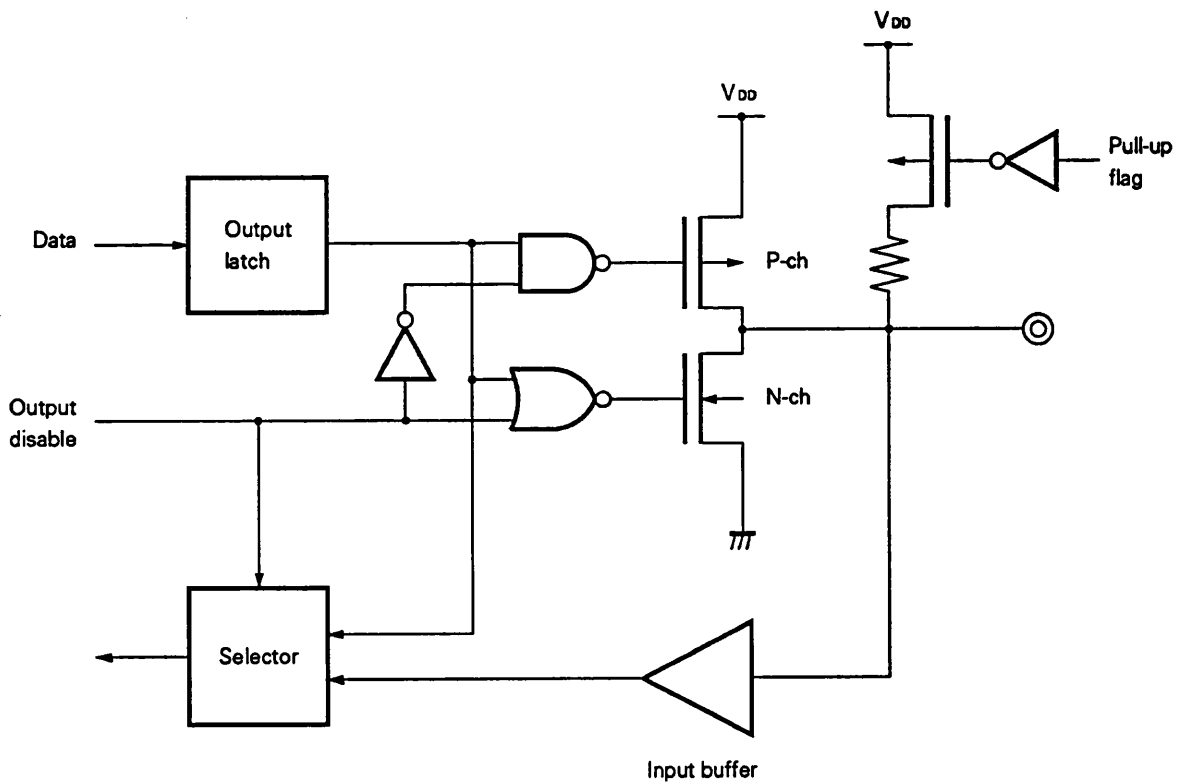
Pin No.	Pin name	Function	Input/output
2 - 5	MD ₃ - MD ₀	Input pins that select an operation mode when writing to program memory or verifying its contents	Input
6 - 13	D ₇ - D ₀	Input/output pins for 8-bit data used when writing to program memory or verifying its contents	Input/output
14	GND	Ground	-
16	RESET	System reset input	Input
17	V _{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.	-
27	CLK	Input pin for address update clocks used when writing to program memory or verifying its contents	Input
28	V _{DD}	Power supply. +6 V is applied to this pin when writing to program memory or verifying its contents.	-

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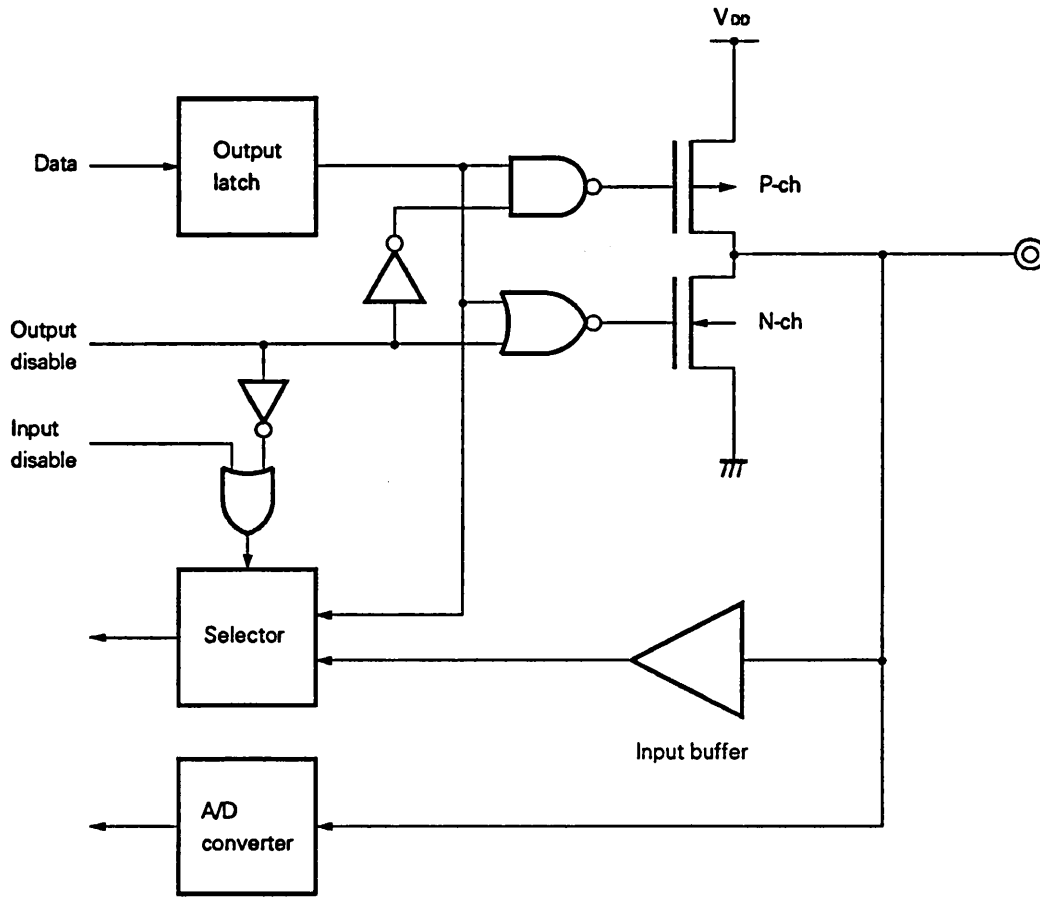
1.3 EQUIVALENT INPUT/OUTPUT CIRCUITS

Below are simplified diagrams of the equivalent circuits for each pin.

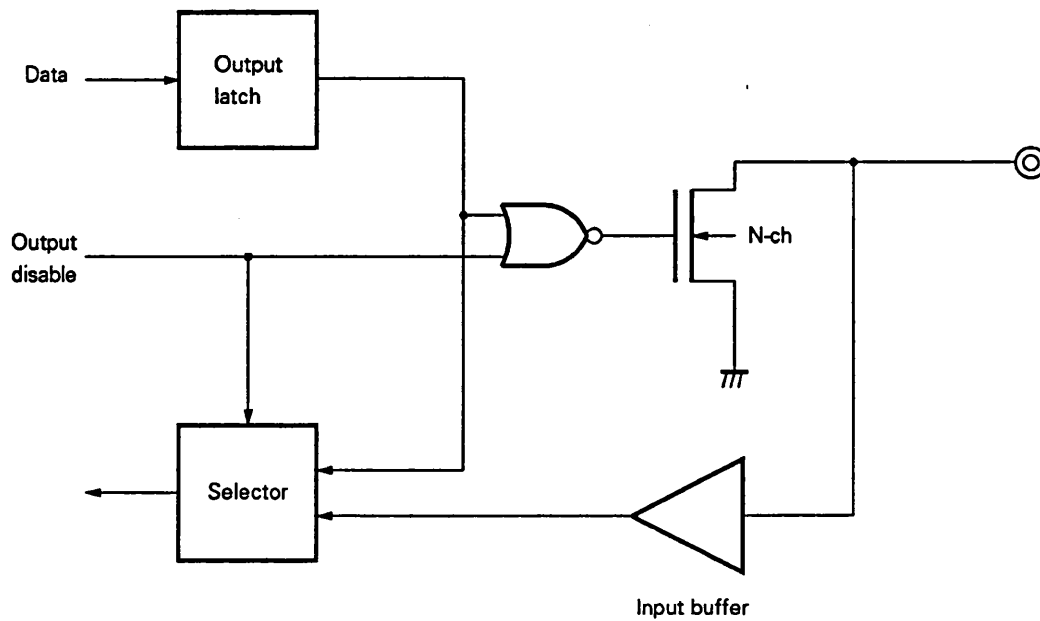
(1) P0A₀ to P0A₃, P0B₀ to P0B₃



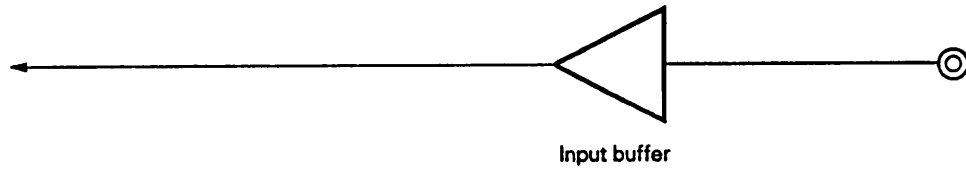
(2) P0C₀/ADC₀ to P0C₃/ADC₃



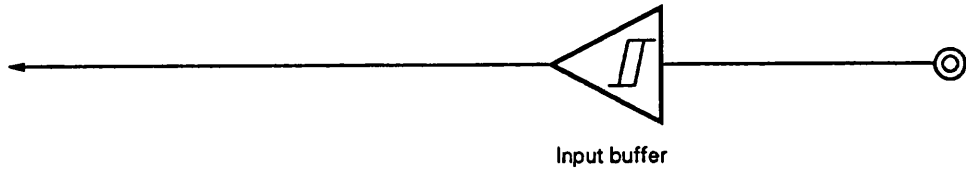
(3) P0D₀ to P0D₃, P1A₀ to P1A₃



(4) P1B₀



(5) INT, $\overline{\text{RESET}}$



1.4 HANDLING UNUSED PINS

Connect unused pins as follows:

Table 1-1 Handling Unused Pins

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Pin			Recommended conditions and handling	
			Internal	External
Port	Input mode	P0A, P0B	Pull-up resistors that can be specified with the software are incorporated.	Leave open.
		P0C	—	Connect to V _{DD} or ground through resistors for each pin. ^{Note 1}
		P0D, P1A, P1B ₀ ^{Note 2}	—	Connect directly to ground.
	Output mode	P0A, P0B, P0C (CMOS ports)	—	Leave open.
		P0D, P1A (N-ch open-drain port)	Outputs low level.	
External interrupt (INT)			—	Connect directly to V _{DD} or ground.
RESET ^{Note 3}			—	Connect directly to V _{DD} .
V _{ADC}			—	Connect directly to V _{DD} .

Notes 1. When a pin is pulled up to V_{DD} (connected to V_{DD} through a resistor) or pulled down to ground (connected to ground through a resistor) outside the chip, take the driving capacity and maximum current consumption of a port into consideration. When using high-resistance pull-up or pull-down resistors, apply appropriate countermeasures to ensure that noise is not attracted by the resistors. Although the optimum pull-up or pull-down resistor varies with the application circuit, in general, a resistor of 10 to 100 kilohms is suitable.

2. Since the P1B₀ pin is also used as the V_{PP} pin in the program memory write/verify mode, connect it directly to ground, when the pin is not used.

3. When designing an application circuit which requires high reliability, be sure to design a circuit to which an external $\overline{\text{RESET}}$ signal can be input. Since the $\overline{\text{RESET}}$ pin is also used for setting the test mode, connect it to V_{DD} directly when not used.

Caution To fix the I/O mode, pull-up resistors that can be specified with the software, and output level of a pin, it is recommended that they should be specified repeatedly within a loop in a program.

1.5 NOTES ON USE OF THE $\overline{\text{RESET}}$ AND P1B₀ PINS (FOR NORMAL MODE ONLY)

The $\overline{\text{RESET}}$ pin has the test mode selecting function for testing the internal operation of the μPD17P136A (IC test), besides the functions shown in Section 1.1.

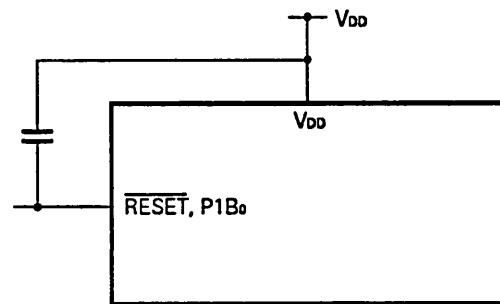
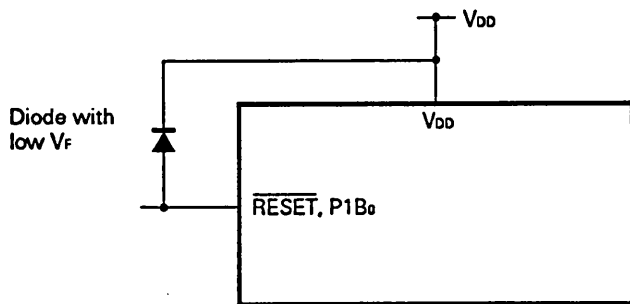
The P1B₀ pin can be used as the V_{PP} pin in the program memory write/verify mode.

Applying a voltage exceeding V_{DD} to the $\overline{\text{RESET}}$ and/or P1B₀ pin causes the μPD17P136A to enter the test mode. When noise exceeding V_{DD} comes in during normal operation, the device is switched to the test mode.

For example, if the wiring from the $\overline{\text{RESET}}$ or P1B₀ pin is too long, noise may be induced on the wiring, causing this mode switching.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- Connect a diode with low V_f between the pin and V_{DD}.
- Connect a capacitor between the pin and V_{DD}.



2. DIFFERENCES BETWEEN THE μPD17134A, μPD17136A, AND μPD17P136A

The μPD17P136A is a one-time PROM version of the μPD17136A, in which the internal masked ROM is replaced with a one-time PROM.

Table 2-1 lists the differences between the μPD17134A, μPD17136A, and μPD17P136A.

The μPD17P136A has the same CPU functions and internal peripheral hardware as those of μPD17134A and μPD17136A except for its program memory, program size, address register size, and mask option.

Part of electrical characteristics is also different between these products. For details of the electrical characteristics, refer to the data sheet of each product.

Table 2-1 Differences between the μPD17134A, μPD17136A, and μPD17P136A

Item	μPD17134A	μPD17136A	μPD17P136A
ROM	Masked ROM		One-time PROM
	1024 × 16 bits (0000H-03FFH)	2048 × 16 bits (0000H-07FFH)	
Program counter (PC)	10 bits	11 bits	
Address register (AR)			
Address stack register			
Pull-up resistors of P0D, P1A, P1B, and RESET pins	Mask option		Not provided
V _{PP} and operation mode selection pins	Not provided		Provided
Quality grade	Standard	<ul style="list-style-type: none"> • Standard (μPD17136A) • Special (μPD17136A(A)) (μPD17136A(A1)) 	Standard

Caution Although a PROM product is highly compatible with a masked ROM product in respect of functions, they differ in internal ROM circuits and part of electrical characteristics. Before changing the PROM product to the masked ROM product in an application system, evaluate the system carefully using the masked ROM product.

3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P136A's internal program memory consists of a 2048 × 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in Table 3-1. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Table 3-1 Pins Used When Writing to Program Memory or Verifying Its Contents

Pin	Function
V _{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.
V _{DD}	Pin for the power supply. +6 V is applied to this pin when writing to program memory or verifying its contents.
RESET	System reset input pin. Apply the specific signal to this pin to initialize the conditions of the microcontroller before switching to the program memory write/verify mode.
CLK	Input pin for address update clocks used when writing to program memory or verifying its contents. Input of four pulses to this pin updates the address of the program memory.
MD ₀ - MD ₃	Input pins that select an operation mode when writing to program memory or verifying its contents
D ₀ - D ₇	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

3.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, RESET = 0 V), the μPD17P136A enters program memory write/verify mode. A specific operating mode is then selected by setting the MD₀ through MD₃ pins as follows. Connect each pin not listed in Table 3-1 to ground through a pull-down register. (However, the OSC₀ pin must be left open.)

Table 3-2 Specification of Operating Modes

Operating mode specification						Operating mode
V _{PP}	V _{DD}	MD ₀	MD ₁	MD ₂	MD ₃	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

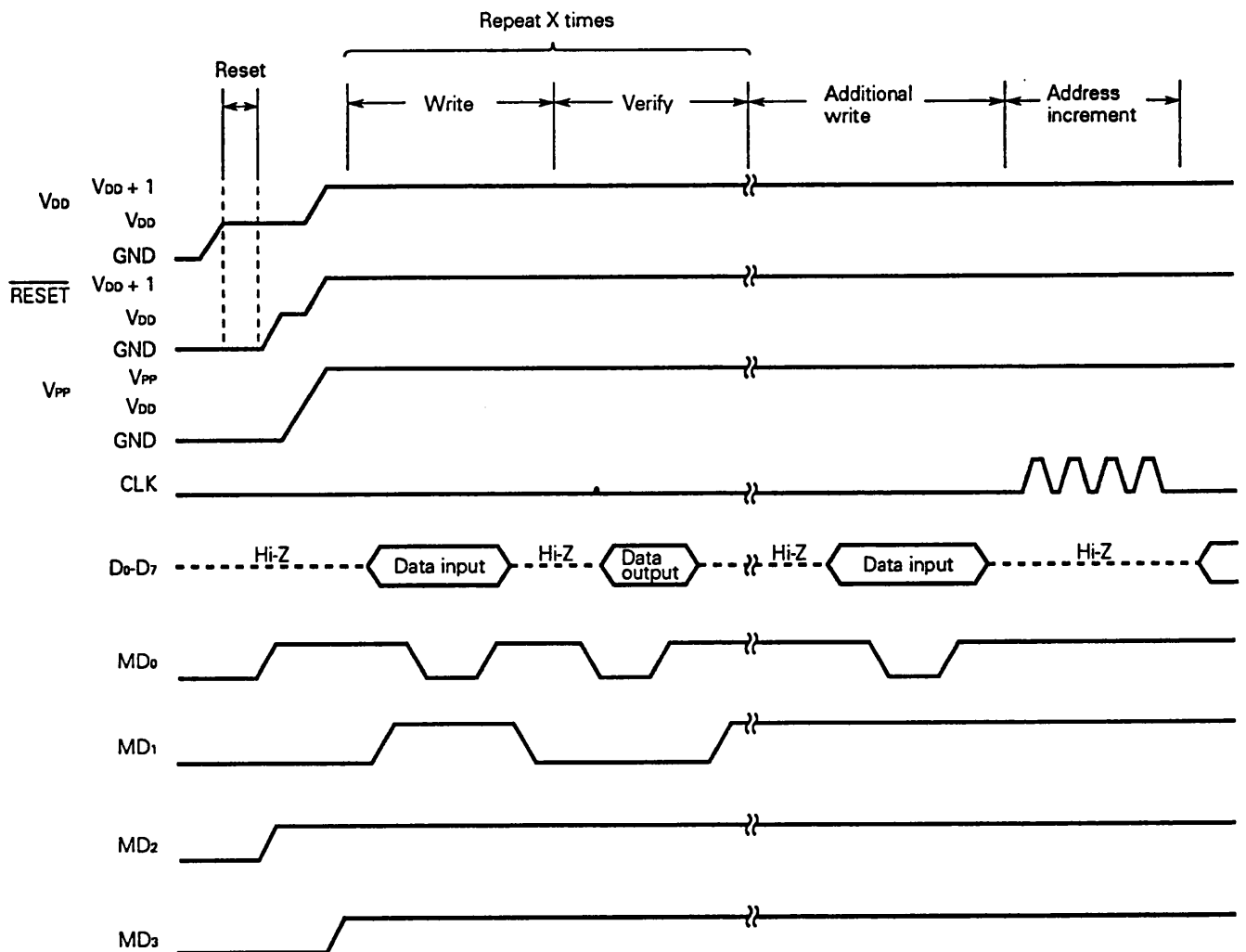
Remark x: Don't care. L (low) or H (high)

3.2 WRITING PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

- (1) Connect all unused pins to GND through resistors. Apply a low-level signal to the CLK pin.
- (2) Apply 5 V to V_{DD} and apply a low-level signal to the V_{PP} and \overline{RESET} pins.
- (3) Wait 10 μs . Then apply 5 V to \overline{RESET} .
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to V_{DD} and \overline{RESET} , and 12.5 V to V_{PP} .
- (6) Select program inhibit mode.
- (7) Write data in 1-ms write mode.
- (8) Select program inhibit mode.
- (9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
- (10) Perform additional write for X (number of repetitions of steps (7) to (9)) \times 1 ms.
- (11) Select program inhibit mode.
- (12) Increment the program memory address by one on reception of four pulses on the CLK pin.
- (13) Repeat steps (7) to (12) until the last address is reached.
- (14) Select program memory address clear mode.
- (15) Apply 5 V to the V_{DD} and V_{PP} pins.
- (16) Turn power off.

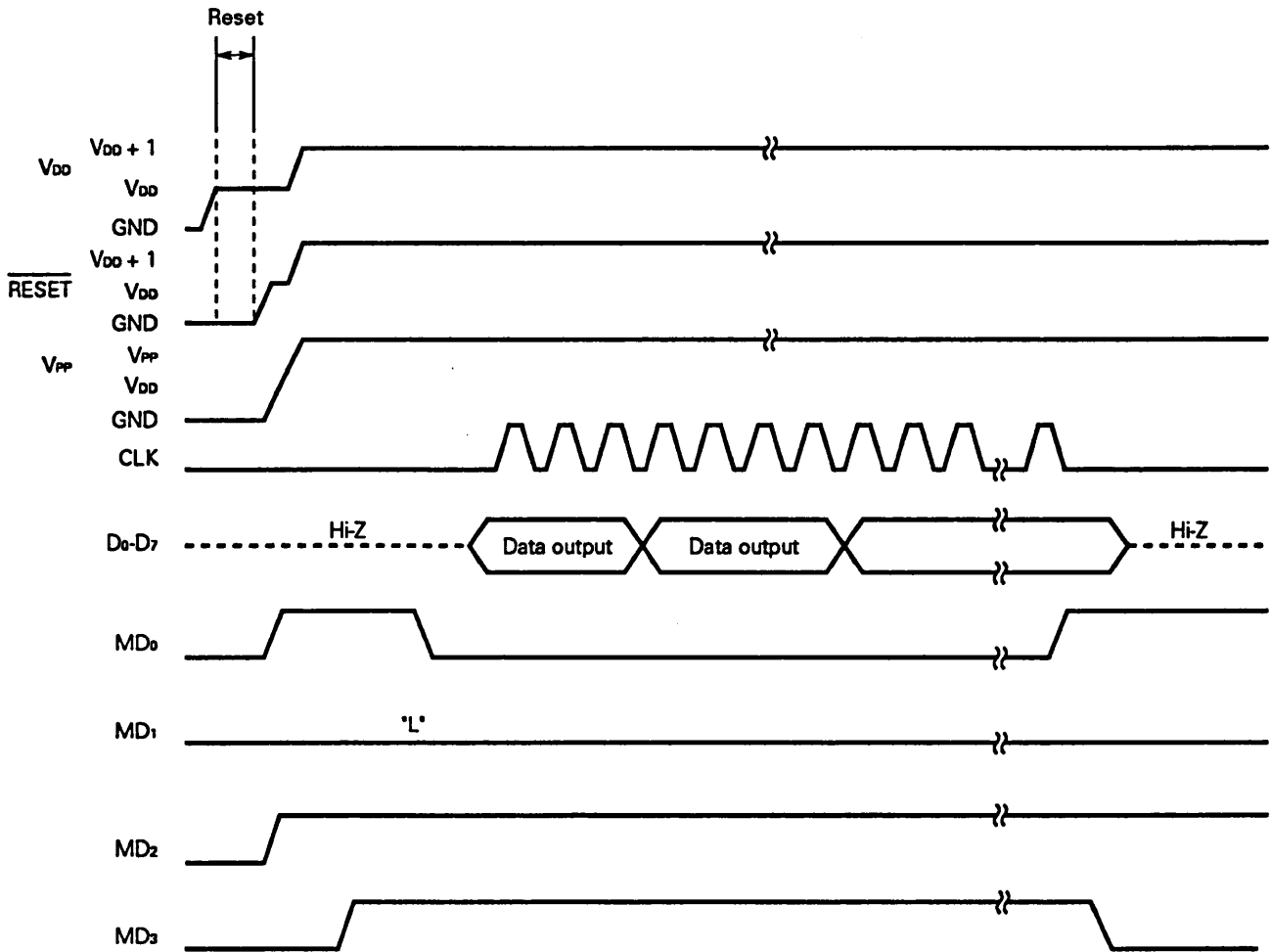
A timing chart for program memory writing steps (2) to (12) is shown below.



3.3 READING PROGRAM MEMORY

- (1) Connect all unused pins to GND through resistors. Apply a low-level signal to the CLK pin.
- (2) Apply 5 V to V_{DD} and apply a low-level signal to the V_{PP} and \overline{RESET} pins.
- (3) Wait 10 μs . Then apply 5 V to \overline{RESET} .
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to V_{DD} and \overline{RESET} , and 12.5 V to V_{PP} .
- (6) Select program inhibit mode.
- (7) Select verify mode. Data is output sequentially one address at a time for every four input clock pulses on the CLK.
- (8) Select program inhibit mode.
- (9) Select program memory address clear mode.
- (10) Apply 5 V to the V_{DD} and V_{PP} pins.
- (11) Turn power off.

A timing chart for program memory reading steps (2) to (9) is shown below.



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions	Rated value	Unit	
Supply voltage	V _{DD}		-0.3 to +7.0	V	
PROM supply voltage	V _{PP}		-0.3 to +13.5	V	
Analog supply voltage	V _{ADC}	V _{ADC} = V _{DD} ± 0.3 V	-0.3 to +7.0	V	
Input voltage	V _I	P0A, P0B, P0C, P1B, INT, RESET	-0.3 to V _{DD} + 0.3	V	
		P0D, P1A	-0.3 to +11.0	V	
Output voltage	V _O	P0A, P0B, P0C	-0.3 to V _{DD} + 0.3	V	
		P0D, P1A	-0.3 to +11.0	V	
High-level output current	I _{OH}	Each of P0A, P0B, and P0C	-15	mA	
		Total of all output pins	-30	mA	
Low-level output current	I _{OL}	Each of P0A, P0B, and P0C	15	mA	
		Each of P0D and P1A	30	mA	
		Total of all output pins	100	mA	
Operating ambient temperature	T _A		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	
Allowable dissipation	P _d	T _A = 85 °C	28-pin plastic shrink DIP	140	mW
			28-pin plastic SOP	85	

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

RECOMMENDED POWER VOLTAGE RANGE (T_A = -40 to +85 °C)

Parameter	Conditions	Min.	Typ.	Max.	Unit
CPU ^{Note}		2.7		5.5	V
A/D converter	Absolute accuracy : ±1.5 LSB or less	4.5		5.5	V
Zerocross detection circuit	Zerocross accuracy: A _{zx} = 120 mV or less	4.5		5.5	V
Power-on/power-down reset circuit	Rising time of the power voltage (V _{DD} = 0 → 2.7 V) : 8192t _{cy} or less	4.5		5.5	V

Note Excluding the A/D converter, power-on/power-down reset circuit, and zerocross detection circuit

Caution In the program memory write/verify mode, the voltage used for programming is applied to pin No. 17, P1B₀/V_{PP}. If a voltage of V_{DD} plus 0.3 V or more is applied to this pin in the normal operation mode, the microcontroller may crash. Design the circuit so that a voltage of this magnitude is never applied to the pin.

Remark t_{cy} = 16/f_{cc} (f_{cc}: frequency of system clock oscillator)

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85 °C)

Parameter	Symbol	Conditions		Min.	Typ.	Max	Unit	
High-level input voltage	V _{IH1}	P0A, P0B, P0C, P1B		0.7V _{DD}		V _{DD}	V	
	V _{IH2}	P0D, P1A		0.7V _{DD}		9	V	
	V _{IH3}	RESET, SCK, SI, INT		0.8V _{DD}		V _{DD}	V	
Low-level input voltage	V _{IL1}	P0A, P0B, P0C, P1B		0		0.3V _{DD}	V	
	V _{IL2}	P0D, P1A, RESET, SCK, SI, INT		0		0.2V _{DD}	V	
High-level output voltage	V _{OH}	P0A, P0B, P0C ^{Note 1}	V _{DD} = 4.5 to 5.5 V I _{OH} = -1.0 mA	V _{DD} - 0.3			V	
			V _{DD} = 2.7 to 4.5 V I _{OH} = -0.5 mA	V _{DD} - 0.3			V	
Low-level output voltage	V _{OL1}	P0A, P0B, P0C, P0D, P1A	V _{DD} = 4.5 to 5.5 V I _{OL} = 1.0 mA			0.3	V	
			V _{DD} = 2.7 to 4.5 V I _{OL} = 0.5 mA			0.3	V	
	V _{OL2}	P0D, P1A	V _{DD} = 4.5 to 5.5 V I _{OL} = 15 mA			1.0	V	
			V _{DD} = 2.7 to 4.5 V I _{OL} = 15 mA			2.0	V	
High-level input leakage current	I _{LH1}	P0A, P0B, P0C, P0D, P1A, P1B V _{IN} = V _{DD}				3	μA	
	I _{LH2}	P0D, P1A, V _{IN} = 9 V				10	μA	
Low-level input leakage current	I _{LL}	P0A, P0B, P0C, P0D, P1A, P1B V _{IN} = 0 V				-5	μA	
High-level output leakage current	I _{LOH1}	P0A, P0B, P0C, P0D, P1A V _{OUT} = V _{DD}				3	μA	
	I _{LOH2}	P0D, P1A, V _{OUT} = 9 V				10	μA	
Low-level output leakage current	I _{LOL}	P0A, P0B, P0C, P0D, P1A V _{OUT} = 0 V				-5	μA	
Built-in pull-up resistor	R _{PULL}	P0A, P0B		50	100	200	kΩ	
Power supply current ^{Note 2}	I _{DD1}	Oper- ating mode	f _{CC} = 2.0 MHz	V _{DD} = 5 V ±10 %		2.0	4.0	mA
				V _{DD} = 3 V ±10 %		1.0	2.5	mA
			f _{CC} = 1.0 MHz	V _{DD} = 5 V ±10 %		1.2	2.4	mA
				V _{DD} = 3 V ±10 %		0.7	2.2	mA
			f _{CC} = 500 kHz	V _{DD} = 5 V ±10 %		1.0	2.0	mA
				V _{DD} = 3 V ±10 %		0.5	2.0	mA
	I _{DD2}	HALT mode	f _{CC} = 2.0 MHz	V _{DD} = 5 V ±10 %		1.7	3.5	mA
				V _{DD} = 3 V ±10 %		0.9	2.4	mA
			f _{CC} = 1.0 MHz	V _{DD} = 5 V ±10 %		1.0	2.0	mA
				V _{DD} = 3 V ±10 %		0.6	2.1	mA
			f _{CC} = 500 kHz	V _{DD} = 5 V ±10 %		0.8	1.6	mA
				V _{DD} = 3 V ±10 %		0.5	2.0	mA
I _{DD3}	STOP mode	V _{DD} = 5 V ±10 %			12	50	μA	
		V _{DD} = 3 V ±10 %			10	45	μA	

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Notes 1. When a pull-up resistor is not incorporated

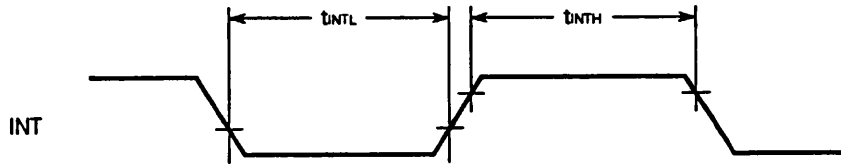
2. This current excludes the current which flows through the A/D converter, zerocross detection circuit, and built-in pull-up resistors.

AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85 °C)

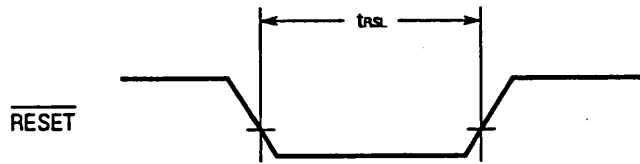
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU clock cycle time (instruction execution time)	t _{cy}		6.6		41	μs
INT high/low level width (external interrupt input)	t _{INTH}	V _{DD} = 4.5 to 5.5 V	10			μs
	t _{INTL}		50			μs
RESET low level width	t _{RSL}	V _{DD} = 4.5 to 5.5 V	10			μs
			50			μs

Remark t_{cy} = 16/f_{cc} (f_{cc}: frequency of system clock oscillator)

Interrupt Input Timing



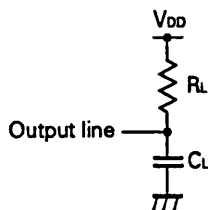
RESET Input Timing



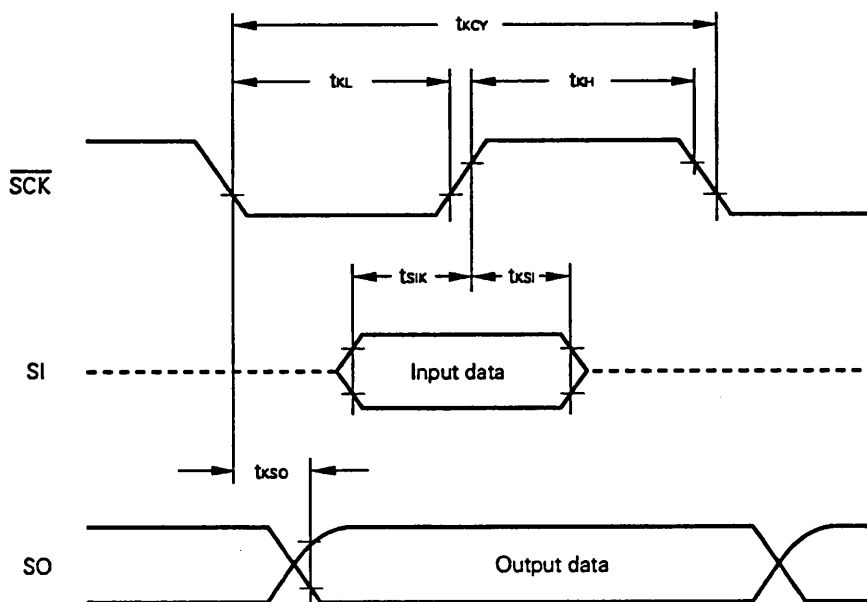
★ SERIAL TRANSFER OPERATION ($V_{DD} = 2.7$ to 5.5 V, $T_A = -40$ to $+85$ °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit		
SCK cycle time	t_{KCY}	Input	$V_{DD} = 4.5$ to 5.5 V	2.0			μs	
				10			μs	
		Output	$R_L = 1$ kΩ, $C_L = 100$ pF	$V_{DD} = 4.5$ to 5.5 V	8.0			μs
					16			μs
SCK high/low level width	t_{KH} , t_{KL}	Input	$V_{DD} = 4.5$ to 5.5 V	1.0			μs	
				5.0			μs	
		Output	$R_L = 1$ kΩ, $C_L = 100$ pF	$V_{DD} = 4.5$ to 5.5 V	$t_{KCY}/2-0.6$			μs
					$t_{KCY}/2-1.2$			μs
SI setup time (with respect to SCK↑)	t_{SIK}		100			ns		
SI hold time (with respect to SCK↑)	t_{SIL}		100			ns		
Delay from SCK↓ to SO	t_{KSO}	$R_L = 1$ kΩ, $C_L = 100$ pF	$V_{DD} = 4.5$ to 5.5 V			0.8	μs	
							1.4	μs

Remark R_L : a resistive load for the output line
 C_L : a capacitive load for the output line



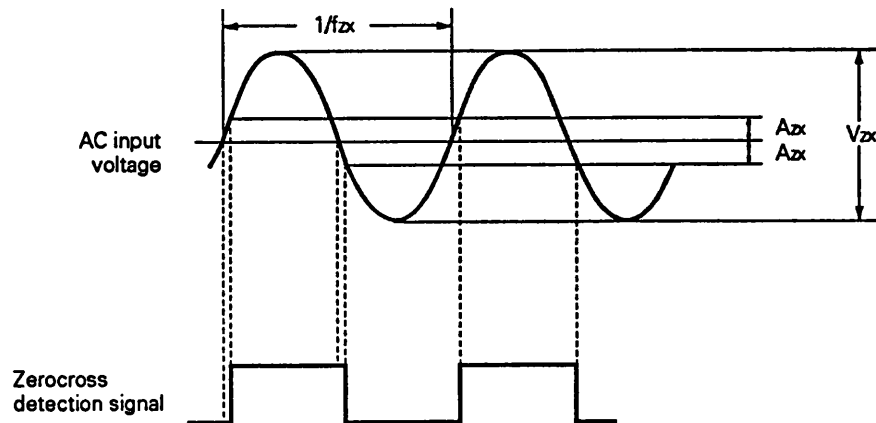
Serial transfer timing



ZEROCROSS DETECTION CIRCUIT CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Zerocross detection input level	V _{zx}	AC input, coupling capacity of 1 μF	1.0		3.0	V _{PP}
Zerocross detection input frequency	f _{zx}		40	50 or 60	1000	Hz
Zerocross accuracy	A _{zx}	50 Hz or 60 Hz		40	120	mV
Zerocross detection circuit current	I _{zx}	There is no AC input		15	90	μA

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Caution The zerocross detection signal delays behind the AC input signal at the rising and falling edges indicated by A_{zx} in the above figure. Actually, however, it may advance. The zerocross detection point does not change in a uniform manner.

A/D CONVERTER CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85 °C, V_{ADC} = V_{DD} ±0.5 %)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Absolute accuracy ^{Note 1}		V _{ADC} = V _{DD}			±1.5	LSB
ADC circuit current	I _{ADC}			1.5	2.0	mA
Conversion time ^{Note 2}	t _{CONV}				25t _{cy}	μs

Notes 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to when ADCEND is set to 1 (200 μs at f_{cc} = 2 MHz)

Remark t_{cy} = 16/f_{cc} (f_{cc}: frequency of system clock oscillator)

CHARACTERISTICS OF THE POWER-ON/POWER-DOWN RESET CIRCUITS (T_A = -40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power voltage rise time required for the power-on reset function	t _{PON}	V _{DD} = 0 → 2.7 V The power voltage (V _{DD}) must change from ground level to 2.7 V.			8192t _{cy}	μs
Voltage detected by the power-down reset circuit	V _{PDR}	When PDRESEN = 1		3.5	4.5	V

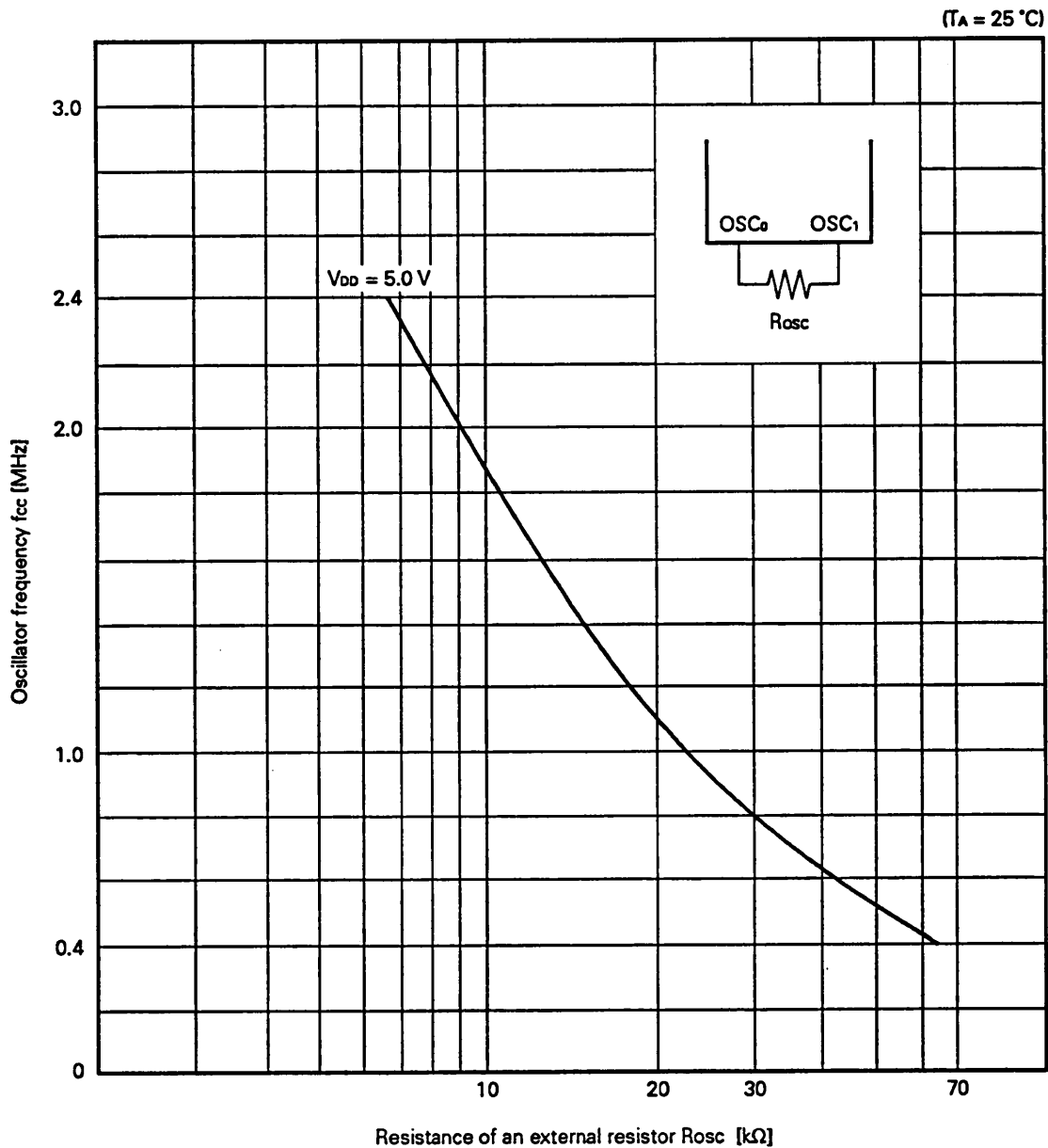
Remark t_{cy} = 16/f_{cc} (f_{cc}: frequency of system clock oscillator)

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = -40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System clock oscillation frequency	f _{cc}	V _{DD} = 4.5 to 5.5 V, R _{osc} = 9.1 kΩ	1.6	2	2.4	MHz
		V _{DD} = 4.5 to 5.5 V, R _{osc} = 22 kΩ	0.8	1	1.2	MHz
		V _{DD} = 2.7 to 5.5 V, R _{osc} = 22 kΩ	0.6	1	1.2	MHz
		V _{DD} = 2.7 to 3.3 V, R _{osc} = 47 kΩ	400	500	600	kHz

Caution The tolerance of a resistance is not considered in the conditions.

f_{cc} vs R_{osc} (for reference)



DC PROGRAMMING CHARACTERISTICS (T_A = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage high	V _{IH1}	Except CLK	0.7V _{DD}		V _{DD}	V
	V _{IH2}	CLK	V _{DD} - 0.5		V _{DD}	V
Input voltage low	V _{IL1}	Except CLK	0		0.3V _{DD}	V
	V _{IL2}	CLK	0		0.4	V
Input leakage current	I _I	V _{IN} = V _{IL} or V _{IH}			10	μA
Output voltage high	V _{OH}	I _{OH} = -1 mA	V _{DD} - 1.0			V
Output voltage low	V _{OL}	I _{OL} = 1.6 mA			0.4	V
V _{DD} power supply current	I _{DD}				30	mA
V _{PP} power supply current	I _{PP}	MD0 = V _{IL} , MD1 = V _{IH}			30	mA

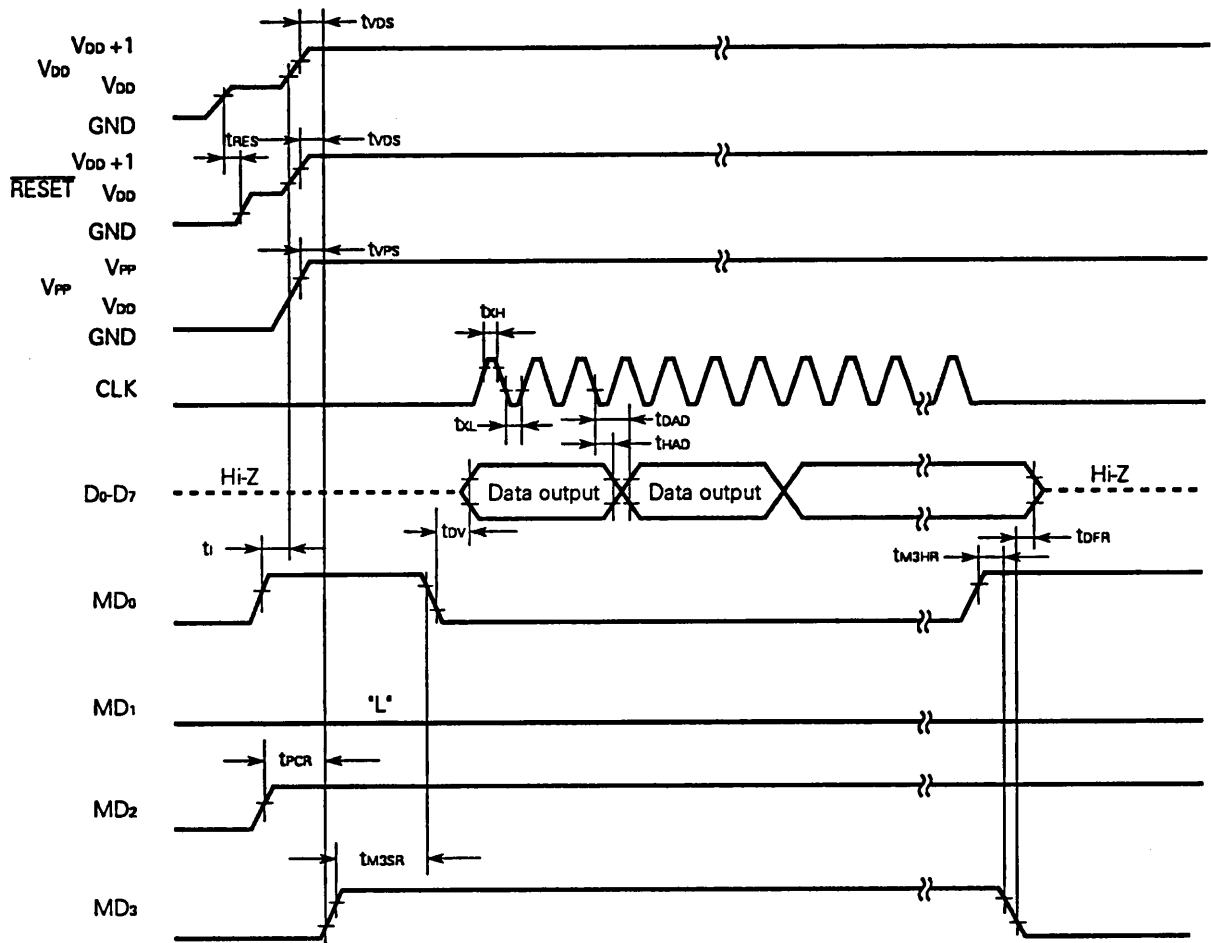
- Cautions**
1. V_{PP} must be under +13.5 V including overshoot.
 2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

AC PROGRAMMING CHARACTERISTICS (T_A = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

Parameter	Symbol	Note 1	Conditions	Min.	Typ.	Max.	Unit
Address setup time ^{Note 2} to MD0↓	t _{AS}	t _{AS}		2			μs
MD1 setup time to MD0↓	t _{M1S}	t _{OES}		2			μs
Data setup time to MD0↓	t _{DS}	t _{DS}		2			μs
Address hold time ^{Note 2} to MD0↑	t _{AH}	t _{AH}		2			μs
Data hold time to MD0↑	t _{DH}	t _{DH}		2			μs
Data output float delay time from MD0↑	t _{DF}	t _{DF}		0		130	ns
V _{PP} setup time to MD3↑	t _{VPS}	t _{VPS}		2			μs
V _{DD} setup time to MD3↑	t _{VDS}	t _{VCS}		2			μs
Initial program pulse width	t _{PW}	t _{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t _{OPW}	t _{OPW}		0.95		21.0	ms
MD0 setup time to MD1↑	t _{MOS}	t _{CES}		2			μs
Data output delay time from MD0↓	t _{DV}	t _{DV}	MD0 = MD1 = V _{IL}			1	μs
MD1 hold time to MD0↑	t _{M1H}	t _{OEH}	t _{M1H} + t _{M1R} ≥ 50 μs	2			μs
MD1 recovery time to MD0↓	t _{M1R}	t _{OR}		2			μs
Program counter reset time	t _{PCR}	-		10			μs
CLK input high, low level range	t _{XH} , t _{XL}	-		0.125			μs
CLK input frequency	f _X	-				2	MHz
Initial mode set time	t _I	-		2			μs
MD3 setup time to MD1↑	t _{M3S}	-		2			μs
MD3 hold time to MD1↓	t _{M3H}	-		2			μs
MD3 setup time to MD0↓	t _{M3SR}	-	When reading program memory	2			μs
Data output delay time from address ^{Note 2}	t _{DAD}	t _{ACC}	When reading program memory			2	μs
Data output hold time from address ^{Note 2}	t _{HAD}	t _{OH}	When reading program memory	0		130	ns
MD3 hold time to MD0↑	t _{M3HR}	-	When reading program memory	2			μs
Data output float delay time from MD3↓	t _{DFR}	-	When reading program memory			2	μs
Reset setup time	t _{RES}			10			μs

- Notes**
1. Symbols used for μPD27C256A (The μPD27C256A is used only for maintenance.)
 2. The internal address is incremented by one at the falling edge of the third clock (CLK) input.

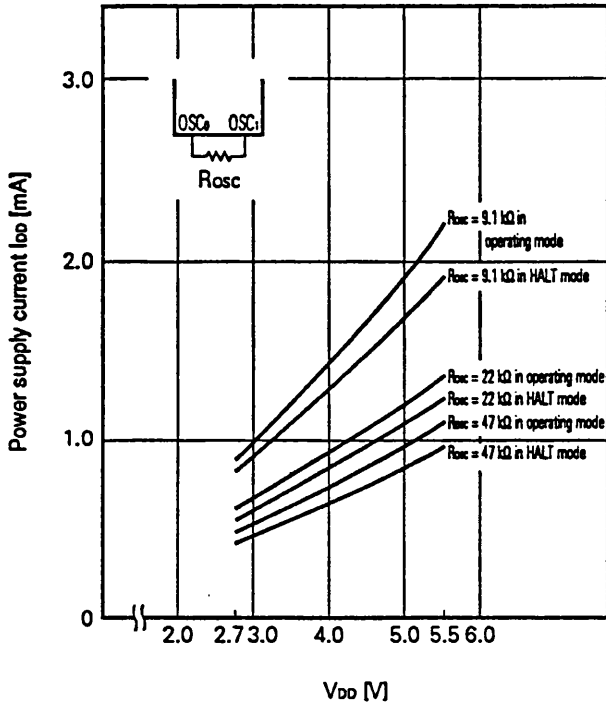
Read Program Memory Timing



★ 5. CHARACTERISTIC CURVES (FOR REFERENCE)

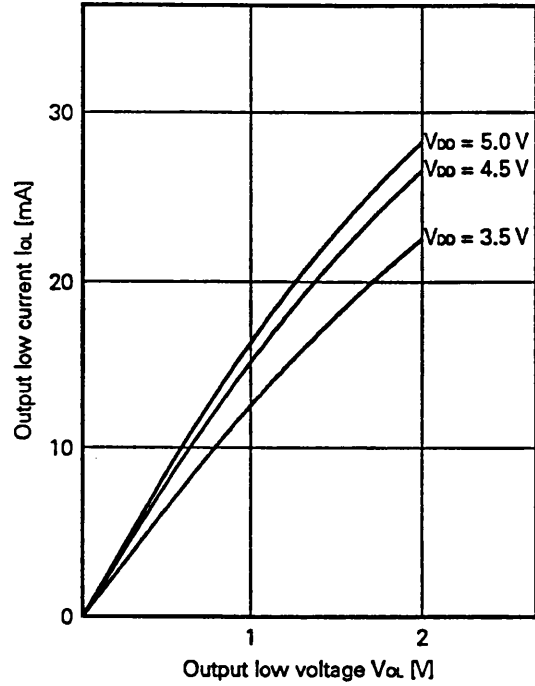
I_{DD} vs V_{DD}

(T_A = 25 °C)



I_{OL} vs V_{OL} 2 (P0D, P1A)

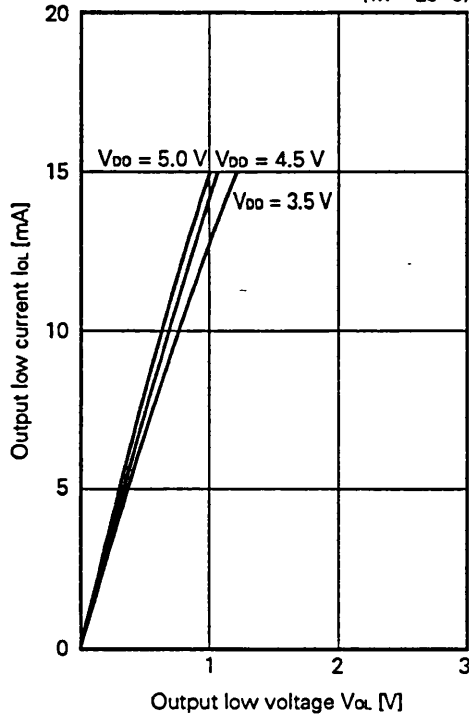
(T_A = 25 °C)



Caution The absolute maximum rating of current is 30 mA per pin.

I_{OL} vs V_{OL} 1 (P0A, P0B, P0C)

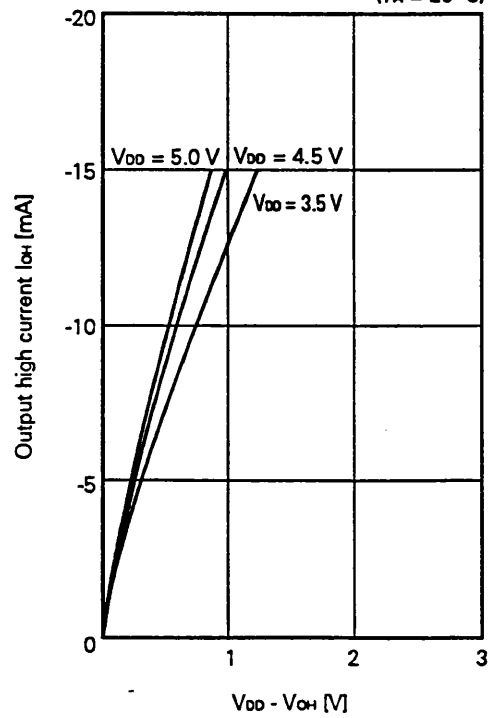
(T_A = 25 °C)



Caution The absolute maximum rating of current is 15 mA per pin.

I_{OH} vs (V_{DD} - V_{OH})

(T_A = 25 °C)

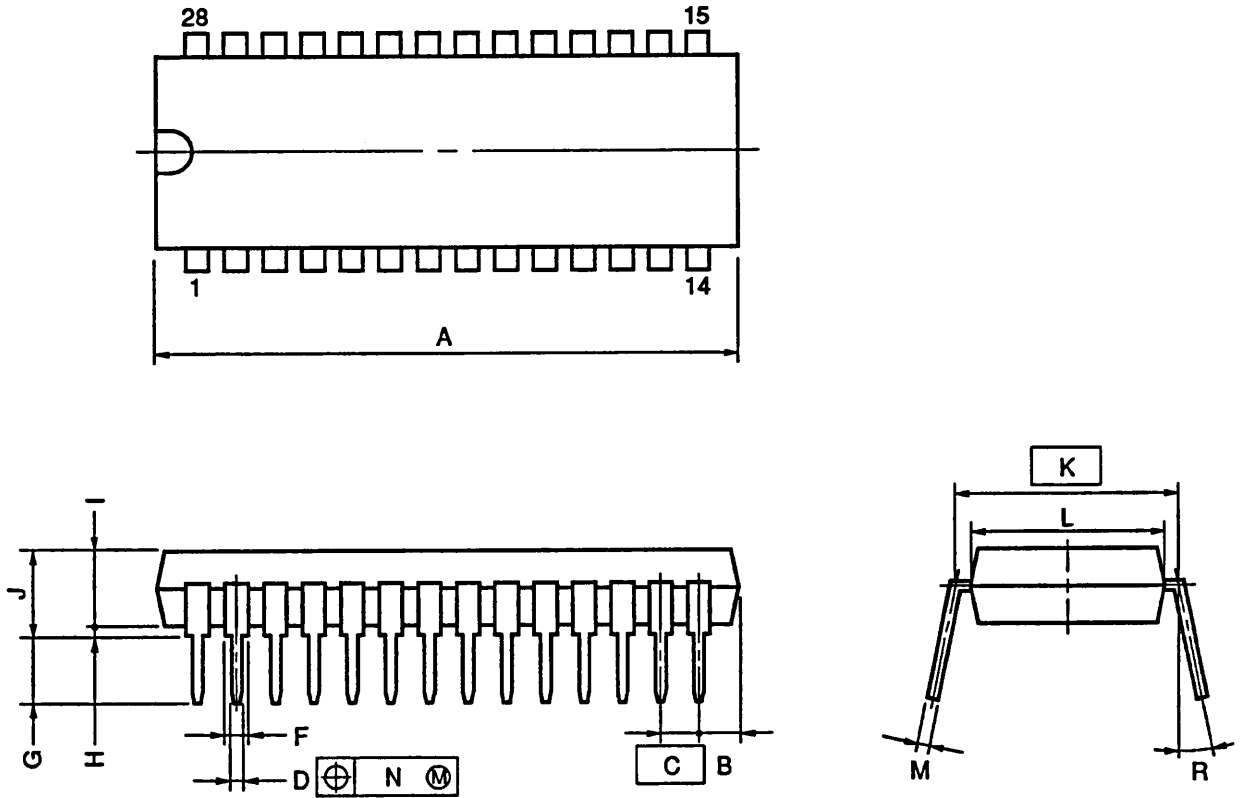


Caution The absolute maximum rating of current is -15 mA per pin.

6. PACKAGE DRAWINGS

PACKAGE DIMENSIONS OF THE 28-PIN PLASTIC SHRINK DIP (400 mil) (UNIT: mm)

28 PIN PLASTIC SHRINK DIP (400 mil)



NOTES

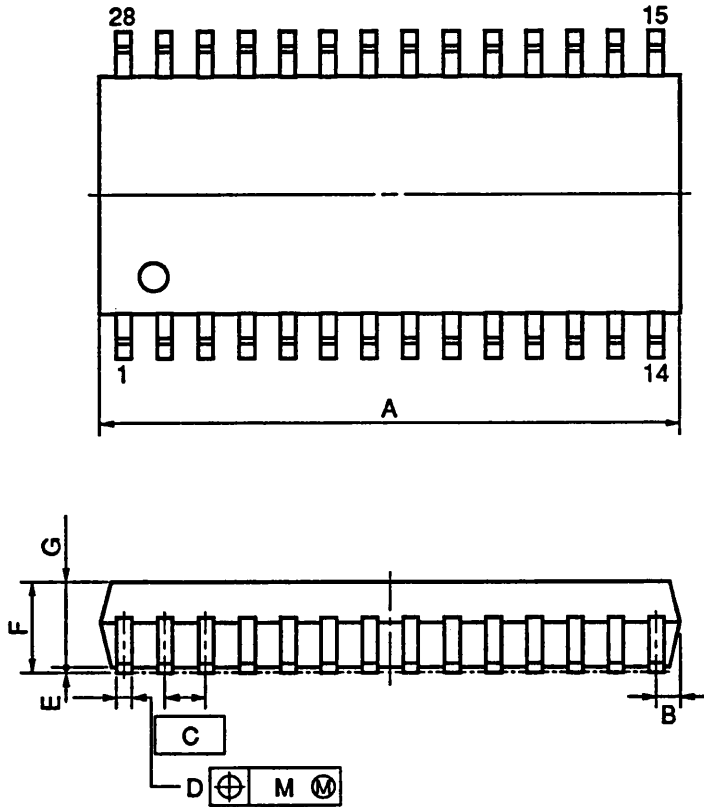
- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

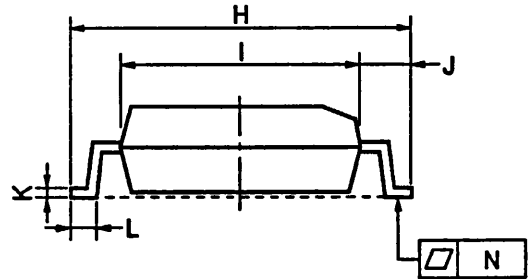
S28C-70-400B-1

PACKAGE DIMENSIONS OF THE 28-PIN PLASTIC SOP (375 mil) (UNIT: mm)

28 PIN PLASTIC SOP (375 mil)



detail of lead end



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.1±0.1	0.004±0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3±0.3	0.406 ^{+0.012} _{-0.013}
I	7.2	0.283
J	1.6	0.063
K	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.002}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.12	0.005
N	0.15	0.006
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

P28GM-50-375B-3

7. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD17P136A.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 7-1 Soldering Conditions for Surface-Mount Devices

μPD17P136AGT: 28-pin plastic SOP (375 mil)

Soldering process	Soldering conditions
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for one side of a device)

Table 7-2 Soldering Conditions for Through Hole Mount Devices

μPD17P136ACT: 28-pin plastic shrink DIP (400 mil)

Soldering process	Soldering conditions
Wave soldering (only for pins)	Solder temperature: 260 °C or less Flow time: 10 seconds or less
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each pin)

Caution In wave soldering, apply solder only to the pins. Care must be taken that jet solder does not come in contact with the main body of the package.

APPENDIX A μPD17134A SUB-SERIES PRODUCTS LIST

Item	Product name					
	μPD17134A	μPD17136A	μPD17P136A	μPD17135A	μPD17137A	μPD17P137A
ROM size	Masked ROM		One-time PROM	Masked ROM		One-time PROM
	2 K bytes (1024 × 16 bits)	4 K bytes (2048 × 16 bits)		2 K bytes (1024 × 16 bits)	4 K bytes (2048 × 16 bits)	
RAM size	112 × 4 bits					
Number of I/O port lines	22 (Input/output pins: 20, Input pins: 1, Sensor input pins (INT pins): 1)					
External interrupt	1 (with sensor input)					
Analog input	8-bit A/D converter (4 channels) (Can be used in an application circuit where V _{DD} is 4.5 to 5.5 V)					
Timer	3 channels					
Serial interface	1 channel					
Stack	Five address stacks and three interrupt stacks					
Power-on/power-down reset circuit	Built-in (Can be used in an application circuit where V _{DD} is 5 V ±10 %)			Built-in (Can be used in an application circuit where V _{DD} is 5 V ±10 % and f _x is 400 kHz to 4 MHz)		
System clock	RC oscillation			Ceramic oscillation		
Instruction execution time	8 μs (at f _{cc} = 2 MHz)			2 μs (at f _x = 8 MHz)		
Standby function	HALT, STOP					
Supply voltage	V _{DD} = 2.7 to 5.5 V			V _{DD} = 2.7 to 5.5 V (at f _x = 400 kHz to 4 MHz) V _{DD} = 4.5 to 5.5 V (at f _x = 400 kHz to 8 MHz)		
Package	28-pin plastic shrink DIP (400 mil) 28-pin plastic SOP (375 mil)					
One time PROM product	μPD17P136A	-	-	μPD17P137A	-	-

I/O: Input/output

APPENDIX B DEVELOPMENT TOOLS

The following support tools are available for developing programs for the μPD17P136A.

Hardware

Name	Description
In-circuit emulator [IE-17-K IE-17K-ET ^{Note 1} EMU-17K ^{Note 2}]	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators applicable to the 17K series. The IE-17K and IE-17K-ET are connected to the PC-9800 series (host machine) or IBM PC/AT TM through the RS-232-C interface. The EMU-17K is inserted into the extension slot of the PC-9800 series (host machine). Use the system evaluation board (SE board) corresponding to each product together with one of these in-circuit emulators. SIMPLEHOST TM , a man machine interface, implements an advanced debug environment. The EMU-17K also enables user to check the contents of the data memory in real time.
SE board (SE-17134)	The SE-17134 is an SE board for the μPD17134A sub-series. It is used solely for evaluating the system. It is also used for debugging in combination with the in-circuit emulator.
Emulation probe (EP-17K28CT)	The EP-17K28CT is an emulation probe for the 17K series 28-pin shrink DIP (400 mil).
Emulation probe (EP-17K28GT)	The EP-17K28GT is an emulation probe for the 17K series 28-pin SOP (375 mil). Use this probe together with the conversion adapter EV-9500GT-28 ^{Note 3} , to check the target system with the corresponding SE board.
Conversion adapter (EV-9500GT-28 ^{Note 3})	The EV-9500GT-28 is an adapter for the 28-pin SOP (375 mil). Use this conversion adapter to connect the emulation probe, EP-17K28GT, to the target system.
PROM Programmer [AF-9703 ^{Note 4} AF-9704 ^{Note 4} AF-9705 ^{Note 4} AF-9706 ^{Note 4}]	The AF-9703, AF-9704, AF-9705, and AF-9706 are PROM writers for the μPD17P136A. Use one of these PROM writers with the program adapter, AF-9808F, to program the μPD17P136A.
Programmer adapter (AF-9808F ^{Note 4})	The AF-9808F is a socket unit for the μPD17P136A. It is used with the AF-9703, AF-9704, AF-9705, and AF-9706.

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Notes 1. Low-end model, operating on an external power supply

2. The EMU-17K is a product of IC Co., Ltd. Contact IC Co., Ltd. (Tokyo, 03-3447-3793) for details.
3. An EP-17K28GT is supplied together with two EV-9500GT-28s. A set of five EV-9500GT-28s is also available.
4. The AF-9703, AF-9704, AF-9705, AF-9706, and AF-9808F are products of Ando Electric Co., Ltd. Contact Ando Electric Co., Ltd. (Tokyo, 03-3733-1151) for details.

★ Software

Name	Description	Host machine	OS	Distribution media	Part number	
17K series assembler (AS17K)	AS17K is an assembler applicable to the 17K series. In developing μPD17P136A program, AS17K is used in combination with a device file (AS17136A).	PC-9800 series	MS-DOSTM	5.25-inch, 2HD	μS5A10AS17K	
				3.5-inch, 2HD	μS5A13AS17K	
		IBM PC/AT	PC DOSTM	5.25-inch, 2HC	μS7B10AS17K	
				3.5-inch, 2HC	μS7B13AS17K	
Device file (AS17136A)	AS17136A is a device file for the μPD17136A and μPD17P136A. It is used together with the assembler (AS17K) which is applicable to the 17K series.	PC-9800 series	MS-DOS	5.25-inch, 2HD	μS5A10AS17134Note	
				3.5-inch, 2HD	μS5A13AS17134Note	
		IBM PC/AT	PC DOS	5.25-inch, 2HC	μS7B10AS17134Note	
				3.5-inch, 2HC	μS7B13AS17134Note	
Support software (SIMPLEHOST)	SIMPLEHOST, running on the WindowsTM, provides man-machine-interface in developing programs by using a personal computer and the in-circuit emulator.	PC-9800 series	MS-DOS	Windows	5.25-inch, 2HD	μS5A10IE17K
					3.5-inch, 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10IE17K
					3.5-inch, 2HC	μS7B13IE17K

Note μSxxxxAS17134 contains AS17134A, AS17135A, AS17136A, and AS17137A.

Remark The following table lists the versions of the operating systems described in the above table.

OS	Versions
MS-DOS	Ver. 3.30 to Ver. 5.00ANote
PC DOS	Ver. 3.1 to Ver. 5.0Note
Windows	Ver. 3.0 to Ver. 3.1

Note MS-DOS versions 5.00 and 5.00A and PC DOS Ver. 5.0 are provided with a task swap function. This function, however, cannot be used in these software packages.

Cautions on CMOS Devices**① Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged. Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② CMOS-specific handling of unused input pins

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor. If handling of unused pins is documented, follow the instructions in the document.

③ Statuses of all MOS devices at initialization

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

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PC/AT and PC DOS are trademarks of IBM Corporation.

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.