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April 1st, 2010
Renesas Electronics Corporation

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4 BIT SINGLE-CHIP MICROCONTROLLER

The μ PD17P104 is a one-time PROM version of the μ PD17104, in which the internal masked ROM of the μ PD17104 is replaced with a one-time PROM that can be written to just once.

Since user programs can be written to the PROM, this microcontroller is suited for program evaluation and small-lot production of the μ PD17104, or for program evaluation of the μ PD17104L.

When reading this document, refer to the publications on the μ PD17104.

FEATURES

- 17K architecture : General registers
- Pin compatible with the μ PD17104 (except for PROM programming function)
- Internal one-time PROM : 1K byte (512 × 16 bits)
- Instruction execution time : 2 μ s (at f_x = 8 MHz, ceramic oscillation)
- Supply voltage : V_{DD} = 2.7 to 6.0 V (f_x = 500 kHz to 2 MHz)
 V_{DD} = 4.5 to 6.0 V (f_x = 500 kHz to 8 MHz)

APPLICATIONS

- Controlling electric appliances or toys
- Implementing circuitry consisting of general-purpose logic ICs, using a single chip

ORDERING INFORMATION

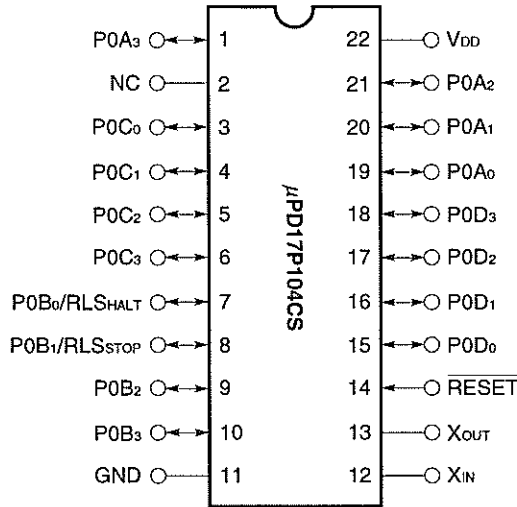
Part number	Package
μ PD17P104CS	22-pin plastic shrink DIP (300 mil)
μ PD17P104GS	24-pin plastic SOP (300 mil)

The information in this document is subject to change without notice.

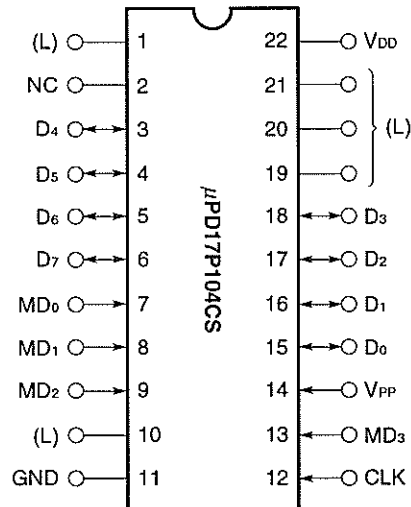
PIN CONFIGURATION (TOP VIEW)

22-pin plastic shrink DIP

(1) Normal operation mode



(2) PROM programming mode

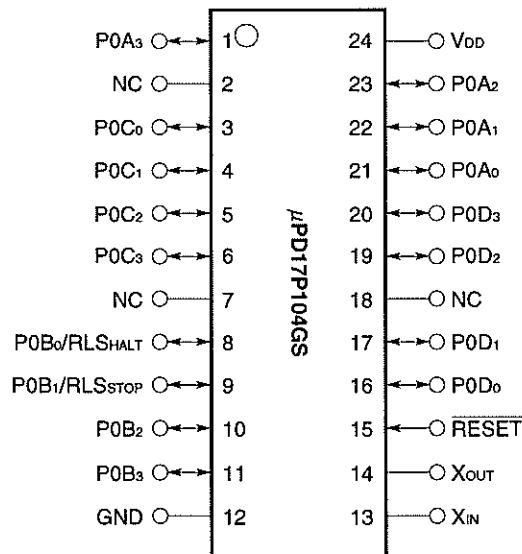


Caution The parentheses above indicate the level of the pins not used in PROM programming mode.

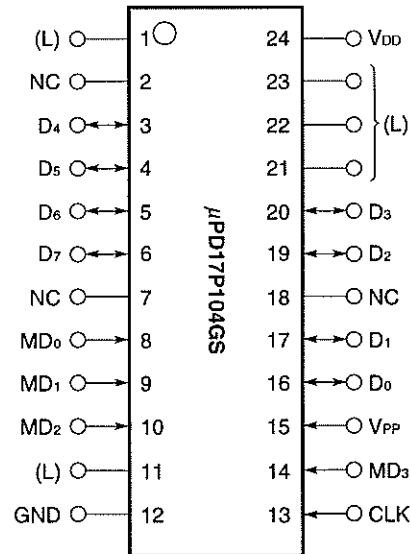
L: Connect each pin to ground through a pull-down resistor.

24-pin plastic SOP

(1) Normal operation mode



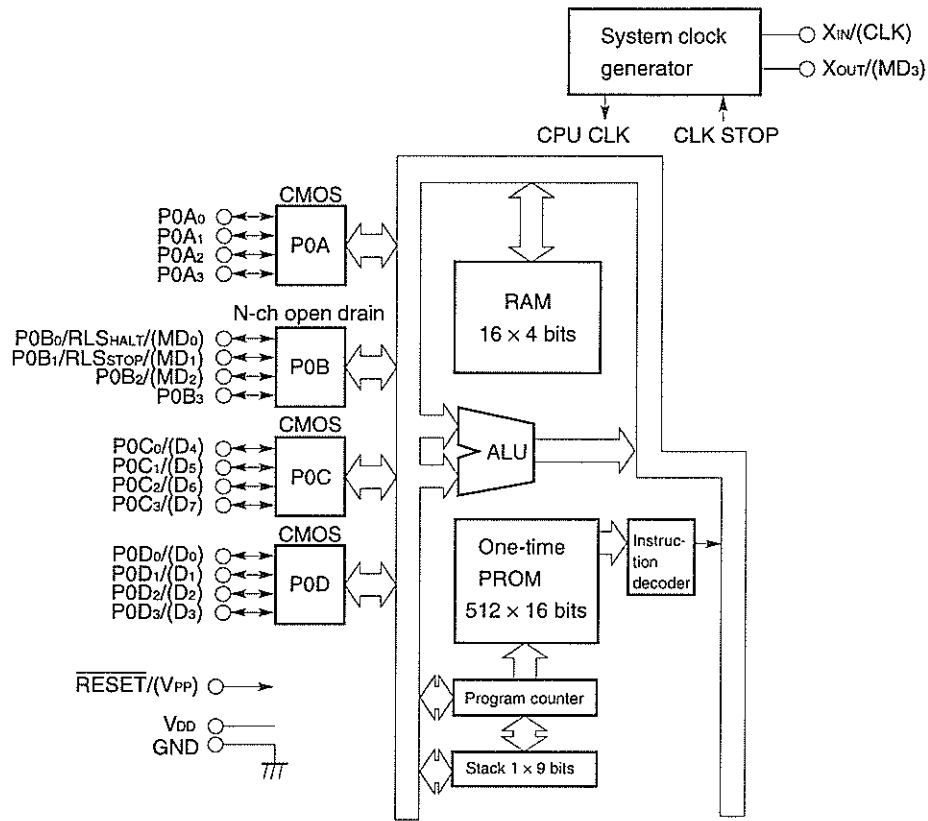
(2) PROM programming mode



Caution The parentheses above indicate the level of the pins not used in PROM programming mode.

L: Connect each pin to ground through a pull-down resistor.

BLOCK DIAGRAM



Remark Pin names enclosed in parentheses are used in PROM programming mode.

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1. PINS

1.1 PIN FUNCTIONS

- Port pins

PinNote	I/O	Function	PROM programming mode	Reset
P0A ₀ - P0A ₃	I/O	CMOS (push-pull) 4-bit I/O port (port 0A)	Must be pulled down	High impedance (input mode)
P0B ₀ /RLSHALT/(MD ₀)	I/O	For releasing HALT mode	Mode selection pin (MD ₀ - MD ₂)	High impedance (input mode)
P0B ₁ /RLSSTOP/(MD ₁)		For releasing STOP mode		
P0B ₂ /(MD ₂)		<ul style="list-style-type: none"> • N-ch open-drain 4-bit I/O port (port 0B) • Withstand voltage of 9 V 		
P0B ₃		Must be pulled down		
P0C ₀ /(D ₄) - P0C ₃ /(D ₇)	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	8-bit data I/O pin (D ₄ - D ₇)	High impedance (input mode)
P0D ₀ /(D ₀) - P0D ₃ /(D ₃)	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	8-bit data I/O pin (D ₀ - D ₃)	High impedance (input mode)

- Non-port pins

PinNote	I/O	Function	PROM programming mode
$\overline{\text{RESET}}/(V_{PP})$	Input	System reset input pin	+12.5 V is applied to this pin (V_{PP}).
V _{DD}	–	Power supply pin	Power supply pin (V _{DD}). +6 V is applied to this pin.
GND	–	GND pin	GND pin
X _{IN} /(CLK)	–	Pins for system clock generation	Program memory address update (CLK)
X _{OUT} /(MD ₃)	–		Mode selection pin (MD ₃)
NC	–	This pin is not internally connected.	

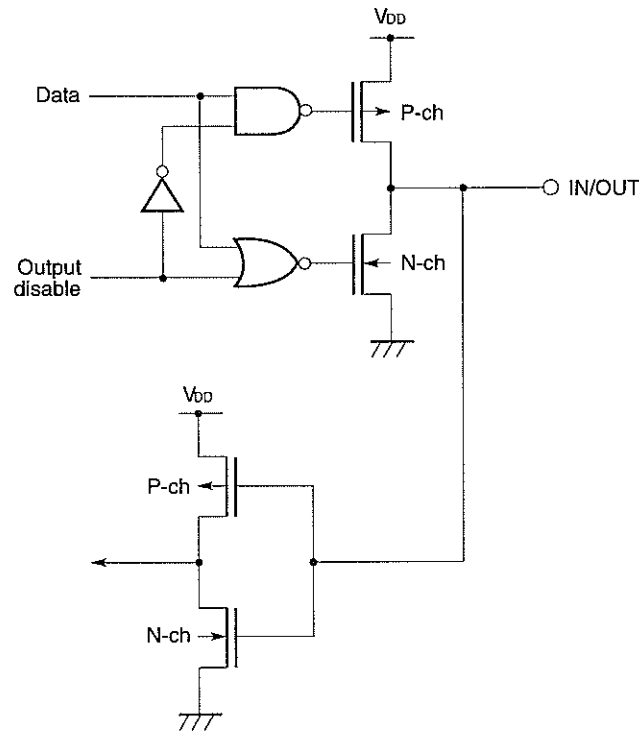
I/O: Input/output

Note Pin names enclosed in parentheses are used in PROM programming mode.

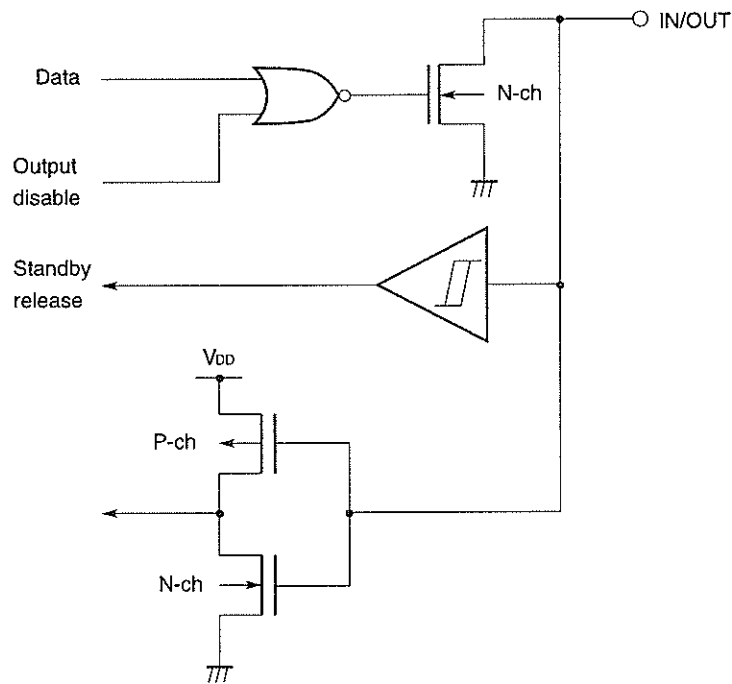
1.2 EQUIVALENT INPUT/OUTPUT CIRCUITS

Below are simplified diagrams of the equivalent input/output circuits.

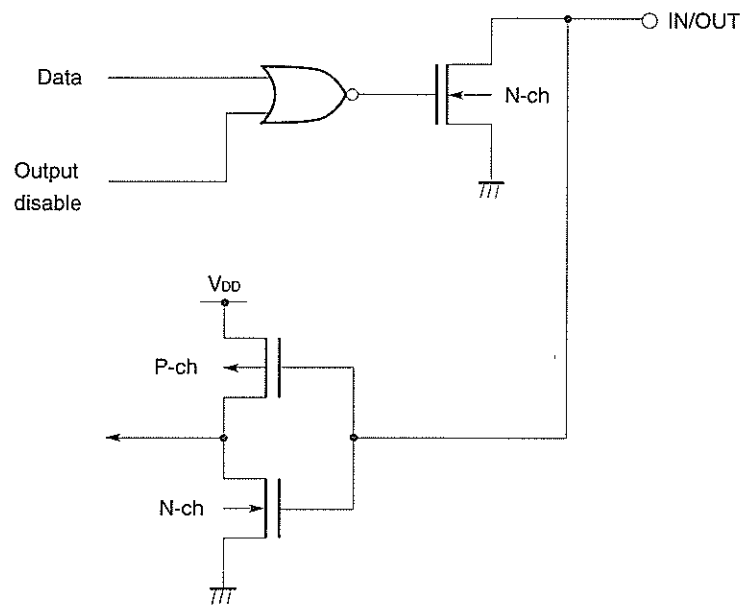
(1) P0A, P0C, and P0D



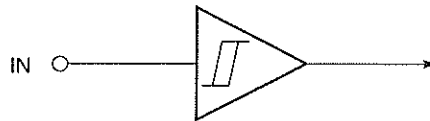
(2) P0B₀ and P0B₁



(3) P0B2 and P0B3



(4) RESET



1.3 HANDLING UNUSED PINS

In normal operation mode, connect unused pins as follows:

★ Table 1-1 Handling Unused Pins

Pin			Recommended conditions and handling	
			Internal	External
Port	Input mode	P0A, P0B, P0C, P0D	—	Connect to V _{DD} or ground through resistors for each pin. ^{Note}
	Output mode	P0A, P0C, P0D (CMOS ports)	—	Leave open.
		P0B (N-ch open-drain port)	Outputs low level.	Leave open.

Note When a pin is pulled up to V_{DD} (connected to V_{DD} through a resistor) or pulled down to ground (connected to ground through a resistor) outside the chip, take the driving capacity and maximum current consumption of a port into consideration. When using high-resistance pull-up or pull-down resistors, apply appropriate countermeasures to ensure that noise is not attracted by the resistors. Although the optimum pull-up or pull-down resistor varies with the application circuit, in general, a resistor of 10 to 100 kilohms is suitable.

Caution To fix the output level of a pin, it is recommended that it should be specified repeatedly within a loop in a program.

★ 1.4 NOTES ON USE OF THE $\overline{\text{RESET}}$ PIN (FOR NORMAL OPERATION MODE ONLY)

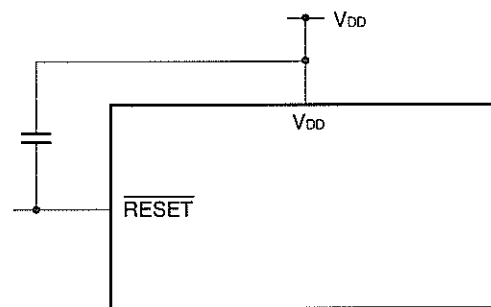
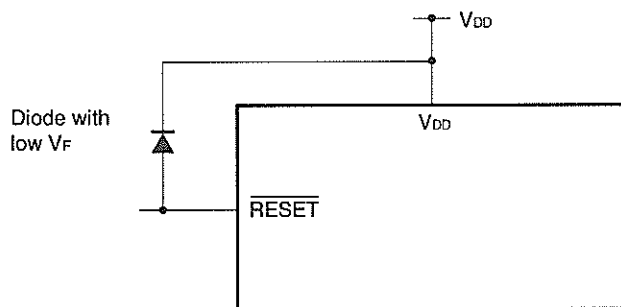
The $\overline{\text{RESET}}$ pin has the test mode selecting function for testing the internal operation of the μPD17P104 (IC test), besides the functions shown in Section 1.1.

Applying a voltage exceeding V_{DD} to the $\overline{\text{RESET}}$ pin causes the μPD17P104 to enter the test mode. When noise exceeding V_{DD} comes in during normal operation, the device is switched to the test mode.

For example, if the wiring from the $\overline{\text{RESET}}$ pin is too long, noise may be induced on the wiring, causing this mode switching.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- Connect a diode with low V_F between the pin and V_{DD}.
- Connect a capacitor between the pin and V_{DD}.



2. DIFFERENCES BETWEEN THE μPD17P104, μPD17104, AND μPD17104L

The μPD17P104 is a one-time PROM version of the μPD17104, in which the internal masked ROM is replaced with a one-time PROM.

Table 2-1 lists the differences between the μPD17P104, μPD17104, and μPD17104L.

The μPD17P104 has the same CPU functions and internal peripheral hardwares as those of μPD17104 and μPD17104L except for its program memory, mask option, oscillation settling time, and supply voltage range.

Part of electrical characteristics is also different between these products. For details of the electrical characteristics, refer to the data sheet of each product.

Table 2-1 Differences between the μPD17P104, μPD17104, and μPD17104L

Item	μPD17P104	μPD17104	μPD17104L
ROM	One-time PROM 512 × 16 bits (0000H - 01FFH)	Masked ROM	
Internal pull-up resistors of P0B ₀ to P0B ₂ pins	Not provided	Mask option	
Internal pull-up resistors of the RESET pin			
V _{PP} and operation mode selection pins	Provided	Not provided	
Oscillation settling time	16/f _x	8/f _x	
Supply voltage	V _{DD} = 2.7 to 6.0 V (at f _x = 500 kHz to 2 MHz) V _{DD} = 4.5 to 6.0 V (at f _x = 500 kHz to 8 MHz)	V _{DD} = 1.8 to 3.6 V (at f _x = 500 kHz to 2 MHz)	
Quality grade	Standard	• Standard (μPD17104)	• Standard (μPD17104L)
Electrical characteristics	Partially differs between these products. Refer to the data sheet of each product for details.		

Caution Although a PROM product is highly compatible with a masked ROM product in respect of functions, they differ in internal ROM circuits and part of electrical characteristics. Before changing the PROM product to the masked ROM product in an application system, evaluate the system carefully using the masked ROM product.

3. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P104's internal program memory consists of a 512 × 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in Table 3-1. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Table 3-1 Pins Used When Writing to Program Memory or Verifying Its Contents

Pin	Function
V _{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.
V _{DD}	Power supply pin. +6 V is applied to this pin when writing to program memory or verifying its contents.
RESET	System reset input pin. Apply the specific signal to this pin to initialize the conditions of the microcontroller before switching to the program memory write/verify mode.
CLK	Input pin for address update clocks used when writing to program memory or verifying its contents. Input of four pulses to this pin updates the address of the program memory.
MD ₀ - MD ₃	Input pins that select an operation mode when writing to program memory or verifying its contents
D ₀ - D ₇	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

★

★

3.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, RESET = 0 V), the μPD17P104 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD₀ through MD₃ pins as follows. Connect each pin not listed in Table 3-1 to ground through a pull-down resistor.

Table 3-2 Specification of Operating Modes

Operating mode specification						Operating mode
V _{PP}	V _{DD}	MD ₀	MD ₁	MD ₂	MD ₃	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

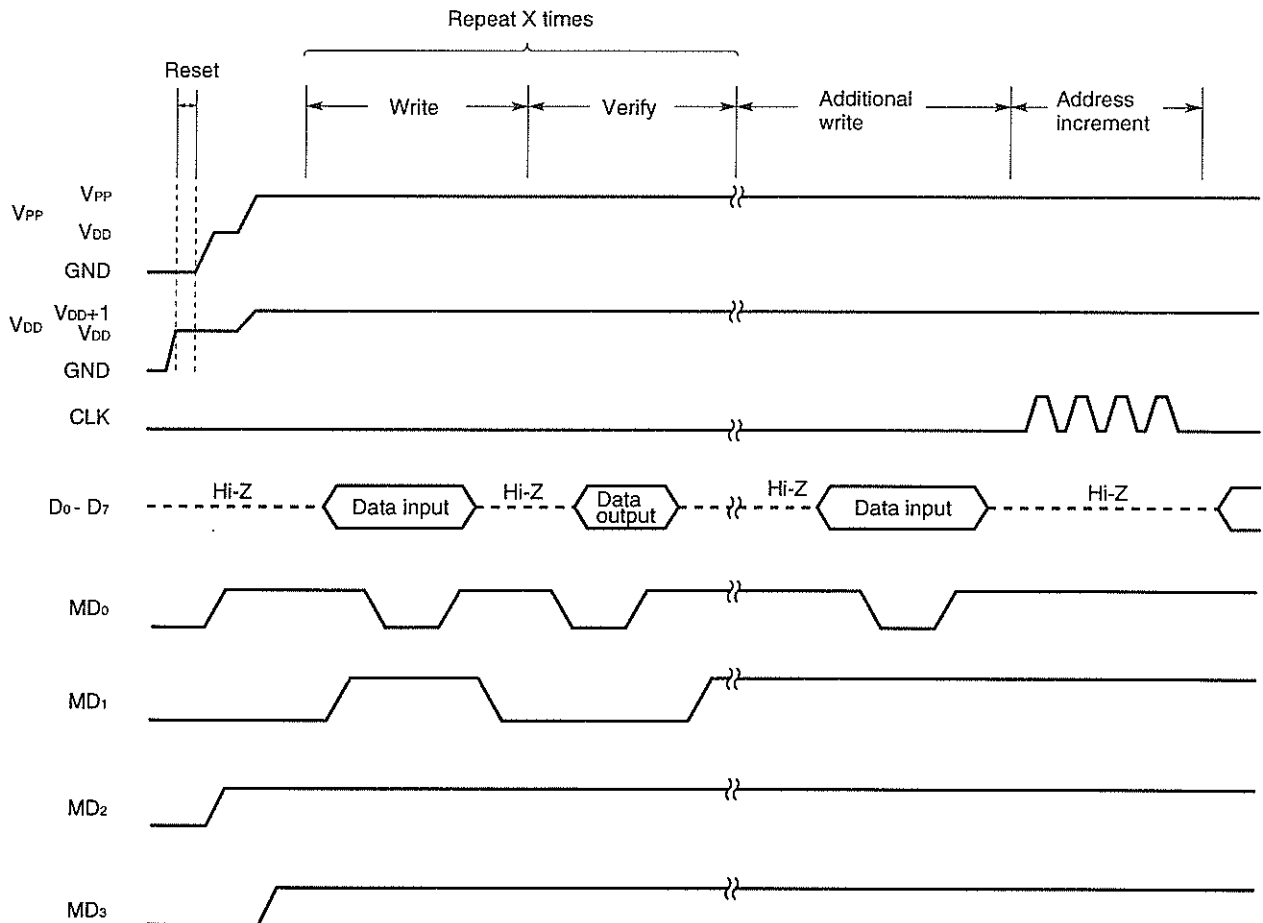
x: Don't care. L (low) or H (high)

3.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

- (1) Pull down the levels of all unused pins to GND by means of resistors. Bring the CLK pin to low level.
- (2) Apply 5 V to the V_{DD} pin and bring the V_{PP} pin to low level.
- (3) Wait 10 μs. Then apply 5 V to the V_{PP} pin.
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
- (6) Select program inhibit mode.
- (7) Write data in 1-ms write mode.
- (8) Select program inhibit mode.
- (9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
- (10) Perform additional write for X (number of repetitions of steps (7) to (9)) × 1 ms.
- (11) Select program inhibit mode.
- (12) Increment the program memory address by one on reception of four pulses on the CLK pin.
- (13) Repeat steps (7) to (12) until the last address is reached.
- (14) Select program memory address clear mode.
- (15) Apply 5 V to the V_{DD} and V_{PP} pins.
- (16) Turn power off.

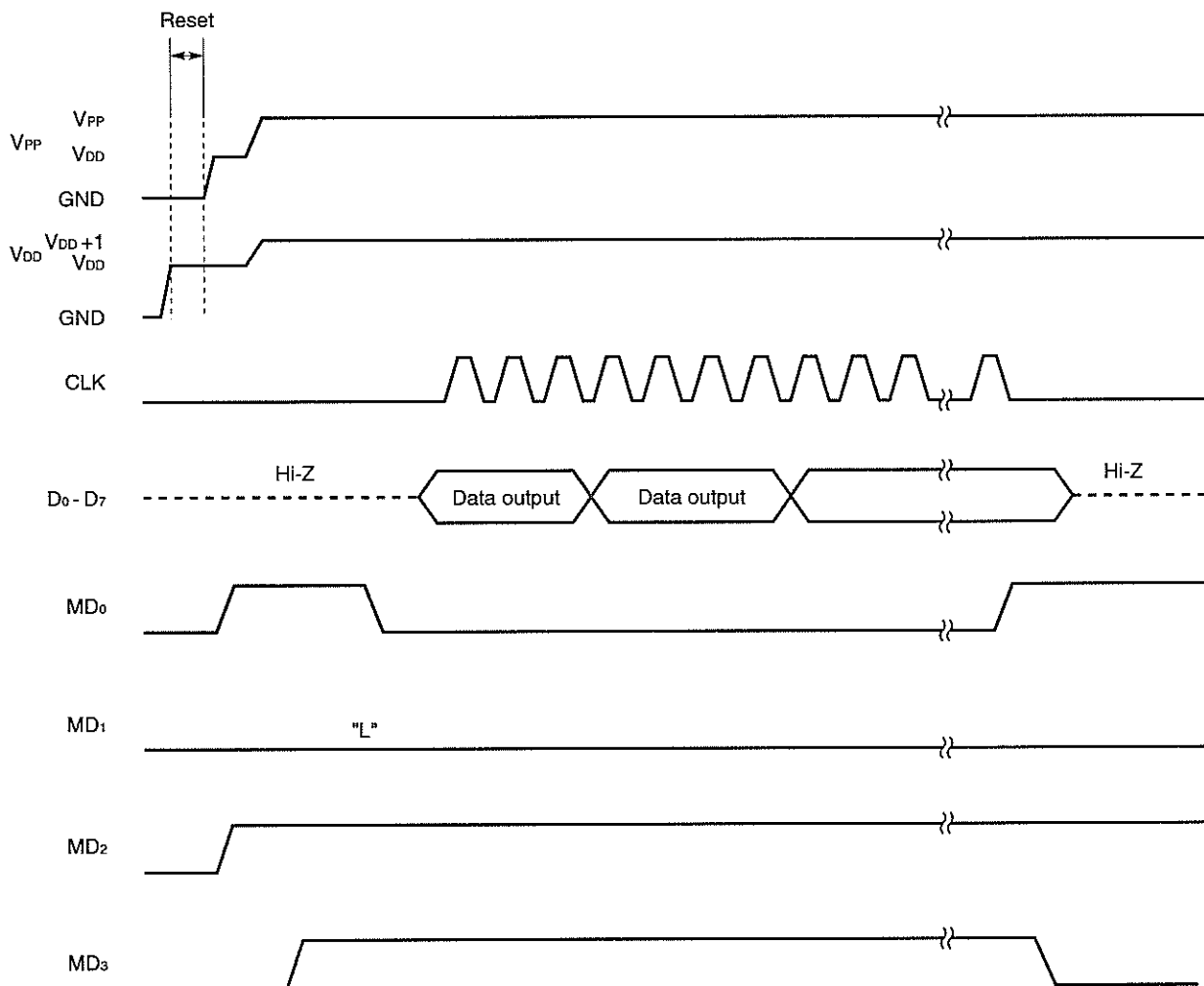
A timing chart for program memory writing steps (2) to (12) is shown below.



3.3 READING PROGRAM MEMORY

- (1) Pull down the levels of all unused pins to GND by means of resistors. Bring the CLK pin to low level.
- (2) Apply 5 V to the V_{DD} pin and bring the V_{PP} pin to low level.
- (3) Wait 10 μs. Then apply 5 V to the V_{PP} pin.
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
- (6) Select program inhibit mode.
- (7) Select verify mode. Data is output sequentially one address at a time for every four input clock pulses on the CLK pin.
- (8) Select program inhibit mode.
- (9) Select program memory address clear mode.
- (10) Apply 5 V to the V_{DD} and V_{PP} pins.
- (11) Turn power off.

A timing chart for program memory reading steps (2) to (9) is shown below.



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V _{DD}			-0.3 to +7.0	V
PROM supply voltage	V _{PP}			-0.3 to +13.5	V
Input voltage	V _I	P0A, P0C, P0D, $\overline{\text{RESET}}$		-0.3 to V _{DD} + 0.3	V
		P0B		-0.3 to +11	V
Output voltage	V _O	P0A, P0C, P0D		-0.3 to V _{DD} + 0.3	V
		P0B		-0.3 to +11	V
High-level output current	I _{OH}	Each of P0A, P0C, and P0D		-5	mA
		Total of all output pins		-15	mA
Low-level output current	I _{OL}	Each of P0A, P0B, P0C, and P0D		30	mA
		Total of all output pins		100	mA
Operating ambient temperature	T _A			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C
Allowable dissipation	P _d	T _A = 85 °C	22-pin plastic shrink DIP	400	mW
			24-pin plastic SOP	250	

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	f = 1 MHz			15	pF
I/O capacitance	C _{IO}	0 V for pins other than pins to be measured			15	pF

I/O: Input/output

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
High-level input voltage	V _{IH1}	P0A, P0C, P0D	0.7V _{DD}		V _{DD}	V	
	V _{IH2}	RESET	0.8V _{DD}		V _{DD}	V	
	V _{IH3}	P0B	0.8V _{DD}		9	V	
Low-level input voltage	V _{IL1}	P0A, P0C, P0D	0		0.3V _{DD}	V	
	V _{IL2}	RESET	0		0.2V _{DD}	V	
	V _{IL3}	P0B	0		0.2V _{DD}	V	
High-level output voltage	V _{OH}	P0A, P0C, P0D V _{DD} = 4.5 to 6.0 V, I _{OH} = -2 mA	V _{DD} - 2.0			V	
		P0A, P0C, P0D, I _{OH} = -200 μA	V _{DD} - 1.0			V	
Low-level output voltage	V _{OL}	P0A, P0B, P0C, P0D V _{DD} = 4.5 to 6.0 V, I _{OL} = 15 mA			2.0	V	
		P0A, P0B, P0C, P0D, I _{OL} = 600 μA			0.5	V	
High-level input leakage current	I _{LIH1}	P0A, P0C, P0D, V _{IN} = V _{DD}			5	μA	
	I _{LIH2}	P0B, V _{IN} = V _{DD}			5	μA	
	I _{LIH3}	P0B, V _{IN} = 9 V			10	μA	
Low-level input leakage current	I _{LIL1}	P0A, P0C, P0D, V _{IN} = 0 V			-5	μA	
	I _{LIL2}	P0B, V _{IN} = 0 V			-5	μA	
High-level output leakage current	I _{LOH1}	P0A, P0C, P0D, V _{OUT} = V _{DD}			5	μA	
	I _{LOH2}	P0B, V _{OUT} = V _{DD}			5	μA	
	I _{LOH3}	P0B, V _{OUT} = 9 V			10	μA	
Low-level output leakage current	I _{LOL}	P0A, P0B, P0C, P0D, V _{OUT} = 0 V			-5	μA	
Power supply current	I _{DD1}	Operation mode	V _{DD} = 5 V ±10 %, f _x = 8.0 MHz		3.5	10.5	mA
			V _{DD} = 3 V ±10 %, f _x = 2.0 MHz		1.1	4.4	mA
	I _{DD2}	HALT mode	V _{DD} = 5 V ±10 %, f _x = 8.0 MHz		2.5	7.5	mA
			V _{DD} = 3 V ±10 %, f _x = 2.0 MHz		1.0	4.0	mA
	I _{DD3}	STOP mode	V _{DD} = 5 V ±10 %		10	50	μA
			V _{DD} = 3 V ±10 %		8	45	μA

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE ($T_A = -40$ to $+85$ °C)

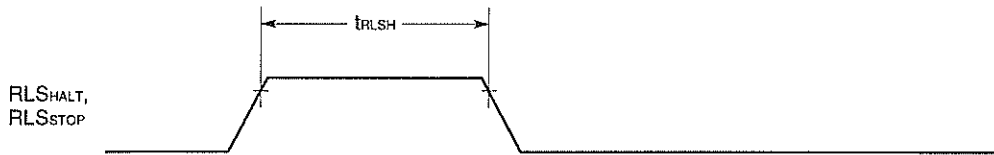
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data hold supply voltage	V_{DDDR}		2.0		6.0	V
Data hold supply current	I_{DDDR}	$V_{DDDR} = 2.0$ V		0.1	5.0	μA

AC CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 6.0 V)

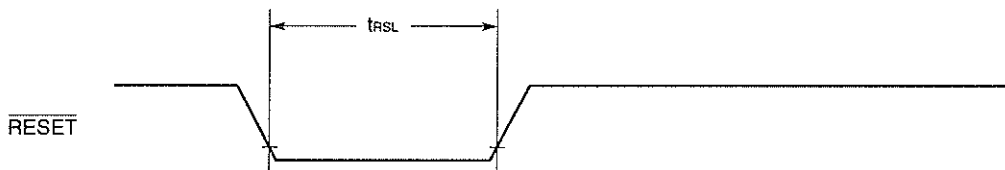
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU clock cycle time (instruction execution time)	t_{CY}	$V_{DD} = 4.5$ to 6.0 V	1.9		33	μs
			7.6		33	μs
RLSHALT, RLSSTOP high level width	t_{RLSH}		10			μs
RESET low level width	t_{RSL}		10			μs

Remark $t_{CY} = 16/f_x$ (f_x : frequency of system clock oscillator)

RLSHALT and RLSSTOP input timing



RESET input timing



SYSTEM CLOCK OSCILLATOR CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 6.0 V)

Resonator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator	Oscillation frequency	$V_{DD} = 2.7$ to 6.0 V	0.49		2.04	MHz
		$V_{DD} = 4.0$ to 6.0 V	0.49		5.00	MHz
		$V_{DD} = 4.5$ to 6.0 V	0.49		8.16	MHz

DC PROGRAMMING CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.5\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage high	V_{IH1}	Except X_{IN}	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	X_{IN}	$V_{DD} - 0.5$		V_{DD}	V
Input voltage low	V_{IL1}	Except X_{IN}	0		$0.3V_{DD}$	V
	V_{IL2}	X_{IN}	0		0.4	V
Input leakage current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
Output voltage high	V_{OH}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
Output voltage low	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	$MD0 = V_{IL}$, $MD1 = V_{IH}$			30	mA

- Cautions**
- V_{PP} must be under +13.5 V including overshoot.
 - V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

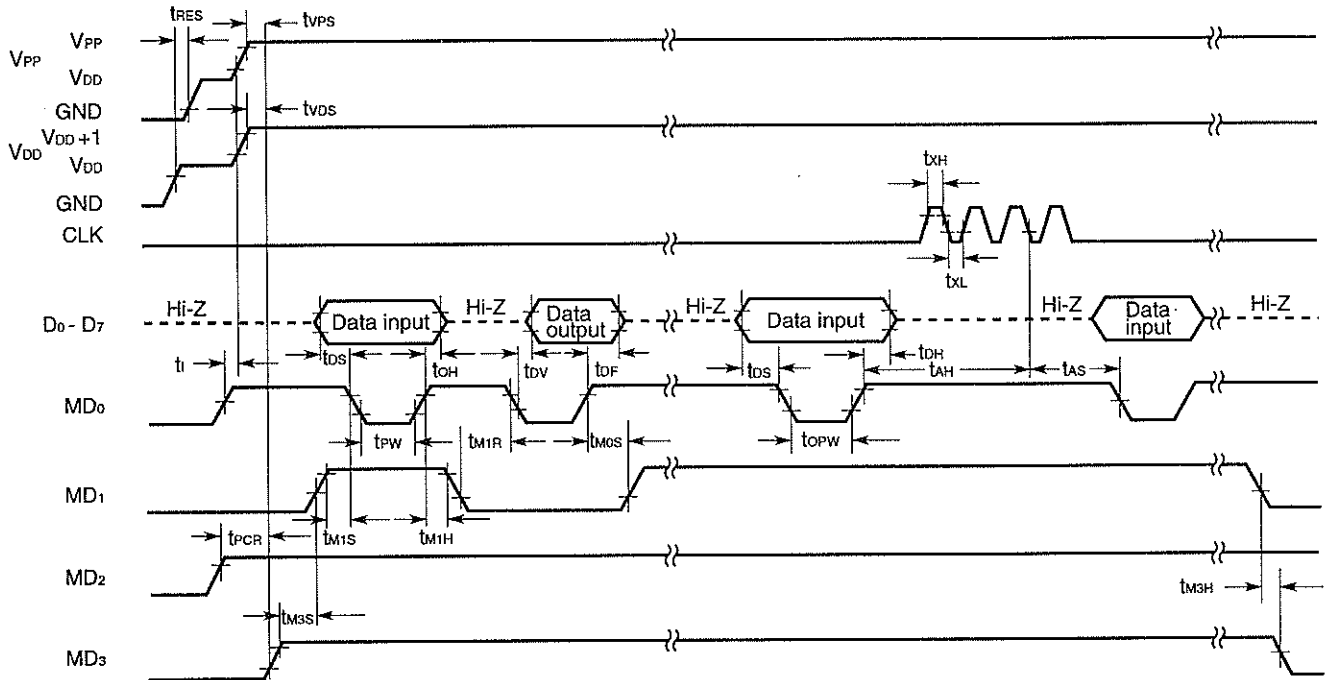
AC PROGRAMMING CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.5\text{ V}$)

Parameter	Symbol	Note 1	Conditions	Min.	Typ.	Max.	Unit
Address setup time ^{Note 2} to MD ₀ ↓	t _{AS}	t _{AS}		2			μs
MD ₁ setup time to MD ₀ ↓	t _{M1S}	t _{OES}		2			μs
Data setup time to MD ₀ ↓	t _{DS}	t _{DS}		2			μs
Address hold time ^{Note 2} to MD ₀ ↑	t _{AH}	t _{AH}		2			μs
Data hold time to MD ₀ ↑	t _{DH}	t _{DH}		2			μs
Delay from MD ₀ ↑ to data output float	t _{DF}	t _{DF}		0		130	ns
V _{PP} setup time to MD ₃ ↑	t _{VPS}	t _{VPS}		2			μs
V _{DD} setup time to MD ₃ ↑	t _{VDS}	t _{VCS}		2			μs
Initial program pulse width	t _{PW}	t _{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t _{OPW}	t _{OPW}		0.95		21.0	ms
MD ₀ setup time to MD ₁ ↑	t _{M0S}	t _{CES}		2			μs
Delay from MD ₀ ↓ to data output	t _{DV}	t _{DV}	MD ₀ = MD ₁ = V _{IL}			1	μs
MD ₁ hold time to MD ₀ ↑	t _{M1H}	t _{OEH}	t _{M1H} + t _{M1R} ≥ 50 μs	2			μs
MD ₁ recovery time to MD ₀ ↓	t _{M1R}	t _{OR}		2			μs
Program counter reset time	t _{PCR}	–		10			μs
CLK input high, low level range	t _{XH} , t _{XL}	–		0.063			μs
CLK input frequency	f _X	–				8	MHz
Initial mode set time	t _i	–		2			μs
MD ₃ setup time to MD ₁ ↑	t _{M3S}	–		2			μs
MD ₃ hold time to MD ₁ ↓	t _{M3H}	–		2			μs
MD ₃ setup time to MD ₀ ↓	t _{M3SR}	–	Read program memory	2			μs
Delay from address ^{Note 2} to data output	t _{DAD}	t _{ACC}	Read program memory			2	μs
Hold time from address ^{Note 2} to data output	t _{HAD}	t _{OH}	Read program memory	0		130	ns
MD ₃ hold time to MD ₀ ↑	t _{M3HR}	–	Read program memory	2			μs
Delay from MD ₃ ↓ to data output float	t _{DFR}	–	Read program memory			2	μs
Reset setup time	t _{RES}			10			μs

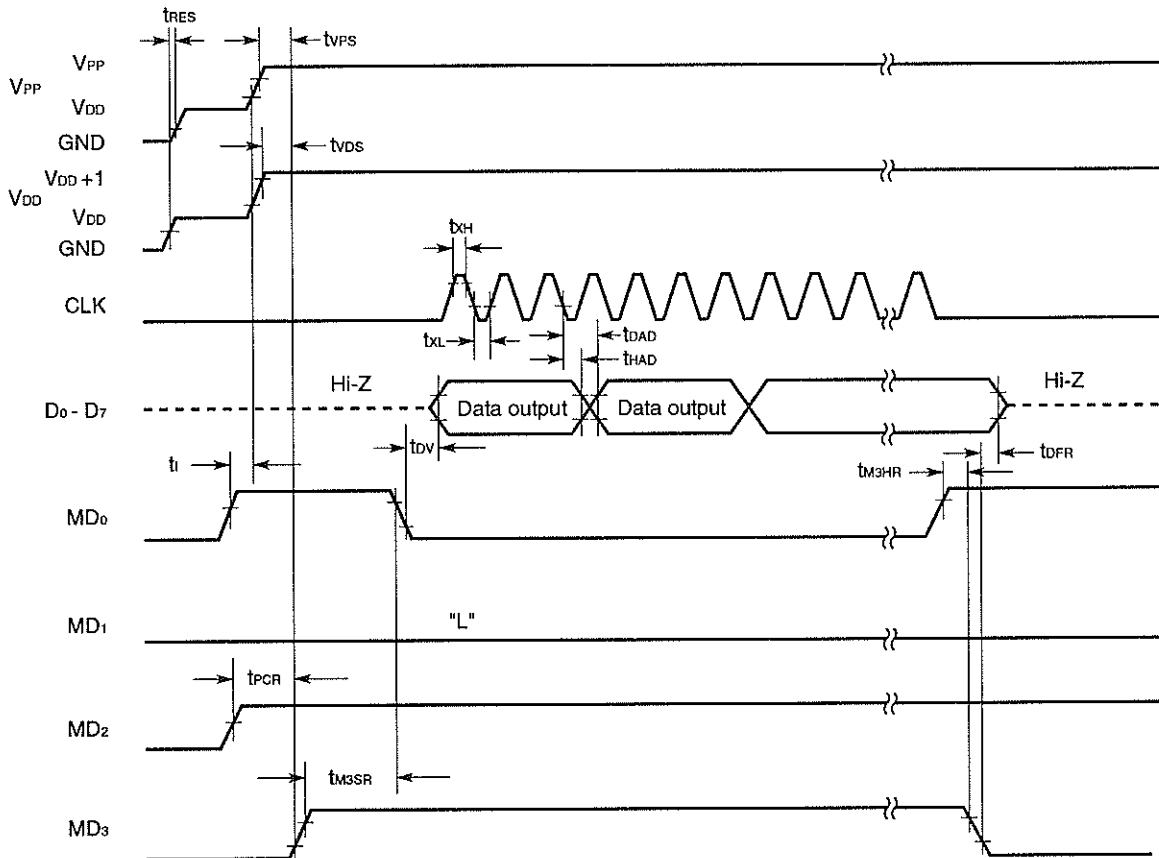
Notes 1. Symbols used for μ PD27C256A (The μ PD27C256A is used for maintenance.)

2. The internal address is incremented by one at the falling edge of the third clock (CLK) input.

Write program memory timing

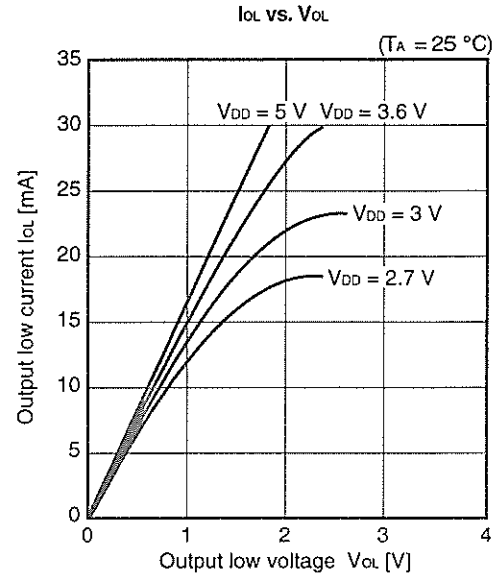
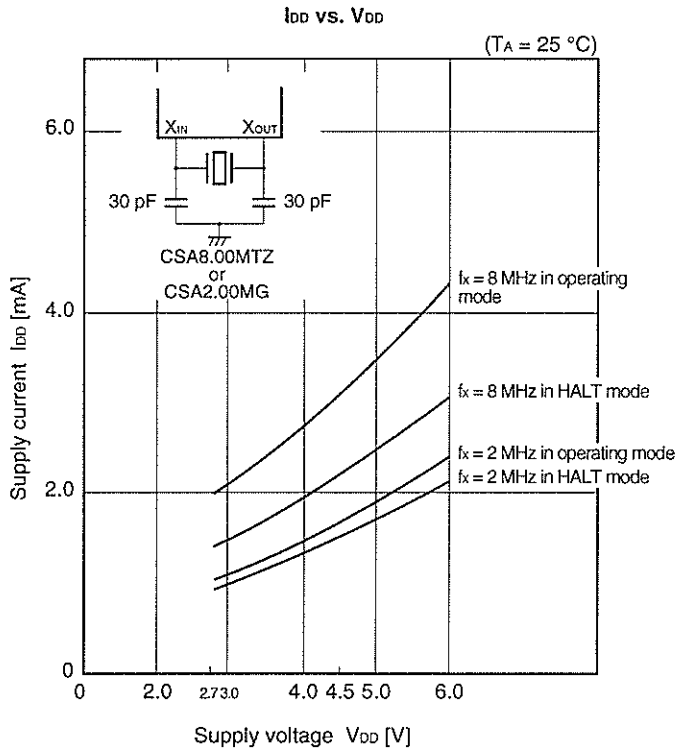


Read program memory timing

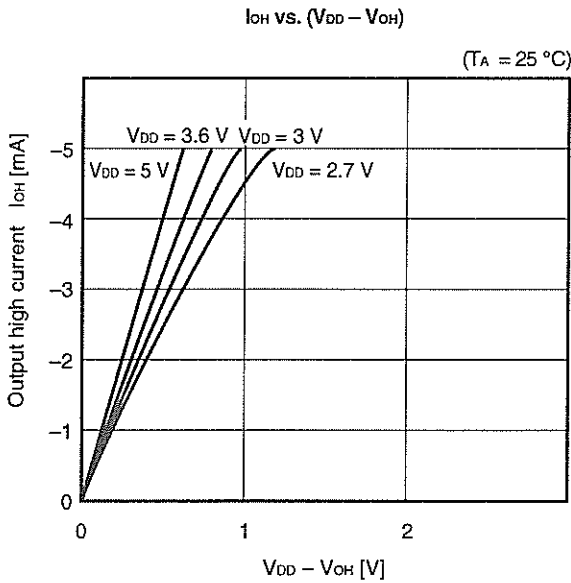


5. CHARACTERISTIC CURVES (FOR REFERENCE)

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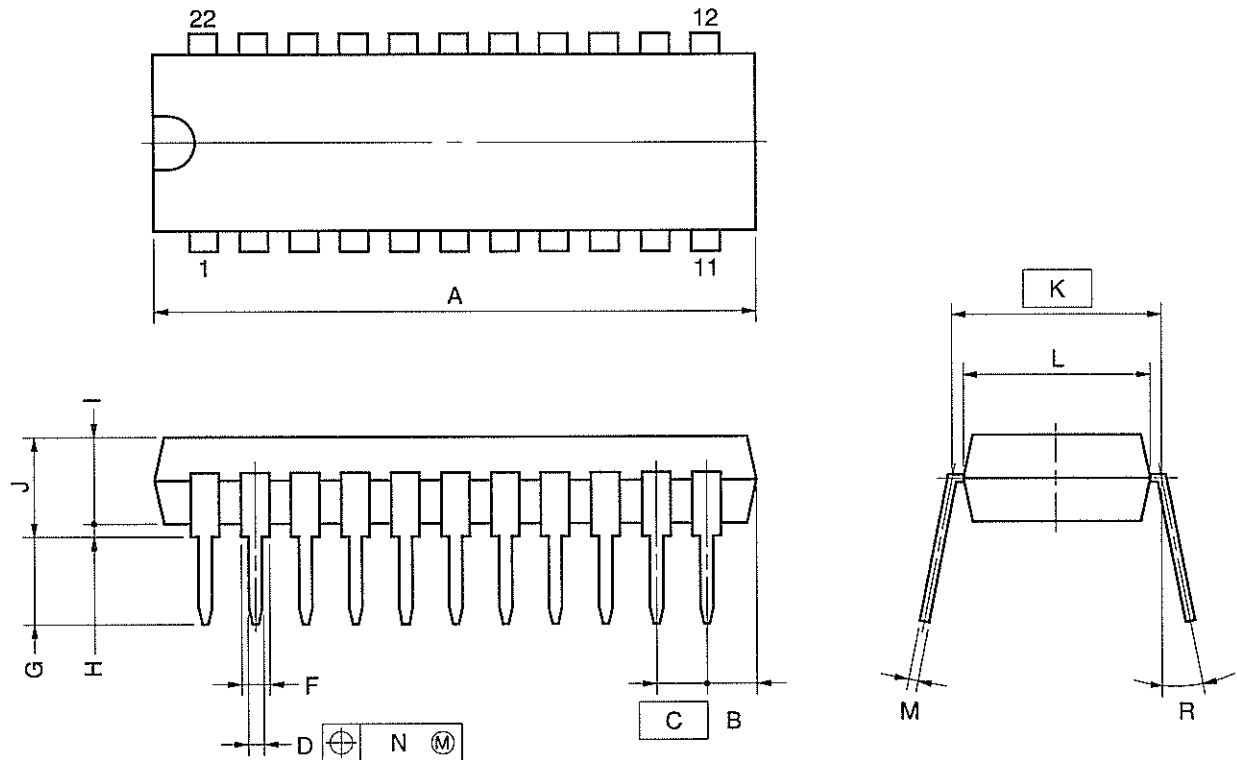
Caution The absolute maximum rating of the current is 30 mA per pin.



Caution The absolute maximum rating of the current is -5 mA per pin.

6. PACKAGE DRAWINGS

22 PIN PLASTIC SHRINK DIP (300 mil)



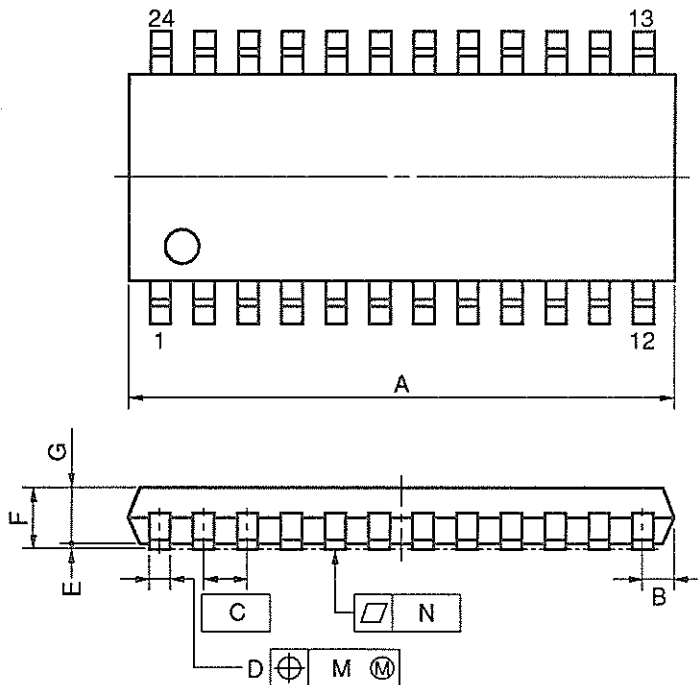
NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

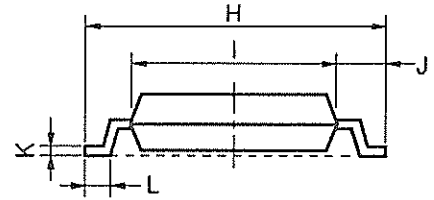
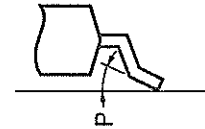
ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

S22C-70-300B-1

24 PIN PLASTIC SOP (300 mil)



detail of lead end



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}
L	0.6±0.2	0.024 ^{+0.008} _{-0.009}
M	0.12	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

P24GM-50-300B-4

7. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD17P104.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

★ **Table 7-1 Soldering Conditions for Surface-Mount Devices**

μPD17P104GS: 24-pin plastic SOP (300 mil)

Soldering process	Soldering conditions
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)

★ **Table 7-2 Soldering Conditions for Through Hole Mount Devices**

μPD17P104CS: 22-pin plastic shrink DIP (300 mil)

Soldering process	Soldering conditions
Wave soldering (only for terminals)	Solder temperature: 260 °C or less Flow time: 10 seconds or less
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each terminal)

Caution In wave soldering, apply solder only to the terminals. Care must be taken that jet solder does not come in contact with the main body of the package.

APPENDIX A TINY MICROCONTROLLER FAMILY

Item	Product name					
	μPD17103	μPD17103L	μPD17P103	μPD17104	μPD17104L	μPD17P104
ROM capacity	Masked ROM		One-time PROM	Masked ROM		One-time PROM
	1K byte (512 × 16 bits)					
RAM capacity	16 × 4 bits					
Number of input/output port pins ^{Note}	11 (3)			16 (4)		
System clock	Ceramic oscillation					
Instruction execution time	2 μs (at f _x = 8 MHz)	8 μs (at f _x = 2 MHz)	2 μs (at f _x = 8 MHz)		8 μs (at f _x = 2 MHz)	2 μs (at f _x = 8 MHz)
Standby function	HALT, STOP					
Supply voltage	<ul style="list-style-type: none"> • 2.7 to 6.0 V (at f_x = 500 kHz to 2 MHz) • 4.5 to 6.0 V (at f_x = 500 kHz to 8 MHz) 	<ul style="list-style-type: none"> • 1.8 to 3.6 V (at f_x = 500 kHz to 2 MHz) 	<ul style="list-style-type: none"> • 2.7 to 6.0 V (at f_x = 500 kHz to 2 MHz) • 4.5 to 6.0 V (at f_x = 500 kHz to 8 MHz) 		<ul style="list-style-type: none"> • 1.8 to 3.6 V (at f_x = 500 kHz to 2 MHz) 	<ul style="list-style-type: none"> • 2.7 to 6.0 V (at f_x = 500 kHz to 2 MHz) • 4.5 to 6.0 V (at f_x = 500 kHz to 8 MHz)
Package	• 16-pin DIP • 16-pin SOP		• 22-pin shrink DIP		• 24-pin SOP	
One-time PROM	μPD17P103		–	μPD17P104		–

★

Item	Product name					
	μPD17107	μPD17107L	μPD17P107	μPD17108	μPD17108L	μPD17P108
ROM capacity	Masked ROM		One-time PROM	Masked ROM		One-time PROM
	1K byte (512 × 16 bits)					
RAM capacity	16 × 4 bits					
Number of input/output port pins ^{Note}	11 (3)			16 (4)		
System clock	RC oscillation					
Instruction execution time	8 μs (at f _{cc} = 1 MHz)	40 μs (at f _{cc} = 200 kHz)	8 μs (at f _{cc} = 1 MHz)		40 μs (at f _{cc} = 200 kHz)	8 μs (at f _{cc} = 1 MHz)
Standby function	HALT, STOP					
Supply voltage	<ul style="list-style-type: none"> • 2.5 to 6.0 V (at f_{cc} = 50 kHz to 250 kHz) • 4.5 to 6.0 V (at f_{cc} = 50 kHz to 1 MHz) 	<ul style="list-style-type: none"> • 1.5 to 3.6 V (at f_{cc} = 50 kHz to 250 kHz) 	<ul style="list-style-type: none"> • 2.5 to 6.0 V (at f_{cc} = 50 kHz to 250 kHz) • 4.5 to 6.0 V (at f_{cc} = 50 kHz to 1 MHz) 		<ul style="list-style-type: none"> • 1.5 to 3.6 V (at f_{cc} = 50 kHz to 250 kHz) 	<ul style="list-style-type: none"> • 2.5 to 6.0 V (at f_{cc} = 50 kHz to 250 kHz) • 4.5 to 6.0 V (at f_{cc} = 50 kHz to 1 MHz)
Package	• 16-pin DIP • 16-pin SOP		• 22-pin shrink DIP		• 24-pin SOP	
One-time PROM	μPD17P107		–	μPD17P108		–

Note A number enclosed in parentheses indicates the number of the N-ch open-drain outputs. N-ch open-drain outputs can be connected to internal pull-up resistors by specifying the mask option.

Remark The μPD17P104 can be used to evaluate programs for the μPD17104L. Note, however, that the allowable supply voltages for the μPD17P104 and μPD17104L do not fall in the same range.

APPENDIX B DEVELOPMENT TOOLS

The following support tools are available for developing programs for the μPD17P104.

Hardware

Name	Description
In-circuit emulator [IE-17K IE-17K-ET ^{Note 1} EMU-17K ^{Note 2}]	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators applicable to the 17K series. The IE-17K and IE-17K-ET are connected to the PC-9800 series (host machine) or IBM PC/AT™ through the RS-232-C interface. The EMU-17K is inserted into the extension slot of the PC-9800 series (host machine). Use the system evaluation board (SE board) corresponding to each product together with one of these in-circuit emulators. <i>SIMPLEHOST</i> ®, a man machine interface, implements an advanced debug environment. The EMU-17K also enables user to check the contents of the data memory in real time.
SE board (SE-17104L)	The SE-17104L is an SE board for the μPD17104, μPD17104L, or μPD17P104. It is used solely for evaluating the system. It is also used for debugging in combination with the in-circuit emulator.
Emulation probe (EP-17104CS)	The EP-17104CS is an emulation probe for the μPD17104, μPD17104L, μPD17P104, μPD17108, μPD17108L, or μPD17P108.
PROM programmer [AF-9703 ^{Note 3} AF-9704 ^{Note 3} AF-9705 ^{Note 3} AF-9706 ^{Note 3}]	The AF-9703, AF-9704, AF-9705, and AF-9706 are PROM programmers for the μPD17P104. Use one of these PROM programmers with the program adapter, AF-9799, to write a program into the μPD17P104.
Program adapter (AF-9799 ^{Note 3})	The AF-9799 is a socket unit for the μPD17P103, μPD17P104, μPD17P107 or μPD17P108. It is used with the AF-9703, AF-9704, AF-9705, or AF-9706.

Notes 1. Low-end model, operating on an external power supply

2. The EMU-17K is a product of IC Co., Ltd. Contact IC Co., Ltd. (Tokyo, 03-3447-3793) for details.

3. The AF-9703, AF-9704, AF-9705, AF-9706, and AF-9799 are products of Ando Electric Co., Ltd. Contact Ando Electric Co., Ltd. (Tokyo, 03-3733-1151) for details.

Software

Name	Description	Host machine	OS		Distribution media	Part number
17K series assembler (AS17K)	AS17K is an assembler applicable to the 17K series. In developing μPD17P104 programs, AS17K is used in combination with a device file (AS17103).	PC-9800 series	MS-DOS™		5.25-inch, 2HD	μS5A10AS17K
					3.5-inch, 2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5.25-inch, 2HC	μS7B10AS17K
					3.5-inch, 2HC	μS7B13AS17K
Device file (AS17103)	AS17103 is a device file for the μPD17104 and μPD17P104. It is used together with the assembler (AS17K), which is applicable to the 17K series.	PC-9800 series	MS-DOS		5.25-inch, 2HD	μS5A10AS17103 Note
					3.5-inch, 2HD	μS5A13AS17103 Note
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10AS17103 Note
					3.5-inch, 2HC	μS7B13AS17103 Note
Support software (SIMPLEHOST)	SIMPLEHOST, running under Windows™, provides man-machine-interface in developing programs by using a personal computer and in-circuit emulator.	PC-9800 series	MS-DOS	Windows	5.25-inch, 2HD	μS5A10IE17K
					3.5-inch, 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10IE17K
					3.5-inch, 2HC	μS7B13IE17K

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Note The μSxxxxAS17103 contains a device file for the μPD17103, μPD17104, μPD17107, μPD17108, μPD17103L, μPD17104L, μPD17107L, or μPD17108L.

Remark The following table lists the versions of the operating systems described in the above table.

★

OS	Versions
MS-DOS	Ver. 3.30 to Ver. 5.00A>Note
PC DOS	Ver. 3.1 to Ver. 5.0Note
Windows	Ver. 3.0 to Ver. 3.1

Note MS-DOS versions 5.00 and 5.00A and PC DOS Ver. 5.0 are provided with a task swap function. This function, however, cannot be used in these software packages.

[MEMO]

Cautions on CMOS Devices**① Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged. Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② CMOS-specific handling of unused input pins

Caution Hold CMOS devices at a fixed input level. Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor. If handling of unused pins is documented, follow the instructions in the document.

③ Statuses of all MOS devices at initialization

Caution The initial status of a MOS device is unpredictable when power is turned on. Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined. When you turn on a device having a reset function, be sure to reset the device first.

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MS-DOS and Windows are trademarks of Microsoft Corporation.
PC/AT and PC DOS are trademarks of IBM Corporation.

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NEC devices are classified into the following three quality grades:

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.