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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD17P001

4-BIT SINGLE-CHIP MICROCONTROLLER WITH ON-CHIP HARDWARE FOR DIGITAL TUNING SYSTEMS

The μPD17P001 is a one-time PROM version of the μPD17001 that has on-chip mask ROM.

The μPD17P001, which can be programmed only once, is suited for testing during development of μPD17001 systems and limited production runs.

The analog characteristics (PLL system) of the μPD17P001 may be different from those of the μPD17001. Therefore, for LPF (Low Pass Filter) time constants, etc., evaluate them with the actual device before you decide them.

Use this data sheet together with μPD17001 documents.

FEATURES

- Compatible with the μPD17001 (except analog characteristics)
- One-time PROM : 8 KB (3836 × 16 bits)
- Operating voltage : V_{DD} = 5 V ± 10 % (during PLL and CPU operation)

ORDERING INFORMATION

Part Number	Package
μPD17P001GH-2A5	48-pin plastic QFP (10 × 14mm, 0.8-mm pitch)

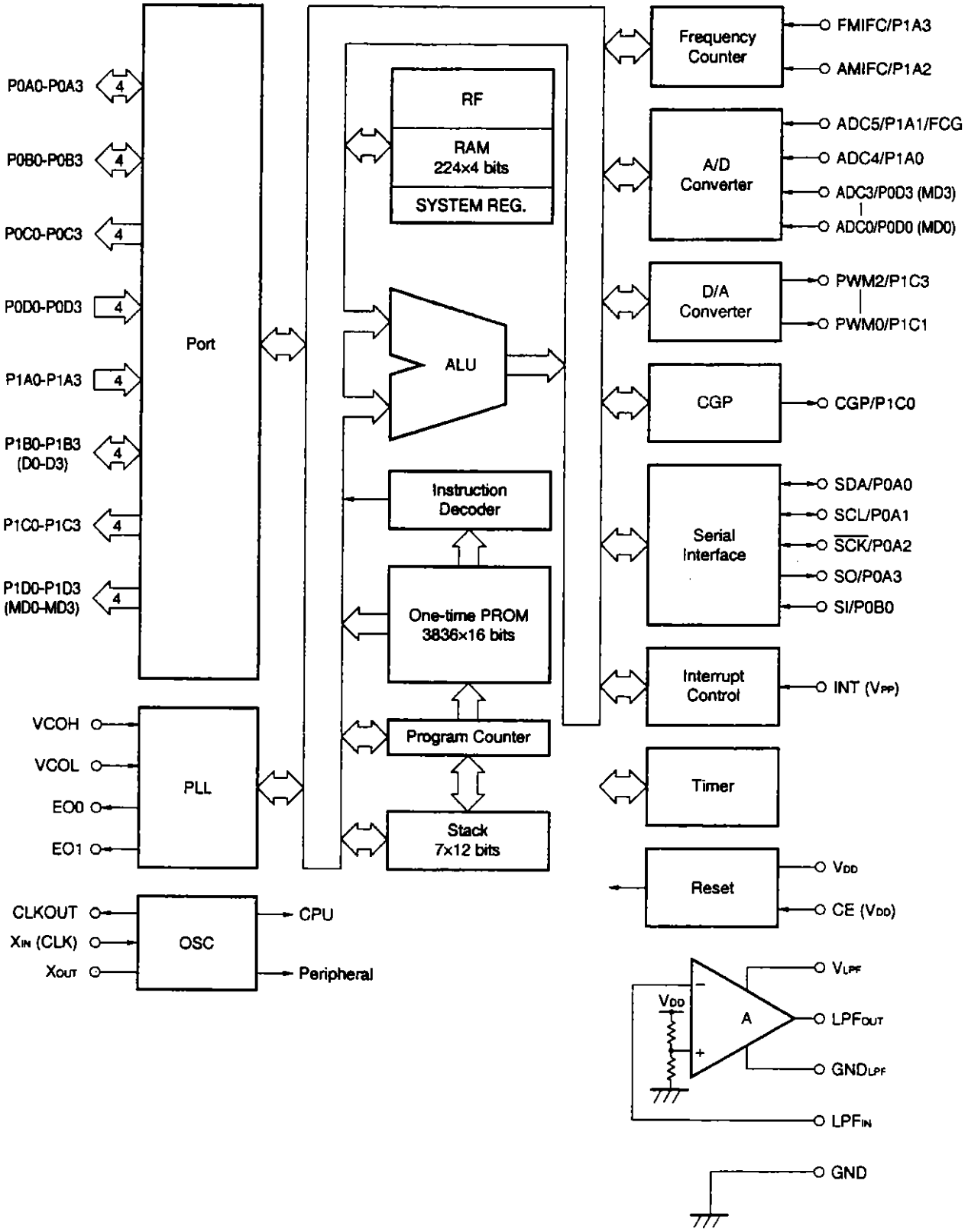
Document No. U11808EJ2V0DS00 (2nd edition)
Date Published January 1997 N
Printed in Japan

FUNCTIONAL OUTLINE

Item \ Part Number	μPD17001	μPD17P001
Program memory (ROM)	Mask ROM	One-time PROM
	• 3836 × 16 bits Table reference possible for all the on-chip ROM area	
General-purpose data memory (RAM)	• 224 × 4 bits Data buffer: 4 × 4 bits, eneral register: 16 × 4 bits	
Instruction execution time	• 4.44 μs (using 4.5-MHz crystal resonator)	
Stack levels	• 7 levels (stack manipulation possible)	
General ports	• I/O ports : 12 • Input ports : 8 • Output ports : 12	
Clock generator port (CGP)	• 1 port (P1C0/CGP pin) VDP (Variable Duty Pulse) and SG (Signal Generator) functions	
Serial interface	• 1 system (2 channels) 2-wire (serial I/O / I²C bus) : 1 channel 3-wire (serial I/O) : 1 channel	
D/A converter	• 8 bits × 3 channels (PWM output, output withstand voltage: 14 V max.)	
A/D converter	• 6 bits × 6 channels (successive approximation by software)	
Interrupt	• 4 channels (maskable interrupt) External : 1 channel (INT pin) Internal : 3 channels (timer, serial interface, frequency counter)	
Timer	• 2 channels Timer carry (1, 5, 100, 250 ms) Timer interrupt (0.11, 1, 5, 100 ms)	
Reset	• Power-on reset • Reset by CE pin (CE pin low level → high level) • Power failure detection function	

Item \ Part Number		μPD17001	μPD17P001
PLL frequency synthesizer	Frequency division method	• Direct division method (VCOL pin 30 MHz MAX.) • Pulse swallow system (VCOL pin 40 MHz MAX.) (VCOH pin 130 MHz MAX.)	
	Reference frequency	• Selected from 12 types by program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz	
	Charge pump	• 2 error-out outputs (pins EO0, EO1)	
	Phase comparator	• Unlock detection by program possible	
	LPF amplifier	• CMOS operational amplifier Output withstand voltage: 14 V MAX.	
Frequency counter		• Frequency measurement P1A3/FMIFC pin 5 to 15 MHz P1A2/AMIFC pin 0.1 to 1 MHz • External gate width measurement P1A1/ADC5/FCG pin	
Supply voltage		V_{DD} = 5 V ± 10 %	
Package		48-pin plastic QFP (10 × 14 mm), 0.8-mm pitch	

BLOCK DIAGRAM

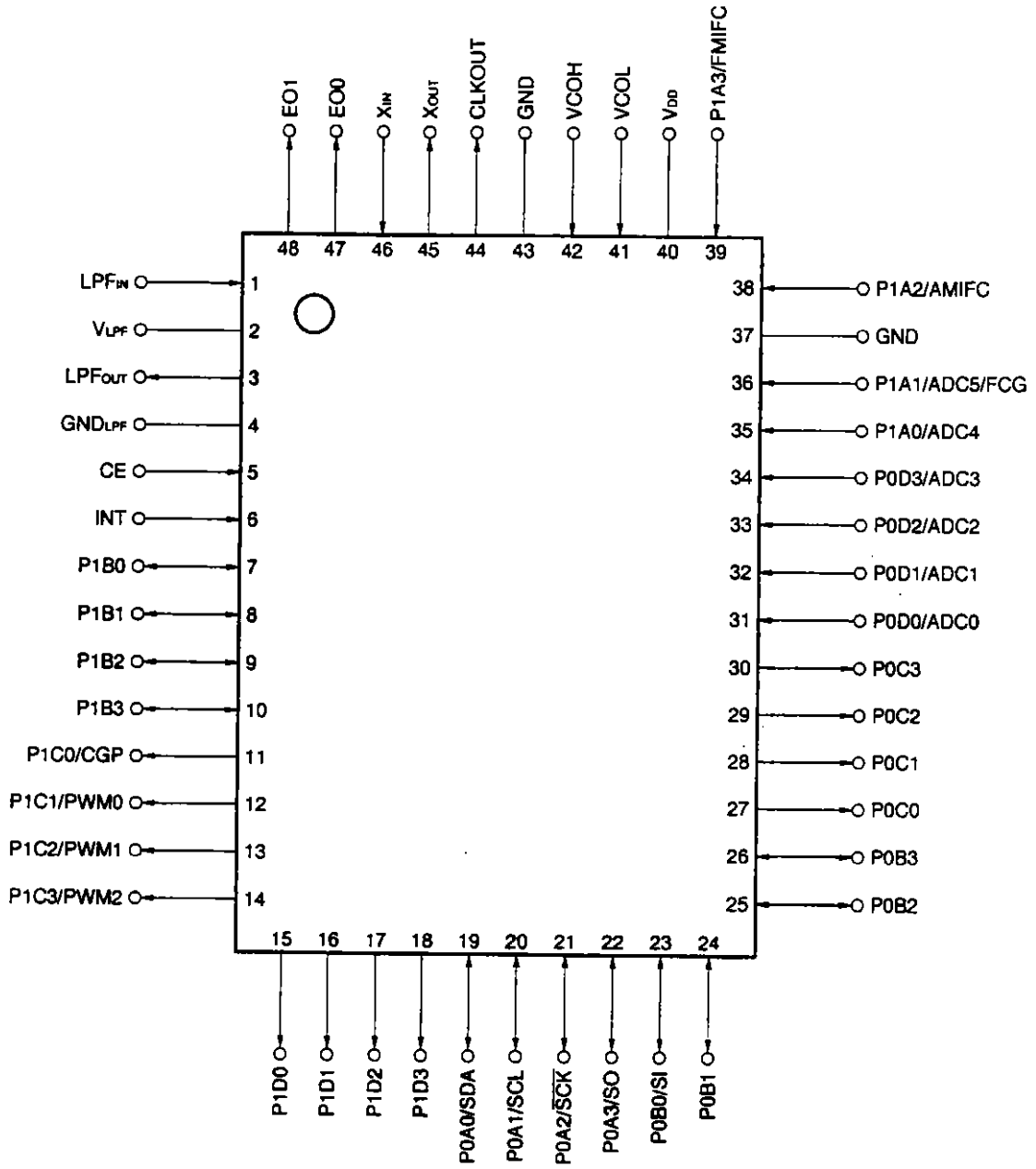


Remark The term in parenthesis indicates the one at the PROM programming mode.

PIN CONFIGURATION (Top View)

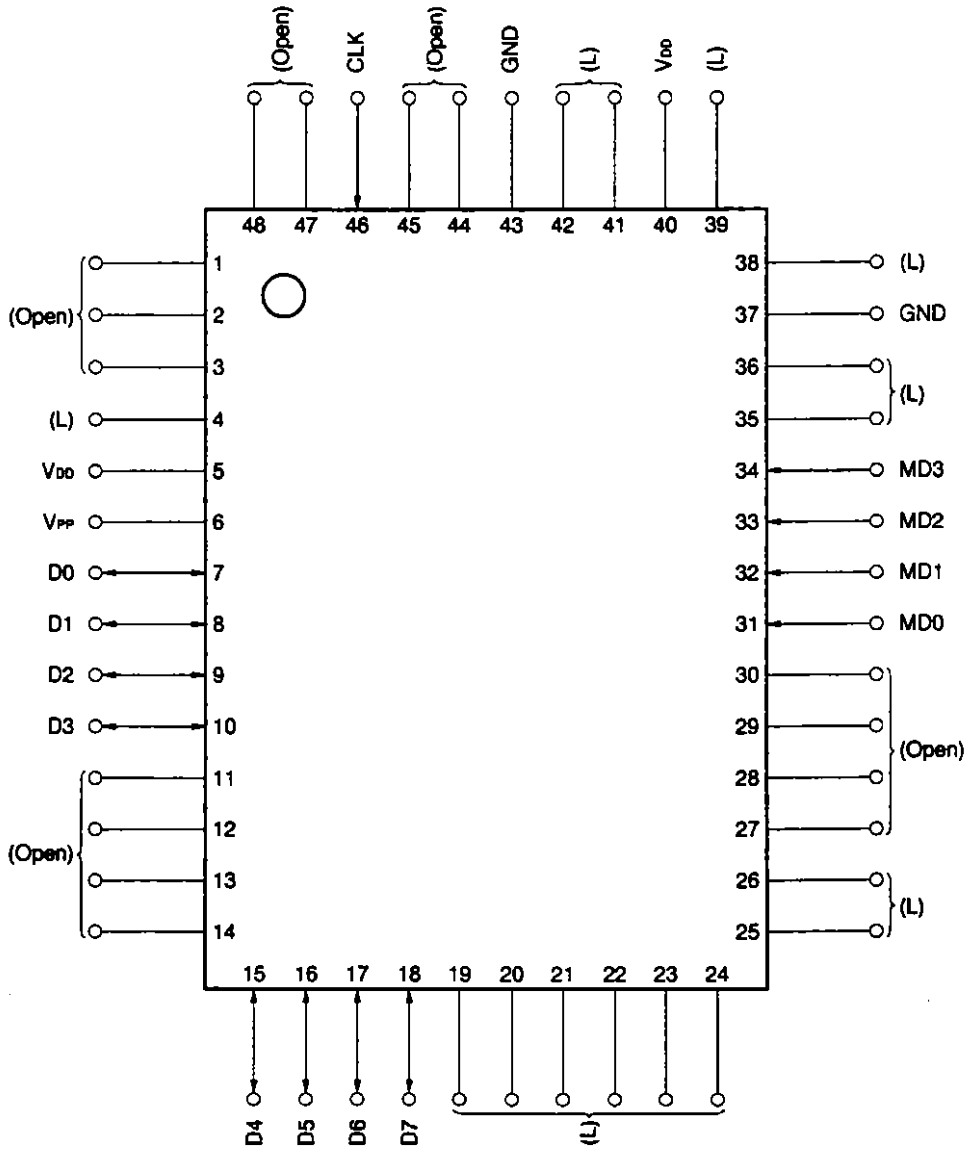
(1) Normal operation mode

- **μPD17P001GH-2A5**



(2) PROM programming mode

- μPD17P001GH-2A5



Caution **Contents in parentheses indicate how to handle unused pins in PROM programming mode.**
L: Connect to GND via a resistor (470 Ω) separately.
OPEN: Leave unconnected.

PIN IDENTIFICATIONS

ADC0-ADC5	: A/D converter input
AMIFC	: AM intermediate frequency counter input
CE	: Chip enable input
CGP	: Clock generator port
CLK	: Address update clock input
CLKOUT	: External microcontroller clock output
D0-D7	: Data input/output
EO0, EO1	: Error-out output
FCG	: External gate counter input
FMIFC	: FM intermediate frequency counter input
GND	: Ground
GND_{LPF}	: LPF amp ground
INT	: External interrupt input
LPF_{IN}	: LPF amp input
LPF_{OUT}	: LPF amp output
MD0-MD3	: Operating mode selection
P0A0-P0A3	: Port 0A
P0B0-P0B3	: Port 0B
P0C0-P0C3	: Port 0C
P0D0-P0D3	: Port 0D
P1A0-P1A3	: Port 1A
P1B0-P1B3	: Port 1B
P1C0-P1C3	: Port 1C
P1D0-P1D3	: Port 1D
PWM0-PWM2	: D/A converter output
$\overline{SCK}$	: Serial clock input/output
SCL	: Serial clock input/output
SDA	: Serial data input/output
SI	; Serial data input
SO	; Serial data output
VCOH	: Local oscillation high input
VCOL	: Local oscillation low input
V_{DD}	: Power supply
V_{LPF}	: LPF amp power supply
V_{PP}	: Program voltage application
X_{IN}, X_{OUT}	: Crystal resonator connection

CONTENTS

1. PIN FUNCTIONS

1.1 Normal Operation Mode

Pin No.	Symbol	Function			Output Format
1	LPF_{IN}	Low pass filer amp input			–
		After reset		When clock is stopped	
		Power-on reset	CE reset		
		Input with pull-up resistor	Input with pull-up resistor	Input with pull-up resistor	
2	V_{LPF}	Power supply of low pass filter amp			–
3	LPF_{OUT}	Output for low pass filter			N-ch open-drain 14 V withstand voltage
		After reset		When clock is stopped	
		Power-on reset	CE reset		
		Low-level output	Low-level output	Low-level output	
4	GND_{LPF}	Ground for low pass filter amp			–
5	CE	Input for device operation selection and CE reset • Device operation selection When CE is high, the PLL frequency synthesizer section can be operated. When CE is low, the PLL frequency synthesizer section is automatically disabled (operation disabled) with the device contents. • CE reset When CE changes from low to high, a reset is executed on the rise of the internal basic timer setting pulse. A reset timing delay function is also available. This function does not accept a low-level or high-level signal of less than 110 to 165 μs to prevent misoperation due to noise. The input signal level of this pin can be detected by the CE pin level judge register (address 07H) of the register file. At this time, the contents of the CE pin level judge register do not change with a low-level or high-level signal of less than 110 to 165 μs, either. This pin is Schmitt-triggered input with hysteresis characteristic. Ensure that no voltage higher than V_{DD} is applied upon powering-on. Application of a voltage higher than V_{DD} may cause misoperation.			–
6	INT	Vectored interrupt input for edge detection. Either rising or falling edge can be selected. This pin is Schmitt-triggered input with hysteresis characteristic. Ensure that no voltage higher than V_{DD} is applied to the INT pin upon powering-on. Application of a voltage higher than V_{DD} may cause misoperation.			–
7 I 10	P1B0 I P1B3	4-bit CMOS input/output port			CMOS push-pull
		After reset		When clock is stopped	
		Power-on reset	CE reset		
		Input	Input	Input	

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th><th>Output Format</th></tr>
<tr><td>11</td><td>P1C0/CGP</td><td>Output of port 1C, D/A converter and clock generator port</td><td>CMOS push-pull</td></tr>
<tr><td>12
|
14</td><td>P1C1/PWM0[Note]
|
P1C3/PWM2[Note]</td><td>• P1C0 to P1C3
• 4-bit output port
• PWM0 to PWM2
• Output of D/A converter with 8-bit resolution
• CGP
• Clock generator port output
<table><tr><th colspan="2">After reset</th><th>When clock is stopped</th></tr><tr><th>Power-on reset</th><th>CE reset</th><th></th></tr><tr><td>Undefined data is output
(P1C0 to P1C3)</td><td>Output
(P1C0 to P1C3)</td><td>Output
(P1C0 to P1C3)</td></tr></table></td><td>N-ch open-drain
14 V withstand
voltage</td></tr>
<tr><td>15
|
18</td><td>P1D0
|
P1D3</td><td>4-bit CMOS output port
<table><tr><th colspan="2">After reset</th><th>When clock is stopped</th></tr><tr><th>Power-on reset</th><th>CE reset</th><th></th></tr><tr><td>Undefined data is output</td><td>Output</td><td>Output</td></tr></table></td><td>CMOS push-pull</td></tr>
<tr><td>19
20</td><td>P0A0/SDA[Note]
P0A1/SCL[Note]</td><td rowspan="2">Input/output of port A, port B and serial interface
• P0A3 to P0A0
• 4-bit input/output port
• Input/output settable bit-wise
• P0B3 to P0B0
• 4-bit CMOS input/output port
• Input/output settable bit-wise
• SDA, SCL
• SDA: Serial data input/output
• SCL: Serial clock input/output
• $\overline{SCK}$, SO, SI
• $\overline{SCK}$: Serial clock input/output
• SO : Serial data output
• SI : Serial data input
(Pins SDA, SCL cannot be used with pins $\overline{SCK}$, SO and SI simultaneously.)
<table><tr><th colspan="2">After reset</th><th>When clock is stopped</th></tr><tr><th>Power-on reset</th><th>CE reset</th><th></th></tr><tr><td>Input
(P0A0-P0A3
P0B1-P0B3)</td><td>Input
(P0A0-P0A3
P0B1-P0B3)</td><td>Input
(P0A0-P0A3
P0B1-P0B3)</td></tr></table></td><td>N-ch open-drain
5 V withstand
voltage</td></tr>
<tr><td>21
22
23
24
|
26</td><td>P0A2/$\overline{SCK}$
P0A3/SO
P0B0/SI
P0B1
|
P0B3</td><td>CMOS push-pull</td></tr>
<tr><td>27
|
30</td><td>P0C0
|
P0C3</td><td>4-bit CMOS output port
<table><tr><th colspan="2">After reset</th><th>When clock is stopped</th></tr><tr><th>Power-on reset</th><th>CE reset</th><th></th></tr><tr><td>Undefined data is output</td><td>Output</td><td>Output</td></tr></table></td><td>CMOS push-pull</td></tr>
</table>

Note Pins P1C1/PWM0 to P1C3/PWM2, P0A0/SDA, P0A1/SCL are N-ch open-drain outputs, so they need external pull-up resistors.

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th><th>Output Format</th></tr>
<tr><td>31
|
34</td><td>P0D0/ADC0
|
P0D3/ADC3</td><td>Input to port 0D, port 1A and A/D converter, and input of external gate counter.
• P0D0 to P0D3, P1A0, P1A2
- 4-bit input port
- Pull-down resistor settable bit-wise
• ADC0 to ADC5
- Analog input to A/D converter with 6-bit resolution
• FCG
- External gate counter input</td><td>–</td></tr>
<tr><td>35
36</td><td>P1A0/ADC4[Note]
P1A1/ADC5/FCG[Note]</td><td>
<table>
<tr><th colspan="2">After reset</th><th rowspan="2">When clock is stopped</th></tr>
<tr><th>Power-on reset</th><th>CE reset</th></tr>
<tr><td>- P0D0-P0D3 with pull-down resistor input
- P1A0-P1A3 input</td><td>- P0D0-P0D3 with pull-down resistor input
- P1A0-P1A3 input</td><td>- P0D0-P0D3 with pull-down resistor input
- P1A0-P1A3 input</td></tr>
</table>
</td><td>N-ch open-drain 5 V withstand voltage</td></tr>
<tr><td>37, 43</td><td>GND</td><td>Ground</td><td>–</td></tr>
<tr><td>38
39</td><td>P1A2/AMIFC
P1A3/FMIFC</td><td>Input of port 1A and frequency counter
• P1A2, P1A3
- 4-bit input port
• AMIFC, FMIFC
- Input of FM, AM intermediate frequency counter
Measurable Frequencies
<table>
<tr><th>Input Pin</th><th>Input Frequency (MHz)</th><th>Input Amplitude (V_{P-P})</th></tr>
<tr><td>P1A3/FMIFC</td><td>5-15</td><td>0.3</td></tr>
<tr><td>P1A2/AMIFC</td><td>0.1-1</td><td>0.3</td></tr>
</table>
Since these pins are alternating-current amp inputs, use a capacitor to cut the DC component of input signals.
<table>
<tr><th colspan="2">After reset</th><th rowspan="2">When clock is stopped</th></tr>
<tr><th>Power-on reset</th><th>CE reset</th></tr>
<tr><td>Input
(P1A2, P1A3)</td><td>Input
(P1A2, P1A3)</td><td>Input
(P1A2, P1A3)</td></tr>
</table>
</td><td>–</td></tr>
<tr><td>40</td><td>V_{DD}</td><td>Power supply. Supply the same potential.
- When CPU and peripheral function are operating : 4.5 to 5.5 V
- When only CPU is operating : 3.9 to 5.5 V
- When clock is stopped : 2.9 to 5.5 V</td><td>–</td></tr>
</table>

Note Pins P1A0/ADC4, P1A1/ADC5/FCG are N-ch open-drain outputs, so they need external pull-up resistors.

Pin No.	Symbol	Function			Output Format
41 42	VCOL VCOH	PLL local oscillation (VCO) frequency is input. • VCOH • Active when VHF mode is selected by program. Otherwise, pull-down. • VCOL • Active when HF, MW mode is selected by program. Otherwise, pull-down. Since these pins are alternating-current amp inputs, use a capacitor to cut the DC component of input signals.			–
		After reset		When clock is stopped	
		Power-on reset	CE reset		
		Input with pull-down resistor	Input with pull-down resistor	Input with pull-down resistor	
44	CLKOUT	Clock output pin for external microcontroller. The same frequency as X_{OUT} is output.			CMOS push-pull
		After reset		When clock is stopped	
		Power-on reset	CE reset		
		Low-level output	Retains previous status.	Low-level output	
45 46	X_{OUT} X_{IN}	Crystal resonator connection pin 4.5 MHz crystal resonator is connected.			–
47 48	EO0 EO1	Outputs from the PLL frequency synthesizer charge pump. The results of phase comparison between the local oscillation divided frequency and the reference frequency are output.			CMOS 3-state
		After reset		When clock is stopped	
		Power-on reset	CE reset		
		High impedance output	High impedance output	High impedance output	

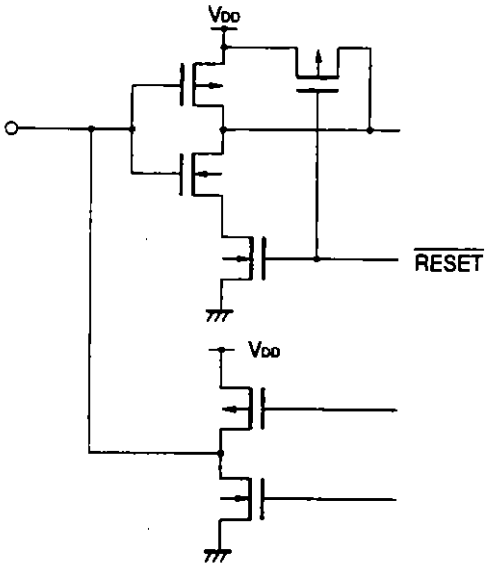
1.2 PROM Programming Mode

Pin No.	Symbol	Function	Output Format
5	V_{DD}	Positive power supply 6 V are applied for program memory writing, reading and verifying.	–
6	V_{PP}	Program voltage application pin for program memory writing, reading and verifying 12.5 V are applied.	–
7 | 10 15 | 18	D0 | D3 D4 | D7	8-bit data input/output for program memory writing, reading and verifying	CMOS push-pull
31 | 34	MD0 | MD3	Input to select operating mode for program memory writing, reading and verifying	–
37	GND	Ground	–
40	V_{DD}	Positive power supply 6 V are applied for program memory writing, reading and verifying.	–
43	GND	Ground	–
46	CLK	Address update clock input for program memory writing, reading and verifying	–

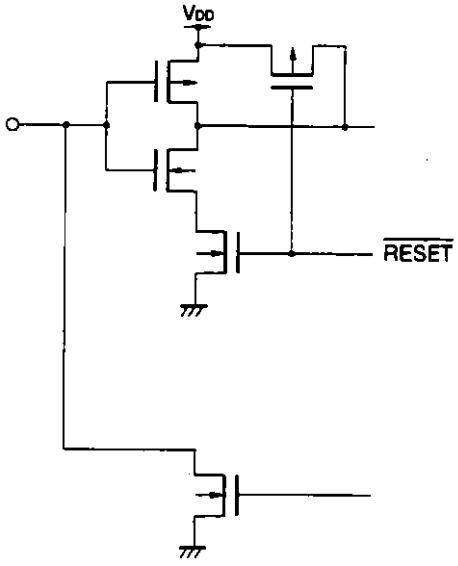
Remark The other pins are not used in the PROM programming mode. How to handle the other pins are described in the section **"PIN CONFIGURATION (2) PROM programming mode"**.

1.3 Pin Equivalent Circuits

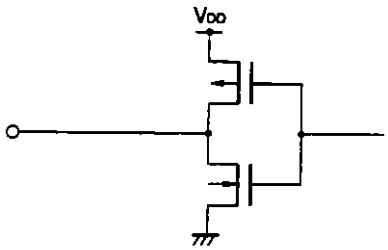
(1) P0A (P0A3/SO, P0A2/$\overline{SCK}$)
P0B (P0B3, P0B2, P0B1, P0B0/SI)
P1B (P1B3, P1B2, P1B1, P1B0)
} (Input/output)



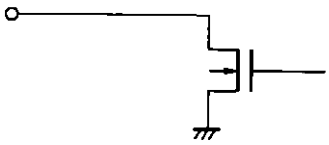
(2) P0A (P0A1/SCL, P0A0/SDA) (Input/output)



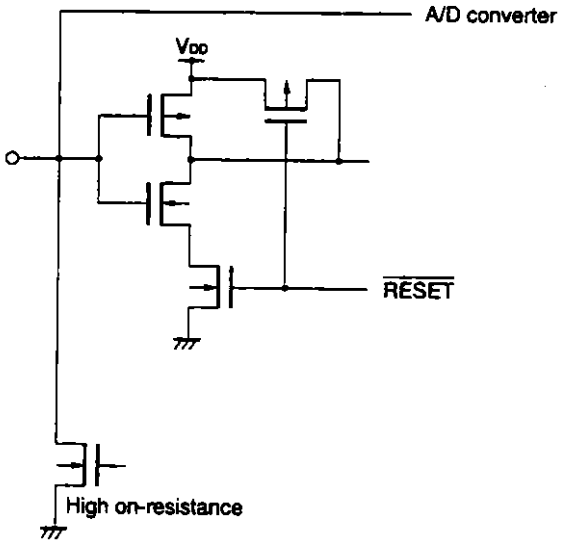
(3) P0C (P0C3, P0C2, P0C1, P0C0)
P1C (P1C0/CGP)
P1D (P1D3, P1D2, P1D1, P1D0) } : (Output)



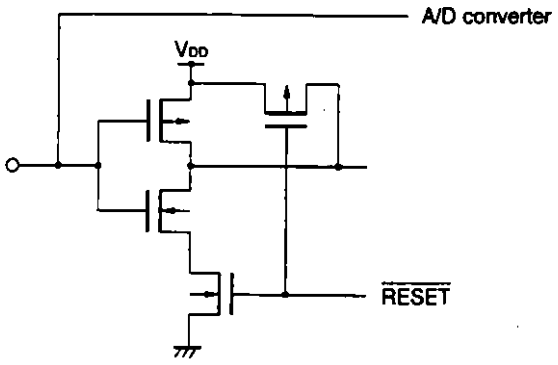
(4) P1C (P1C3/PWM2, P1C2/PWM1, P1C1/PWM0) : (Output)



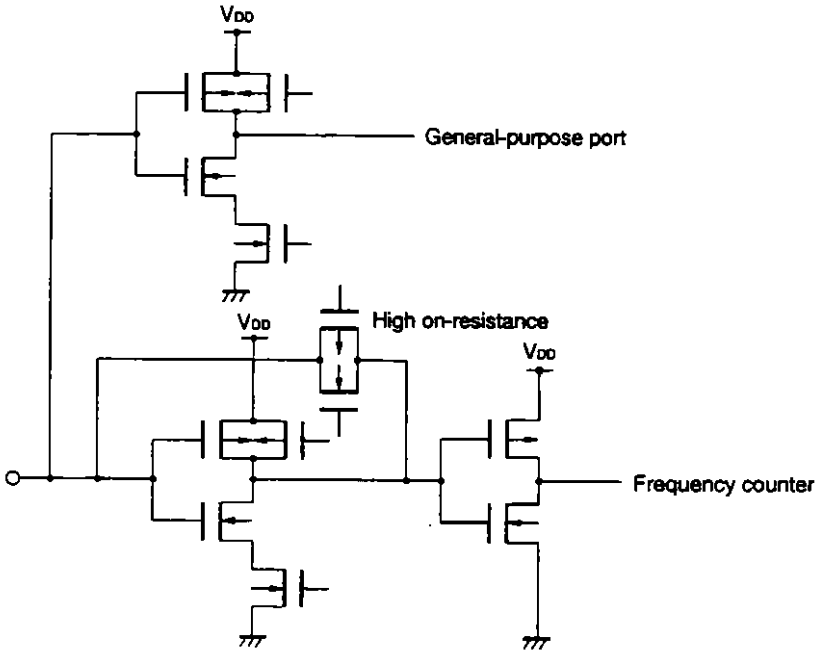
(5) P0D (P0D3/ADC3, P0D2/ADC2, P0D1/ADC1, P0D0/ADC0) : (Input)



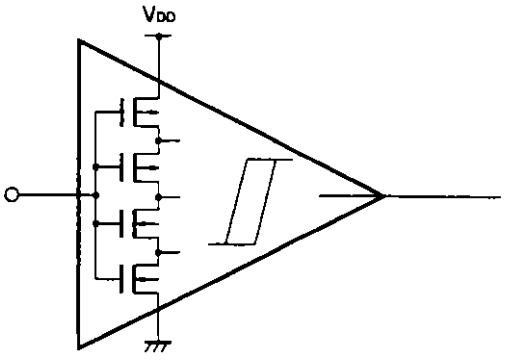
(6) P1A (P1A1/ADC5/FCG, P1A0/ADC4) : (Input)



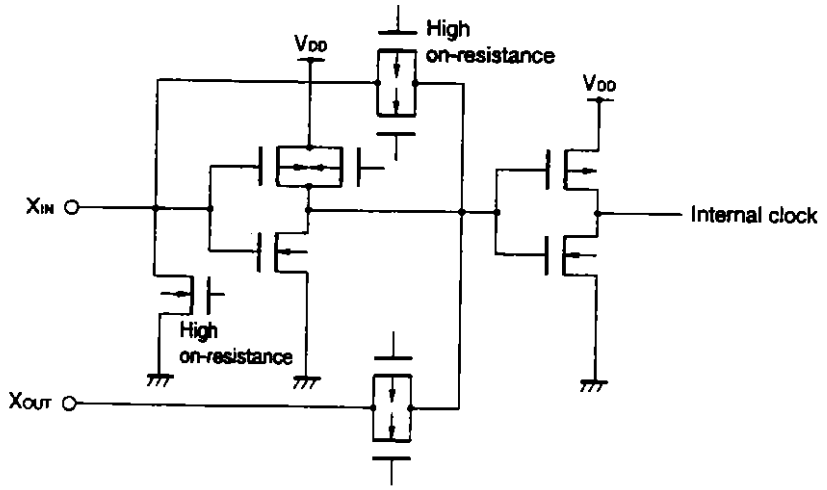
(7) P1A (P1A3/FMIFC, P1A2/AMIFC) : (Input)



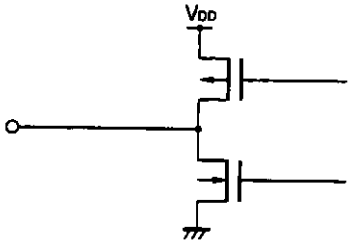
(8) CE, INT : (Schmitt-triggered input)



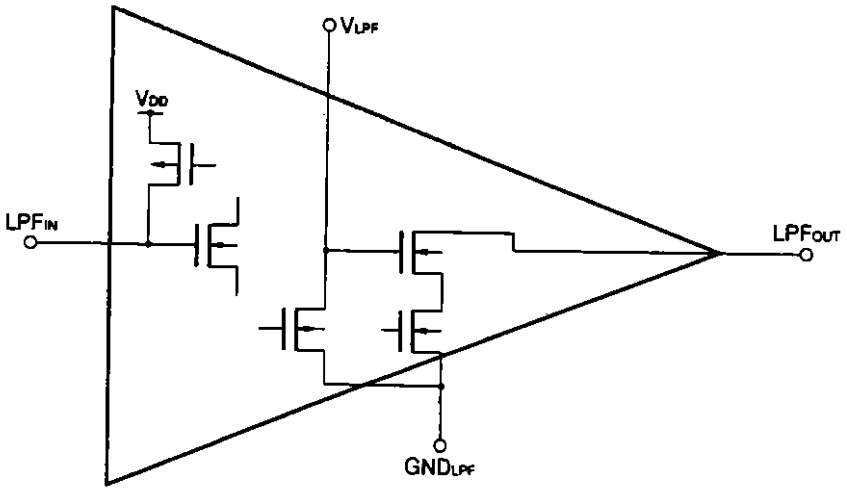
(9) X_{OUT} : (Output), X_{IN} : (Input)



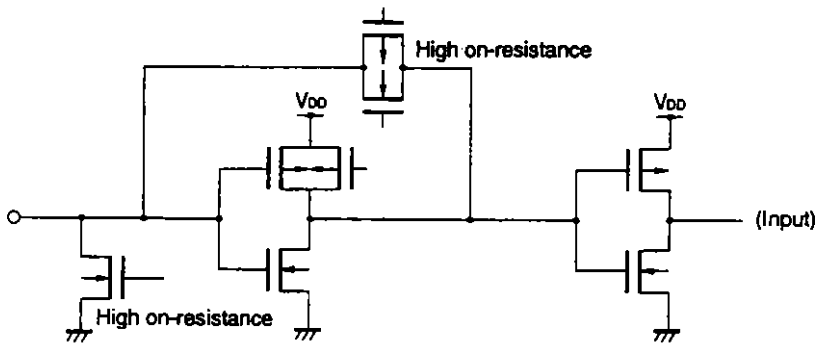
(10) EO1, EO0 : (Output)



(11) LPF_{IN} : (Input), LPF_{OUT} : (Output), V_{LPF}



(12) VCOH, VCOL : (Input)



1.4 Handling of Unused Pins

The following are recommended for handling unused pins.

Table 1-1. Handling of Unused Pins

Pin Name		Input/Output System	Recommended Handling of Unused Pin
Port pins	P0A0/SDA P0A1/SCL P0A2/$\overline{SCK}$ P0A3/SO P0B0/SI P0B1-P0B3	Input/output[Note 1]	Set them to general-purpose input port by software and connect each pin to V_{DD} or GND via a resistor[Note 2].
	P0C0-P0C3	CMOS push-pull output	Leave open.
	P0D0/ADC0-P0D3/ADC3	Input	Connect each pin to GND via a resistor[Note 2].
	P1A0/ADC4 P1A1/ADC5/FCG		Connect each pin to V_{DD} or GND via a resistor[Note 2].
	P1A2/AMIFC[Note 3] P1A3/FMIFC[Note 3]		Set them to a port and connect each pin to V_{DD} or GND via a resistor[Note 2].
	P1B0-P1B3	Input/output[Note 1]	Set them to general-purpose input port by software and connect each pin to V_{DD} or GND via a resistor[Note 2].
	P1C0/CGP	CMOS push-pull output	Leave open.
	P1C1/PWM0-P1C3/PWM2	N-ch open-drain output	Set them to low-level output by software and leave them open.
	P1D0-P1D3	CMOS push-pull output	Leave open.
Non-port pins	CE	Input	Connect to V_{DD} via a resistor[Note 2].
	EO0, EO1	Output	Leave open.
	GND_{LPF}	–	Connect to GND.
	INT	Input	Connect to V_{DD} or GND via a resistor[Note 2].
	LPF_{IN}	Input	Leave open or connect to V_{DD}.
	LPF_{OUT}	N-ch open-drain output	Leave open or connect to GND.
	VCOH, VCOL	Input	Set them to PLL disable by software and leave them open.
	V_{LPF}	–	Leave open or connect to GND.

Notes 1. Input ports go to input mode when the power supply rises, when the clock stops, and on CE reset.

2. Be careful of the fact that when an external pull-up (connection to V_{DD} through a resistor) or pull-down (connection GND through a resistor) is made, if the pull-up or pull-down is done through a resistor with a high value, because the pin comes near to being in high impedance, the (through) current consumption increases. This also depends on the application circuit, but a typical value for a pull-up or pull-down resistor is a few tens of kΩ.

3. Do not set these pins to AMIFC and FMIFC. If set, current consumption increases.

1.5 Notes on Using the CE and INT Pins (Only in Normal Operation Mode)

In addition to the functions shown in 1.1 Normal Operation Mode, the CE pin also has the function of setting a test mode (for IC testing) in which the internal operations of the μPD17P001 are tested.

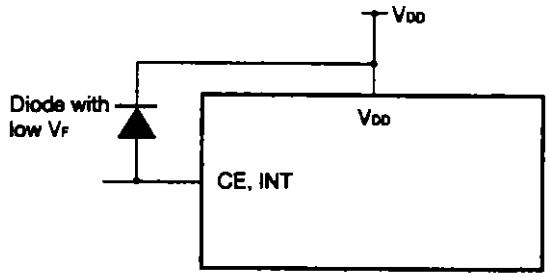
Also, the INT pin has the function of the V_{PP} pin for program memory write/verify.

When a voltage higher than V_{DD} is applied to either of these pins, the test or program memory write/verify mode is set. This means that, even during normal operation, the μPD17P001 may be set in the test mode if noise exceeding V_{DD} is applied.

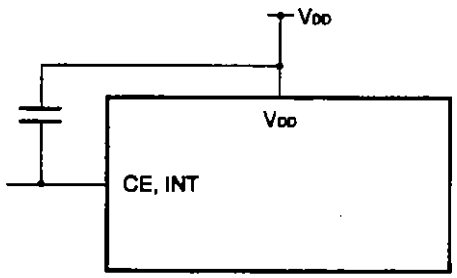
For example, if the wiring length of the CE or INT pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- **Connect diode with low V_F between V_{DD} and CE/INT pin**



- **Connect capacitor between V_{DD} and CE/INT pin**



2. WRITE, READ, AND VERIFY OF ONE-TIME PROM (PROGRAM MEMORY)

The program memory contained in the μPD17P001 is the 3836 × 16-bit one-time PROM that can electrically be written one time only. This PROM is accessed in 16 bits per word in normal operation mode, and in 8 bits per word in write, read, verify modes. The 16 bits of a word in normal mode are divided into higher 8 bits and lower 8 bits which are assigned to even and odd addresses, respectively.

When the PROM is written, read, or verified, set this device into the PROM mode. In this mode, these pins are used as shown in the table below. Notice that no address input pins are provided. Addresses are automatically updated by the clock signal supplied from the CLK pin.

Table 2-1. Pins Used in Program Memory Write, Read, and Verify Modes

Pin	Function
VPP	Programming voltage (+12.5 V) application
CLK	Address update clock input
MD0-MD3	Operation mode selection
D0-D7	8-bit data input/output
V_{DD}	Power supply voltage (+6 V) application

To write the internal PROM, use the NEC-specified PROM programming equipment (PROM programmer) and program adapter as listed below.

PROM programmer	AF-9703	(Ando Electric Corporation)
	AF-9704	(Ando Electric Corporation)
	AF-9705	(Ando Electric Corporation)
	AF-9706	(Ando Electric Corporation)
Program adapter	AF-9796	(Ando Electric Corporation)

Remark For details on these PROM programmer and program adapter, consult with Ando Electric Corporation (03-3733-1163 Tokyo, Japan).

2.1 Operation Modes in Program Memory Write/Read/Verify

When +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin, this device enters the program memory write/read/verify modes. Operation mode is determined by the setting of MD0 to MD3 pins as indicated in the table below.

All input pins irrelevant to the program memory write/read/verify operation should be left unconnected or connected to GND via a pull-down resistor of 470 Ω (Refer to **PIN CONFIGURATION (2) PROM programming mode**).

Table 2-2. Operation Modes in Program Memory Write/Read/Verify

Pin States						Operation Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+5 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write
		L	L	H	H	Read, Verify
		H	X	H	H	Program inhibit

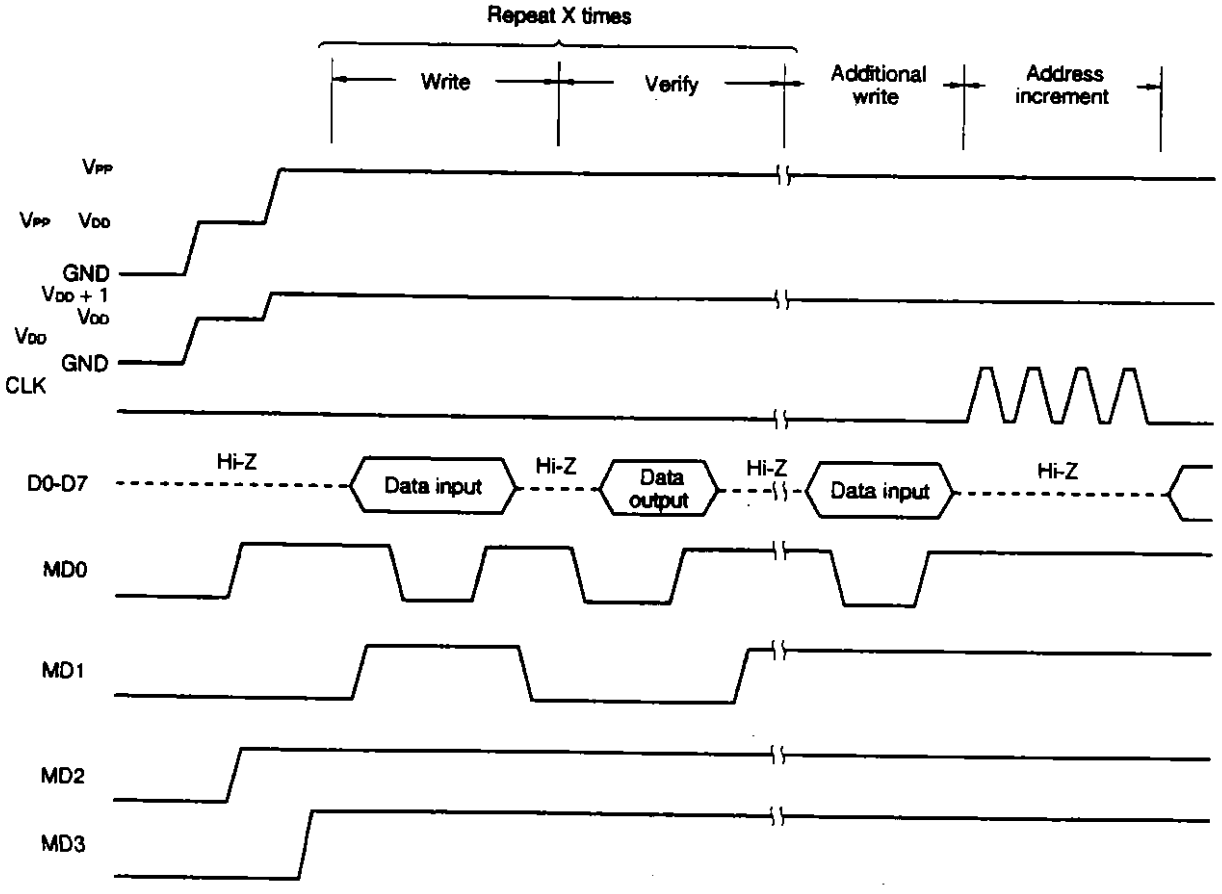
Remark X: L or H

2.2 PROM Write Procedure

Data can be written to the PROM in high speeds by using the following procedures.

(1) Set the pins not used for programming as indicated in PIN CONFIGURATION (2) PROM programming mode. Set the CLK pin to low level.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Provide a 10-μs wait state.
(4) Program memory address 0 clear mode is entered.
(5) Supply +6 V to the V_{DD} pin, and +12.5 V to the V_{PP} pin.
(6) Program inhibit mode is entered.
(7) Provide write data for 1 ms in write mode.
(8) Program inhibit mode is entered.
(9) Use the verify mode to test data. If the data has been written, proceed to (10). If not, repeat steps (7) to (9).
(10) Provide write data (for additional writing) for 1 ms times the number of repeats performed between steps (7) to (9).
(11) Program inhibit mode is entered.
(12) Provide four pulses to the CLK pin to increment the address.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Program memory address 0 clear mode.
(15) Supply +5 V to V_{DD} and V_{PP} pins.
(16) Turn off the power for this device.

The procedures from (2) to (12) are illustrated in the chart below.

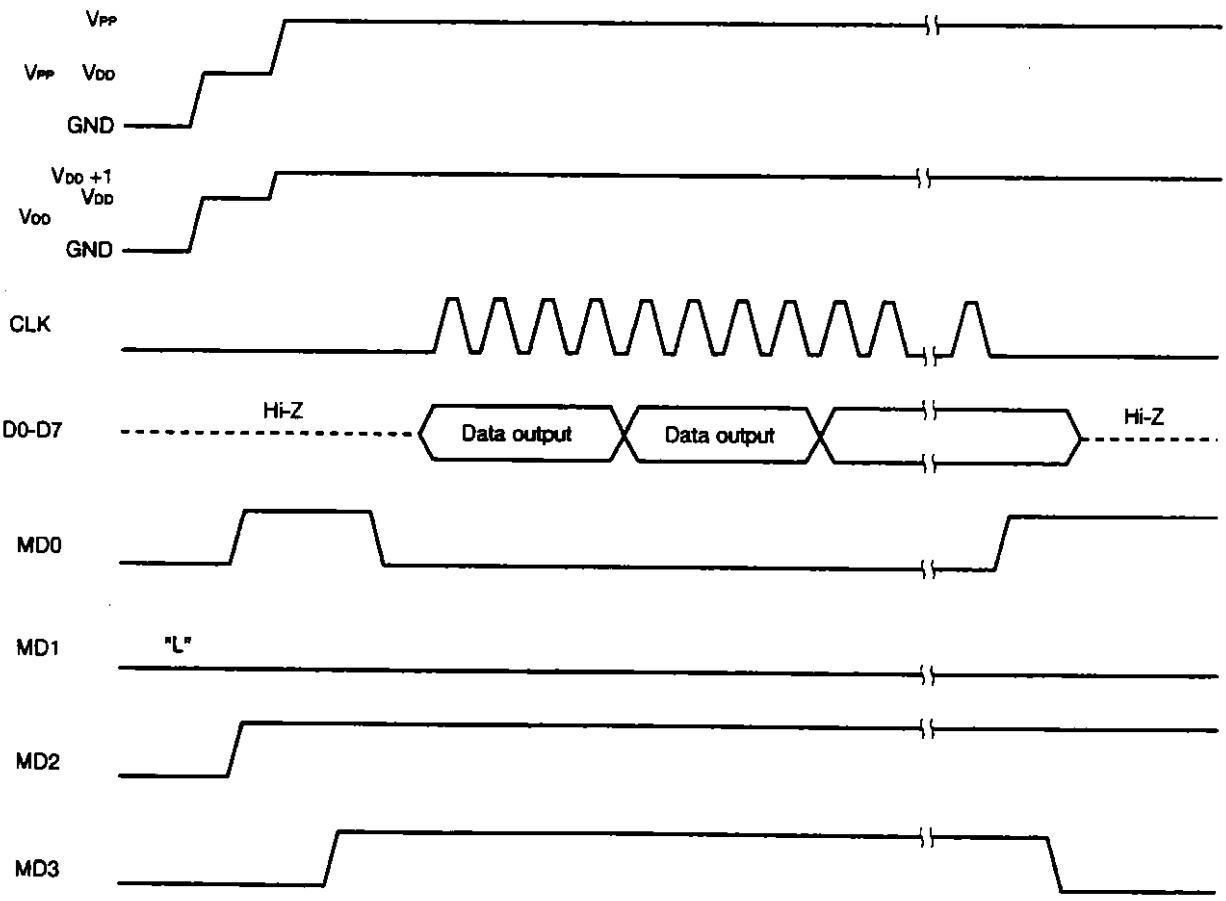


2.3 PROM Read Procedure

Data can be read from the PROM by using the following procedures.

(1) Set the pins not used for programming as indicated in PIN CONFIGURATION (2) PROM programming mode. Set the CLK pin to low level.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Provide a 10-μs wait state.
(4) Program memory address 0 clear mode is entered.
(5) Supply +6 V to the V_{DD} pin, and +12.5 V to the V_{PP} pin.
(6) Program inhibit mode is entered.
(7) Use the verify mode to output data. Provide clock pulses to the CLK pin to output the data of an address. The address is automatically incremented every four clock pulses. Repeat the four-pulse cycles until the last address is reached.
(8) Program inhibit mode is entered.
(9) Program memory address 0 clear mode.
(10) Supply +5 V to the V_{DD} and V_{PP} pins.
(11) Turn off the power for this device.

The procedures from (2) to (9) are illustrated in the chart below.



3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.3 to +6.0	V
Input voltage	V_I		−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Except for P1C1-P1C3, P0A0, P0A1, LPF_{OUT}	−0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin	−12	mA
		All pins	−20	mA
Low-level output current	I_{OL}	1 pin	12	mA
		All pins	20	mA
Output withstand voltage	V_{BDS1}	P1C1-P1C3, LPF_{OUT}	16.0	V
	V_{BDS2}	P0A0, P0A1	V_{DD} + 0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Product quality may suffer if the absolute maximum ratings are exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = −40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	During CPU and PLL operation	4.5	5.0	5.5	V
	V_{DD2}	During CPU operation, PLL stopped	3.9	5.0	5.5	V
Data retention voltage	V_{DDR}	Crystal oscillation stops	2.9		5.5	V
Output withstand voltage	V_{BDS}	P1C1-P1C3, LPF_{OUT}			14.0	V
Supply voltage rise time	t_{RISE}	V_{DD} = 0 → 4.5 V			500	ms
Input amplitude	V_{IN1}	VCOL, VCOH	0.5		V_{DD}	V_{P-P}
	V_{IN2}	AMIFC, FMIFC	0.5		V_{DD}	V_{P-P}

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	When CPU and PLL are operating	4.5	5.0	5.5	V
	V_{DD2}	When CPU is operating and PLL is stopped	3.9	5.0	5.5	V
Supply current	I_{DD1}	When CPU is operating and PLL is stopped X_{IN} pin sine wave input (f_{IN} = 4.5 MHz, V_{IN} = V_{DD}), T_A = 25 °C		2.6		mA
Data retention voltage	V_{DDR1}	Use of power failure detection method using timer FF For crystal oscillation	3.5		5.5	V
	V_{DDR2}	Retention of data memory (RAM)	2.9		5.5	V
Data retention current	I_{DDR1}	When crystal oscillation is stopped T_A = 25 °C		2	15	μA
	I_{DDR1}	When crystal oscillation is stopped V_{DD} = 5.0 V, T_A = 25 °C		2	10	μA
High-level input voltage	V_{IH1}	P0A0-P0A3, P0B0-P0B3, P1A0-P1A3, P1B0-P1B3, CE, INT	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P0D0-P0D3	0.6 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}	P0A0-P0A3, P0B0-P0B3, P0D0-P0D3, P1A0-P1A3, P1B0-P1B3, CE, INT	0		0.2 V_{DD}	V
High-level output current	I_{OH1}	P0A2, P0A3, P0B0-P0B3, PC0-P0C3, P1B0-P1B3, P1C0, P1D0-P1D3 V_{OH} = V_{DD}–1 V	–1.0	–5.0		mA
	I_{OH2}	EO0, EO1 V_{OH} = V_{DD}–1 V	–1.0	–4.0		mA
Low-level output current	I_{OL1}	P0A2, P0A3, P0B0-P0B3, P1B0-P1B3, P1C0, P1D0-P1D3 V_{OL} = 1 V	1.0	7.0		mA
	I_{OL2}	P0C0-P0C3 V_{OL} = 1 V	0.7	1.2		mA
	I_{OL3}	EO0, EO1 V_{OL} = 1 V	1.0	3.5		mA
	I_{OL4}	P1C1-P1C3 V_{OL} = 1 V	1.0	2.0		mA
	I_{OL5}	P0A0, P0A1 V_{OL} = 1 V	1.0	10.0		mA
High-level input current	I_{IH1}	When VCOH is pulled down V_{IH} = V_{DD}	0.1	0.8		mA
	I_{IH2}	When VCOL is pulled down V_{IH} = V_{DD}	0.1	0.8		mA
	I_{IH3}	When X_{IN} is pulled down V_{IH} = V_{DD}	0.1	1.3		mA
	I_{IH4}	When P0D0 to P0D3 are pulled down V_{IH} = V_{DD}	0.05	0.13	0.30	mA
Output off-leakage current	I_{L1}	P0A0, P0A1 V_{OH} = V_{DD}			500	nA
	I_{L2}	P1C1-P1C3 V_{OH} = 14 V			500	nA
	I_{L3}	EO0, EO1 V_{OH} = V_{DD}, V_{CL} = 0 V			±100	nA

AC Characteristics (T_A = −40 to +85 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN1}	VCOL pin MF mode Sine wave input V_{IN} = 0.3 V_{P-P}	0.5		30	MHz
	f_{IN2}	VCOL pin HF mode Sine wave input V_{IN} = 0.3 V_{P-P}	5		40	MHz
	f_{IN3}	VCOH pin Sine wave input V_{IN} = 0.3 V_{P-P}	9		130	MHz
	f_{IN4}	AMIFC pin Sine wave input V_{IN} = 0.3 V_{P-P}	0.1		1	MHz
	f_{IN5}	FMIFC pin Sine wave input V_{IN} = 0.3 V_{P-P}	5		15	MHz
A/D conversion resolution					6	bit
A/D conversion overall error		T_A = −10 to +50 °C		±1	±1.5	LSB

Reference Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2}	When CPU and PLL are operating VCOH pin sine wave input f_{IN} = 130 MHz, V_{IN} = 0.5 V_{P-P}, V_{DD} = 5 V, T_A = 25 °C		15		mA

DC Programming Characteristics (T_A = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Except for CLK	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} − 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Except for CLK	0		0.3 V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			±10	μA
High-level output voltage	V_{OH}	I_{OH} = −1 mA	V_{DD} − 1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD_0 = V_{IL}, MD_1 = V_{IH}			30	mA

Cautions 1. V_{PP} must not exceed +13.5 V including overshoot.

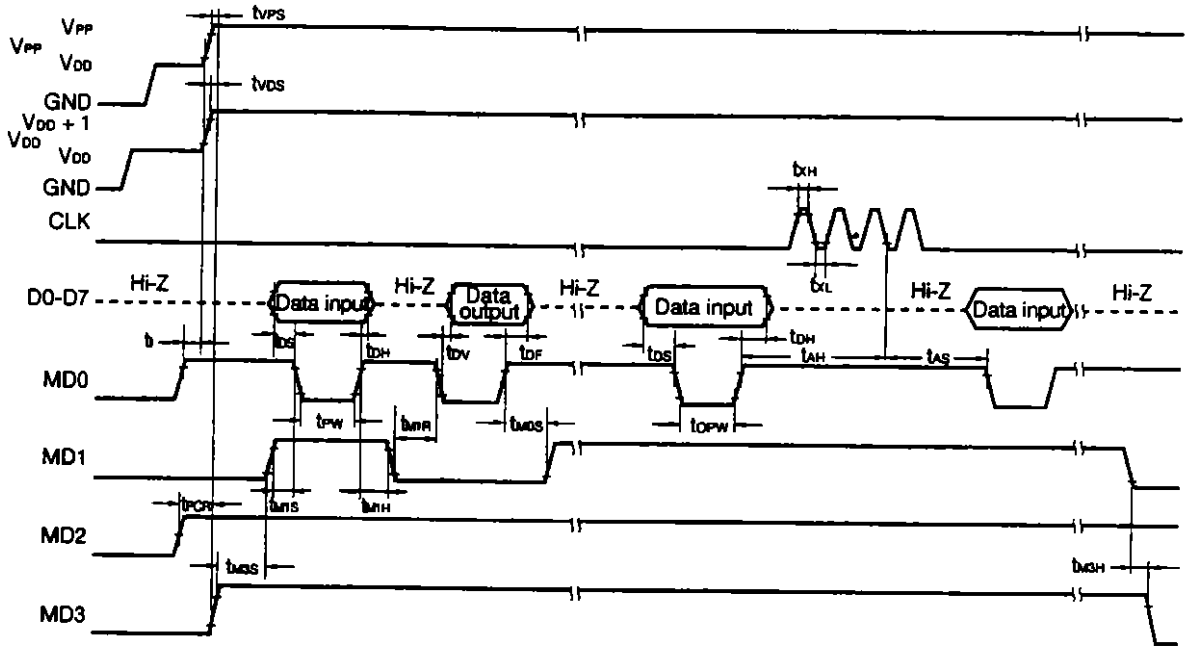
2. V_{DD} should be applied before V_{PP} and cut after V_{PP}.

AC Programming Characteristics (T_A = 25 °C, V_{DD} = 6.0 ± 2.5 V, V_{PP} = 12.5 ± 0.5 V)

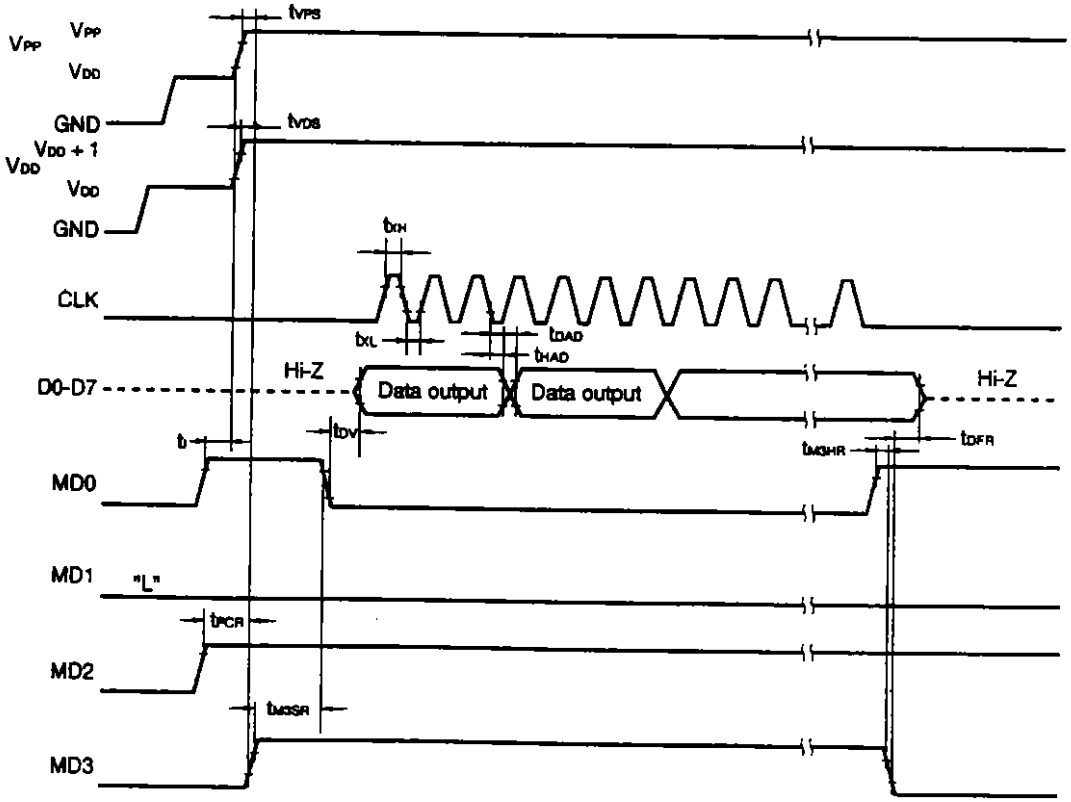
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time Note (vs. MD0↓)	t_{AS}		2			μs
MD1 setup time (vs. MD0↓)	t_{M1S}		2			μs
Data setup time (vs. MD0↓)	t_{DS}		2			μs
Address hold time Note (vs. MD0↑)	t_{AH}		2			μs
Data hold time (vs. MD0↑)	t_{DH}		2			μs
MD0↑→ data output float delay time	t_{DF}		0		130	ns
V_{PP} setup time (vs. MD3↑)	t_{VPS}		2			μs
V_{DD} setup time (vs. MD3↑)	t_{VDS}		2			μs
Initial program pulse width	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}		0.95		21.0	ms
MD0 setup time (vs. MD1↑)	t_{M0S}		2			μs
MD0↓→ data output delay time	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (vs. MD0↑)	t_{M1H}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 recovery time (vs. MD0↓)	t_{M1R}		2			μs
Program counter reset time	t_{PCR}		10			μs
CLK input high-/low-level width	t_{XH}, t_{XL}		0.125			μs
CLK input frequency	f_X				4.19	MHz
Initial mode setting time	t_I		2			μs
MD3 setup time (vs. MD1↑)	t_{M3S}		2			μs
MD3 hold time (vs. MD1↓)	t_{M3H}		2			μs
MD3 setup time (vs. MD0↓)	t_{M3SR}	When program memory is read	2			μs
Address Note → data output delay time	t_{DAD}				2	μs
Address Note → data output hold time	t_{HAD}		0		130	ns
MD3 hold time (vs. MD0↑)	t_{M3HR}		2			μs
MD3↓→ data output float delay time	t_{DFR}				2	μs

Note The internal address increment (+1) is performed on the fall of the 3rd clock, where 4 clocks comprise one cycle. The internal clock is not connected to a pin.

Program Memory Write Timing

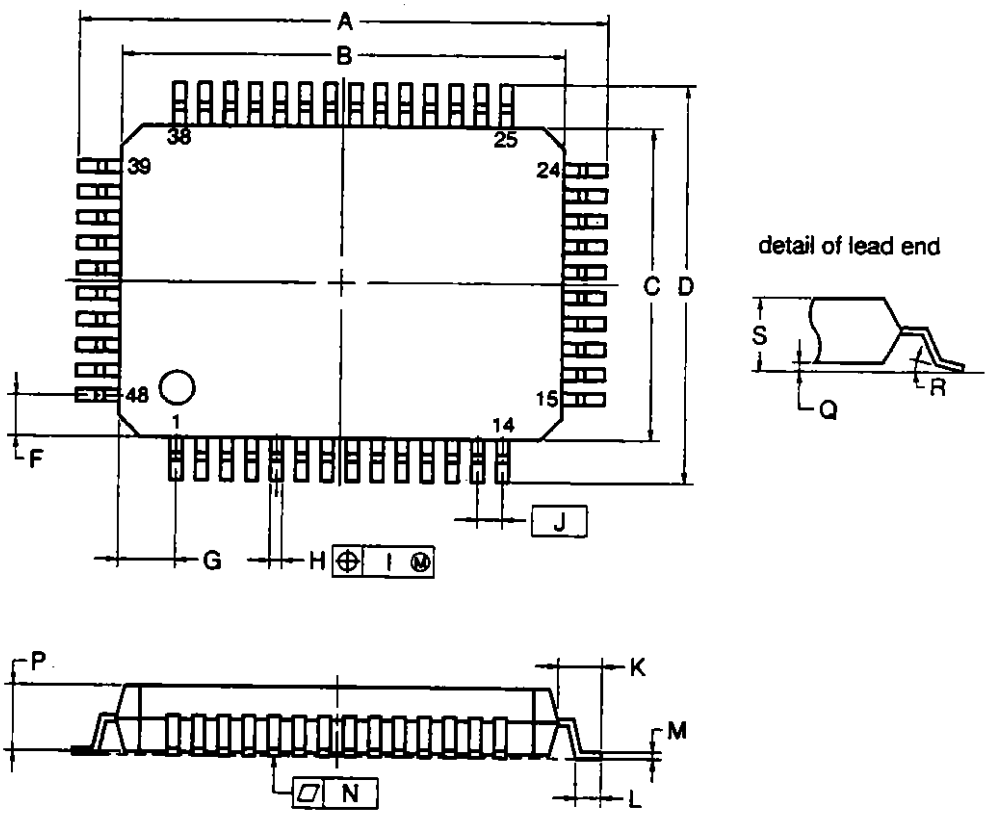


Program Memory Read Timing



4. PACKAGE DRAWING

48 PIN PLASTIC QFP (10×14)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.8±0.4	$0.661^{+0.017}_{-0.016}$
B	14.0±0.2	0.551±0.008
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	12.8±0.4	0.504±0.016
F	1.4	0.055
G	1.8	0.071
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.2±0.1	$0.087^{+0.004}_{-0.005}$
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	2.5 MAX.	0.099 MAX.

P48GH-80-2A5-4

5. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 5-1. Surface Mount Type Soldering Conditions

μPD17P001GH-2A5: 48-Pin Plastic QFP (10 × 14 mm, 0.8-mm pitch)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C Duration: 30 sec. max. (210 °C or above) Number of times: Max. 2 Time limit: 7 days[Note] (thereafter 20 hours 125 °C prebaking required) <Caution> Baking cannot be applied to other than heat-resistant trays (magazine, taping, non-heat-resistant trays) when the product is wrapped.	IR35-207-2
VPS	Package peak temperature: 215 °C Duration: 40 sec. max. (200 °C or above) Number of times: Max. 2 Time limit: 7 days[Note] (thereafter 20 hours 125 °C prebaking required) <Caution> Baking cannot be applied to other than heat-resistant trays (magazine, taping, non-heat-resistant trays) when the product is wrapped.	VP15-207-2
Wave soldering	Solder bath temperature: 260 °C or less Duration: 10 sec. max. Number of times: one Preparatory heating temperature: 120 °C max. (package surface temperature) Time limit: 7 days[Note] (thereafter 20 hours 125 °C prebaking required) <Caution> Baking cannot be applied to other than heat-resistant trays (magazine, taping, non-heat-resistant trays) when the product is wrapped.	WS60-207-1
Partial heating	Pin temperature: 300 °C or less Duration: 3 sec. max. (per side of device)	–

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65% RH.

Caution Use of more than one soldering method should be avoided (except in the case of pin heating).

APPENDIX DEVELOPMENT TOOLS

The following tools are available to provide μPD17P001's program development environment.

Hardware

Product	Description
In-circuit emulator (IE-17K IE-17K-ET Note 1 EMU-17K Note 2)	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators common to the 17K series. The IE-17K and IE-17K-ET should be connected with the host computer (PC-9800 series or IBM PC/AT™) through an RS-232-C cable. The EMU-17K should be installed to an extension slot in the host computer (PC-9800 series). Each of the three products function as a dedicated emulator for each device by connecting it with an individual system evaluation board (SE board). Using *SIMPLEHOST*™ which features an excellent user-machine interface, makes user's debugging environment more powerful. If the EMU-17K is used, user can monitor the contents of the data memory in real time.
SE board (SE-17001)	This SE board is for the μPD17P001 and 17001. This board can perform evaluations of user's system. To debug user's programs, use it together with an in-circuit emulator.
Emulation probe (EP-17001GH)	This probe is used when emulating the μPD17P001GH.
Conversion socket (EV-9200GH-48 Note 3)	This socket converts pin arrangement for the 48-pin plastic QFP (10 × 14 mm) to connect the emulation probe EP-17001 to the target system.
PROM programmer (AF-9703 Note 4 AF-9704 Note 4 AF-9705 Note 4 AF-9706 Note 4)	These products write programs to the internal PROM of the μPD17P001. To perform programming, the program adapter AF-9796 is required to connect to the PROM programmer.
Program adapter (AF-9796 Note 4)	This adapter is used together with the PROM programmer to program the PROM in the μPD17P001.

Notes 1. Inexpensive type: Power supply is required to connect externally.

2. Manufactured by IC Corporation. For details, call 03-3447-3793 Tokyo, Japan.
3. If the EP-17001GH is purchased, one EV-9200GH-48 is attached as a companion product. EV-9200GH-48s can separately be purchased in 5-piece units.
4. Manufactured by Ando Electric Corporation. For details, call 03-3733-1151 Tokyo, Japan.

Software

Product	Description	Host Computer	OS		Media	Ordering Code
17K series assembler (AS17K)	This assembler can be used for all 17K series devices. To develop program of the μPD17P001, the device file (AS17001) are also required.	PC-9800 Series	MS-DOS™		5 inch 2HD	μS5A10AS17K
					3.5 inch 2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5 inch 2HC	μS7B10AS17K
					3.5 inch 2HC	μS7B13AS17K
Device file (AS17001)	This product is the device file for the μPD17P001. This device file is used together with the assembler AS17K.	PC-9800 series	MS-DOS		5 inch 2HD	μS5A10AS17001
					3.5 inch 2HD	μS5A13AS17001
		IBM PC/AT	PC DOS		5 inch 2HC	μS7B10AS17001
					3.5 inch 2HC	μS7B13AS17001
Support software (*SIMPLEHOST*)	This software is used to develop programs using an in-circuit emulator and the host computer. This product runs under Windows™ system and provides users with an excellent user-machine interface.	PC-9800 Series	MS-DOS	Windows	5 inch 2HD	μS5A10IE17K
					3.5 inch 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5 inch 2HC	μS7B10IE17K
					3.5 inch 2HC	μS7B13IE17K

Remark These products run with the versions of the operation systems shown below.

OS	Version
MS-DOS	Ver.3.30 to Ver.5.00A Note
PC DOS	Ver.3.1 to Ver.5.0 Note
Windows	Ver.3.0 to Ver.3.1

Note With these products, the task swap function is disabled though the Ver.5.00/5.00A of MS-DOS and Ver.5.0 of the PC DOS support the task swap function.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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