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April 1st, 2010
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RENESAS

MOS INTEGRATED CIRCUIT

μPD178F048

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD178F048 is a flash memory version of the μPD178046 and 178048, and is provided with a flash memory to/from which data can be written/erased with the microcontroller mounted on a printed circuit board. Therefore, it is suitable for test production when developing systems and systems for which frequent upgrading is expected.

The functions are described in detail in the following User's Manuals. Be sure to read them before starting design.

μPD178048 Subseries User's Manual : To be prepared
78K/0 Series User's Manual - Instructions : U12326E

FEATURES

- OSD (On Screen Display) controller and PWM (Pulse Width Modulation) output
- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory: 60 Kbytes**Note**
- Character ROM (CROM): 6912 bytes (256 character types)
- Internal high-speed RAM: 512 bytes
- Internal extension RAM: 512 bytes
- Video RAM: 432 bytes (12 × 24 characters Max.)
- Operable at the same supply voltage as mask ROM versions (V_{DD} = 4.5 to 5.5 V)

Note The capacity of the flash memory can be changed by using the internal memory size switching register (IMS).

Remark For the differences between the flash memory version and mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD178F048 AND MASK ROM VERSIONS**.

The electrical specifications (such as supply current) in the μPD178F048 differ from those of the mask ROM versions. Confirm these differences before mass-producing any application set.

APPLICATION FIELD

TVs

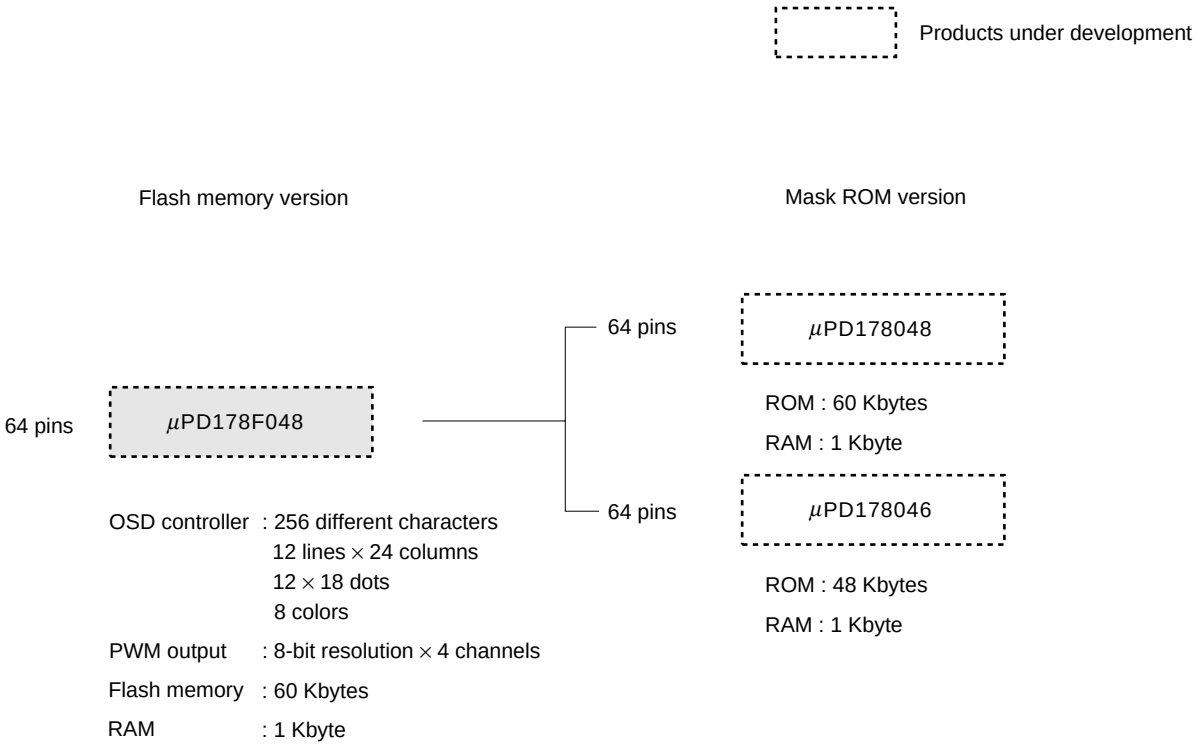
ORDERING INFORMATION

Part Number	Package
μPD178F048CW	64-pin plastic shrink DIP (750 mils)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Document No. U13056EJ1V0PM00
Date Published April 1998 N CP (K)
Printed in Japan

μPD178048 SUBSERIES LINEUP



FUNCTION OUTLINE

(1/2)

Item		Functions
Internal memory	Flash memory	60 Kbytes
	Character ROM (CROM)	6912 bytes (256 character types)
	High-speed RAM	512 bytes
	Extension RAM	512 bytes
	Video RAM (VRAM)	432 bytes (12 × 24 characters Max.)
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (with 5.0-MHz crystal resonator)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test Boolean operation) • BCD adjust, etc.
I/O port		Total : 46 pins • CMOS input : 4 pins • CMOS I/O : 37 pins • N-ch open-drain output : 5 pins
A/D converter		8-bit resolution × 4 channels
Serial interface		• I^2C bus mode[Note] : 2 channels (shift register: 1 channel) • 3-wire serial I/O mode : 1 channel
Timer		• Basic timer (timer carry (10 Hz)) : 1 channel • 8-bit timer/event counter : 1 channel • 8-bit timer : 1 channel • 8-bit event counter : 1 channel • 8-bit remote control timer : 1 channel • Watchdog timer : 1 channel
PWM output		• 8-bit resolution × 4 channels • 14-bit resolution × 1 channel
OSD controller	Number of characters displayed	Maximum 288 characters per screen (12 lines × 24 columns)
	Number of character types	256 (contained in CROM)
	Character format	12 (width) × 18 (height) dots
	Character size	Selectable from 1 × 1, 2 × 2, 3 × 3, and 4 × 4
	Character color	8
	Character frame	Selectable from with/without frame per screen
	Background	Selectable from without background, knockout, and solid. Background color specifiable (8 colors).
	Half blanking	Specifiable per character
Vectored interrupt source	Maskable	Internal: 11, External: 5
	Non-maskable	Internal: 1
	Software	1

Note If the I^2C bus mode is used (including when the mode is implemented in software without using peripheral hardware), consult NEC when ordering a mask.

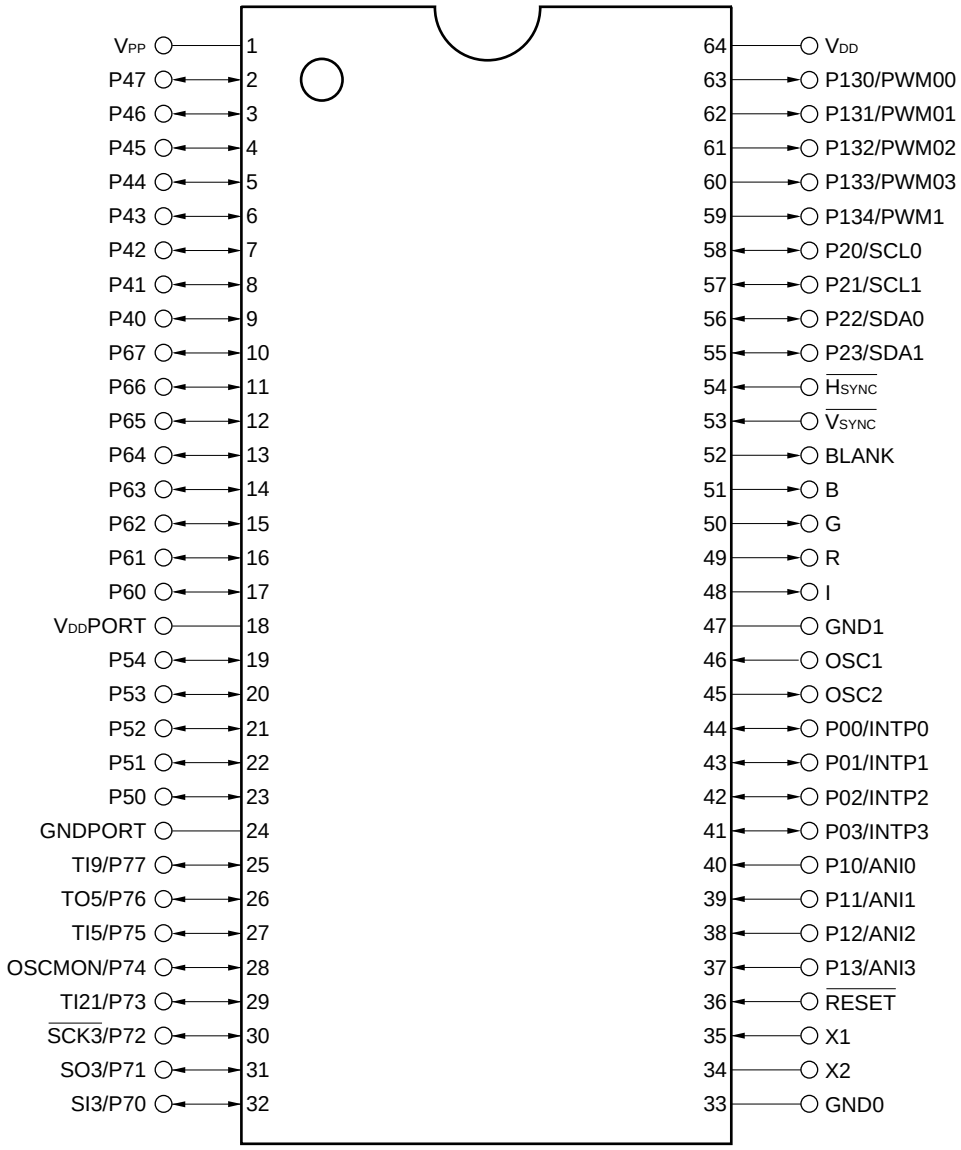
(2/2)

Item	Functions
Standby function	• HALT mode • STOP mode
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Reset by power-ON clear circuit • Detection of less than 4.5 V[Note] (during CPU operation and when turning on the power supply voltage • Detection of less than 2.5 V[Note] (in STOP mode)
Supply voltage	V_{DD} = 4.5 to 5.5 V
Package	64-pin plastic shrink DIP (750 mils)

Note These are maximum values. In practice, reset occurs at lower voltages than those indicated here.

PIN CONFIGURATION (Top View)

- **64-pin plastic shrink DIP (750 mils)**
  μPD178F048CW



Cautions 1. Directly connect the V_{PP} pin to GND0 or GND1 in normal operating mode.

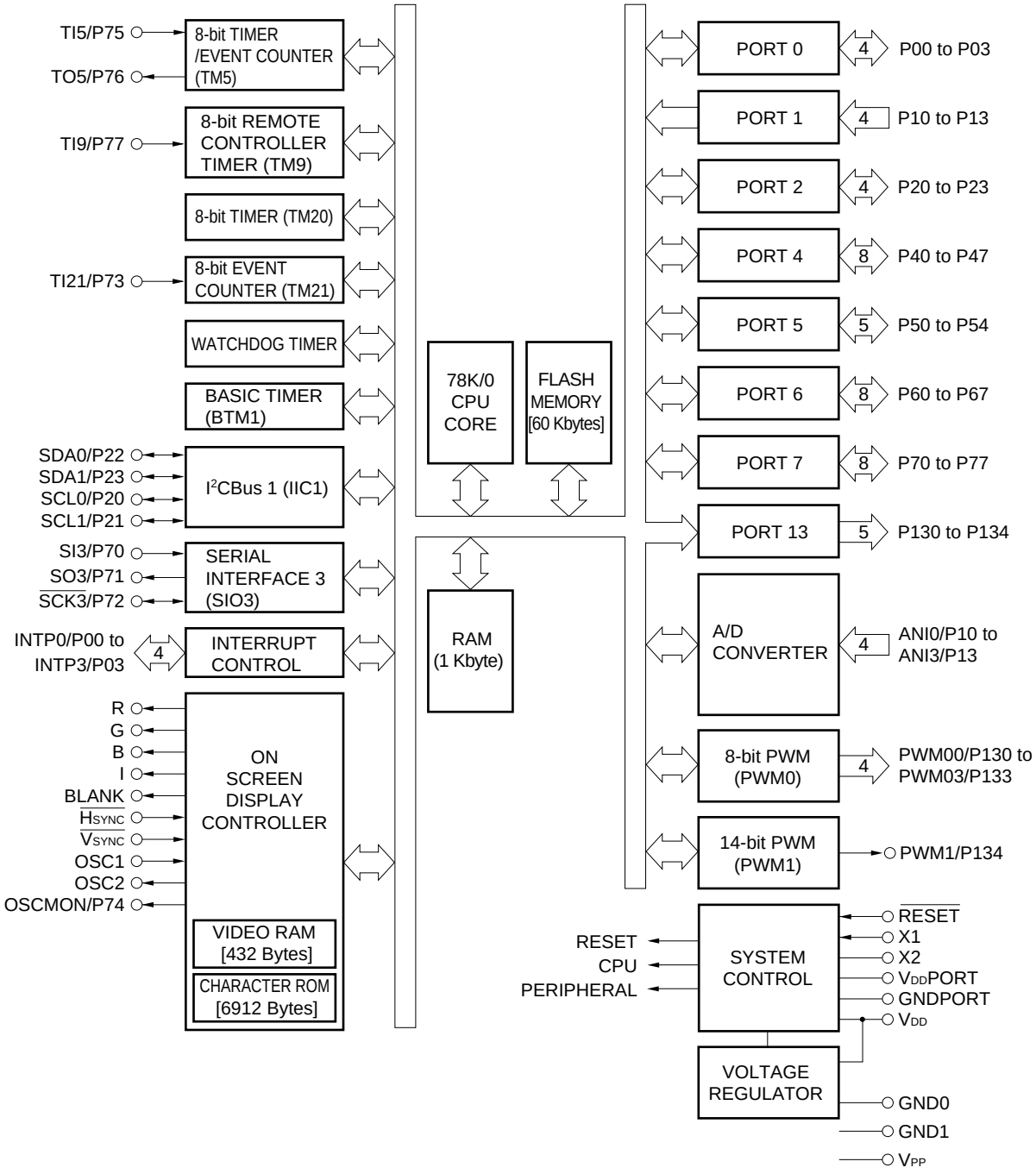
2. Keep the voltage at V_{DD}PORT same as that at the V_{DD} pin.

3. Keep the voltage at GNDPORT same as that at GND0 or GND1.

Pin Identification

ANI0 to ANI3 : A/D converter input
B : Character signal output
BLANK : Blanking signal output
G : Character signal output
GND0, GND1 : Ground
GNDPORT : Ground port
$\overline{H_{SYNC}}$: Horizontal sync signal input
I : Character signal output
INTP0 to INTP3 : Interrupt input
OSC1, OSC2 : Connection of LC for OSD dot clock oscillation
OSCMON : OSD clock output
P00 to P03 : Port 0
P10 to P13 : Port 1
P20 to P23 : Port 2
P40 to P47 : Port 4
P50 to P54 : Port 5
P60 to P67 : Port 6
P70 to P77 : Port 7
P130 to P134 : Port 13
PWM00 to PWM03 : 8-bit PWM output
PWM1 : 14-bit PWM output
R : Character signal output
$\overline{RESET}$: Reset input
$\overline{SCK3}$: Serial clock input/output
SCL0, SCL1 : Serial clock input/output
SDA0, SDA1 : Serial data input/output
SI3 : Serial data input
SO3 : Serial data output
TI5, TI9, TI21 : 8-bit timer clock input
TO5 : 8-bit timer output
V_{DD} : Power supply
V_{DD}PORT : Port power supply
V_{PP} : Programming power supply
$\overline{V_{SYNC}}$: Vertical sync signal input
X1, X2 : Connection of crystal resonator for system clock oscillation

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD178F048 AND MASK ROM VERSIONS

The μPD178F048 is provided with a flash memory to/from which data can be written/erased with the device mounted on a printed circuit board. The differences between the flash memory version (μPD178F048) and mask ROM versions (μPD178046 and 178048) are shown in Table 1-1.

Table 1-1. Differences Between μPD178F048 and Mask ROM Versions

Item		μPD178F048	μPD178046, 178048
Internal memory	ROM type	Flash memory	Mask ROM
	ROM capacity	60 Kbytes	μPD178046: 48 Kbytes μPD178048: 60 Kbytes
ROM correction		Not provided	Provided
Internal ROM capacity setting by means of internal memory size switching register (IMS)		Equivalent to mask ROM version	μPD178046: 4CH μPD178048: 4FH
IC pin		Not provided	Provided
V_{PP} pin		Provided	Not provided
Electrical specifications and recommended soldering conditions		Some characteristics and soldering conditions of the flash memory version differ from those of the mask ROM versions.	

2. PIN FUNCTION LIST

2.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0 4-bit I/O port Can be set in input or output mode in 1-bit units.	Input	INTP0 to INTP3
P10 to P13	Input	Port 1 4-bit input port	Input	ANI0 to ANI3
P20, P21	I/O	Port 2 4-bit I/O port Can be set in input or output mode in 1-bit units.	Input	SCL0, SCL1
P22, P23				SDA0, SDA1
P40 to P47	I/O	Port 4 8-bit I/O port Can be set in input or output mode in 1-bit units.	Input	—
P50 to P54	I/O	Port 5 5-bit I/O port Can be set in input or output mode in 1-bit units.	Input	—
P60 to P67	I/O	Port 6 8-bit I/O port Can be set in input or output mode in 1-bit units.	Input	—
P70	I/O	Port 7 8-bit I/O port Can be set in input or output mode in 1-bit units.	Input	SI3
P71				SO3
P72				$\overline{\text{SCK3}}$
P73				TI21
P74				OSCMON
P75				TI5
P76				TO5
P77				TI9
P130 to P133	Output	Port 13 5-bit output port N-ch open-drain output port (5-V withstand)	—	PWM00 to PWM03
P134				PWM1

2.2 Non-Port Pins

Pin Name	I/O	Function		After Reset	Alternate Function
INTP0 to INTP3	Input	External maskable interrupt input whose valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.		Input	P00 to P03
SI3	Input	Serial data input to serial interface		Input	P70
SO3	Output	Serial data output from serial interface		Input	P71
SDA0, SDA1	I/O	Serial data input/output to/from serial interface	N-ch open-drain I/O	Input	P22, P23
$\overline{SCK3}$	I/O	Serial clock input/output to/from serial interface.		Input	P72
SCL0, SCL1	I/O		N-ch open-drain I/O	Input	P20, P21
TI5	Input	External count clock input to 8-bit timer/event counter (TM5)		Input	P75
TI9		External count clock input to 8-bit remote control timer (TM9)			P77
TI21		External count clock input to 8-bit event counter (TM21)			P73
TO5	Output	8-bit timer/event counter (TM5) output		Input	P76
ANI0 to ANI3	Input	Analog input to A/D converter		Input	P10 to P13
PWM00 to PWM03	Output	8-bit PWM output	N-ch open-drain I/O	—	P130 to P133
PWM1		14-bit PWM output			P134
OSCMON	Output	OSD clock output		Input	P74
$\overline{V_{SYNC}}$	Input	OSD vertical sync signal input		Input	—
$\overline{H_{SYNC}}$		OSD horizontal sync signal input			—
R	Output	RED output for OSD character and background		Low-level output	—
G		GREEN output for OSD character and background			—
B		BLUE output for OSD character and background			—
I		Character background output for OSD character and background in knockout mode			—
BLANK		OSD blanking signal output			—
$\overline{RESET}$	Input	System reset input		—	—
X1	Input	Connection of crystal resonator for system clock oscillation		—	—
X2	—			—	—
OSC1	Input	Connection of LC for OSD dot clock oscillation		—	—
OSC2	Output			—	—
V_{DD}	—	Positive power supply		—	—
GND0, GND1	—	Ground		—	—
V_{DD}PORT	—	Port power supply		—	—
GNDPORT	—	Port ground		—	—
V_{PP}	—	Pin to apply high voltage at program writing/verifying Directly connect this pin to GND0 or GND1 in normal operating mode.		—	—

2.3 I/O Circuits of Pins and Recommended Connection of Unused Pins

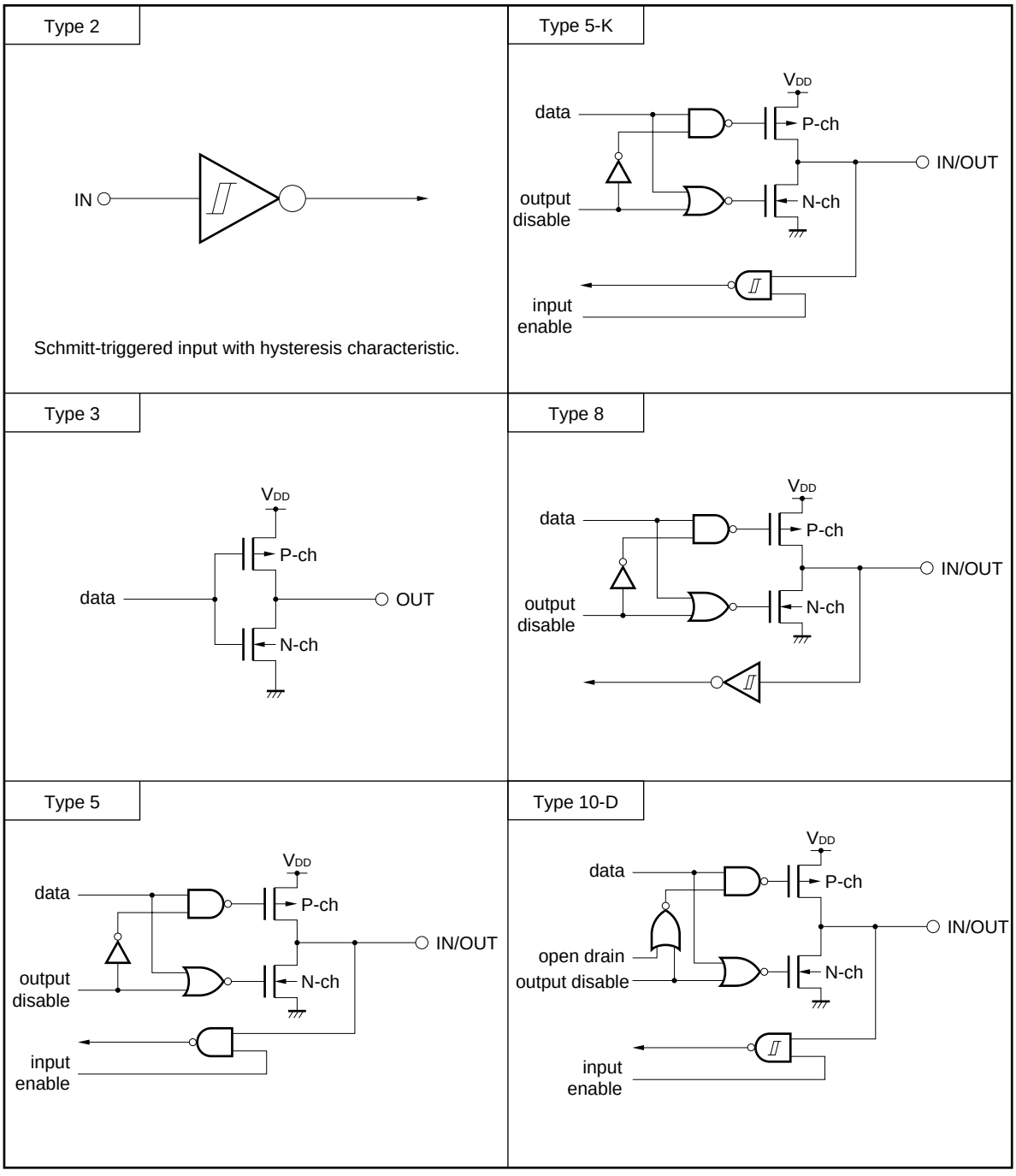
Table 2-1 shows the types of the I/O circuits of the respective pins and the recommended connections of the pins when they are not used.

For the configuration of the I/O circuit of each pin, refer to Figure 2-1.

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins

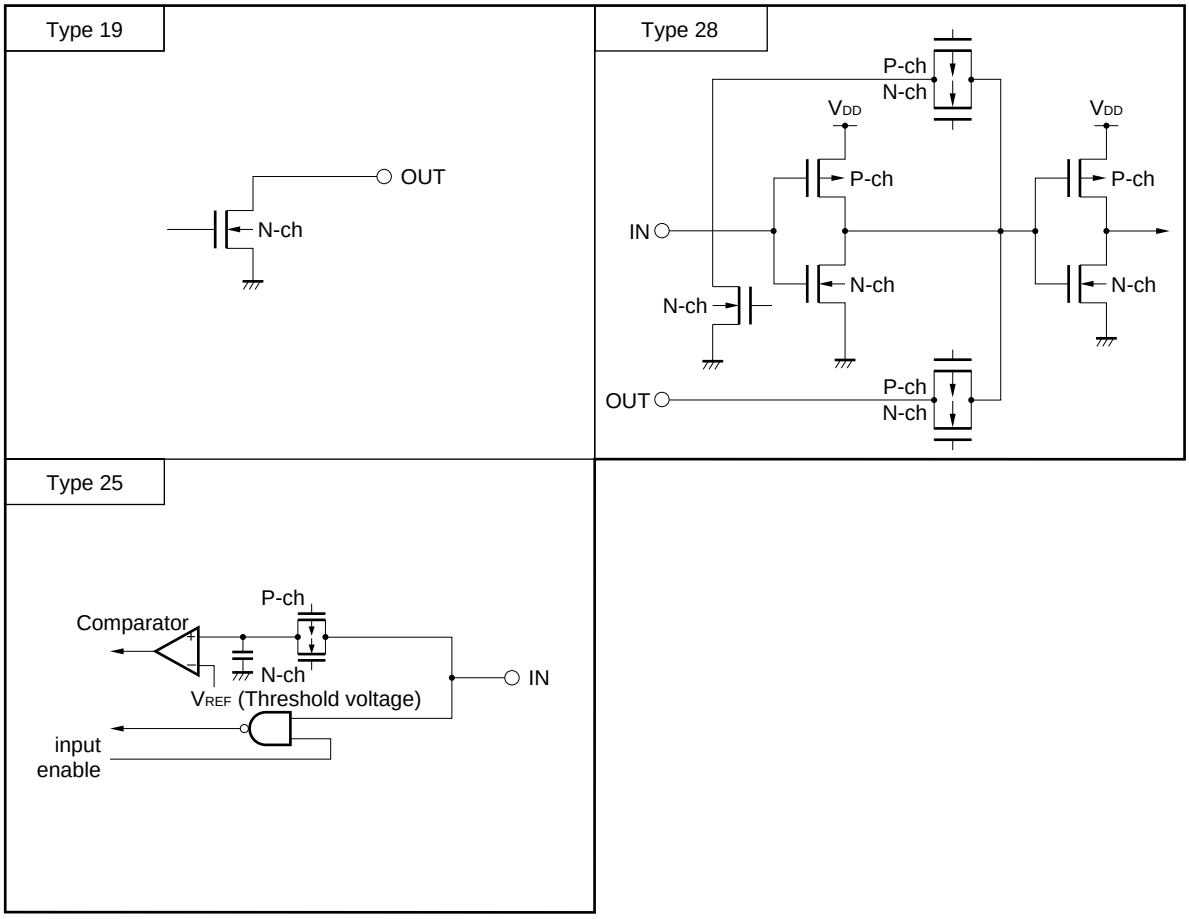
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P00/INTP0 to P03/INTP3	8	I/O	Set these pins in general-purpose input port by software, and connect each of them to GND0, GND1, or GNDPORT via a resistor.
P10/ANI0 to P13/ANI3	25	Input	Connect independently these pins to V_{DD}, V_{DD}PORT, GND0, GND1, or GNDPORT via a resistor.
P20/SCL0, P21/SCL1	10-D	I/O	Set these pins in general-purpose input port by software, and connect each of them to V_{DD}, V_{DD}PORT, GND0, GND1, or GNDPORT via a resistor.
P22/SDA0, P23/SDA1			
P40 to P47	5		
P50 to P54			
P60 to P67			
P70/SI3	5-K		
P71/SO3	5		
P72/$\overline{\text{SCK3}}$	5-K		
P73/TI21			
P74/OSCMON	5		
P75/TI5	5-K		
P76/TO5	5		
P77/TI9	5-K		
P130/PWM00 to P133/PWM03	19	Output	Set these pins to low-level output by software and leave them open.
P134/PWM1			
$\overline{V_{SYNC}}$	2	Input	Connect independently these pins to GND0 or GND1 via a resistor.
$\overline{H_{SYNC}}$			
R	3	Output	Set OSD display to off by software, and leave open.
G			
B			
I			
BLANK			
$\overline{\text{RESET}}$	2	Input	—
OSC1	28	Input	Set LC oscillation to off by software, and leave open.
OSC2		Output	Leave open.
V_{PP}	—	—	Connect directly to GND0 or GND1.

Figure 2-1. Pin I/O Circuits (1/2)



Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT, respectively.

Figure 2-1. Pin I/O Circuits (2/2)



Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT, respectively.

3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

The internal memory capacity of the μPD178F048 can be changed using the internal memory size switching register (IMS). By using this register, the memory of the μPD178F048 can be mapped in the same manner as a mask ROM version with a different internal memory capacity.

Use an 8-bit memory manipulation instruction to set IMS.

This register is set to CFH after reset.

Figure 3-1. Format of Internal Memory Size Switching Register (IMS)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	1	0	512 bytes
Others			Setting prohibited

RAM3	RAM2	RAM1	RAM0	Internal ROM capacity selection
1	1	0	0	48 Kbytes
1	1	1	1	60 Kbytes
Others				Setting prohibited

Table 3-1 shows the setting of IMS to perform the same memory mapping as that of a mask ROM version.

Table 3-1. Setting of Internal Memory Size Switching Register

Product	Setting of IMS
μPD178046	4CH
μPD178048	4FH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

The internal expansion RAM capacity of the μPD178F048 can be changed using the internal expansion RAM size switching register (IXS). By using this register, the memory of the μPD178F048 can be mapped in the same manner as a mask ROM version with a different internal expansion RAM capacity.

Use an 8-bit memory manipulation instruction to set IXS.

This register is set to 0CH after reset.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register (IXS)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal extension RAM capacity selection
0	1	0	1	1	512 bytes
Others					Setting prohibited

Table 4-1 shows the setting of IXS to perform the same memory mapping as that of a mask ROM version.

Table 4-1. Setting of Internal Expansion RAM Size Switching Register

Product	Setting of IXS
μPD178046, 178048	0BH

5. FLASH MEMORY PROGRAMMING

The flash memory can be written on-board, i.e., with the μPD178F048 mounted on the target system.

To do so, connect a dedicated flash programmer (Flashpro II (part number FL-PR2)) to the host machine and target system.

The flash memory can also be written on a flash memory writing adapter connected to Flashpro II.

Remark Flashpro II is a product of Naito Densei Machidaseisakusho Co., Ltd.

5.1 Selecting Communication Mode

The flash memory is written by using Flashpro II and by means of serial communication. Select a communication mode from those listed in Table 5-1. To select a communication mode, the format shown in Figure 5-1 is used. Each communication mode is selected depending on the number of V_{PP} pulses shown in Table 5-1.

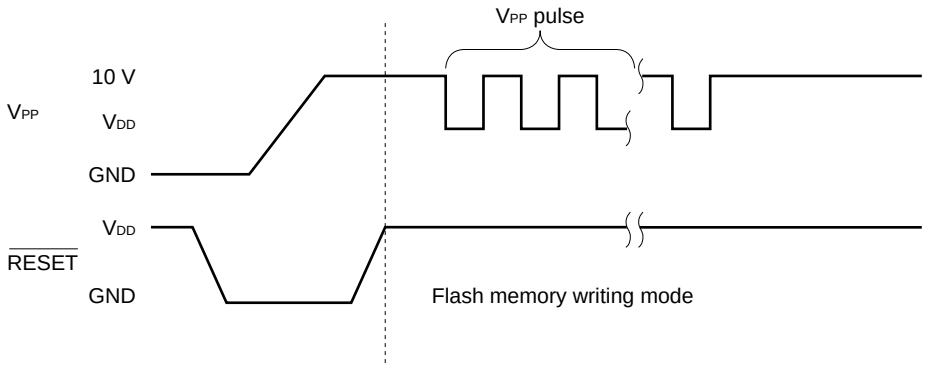
Table 5-1. Communication Modes

Communication Mode	Number of Channels	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O (IIC1)	1	SI3/P70 SO3/P71 $\overline{SCK3}$/P72	0
Pseudo 3-wire serial I/O[Note]	1	P50 (serial clock input) P51 (serial data output) P52 (serial data input)	12

Note Performs serial transfer by controlling a port by software.

Caution Be sure to select a communication mode by the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Communication Mode Selection Format



5.2 Flash Memory Programming Function

An operation such as writing the flash memory is performed when a command or data is transmitted/received in the selected communication mode. The major flash memory programming functions are listed in Table 5-2.

Table 5-2. Major Flash Memory Programming Functions

Function	Description
Reset	Used to stop writing or detect communication synchronization.
Batch verify	Compares all contents of memory with input data.
Batch erase	Erases all memory contents.
Batch blank check	Checks erased status of entire memory.
High-speed write	Writes data to flash memory starting from write start address and based on number of data (bytes) to be written.
Successive write	Successively writes data to flash memory based on information input for high-speed write.
Status	Used to check current operation mode and end of current operation.
Oscillation frequency setting	Inputs frequency information of resonator.
Erase time setting	Inputs erase time of memory.
Silicon signature read	Outputs device name, memory capacity, and block information of device.

5.3 Connecting Flashpro II

Connection with Flashpro II differs depending on the communication mode (3-wire serial I/O or pseudo 3-wire serial I/O). Figures 5-2 and 5-3 show the connection in the respective modes.

Figure 5-2. Connection of Flashpro II in 3-wire Serial I/O Mode

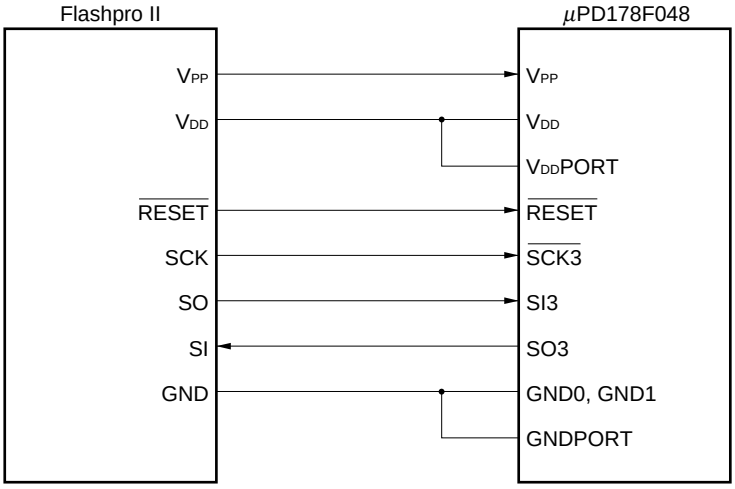
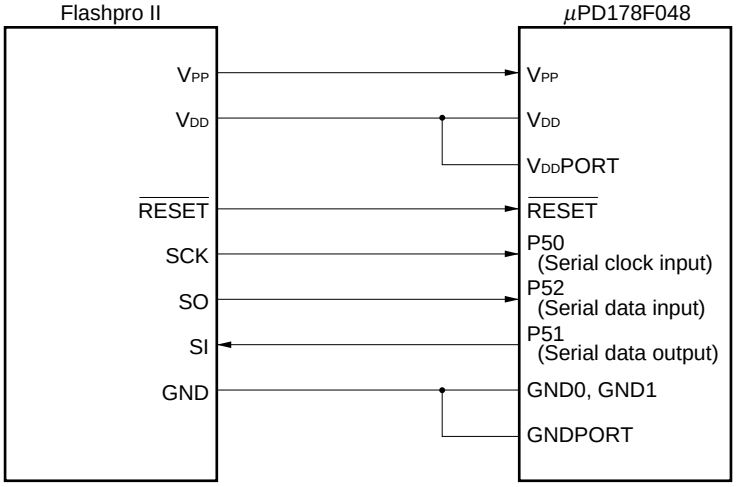
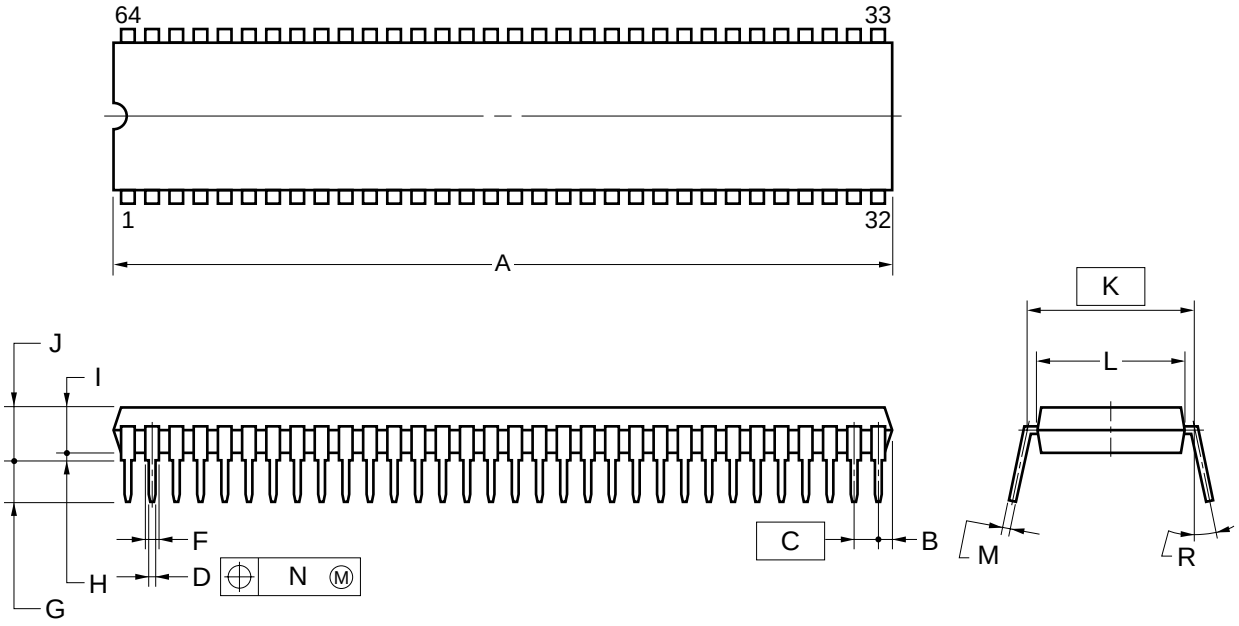


Figure 5-3. Connection of Flashpro II in Pseudo 3-wire Serial I/O Mode



6. PACKAGE DRAWING

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTES

1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	$58.0^{+0.68}_{-0.20}$	$2.283^{+0.028}_{-0.008}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	$4.05^{+0.26}_{-0.20}$	$0.159^{+0.011}_{-0.008}$
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0±0.2	$0.669^{+0.009}_{-0.008}$
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0 to 15°	0 to 15°

P64C-70-750A,C-3

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD178F048.
Also refer to **(5) Notes on using development tools**.

(1) Language processor software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF178048**Note**	Device file for μPD178048 Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) Flash memory writing tools

Fashpro II	Dedicated flash memory programmer
Product name undecided**Note**	Flash writing adapter

(3) Debugging tools

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter used when PC-9800 series (except notebook type) is used as host machine
IE-70000-CD-IF	PC card and interface cable used when notebook type PC-9800 series is used as host machine
IE-70000-PC-IF-C	Interface adapter used when IBM PC/AT™ or compatible is used as host machine
IE-178048-NS-EM1**Note**	Emulation board to emulate μPD178048 Subseries
Product name undecided**Note**	Emulation probe for 64-pin plastic shrink DIP
ID78K0-NS**Note**	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF178048**Note**	Device file for μPD178048 Subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Notes on using development tools

- Use ID78K0-NS and SM78K0 in combination with DF178048.
- Use RX78K/0 in combination with RA78K/0 and DF178048.
- Flashpro II, flash writing adapter (product name undecided), and emulation probe (product name undecided) are products of Naito Densei Machidaseisakusho Co., Ltd. (Phone: +81-44-822-3813). Consult an authorized NEC distributor when purchasing these products.
- For development tools made by third parties, refer to **78K/0 Series Selection Guide (U11126E)**.
- The host machine corresponding to each software package is as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT and Compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UM™] SPARCstation™ [SunOS™] NEWS (RISC)™ [NEWS-OS™]
RA78K/0	√Note	√
CC78K/0	√Note	√
ID78K0-NS	√	—
SM78K0	√	—
RX78K/0	√Note	√
MX78K0	√Note	√

Note This software is based on DOS.

APPENDIX B. RELATED DOCUMENTS

Device Documents

Title		Document No.	
		English	Japanese
μPD178046, 178048 Preliminary Product Information		To be prepared	U13183J
μPD178048 Subseries User's Manual		To be prepared	To be prepared
78K/0 Series User's Manual — Instructions		U12326E	U12326J
78K/0 Series Instruction Set		—	U10904J
78K/0 Series Instruction Table		—	U10903J
μPD178048 Subseries Special Function Register Table		—	To be prepared
78K/0 Series Application Note	Basics (I)	IEA-1288	U12704J

Development Tool Documents (User's Manual)

Title		Document No.	
		English	Japanese
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K0 C Compiler Application Note	Programming Know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	U12322J
IE-78K0-NS		To be prepared	To be prepared
IE-178048-NS-EM1		To be prepared	To be prepared
SM78K0 System Simulator Windows Based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Parts User open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger PC Based	Reference	To be prepared	U12900J

Caution The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.

Related Documents for Embedded Software (User's Manual)

Title		Document No.	
		English	Japanese
78K/0 Series Real-time OS	Fundamentals	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Fundamental	U12257E	U12257J

Other Documents

Title	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Guides on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Device by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer-related Product Guide (Products by other Manufacturers)	—	U11416J

Caution The contents of the above documents are subject to change without notice. Ensure that the latest versions are used in design work, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Purchase of NEC I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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