To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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RENESAS

MOS INTEGRATED CIRCUIT

μPD16782A

SOURCE DRIVER FOR 300/288-OUTPUT TFT-LCD

DESCRIPTION

μPD16782A is a source driver for TFT liquid crystal panels. This IC consists of a multiplexer circuit supporting a variety of pixel arrays, a shift register that generates sampling timing, and two sample and hold circuits that sample analog voltages. Because the two sample and hold circuits alternately execute sampling and holding, a high definition can be obtained.

Besides, according to the pixel arrangement of the LCD panel, it can respond to simultaneous sampling and successive sampling. It is ideal for a wide range of applications, including navigation systems and automobile LCD-TVs.

FEATURES

- Can be driven on 5 V (Dynamic range: 4.6 V, V_{DD2} = 5.0 V)
- 300/288-output
- f_{CLK} = 15 MHz MAX. (V_{DD1} = 3.0 V)
- Simultaneous/sequential sampling selectable according to pixel array
  Simultaneous sampling: Vertical stripe
  Sequential sampling: Vertical stripe, delta array, mosaic array
- Two sets of sample and hold circuits
- Stripe, delta, and mosaic pixel arrays supported by internal multiplexer circuit
- Left and right shift selected by R,/L pin
- COG mounting possible

Remark /xxx indicates active low signal.

ORDERING INFORMATION

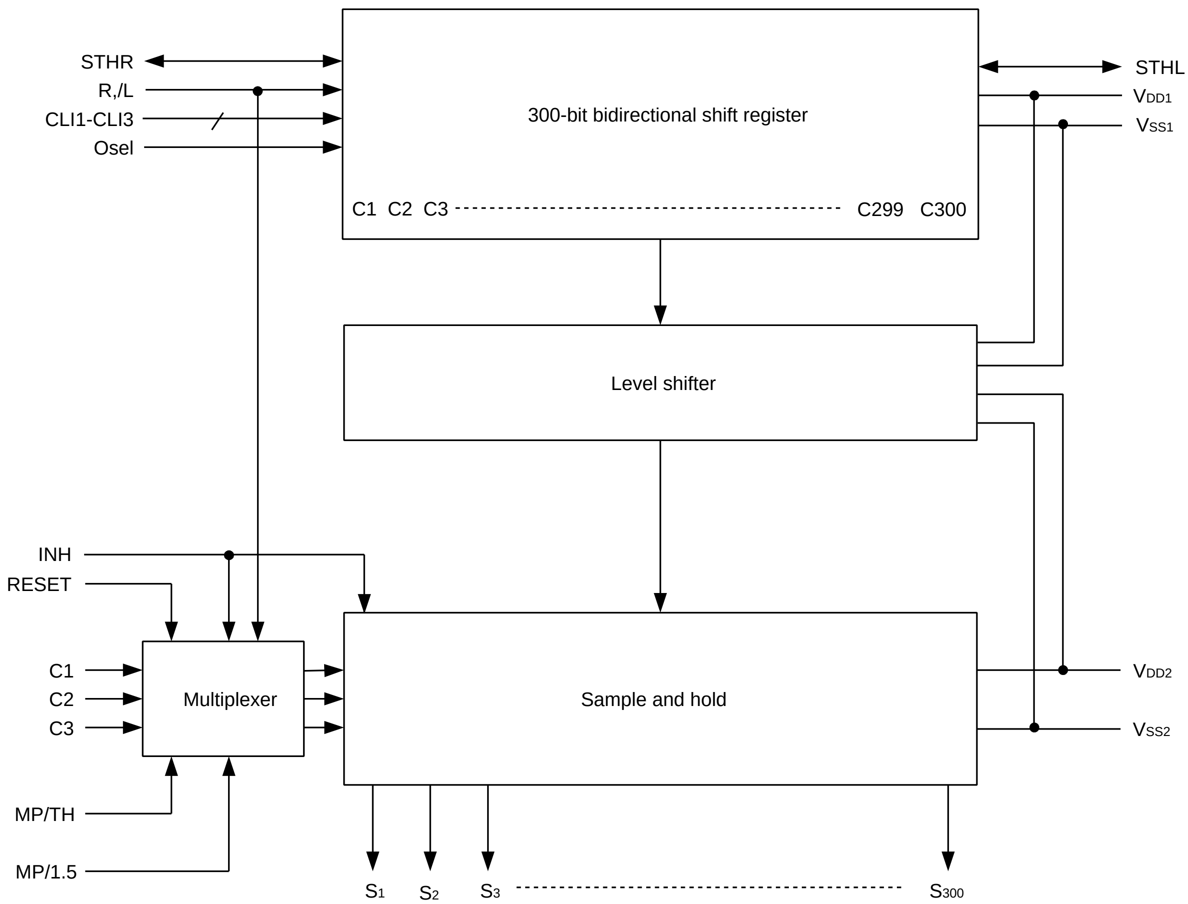
Part Number	Package
μ PD16782AP	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

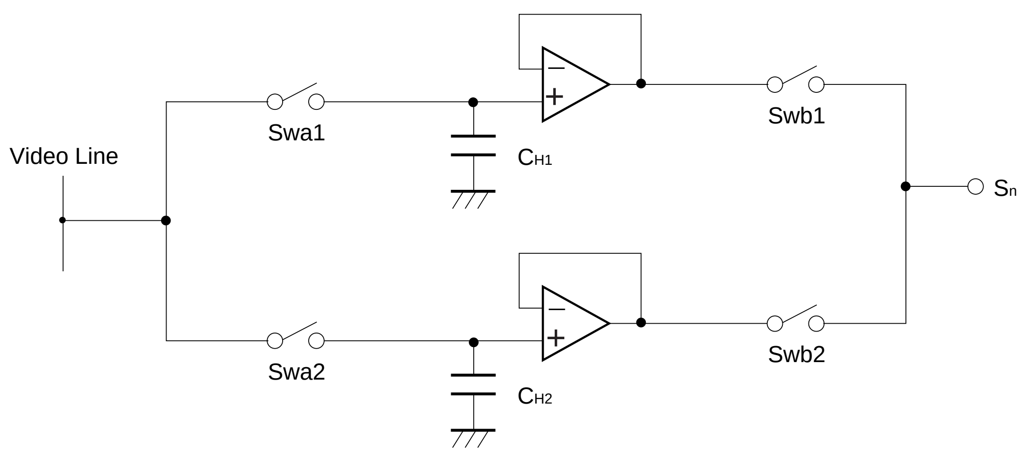
Document No. S16593EJ1V0DS00 (1st edition)
Date Published January 2004 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM



2. SAMPLE AND HOLD CIRCUIT AND OUTPUT CIRCUIT



3. PIN CONFIGURATION

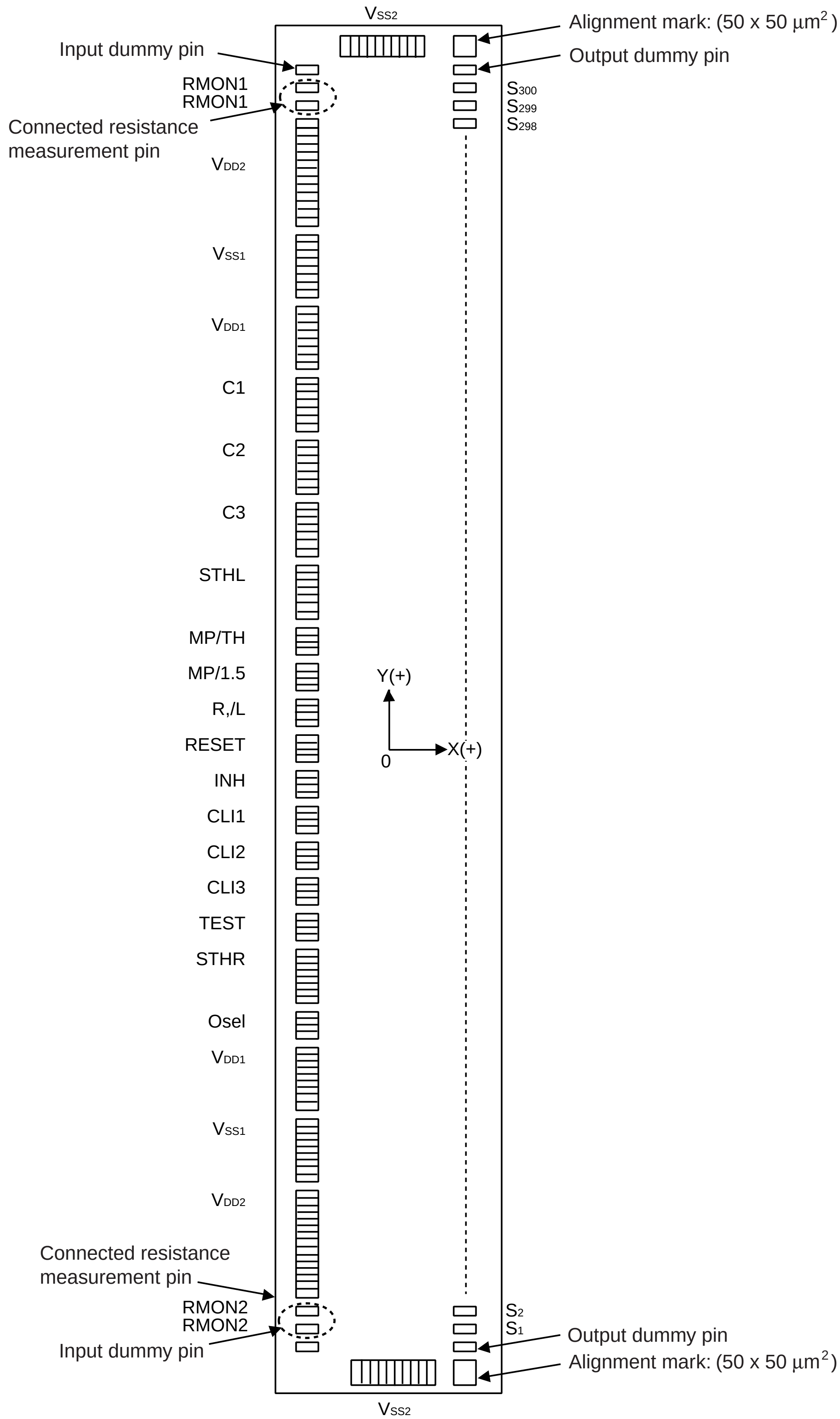


Table 3–1. Pad Coordinate (1/4)

No.	Pad Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
1	Dummy1	-464.0	8451.0	100:60
2	RMON1	-464.0	8014.2	100:60
3	RMON1	-464.0	7842.0	100:60
4	V_{DD2}	-464.0	7538.6	100:60
5	V_{DD2}	-464.0	7458.6	100:60
6	V_{DD2}	-464.0	7378.6	100:60
7	V_{DD2}	-464.0	7298.6	100:60
8	V_{DD2}	-464.0	7218.6	100:60
9	V_{DD2}	-464.0	7138.6	100:60
10	V_{DD2}	-464.0	7058.6	100:60
11	V_{DD2}	-464.0	6978.6	100:60
12	V_{DD2}	-464.0	6898.6	100:60
13	V_{DD2}	-464.0	6818.6	100:60
14	V_{DD2}	-464.0	6738.6	100:60
15	V_{DD2}	-464.0	6658.6	100:60
16	V_{SS1}	-464.0	6181.0	100:60
17	V_{SS1}	-464.0	6101.0	100:60
18	V_{SS1}	-464.0	6021.0	100:60
19	V_{SS1}	-464.0	5941.0	100:60
20	V_{SS1}	-464.0	5861.0	100:60
21	V_{SS1}	-464.0	5781.0	100:60
22	V_{SS1}	-464.0	5701.0	100:60
23	V_{DD1}	-464.0	5239.4	100:60
24	V_{DD1}	-464.0	5159.4	100:60
25	V_{DD1}	-464.0	5079.4	100:60
26	V_{DD1}	-464.0	4999.4	100:60
27	V_{DD1}	-464.0	4919.4	100:60
28	V_{DD1}	-464.0	4839.4	100:60
29	V_{DD1}	-464.0	4759.4	100:60
30	C1	-464.0	4335.2	100:60
31	C1	-464.0	4255.2	100:60
32	C1	-464.0	4175.2	100:60
33	C1	-464.0	4095.2	100:60
34	C1	-464.0	4015.2	100:60
35	C1	-464.0	3935.2	100:60
36	C2	-464.0	3470.4	100:60
37	C2	-464.0	3390.4	100:60
38	C2	-464.0	3310.4	100:60
39	C2	-464.0	3230.4	100:60
40	C2	-464.0	3150.4	100:60
41	C2	-464.0	3070.4	100:60
42	C3	-464.0	2605.6	100:60
43	C3	-464.0	2525.6	100:60
44	C3	-464.0	2445.6	100:60
45	C3	-464.0	2365.6	100:60
46	C3	-464.0	2285.6	100:60
47	C3	-464.0	2205.6	100:60
48	STHL	-464.0	1384.2	100:60
49	STHL	-464.0	1304.2	100:60
50	STHL	-464.0	1224.2	100:60
51	STHL	-464.0	1144.2	100:60
52	STHL	-464.0	1064.2	100:60
53	STHL	-464.0	984.2	100:60
54	MP/TH	-464.0	538.6	100:60
55	MP/TH	-464.0	458.6	100:60
56	MP/TH	-464.0	378.6	100:60
57	MP/1.5	-464.0	145.5	100:60
58	MP/1.5	-464.0	65.5	100:60
59	MP/1.5	-464.0	-14.5	100:60
60	R,/L	-464.0	-247.6	100:60
61	R,/L	-464.0	-327.6	100:60
62	R,/L	-464.0	-407.6	100:60
63	RESET	-464.0	-640.7	100:60
64	RESET	-464.0	-720.7	100:60
65	RESET	-464.0	-800.7	100:60
66	INH	-464.0	-1033.8	100:60
67	INH	-464.0	-1113.8	100:60
68	INH	-464.0	-1193.8	100:60
69	CLI1	-464.0	-1427.0	100:60
70	CLI1	-464.0	-1507.0	100:60
71	CLI1	-464.0	-1587.0	100:60
72	CLI2	-464.0	-1820.1	100:60
73	CLI2	-464.0	-1900.1	100:60
74	CLI2	-464.0	-1980.1	100:60
75	CLI3	-464.0	-2213.2	100:60
76	CLI3	-464.0	-2293.2	100:60
77	CLI3	-464.0	-2373.2	100:60
78	TEST	-464.0	-2606.3	100:60
79	TEST	-464.0	-2686.3	100:60
80	TEST	-464.0	-2766.3	100:60
81	STHR	-464.0	-3227.0	100:60
82	STHR	-464.0	-3307.0	100:60
83	STHR	-464.0	-3387.0	100:60
84	STHR	-464.0	-3467.0	100:60
85	STHR	-464.0	-3547.0	100:60
86	STHR	-464.0	-3627.0	100:60
87	Osel	-464.0	-4170.4	100:60
88	Osel	-464.0	-4250.4	100:60
89	Osel	-464.0	-4330.4	100:60
90	V_{DD1}	-464.0	-4759.4	100:60
91	V_{DD1}	-464.0	-4839.4	100:60
92	V_{DD1}	-464.0	-4919.4	100:60
93	V_{DD1}	-464.0	-4999.4	100:60
94	V_{DD1}	-464.0	-5079.4	100:60
95	V_{DD1}	-464.0	-5159.4	100:60
96	V_{DD1}	-464.0	-5239.4	100:60
97	V_{SS1}	-464.0	-5701.0	100:60
98	V_{SS1}	-464.0	-5781.0	100:60
99	V_{SS1}	-464.0	-5861.0	100:60
100	V_{SS1}	-464.0	-5941.0	100:60
101	V_{SS1}	-464.0	-6021.0	100:60
102	V_{SS1}	-464.0	-6101.0	100:60
103	V_{SS1}	-464.0	-6181.0	100:60
104	V_{DD2}	-464.0	-6658.6	100:60
105	V_{DD2}	-464.0	-6738.6	100:60
106	V_{DD2}	-464.0	-6818.6	100:60
107	V_{DD2}	-464.0	-6898.6	100:60
108	V_{DD2}	-464.0	-6978.6	100:60
109	V_{DD2}	-464.0	-7058.6	100:60
110	V_{DD2}	-464.0	-7138.6	100:60

Table 3–1. Pad Coordinate (2/4)

No.	Pad Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
111	V_{DD2}	-464.0	-7218.6	100:60
112	V_{DD2}	-464.0	-7298.6	100:60
113	V_{DD2}	-464.0	-7378.6	100:60
114	V_{DD2}	-464.0	-7458.6	100:60
115	V_{DD2}	-464.0	-7538.6	100:60
116	RMON2	-464.0	-7842.0	100:60
117	RMON2	-464.0	-8014.2	100:60
118	Dummy2	-464.0	-8451.0	100:60
119	V_{SS2}	-399.8	-8769.0	60□ 100
120	V_{SS2}	-319.8	-8769.0	60□ 100
121	V_{SS2}	-239.8	-8769.0	60□ 100
122	V_{SS2}	-159.8	-8769.0	60□ 100
123	V_{SS2}	-79.8	-8769.0	60□ 100
124	V_{SS2}	0.2	-8769.0	60□ 100
125	V_{SS2}	80.2	-8769.0	60□ 100
126	V_{SS2}	160.2	-8769.0	60□ 100
127	V_{SS2}	240.2	-8769.0	60□ 100
128	V_{SS2}	320.2	-8769.0	60□ 100
129	Dummy3	402.0	-8642.5	80:37
130	S_1	402.0	-8585.5	80:37
131	S_2	402.0	-8528.5	80:37
132	S_3	402.0	-8471.5	80:37
133	S_4	402.0	-8414.5	80:37
134	S_5	402.0	-8357.5	80:37
135	S_6	402.0	-8300.5	80:37
136	S_7	402.0	-8243.5	80:37
137	S_8	402.0	-8186.5	80:37
138	S_9	402.0	-8129.5	80:37
139	S_{10}	402.0	-8072.5	80:37
140	S_{11}	402.0	-8015.5	80:37
141	S_{12}	402.0	-7958.5	80:37
142	S_{13}	402.0	-7901.5	80:37
143	S_{14}	402.0	-7844.5	80:37
144	S_{15}	402.0	-7787.5	80:37
145	S_{16}	402.0	-7730.5	80:37
146	S_{17}	402.0	-7673.5	80:37
147	S_{18}	402.0	-7616.5	80:37
148	S_{19}	402.0	-7559.5	80:37
149	S_{20}	402.0	-7502.5	80:37
150	S_{21}	402.0	-7445.5	80:37
151	S_{22}	402.0	-7388.5	80:37
152	S_{23}	402.0	-7331.5	80:37
153	S_{24}	402.0	-7274.5	80:37
154	S_{25}	402.0	-7217.5	80:37
155	S_{26}	402.0	-7160.5	80:37
156	S_{27}	402.0	-7103.5	80:37
157	S_{28}	402.0	-7046.5	80:37
158	S_{29}	402.0	-6989.5	80:37
159	S_{30}	402.0	-6932.5	80:37
160	S_{31}	402.0	-6875.5	80:37
161	S_{32}	402.0	-6818.5	80:37
162	S_{33}	402.0	-6761.5	80:37
163	S_{34}	402.0	-6704.5	80:37
164	S_{35}	402.0	-6647.5	80:37
165	S_{36}	402.0	-6590.5	80:37
166	S_{37}	402.0	-6533.5	80:37
167	S_{38}	402.0	-6476.5	80:37
168	S_{39}	402.0	-6419.5	80:37
169	S_{40}	402.0	-6362.5	80:37
170	S_{41}	402.0	-6305.5	80:37
171	S_{42}	402.0	-6248.5	80:37
172	S_{43}	402.0	-6191.5	80:37
173	S_{44}	402.0	-6134.5	80:37
174	S_{45}	402.0	-6077.5	80:37
175	S_{46}	402.0	-6020.5	80:37
176	S_{47}	402.0	-5963.5	80:37
177	S_{48}	402.0	-5906.5	80:37
178	S_{49}	402.0	-5849.5	80:37
179	S_{50}	402.0	-5792.5	80:37
180	S_{51}	402.0	-5735.5	80:37
181	S_{52}	402.0	-5678.5	80:37
182	S_{53}	402.0	-5621.5	80:37
183	S_{54}	402.0	-5564.5	80:37
184	S_{55}	402.0	-5507.5	80:37
185	S_{56}	402.0	-5450.5	80:37
186	S_{57}	402.0	-5393.5	80:37
187	S_{58}	402.0	-5336.5	80:37
188	S_{59}	402.0	-5279.5	80:37
189	S_{60}	402.0	-5222.5	80:37
190	S_{61}	402.0	-5165.5	80:37
191	S_{62}	402.0	-5108.5	80:37
192	S_{63}	402.0	-5051.5	80:37
193	S_{64}	402.0	-4994.5	80:37
194	S_{65}	402.0	-4937.5	80:37
195	S_{66}	402.0	-4880.5	80:37
196	S_{67}	402.0	-4823.5	80:37
197	S_{68}	402.0	-4766.5	80:37
198	S_{69}	402.0	-4709.5	80:37
199	S_{70}	402.0	-4652.5	80:37
200	S_{71}	402.0	-4595.5	80:37
201	S_{72}	402.0	-4538.5	80:37
202	S_{73}	402.0	-4481.5	80:37
203	S_{74}	402.0	-4424.5	80:37
204	S_{75}	402.0	-4367.5	80:37
205	S_{76}	402.0	-4310.5	80:37
206	S_{77}	402.0	-4253.5	80:37
207	S_{78}	402.0	-4196.5	80:37
208	S_{79}	402.0	-4139.5	80:37
209	S_{80}	402.0	-4082.5	80:37
210	S_{81}	402.0	-4025.5	80:37
211	S_{82}	402.0	-3968.5	80:37
212	S_{83}	402.0	-3911.5	80:37
213	S_{84}	402.0	-3854.5	80:37
214	S_{85}	402.0	-3797.5	80:37
215	S_{86}	402.0	-3740.5	80:37
216	S_{87}	402.0	-3683.5	80:37
217	S_{88}	402.0	-3626.5	80:37
218	S_{89}	402.0	-3569.5	80:37
219	S_{90}	402.0	-3512.5	80:37
220	S_{91}	402.0	-3455.5	80:37

Table 3–1. Pad Coordinate (3/4)

No.	Pad Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
221	S_{92}	402.0	-3398.5	80:37
222	S_{93}	402.0	-3341.5	80:37
223	S_{94}	402.0	-3284.5	80:37
224	S_{95}	402.0	-3227.5	80:37
225	S_{96}	402.0	-3170.5	80:37
226	S_{97}	402.0	-3113.5	80:37
227	S_{98}	402.0	-3056.5	80:37
228	S_{99}	402.0	-2999.5	80:37
229	S_{100}	402.0	-2942.5	80:37
230	S_{101}	402.0	-2885.5	80:37
231	S_{102}	402.0	-2828.5	80:37
232	S_{103}	402.0	-2771.5	80:37
233	S_{104}	402.0	-2714.5	80:37
234	S_{105}	402.0	-2657.5	80:37
235	S_{106}	402.0	-2600.5	80:37
236	S_{107}	402.0	-2543.5	80:37
237	S_{108}	402.0	-2486.5	80:37
238	S_{109}	402.0	-2429.5	80:37
239	S_{110}	402.0	-2372.5	80:37
240	S_{111}	402.0	-2315.5	80:37
241	S_{112}	402.0	-2285.5	80:37
242	S_{113}	402.0	-2201.5	80:37
243	S_{114}	402.0	-2144.5	80:37
244	S_{115}	402.0	-2087.5	80:37
245	S_{116}	402.0	-2030.5	80:37
246	S_{117}	402.0	-1973.5	80:37
247	S_{118}	402.0	-1916.5	80:37
248	S_{119}	402.0	-1859.5	80:37
249	S_{120}	402.0	-1802.5	80:37
250	S_{121}	402.0	-1745.5	80:37
251	S_{122}	402.0	-1688.5	80:37
252	S_{123}	402.0	-1631.5	80:37
253	S_{124}	402.0	-1574.5	80:37
254	S_{125}	402.0	-1517.5	80:37
255	S_{126}	402.0	-1460.5	80:37
256	S_{127}	402.0	-1403.5	80:37
257	S_{128}	402.0	-1346.5	80:37
258	S_{129}	402.0	-1289.5	80:37
259	S_{130}	402.0	-1232.5	80:37
260	S_{131}	402.0	-1175.5	80:37
261	S_{132}	402.0	-1118.5	80:37
262	S_{133}	402.0	-1061.5	80:37
263	S_{134}	402.0	-1004.5	80:37
264	S_{135}	402.0	-947.5	80:37
265	S_{136}	402.0	-890.5	80:37
266	S_{137}	402.0	-833.5	80:37
267	S_{138}	402.0	-776.5	80:37
268	S_{139}	402.0	-719.5	80:37
269	S_{140}	402.0	-662.5	80:37
270	S_{141}	402.0	-605.5	80:37
271	S_{142}	402.0	-548.5	80:37
272	S_{143}	402.0	-491.5	80:37
273	S_{144}	402.0	-434.5	80:37
274	S_{145}	402.0	-377.5	80:37
275	S_{146}	402.0	-320.5	80:37

No.	Pad Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
276	S_{147}	402.0	-263.5	80:37
277	S_{148}	402.0	-206.5	80:37
278	S_{149}	402.0	-149.5	80:37
279	S_{150}	402.0	-92.5	80:37
280	S_{151}	402.0	-35.5	80:37
281	S_{152}	402.0	21.5	80:37
282	S_{153}	402.0	78.5	80:37
283	S_{154}	402.0	135.5	80:37
284	S_{155}	402.0	192.5	80:37
285	S_{156}	402.0	249.5	80:37
286	S_{157}	402.0	306.5	80:37
287	S_{158}	402.0	363.5	80:37
288	S_{159}	402.0	420.5	80:37
289	S_{160}	402.0	477.5	80:37
290	S_{161}	402.0	534.5	80:37
291	S_{162}	402.0	591.5	80:37
292	S_{163}	402.0	648.5	80:37
293	S_{164}	402.0	705.5	80:37
294	S_{165}	402.0	762.5	80:37
295	S_{166}	402.0	819.5	80:37
296	S_{167}	402.0	876.5	80:37
297	S_{168}	402.0	933.5	80:37
298	S_{169}	402.0	990.5	80:37
299	S_{170}	402.0	1047.5	80:37
300	S_{171}	402.0	1104.5	80:37
301	S_{172}	402.0	1161.5	80:37
302	S_{173}	402.0	1218.5	80:37
303	S_{174}	402.0	1275.5	80:37
304	S_{175}	402.0	1332.5	80:37
305	S_{176}	402.0	1389.5	80:37
306	S_{177}	402.0	1446.5	80:37
307	S_{178}	402.0	1503.5	80:37
308	S_{179}	402.0	1560.5	80:37
309	S_{180}	402.0	1617.5	80:37
310	S_{181}	402.0	1674.5	80:37
311	S_{182}	402.0	1731.5	80:37
312	S_{183}	402.0	1788.5	80:37
313	S_{184}	402.0	1845.5	80:37
314	S_{185}	402.0	1902.5	80:37
315	S_{186}	402.0	1959.5	80:37
316	S_{187}	402.0	2016.5	80:37
317	S_{188}	402.0	2073.5	80:37
318	S_{189}	402.0	2130.5	80:37
319	S_{190}	402.0	2187.5	80:37
320	S_{191}	402.0	2244.5	80:37
321	S_{192}	402.0	2301.5	80:37
322	S_{193}	402.0	2358.5	80:37
323	S_{194}	402.0	2415.5	80:37
324	S_{195}	402.0	2472.5	80:37
325	S_{196}	402.0	2529.5	80:37
326	S_{197}	402.0	2586.5	80:37
327	S_{198}	402.0	2643.5	80:37
328	S_{199}	402.0	2700.5	80:37
329	S_{200}	402.0	2757.5	80:37
330	S_{201}	402.0	2814.5	80:37

Table 3–1. Pad Coordinate (4/4)

No.	Pad Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
331	S_{202}	402.0	2871.5	80:37
332	S_{203}	402.0	2928.5	80:37
333	S_{204}	402.0	2985.5	80:37
334	S_{205}	402.0	3042.5	80:37
335	S_{206}	402.0	3099.5	80:37
336	S_{207}	402.0	3156.5	80:37
337	S_{208}	402.0	3213.5	80:37
338	S_{209}	402.0	3270.5	80:37
339	S_{210}	402.0	3327.5	80:37
340	S_{211}	402.0	3384.5	80:37
341	S_{212}	402.0	3441.5	80:37
342	S_{213}	402.0	3498.5	80:37
343	S_{214}	402.0	3555.5	80:37
344	S_{215}	402.0	3612.5	80:37
345	S_{216}	402.0	3669.5	80:37
346	S_{217}	402.0	3726.5	80:37
347	S_{218}	402.0	3783.5	80:37
348	S_{219}	402.0	3840.5	80:37
349	S_{220}	402.0	3897.5	80:37
350	S_{221}	402.0	3954.5	80:37
351	S_{222}	402.0	4011.5	80:37
352	S_{223}	402.0	4068.5	80:37
353	S_{224}	402.0	4125.5	80:37
354	S_{225}	402.0	4128.5	80:37
355	S_{226}	402.0	4239.5	80:37
356	S_{227}	402.0	4296.5	80:37
357	S_{228}	402.0	4353.5	80:37
358	S_{229}	402.0	4410.5	80:37
359	S_{230}	402.0	4467.5	80:37
360	S_{231}	402.0	4524.5	80:37
361	S_{232}	402.0	4581.5	80:37
362	S_{233}	402.0	4638.5	80:37
363	S_{234}	402.0	4695.5	80:37
364	S_{235}	402.0	4752.5	80:37
365	S_{236}	402.0	4809.5	80:37
366	S_{237}	402.0	4866.5	80:37
367	S_{238}	402.0	4923.5	80:37
368	S_{239}	402.0	4980.5	80:37
369	S_{240}	402.0	5037.5	80:37
370	S_{241}	402.0	5094.5	80:37
371	S_{242}	402.0	5151.5	80:37
372	S_{243}	402.0	5208.5	80:37
373	S_{244}	402.0	5265.5	80:37
374	S_{245}	402.0	5322.5	80:37
375	S_{246}	402.0	5379.5	80:37
376	S_{247}	402.0	5436.5	80:37
377	S_{248}	402.0	5493.5	80:37
378	S_{249}	402.0	5550.5	80:37
379	S_{250}	402.0	5607.5	80:37
380	S_{251}	402.0	5664.5	80:37
381	S_{252}	402.0	5721.5	80:37
382	S_{253}	402.0	5778.5	80:37
383	S_{254}	402.0	5835.5	80:37
384	S_{255}	402.0	5892.5	80:37
385	S_{256}	402.0	5949.5	80:37
386	S_{257}	402.0	6006.5	80:37
387	S_{258}	402.0	6063.5	80:37
388	S_{259}	402.0	6120.5	80:37
389	S_{260}	402.0	6177.5	80:37
390	S_{261}	402.0	6234.5	80:37
391	S_{262}	402.0	6291.5	80:37
392	S_{263}	402.0	6348.5	80:37
393	S_{264}	402.0	6405.5	80:37
394	S_{265}	402.0	6462.5	80:37
395	S_{266}	402.0	6519.5	80:37
396	S_{267}	402.0	6576.5	80:37
397	S_{268}	402.0	6633.5	80:37
398	S_{269}	402.0	6690.5	80:37
399	S_{270}	402.0	6747.5	80:37
400	S_{271}	402.0	6804.5	80:37
401	S_{272}	402.0	6861.5	80:37
402	S_{273}	402.0	6918.5	80:37
403	S_{274}	402.0	6975.5	80:37
404	S_{275}	402.0	7032.5	80:37
405	S_{276}	402.0	7089.5	80:37
406	S_{277}	402.0	7146.5	80:37
407	S_{278}	402.0	7203.5	80:37
408	S_{279}	402.0	7260.5	80:37
409	S_{280}	402.0	7317.5	80:37
410	S_{281}	402.0	7374.5	80:37
411	S_{282}	402.0	7431.5	80:37
412	S_{283}	402.0	7488.5	80:37
413	S_{284}	402.0	7545.5	80:37
414	S_{285}	402.0	7602.5	80:37
415	S_{286}	402.0	7659.5	80:37
416	S_{287}	402.0	7716.5	80:37
417	S_{288}	402.0	7773.5	80:37
418	S_{289}	402.0	7830.5	80:37
419	S_{290}	402.0	7887.5	80:37
420	S_{291}	402.0	7944.5	80:37
421	S_{292}	402.0	8001.5	80:37
422	S_{293}	402.0	8058.5	80:37
423	S_{294}	402.0	8115.5	80:37
424	S_{295}	402.0	8172.5	80:37
425	S_{296}	402.0	8229.5	80:37
426	S_{297}	402.0	8286.5	80:37
427	S_{298}	402.0	8343.5	80:37
428	S_{299}	402.0	8400.5	80:37
429	S_{300}	402.0	8457.5	80:37
430	Dummy4	402.0	8514.5	80:37
431	V_{SS2}	320.2	8769.0	60:100
432	V_{SS2}	240.2	8769.0	60:100
433	V_{SS2}	160.2	8769.0	60:100
434	V_{SS2}	80.2	8769.0	60:100
435	V_{SS2}	0.2	8769.0	60:100
436	V_{SS2}	-79.8	8769.0	60:100
437	V_{SS2}	-159.8	8769.0	60:100
438	V_{SS2}	-239.8	8769.0	60:100
439	V_{SS2}	-319.8	8769.0	60:100
440	V_{SS2}	-399.8	8769.0	60:100
441	Alignment mark	429.2	8779.8	
442	Alignment mark	429.2	-8779.8	

Bump specs (standard reference value)

Parameter	Specifications
Bump size tolerance	±5 μm
Bump height (design center value)	17 μm
Bump height tolerance (within lot)	±4 μm
Bump height tolerance (within chip)	Range: 3 μm
Bump hardness	50 ± 20 Hv

★ 4. PIN FUNCTIONS

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Pad No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>C1 to C3</td><td>Video signal</td><td>30, 47</td><td>Input</td><td>Input R, G, and B video signals.</td></tr>
<tr><td>S_1 to S_{300}</td><td>Video signal</td><td>130 to 429</td><td>Output</td><td>Video signal output pins. Video signals which are sampled and held, are output to these pins during horizontal period.</td></tr>
<tr><td>STHR,
STHL</td><td>Cascade</td><td>81 to 86,
48 to 53</td><td>I/O</td><td>Start pulse I/O pins of sample hold timing.
In the case of right shift, STHR becomes an input pin and STHL becomes an output pin.
In the case of left shift, STHL becomes an input pin and STHR becomes an output pin.</td></tr>
<tr><td>CLI1 to
CLI3</td><td>Shift clock</td><td>69 to 77</td><td>Input</td><td>A start pulse is read at the rising edge of CLI1. Sampling pulse SHPn is generated at the rising edge of CLI1 to CLI3 in the sequential sampling mode, and at the rising edge of CLI1 in the simultaneous sampling mode (for details, refer to 5.1.5 Relation between Shift Clock CLIn and Internal Sampling Pulse SHPn).</td></tr>
<tr><td>INH</td><td>Inhibit</td><td>66 to 68</td><td>Input</td><td>At the falling edge of INH, it is done that the change of Multiplexer circuits and the conversion of 2 sets of Sample and Hold circuits.</td></tr>
<tr><td>RESET</td><td>Reset</td><td>63 to 65</td><td>Input</td><td>Resets the select counter of the multiplexer and the selector circuit of the two sample and hold circuits during RESET=H. After reset, the multiplexer is turned OFF, so sure to input one pulse of the INH signal before inputting the video signal. If the video signal is input without the INH signal, sampling is not executed.</td></tr>
<tr><td>MP/TH</td><td>Multiplexer circuit select (1)</td><td>54 to 56</td><td>Input</td><td rowspan="2">In the combination of MP/TH and MP/1.5, it can support to the following modes.
<table>
<tr><th>Mode</th><th>MP/TH</th><th>MP/1.5</th></tr>
<tr><td>Vertical stripe array (Simultaneous sampling)</td><td>L</td><td>L</td></tr>
<tr><td>Vertical stripe array (Sequential sampling)</td><td>L</td><td>H</td></tr>
<tr><td>Mosaic array</td><td>H</td><td>L</td></tr>
<tr><td>Double-side delta array</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>MP/1.5</td><td>Multiplexer circuit select (2)</td><td>57 to 59</td><td>Input</td></tr>
<tr><td>R,/L</td><td>Shift direction select</td><td>60 to 62</td><td>Input</td><td>R,/L = H: Right shift: STHR → S_1 → S_{300} → STHL
R,/L = L: Left shift: STHL → S_{300} → S_1 → STHR</td></tr>
<tr><td>Osel</td><td>Selection of number of outputs switching</td><td>87 to 89</td><td>Input</td><td>Selects number of outputs.
O_{sel} = L: 288 output mode
O_{sel} = H: 300 output mode
Output pins S_{145} to S_{156} are invalid in 288 output mode. When Osel=L, the output signals of S145 to S156 become same as S_{157} to S_{168} (R,/L = H) or S_{133} to S_{144} (R,/L = L).</td></tr>
<tr><td>RMON1,
RMON2</td><td>Monitor</td><td>2, 3, 116, 117</td><td>–</td><td>This pin can measure the connection resistance at the time of COG mounting.
RMON1 and RMON2 are each short inside IC.
It does not connect with other pins inside IC.</td></tr>
<tr><td>Dummy1 to Dummy4</td><td>Dummy</td><td>1, 118,
129, 430</td><td>–</td><td>No dummy pins are connected with other pins inside IC.</td></tr>
<tr><td>V_{DD1}</td><td>Logic power supply</td><td>23 to 29,
90 to 96</td><td>–</td><td>3.0 to 5.5 V</td></tr>
<tr><td>V_{DD2}</td><td>Driver power supply</td><td>4 to 15,
104 to 115</td><td>–</td><td>5.0 ± 0.5 V</td></tr>
<tr><td>V_{SS1}</td><td>Logic ground</td><td>16 to 22,
97 to 103</td><td>–</td><td>Connect this pin to ground of system.</td></tr>
<tr><td>V_{SS2}</td><td>Driver ground</td><td>119 to 128,
431 to 440</td><td>–</td><td>Connect this pin to ground of system.</td></tr>
<tr><td>TEST</td><td>Test</td><td>78 to 80</td><td>–</td><td>Fix this pin to low level.</td></tr>
</table>

5. FUNCTIONAL DESCRIPTION

5.1 Multiplexer Circuit

This circuit selects RGB video signals input to the C1 to C3 pins according to the pixel array of the liquid crystal panel, and outputs the signals to the S_1 ~ S_{300} pins.

Vertical stripe array(Simultaneous sampling/Sequential sampling), double-side delta array (Sequential sampling), or mosaic array (Sequential sampling) can be selected by using the MP/TH and MP/1.5 pins.

5.1.1 Vertical stripe array mode (Simultaneous sampling) (MP/TH = L, MP/1.5 = L)

In this mode, the relation between video signals C1 to C3, and output pins is as shown below. This mode is used to drive a panel of vertical stripe array. In this mode, the multiplexer circuit is in the through status.

Please input the shift clock only to CL1 pin, and fix CL2 and CL3 pin to low level.

Refer to **5.1.5 Relation between Shift Clock CLIn and Internal Sampling Pulse SHPn**.

Table 5–1. Relation between Video Signals C1 to C3, and Output Pins (during right shift)

Line No. (number of INHs)	RESET	INH	S_1 (S_{300})	S_2 (S_{299})	S_3 (S_{298})	S_4 (S_{297})	...	S_{299} (S_2)	S_{300} (S_1)
0	H	L	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
1	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–1. Pixel Arrangement of Vertical Stripe Array and Multiplexer Operation

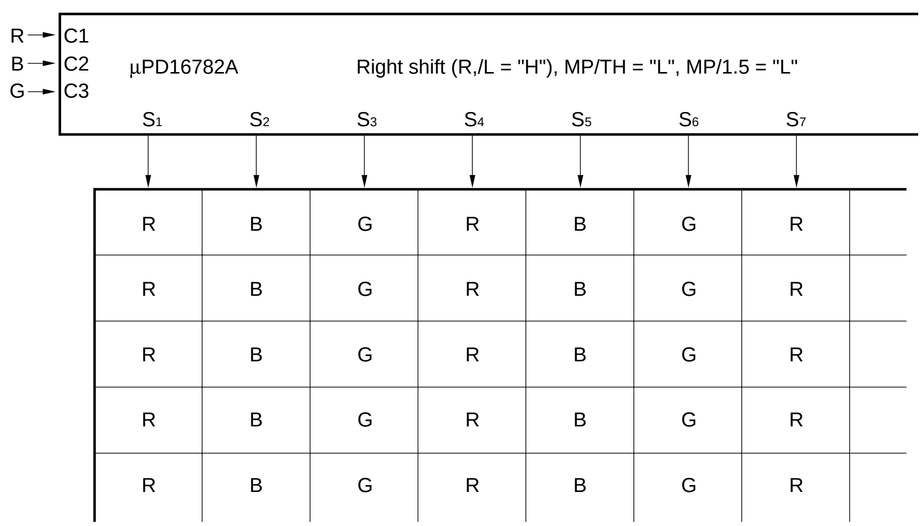
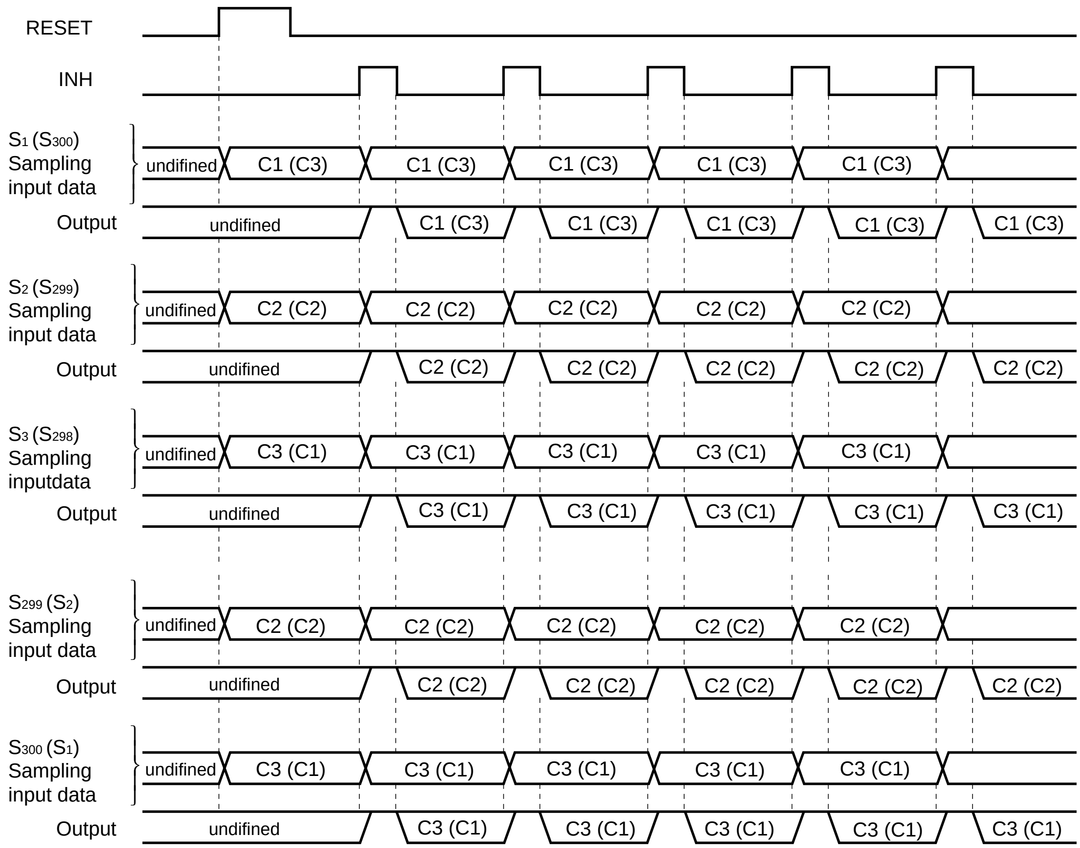


Figure 5–2. Timing Chart of Vertical Stripe Array



5.1.2 Vertical stripe array mode (sequential sampling) (MP/TH = L, MP/1.5 = H)

Please input the shift clock to CL1, CL2 and CL3 pin.

Refer to **5.1.5 Relation between Shift Clock CLIn and Internal Sampling Pulse SHPn**.

Table 5–2. Relation between Video Signals C1 to C3, and Output Pins (during right shift)

Line No. (number of INHs)	RESET	INH	S_1 (S_{300})	S_2 (S_{299})	S_3 (S_{298})	S_4 (S_{297})	...	S_{299} (S_2)	S_{300} (S_1)
0	H	L	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
1	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–3. Pixel Arrangement of Vertical Stripe Array and Multiplexer Operation

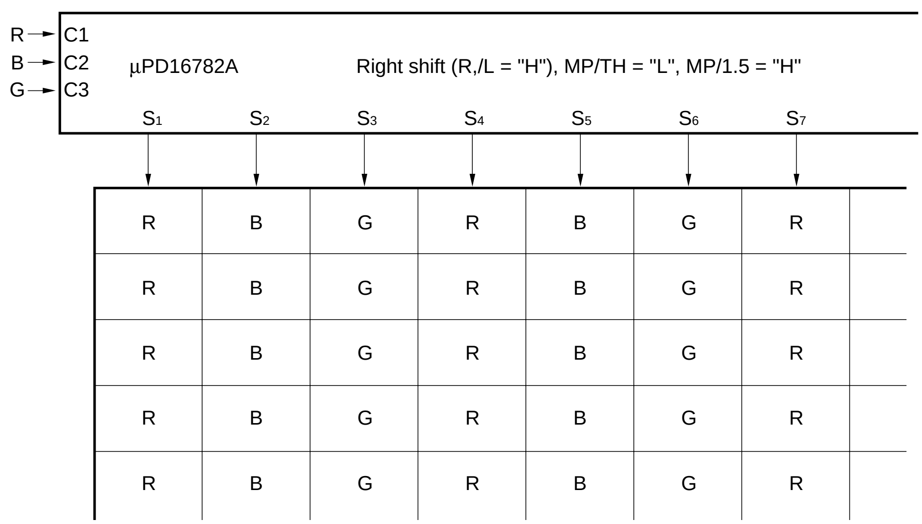
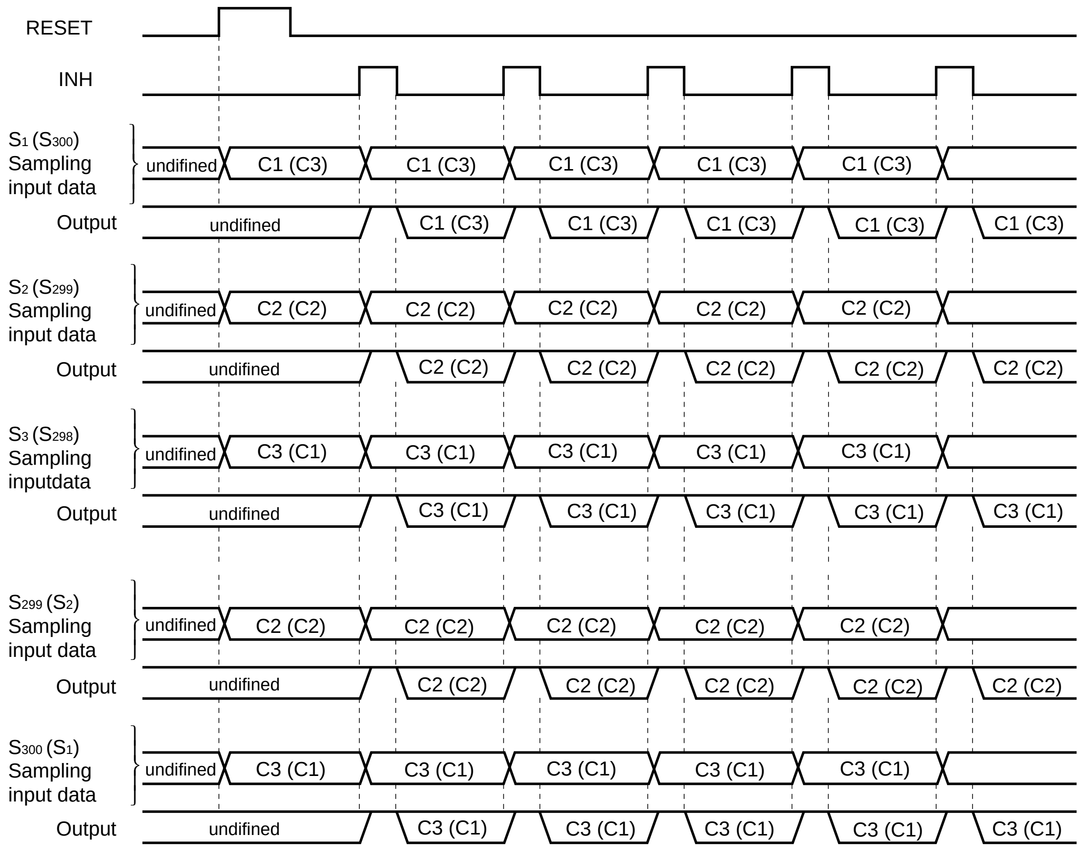


Figure 5–4. Timing Chart of Vertical Stripe Array



5.1.3 Double-side delta array mode (MP/TH = H, MP/1.5 = H)

Table 5–3. Relation between Video Signals C1 to C3 and Output Pins

Line No. (number of INHs)	RESET	INH	S_1 (S_{300})	S_2 (S_{299})	S_3 (S_{298})	S_4 (S_{297})	...	S_{299} (S_2)	S_{300} (S_1)
0	H	L	Undefined	Undefined	Undefined	Undefined	...	Undefined	Undefined
1	L	↓	Sampling C2 (C3)	Sampling C3 (C2)	Sampling C1 (C1)	Sampling C2 (C3)	...	Sampling C3 (C2)	Sampling C1 (C1)
2	L	↓	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	Output C2 (C3)	...	Output C3 (C2)	Output C1 (C1)
3	L	↓	Output C1 (C1)	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	...	Output C2 (C3)	Output C3 (C2)
4	L	↓	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	Output C2 (C3)	...	Output C3 (C2)	Output C1 (C1)
5	L	↓	Output C1 (C1)	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	...	Output C2 (C3)	Output C3 (C2)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–5. Pixel Arrangement of Double-Side Delta Array and Multiplexer Operation

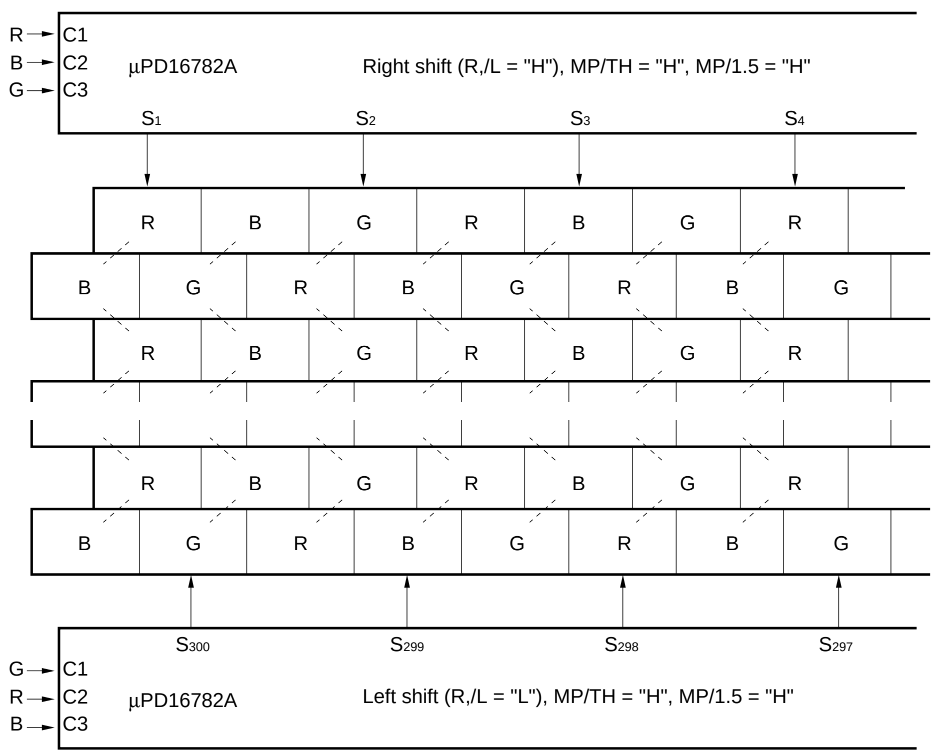
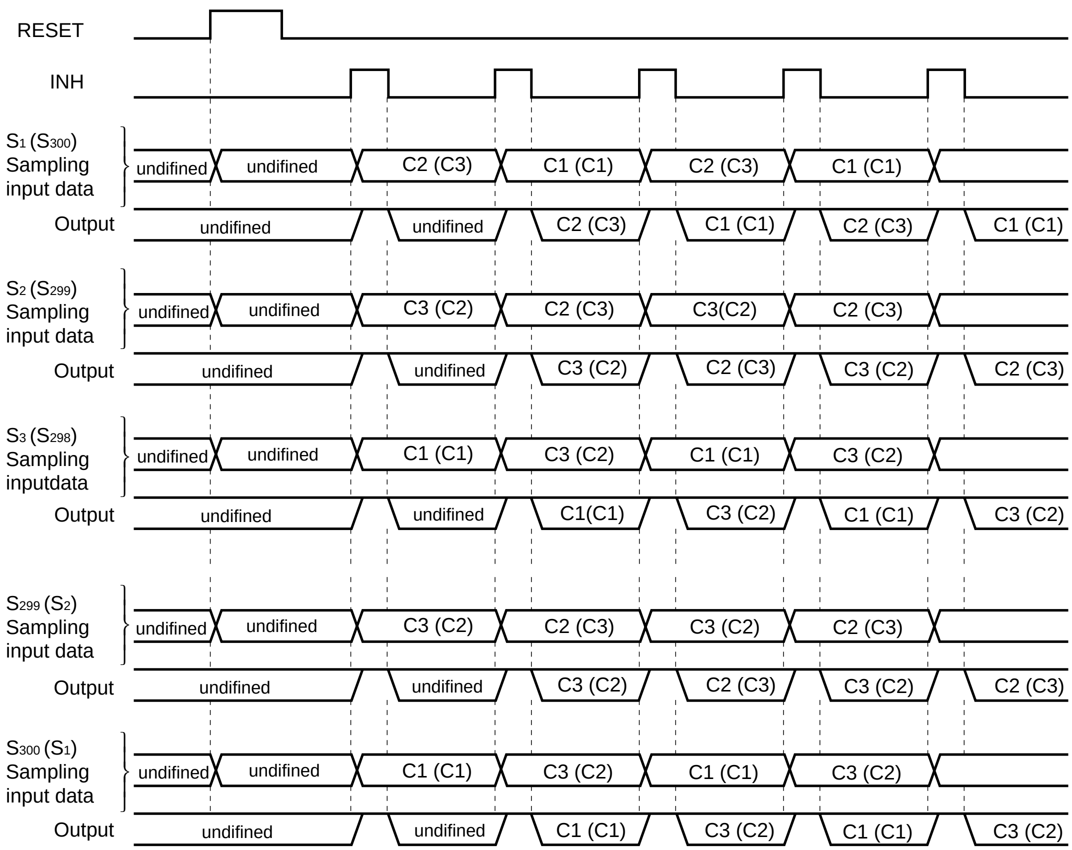


Figure 5–6. Timing Chart of Both-Sides Delta Array



5.1.4 Mosaic array mode (MP/TH = H, MP/1.5 = L)

Table 5–4. Relation between Video Signals C1 to C3, and Output Pins

Line No. (number of INHs)	RESET	INH	S_1 (S_{300})	S_2 (S_{299})	S_3 (S_{298})	S_4 (S_{297})	...	S_{299} (S_2)	S_{300} (S_1)
0	H	L	Undefined	Undefined	Undefined	Undefined	...	Undefined	Undefined
1	L	↓	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C3 (C2)	Output C1 (C1)	Output C2 (C3)	Output C3 (C2)	...	Output C1 (C1)	Output C2 (C3)
4	L	↓	Output C2 (C1)	Output C3 (C3)	Output C1 (C2)	Output C2 (C1)	...	Output C3 (C3)	Output C1 (C2)
5	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–7. Pixel Arrangement of Mosaic Array and Multiplexer Operation

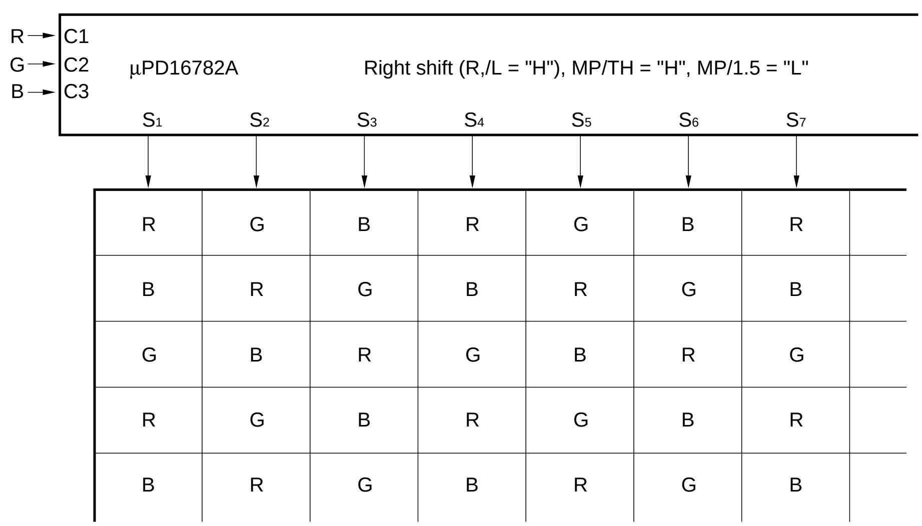
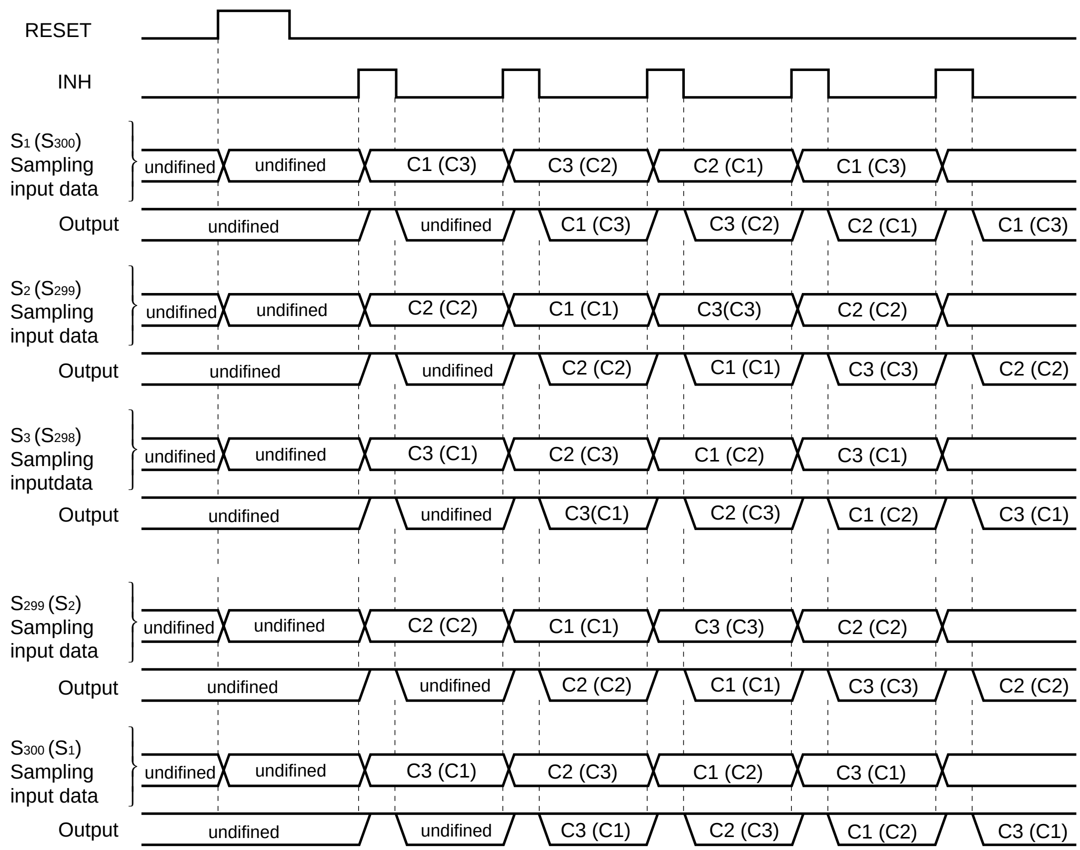
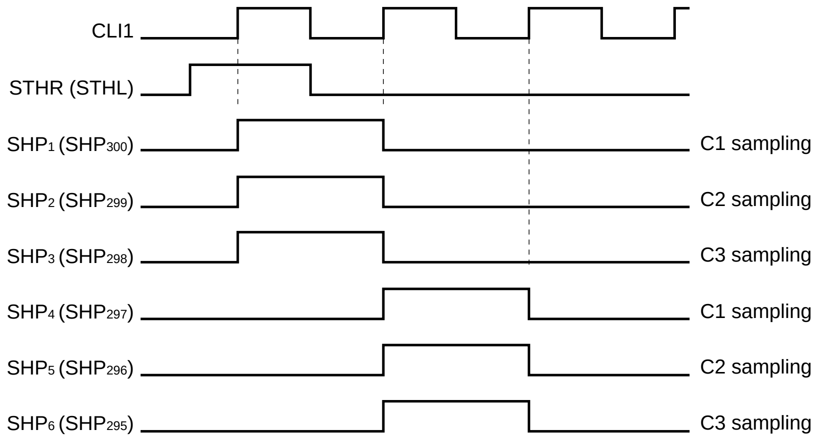


Figure 5–8. Timing Chart of Mosaic Array



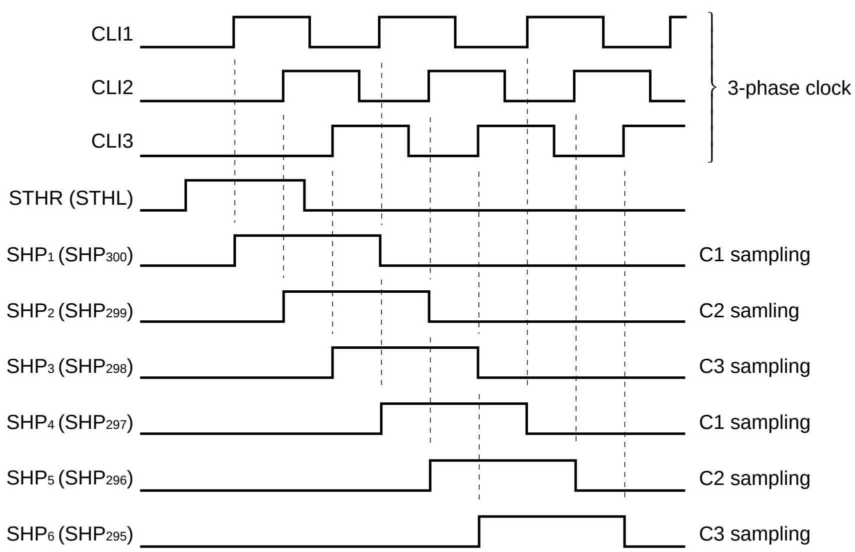
5.1.5 Relation between Shift Clock CLIn and Internal Sampling Pulse SHPn

(1) Simultaneous sampling (( ) indicates the case of left shift.)



Remark C1 through C3 are sampled while SHPn is high level.

(2) Sequential sampling (( ) indicates the case of left shift.)

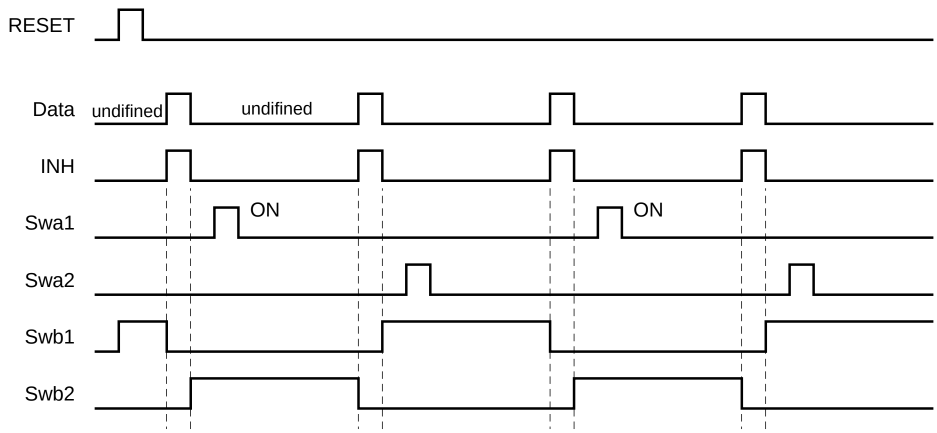


Remarks 1. Input a three-phase clock to shift clock pins CLI1 to CLI3.

2. The video signals (C1 to C3) are sampled while SHPn is high level.

5.2 Sample and Hold Circuit

The sample and hold circuit samples and holds the video signals input to C1 ~ C3 selected by the multiplexer circuit in the timing shown below. Swa1 to Swb2 are reset by the RESET signal and change at the rising and falling edges of the INH signal.



5.3 Output Operation Timing

The sampled video signals are output to the LCD panel by output currents I_{VOL} and I_{VOH} via output buffer.

And be sure to input 5 or more CLKs of CLI1 during INH=H period.

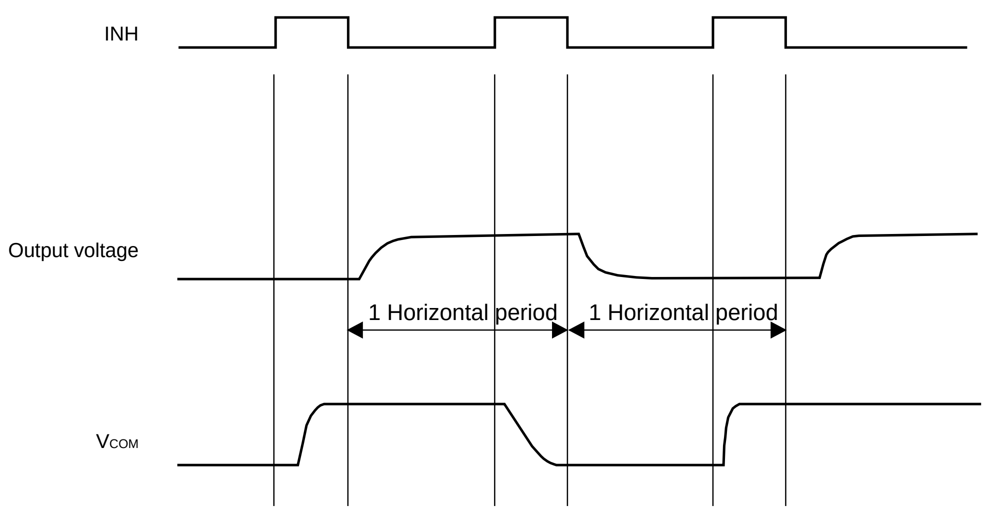
The output operation of this IC is controlled by INH signals.

INH = Hi-Z

INH = Connected with internal circuit (switch sample and hold circuit at the falling edge.)

Therefore, inverting V_{COM} while INH = L causes current flow to the IC output pins, which may result wrong working. V_{COM} Inversion should be done during INH = H (Hi-Z) and output operation to the LCD should be done after the V_{COM} becomes stable enough.

Be sure to sufficiently evaluate the picture quality.



Cautions 1. In order to prevent destruction due to latch-up, keep the power-on sequence [V_{DD1} → logic input → V_{DD2} → video signal input] and power-off in the reverse sequence. Observe this power sequence even during the transition period.

2. The μPD16782A is designed to input successive signals such as chrome signals. The input band of the video signals is designed to be 9 MHz MAX. If video signals faster than that are input, display is not performed correctly.

3. Insert a bypass capacitor of 0.1 μF between V_{DD1} and V_{SS1} and between V_{DD2} and V_{SS2}. If the power supply is not reinforced, the sampling voltage may be abnormal if the supply voltage fluctuates.

4. Even if the start pulse width is extended by half a clock or more, sampling start timing SHP_1 is not affected, and the sampling operation is performed normally.

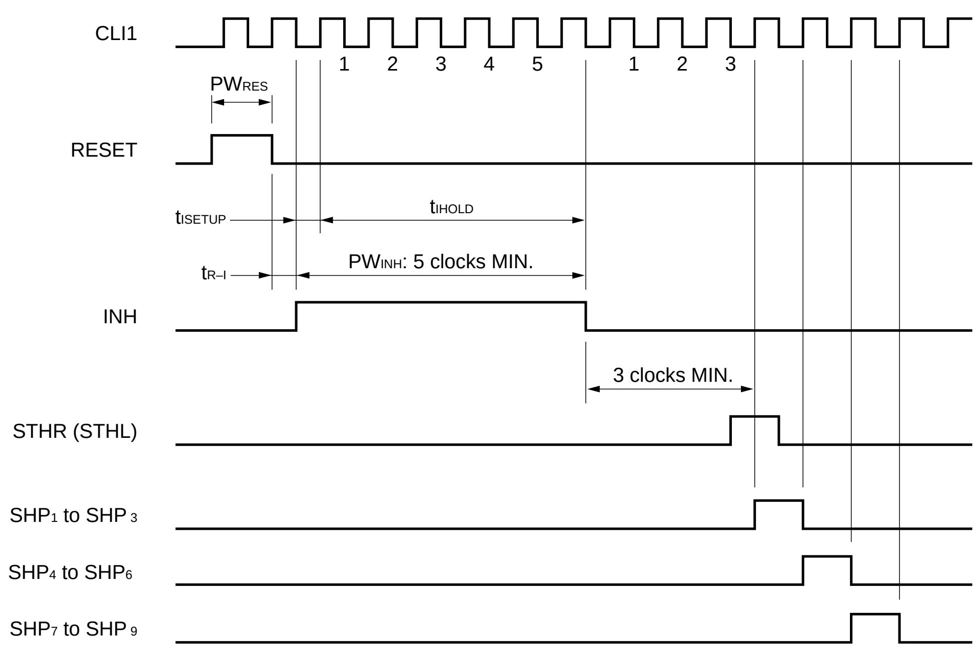
5. To reset the IC after power-on, the below timing sequence should be kept. (The following timing charts show simultaneous sampling.)

If RESET signal is input 1 time after power-on , it is not required after that. Besides, please be sure to input INH signal after RESET signal input.

RESET pulse width: 66 ns MIN.

t_{R-1}: 81 ns MIN.

INH pulse width: 5 CLK MIN. (CLI1 is active)



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = 0 V)

Parameter	Symbol	Condition	Ratings	Unit
Logic supply voltage	V_{DD1}		–0.5 to +6.0	V
Driver supply voltage	V_{DD2}		–0.5 to +6.0	V
Logic input voltage	V_I		–0.5 to V_{DD1} +0.5	V
Video input voltage	V_{VI}	C1 to C3	–0.5 to V_{DD2} +0.5	V
Logic output voltage	V_{01}		–0.5 to V_{DD1} +0.5	V
Driver output voltage	V_{02}		–0.5 to V_{DD2} +0.5	V
Driver output current	I_{O2}		±10	mA
Operating ambient temperature	T_A		–30 to +85	°C
Storage temperature	T_{stg}		–65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –30 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}		3.0	3.3	5.5	V
Driver supply voltage	V_{DD2}		4.5	5.0	5.5	V
Video input voltage	V_{VI}		V_{SS2} + 0.2		V_{DD2} – 0.2	V
Driver output voltage	V_{02}		V_{SS2} + 0.2		V_{DD2} – 0.2	V
High level Input voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low level Input voltage	V_{IL}		0		0.3 V_{DD1}	V

Electrical Characteristics (T_A = –30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

	Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
	Maximum video signal output voltage	V_{VOH}			V_{DD2} – 0.2			V
	Minimum video signal output voltage	V_{VOL}					0.2	V
	Logic high level output voltage	V_{LOH}	STHL, STHR pins, I_{OH} = –1.0 mA		0.9 V_{DD1}			V
	Logic low level output voltage	V_{LOL}	STHL, STHR pins, I_{OL} = 1.0 mA				0.1 V_{DD1}	V
	Video signal high level output current	I_{VOH}	INH = L, V_{OF} = V_{DD2} – 1.0 V, V_O = V_{DD2} – 0.5 V			–0.20	–0.08	mA
	Video signal low level output current	I_{VOL}	INH = L, V_{OF} = 1.0 V, V_O = 0.5 V		0.08	0.20		mA
	Reference voltage 1	V_{REF1}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 0.5 V			0.49		V
	Reference voltage 2	V_{REF2}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 2.0 V			1.99		V
	Reference voltage 3	V_{REF3}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 3.5 V			3.49		V
★	Output voltage deviation 1	ΔV_{VO1}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 0.5 V				±30	mV
★	Output voltage deviation 2	ΔV_{VO2}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 2.0 V				±30	mV
★	Output voltage deviation 3	ΔV_{VO3}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 3.5 V				±30	mV
	Logic input leakage current	I_{LL}	Logic input except Osel				±1.0	μA
			O_{sel}, V_I = V_{DD} = 3.3 V			90		μA
	Video input leakage current	I_{VL}					±10	μA
	Logic dynamic current consumption	I_{DD1}	f_{CLI} = 14 MHz, V_{VI} = 2.0 V, no load, f_{INH} = 15.4 kHz, PW_{INH} = 5.0 μs	V_{DD1} = 3.3 ± 0.3 V			3	mA
				V_{DD1} = 5.0 ± 0.5 V			4.5	mA
	Driver dynamic current consumption	I_{DD2}	f_{CLI} = 14 MHz, V_{VI} = 2.0 V, no load, f_{INH} = 15.4 kHz, PW_{INH} = 5.0 μs				12	mA

Remarks 1. V_{OF}: output applied voltage, V_O: output voltage without load

2. The reference values are typical values only. The output deviation is only guaranteed within the chip.

Switching Characteristics (T_A = –30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse propagation delay time	t_{PHL}	C_L = 20 pF	10		54	ns
	t_{PLH}	C_L = 20 pF	10		54	ns
Clock frequency 1	f_{CLK1}				15	MHz
Clock frequency 2	f_{CLK2}	With 3-phase clock input			15	MHz
Logic input capacitance	C_{I1}	Other than STHL, STHR			15	pF
STHL, STHR input capacitance	C_{I2}	STHL, STHR			20	pF
Video input capacitance	C_3	C1 to C3, V_{VI} = 2.0 V			50	pF

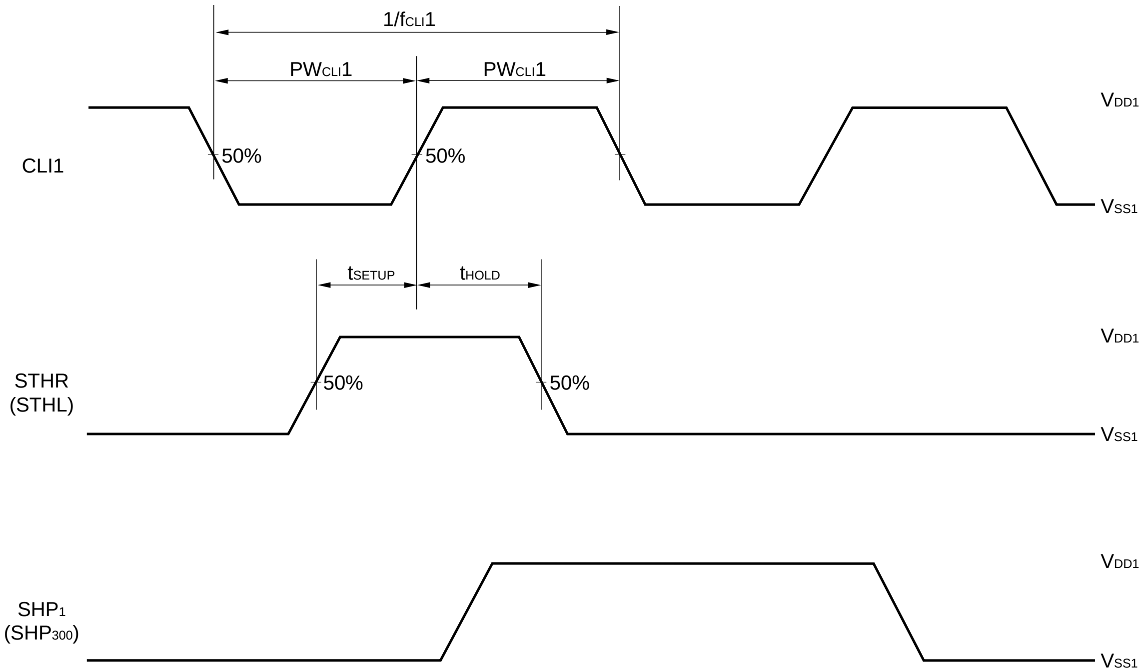
Timing Requirements (T_A = –30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLI}	Duty = 50%	33			ns
CLK-CLK time	t_{CL1-2}		16.6			ns
	t_{CL2-3}		16.6			ns
	t_{CL3-1}		16.6			ns
		t_{CL1-2} + t_{CL2-3} + t_{CL3-1}			$1/f_{CLI1}$	ns
Start pulse setup time	t_{SETUP}		8			ns
Start pulse hold time	t_{HOLD}		8			ns
Reset pulse width	PW_{RES}		66			ns
INH setup time	t_{ISETUP}		33			ns
INH hold time	t_{IHOLD}		33			ns
Reset-INH time	t_{R-I}		81			ns
INH pulse width	PW_{INH}	CLI1	5			CLK

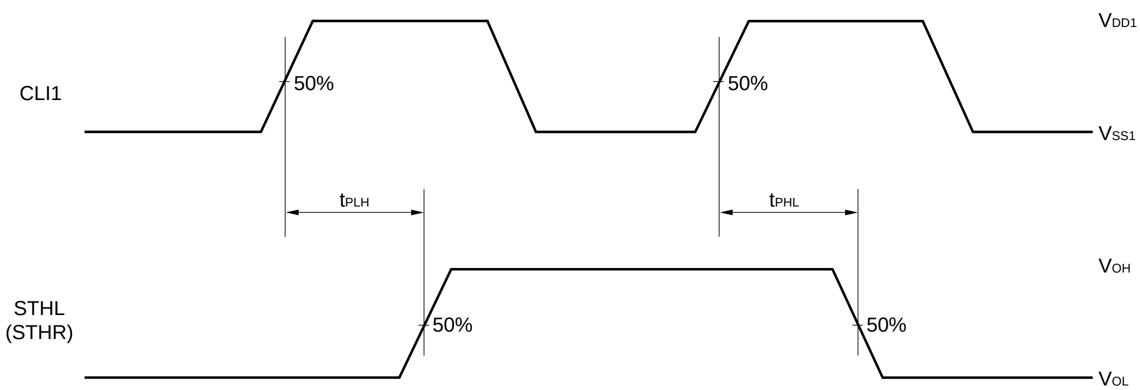
Remark Keep the rise and fall times of the logic input signals to within t_r = t_f = 5 ns (10 to 90%).
As an example, the switching characteristic wave of CLI1 is defined on the next page.

Switching Characteristic Waveform (Simultaneous/successive sampling)

Start Pulse Input Timing

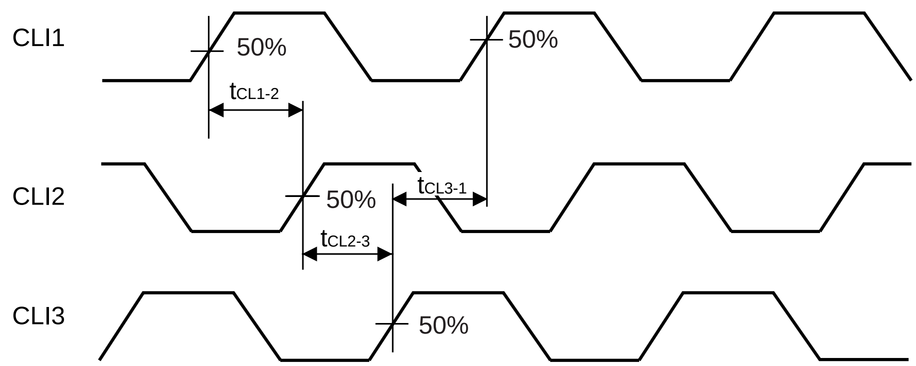


Start Pulse Output Timing

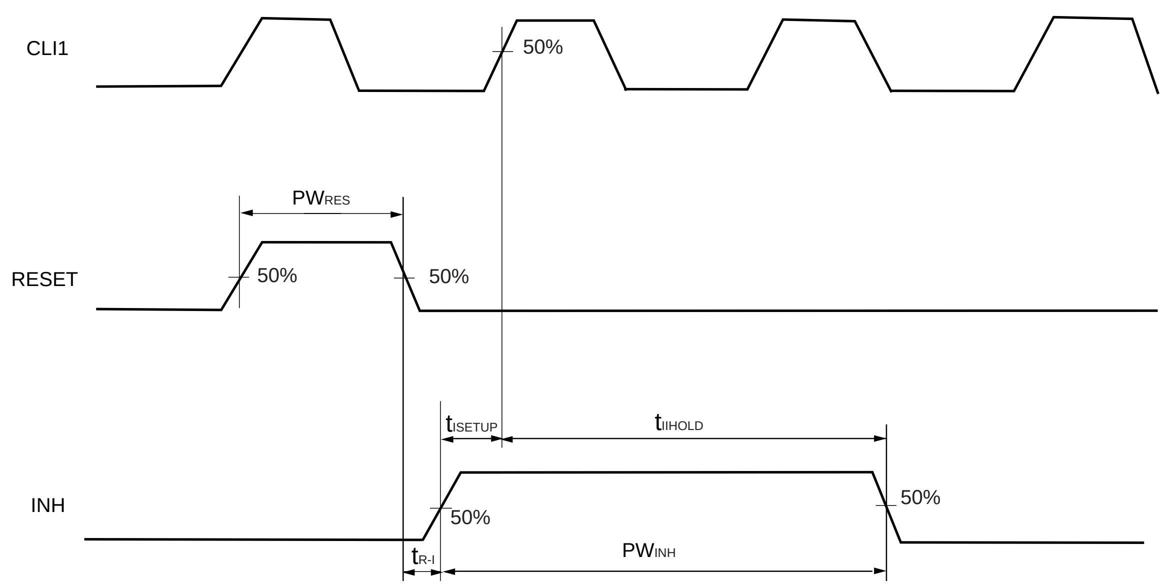


Remark The input/output timing of the start pulse is the same for simultaneous/successive sampling.

Clock Input Timing



RESET INH Pulse Timing



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)