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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256-GRAY SCALES)

DESCRIPTION

The μ PD16754 is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ -corrected by an internal D/A converter and 8-by-2 external power modules.

Because the output dynamic range is as large as $V_{DD2} - 0.2$ V to $V_{SS2} + 0.2$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a clock frequency of 40 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels.

FEATURES

- CMOS level input
- 384 Outputs
- Input of 8 bits (gradation data) by 6 dots
- Capable of outputting 256 values by means of 8-by-2 external power modules (16 units) and a D/A converter
- Logic power supply voltage (V_{DD1}): 3.0 to 3.6 V
- Driver power supply voltage (V_{DD2}): 8.5 to 9.5 V
- Output dynamic range $V_{DD2} - 0.2$ V to $V_{SS2} + 0.2$ V
- High-speed data transfer: $f_{CLK} = 40$ MHz MAX. (internal data transfer speed when operating at $V_{DD1} = 3.0$ V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Display data inversion function (POL21, POL22)

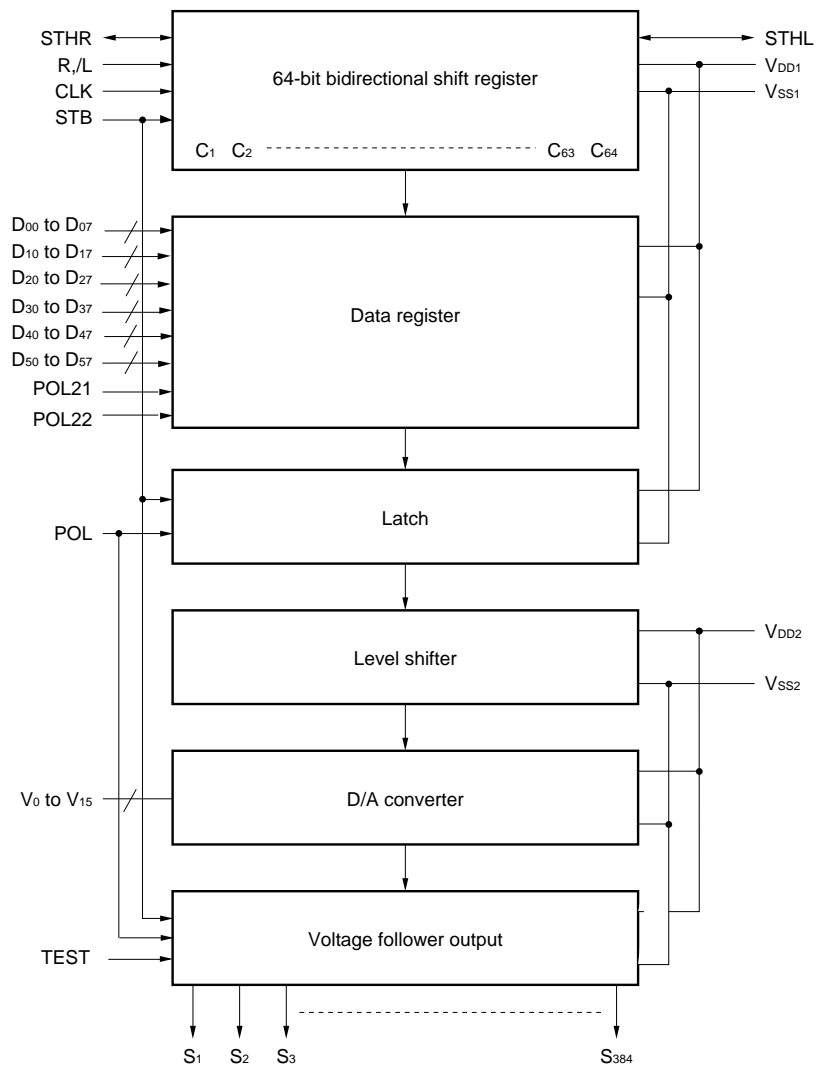
ORDERING INFORMATION

Part Number	Package
μ PD16754N - xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

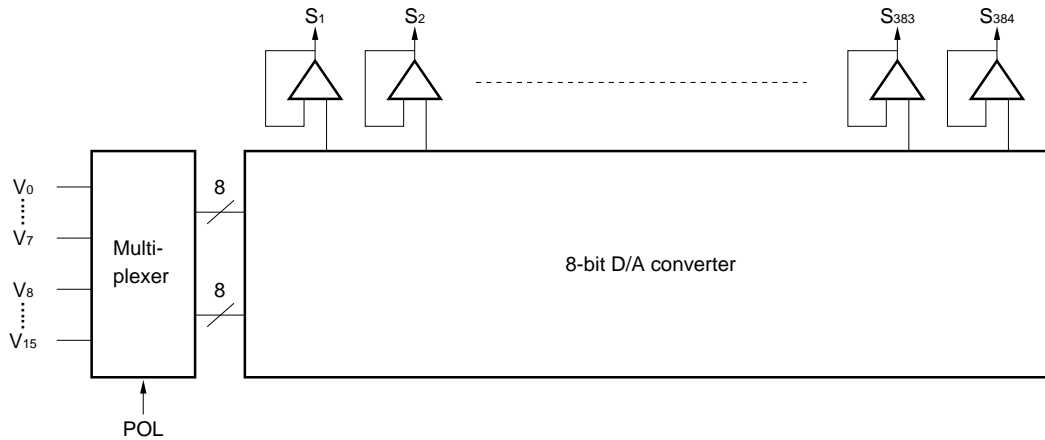
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★ 1. BLOCK DIAGRAM

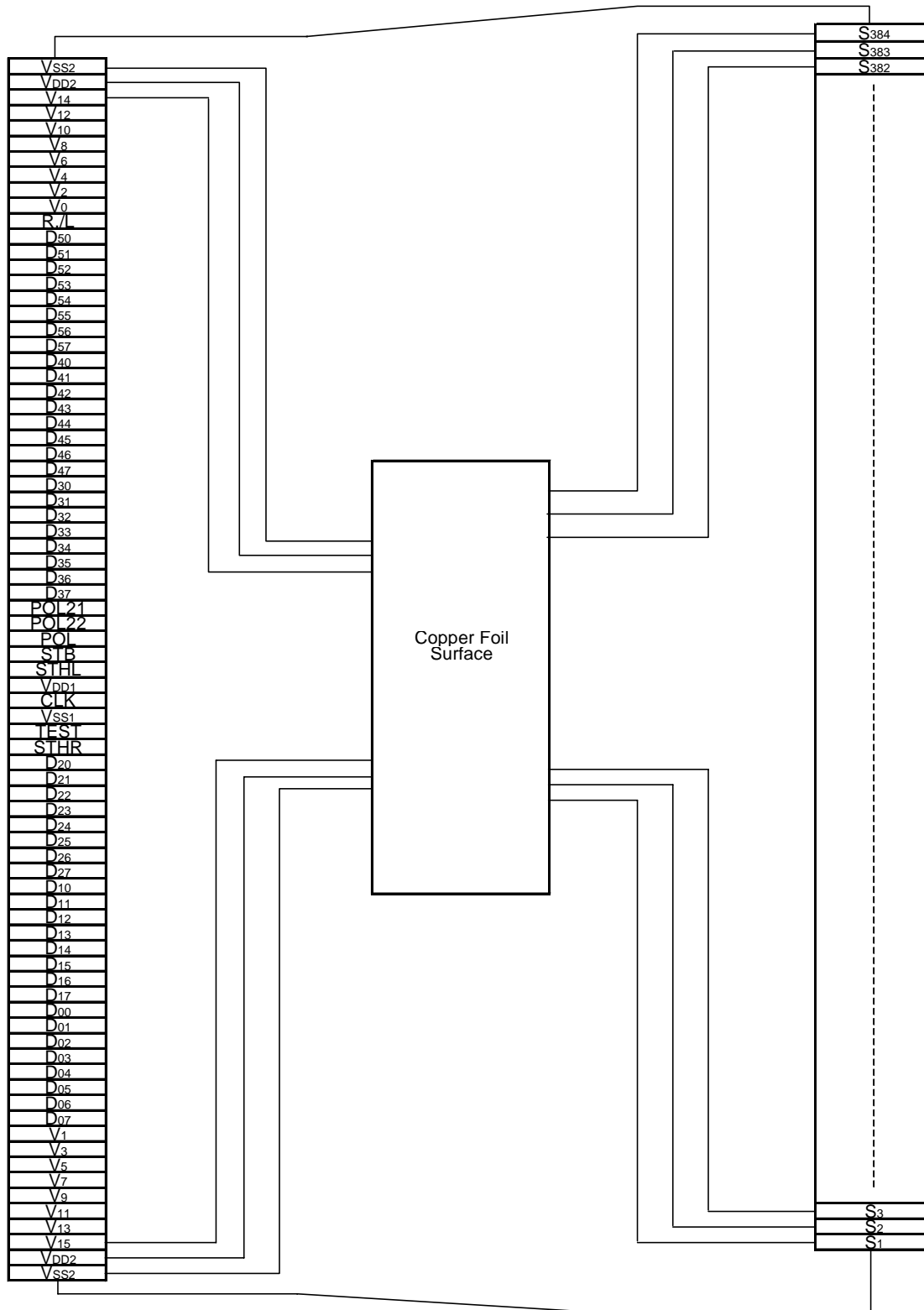


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16754N - xxx) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S ₁ to S ₃₈₄	Driver	Output	The D/A converted 256-gray-scale analog voltage is output.
D ₀₀ to D ₀₇	Display data	Input	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). D _{X0} : LSB, D _{X7} : MSB
D ₁₀ to D ₁₇			
D ₂₀ to D ₂₇			
D ₃₀ to D ₃₇			
D ₄₀ to D ₄₇			
D ₅₀ to D ₅₇			
R _{,/L}	Shift direction control	Input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R _{,/L} = H: STHR input, S ₁ → S ₃₈₄ , STHL output R _{,/L} = L: STHL input, S ₃₈₄ → S ₁ , STHR output
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK. R _{,/L} = H (right shift): STHR input, STHL output R _{,/L} = L (left shift): STHL input, STHR output A high level should be input as the pulse of one cycle of the clock signal. If the start pulse input is more then 2CLK, the first 1CLK of the high-level input is valid.
STHL	Left shift start pulse	I/O	
CLK	Shift clock	Input	Refers to the shift register's shift clock input. At the rising edge of the 64th after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 66th clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity	Input	POL = L: The S _{2n-1} output uses V ₀ to V ₇ as the reference supply. The S _{2n} output uses V ₈ to V ₁₅ as the reference supply. POL = H: The S _{2n-1} output uses V ₈ to V ₁₅ as the reference supply. The S _{2n} output uses V ₀ to V ₇ as the reference supply. S _{2n-1} indicates the odd output: and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time (t _{POL-STB}) with respect to STB's rising edge.
POL21, POL22	Data inversion	Input	Data inversion can invert when display data is loaded. POL21: Invert/not invert of display data D ₀₀ to D ₀₇ , D ₁₀ to D ₁₇ , D ₂₀ to D ₂₇ . POL22: Invert/not invert of display data D ₃₀ to D ₃₇ , D ₄₀ to D ₄₇ , D ₅₀ to D ₅₇ . POL21, POL22 = H: Data inversion loads display data after inverting it. POL21, POL22 = L: Data inversion does not invert input data.
TEST	TEST	Input	When this function is required, leave this pin = H or open. TEST is pulled up to the V _{DD1} power supply inside the IC.

(2/2)

Pin Symbol	Pin Name	I/O	Description
V ₀ to V ₁₅	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.2 V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2}$ $0.5 V_{DD2} - 0.3 \geq V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} \geq V_{SS2} + 0.2 V$
V _{DD1}	Logic power supply	–	3.0 to 3.6 V
V _{DD2}	Driver power supply	–	8.5 to 9.5 V
V _{SS1}	Logic ground	–	Grounding
V _{SS2}	Driver ground	–	Grounding

- Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V₀ to V₁₅ in that order. Reverse this sequence to shut down (Simultaneous power application to V_{DD2} and V₀ to V₁₅ is possible.).**
- 2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V₀, V₁, V₂, ..., V₁₅) and V_{SS2}.**

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors.

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2} , common electrode potential V_{COM} , and γ -corrected voltages V_0 to V_{15} and the input data.

Be sure to maintain the voltage relationships as follows:

$$V_{DD2} - 0.2\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2}$$

$$0.5 V_{DD2} - 0.3 \geq V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} \geq V_{SS2} + 0.2\text{ V}.$$

Figures 5-2 shows γ -corrected power supply voltage and ladder resistors ratio and Figures 5-3 shows the relationship between the input data and the output voltage and the resistance values of the resistor strings.

★ Figure 5-1. Relationship between Input Data and γ -corrected Power Supplies

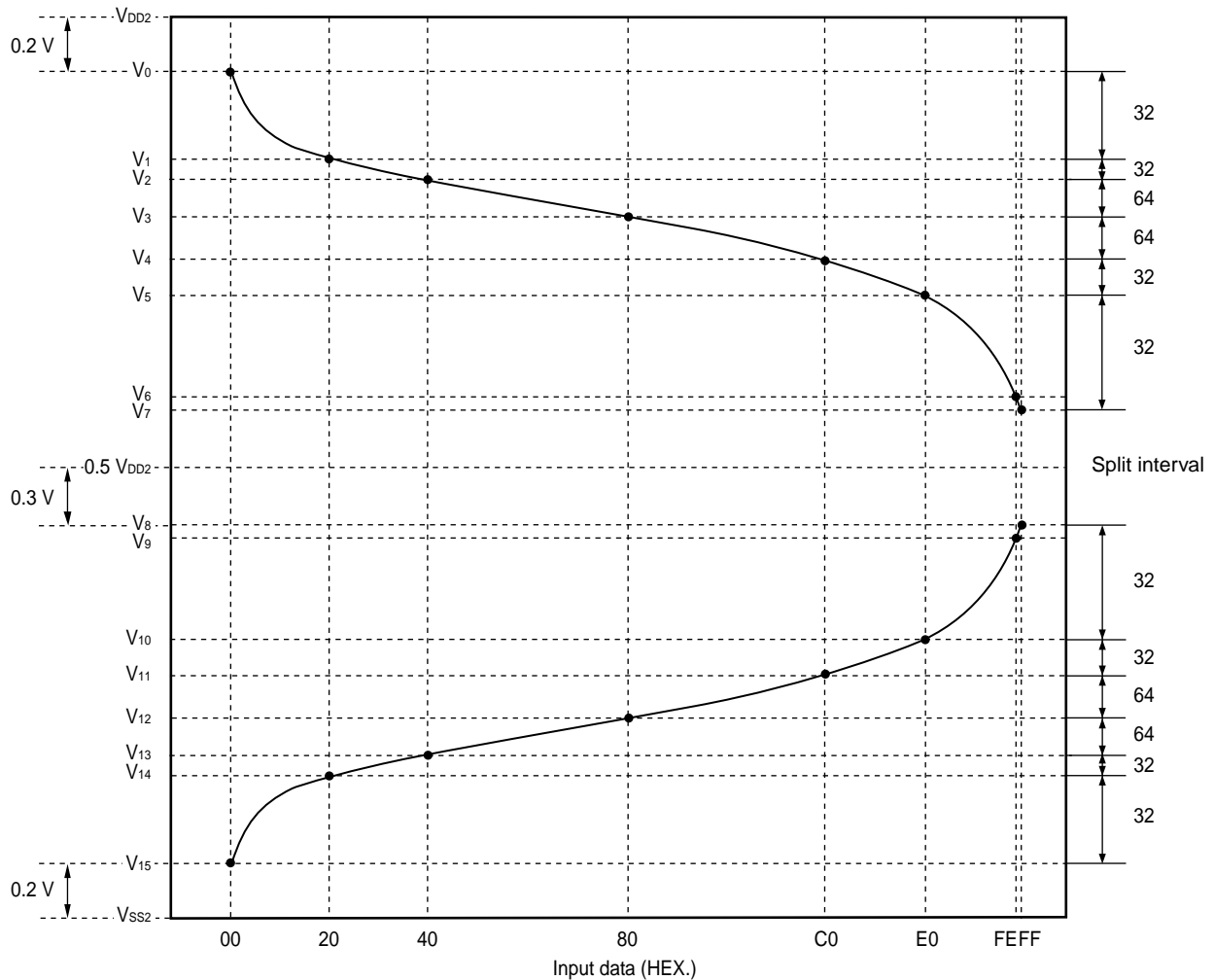
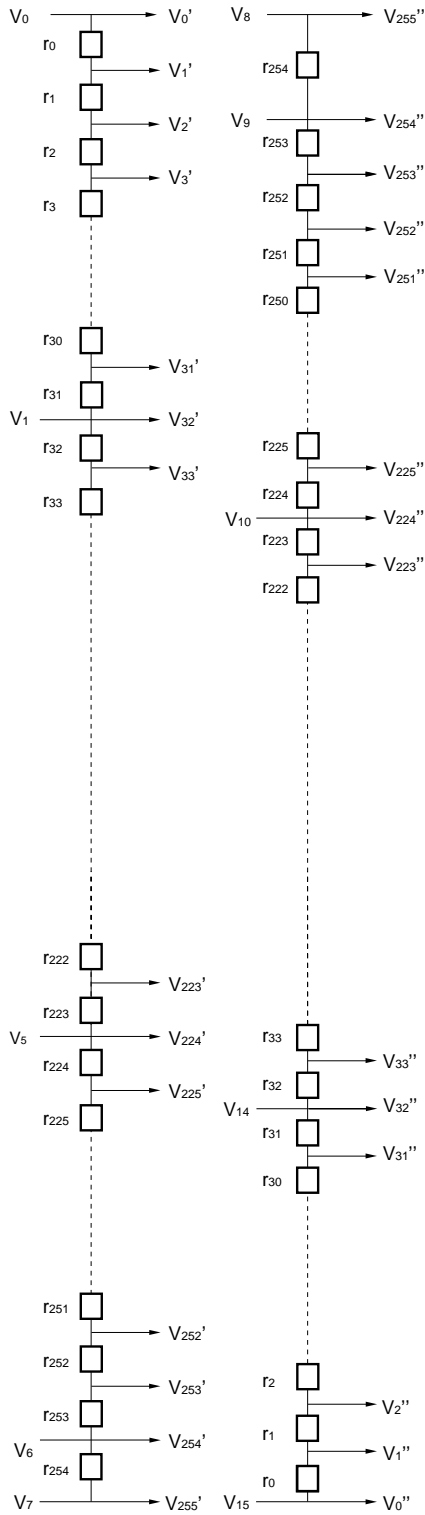




Figure 5-2. γ -corrected Voltages and Ladder Resistors Ratio



m	Ratio 1	Ratio 2	Value	m	Ratio 1	Ratio 2	Value	m	Ratio 1	Ratio 2	Value	m	Ratio 1	Ratio 2	Value	
r0	16.0	0.0267	400.0	r64	1.0	0.0017	25.0	r128	1.0	0.0017	25.0	r192	1.7	0.0028	42.5	
r1	14.5	0.0242	362.5	r65	1.0	0.0017	25.0	r129	1.0	0.0017	25.0	r193	1.7	0.0028	42.5	
r2	13.0	0.0217	325.0	r66	1.0	0.0017	25.0	r130	1.0	0.0017	25.0	r194	1.7	0.0028	42.5	
r3	11.5	0.0192	287.5	r67	1.0	0.0017	25.0	r131	1.0	0.0017	25.0	r195	1.7	0.0028	42.5	
r4	10.0	0.0167	250.0	r68	1.0	0.0017	25.0	r132	1.0	0.0017	25.0	r196	1.7	0.0028	42.5	
r5	8.9	0.0148	222.5	r69	1.0	0.0017	25.0	r133	1.0	0.0017	25.0	r197	1.7	0.0028	42.5	
r6	7.8	0.0130	195.0	r70	1.0	0.0017	25.0	r134	1.0	0.0017	25.0	r198	1.7	0.0028	42.5	
r7	6.8	0.0113	170.0	r71	1.0	0.0017	25.0	r135	1.0	0.0017	25.0	r199	1.7	0.0028	42.5	
r8	5.8	0.0097	145.0	r72	1.0	0.0017	25.0	r136	1.0	0.0017	25.0	r200	1.9	0.0032	47.5	
r9	4.8	0.0080	120.0	r73	1.0	0.0017	25.0	r137	1.0	0.0017	25.0	r201	1.9	0.0032	47.5	
r10	4.8	0.0080	120.0	r74	1.0	0.0017	25.0	r138	1.0	0.0017	25.0	r202	1.9	0.0032	47.5	
r11	4.8	0.0080	120.0	r75	1.0	0.0017	25.0	r139	1.0	0.0017	25.0	r203	1.9	0.0032	47.5	
r12	3.8	0.0063	95.0	r76	1.0	0.0017	25.0	r140	1.0	0.0017	25.0	r204	1.9	0.0032	47.5	
r13	3.8	0.0063	95.0	r77	1.0	0.0017	25.0	r141	1.0	0.0017	25.0	r205	1.9	0.0032	47.5	
r14	3.8	0.0063	95.0	r78	1.0	0.0017	25.0	r142	1.0	0.0017	25.0	r206	1.9	0.0032	47.5	
r15	3.0	0.0050	75.0	r79	1.0	0.0017	25.0	r143	1.0	0.0017	25.0	r207	1.9	0.0032	47.5	
r16	3.0	0.0050	75.0	r80	1.0	0.0017	25.0	r144	1.0	0.0017	25.0	r208	2.1	0.0035	52.5	
r17	3.0	0.0050	75.0	r81	1.0	0.0017	25.0	r145	1.0	0.0017	25.0	r209	2.1	0.0035	52.5	
r18	2.5	0.0042	62.5	r82	1.0	0.0017	25.0	r146	1.0	0.0017	25.0	r210	2.1	0.0035	52.5	
r19	2.5	0.0042	62.5	r83	1.0	0.0017	25.0	r147	1.0	0.0017	25.0	r211	2.1	0.0035	52.5	
r20	2.5	0.0042	62.5	r84	1.0	0.0017	25.0	r148	1.0	0.0017	25.0	r212	2.1	0.0035	52.5	
r21	2.0	0.0033	50.0	r85	1.0	0.0017	25.0	r149	1.0	0.0017	25.0	r213	2.1	0.0035	52.5	
r22	2.0	0.0033	50.0	r86	1.0	0.0017	25.0	r150	1.0	0.0017	25.0	r214	2.1	0.0035	52.5	
r23	2.0	0.0033	50.0	r87	1.0	0.0017	25.0	r151	1.0	0.0017	25.0	r215	2.1	0.0035	52.5	
r24	1.5	0.0025	37.5	r88	1.0	0.0017	25.0	r152	1.1	0.0018	27.5	r216	2.3	0.0038	57.5	
r25	1.5	0.0025	37.5	r89	1.0	0.0017	25.0	r153	1.1	0.0018	27.5	r217	2.3	0.0038	57.5	
r26	1.5	0.0025	37.5	r90	1.0	0.0017	25.0	r154	1.1	0.0018	27.5	r218	2.3	0.0038	57.5	
r27	1.5	0.0025	37.5	r91	1.0	0.0017	25.0	r155	1.1	0.0018	27.5	r219	2.3	0.0038	57.5	
r28	1.5	0.0025	37.5	r92	1.0	0.0017	25.0	r156	1.1	0.0018	27.5	r220	2.3	0.0038	57.5	
r29	1.5	0.0025	37.5	r93	1.0	0.0017	25.0	r157	1.1	0.0018	27.5	r221	2.3	0.0038	57.5	
r30	1.5	0.0025	37.5	r94	1.0	0.0017	25.0	r158	1.1	0.0018	27.5	r222	2.3	0.0038	57.5	
r31	1.5	0.0025	37.5	r95	1.0	0.0017	25.0	r159	1.1	0.0018	27.5	r223	2.3	0.0038	57.5	
r32	1.4	0.0023	35.0	r96	1.0	0.0017	25.0	r160	1.2	0.0020	30.0	r224	2.3	0.0038	57.5	
r33	1.4	0.0023	35.0	r97	1.0	0.0017	25.0	r161	1.2	0.0020	30.0	r225	2.8	0.0047	70.0	
r34	1.4	0.0023	35.0	r98	1.0	0.0017	25.0	r162	1.2	0.0020	30.0	r226	2.8	0.0047	70.0	
r35	1.4	0.0023	35.0	r99	1.0	0.0017	25.0	r163	1.2	0.0020	30.0	r227	2.8	0.0047	70.0	
r36	1.4	0.0023	35.0	r100	1.0	0.0017	25.0	r164	1.2	0.0020	30.0	r228	3.3	0.0055	82.5	
r37	1.4	0.0023	35.0	r101	1.0	0.0017	25.0	r165	1.2	0.0020	30.0	r229	3.3	0.0055	82.5	
r38	1.4	0.0023	35.0	r102	1.0	0.0017	25.0	r166	1.2	0.0020	30.0	r230	3.3	0.0055	82.5	
r39	1.4	0.0023	35.0	r103	1.0	0.0017	25.0	r167	1.2	0.0020	30.0	r231	3.8	0.0063	95.0	
r40	1.3	0.0022	32.5	r104	1.0	0.0017	25.0	r168	1.3	0.0022	32.5	r232	3.8	0.0063	95.0	
r41	1.3	0.0022	32.5	r105	1.0	0.0017	25.0	r169	1.3	0.0022	32.5	r233	3.8	0.0063	95.0	
r42	1.3	0.0022	32.5	r106	1.0	0.0017	25.0	r170	1.3	0.0022	32.5	r234	4.5	0.0075	112.5	
r43	1.3	0.0022	32.5	r107	1.0	0.0017	25.0	r171	1.3	0.0022	32.5	r235	4.5	0.0075	112.5	
r44	1.3	0.0022	32.5	r108	1.0	0.0017	25.0	r172	1.3	0.0022	32.5	r236	4.5	0.0075	112.5	
r45	1.3	0.0022	32.5	r109	1.0	0.0017	25.0	r173	1.3	0.0022	32.5	r237	5.2	0.0087	130.0	
r46	1.3	0.0022	32.5	r110	1.0	0.0017	25.0	r174	1.3	0.0022	32.5	r238	5.2	0.0087	130.0	
r47	1.3	0.0022	32.5	r111	1.0	0.0017	25.0	r175	1.3	0.0022	32.5	r239	5.9	0.0098	147.5	
r48	1.2	0.0020	30.0	r112	1.0	0.0017	25.0	r176	1.4	0.0023	35.0	r240	5.9	0.0098	147.5	
r49	1.2	0.0020	30.0	r113	1.0	0.0017	25.0	r177	1.4	0.0023	35.0	r241	6.6	0.0110	165.0	
r50	1.2	0.0020	30.0	r114	1.0	0.0017	25.0	r178	1.4	0.0023	35.0	r242	6.6	0.0110	165.0	
r51	1.2	0.0020	30.0	r115	1.0	0.0017	25.0	r179	1.4	0.0023	35.0	r243	7.3	0.0122	182.5	
r52	1.2	0.0020	30.0	r116	1.0	0.0017	25.0	r180	1.4	0.0023	35.0	r244	7.3	0.0122	182.5	
r53	1.2	0.0020	30.0	r117	1.0	0.0017	25.0	r181	1.4	0.0023	35.0	r245	8.0	0.0133	200.0	
r54	1.2	0.0020	30.0	r118	1.0	0.0017	25.0	r182	1.4	0.0023	35.0	r246	8.0	0.0133	200.0	
r55	1.2	0.0020	30.0	r119	1.0	0.0017	25.0	r183	1.4	0.0023	35.0	r247	9.0	0.0150	225.0	
r56	1.1	0.0018	27.5	r120	1.0	0.0017	25.0	r184	1.5	0.0025	37.5	r248	9.0	0.0150	225.0	
r57	1.1	0.0018	27.5	r121	1.0	0.0017	25.0	r185	1.5	0.0025	37.5	r249	10.0	0.0167	250.0	
r58	1.1	0.0018	27.5	r122	1.0	0.0017	25.0	r186	1.5	0.0025	37.5	r250	10.0	0.0167	250.0	
r59	1.1	0.0018	27.5	r123	1.0	0.0017	25.0	r187	1.5	0.0025	37.5	r251	12.0	0.0200	300.0	
r60	1.1	0.0018	27.5	r124	1.0	0.0017	25.0	r188	1.5	0.0025	37.5	r252	12.0	0.0200	300.0	
r61	1.1	0.0018	27.5	r125	1.0	0.0017	25.0	r189	1.5	0.0025	37.5	r253	14.0	0.0233	350.0	
r62	1.1	0.0018	27.5	r126	1.0	0.0017	25.0	r190	1.5	0.0025	37.5	r254	14.0	0.0233	350.0	
r63	1.1	0.0018	27.5	r127	1.0	0.0017	25.0	r191	1.5	0.0025	37.5	Total resistance			15003	
															Minimum resistance value	25.0

Caution There is no connection between V7 and V8 in the chip.



Figure 5-3. Relationship between Input Data and Output Voltage (Output Voltage 1) (1/2)

VDD2 - 0.2 V ≥ V0 > V1 > V2 > V3 > V4 > V5 > V6 > V7 ≥ 0.5 VDD2 (POL21, POL22 = L)

Table with 4 columns: Data, Output Voltage, Data, Output Voltage, Data, Output Voltage, Data, Output Voltage. It lists various input data points (e.g., 00H, 01H, 02H) and their corresponding output voltages (e.g., V0, V1, V2) with numerical values and ranges.



Figure 5-3. Relationship between Input Data and Output Voltage (Output Voltage 2) (2/2)

0.5 V_{DD2} - 0.3 V ≥ V₈ > V₉ > V₁₀ > V₁₁ > V₁₂ > V₁₃ > V₁₄ > V₁₅ ≥ V_{DD2} + 0.2 V (POL21, POL22 = L)

Table with 4 columns: Data, Output Voltage, Data, Output Voltage, Data, Output Voltage, Data, Output Voltage. Rows contain data points for various input conditions and their corresponding output voltages.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 8 bits × 2 RGBs (6 dots)

Input width: 48 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

(2) R,/L = L (Left shift)

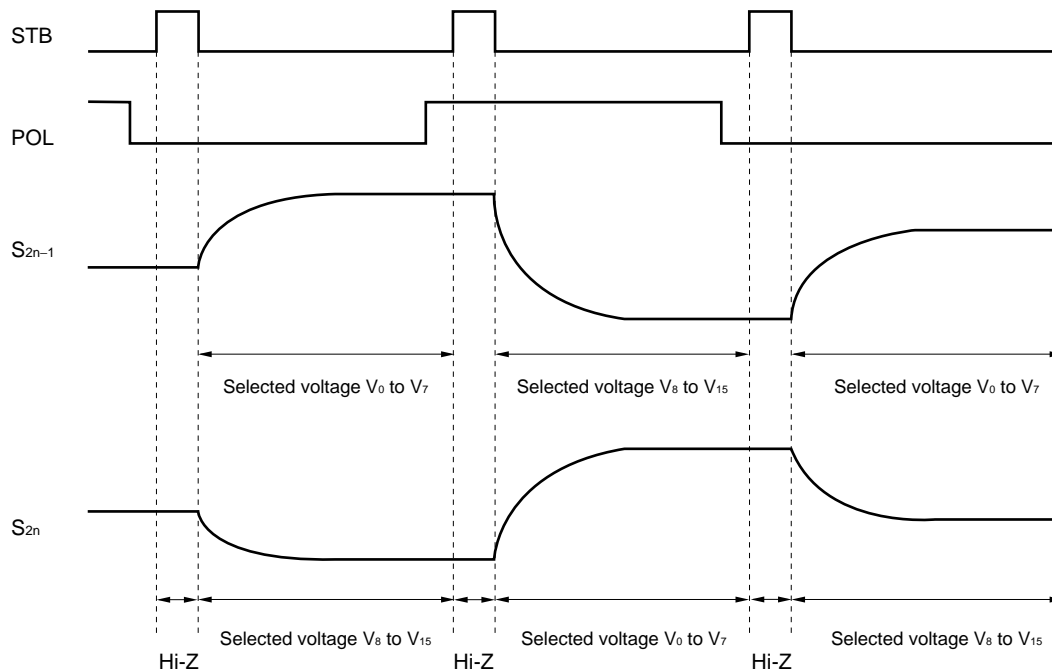
Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

POL	S _{2n-1} <small>Note</small>	S _{2n} <small>Note</small>
L	V ₀ to V ₇	V ₈ to V ₁₅
H	V ₈ to V ₁₅	V ₀ to V ₇

Note S_{2n-1} (Odd output), S_{2n} (Even output)

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

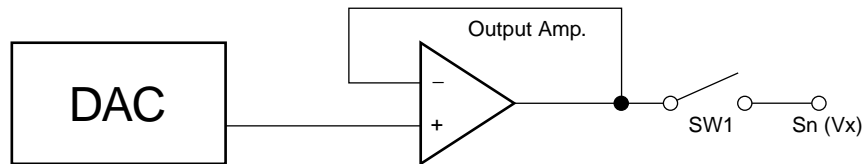


Remark Hi-Z: High impedance

8. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

Figure 8–1. Output Circuit Block Diagram

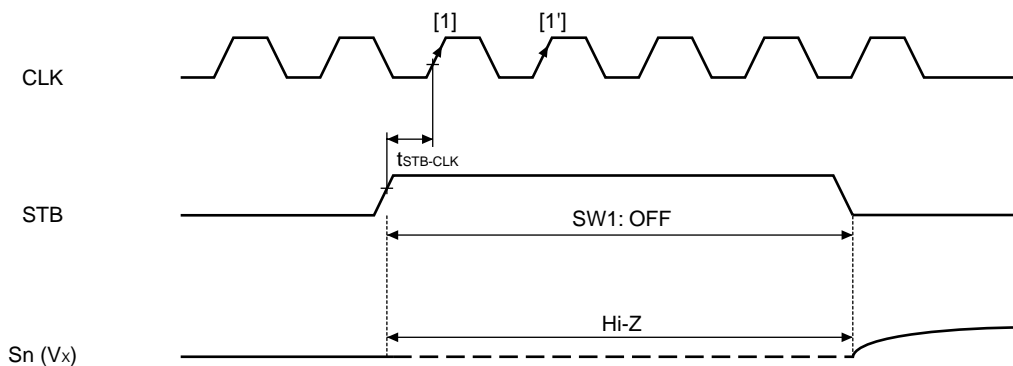


SW1 switches according to the level of STB signal.

STB = L: SW = ON

STB = H: SW = OFF

Figure 8–2. Output Circuit Timing Chart



STB = H is loaded with the rising edge of CLK [1]. However, when not satisfying the specification of $t_{STB-CLK}$, STB = H is loaded with the rising edge of the next CLK [1'].

Latch operation of display data is completed with the falling edge of the next CLK which loaded STB = H.

Therefore, in order to complete latch operation of display data, it is necessary to input at least 2CLK in STB = H period.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V _{DD1}	-0.5 to +4.0	V
Driver Part Supply Voltage	V _{DD2}	-0.5 to +10.0	V
Logic Part Input Voltage	V _{I1}	-0.5 to V _{DD1} + 0.5	V
Driver Part Input Voltage	V _{I2}	-0.5 to V _{DD2} + 0.5	V
Logic Part Output Voltage	V _{O1}	-0.5 to V _{DD1} + 0.5	V
Driver Part Output Voltage	V _{O2}	-0.5 to V _{DD2} + 0.5	V
Operating Ambient Temperature	T _A	-10 to +75	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V _{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V _{DD2}	8.5	9.0	9.5	V
High Level Input Voltage	V _{IH}	0.7 V _{DD1}		V _{DD1}	V
Low Level Input Voltage	V _{IL}	0		0.3 V _{DD1}	V
γ-Corrected Voltage	V ₀ to V ₇	0.5 V _{DD2}		V _{DD2} - 0.2	V
	V ₈ to V ₁₅	0.2		0.5 V _{DD2} - 0.3	V
Driver Part Output Voltage	V _O	V _{SS2} + 0.2		V _{DD2} - 0.2	V
Clock Frequency	f _{CLK}			40	MHz

Electrical Characteristics (T_A = -10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 8.5 to 9.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Leak Current	I _{IL}			±0.1	±1.0	μA
High Level Output Voltage	V _{OH}	STHR (STHL), I _{OH} = 0 mA	V _{DD1} - 0.1			V
Low Level Output Voltage	V _{OL}	STHR (STHL), I _{OL} = 0 mA			0.1	V
γ-Corrected Supply Resistance	R _γ	V ₀ to V ₇ = V ₈ to V ₁₅ = 4.0 V	4.4	8.9	17.8	kΩ
★ Driver Output Current	I _{VOH}	V _X = 7.0 V, V _{OUT} = 6.5 V ^{Note}		-0.185	-0.09	mA
	I _{VOL}	V _X = 1.0 V, V _{OUT} = 1.5 V ^{Note}	0.12	0.238		mA
Output Voltage Deviation	ΔV _O	V _O = 0.2 V to 1.2 V V _O = V _{DD2} - 1.2 V to V _{DD2} - 0.2 V		±30	±50	mV
		V _O = 1.2 V to 0.5 V _{DD2} - 0.3 V V _O = 0.5 V _{DD2} to V _{DD2} - 1.2 V		±10	±20	mV
Output Swing Difference Deviation	ΔV _{P-P}	V _O = 0.2 V to 0.8 V V _O = V _{DD2} - 0.8 V to V _{DD2} - 0.2 V		±20	±40	mV
		V _O = 0.8 V to 1.2 V V _O = V _{DD2} - 1.2 V to V _{DD2} - 0.8 V		±10	±20	mV
		V _O = 1.2 V to 0.5 V _{DD2} - 0.3 V V _O = 0.5 V _{DD2} to V _{DD2} - 1.2 V		±3	±10	mV
★ Output Swing Average Difference Deviation	AV _O	V _{DD2} = 8.5 V, V _O = 7.9 V, V ₃ = 6.22 V, V ₇ = 4.0 V, V ₈ = 4.0 V, V ₁₂ = 1.78 V, V ₁₅ = 0.1 V, V ₁ , V ₂ , V ₄ to V ₆ , V ₉ to V ₁₁ , V ₁₃ , V ₁₄ : Open, T _A = 25°C, Input data: 80H	4.433		4.447	V
Logic Part Dynamic Current Consumption	I _{DD1}	V _{DD1} , with no load		0.8	6.0	mA
★ Driver Part Dynamic Current Consumption	I _{DD2}	V _{DD2} , with no load		4.5	11.0	mA

Note V_X refers to the output voltage of analog output pins S₁ to S₃₈₄. V_{OUT} refers to the voltage applied to analog output pins S₁ to S₃₈₄.

- Cautions**
1. The STB cycle is defined to be 20 μs at f_{CLK} = 40 MHz.
 2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
 3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

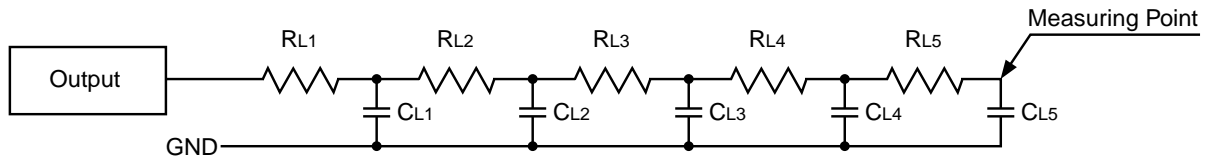
Switching Characteristics ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.0$ to 3.6 V, $V_{DD2} = 8.5$ to 9.5 V, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	$C_L = 15$ pF		8	20	ns
Driver Output Delay Time	t_{PLH2}	$C_L = 75$ pF, $R_L = 5$ kΩ		3	6	μs
	t_{PLH3}			4	8	μs
	t_{PHL2}			3	6	μs
	t_{PHL3}			4	8	μs
Input Capacitance	C_{i1}	STHR (STHL) excluded, $T_A = 25^\circ\text{C}$		4.8	10	pF
	C_{i2}	STHR (STHL), $T_A = 25^\circ\text{C}$		8.6	15	pF

<Measure Condition>

$R_{Ln} = 1$ kΩ

$C_{Ln} = 15$ pF



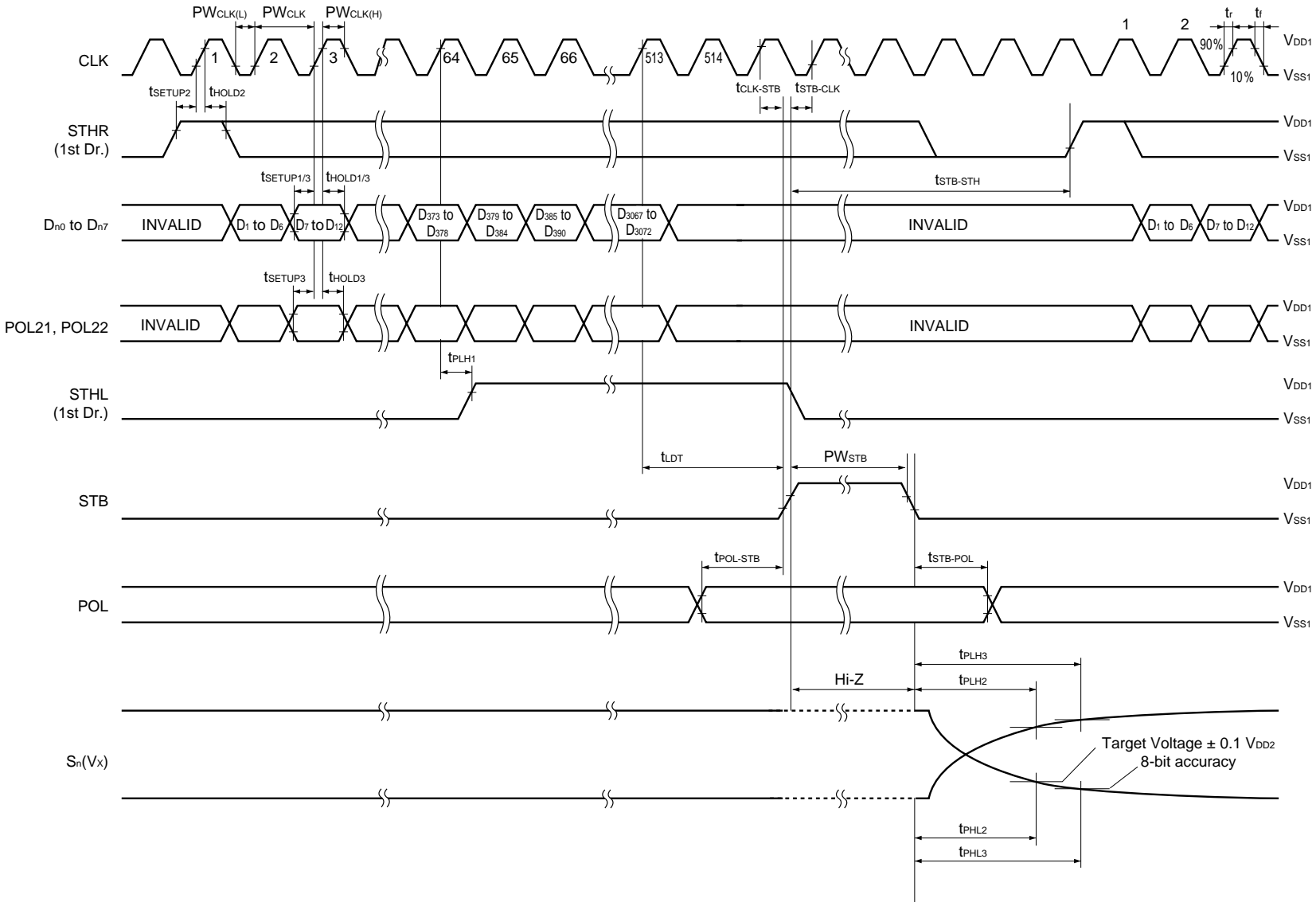
Timing Requirement ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.0$ to 3.6 V, $V_{SS1} = 0$ V, $t_r = t_f = 5.0$ ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		25			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	t_{SETUP1}		2			ns
Data Hold Time	t_{HOLD1}		2			ns
Start Pulse Setup Time	t_{SETUP2}		2			ns
Start Pulse Hold Time	t_{HOLD2}		2			ns
POL21, POL22 Setup Time	t_{SETUP3}		2			ns
POL21, POL22 Hold Time	t_{HOLD3}		2			ns
STB Pulse Width	PW_{STB}		2			μs
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK $\uparrow \rightarrow$ STB \uparrow	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB $\uparrow \rightarrow$ CLK \uparrow	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB $\uparrow \rightarrow$ STHR (STHL) \uparrow	2			CLK
POL-STB Time	$t_{POL-STB}$	POL \uparrow or $\downarrow \rightarrow$ STB \uparrow	-5			ns
STB-POL Time	$t_{STB-POL}$	STB $\downarrow \rightarrow$ POL \downarrow or \uparrow	6			ns

Remark Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.

★ Switching Characteristics Waveform (R,I/L = H)

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.



★ 10. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μ PD16754.

For more details, refer to the **Semiconductor Device Mount Manual**

(<http://www.necel.com/pkg/en/mount/index.html>).

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

 μ PD16754N - xxx: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds, pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm ² , time 3 to 5 seconds. Real bonding 165 to 180°C, pressure 25 to 45 kg/cm ² , time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

- ★ Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

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