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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16750

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256-GRAY SCALES)

DESCRIPTION

The μPD16750 is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ-corrected by an internal D/A converter and 8-by-2 external power modules. Because the output dynamic range is as large as V_{DD2} – 0.2 V to V_{SS2} + 0.2 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 40 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels. This driver is applicable to SXGA TFT-LCD panels by input display signal 2 systems (Clock divide).

FEATURES

- CMOS level input
- 384 outputs
- Input of 8 bits (gradation data) by 6 dots
- Capable of outputting 256 values by means of 8-by-2 external power modules (16 units) and a D/A converter
- Output dynamic range: V_{DD2} – 0.2 V to V_{SS2} + 0.2 V
- High-speed data transfer: f_{CLK} = 40 MHz (internal data transfer speed when operating at 3.0 V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Display data inversion function (POL21/22)
- Logic power supply voltage (V_{DD1}) : 3.3 V ± 0.3 V
- Driver power supply voltage (V_{DD2}) : 9.0 V ± 0.5 V
- Low power control function (LPC)

ORDERING INFORMATION

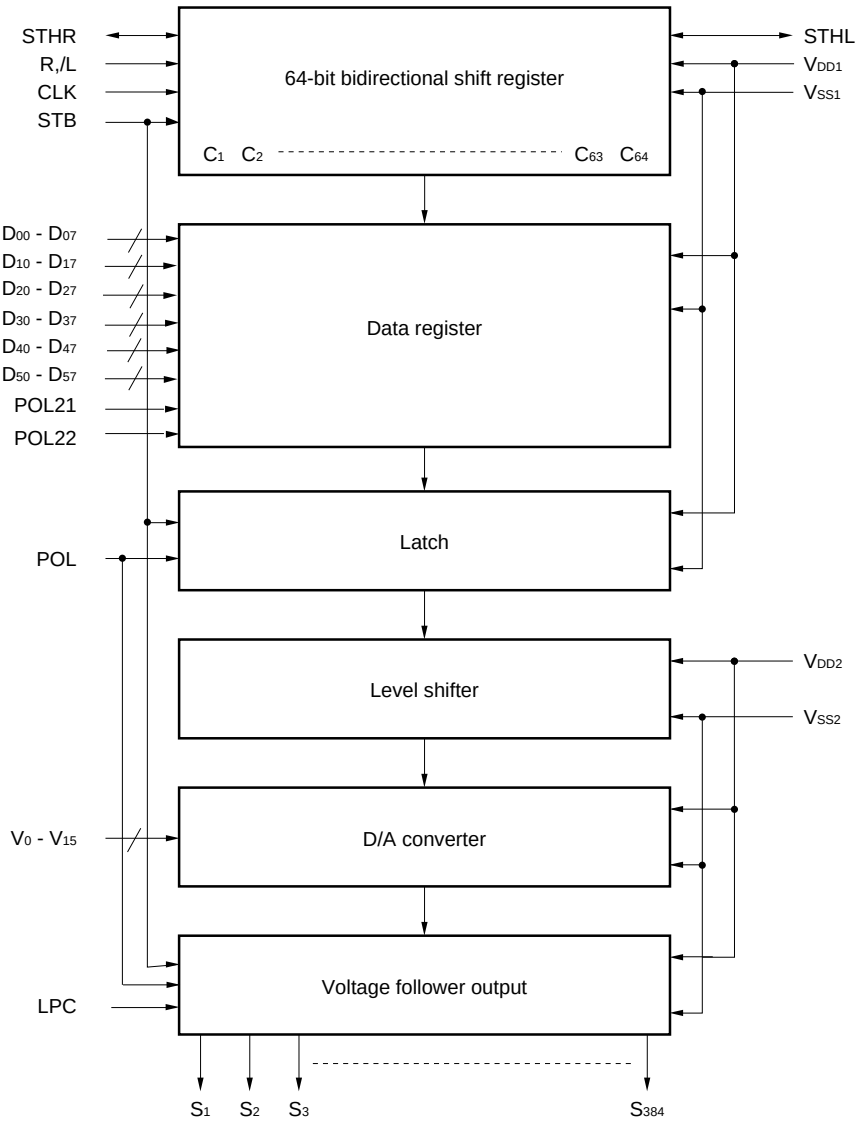
Part Number	Package
μPD16750N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

Document No. S13719EJ4V0DS00 (4th edition)
Date Published April 2000 NS CP (K)
Printed in Japan

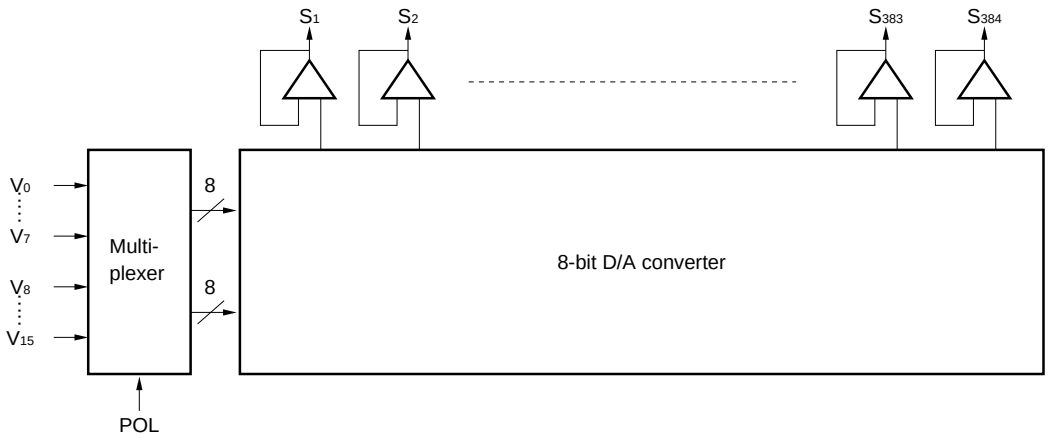
The mark ★ shows major revised points.

1. BLOCK DIAGRAM

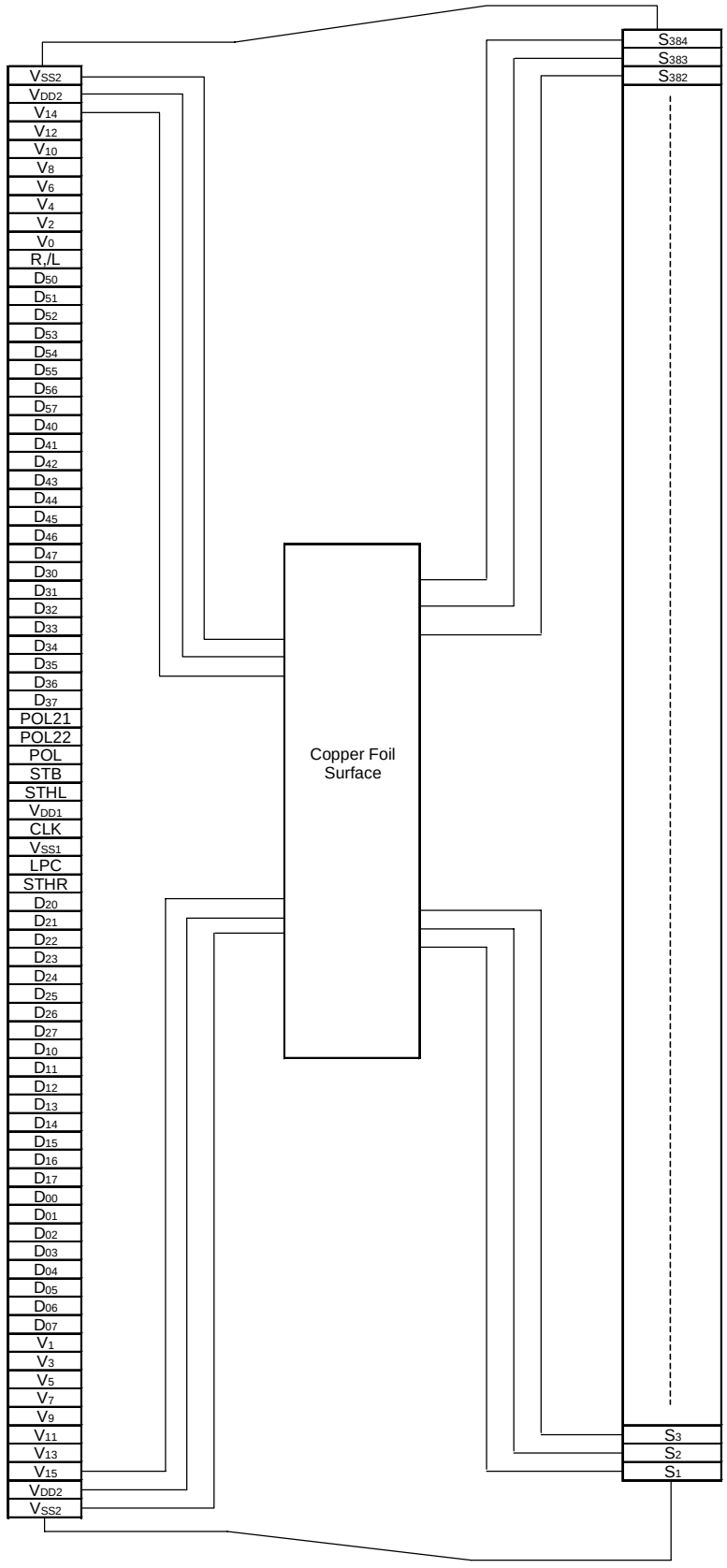


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16750N-xxx)



★ ★

Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{384}	Driver output	The D/A converted 256-gray-scale analog voltage is output.
D_{00} to D_{07}	Display data input	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X7}: MSB
D_{10} to D_{17}		
D_{20} to D_{27}		
D_{30} to D_{37}		
D_{40} to D_{47}		
D_{50} to D_{57}		
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H : STHR input, $S_1 \rightarrow S_{384}$, STHL output R,/L = L : STHL input, $S_{384} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse output pin. R,/L = L : Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L : The S_{2n-1} output uses V_0 to V_7 as the reference supply. The S_{2n} output uses V_8 to V_{15} as the reference supply. POL = H : The S_{2n-1} output uses V_8 to V_{15} as the reference supply. The S_{2n} output uses V_0 to V_7 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time($t_{POL-STB}$) with respect to STB's rising edge.
POL21 POL22	Data inversion	Data inversion can invert when display data is loaded. POL21/22 = H : Data inversion loads display data after inverting it. POL21/22 = L : Data inversion does not invert input data. POL21: D_{00} to D_{07}, D_{10} to D_{17}, D_{20} to D_{27} POL22: D_{30} to D_{37}, D_{40} to D_{47}, D_{50} to D_{57}
LPC	Low power control input	The output buffer constant current source is blocked, reducing current consumption. In lower power mode (LPC = L: DC-level input possible), the ordinary static current consumption can be reduced by approx. 33 %.
V_0 to V_{15}	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.2\ V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5\ V_{DD2}$ $0.5\ V_{DD2} - 0.3\ V > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.2\ V$
V_{DD1}	Logic power supply	3.3 V ± 0.3 V
V_{DD2}	Driver power supply	9.0 V ± 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_{15} in that order. Reverse this sequence to shut down (Simultaneous power application to V_{DD2} and V_0 to V_{15} is possible.).

2. To stabilize the supply voltage, please be sure to insert a 0.1-μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2,....., V_{15}) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_{15} and the input data. Be sure to maintain the voltage relationships of

$$V_{DD2} - 0.2\ V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5\ V_{DD2},$$

$$0.5\ V_{DD2} - 0.3\ V > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.2\ V$$

Figures 5–2 and 5–3 show the relationship between the input data and the output voltage. This driver IC is designed for only single-sided mounting. Therefore, please do not use it for γ-corrected power supply level inversion in double-sided mounting.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies

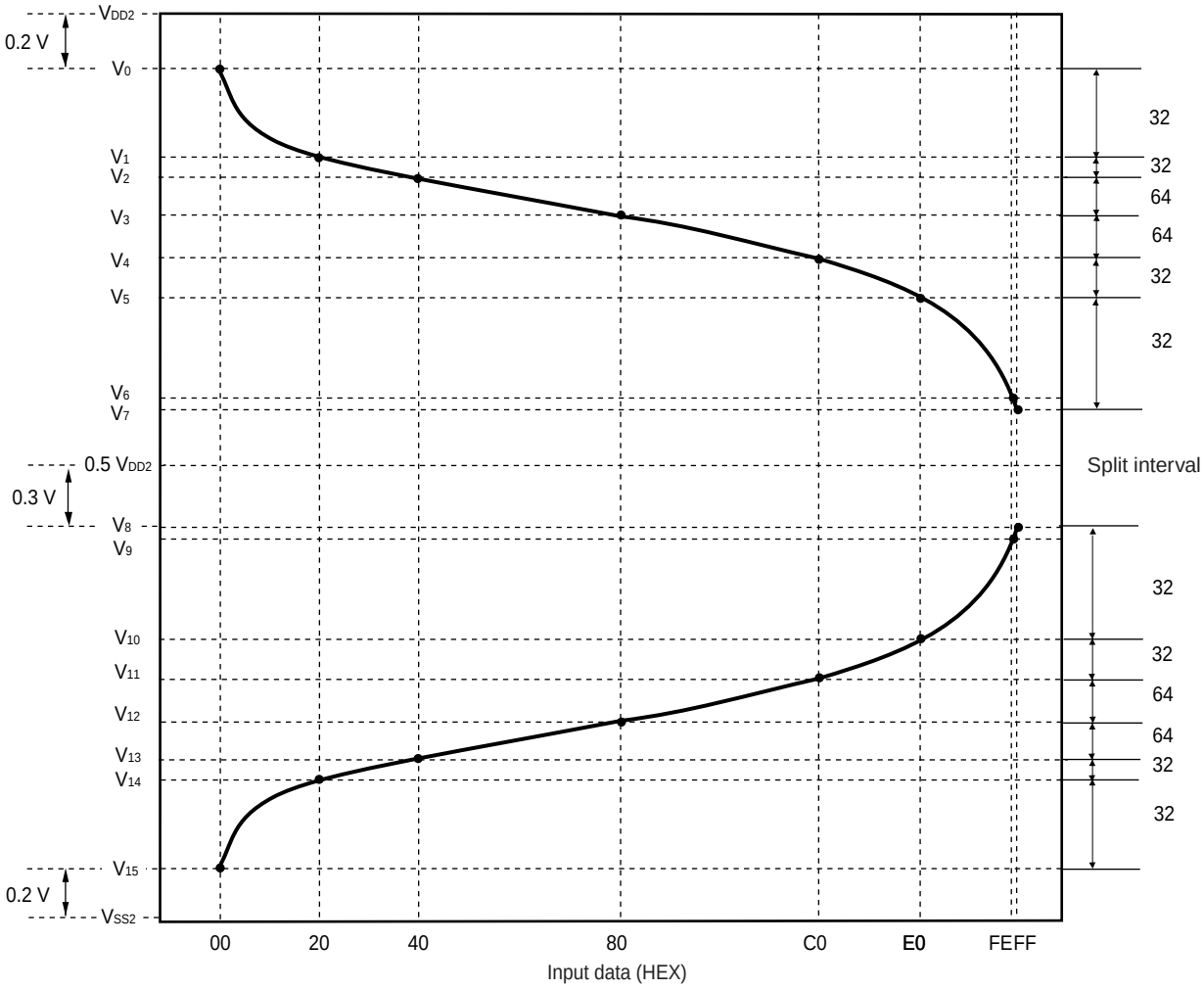
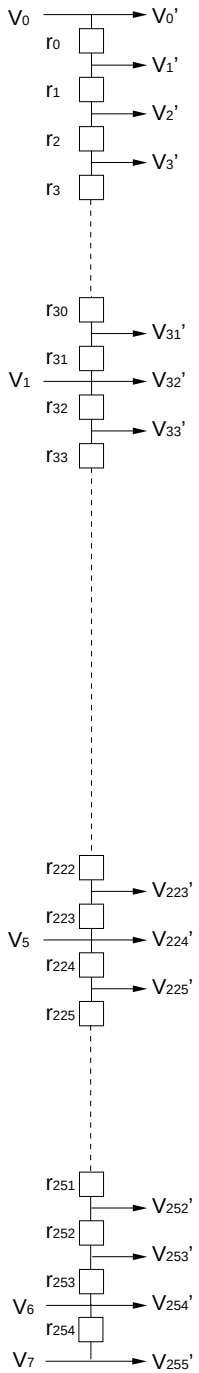


Figure 5–2. Relationship between Input Data and Output Voltage (1/4)

V_{DD2} – 0.2 V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5 V_{DD2}, POL21/22 = L

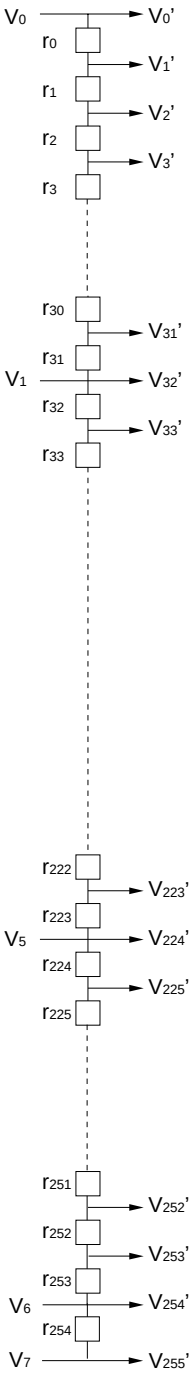


Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
00H	0	0	0	0	0	0	0	0	V_0'	V_0	r0	400.0
01H	0	0	0	0	0	0	0	1	V_1'	$V_1+(V_0-V_1)$ X 3465.0 / 3865	r1	362.5
02H	0	0	0	0	0	0	1	0	V_2'	$V_1+(V_0-V_1)$ X 3102.5 / 3865	r2	325.0
03H	0	0	0	0	0	0	1	1	V_3'	$V_1+(V_0-V_1)$ X 2777.5 / 3865	r3	287.5
04H	0	0	0	0	0	1	0	0	V_4'	$V_1+(V_0-V_1)$ X 2490.0 / 3865	r4	250.0
05H	0	0	0	0	0	1	0	1	V_5'	$V_1+(V_0-V_1)$ X 2240.0 / 3865	r5	222.5
06H	0	0	0	0	0	1	1	0	V_6'	$V_1+(V_0-V_1)$ X 2017.5 / 3865	r6	195.0
07H	0	0	0	0	0	1	1	1	V_7'	$V_1+(V_0-V_1)$ X 1822.5 / 3865	r7	170.0
08H	0	0	0	0	1	0	0	0	V_8'	$V_1+(V_0-V_1)$ X 1652.5 / 3865	r8	145.0
09H	0	0	0	0	1	0	0	1	V_9'	$V_1+(V_0-V_1)$ X 1507.5 / 3865	r9	120.0
0AH	0	0	0	0	1	0	1	0	V_{10}'	$V_1+(V_0-V_1)$ X 1387.5 / 3865	r10	120.0
0BH	0	0	0	0	1	0	1	1	V_{11}'	$V_1+(V_0-V_1)$ X 1267.5 / 3865	r11	120.0
0CH	0	0	0	0	1	1	0	0	V_{12}'	$V_1+(V_0-V_1)$ X 1147.5 / 3865	r12	95.0
0DH	0	0	0	0	1	1	0	1	V_{13}'	$V_1+(V_0-V_1)$ X 1052.5 / 3865	r13	95.0
0EH	0	0	0	0	1	1	1	0	V_{14}'	$V_1+(V_0-V_1)$ X 957.5 / 3865	r14	95.0
0FH	0	0	0	0	1	1	1	1	V_{15}'	$V_1+(V_0-V_1)$ X 862.5 / 3865	r15	75.0
10H	0	0	0	1	0	0	0	0	V_{16}'	$V_1+(V_0-V_1)$ X 787.5 / 3865	r16	75.0
11H	0	0	0	1	0	0	0	1	V_{17}'	$V_1+(V_0-V_1)$ X 712.5 / 3865	r17	75.0
12H	0	0	0	1	0	0	1	0	V_{18}'	$V_1+(V_0-V_1)$ X 637.5 / 3865	r18	62.5
13H	0	0	0	1	0	0	1	1	V_{19}'	$V_1+(V_0-V_1)$ X 575.0 / 3865	r19	62.5
14H	0	0	0	1	0	1	0	0	V_{20}'	$V_1+(V_0-V_1)$ X 512.5 / 3865	r20	62.5
15H	0	0	0	1	0	1	0	1	V_{21}'	$V_1+(V_0-V_1)$ X 450.0 / 3865	r21	50.0
16H	0	0	0	1	0	1	1	0	V_{22}'	$V_1+(V_0-V_1)$ X 400.0 / 3865	r22	50.0
17H	0	0	0	1	0	1	1	1	V_{23}'	$V_1+(V_0-V_1)$ X 350.0 / 3865	r23	50.0
18H	0	0	0	1	1	0	0	0	V_{24}'	$V_1+(V_0-V_1)$ X 300.0 / 3865	r24	37.5
19H	0	0	0	1	1	0	0	1	V_{25}'	$V_1+(V_0-V_1)$ X 262.5 / 3865	r25	37.5
1AH	0	0	0	1	1	0	1	0	V_{26}'	$V_1+(V_0-V_1)$ X 225.0 / 3865	r26	37.5
1BH	0	0	0	1	1	0	1	1	V_{27}'	$V_1+(V_0-V_1)$ X 187.5 / 3865	r27	37.5
1CH	0	0	0	1	1	1	0	0	V_{28}'	$V_1+(V_0-V_1)$ X 150.0 / 3865	r28	37.5
1DH	0	0	0	1	1	1	0	1	V_{29}'	$V_1+(V_0-V_1)$ X 112.5 / 3865	r29	37.5
1EH	0	0	0	1	1	1	1	0	V_{30}'	$V_1+(V_0-V_1)$ X 75.0 / 3865	r30	37.5
1FH	0	0	0	1	1	1	1	1	V_{31}'	$V_1+(V_0-V_1)$ X 37.5 / 3865	r31	37.5
20H	0	0	1	0	0	0	0	0	V_{32}'	V_1	r32	35.0
21H	0	0	1	0	0	0	0	1	V_{33}'	$V_2+(V_1-V_2)$ X 965.0 / 1000	r33	35.0
22H	0	0	1	0	0	0	1	0	V_{34}'	$V_2+(V_1-V_2)$ X 930.0 / 1000	r34	35.0
23H	0	0	1	0	0	0	1	1	V_{35}'	$V_2+(V_1-V_2)$ X 895.0 / 1000	r35	35.0
24H	0	0	1	0	0	1	0	0	V_{36}'	$V_2+(V_1-V_2)$ X 860.0 / 1000	r36	35.0
25H	0	0	1	0	0	1	0	1	V_{37}'	$V_2+(V_1-V_2)$ X 825.0 / 1000	r37	35.0
26H	0	0	1	0	0	1	1	0	V_{38}'	$V_2+(V_1-V_2)$ X 790.0 / 1000	r38	35.0
27H	0	0	1	0	0	1	1	1	V_{39}'	$V_2+(V_1-V_2)$ X 755.0 / 1000	r39	35.0
28H	0	0	1	0	1	0	0	0	V_{40}'	$V_2+(V_1-V_2)$ X 720.0 / 1000	r40	32.5
29H	0	0	1	0	1	0	0	1	V_{41}'	$V_2+(V_1-V_2)$ X 687.5 / 1000	r41	32.5
2AH	0	0	1	0	1	0	1	0	V_{42}'	$V_2+(V_1-V_2)$ X 655.0 / 1000	r42	32.5
2BH	0	0	1	0	1	0	1	1	V_{43}'	$V_2+(V_1-V_2)$ X 622.5 / 1000	r43	32.5
2CH	0	0	1	0	1	1	0	0	V_{44}'	$V_2+(V_1-V_2)$ X 590.0 / 1000	r44	32.5
2DH	0	0	1	0	1	1	0	1	V_{45}'	$V_2+(V_1-V_2)$ X 557.5 / 1000	r45	32.5
2EH	0	0	1	0	1	1	1	0	V_{46}'	$V_2+(V_1-V_2)$ X 525.0 / 1000	r46	32.5
2FH	0	0	1	0	1	1	1	1	V_{47}'	$V_2+(V_1-V_2)$ X 492.5 / 1000	r47	32.5
30H	0	0	1	1	0	0	0	0	V_{48}'	$V_2+(V_1-V_2)$ X 460.0 / 1000	r48	30.0
31H	0	0	1	1	0	0	0	1	V_{49}'	$V_2+(V_1-V_2)$ X 430.0 / 1000	r49	30.0
32H	0	0	1	1	0	0	1	0	V_{50}'	$V_2+(V_1-V_2)$ X 400.0 / 1000	r50	30.0
33H	0	0	1	1	0	0	1	1	V_{51}'	$V_2+(V_1-V_2)$ X 370.0 / 1000	r51	30.0
34H	0	0	1	1	0	1	0	0	V_{52}'	$V_2+(V_1-V_2)$ X 340.0 / 1000	r52	30.0
35H	0	0	1	1	0	1	0	1	V_{53}'	$V_2+(V_1-V_2)$ X 310.0 / 1000	r53	30.0
36H	0	0	1	1	0	1	1	0	V_{54}'	$V_2+(V_1-V_2)$ X 280.0 / 1000	r54	30.0
37H	0	0	1	1	0	1	1	1	V_{55}'	$V_2+(V_1-V_2)$ X 250.0 / 1000	r55	30.0
38H	0	0	1	1	1	0	0	0	V_{56}'	$V_2+(V_1-V_2)$ X 220.0 / 1000	r56	27.5
39H	0	0	1	1	1	0	0	1	V_{57}'	$V_2+(V_1-V_2)$ X 192.5 / 1000	r57	27.5
3AH	0	0	1	1	1	0	1	0	V_{58}'	$V_2+(V_1-V_2)$ X 165.0 / 1000	r58	27.5
3BH	0	0	1	1	1	0	1	1	V_{59}'	$V_2+(V_1-V_2)$ X 137.5 / 1000	r59	27.5
3CH	0	0	1	1	1	1	0	0	V_{60}'	$V_2+(V_1-V_2)$ X 110.0 / 1000	r60	27.5
3DH	0	0	1	1	1	1	0	1	V_{61}'	$V_2+(V_1-V_2)$ X 82.5 / 1000	r61	27.5
3EH	0	0	1	1	1	1	1	0	V_{62}'	$V_2+(V_1-V_2)$ X 55.0 / 1000	r62	27.5
3FH	0	0	1	1	1	1	1	1	V_{63}'	$V_2+(V_1-V_2)$ X 27.5 / 1000	r63	27.5

Caution There is no connection between V_7 and V_8 in the chip.

Figure 5–2. Relationship between Input Data and Output Voltage (2/4)

V_{DD2} – 0.2 V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5 V_{DD2}, POL21/22 = L

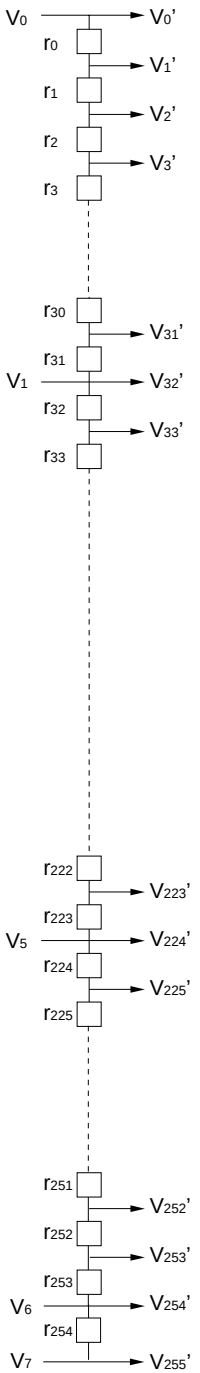


Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
40H	0	1	0	0	0	0	0	0	V_{64}'	V_2	r64	25.0
41H	0	1	0	0	0	0	0	1	V_{65}'	$V_3+(V_2-V_3)$ X 1575 / 1600	r65	25.0
42H	0	1	0	0	0	0	1	0	V_{66}'	$V_3+(V_2-V_3)$ X 1550 / 1600	r66	25.0
43H	0	1	0	0	0	0	1	1	V_{67}'	$V_3+(V_2-V_3)$ X 1525 / 1600	r67	25.0
44H	0	1	0	0	0	1	0	0	V_{68}'	$V_3+(V_2-V_3)$ X 1500 / 1600	r68	25.0
45H	0	1	0	0	0	1	0	1	V_{69}'	$V_3+(V_2-V_3)$ X 1475 / 1600	r69	25.0
46H	0	1	0	0	0	1	1	0	V_{70}'	$V_3+(V_2-V_3)$ X 1450 / 1600	r70	25.0
47H	0	1	0	0	0	1	1	1	V_{71}'	$V_3+(V_2-V_3)$ X 1425 / 1600	r71	25.0
48H	0	1	0	0	1	0	0	0	V_{72}'	$V_3+(V_2-V_3)$ X 1400 / 1600	r72	25.0
49H	0	1	0	0	1	0	0	1	V_{73}'	$V_3+(V_2-V_3)$ X 1375 / 1600	r73	25.0
4AH	0	1	0	0	1	0	1	0	V_{74}'	$V_3+(V_2-V_3)$ X 1350 / 1600	r74	25.0
4BH	0	1	0	0	1	0	1	1	V_{75}'	$V_3+(V_2-V_3)$ X 1325 / 1600	r75	25.0
4CH	0	1	0	0	1	1	0	0	V_{76}'	$V_3+(V_2-V_3)$ X 1300 / 1600	r76	25.0
4DH	0	1	0	0	1	1	0	1	V_{77}'	$V_3+(V_2-V_3)$ X 1275 / 1600	r77	25.0
4EH	0	1	0	0	1	1	1	0	V_{78}'	$V_3+(V_2-V_3)$ X 1250 / 1600	r78	25.0
4FH	0	1	0	0	1	1	1	1	V_{79}'	$V_3+(V_2-V_3)$ X 1225 / 1600	r79	25.0
50H	0	1	0	1	0	0	0	0	V_{80}'	$V_3+(V_2-V_3)$ X 1200 / 1600	r80	25.0
51H	0	1	0	1	0	0	0	1	V_{81}'	$V_3+(V_2-V_3)$ X 1175 / 1600	r81	25.0
52H	0	1	0	1	0	0	1	0	V_{82}'	$V_3+(V_2-V_3)$ X 1150 / 1600	r82	25.0
53H	0	1	0	1	0	0	1	1	V_{83}'	$V_3+(V_2-V_3)$ X 1125 / 1600	r83	25.0
54H	0	1	0	1	0	1	0	0	V_{84}'	$V_3+(V_2-V_3)$ X 1100 / 1600	r84	25.0
55H	0	1	0	1	0	1	0	1	V_{85}'	$V_3+(V_2-V_3)$ X 1075 / 1600	r85	25.0
56H	0	1	0	1	0	1	1	0	V_{86}'	$V_3+(V_2-V_3)$ X 1050 / 1600	r86	25.0
57H	0	1	0	1	0	1	1	1	V_{87}'	$V_3+(V_2-V_3)$ X 1025 / 1600	r87	25.0
58H	0	1	0	1	1	0	0	0	V_{88}'	$V_3+(V_2-V_3)$ X 1000 / 1600	r88	25.0
59H	0	1	0	1	1	0	0	1	V_{89}'	$V_3+(V_2-V_3)$ X 975 / 1600	r89	25.0
5AH	0	1	0	1	1	0	1	0	V_{90}'	$V_3+(V_2-V_3)$ X 950 / 1600	r90	25.0
5BH	0	1	0	1	1	0	1	1	V_{91}'	$V_3+(V_2-V_3)$ X 925 / 1600	r91	25.0
5CH	0	1	0	1	1	1	0	0	V_{92}'	$V_3+(V_2-V_3)$ X 900 / 1600	r92	25.0
5DH	0	1	0	1	1	1	0	1	V_{93}'	$V_3+(V_2-V_3)$ X 875 / 1600	r93	25.0
5EH	0	1	0	1	1	1	1	0	V_{94}'	$V_3+(V_2-V_3)$ X 850 / 1600	r94	25.0
5FH	0	1	0	1	1	1	1	1	V_{95}'	$V_3+(V_2-V_3)$ X 825 / 1600	r95	25.0
60H	0	1	1	0	0	0	0	0	V_{96}'	$V_3+(V_2-V_3)$ X 800 / 1600	r96	25.0
61H	0	1	1	0	0	0	0	1	V_{97}'	$V_3+(V_2-V_3)$ X 775 / 1600	r97	25.0
62H	0	1	1	0	0	0	1	0	V_{98}'	$V_3+(V_2-V_3)$ X 750 / 1600	r98	25.0
63H	0	1	1	0	0	0	1	1	V_{99}'	$V_3+(V_2-V_3)$ X 725 / 1600	r99	25.0
64H	0	1	1	0	0	1	0	0	V_{100}'	$V_3+(V_2-V_3)$ X 700 / 1600	r100	25.0
65H	0	1	1	0	0	1	0	1	V_{101}'	$V_3+(V_2-V_3)$ X 675 / 1600	r101	25.0
66H	0	1	1	0	0	1	1	0	V_{102}'	$V_3+(V_2-V_3)$ X 650 / 1600	r102	25.0
67H	0	1	1	0	0	1	1	1	V_{103}'	$V_3+(V_2-V_3)$ X 625 / 1600	r103	25.0
68H	0	1	1	0	1	0	0	0	V_{104}'	$V_3+(V_2-V_3)$ X 600 / 1600	r104	25.0
69H	0	1	1	0	1	0	0	1	V_{105}'	$V_3+(V_2-V_3)$ X 575 / 1600	r105	25.0
6AH	0	1	1	0	1	0	1	0	V_{106}'	$V_3+(V_2-V_3)$ X 550 / 1600	r106	25.0
6BH	0	1	1	0	1	0	1	1	V_{107}'	$V_3+(V_2-V_3)$ X 525 / 1600	r107	25.0
6CH	0	1	1	0	1	1	0	0	V_{108}'	$V_3+(V_2-V_3)$ X 500 / 1600	r108	25.0
6DH	0	1	1	0	1	1	0	1	V_{109}'	$V_3+(V_2-V_3)$ X 475 / 1600	r109	25.0
6EH	0	1	1	0	1	1	1	0	V_{110}'	$V_3+(V_2-V_3)$ X 450 / 1600	r110	25.0
6FH	0	1	1	0	1	1	1	1	V_{111}'	$V_3+(V_2-V_3)$ X 425 / 1600	r111	25.0
70H	0	1	1	1	0	0	0	0	V_{112}'	$V_3+(V_2-V_3)$ X 400 / 1600	r112	25.0
71H	0	1	1	1	0	0	0	1	V_{113}'	$V_3+(V_2-V_3)$ X 375 / 1600	r113	25.0
72H	0	1	1	1	0	0	1	0	V_{114}'	$V_3+(V_2-V_3)$ X 350 / 1600	r114	25.0
73H	0	1	1	1	0	0	1	1	V_{115}'	$V_3+(V_2-V_3)$ X 325 / 1600	r115	25.0
74H	0	1	1	1	0	1	0	0	V_{116}'	$V_3+(V_2-V_3)$ X 300 / 1600	r116	25.0
75H	0	1	1	1	0	1	0	1	V_{117}'	$V_3+(V_2-V_3)$ X 275 / 1600	r117	25.0
76H	0	1	1	1	0	1	1	0	V_{118}'	$V_3+(V_2-V_3)$ X 250 / 1600	r118	25.0
77H	0	1	1	1	0	1	1	1	V_{119}'	$V_3+(V_2-V_3)$ X 225 / 1600	r119	25.0
78H	0	1	1	1	1	0	0	0	V_{120}'	$V_3+(V_2-V_3)$ X 200 / 1600	r120	25.0
79H	0	1	1	1	1	0	0	1	V_{121}'	$V_3+(V_2-V_3)$ X 175 / 1600	r121	25.0
7AH	0	1	1	1	1	0	1	0	V_{122}'	$V_3+(V_2-V_3)$ X 150 / 1600	r122	25.0
7BH	0	1	1	1	1	0	1	1	V_{123}'	$V_3+(V_2-V_3)$ X 125 / 1600	r123	25.0
7CH	0	1	1	1	1	1	0	0	V_{124}'	$V_3+(V_2-V_3)$ X 100 / 1600	r124	25.0
7DH	0	1	1	1	1	1	0	1	V_{125}'	$V_3+(V_2-V_3)$ X 75 / 1600	r125	25.0
7EH	0	1	1	1	1	1	1	0	V_{126}'	$V_3+(V_2-V_3)$ X 50 / 1600	r126	25.0
7FH	0	1	1	1	1	1	1	1	V_{127}'	$V_3+(V_2-V_3)$ X 25 / 1600	r127	25.0

Caution There is no connection between V_7 and V_8 in the chip.

Figure 5–2. Relationship between Input Data and Output Voltage (3/4)

V_{DD2} – 0.2 V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5 V_{DD2}, POL21/22 = L

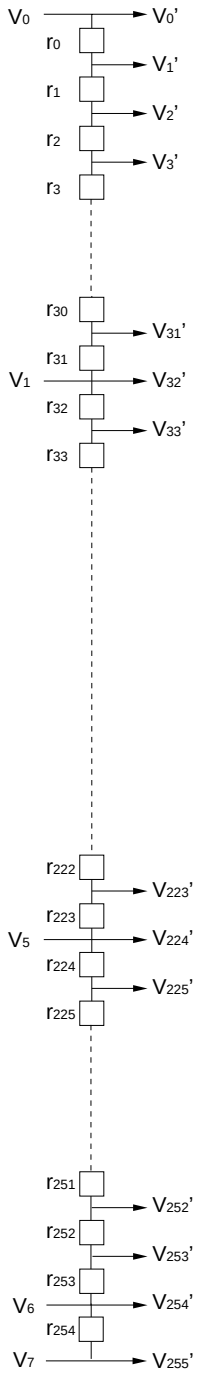


Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
80H	1	0	0	0	0	0	0	0	V_{128}'	V_3	r128	25.0
81H	1	0	0	0	0	0	0	1	V_{129}'	$V_4+(V_3-V_4)$ X 1875.0 / 1900.0	r129	25.0
82H	1	0	0	0	0	0	1	0	V_{130}'	$V_4+(V_3-V_4)$ X 1850.0 / 1900.0	r130	25.0
83H	1	0	0	0	0	0	1	1	V_{131}'	$V_4+(V_3-V_4)$ X 1825.0 / 1900.0	r131	25.0
84H	1	0	0	0	0	1	0	0	V_{132}'	$V_4+(V_3-V_4)$ X 1800.0 / 1900.0	r132	25.0
85H	1	0	0	0	0	1	0	1	V_{133}'	$V_4+(V_3-V_4)$ X 1775.0 / 1900.0	r133	25.0
86H	1	0	0	0	0	1	1	0	V_{134}'	$V_4+(V_3-V_4)$ X 1750.0 / 1900.0	r134	25.0
87H	1	0	0	0	0	1	1	1	V_{135}'	$V_4+(V_3-V_4)$ X 1725.0 / 1900.0	r135	25.0
88H	1	0	0	0	1	0	0	0	V_{136}'	$V_4+(V_3-V_4)$ X 1700.0 / 1900.0	r136	25.0
89H	1	0	0	0	1	0	0	1	V_{137}'	$V_4+(V_3-V_4)$ X 1675.0 / 1900.0	r137	25.0
8AH	1	0	0	0	1	0	1	0	V_{138}'	$V_4+(V_3-V_4)$ X 1650.0 / 1900.0	r138	25.0
8BH	1	0	0	0	1	0	1	1	V_{139}'	$V_4+(V_3-V_4)$ X 1625.0 / 1900.0	r139	25.0
8CH	1	0	0	0	1	1	0	0	V_{140}'	$V_4+(V_3-V_4)$ X 1600.0 / 1900.0	r140	25.0
8DH	1	0	0	0	1	1	0	1	V_{141}'	$V_4+(V_3-V_4)$ X 1575.0 / 1900.0	r141	25.0
8EH	1	0	0	0	1	1	1	0	V_{142}'	$V_4+(V_3-V_4)$ X 1550.0 / 1900.0	r142	25.0
8FH	1	0	0	0	1	1	1	1	V_{143}'	$V_4+(V_3-V_4)$ X 1525.0 / 1900.0	r143	25.0
90H	1	0	0	1	0	0	0	0	V_{144}'	$V_4+(V_3-V_4)$ X 1500.0 / 1900.0	r144	25.0
91H	1	0	0	1	0	0	0	1	V_{145}'	$V_4+(V_3-V_4)$ X 1475.0 / 1900.0	r145	25.0
92H	1	0	0	1	0	0	1	0	V_{146}'	$V_4+(V_3-V_4)$ X 1450.0 / 1900.0	r146	25.0
93H	1	0	0	1	0	0	1	1	V_{147}'	$V_4+(V_3-V_4)$ X 1425.0 / 1900.0	r147	25.0
94H	1	0	0	1	0	1	0	0	V_{148}'	$V_4+(V_3-V_4)$ X 1400.0 / 1900.0	r148	25.0
95H	1	0	0	1	0	1	0	1	V_{149}'	$V_4+(V_3-V_4)$ X 1375.0 / 1900.0	r149	25.0
96H	1	0	0	1	0	1	1	0	V_{150}'	$V_4+(V_3-V_4)$ X 1350.0 / 1900.0	r150	25.0
97H	1	0	0	1	0	1	1	1	V_{151}'	$V_4+(V_3-V_4)$ X 1325.0 / 1900.0	r151	25.0
98H	1	0	0	1	1	0	0	0	V_{152}'	$V_4+(V_3-V_4)$ X 1300.0 / 1900.0	r152	27.5
99H	1	0	0	1	1	0	0	1	V_{153}'	$V_4+(V_3-V_4)$ X 1272.5 / 1900.0	r153	27.5
9AH	1	0	0	1	1	0	1	0	V_{154}'	$V_4+(V_3-V_4)$ X 1245.0 / 1900.0	r154	27.5
9BH	1	0	0	1	1	0	1	1	V_{155}'	$V_4+(V_3-V_4)$ X 1217.5 / 1900.0	r155	27.5
9CH	1	0	0	1	1	1	0	0	V_{156}'	$V_4+(V_3-V_4)$ X 1190.0 / 1900.0	r156	27.5
9DH	1	0	0	1	1	1	0	1	V_{157}'	$V_4+(V_3-V_4)$ X 1162.5 / 1900.0	r157	27.5
9EH	1	0	0	1	1	1	1	0	V_{158}'	$V_4+(V_3-V_4)$ X 1135.0 / 1900.0	r158	27.5
9FH	1	0	0	1	1	1	1	1	V_{159}'	$V_4+(V_3-V_4)$ X 1107.5 / 1900.0	r159	27.5
A0H	1	0	1	0	0	0	0	0	V_{160}'	$V_4+(V_3-V_4)$ X 1080.0 / 1900.0	r160	30.0
A1H	1	0	1	0	0	0	0	1	V_{161}'	$V_4+(V_3-V_4)$ X 1050.0 / 1900.0	r161	30.0
A2H	1	0	1	0	0	0	1	0	V_{162}'	$V_4+(V_3-V_4)$ X 1020.0 / 1900.0	r162	30.0
A3H	1	0	1	0	0	0	1	1	V_{163}'	$V_4+(V_3-V_4)$ X 990.0 / 1900.0	r163	30.0
A4H	1	0	1	0	0	1	0	0	V_{164}'	$V_4+(V_3-V_4)$ X 960.0 / 1900.0	r164	30.0
A5H	1	0	1	0	0	1	0	1	V_{165}'	$V_4+(V_3-V_4)$ X 930.0 / 1900.0	r165	30.0
A6H	1	0	1	0	0	1	1	0	V_{166}'	$V_4+(V_3-V_4)$ X 900.0 / 1900.0	r166	30.0
A7H	1	0	1	0	0	1	1	1	V_{167}'	$V_4+(V_3-V_4)$ X 870.0 / 1900.0	r167	30.0
A8H	1	0	1	0	1	0	0	0	V_{168}'	$V_4+(V_3-V_4)$ X 840.0 / 1900.0	r168	32.5
A9H	1	0	1	0	1	0	0	1	V_{169}'	$V_4+(V_3-V_4)$ X 807.5 / 1900.0	r169	32.5
AAH	1	0	1	0	1	0	1	0	V_{170}'	$V_4+(V_3-V_4)$ X 775.0 / 1900.0	r170	32.5
ABH	1	0	1	0	1	0	1	1	V_{171}'	$V_4+(V_3-V_4)$ X 742.5 / 1900.0	r171	32.5
ACH	1	0	1	0	1	1	0	0	V_{172}'	$V_4+(V_3-V_4)$ X 710.0 / 1900.0	r172	32.5
ADH	1	0	1	0	1	1	0	1	V_{173}'	$V_4+(V_3-V_4)$ X 677.5 / 1900.0	r173	32.5
AEH	1	0	1	0	1	1	1	0	V_{174}'	$V_4+(V_3-V_4)$ X 645.0 / 1900.0	r174	32.5
AFH	1	0	1	0	1	1	1	1	V_{175}'	$V_4+(V_3-V_4)$ X 612.5 / 1900.0	r175	32.5
B0H	1	0	1	1	0	0	0	0	V_{176}'	$V_4+(V_3-V_4)$ X 580.0 / 1900.0	r176	35.0
B1H	1	0	1	1	0	0	0	1	V_{177}'	$V_4+(V_3-V_4)$ X 545.0 / 1900.0	r177	35.0
B2H	1	0	1	1	0	0	1	0	V_{178}'	$V_4+(V_3-V_4)$ X 510.0 / 1900.0	r178	35.0
B3H	1	0	1	1	0	0	1	1	V_{179}'	$V_4+(V_3-V_4)$ X 475.0 / 1900.0	r179	35.0
B4H	1	0	1	1	0	1	0	0	V_{180}'	$V_4+(V_3-V_4)$ X 440.0 / 1900.0	r180	35.0
B5H	1	0	1	1	0	1	0	1	V_{181}'	$V_4+(V_3-V_4)$ X 405.0 / 1900.0	r181	35.0
B6H	1	0	1	1	0	1	1	0	V_{182}'	$V_4+(V_3-V_4)$ X 370.0 / 1900.0	r182	35.0
B7H	1	0	1	1	0	1	1	1	V_{183}'	$V_4+(V_3-V_4)$ X 335.0 / 1900.0	r183	35.0
B8H	1	0	1	1	1	0	0	0	V_{184}'	$V_4+(V_3-V_4)$ X 300.0 / 1900.0	r184	37.5
B9H	1	0	1	1	1	0	0	1	V_{185}'	$V_4+(V_3-V_4)$ X 262.5 / 1900.0	r185	37.5
BAH	1	0	1	1	1	0	1	0	V_{186}'	$V_4+(V_3-V_4)$ X 225.0 / 1900.0	r186	37.5
BBH	1	0	1	1	1	0	1	1	V_{187}'	$V_4+(V_3-V_4)$ X 187.5 / 1900.0	r187	37.5
BCH	1	0	1	1	1	1	0	0	V_{188}'	$V_4+(V_3-V_4)$ X 150.0 / 1900.0	r188	37.5
BDH	1	0	1	1	1	1	0	1	V_{189}'	$V_4+(V_3-V_4)$ X 112.5 / 1900.0	r189	37.5
BEH	1	0	1	1	1	1	1	0	V_{190}'	$V_4+(V_3-V_4)$ X 75.0 / 1900.0	r190	37.5
BFH	1	0	1	1	1	1	1	1	V_{191}'	$V_4+(V_3-V_4)$ X 37.5 / 1900.0	r191	37.5

Caution There is no connection between V_7 and V_8 in the chip.

Figure 5–2. Relationship between Input Data and Output Voltage (4/4)

V_{DD2} – 0.2 V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5 V_{DD2}

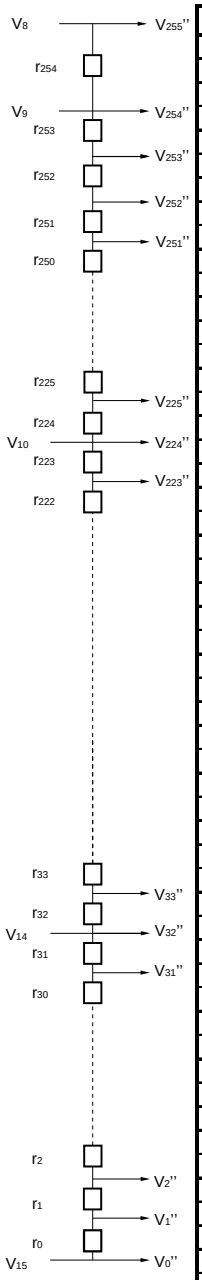


Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage					rn	(Ω)
C0H	1	1	0	0	0	0	0	0	V_{192}'	V_4				r192	42.5
C1H	1	1	0	0	0	0	0	1	V_{193}'	V_5+(V_4-V_5) X	1557.5	/	1600.0	r193	42.5
C2H	1	1	0	0	0	0	1	0	V_{194}'	V_5+(V_4-V_5) X	1515.0	/	1600.0	r194	42.5
C3H	1	1	0	0	0	0	1	1	V_{195}'	V_5+(V_4-V_5) X	1472.5	/	1600.0	r195	42.5
C4H	1	1	0	0	0	1	0	0	V_{196}'	V_5+(V_4-V_5) X	1430.0	/	1600.0	r196	42.5
C5H	1	1	0	0	0	1	0	1	V_{197}'	V_5+(V_4-V_5) X	1387.5	/	1600.0	r197	42.5
C6H	1	1	0	0	0	1	1	0	V_{198}'	V_5+(V_4-V_5) X	1345.0	/	1600.0	r198	42.5
C7H	1	1	0	0	0	1	1	1	V_{199}'	V_5+(V_4-V_5) X	1302.5	/	1600.0	r199	42.5
C8H	1	1	0	0	1	0	0	0	V_{200}'	V_5+(V_4-V_5) X	1260.0	/	1600.0	r200	47.5
C9H	1	1	0	0	1	0	0	1	V_{201}'	V_5+(V_4-V_5) X	1212.5	/	1600.0	r201	47.5
CAH	1	1	0	0	1	0	1	0	V_{202}'	V_5+(V_4-V_5) X	1165.0	/	1600.0	r202	47.5
CBH	1	1	0	0	1	0	1	1	V_{203}'	V_5+(V_4-V_5) X	1117.5	/	1600.0	r203	47.5
CCH	1	1	0	0	1	1	0	0	V_{204}'	V_5+(V_4-V_5) X	1070.0	/	1600.0	r204	47.5
CDH	1	1	0	0	1	1	0	1	V_{205}'	V_5+(V_4-V_5) X	1022.5	/	1600.0	r205	47.5
CEH	1	1	0	0	1	1	1	0	V_{206}'	V_5+(V_4-V_5) X	975.0	/	1600.0	r206	47.5
CFH	1	1	0	0	1	1	1	1	V_{207}'	V_5+(V_4-V_5) X	927.5	/	1600.0	r207	47.5
D0H	1	1	0	1	0	0	0	0	V_{208}'	V_5+(V_4-V_5) X	880.0	/	1600.0	r208	52.5
D1H	1	1	0	1	0	0	0	1	V_{209}'	V_5+(V_4-V_5) X	827.5	/	1600.0	r209	52.5
D2H	1	1	0	1	0	0	1	0	V_{210}'	V_5+(V_4-V_5) X	775.0	/	1600.0	r210	52.5
D3H	1	1	0	1	0	0	1	1	V_{211}'	V_5+(V_4-V_5) X	722.5	/	1600.0	r211	52.5
D4H	1	1	0	1	0	1	0	0	V_{212}'	V_5+(V_4-V_5) X	670.0	/	1600.0	r212	52.5
D5H	1	1	0	1	0	1	0	1	V_{213}'	V_5+(V_4-V_5) X	617.5	/	1600.0	r213	52.5
D6H	1	1	0	1	0	1	1	0	V_{214}'	V_5+(V_4-V_5) X	565.0	/	1600.0	r214	52.5
D7H	1	1	0	1	0	1	1	1	V_{215}'	V_5+(V_4-V_5) X	512.5	/	1600.0	r215	52.5
D8H	1	1	0	1	1	0	0	0	V_{216}'	V_5+(V_4-V_5) X	460.0	/	1600.0	r216	57.5
D9H	1	1	0	1	1	0	0	1	V_{217}'	V_5+(V_4-V_5) X	402.5	/	1600.0	r217	57.5
DAH	1	1	0	1	1	0	1	0	V_{218}'	V_5+(V_4-V_5) X	345.0	/	1600.0	r218	57.5
DBH	1	1	0	1	1	0	1	1	V_{219}'	V_5+(V_4-V_5) X	287.5	/	1600.0	r219	57.5
DCH	1	1	0	1	1	1	0	0	V_{220}'	V_5+(V_4-V_5) X	230.0	/	1600.0	r220	57.5
DDH	1	1	0	1	1	1	0	1	V_{221}'	V_5+(V_4-V_5) X	172.5	/	1600.0	r221	57.5
DEH	1	1	0	1	1	1	1	0	V_{222}'	V_5+(V_4-V_5) X	115.0	/	1600.0	r222	57.5
DFH	1	1	0	1	1	1	1	1	V_{223}'	V_5+(V_4-V_5) X	57.5	/	1600.0	r223	57.5
E0H	1	1	1	0	0	0	0	0	V_{224}'	V_5				r224	57.5
E1H	1	1	1	0	0	0	0	1	V_{225}'	V_6+(V_5-V_6) X	4630.0	/	4687.5	r225	70.0
E2H	1	1	1	0	0	0	1	0	V_{226}'	V_6+(V_5-V_6) X	4560.0	/	4687.5	r226	70.0
E3H	1	1	1	0	0	0	1	1	V_{227}'	V_6+(V_5-V_6) X	4490.0	/	4687.5	r227	70.0
E4H	1	1	1	0	0	1	0	0	V_{228}'	V_6+(V_5-V_6) X	4420.0	/	4687.5	r228	82.5
E5H	1	1	1	0	0	1	0	1	V_{229}'	V_6+(V_5-V_6) X	4337.5	/	4687.5	r229	82.5
E6H	1	1	1	0	0	1	1	0	V_{230}'	V_6+(V_5-V_6) X	4255.0	/	4687.5	r230	82.5
E7H	1	1	1	0	0	1	1	1	V_{231}'	V_6+(V_5-V_6) X	4172.5	/	4687.5	r231	95.0
E8H	1	1	1	0	1	0	0	0	V_{232}'	V_6+(V_5-V_6) X	4077.5	/	4687.5	r232	95.0
E9H	1	1	1	0	1	0	0	1	V_{233}'	V_6+(V_5-V_6) X	3982.5	/	4687.5	r233	95.0
EAH	1	1	1	0	1	0	1	0	V_{234}'	V_6+(V_5-V_6) X	3887.5	/	4687.5	r234	112.5
EBH	1	1	1	0	1	0	1	1	V_{235}'	V_6+(V_5-V_6) X	3775.0	/	4687.5	r235	112.5
ECH	1	1	1	0	1	1	0	0	V_{236}'	V_6+(V_5-V_6) X	3662.5	/	4687.5	r236	112.5
EDH	1	1	1	0	1	1	0	1	V_{237}'	V_6+(V_5-V_6) X	3550.0	/	4687.5	r237	130.0
EEH	1	1	1	0	1	1	1	0	V_{238}'	V_6+(V_5-V_6) X	3420.0	/	4687.5	r238	130.0
EFH	1	1	1	0	1	1	1	1	V_{239}'	V_6+(V_5-V_6) X	3290.0	/	4687.5	r239	147.5
F0H	1	1	1	1	0	0	0	0	V_{240}'	V_6+(V_5-V_6) X	3142.5	/	4687.5	r240	147.5
F1H	1	1	1	1	0	0	0	1	V_{241}'	V_6+(V_5-V_6) X	2995.0	/	4687.5	r241	165.0
F2H	1	1	1	1	0	0	1	0	V_{242}'	V_6+(V_5-V_6) X	2830.0	/	4687.5	r242	165.0
F3H	1	1	1	1	0	0	1	1	V_{243}'	V_6+(V_5-V_6) X	2665.0	/	4687.5	r243	182.5
F4H	1	1	1	1	0	1	0	0	V_{244}'	V_6+(V_5-V_6) X	2482.5	/	4687.5	r244	182.5
F5H	1	1	1	1	0	1	0	1	V_{245}'	V_6+(V_5-V_6) X	2300.0	/	4687.5	r245	200.0
F6H	1	1	1	1	0	1	1	0	V_{246}'	V_6+(V_5-V_6) X	2100.0	/	4687.5	r246	200.0
F7H	1	1	1	1	0	1	1	1	V_{247}'	V_6+(V_5-V_6) X	1900.0	/	4687.5	r247	225.0
F8H	1	1	1	1	1	0	0	0	V_{248}'	V_6+(V_5-V_6) X	1675.0	/	4687.5	r248	225.0
F9H	1	1	1	1	1	0	0	1	V_{249}'	V_6+(V_5-V_6) X	1450.0	/	4687.5	r249	250.0
FAH	1	1	1	1	1	0	1	0	V_{250}'	V_6+(V_5-V_6) X	1200.0	/	4687.5	r250	250.0
FBH	1	1	1	1	1	0	1	1	V_{251}'	V_6+(V_5-V_6) X	950.0	/	4687.5	r251	300.0
FCH	1	1	1	1	1	1	0	0	V_{252}'	V_6+(V_5-V_6) X	650.0	/	4687.5	r252	300.0
FDH	1	1	1	1	1	1	0	1	V_{253}'	V_6+(V_5-V_6) X	350.0	/	4687.5	r253	350.0
FEH	1	1	1	1	1	1	1	0	V_{254}'	V_6				r254	350.0
FFH	1	1	1	1	1	1	1	1	V_{255}'	V_7				TOTAL	15002.5

Caution There is no connection between V_7 and V_8 in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (1/4)

0.5 V_{DD2} – 0.3 V > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.2 V, POL21/22 = L

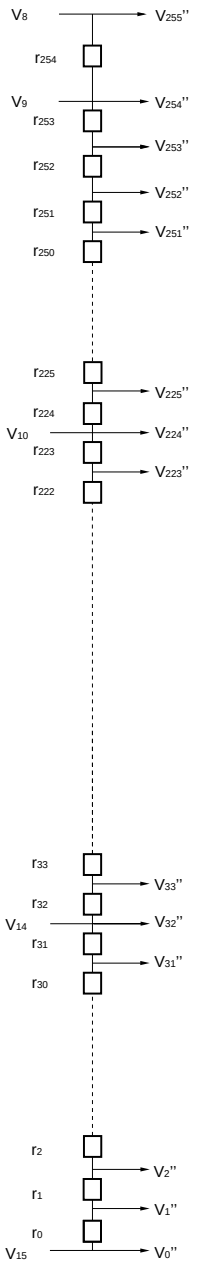


Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
00H	0	0	0	0	0	0	0	0	V_0"	V_{15}	r0	400.0
01H	0	0	0	0	0	0	0	1	V_1"	$V_{15}+(V_{14}-V_{15})$ X 400.0 / 3865	r1	362.5
02H	0	0	0	0	0	0	1	0	V_2"	$V_{15}+(V_{14}-V_{15})$ X 762.5 / 3865	r2	325.0
03H	0	0	0	0	0	0	1	1	V_3"	$V_{15}+(V_{14}-V_{15})$ X 1087.5 / 3865	r3	287.5
04H	0	0	0	0	0	1	0	0	V_4"	$V_{15}+(V_{14}-V_{15})$ X 1375.0 / 3865	r4	250.0
05H	0	0	0	0	0	1	0	1	V_5"	$V_{15}+(V_{14}-V_{15})$ X 1625.0 / 3865	r5	222.5
06H	0	0	0	0	0	1	1	0	V_6"	$V_{15}+(V_{14}-V_{15})$ X 1847.5 / 3865	r6	195.0
07H	0	0	0	0	0	1	1	1	V_7"	$V_{15}+(V_{14}-V_{15})$ X 2042.5 / 3865	r7	170.0
08H	0	0	0	0	1	0	0	0	V_8"	$V_{15}+(V_{14}-V_{15})$ X 2212.5 / 3865	r8	145.0
09H	0	0	0	0	1	0	0	1	V_9"	$V_{15}+(V_{14}-V_{15})$ X 2357.5 / 3865	r9	120.0
0AH	0	0	0	0	1	0	1	0	V_{10}"	$V_{15}+(V_{14}-V_{15})$ X 2477.5 / 3865	r10	120.0
0BH	0	0	0	0	1	0	1	1	V_{11}"	$V_{15}+(V_{14}-V_{15})$ X 2597.5 / 3865	r11	120.0
0CH	0	0	0	0	1	1	0	0	V_{12}"	$V_{15}+(V_{14}-V_{15})$ X 2717.5 / 3865	r12	95.0
0DH	0	0	0	0	1	1	0	1	V_{13}"	$V_{15}+(V_{14}-V_{15})$ X 2812.5 / 3865	r13	95.0
0EH	0	0	0	0	1	1	1	0	V_{14}"	$V_{15}+(V_{14}-V_{15})$ X 2907.5 / 3865	r14	95.0
0FH	0	0	0	0	1	1	1	1	V_{15}"	$V_{15}+(V_{14}-V_{15})$ X 3002.5 / 3865	r15	75.0
10H	0	0	0	1	0	0	0	0	V_{16}"	$V_{15}+(V_{14}-V_{15})$ X 3077.5 / 3865	r16	75.0
11H	0	0	0	1	0	0	0	1	V_{17}"	$V_{15}+(V_{14}-V_{15})$ X 3152.5 / 3865	r17	75.0
12H	0	0	0	1	0	0	1	0	V_{18}"	$V_{15}+(V_{14}-V_{15})$ X 3227.5 / 3865	r18	62.5
13H	0	0	0	1	0	0	1	1	V_{19}"	$V_{15}+(V_{14}-V_{15})$ X 3290.0 / 3865	r19	62.5
14H	0	0	0	1	0	1	0	0	V_{20}"	$V_{15}+(V_{14}-V_{15})$ X 3352.5 / 3865	r20	62.5
15H	0	0	0	1	0	1	0	1	V_{21}"	$V_{15}+(V_{14}-V_{15})$ X 3415.0 / 3865	r21	50.0
16H	0	0	0	1	0	1	1	0	V_{22}"	$V_{15}+(V_{14}-V_{15})$ X 3465.0 / 3865	r22	50.0
17H	0	0	0	1	0	1	1	1	V_{23}"	$V_{15}+(V_{14}-V_{15})$ X 3515.0 / 3865	r23	50.0
18H	0	0	0	1	1	0	0	0	V_{24}"	$V_{15}+(V_{14}-V_{15})$ X 3565.0 / 3865	r24	37.5
19H	0	0	0	1	1	0	0	1	V_{25}"	$V_{15}+(V_{14}-V_{15})$ X 3602.5 / 3865	r25	37.5
1AH	0	0	0	1	1	0	1	0	V_{26}"	$V_{15}+(V_{14}-V_{15})$ X 3640.0 / 3865	r26	37.5
1BH	0	0	0	1	1	0	1	1	V_{27}"	$V_{15}+(V_{14}-V_{15})$ X 3677.5 / 3865	r27	37.5
1CH	0	0	0	1	1	1	0	0	V_{28}"	$V_{15}+(V_{14}-V_{15})$ X 3715.0 / 3865	r28	37.5
1DH	0	0	0	1	1	1	0	1	V_{29}"	$V_{15}+(V_{14}-V_{15})$ X 3752.5 / 3865	r29	37.5
1EH	0	0	0	1	1	1	1	0	V_{30}"	$V_{15}+(V_{14}-V_{15})$ X 3790.0 / 3865	r30	37.5
1FH	0	0	0	1	1	1	1	1	V_{31}"	$V_{15}+(V_{14}-V_{15})$ X 3827.5 / 3865	r31	37.5
20H	0	0	1	0	0	0	0	0	V_{32}"	V_{14}	r32	35.0
21H	0	0	1	0	0	0	0	1	V_{33}"	$V_{14}+(V_{13}-V_{14})$ X 35.0 / 1000	r33	35.0
22H	0	0	1	0	0	0	1	0	V_{34}"	$V_{14}+(V_{13}-V_{14})$ X 70.0 / 1000	r34	35.0
23H	0	0	1	0	0	0	1	1	V_{35}"	$V_{14}+(V_{13}-V_{14})$ X 105.0 / 1000	r35	35.0
24H	0	0	1	0	0	1	0	0	V_{36}"	$V_{14}+(V_{13}-V_{14})$ X 140.0 / 1000	r36	35.0
25H	0	0	1	0	0	1	0	1	V_{37}"	$V_{14}+(V_{13}-V_{14})$ X 175.0 / 1000	r37	35.0
26H	0	0	1	0	0	1	1	0	V_{38}"	$V_{14}+(V_{13}-V_{14})$ X 210.0 / 1000	r38	35.0
27H	0	0	1	0	0	1	1	1	V_{39}"	$V_{14}+(V_{13}-V_{14})$ X 245.0 / 1000	r39	35.0
28H	0	0	1	0	1	0	0	0	V_{40}"	$V_{14}+(V_{13}-V_{14})$ X 280.0 / 1000	r40	32.5
29H	0	0	1	0	1	0	0	1	V_{41}"	$V_{14}+(V_{13}-V_{14})$ X 312.5 / 1000	r41	32.5
2AH	0	0	1	0	1	0	1	0	V_{42}"	$V_{14}+(V_{13}-V_{14})$ X 345.0 / 1000	r42	32.5
2BH	0	0	1	0	1	0	1	1	V_{43}"	$V_{14}+(V_{13}-V_{14})$ X 377.5 / 1000	r43	32.5
2CH	0	0	1	0	1	1	0	0	V_{44}"	$V_{14}+(V_{13}-V_{14})$ X 410.0 / 1000	r44	32.5
2DH	0	0	1	0	1	1	0	1	V_{45}"	$V_{14}+(V_{13}-V_{14})$ X 442.5 / 1000	r45	32.5
2EH	0	0	1	0	1	1	1	0	V_{46}"	$V_{14}+(V_{13}-V_{14})$ X 475.0 / 1000	r46	32.5
2FH	0	0	1	0	1	1	1	1	V_{47}"	$V_{14}+(V_{13}-V_{14})$ X 507.5 / 1000	r47	32.5
30H	0	0	1	1	0	0	0	0	V_{48}"	$V_{14}+(V_{13}-V_{14})$ X 540.0 / 1000	r48	30.0
31H	0	0	1	1	0	0	0	1	V_{49}"	$V_{14}+(V_{13}-V_{14})$ X 570.0 / 1000	r49	30.0
32H	0	0	1	1	0	0	1	0	V_{50}"	$V_{14}+(V_{13}-V_{14})$ X 600.0 / 1000	r50	30.0
33H	0	0	1	1	0	0	1	1	V_{51}"	$V_{14}+(V_{13}-V_{14})$ X 630.0 / 1000	r51	30.0
34H	0	0	1	1	0	1	0	0	V_{52}"	$V_{14}+(V_{13}-V_{14})$ X 660.0 / 1000	r52	30.0
35H	0	0	1	1	0	1	0	1	V_{53}"	$V_{14}+(V_{13}-V_{14})$ X 690.0 / 1000	r53	30.0
36H	0	0	1	1	0	1	1	0	V_{54}"	$V_{14}+(V_{13}-V_{14})$ X 720.0 / 1000	r54	30.0
37H	0	0	1	1	0	1	1	1	V_{55}"	$V_{14}+(V_{13}-V_{14})$ X 750.0 / 1000	r55	30.0
38H	0	0	1	1	1	0	0	0	V_{56}"	$V_{14}+(V_{13}-V_{14})$ X 780.0 / 1000	r56	27.5
39H	0	0	1	1	1	0	0	1	V_{57}"	$V_{14}+(V_{13}-V_{14})$ X 807.5 / 1000	r57	27.5
3AH	0	0	1	1	1	0	1	0	V_{58}"	$V_{14}+(V_{13}-V_{14})$ X 835.0 / 1000	r58	27.5
3BH	0	0	1	1	1	0	1	1	V_{59}"	$V_{14}+(V_{13}-V_{14})$ X 862.5 / 1000	r59	27.5
3CH	0	0	1	1	1	1	0	0	V_{60}"	$V_{14}+(V_{13}-V_{14})$ X 890.0 / 1000	r60	27.5
3DH	0	0	1	1	1	1	0	1	V_{61}"	$V_{14}+(V_{13}-V_{14})$ X 917.5 / 1000	r61	27.5
3EH	0	0	1	1	1	1	1	0	V_{62}"	$V_{14}+(V_{13}-V_{14})$ X 945.0 / 1000	r62	27.5
3FH	0	0	1	1	1	1	1	1	V_{63}"	$V_{14}+(V_{13}-V_{14})$ X 972.5 / 1000	r63	27.5

Caution There is no connection between V_7 and V_8 in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (2/4)

0.5 V_{DD2} – 0.3 V > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.2 V, POL21/22 = L

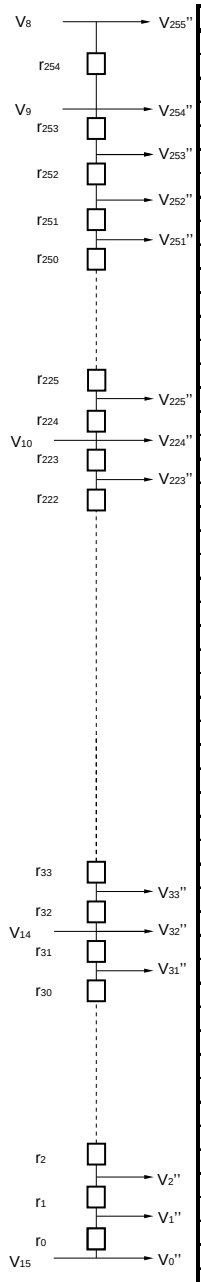


Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage					rn	(Ω)
40H	0	1	0	0	0	0	0	0	V_{64}''	V_{13}				r64	25.0
41H	0	1	0	0	0	0	0	1	V_{65}''	$V_{13}+(V_{12}-V_{13})$ X	25	/	1600	r65	25.0
42H	0	1	0	0	0	0	1	0	V_{66}''	$V_{13}+(V_{12}-V_{13})$ X	50	/	1600	r66	25.0
43H	0	1	0	0	0	0	1	1	V_{67}''	$V_{13}+(V_{12}-V_{13})$ X	75	/	1600	r67	25.0
44H	0	1	0	0	0	1	0	0	V_{68}''	$V_{13}+(V_{12}-V_{13})$ X	100	/	1600	r68	25.0
45H	0	1	0	0	0	1	0	1	V_{69}''	$V_{13}+(V_{12}-V_{13})$ X	125	/	1600	r69	25.0
46H	0	1	0	0	0	1	1	0	V_{70}''	$V_{13}+(V_{12}-V_{13})$ X	150	/	1600	r70	25.0
47H	0	1	0	0	0	1	1	1	V_{71}''	$V_{13}+(V_{12}-V_{13})$ X	175	/	1600	r71	25.0
48H	0	1	0	0	1	0	0	0	V_{72}''	$V_{13}+(V_{12}-V_{13})$ X	200	/	1600	r72	25.0
49H	0	1	0	0	1	0	0	1	V_{73}''	$V_{13}+(V_{12}-V_{13})$ X	225	/	1600	r73	25.0
4AH	0	1	0	0	1	0	1	0	V_{74}''	$V_{13}+(V_{12}-V_{13})$ X	250	/	1600	r74	25.0
4BH	0	1	0	0	1	0	1	1	V_{75}''	$V_{13}+(V_{12}-V_{13})$ X	275	/	1600	r75	25.0
4CH	0	1	0	0	1	1	0	0	V_{76}''	$V_{13}+(V_{12}-V_{13})$ X	300	/	1600	r76	25.0
4DH	0	1	0	0	1	1	0	1	V_{77}''	$V_{13}+(V_{12}-V_{13})$ X	325	/	1600	r77	25.0
4EH	0	1	0	0	1	1	1	0	V_{78}''	$V_{13}+(V_{12}-V_{13})$ X	350	/	1600	r78	25.0
4FH	0	1	0	0	1	1	1	1	V_{79}''	$V_{13}+(V_{12}-V_{13})$ X	375	/	1600	r79	25.0
50H	0	1	0	1	0	0	0	0	V_{80}''	$V_{13}+(V_{12}-V_{13})$ X	400	/	1600	r80	25.0
51H	0	1	0	1	0	0	0	1	V_{81}''	$V_{13}+(V_{12}-V_{13})$ X	425	/	1600	r81	25.0
52H	0	1	0	1	0	0	1	0	V_{82}''	$V_{13}+(V_{12}-V_{13})$ X	450	/	1600	r82	25.0
53H	0	1	0	1	0	0	1	1	V_{83}''	$V_{13}+(V_{12}-V_{13})$ X	475	/	1600	r83	25.0
54H	0	1	0	1	0	1	0	0	V_{84}''	$V_{13}+(V_{12}-V_{13})$ X	500	/	1600	r84	25.0
55H	0	1	0	1	0	1	0	1	V_{85}''	$V_{13}+(V_{12}-V_{13})$ X	525	/	1600	r85	25.0
56H	0	1	0	1	0	1	1	0	V_{86}''	$V_{13}+(V_{12}-V_{13})$ X	550	/	1600	r86	25.0
57H	0	1	0	1	0	1	1	1	V_{87}''	$V_{13}+(V_{12}-V_{13})$ X	575	/	1600	r87	25.0
58H	0	1	0	1	1	0	0	0	V_{88}''	$V_{13}+(V_{12}-V_{13})$ X	600	/	1600	r88	25.0
59H	0	1	0	1	1	0	0	1	V_{89}''	$V_{13}+(V_{12}-V_{13})$ X	625	/	1600	r89	25.0
5AH	0	1	0	1	1	0	1	0	V_{90}''	$V_{13}+(V_{12}-V_{13})$ X	650	/	1600	r90	25.0
5BH	0	1	0	1	1	0	1	1	V_{91}''	$V_{13}+(V_{12}-V_{13})$ X	675	/	1600	r91	25.0
5CH	0	1	0	1	1	1	0	0	V_{92}''	$V_{13}+(V_{12}-V_{13})$ X	700	/	1600	r92	25.0
5DH	0	1	0	1	1	1	0	1	V_{93}''	$V_{13}+(V_{12}-V_{13})$ X	725	/	1600	r93	25.0
5EH	0	1	0	1	1	1	1	0	V_{94}''	$V_{13}+(V_{12}-V_{13})$ X	750	/	1600	r94	25.0
5FH	0	1	0	1	1	1	1	1	V_{95}''	$V_{13}+(V_{12}-V_{13})$ X	775	/	1600	r95	25.0
60H	0	1	1	0	0	0	0	0	V_{96}''	$V_{13}+(V_{12}-V_{13})$ X	800		1600	r96	25.0
61H	0	1	1	0	0	0	0	1	V_{97}''	$V_{13}+(V_{12}-V_{13})$ X	825	/	1600	r97	25.0
62H	0	1	1	0	0	0	1	0	V_{98}''	$V_{13}+(V_{12}-V_{13})$ X	850	/	1600	r98	25.0
63H	0	1	1	0	0	0	1	1	V_{99}''	$V_{13}+(V_{12}-V_{13})$ X	875	/	1600	r99	25.0
64H	0	1	1	0	0	1	0	0	V_{100}''	$V_{13}+(V_{12}-V_{13})$ X	900	/	1600	r100	25.0
65H	0	1	1	0	0	1	0	1	V_{101}''	$V_{13}+(V_{12}-V_{13})$ X	925	/	1600	r101	25.0
66H	0	1	1	0	0	1	1	0	V_{102}''	$V_{13}+(V_{12}-V_{13})$ X	950	/	1600	r102	25.0
67H	0	1	1	0	0	1	1	1	V_{103}''	$V_{13}+(V_{12}-V_{13})$ X	975	/	1600	r103	25.0
68H	0	1	1	0	1	0	0	0	V_{104}''	$V_{13}+(V_{12}-V_{13})$ X	1000	/	1600	r104	25.0
69H	0	1	1	0	1	0	0	1	V_{105}''	$V_{13}+(V_{12}-V_{13})$ X	1025	/	1600	r105	25.0
6AH	0	1	1	0	1	0	1	0	V_{106}''	$V_{13}+(V_{12}-V_{13})$ X	1050	/	1600	r106	25.0
6BH	0	1	1	0	1	0	1	1	V_{107}''	$V_{13}+(V_{12}-V_{13})$ X	1075	/	1600	r107	25.0
6CH	0	1	1	0	1	1	0	0	V_{108}''	$V_{13}+(V_{12}-V_{13})$ X	1100	/	1600	r108	25.0
6DH	0	1	1	0	1	1	0	1	V_{109}''	$V_{13}+(V_{12}-V_{13})$ X	1125	/	1600	r109	25.0
6EH	0	1	1	0	1	1	1	0	V_{110}''	$V_{13}+(V_{12}-V_{13})$ X	1150	/	1600	r110	25.0
6FH	0	1	1	0	1	1	1	1	V_{111}''	$V_{13}+(V_{12}-V_{13})$ X	1175	/	1600	r111	25.0
70H	0	1	1	1	0	0	0	0	V_{112}''	$V_{13}+(V_{12}-V_{13})$ X	1200	/	1600	r112	25.0
71H	0	1	1	1	0	0	0	1	V_{113}''	$V_{13}+(V_{12}-V_{13})$ X	1225	/	1600	r113	25.0
72H	0	1	1	1	0	0	1	0	V_{114}''	$V_{13}+(V_{12}-V_{13})$ X	1250	/	1600	r114	25.0
73H	0	1	1	1	0	0	1	1	V_{115}''	$V_{13}+(V_{12}-V_{13})$ X	1275	/	1600	r115	25.0
74H	0	1	1	1	0	1	0	0	V_{116}''	$V_{13}+(V_{12}-V_{13})$ X	1300	/	1600	r116	25.0
75H	0	1	1	1	0	1	0	1	V_{117}''	$V_{13}+(V_{12}-V_{13})$ X	1325	/	1600	r117	25.0
76H	0	1	1	1	0	1	1	0	V_{118}''	$V_{13}+(V_{12}-V_{13})$ X	1350	/	1600	r118	25.0
77H	0	1	1	1	0	1	1	1	V_{119}''	$V_{13}+(V_{12}-V_{13})$ X	1375	/	1600	r119	25.0
78H	0	1	1	1	1	0	0	0	V_{120}''	$V_{13}+(V_{12}-V_{13})$ X	1400	/	1600	r120	25.0
79H	0	1	1	1	1	0	0	1	V_{121}''	$V_{13}+(V_{12}-V_{13})$ X	1425	/	1600	r121	25.0
7AH	0	1	1	1	1	0	1	0	V_{122}''	$V_{13}+(V_{12}-V_{13})$ X	1450	/	1600	r122	25.0
7BH	0	1	1	1	1	0	1	1	V_{123}''	$V_{13}+(V_{12}-V_{13})$ X	1475	/	1600	r123	25.0
7CH	0	1	1	1	1	1	0	0	V_{124}''	$V_{13}+(V_{12}-V_{13})$ X	1500	/	1600	r124	25.0
7DH	0	1	1	1	1	1	0	1	V_{125}''	$V_{13}+(V_{12}-V_{13})$ X	1525	/	1600	r125	25.0
7EH	0	1	1	1	1	1	1	0	V_{126}''	$V_{13}+(V_{12}-V_{13})$ X	1550	/	1600	r126	25.0
7FH	0	1	1	1	1	1	1	1	V_{127}''	$V_{13}+(V_{12}-V_{13})$ X	1575	/	1600	r127	25.0

Caution There is no connection between V_7 and V_8 in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (3/4)

0.5 V_{DD2} – 0.3 V > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.2 V, POL21/22 = L

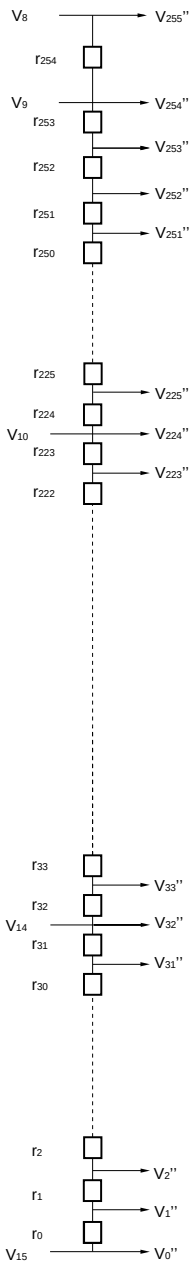


Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
80H	1	0	0	0	0	0	0	0	V_{128}''	V_{12}	r128	25.0
81H	1	0	0	0	0	0	0	1	V_{129}''	$V_{12}+(V_{11}-V_{12})$ X 25.0 / 1900.0	r129	25.0
82H	1	0	0	0	0	0	1	0	V_{130}''	$V_{12}+(V_{11}-V_{12})$ X 50.0 / 1900.0	r130	25.0
83H	1	0	0	0	0	0	1	1	V_{131}''	$V_{12}+(V_{11}-V_{12})$ X 75.0 / 1900.0	r131	25.0
84H	1	0	0	0	0	1	0	0	V_{132}''	$V_{12}+(V_{11}-V_{12})$ X 100.0 / 1900.0	r132	25.0
85H	1	0	0	0	0	1	0	1	V_{133}''	$V_{12}+(V_{11}-V_{12})$ X 125.0 / 1900.0	r133	25.0
86H	1	0	0	0	0	1	1	0	V_{134}''	$V_{12}+(V_{11}-V_{12})$ X 150.0 / 1900.0	r134	25.0
87H	1	0	0	0	0	1	1	1	V_{135}''	$V_{12}+(V_{11}-V_{12})$ X 175.0 / 1900.0	r135	25.0
88H	1	0	0	0	1	0	0	0	V_{136}''	$V_{12}+(V_{11}-V_{12})$ X 200.0 / 1900.0	r136	25.0
89H	1	0	0	0	1	0	0	1	V_{137}''	$V_{12}+(V_{11}-V_{12})$ X 225.0 / 1900.0	r137	25.0
8AH	1	0	0	0	1	0	1	0	V_{138}''	$V_{12}+(V_{11}-V_{12})$ X 250.0 / 1900.0	r138	25.0
8BH	1	0	0	0	1	0	1	1	V_{139}''	$V_{12}+(V_{11}-V_{12})$ X 275.0 / 1900.0	r139	25.0
8CH	1	0	0	0	1	1	0	0	V_{140}''	$V_{12}+(V_{11}-V_{12})$ X 300.0 / 1900.0	r140	25.0
8DH	1	0	0	0	1	1	0	1	V_{141}''	$V_{12}+(V_{11}-V_{12})$ X 325.0 / 1900.0	r141	25.0
8EH	1	0	0	0	1	1	1	0	V_{142}''	$V_{12}+(V_{11}-V_{12})$ X 350.0 / 1900.0	r142	25.0
8FH	1	0	0	0	1	1	1	1	V_{143}''	$V_{12}+(V_{11}-V_{12})$ X 375.0 / 1900.0	r143	25.0
90H	1	0	0	1	0	0	0	0	V_{144}''	$V_{12}+(V_{11}-V_{12})$ X 400.0 / 1900.0	r144	25.0
91H	1	0	0	1	0	0	0	1	V_{145}''	$V_{12}+(V_{11}-V_{12})$ X 425.0 / 1900.0	r145	25.0
92H	1	0	0	1	0	0	1	0	V_{146}''	$V_{12}+(V_{11}-V_{12})$ X 450.0 / 1900.0	r146	25.0
93H	1	0	0	1	0	0	1	1	V_{147}''	$V_{12}+(V_{11}-V_{12})$ X 475.0 / 1900.0	r147	25.0
94H	1	0	0	1	0	1	0	0	V_{148}''	$V_{12}+(V_{11}-V_{12})$ X 500.0 / 1900.0	r148	25.0
95H	1	0	0	1	0	1	0	1	V_{149}''	$V_{12}+(V_{11}-V_{12})$ X 525.0 / 1900.0	r149	25.0
96H	1	0	0	1	0	1	1	0	V_{150}''	$V_{12}+(V_{11}-V_{12})$ X 550.0 / 1900.0	r150	25.0
97H	1	0	0	1	0	1	1	1	V_{151}''	$V_{12}+(V_{11}-V_{12})$ X 575.0 / 1900.0	r151	25.0
98H	1	0	0	1	1	0	0	0	V_{152}''	$V_{12}+(V_{11}-V_{12})$ X 600.0 / 1900.0	r152	27.5
99H	1	0	0	1	1	0	0	1	V_{153}''	$V_{12}+(V_{11}-V_{12})$ X 627.5 / 1900.0	r153	27.5
9AH	1	0	0	1	1	0	1	0	V_{154}''	$V_{12}+(V_{11}-V_{12})$ X 655.0 / 1900.0	r154	27.5
9BH	1	0	0	1	1	0	1	1	V_{155}''	$V_{12}+(V_{11}-V_{12})$ X 682.5 / 1900.0	r155	27.5
9CH	1	0	0	1	1	1	0	0	V_{156}''	$V_{12}+(V_{11}-V_{12})$ X 710.0 / 1900.0	r156	27.5
9DH	1	0	0	1	1	1	0	1	V_{157}''	$V_{12}+(V_{11}-V_{12})$ X 737.5 / 1900.0	r157	27.5
9EH	1	0	0	1	1	1	1	0	V_{158}''	$V_{12}+(V_{11}-V_{12})$ X 765.0 / 1900.0	r158	27.5
9FH	1	0	0	1	1	1	1	1	V_{159}''	$V_{12}+(V_{11}-V_{12})$ X 792.5 / 1900.0	r159	27.5
A0H	1	0	1	0	0	0	0	0	V_{160}''	$V_{12}+(V_{11}-V_{12})$ X 820.0 / 1900.0	r160	30.0
A1H	1	0	1	0	0	0	0	1	V_{161}''	$V_{12}+(V_{11}-V_{12})$ X 850.0 / 1900.0	r161	30.0
A2H	1	0	1	0	0	0	1	0	V_{162}''	$V_{12}+(V_{11}-V_{12})$ X 880.0 / 1900.0	r162	30.0
A3H	1	0	1	0	0	0	1	1	V_{163}''	$V_{12}+(V_{11}-V_{12})$ X 910.0 / 1900.0	r163	30.0
A4H	1	0	1	0	0	1	0	0	V_{164}''	$V_{12}+(V_{11}-V_{12})$ X 940.0 / 1900.0	r164	30.0
A5H	1	0	1	0	0	1	0	1	V_{165}''	$V_{12}+(V_{11}-V_{12})$ X 970.0 / 1900.0	r165	30.0
A6H	1	0	1	0	0	1	1	0	V_{166}''	$V_{12}+(V_{11}-V_{12})$ X 1000.0 / 1900.0	r166	30.0
A7H	1	0	1	0	0	1	1	1	V_{167}''	$V_{12}+(V_{11}-V_{12})$ X 1030.0 / 1900.0	r167	30.0
A8H	1	0	1	0	1	0	0	0	V_{168}''	$V_{12}+(V_{11}-V_{12})$ X 1060.0 / 1900.0	r168	32.5
A9H	1	0	1	0	1	0	0	1	V_{169}''	$V_{12}+(V_{11}-V_{12})$ X 1092.5 / 1900.0	r169	32.5
AAH	1	0	1	0	1	0	1	0	V_{170}''	$V_{12}+(V_{11}-V_{12})$ X 1125.0 / 1900.0	r170	32.5
ABH	1	0	1	0	1	0	1	1	V_{171}''	$V_{12}+(V_{11}-V_{12})$ X 1157.5 / 1900.0	r171	32.5
ACH	1	0	1	0	1	1	0	0	V_{172}''	$V_{12}+(V_{11}-V_{12})$ X 1190.0 / 1900.0	r172	32.5
ADH	1	0	1	0	1	1	0	1	V_{173}''	$V_{12}+(V_{11}-V_{12})$ X 1222.5 / 1900.0	r173	32.5
AEH	1	0	1	0	1	1	1	0	V_{174}''	$V_{12}+(V_{11}-V_{12})$ X 1255.0 / 1900.0	r174	32.5
AFH	1	0	1	0	1	1	1	1	V_{175}''	$V_{12}+(V_{11}-V_{12})$ X 1287.5 / 1900.0	r175	32.5
B0H	1	0	1	1	0	0	0	0	V_{176}''	$V_{12}+(V_{11}-V_{12})$ X 1320.0 / 1900.0	r176	35.0
B1H	1	0	1	1	0	0	0	1	V_{177}''	$V_{12}+(V_{11}-V_{12})$ X 1355.0 / 1900.0	r177	35.0
B2H	1	0	1	1	0	0	1	0	V_{178}''	$V_{12}+(V_{11}-V_{12})$ X 1390.0 / 1900.0	r178	35.0
B3H	1	0	1	1	0	0	1	1	V_{179}''	$V_{12}+(V_{11}-V_{12})$ X 1425.0 / 1900.0	r179	35.0
B4H	1	0	1	1	0	1	0	0	V_{180}''	$V_{12}+(V_{11}-V_{12})$ X 1460.0 / 1900.0	r180	35.0
B5H	1	0	1	1	0	1	0	1	V_{181}''	$V_{12}+(V_{11}-V_{12})$ X 1495.0 / 1900.0	r181	35.0
B6H	1	0	1	1	0	1	1	0	V_{182}''	$V_{12}+(V_{11}-V_{12})$ X 1530.0 / 1900.0	r182	35.0
B7H	1	0	1	1	0	1	1	1	V_{183}''	$V_{12}+(V_{11}-V_{12})$ X 1565.0 / 1900.0	r183	35.0
B8H	1	0	1	1	1	0	0	0	V_{184}''	$V_{12}+(V_{11}-V_{12})$ X 1600.0 / 1900.0	r184	37.5
B9H	1	0	1	1	1	0	0	1	V_{185}''	$V_{12}+(V_{11}-V_{12})$ X 1637.5 / 1900.0	r185	37.5
BAH	1	0	1	1	1	0	1	0	V_{186}''	$V_{12}+(V_{11}-V_{12})$ X 1675.0 / 1900.0	r186	37.5
BBH	1	0	1	1	1	0	1	1	V_{187}''	$V_{12}+(V_{11}-V_{12})$ X 1712.5 / 1900.0	r187	37.5
BCH	1	0	1	1	1	1	0	0	V_{188}''	$V_{12}+(V_{11}-V_{12})$ X 1750.0 / 1900.0	r188	37.5
BDH	1	0	1	1	1	1	0	1	V_{189}''	$V_{12}+(V_{11}-V_{12})$ X 1787.5 / 1900.0	r189	37.5
BEH	1	0	1	1	1	1	1	0	V_{190}''	$V_{12}+(V_{11}-V_{12})$ X 1825.0 / 1900.0	r190	37.5
BFH	1	0	1	1	1	1	1	1	V_{191}''	$V_{12}+(V_{11}-V_{12})$ X 1862.5 / 1900.0	r191	37.5

Caution There is no connection between V_7 and V_8 in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (4/4)

$0.5\ V_{DD2} - 0.3\ V > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.2\ V$, POL21/22 = L



Data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
C0H	1	1	0	0	0	0	0	0	V_{192}"	V_{11}	r192	42.5
C1H	1	1	0	0	0	0	0	1	V_{193}"	$V_{11}+(V_{10}-V_{11})$ X 42.5 / 1600.0	r193	42.5
C2H	1	1	0	0	0	0	1	0	V_{194}"	$V_{11}+(V_{10}-V_{11})$ X 85.0 / 1600.0	r194	42.5
C3H	1	1	0	0	0	0	1	1	V_{195}"	$V_{11}+(V_{10}-V_{11})$ X 127.5 / 1600.0	r195	42.5
C4H	1	1	0	0	0	1	0	0	V_{196}"	$V_{11}+(V_{10}-V_{11})$ X 170.0 / 1600.0	r196	42.5
C5H	1	1	0	0	0	1	0	1	V_{197}"	$V_{11}+(V_{10}-V_{11})$ X 212.5 / 1600.0	r197	42.5
C6H	1	1	0	0	0	1	1	0	V_{198}"	$V_{11}+(V_{10}-V_{11})$ X 255.0 / 1600.0	r198	42.5
C7H	1	1	0	0	0	1	1	1	V_{199}"	$V_{11}+(V_{10}-V_{11})$ X 297.5 / 1600.0	r199	42.5
C8H	1	1	0	0	1	0	0	0	V_{200}"	$V_{11}+(V_{10}-V_{11})$ X 340.0 / 1600.0	r200	47.5
C9H	1	1	0	0	1	0	0	1	V_{201}"	$V_{11}+(V_{10}-V_{11})$ X 387.5 / 1600.0	r201	47.5
CAH	1	1	0	0	1	0	1	0	V_{202}"	$V_{11}+(V_{10}-V_{11})$ X 435.0 / 1600.0	r202	47.5
CBH	1	1	0	0	1	0	1	1	V_{203}"	$V_{11}+(V_{10}-V_{11})$ X 482.5 / 1600.0	r203	47.5
CCH	1	1	0	0	1	1	0	0	V_{204}"	$V_{11}+(V_{10}-V_{11})$ X 530.0 / 1600.0	r204	47.5
CDH	1	1	0	0	1	1	0	1	V_{205}"	$V_{11}+(V_{10}-V_{11})$ X 577.5 / 1600.0	r205	47.5
CEH	1	1	0	0	1	1	1	0	V_{206}"	$V_{11}+(V_{10}-V_{11})$ X 625.0 / 1600.0	r206	47.5
CFH	1	1	0	0	1	1	1	1	V_{207}"	$V_{11}+(V_{10}-V_{11})$ X 672.5 / 1600.0	r207	47.5
D0H	1	1	0	1	0	0	0	0	V_{208}"	$V_{11}+(V_{10}-V_{11})$ X 720.0 / 1600.0	r208	52.5
D1H	1	1	0	1	0	0	0	1	V_{209}"	$V_{11}+(V_{10}-V_{11})$ X 772.5 / 1600.0	r209	52.5
D2H	1	1	0	1	0	0	1	0	V_{210}"	$V_{11}+(V_{10}-V_{11})$ X 825.0 / 1600.0	r210	52.5
D3H	1	1	0	1	0	0	1	1	V_{211}"	$V_{11}+(V_{10}-V_{11})$ X 877.5 / 1600.0	r211	52.5
D4H	1	1	0	1	0	1	0	0	V_{212}"	$V_{11}+(V_{10}-V_{11})$ X 930.0 / 1600.0	r212	52.5
D5H	1	1	0	1	0	1	0	1	V_{213}"	$V_{11}+(V_{10}-V_{11})$ X 982.5 / 1600.0	r213	52.5
D6H	1	1	0	1	0	1	1	0	V_{214}"	$V_{11}+(V_{10}-V_{11})$ X 1035.0 / 1600.0	r214	52.5
D7H	1	1	0	1	0	1	1	1	V_{215}"	$V_{11}+(V_{10}-V_{11})$ X 1087.5 / 1600.0	r215	52.5
D8H	1	1	0	1	1	0	0	0	V_{216}"	$V_{11}+(V_{10}-V_{11})$ X 1140.0 / 1600.0	r216	57.5
D9H	1	1	0	1	1	0	0	1	V_{217}"	$V_{11}+(V_{10}-V_{11})$ X 1197.5 / 1600.0	r217	57.5
DAH	1	1	0	1	1	0	1	0	V_{218}"	$V_{11}+(V_{10}-V_{11})$ X 1255.0 / 1600.0	r218	57.5
DBH	1	1	0	1	1	0	1	1	V_{219}"	$V_{11}+(V_{10}-V_{11})$ X 1312.5 / 1600.0	r219	57.5
DCH	1	1	0	1	1	1	0	0	V_{220}"	$V_{11}+(V_{10}-V_{11})$ X 1370.0 / 1600.0	r220	57.5
DDH	1	1	0	1	1	1	0	1	V_{221}"	$V_{11}+(V_{10}-V_{11})$ X 1427.5 / 1600.0	r221	57.5
DEH	1	1	0	1	1	1	1	0	V_{222}"	$V_{11}+(V_{10}-V_{11})$ X 1485.0 / 1600.0	r222	57.5
DFH	1	1	0	1	1	1	1	1	V_{223}"	$V_{11}+(V_{10}-V_{11})$ X 1542.5 / 1600.0	r223	57.5
E0H	1	1	1	0	0	0	0	0	V_{224}"	V_{10}	r224	57.5
E1H	1	1	1	0	0	0	0	1	V_{225}"	$V_{10}+(V_9-V_{10})$ X 57.5 / 4687.5	r225	70.0
E2H	1	1	1	0	0	0	1	0	V_{226}"	$V_{10}+(V_9-V_{10})$ X 127.5 / 4687.5	r226	70.0
E3H	1	1	1	0	0	0	1	1	V_{227}"	$V_{10}+(V_9-V_{10})$ X 197.5 / 4687.5	r227	70.0
E4H	1	1	1	0	0	1	0	0	V_{228}"	$V_{10}+(V_9-V_{10})$ X 267.5 / 4687.5	r228	82.5
E5H	1	1	1	0	0	1	0	1	V_{229}"	$V_{10}+(V_9-V_{10})$ X 350.0 / 4687.5	r229	82.5
E6H	1	1	1	0	0	1	1	0	V_{230}"	$V_{10}+(V_9-V_{10})$ X 432.5 / 4687.5	r230	82.5
E7H	1	1	1	0	0	1	1	1	V_{231}"	$V_{10}+(V_9-V_{10})$ X 515.0 / 4687.5	r231	95.0
E8H	1	1	1	0	1	0	0	0	V_{232}"	$V_{10}+(V_9-V_{10})$ X 610.0 / 4687.5	r232	95.0
E9H	1	1	1	0	1	0	0	1	V_{233}"	$V_{10}+(V_9-V_{10})$ X 705.0 / 4687.5	r233	95.0
EAH	1	1	1	0	1	0	1	0	V_{234}"	$V_{10}+(V_9-V_{10})$ X 800.0 / 4687.5	r234	112.5
EBH	1	1	1	0	1	0	1	1	V_{235}"	$V_{10}+(V_9-V_{10})$ X 912.5 / 4687.5	r235	112.5
ECH	1	1	1	0	1	1	0	0	V_{236}"	$V_{10}+(V_9-V_{10})$ X 1025.0 / 4687.5	r236	112.5
EDH	1	1	1	0	1	1	0	1	V_{237}"	$V_{10}+(V_9-V_{10})$ X 1137.5 / 4687.5	r237	130.0
EEH	1	1	1	0	1	1	1	0	V_{238}"	$V_{10}+(V_9-V_{10})$ X 1267.5 / 4687.5	r238	130.0
EFH	1	1	1	0	1	1	1	1	V_{239}"	$V_{10}+(V_9-V_{10})$ X 1397.5 / 4687.5	r239	147.5
F0H	1	1	1	1	0	0	0	0	V_{240}"	$V_{10}+(V_9-V_{10})$ X 1545.0 / 4687.5	r240	147.5
F1H	1	1	1	1	0	0	0	1	V_{241}"	$V_{10}+(V_9-V_{10})$ X 1692.5 / 4687.5	r241	165.0
F2H	1	1	1	1	0	0	1	0	V_{242}"	$V_{10}+(V_9-V_{10})$ X 1857.5 / 4687.5	r242	165.0
F3H	1	1	1	1	0	0	1	1	V_{243}"	$V_{10}+(V_9-V_{10})$ X 2022.5 / 4687.5	r243	182.5
F4H	1	1	1	1	0	1	0	0	V_{244}"	$V_{10}+(V_9-V_{10})$ X 2205.0 / 4687.5	r244	182.5
F5H	1	1	1	1	0	1	0	1	V_{245}"	$V_{10}+(V_9-V_{10})$ X 2387.5 / 4687.5	r245	200.0
F6H	1	1	1	1	0	1	1	0	V_{246}"	$V_{10}+(V_9-V_{10})$ X 2587.5 / 4687.5	r246	200.0
F7H	1	1	1	1	0	1	1	1	V_{247}"	$V_{10}+(V_9-V_{10})$ X 2787.5 / 4687.5	r247	225.0
F8H	1	1	1	1	1	0	0	0	V_{248}"	$V_{10}+(V_9-V_{10})$ X 3012.5 / 4687.5	r248	225.0
F9H	1	1	1	1	1	0	0	1	V_{249}"	$V_{10}+(V_9-V_{10})$ X 3237.5 / 4687.5	r249	250.0
FAH	1	1	1	1	1	0	1	0	V_{250}"	$V_{10}+(V_9-V_{10})$ X 3487.5 / 4687.5	r250	250.0
FBH	1	1	1	1	1	0	1	1	V_{251}"	$V_{10}+(V_9-V_{10})$ X 3737.5 / 4687.5	r251	300.0
FCH	1	1	1	1	1	1	0	0	V_{252}"	$V_{10}+(V_9-V_{10})$ X 4037.5 / 4687.5	r252	300.0
FDH	1	1	1	1	1	1	0	1	V_{253}"	$V_{10}+(V_9-V_{10})$ X 4337.5 / 4687.5	r253	350.0
FEH	1	1	1	1	1	1	1	0	V_{254}"	V_9	r254	350.0
FFH	1	1	1	1	1	1	1	1	V_{255}"	V_8	TOTAL	15002.5

Caution There is no connection between V_7 and V_8 in the chip.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 8 bits x 2 RGBs (6 dots)

Input width : 48 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	···	D_{40} to D_{47}	D_{50} to D_{57}

(2) R,/L = L (Left shift)

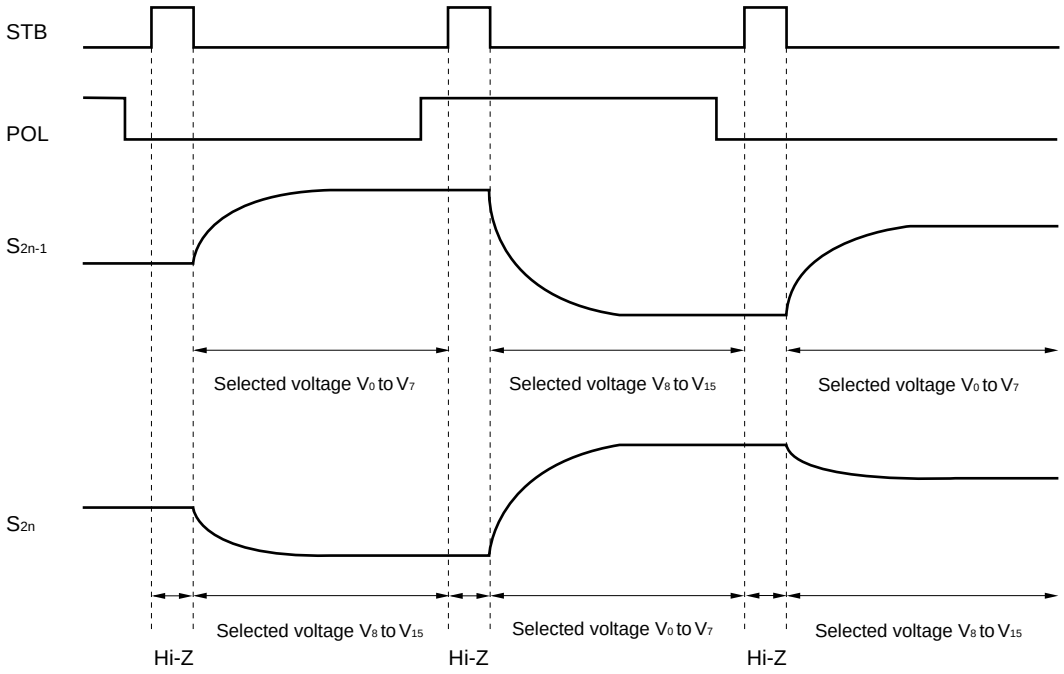
Output	S_1	S_2	S3	S4	···	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	···	D_{40} to D_{47}	D_{50} to D_{57}

POL	S_{2n-1} **Note**	S_{2n} **Note**
L	V_0 to V_7	V_8 to V_{15}
H	V_8 to V_{15}	V_0 to V_7

Note S_{2n-1} (Odd output), S_{2n} (Even output)

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	8.5	9.0	9.5	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_7	0.5 V_{DD2}		V_{DD2} – 0.2	V
	V_8 to V_{15}	V_{SS2} + 0.2		0.5 V_{DD2} – 0.3	V
Driver Part Output Voltage	V_O	V_{SS2} + 0.2		V_{DD2} – 0.2	V
Clock Frequency	f_{CLK}			40	MHz

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 9.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}				±0.1	±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1} – 0.1		V_{DD1}	V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA		0		0.1	V
γ-Corrected Supply Current	I_γ	V_0 to V_7 = V_8 to V_{15} = 4.0 V	V_0 pin, V_8 pin	225	450	900	μA
			V_7 pin, V_{15} pin	–900	–450	–225	μA
Driver Output Current	I_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V Note			–185	–90	μA
	I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V Note		120	238		μA
Output Voltage Deviation	ΔV_O	V_O = 0.2 V to 1.2 V V_O = V_{DD2} – 1.2 V to V_{DD2} – 0.2 V			±30	±50	mV
		V_O = 1.2 V to 0.5 V_{DD2} – 0.3 V V_O = 0.5 V_{DD2} to V_{DD2} – 1.2 V			±10	±20	mV
Output Swing Difference Deviation	ΔV_{P-P}	V_O = 0.2 V to 0.8 V V_O = V_{DD2} – 0.8 V to V_{DD2} – 0.2 V			±20	±40	mV
		V_O = 0.8 V to 1.2 V V_O = V_{DD2} – 1.2 V to V_{DD2} – 0.8 V			±10	±20	mV
		V_O = 1.2 V to 0.5 V_{DD2} – 0.3 V V_O = 0.5 V_{DD2} to V_{DD2} – 1.2 V			±3	±10	mV
Output Swing Average Difference Deviation	AV_O	V_{DD2} = 8.5 V, V_0 = 7.9 V, V_3 = 6.22 V, V_7 = 4.0 V, V_8 = 4.0 V, V_{12} = 1.78 V, V_{12} = 0.1 V, V_1, V_2, V_4, V_5, V_6, V_9, V_{10}, V_{11}, V_{13}, V_{14} : Open, T_A = 25°C, Input data: 80 H		4.433	4.440	4.447	V
Output Voltage Range	V_O			0.2		V_{DD2} – 0.2	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}, with no load			0.8	6.0	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2}, with no load			4.5	11.0	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{384}.

V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Cautions 1. The STB cycle is defined to be 20 μs at $f_{CLK.}$ = 40 MHz.

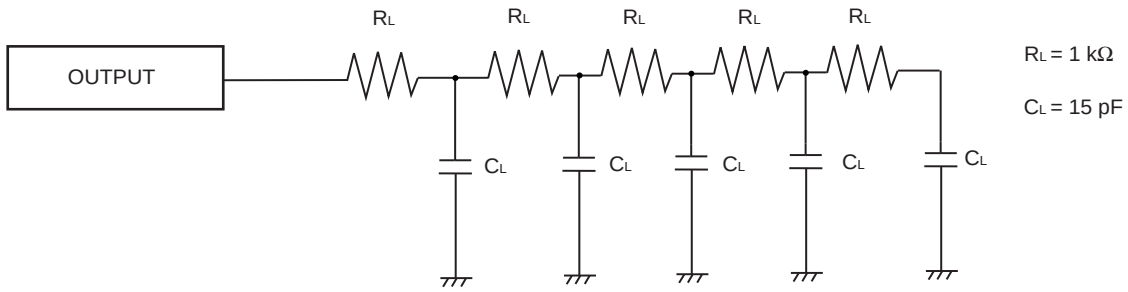
2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 9.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF		8	20	ns
Driver Output Delay Time	t_{PLH2}	C_L = 75 pF, R_L = 5 kΩ		3	6	μs
	t_{PLH3}			4	8	μs
	t_{PHL2}			3	6	μs
	t_{PHL3}			4	8	μs
Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = 25°C		4.8	10	pF
	C_{I2}	STHR (STHL),T_A = 25°C		8.6	15	pF

<Measurement Condition>



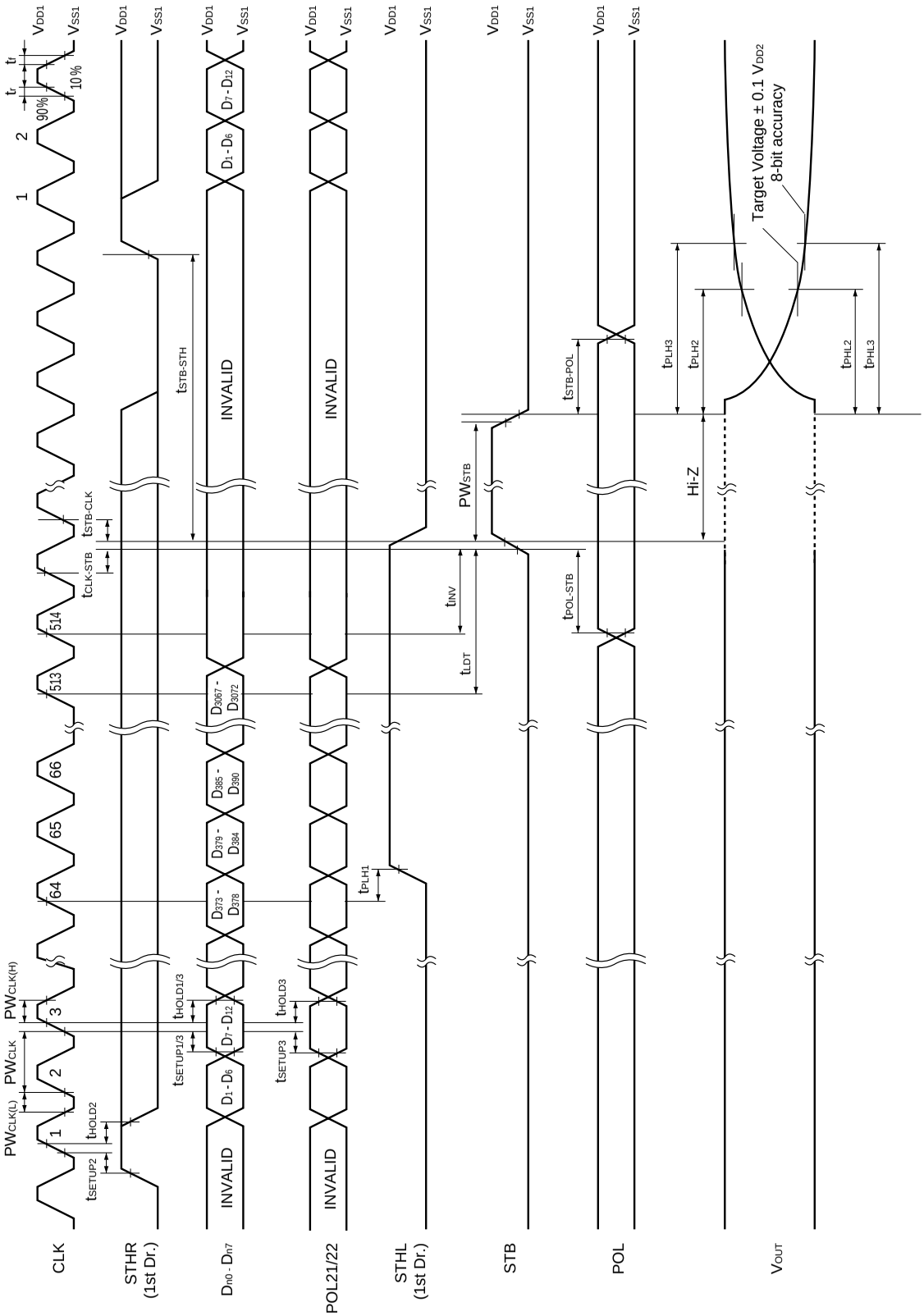
Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 3.3 V ± 0.3 V, V_{SS1} = 0 V, $t_r = t_f$ = 8.0 ns)

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	Clock Pulse Width	PW_{CLK}		25			ns
	Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
	Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
	Data Setup Time	t_{SETUP1}		2			ns
	Data Hold Time	t_{HOLD1}		2			ns
	Start Pulse Setup Time	t_{SETUP2}		2			ns
	Start Pulse Hold Time	t_{HOLD2}		2			ns
★	POL21/22 Setup Time	t_{SETUP3}		2			ns
★	POL21/22 Hold Time	t_{HOLD3}		2			ns
	Start Pulse Low Period	t_{SPL}		1			CLK
	STB Pulse Width	PW_{STB}		2			μs
	Data Invalid Period	t_{INV}		1			CLK
	Last Data Timing	t_{LDT}		2			CLK
	CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	6			ns
	STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	6			ns
	Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
	POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
	STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

9. SWITCHING CHARACTERISTIC WAVEFORM (R,/L= H)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



Phase-out/Discontinued

10. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16750.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16750N-xxx : TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C : pressure 3 to 8 kg/cm^2: time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2: time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)

M7 98.8